The evolution of low defect density structures in silicon-on-sapphire thin films during post-ion implantation heat treatments

Author/Contributor:
McKenzie, Warren Richard; Domyo, Hiroshi; Ho, Tran; Munroe, Paul

Publication details:
Microscopy of Semiconducting Materials Microscopy of Semiconducting Materials, Proceedings of the 14th Conference
pp. 328-329
978-3-540-31914-6 (ISBN)
0930-8989 (ISSN)

Event details:
Microscopy of Semiconducting Materials
Oxford, UK

Publication Date:
2005

Publisher DOI:
http://dx.doi.org/10.1007/3-540-31915-8_78

The evolution of low defect density structures in silicon-on-sapphire thin films during post-ion implantation heat treatments

W R McKenzie[1], H Domyo[2], T Ho[2], P R Munroe[1]

[1]School of Materials Science and Engineering, University of New South Wales, SYDNEY, NSW 2052, Australia
[2]Peregrine Semiconductor Australia Pty Ltd, HOMEBUSH, NSW 2140 Australia

ABSTRACT: (100) silicon thin films grown on $(1\bar{1}02)$ sapphire substrates is the most significant of the silicon-on-insulator technologies and has been used for many years in the production of integrated circuits. This paper presents a TEM study of the evolution of crystalline defects during the heat treatments designed to improve the quality of the films. Planar defects were found to be isolated to the outer surface of the films, whilst dislocations were abundant throughout. Defect density was considerably reduced by annealing at higher temperatures.

1. INTRODUCTION

Silicon-on-insulator technologies offer many advantages over conventional bulk silicon in the performance of integrated circuits (IC's). Silicon-on-sapphire (SOS) is the most mature and significant of these technologies and is currently being used in the production of high density IC's.

The crystalline defects in (100) silicon films on $(1\bar{1}02)$ sapphire substrates, grown by chemical vapour deposition (CVD), include planar defects lying parallel to {111} silicon planes, domain mis-orientation and misfit dislocations running approximately perpendicular to the sapphire interface.

Planar defects are believed to form as a result of stress in the film from a lattice mismatch between the silicon and sapphire (Ponce 1982). Domain mis-orientation dislocations, formed at the boundaries of (100) silicon domains, have been identified to form in the early stages of CVD processing (Abrahams et al 1976). Misfit dislocations are thought to form at the sapphire interface as a result of a lattice mismatch between the silicon and substrate (Ponce 1982). The lack of misfit dislocations has been speculated in many studies to be a result of an incoherent interface formed due to the high degree of freedom of Si-O bonds at the sapphire interface (Ponce 1982).

In the quest to make transistors smaller, faster and use less power, many advances have been made to the manufacture of SOS films in order to reduce the number of crystalline defects. The most important improvement made to as-grown SOS films was initially described by Lau et al (1979). This "improvement" process involves firing energetic silicon ions at the CVD silicon film to produce an amorphous layer to all but the outer surface of the silicon. The film is annealed to allow solid phase epitaxial regrowth from this remaining crystalline seed back towards the sapphire interface at ~550^{o}C. Once the re-crystallisation is complete a higher temperature treatment is used to anneal out most remaining unstable defects (above 900^{o}C) leaving a film with a very low defect density.

It has been reported that the density of dislocations is not noticeably affected by the ion implantation and regrowth anneal (Carey et al 1983). The most important improvement to the films quality is in the reduction in the number of planar defects. This has been predicted to be from overgrowth since the (100) silicon grows ~10 times faster than the {221} material in the planar defects, during regrowth at 550^{o}C (Amano and Carey 1981).

This paper takes a closer look at the improvement process by analysing samples at various stages of the ~550^{o}C regrowth anneal to investigate their defect structure using transmission electron microscopy (TEM). The aim of this work is to identify the source and methods of termination of the remaining defects in order to further improve the quality of the films.

2. EXPERIMENTAL PROCEDURE

Silicon on sapphire films were prepared by Peregrine Semiconductor Australia Pty Ltd. The process to fabricate the films, described by Amano and Carey (1981), was followed up until the first annealing stage. The specimens were heated in a nitrogen atmosphere to 550^{o}C at a rate of approximatly 30^{o}C/min. Samples were produced corresponding to annealing times of 0, 30 and 60 minutes at this temperature before being air-cooled. Other SOS specimens were examined including a CVD only film, a post ion implantation, and a fully processed (~550^{o}C and >900^{o}C anneals) film.

For each sample a cross-sectional TEM specimen was prepared using an FEI Nova 200 Nanolab focussed ion beam (FIB) instrument. This was done by way of the "lift-out" technique, details of which are given by Giannuzzi and Stevie (1997). This process involves milling and detaching a TEM foil from the bulk with the FIB then transferring the foil to a carbon coated copper TEM grid using a micromanipulator. TEM samples were analysed with a 200kV Philips CM-200 TEM using a double tilt holder. For the specimen annealed at 550^{o}C, specimens were imaged using diffraction conditions to generate contrast from either the twins or the dislocations.

3. RESULTS AND DISCUSSION

Figures 1A shows the as-grown CVD silicon film with planar defects, parallel to {111} planes, it can be seen that they have a higher density closer to the sapphire-silicon interface. Figure 1B shows the structure following ion implantation, the region adjacent to the sapphire has become amorphous (a-Si), but the region furthest from that interface remains crystalline (c-Si), although heavily damaged. Figure 1C shows the remaining crystalline region that acts as a seed during re-growth, at an orientation that highlights the presence of residual planar defects in this area.

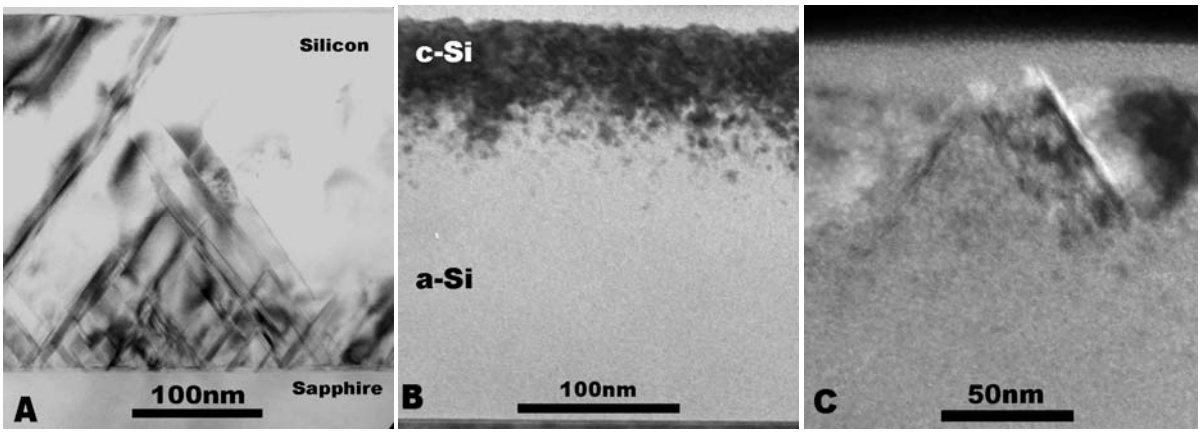

Figure 1: Bright field TEM images of A) As-deposited CVD silicon showing the twin structure. B) the silicon film after the ion implant showing the crystalline (c-Si) and amorphous (a-Si) regions. C) The c-Si region shown in B tilted to diffraction conditions to highlight the presence of planar defects.

The re-growth of the crystalline silicon during post-implantation annealing can be seen in Figure 2. The time each specimen was held at 550^{o}C is indicated. For the 0 minute anneal (i.e. air-cooled immediately once 550^{o}C is reached), approximately 2/3 of the silicon film is seen to have re-crystallised with the boundary between the a-Si and c-Si moving as an interface towards the sapphire in a non-uniform manner. Presumably, this regowth occurred during the heating cycle to 550^{o}C. At this point the planar defects appear to have almost completely regrown with the (100) Si, but have been terminated very close to this interface. After 30 minutes most of the crystalline silicon has re-grown except for an isolated patch of a-Si remaining at the sapphire interface. It is only after 60 minutes that all the a-Si has re-crystallised. It can be seen that the faults have not extended whilst the specimen is held at 550^{o}C. These results suggest that the re-crystallisation grows both (100) and {221} silicon at equal rates during heating to 550^{o}C, where most re-crystallisation takes place. It is only at a temperature of 550^{o}C where the (100) silicon finally overgrows the {221} material, so that the planar faults are terminated.

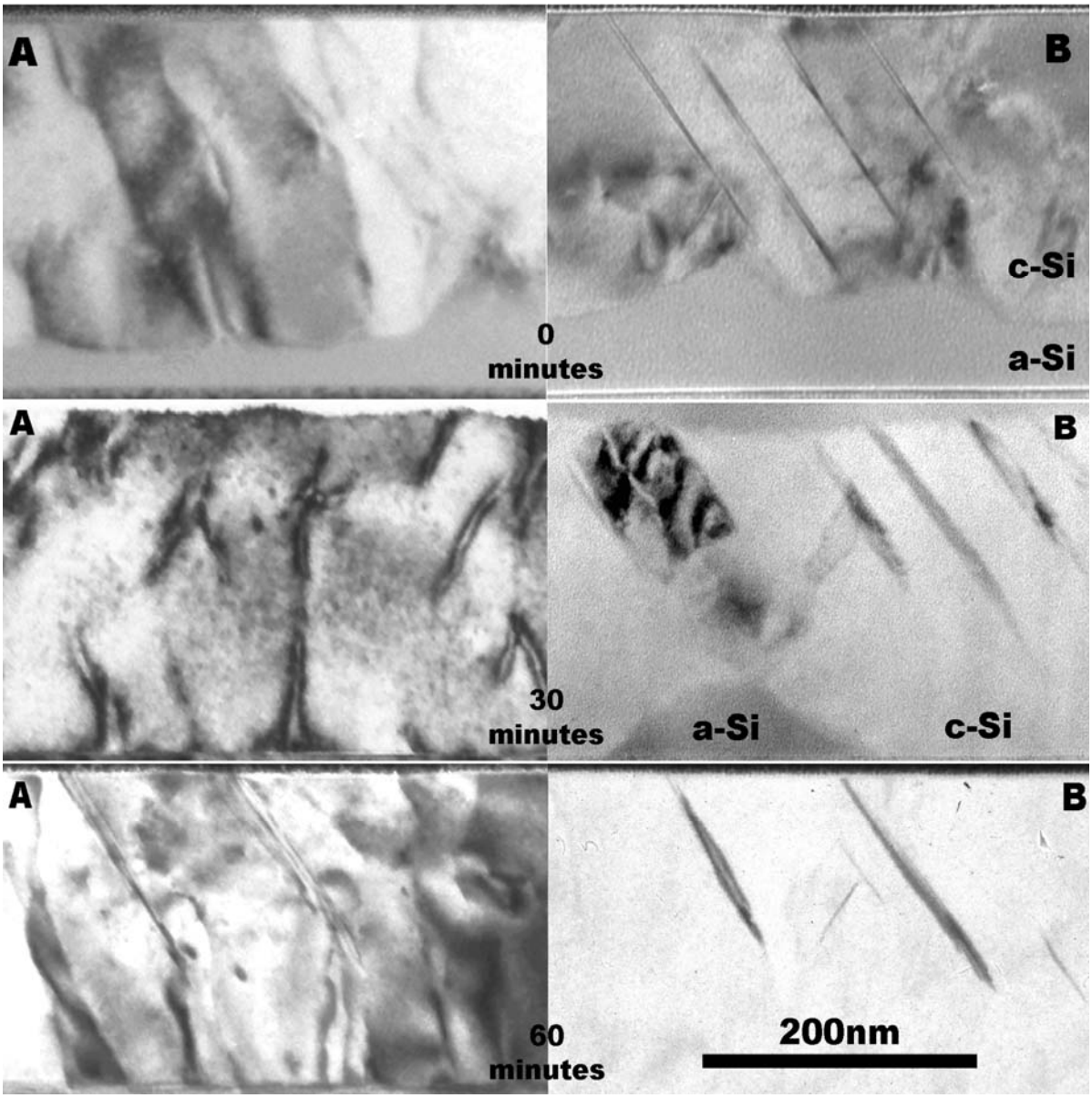

Figure 2: Bright field TEM images taken with a beam orientation parallel to: A {200} plane to highlight dislocations, labeled "A", and a {111} plane to highlight planar faults, labeled "B". Annealing times for each sample at 550°C are indicated. All samples are of the same magnification.

Images in Figure 2 labelled A were taken at orientations to emphasise dislocation contrast. They show the evolution of dislocations as a function of the re-growth of the crystalline silicon at this temperature. For the 0 minute sample dislocations appear as boundaries to areas of differing contrast indicating regions of slightly different crystallographic orientation. This suggests that these defects are domain mis-orientation dislocations. For the 30 and 60 minute anneal samples, dislocations, typically spaced 50-100nm apart, extend in an approximately perpendicular direction from the silicon-sapphire interface up towards the free surface. It is likely such defects are associated with the lattice misfit between the silicon and sapphire. These form to accommodate the lattice strains generated as the crystalline silicon approaches the sapphire.

After the final anneal above 900°C, seen in Figure 3, all dislocations appear to have been removed giving evidence supporting the theory that the flexibility of oxygen bonds at the interface accounts for some of the lattice mismatch previously forming the dislocations (Ponce 1982).

Prior to device processing, this outer silicon layer, containing most of the planar faults, is etched leaving a thinner film free of planar defects. Figure 3 shows this remaining layer in a film that has been subject to an additional heat treatment above 900°C. The remaining planar defect in this image is believed to be one of few extending through the entire film. The residual dislocation density is very low.

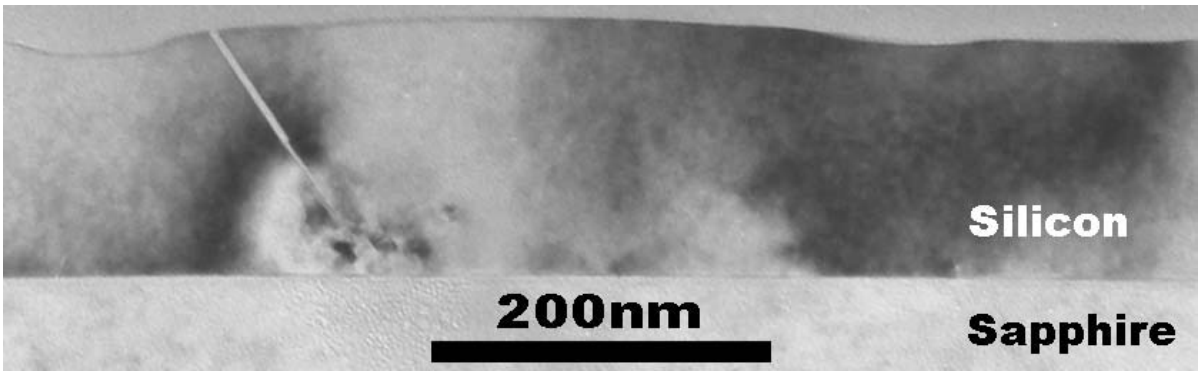

Figure 3: Bright field TEM image showing the silicon film structure after completion of the improvement process showing a single planar defect.

4. CONCLUSIONS

The re-crystallisation process and defect growth have been characterised as a function of annealing time for heat treatments carried out at 550°C as part of the improvement process used to reduce the defect density of silicon on sapphire thin films. The re-crystallisation proceeds, non-uniformly, as an interfacial movement from the seed crystal towards the silicon-sapphire interface. Most re-growth occurred during the heating cycle to 550°C. However, the film was only seen to become fully crystalline after holding for 60 minutes at this temperature.

Planar defects in the re-grown material originate from those remaining in the crystalline seed after the ion implant. These are seen to grow with the amorphous-crystalline interface towards the sapphire during heat-up, but their growth is limited by overgrowth of the (100) silicon once 550°C is reached.

Domain mis-orientation and lattice mismatch dislocations were present in the films processed at 550°C only. These appear to be removed during subsequent annealing above 900°C.

ACKNOWLEDGMENTS

The authors wish to thank the Australian Research Council for the provision of funding and Associate Professor Michael Ferry for useful discussions.

REFERENCES

Abrahams M S, Buiocchi C J, Smith R T, Corboy J F Jr., Blanc J and Cullen G W 1976 J. Appl. Phys. **47**(12), 5139

Amano J and Carey K 1981 Appl. Phys. Lett. **39**(2), 163

Carey K W, Ponce F A, Amano J and Aranovich J 1983 J. Appl. Phys. **54**(8) 4414

Giannuzzi L A, Stevie F A 1999 Micron **30,** 197

Lau S S, Matteson S, Mayer J W, Revesz P, Gyulai J, Roth J, Sigmon T W and Cass T 1979 Appl. Phys. Lett. **34**(1), 76

Ponce F A 1982 Appl. Phys. Lett. **41**(4), 371