A 5V charge pump in a standard 1.8V 0.18μm CMOS process

by

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Submitted to the School of Electrical Engineering and Telecommunications in partial fulfilment of the requirements for the degree of Master of Engineering at

The University of New South Wales 2005
CERTIFICATE OF ORIGINALITY

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I also declare that the intellectual content of this thesis is the product of my own work, except to the extent that assistance from others in the project's design and conception or in style, presentation and linguistic expression is acknowledged.

(Signed)
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Tawfique Hasan
Abstract

The steady but aggressive downscaling of semiconductor devices over the last few decades has been the most important stimulus to the unprecedented growth of Integrated Circuits. For better circuit performance and reliability, power supplies for newer CMOS generations have been scaled down disproportionately. However, in many state of art applications, some circuit components still need higher than the nominal supply voltage for proper operation. The function of charge pump circuits is to provide this higher voltage by stepping up the regular dc supply.

Even with scaled down supply voltages, ensuring reliability of current CMOS devices is a big challenge mainly because of their extremely small dimensions. Since charge pumps are used to produce higher than the nominal supply voltage, device reliability restrictions have forced designers to use high voltage tolerant CMOS devices instead of their standard low voltage counterparts in practical implementations of these circuits.

This work proposes a new charge pump topology which enables the usage of standard low voltage CMOS devices without violating any of the typical voltage stress reliability problems. The design is implemented in TSMC 1.8 V 0.18 μm 6 Metal CMOS process. The layout including auxiliary circuitry measures 600μm x 630μm. The proposed design steps up the output voltage to 5.12 V with a 250 kΩ load (with a 150 pF smoothing capacitor in parallel) at a clock frequency of 2.5 MHz. The efficiency of the fully integrated charge pump circuit itself is close to 77%. The design satisfies typical voltage stress related reliability requirements and is an attractive alternative to costlier conventional charge pumps for applications requiring low and moderate loads.
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#### 3VDD Charge pump specifications

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<td>Output voltage</td>
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<tr>
<td>Loading condition</td>
<td>250 kΩ (with 150 pF smoothing capacitor in parallel)</td>
</tr>
<tr>
<td>Output ripple voltage</td>
<td>≈50 mV</td>
</tr>
<tr>
<td>Circuit efficiency</td>
<td>77%</td>
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<td>Complete layout area</td>
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<td>Anode Hole Injection</td>
<td>AHI</td>
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<tr>
<td>Anode Hydrogen Release</td>
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<td>Capacitor Top Metal</td>
<td>CTM</td>
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<td>Charge Transfer Switch</td>
<td>CTS</td>
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<td>Channel Hot Carrier Injection</td>
<td>CHCI</td>
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<td>Drain Avalanche Hot Carrier Injection</td>
<td>DAHCI</td>
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<td>Fowler-Nordheim</td>
<td>FN</td>
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<td>High Voltage Tolerant</td>
<td>HVT</td>
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<td>Hot Carrier Injection</td>
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<tr>
<td>Lightly Doped Drain</td>
<td>LDD</td>
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<td>Metal Insulator Metal</td>
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<td>Smart Voltage eXtension</td>
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<td>Standard Low Voltage</td>
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<td>Stress Induced Leakage Current</td>
<td>SILC</td>
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<td>TDDB</td>
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<td>Quasi Breakdown</td>
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Chapter 1

Introduction

1.1 Background

During the last couple of decades, revolution in electronics has literally changed the way we live. Old ideas have been polished and improved significantly and new ideas and applications have emerged in almost every facets of our life. All of these have become possible due to aggressive scaling down of CMOS devices to achieve better performance in terms of silicon area, speed and power consumption. This scenario equally applies to both portable and non portable digital and analog electronic equipments. It is still thriving and will probably keep downscaling for many years to come.

To keep pace with the aggressive CMOS scaling and at the same time, to maintain a balance between circuit performance and reliability, power supplies for newer CMOS generations have been lowered disproportionately over the last few years. However, in almost all the electronic devices, some circuit parts and components need higher than the regular supply voltage to operate properly. Naturally, for portable systems, need for this higher voltage spells trouble. Charge pump circuits come to the rescue by stepping up the regular supply voltage though they introduce some additional problems, like
higher cost due to additional processing in incorporating specialized High Voltage Tolerant (HVT) CMOS devices.

Over the last few years, it has almost become a convention to use HVT CMOS devices for charge pumps to maintain an acceptable level of reliability, simply because the circuit deals with higher than the regular supply voltage. However, as expected, additional process steps are needed for HVT devices in addition to the Standard Low Voltage (SLV) CMOS process steps, hence, incurring additional cost. This area of electronics have not developed much mainly because of numerous physical limitations of SLV CMOS devices. However, if properly designed, after considering issues related to reliability and circuit performance, circuits with SLV CMOS devices can prove themselves as a cheaper and competitive alternative.

In this work, we have explored the possibility of designing a fully integrated charge pump in a standard 1.8 V 0.18 μm low voltage CMOS process without compromising the Voltage Stress Related (VSR) reliability issues. The proposed circuit produces an output voltage of 5.12 V with a 250 kΩ load resistor (with a 150 pF smoothing capacitor in parallel) at a clock frequency of 2.5 MHz. The efficiency of the charge pump alone is 77% with the abovementioned load. It satisfies all the basic VSR reliability requirements and offers a cheaper alternative than the conventional charge pumps designed with HVT CMOS devices.
1.2 Thesis overview

In this thesis, reliability issues of current CMOS generations are discussed in brief which is followed by a review of different circuit topologies of conventional charge pumps designed with HVT CMOS devices. Then the design issues and the newly developed circuit topology are discussed in detail. Finally, comparisons and simulation results are presented.

A brief introduction of the background of this work is presented in Chapter 1. This chapter also outlines the thesis contents.

A detailed discussion on VSR reliability and lifetime issues are presented in Chapter 2. This chapter ends with a typical design guideline for the proposed charge pump designed with an SLV CMOS process.

Chapter 3 concentrates on conventional charge pump structures designed with HVT CMOS devices. In this chapter, different structures starting from the very first voltage multiplier designed in 1930s to a number of modern charge pumps are discussed with their working principles summarized.

In Chapter 4, potential VSR reliability issues in a conventional NMOS cross-coupled symmetrical charge pump circuit are discussed. Then the basic design methodology of the proposed charge pump circuit is presented. Finally, the circuit structures of different blocks of the newly designed charge pump are discussed in detail.
Simulation results of different parts of the circuit and relevant analysis with regard to VSR reliability are presented in Chapter 5. Circuit performance and efficiency with different loading conditions and parameters are also included in this chapter.

Chapter 6 primarily deals with post layout simulation results. Layout design of Metal Insulator Metal (MIM) capacitors and post layout simulation results are presented in this chapter.

Finally, design limitations and avenues on future improvement conclude the thesis contents in Chapter 7.
Chapter 2

VSR reliability issues for current CMOS generations

2.1 Introduction

A clear understanding of the relationship between circuit lifetime and device stress has become increasingly important in newer CMOS generations. During the last few decades, debate on device reliability has shifted from a mere academic research interest into one of the biggest industry level concerns to guarantee the lifetime of submicron devices [1].

![Figure 2.1: Evolution of electric fields in oxide and silicon over the years [1].](image)

As the device dimensions and supply voltage get smaller in a bid to achieve better performance, reduced power and smaller die area, the maximum allowable voltage stresses in devices have to be reduced to ensure a reasonable lifetime [2], [3], [4]. However, with disproportionate scaled-down supply voltages, devices in newer CMOS generations have to cope with increasingly higher vertical and horizontal electric
field stresses in the gate dielectric and channel regions [5]. Fig. 2.1 gives a fair idea about the stresses that submicron devices have experienced over the years.

Reduced device dimensions especially gate oxide thickness, channel length and junction depth, increased substrate doping densities accompanied by disproportionate scaling of power supply voltage are the primary reasons for this significant increase in vertical and lateral electric fields in MOS transistors [5]. Of these two electric fields, the first causes Gate Oxide Breakdown (more commonly known as Time Dependent Dielectric Breakdown or TDDB) and the latter is primarily responsible for Hot Carrier Degradation. Besides, current submicron device designs are also restricted by another less commonly considered lifetime threatening mechanism, namely, Junction Breakdown which is caused by high electric fields across reverse biased junctions in MOS devices.

High electric field across the gate oxide may lead to generation of defects or charge traps. Charges trapped in these regions increase the local electric fields which, in turn, increase the tunneling current generating newer charge traps [6]. This cumulative effect severely degrades the gate oxide leading to eventual device failure.

Under the influence of high lateral electric field, carriers flowing from source to drain may gain sufficient energy between the edge of channel pinch-off region and drain diffusion area. These highly energized carriers or ‘Hot Carriers’ may gain sufficient energy to surmount the energy barrier at Si-SiO₂ interface and get injected into the gate oxide resulting in serious long term reliability problems especially near the drain regions [3], [7].
The third device related lifetime threatening mechanism is junction breakdown although in modern CMOS processes, this problem normally does not pose serious limitations to common High Voltage Tolerant (HVT) circuit designs with SLV devices. This is partly because of the fact that the junction breakdown voltages are typically a few times higher than the nominal supply voltage. Since these reliability issues arise from voltage stresses, they can be collectively called as Voltage Stress Related (VSR) reliability issues.

Therefore, designing High Voltage Tolerant (HVT) circuits with Standard Low Voltage (SLV) CMOS process must be accompanied by a good understanding of the physical mechanisms related to these VSR reliability issues to ensure sufficient device lifetime.

This chapter mainly focuses on details of VSR reliability issues and means of avoiding them by designing HVT circuits with SLV CMOS devices. Possible design restrictions imposed by these issues will also be explored. Finally, design guidelines for the proposed circuit topology conclude this chapter.

2.2 Time Dependent Dielectric Breakdown (TDDB)

TDDB has remained a primary battleground and a fertile research area among reliability engineers and researchers for decades. No unified model has been found which can successfully explain the mechanism behind the gate oxide breakdown of different oxide thickness and physical properties. However, it is widely accepted that the TDDB related device failure consists of two steps; gradual wear-out of the insulating properties followed by an eventual breakdown.
TDDB can occur at any gate voltage even at voltages lower than the one specified by foundry [6]. Electrons breaching the oxide potential barrier are accelerated through the oxide by electric field applied. At the end of travel through the oxide, these electrons deposit their energy at the SiO₂-Si interface. The interface is already strained because of the large mismatch of thermal coefficient of expansion between Si (2 ppm/°C) and SiO₂ (0.3 ppm/°C). Therefore, the electrons which tunnel through the oxide may break the bonds at the interface creating more charge traps. The interface trap generation rate has been found to be exponentially dependent on oxide electric field at room temperature [8]. Local tunneling current can be greatly influenced by these trapped charges creating more traps and thus, increasing the tunneling current leading to oxide breakdown.

Typically, a compromise between gate oxide thickness and operating voltage is made for successful device operation with optimized speed and lifetime target [6].

However, for ultra thin oxides in newer CMOS processes, Stress Induced Leakage Current (SILC) and Quasi Breakdown (QB) [9], [10] are thought to be the other reasons for oxide breakdown though their detailed physical mechanisms are not yet fully understood.

Tunneling mechanisms of electrons through the oxide potential barrier are discussed in the next two subsections.
2.2.1 Fowler-Nordheim (FN) tunneling

Historically, it has been considered that, the lifetime of gate oxide is dictated by the total amount of charge flowing though it. The oxide tunneling current is modeled by the FN equation [11]:

\[ J = AE^2 e^{\left(\frac{B}{E}\right)} \]  

(2.1)

where, \( J \) is the oxide tunneling current density, \( E \) is the electric field, \( A \) and \( B \) are two constants related to the electron’s effective mass in the oxide conduction band and Si-SiO₂ barrier heights.

This current originates from quantum-mechanical tunneling of electrons through the triangular shaped Si-SiO₂ potential barrier from the Si conduction band to the SiO₂ conduction band [1]. FN tunneling can be either steady state or ballistic depending upon oxide voltage and oxide thickness [12].

However, for current submicron technologies gate oxide leakage current does not follow FN equation. Instead, it is largely governed by direct tunneling mechanism [13].

2.2.2 Direct Tunneling

For an oxide voltage (\( V_{OX} \)) lower than the 3V Si-SiO₂ barrier height, the electron tunneling barrier changes from triangular to trapezoidal shape. In such situation, electrons can tunnel directly from cathode to anode without appearing in the oxide.
conduction band. The process is ballistic since the electrons do not scatter before they enter anode [12]. The direct tunneling current density cannot be described in a closed analytic form unlike FN tunneling [1]. However, they show strong dependence on the thickness of gate oxide [2].

Fig 2.2 compares between (a) FN tunneling and (b) direct tunneling. The average kinetic energy, $KE_{Si}$ of electrons entering the anode equals to $qV_{OX}$ before scattering occurs. The maximum energy delivered to anode is $qV_G$. Therefore, for modern SLV CMOS processes, direct tunneling is a major contributor to oxide leakage current.

2.2.3 Stress Induced Leakage Current (SILC)

For oxides with a thickness of less than 5nm, the other contributor to leakage current is SILC. Fig. 2.3 shows the SILC remains almost constant for thin oxides whereas, for thick oxides, it is relaxed with time [15]. Unlike FN or direct tunneling, SILC has been observed to be equally distributed to all over the gate oxide and therefore, is not a localized effect [10]. Hence, it is proportional to gate oxide area. SILC has been
reported to be accompanied with creation of interface traps [16] as well as bulk oxide neutral charge traps [17].

![SILC for different oxide thickness](image)

Figure 2.3: SILC for different oxide thickness. It is clearly seen that SILC is a transient phenomena for thick oxides whereas for thin oxides, it contributes to a constant leakage current [15].

### 2.2.4 Interface trap generation models; AHI and AHR

The interface trap generation mechanism due to gate oxide stress can primarily be modeled by the Anode Hole Injection (AHI) model described by Schuegraf et al. [18]. As indicated by AHI model, injection can occur at an oxide voltage of 6 volts or more. In this process, electrons entering the anode create electron hole pairs by impact ionization. The created holes are injected back into the oxide which acts as charge traps at the Si-SiO₂ interface as well as inside the bulk oxide. However, the original model cannot successfully describe trap generations at low voltages. A revised model [19] offers some explanation in this regard.
The other model is Anode Hydrogen Release (AHR). Hydrogen release occurs at an oxide voltage of 5 volts [20] which is strongly suggested to be one of the reasons of trap generation.

However, generation of charge traps has been observed at much lower voltages than suggested by AHI and AHR models [21] indicating that gradual degradation of oxide takes place at voltages lower than the thresholds for AHI and AHR. At voltages below the threshold, electrons dissipating the maximum energy at anode will be the most important factor for trap generation [12]. Contribution from SILC is also strongly believed to play a vital role [10]. For current deep submicron processes, this is the most likely scenario.

2.2.5 TDDB reliability requirement for the proposed design

However, as expected, all these models are heavily dependent on process induced defect contents, oxide properties as well as fabrication process steps. Therefore, it is not possible to use extracted parameters from one fabrication process to predict the lifetime of another. To make the matter worse, due to imperfect modeling of TDDB, an accurate prediction of gate oxide lifetime by extrapolation is not possible. Therefore, to be on the safe side, it is always best to stay within the boundary of the foundry specified operating voltage [6] which is set conservatively after extensive experiments on the particular process. For the proposed charge pump design with SLV CMOS devices, the allowable operating voltage is 1.8 volts which translates into around 4.5 MV/cm oxide stress.
2.3 Hot Carrier Injection (HCI)

Under the influence of the increased horizontal electric field that have been discussed earlier in this chapter, carriers flowing from source to drain may acquire high kinetic energy (or in other words, may become 'hot carriers') between the channel pinch off region and drain diffusion in a MOS transistor. If an electron in the channel have sufficient energy to overcome the SiO₂-Si barrier potential of 3.2 ev, it can be injected into the gate oxide. This mechanism is commonly known as Channel Hot Carrier Injection (CHCI). These accelerated carriers with high energy create electron-hole pairs by impact ionization with silicon lattices near the drain end of the channel. Again, these electron-hole pairs can be subjected to further impact ionization leading to an avalanche effect [22]. This mechanism is known as Drain Avalanche Hot Carrier Injection (DAHCI). The generated carriers give rise to hole (for NMOS) or electron (for PMOS) substrate current. Fig. 2.4 shows a schematic diagram illustrating these hot carrier injection mechanisms.

These injected carriers result in permanent changes in the oxide-interface charge distribution and thereby, permanently degrade the transconductance of MOS transistors.
Eventually carrier mobility decreases and the transistor threshold drifts away making it unable to create a channel [6].

However, it must be kept in mind that gate oxide stress can significantly influence the HCI process when the associated devices are in saturation. Experimental evidence also suggests that HCI degradation is closely intertwined with charge de-trapping and tunneling mechanisms [24]. Other hot carrier injection mechanisms can also degrade device characteristics [22]. Therefore, HCI related device failure depends on the extent of usage of the associated devices and extrapolated results cannot truly ensure device lifetime predictions.

2.3.1 Hot carrier degradation factors

It is widely accepted that HCI related damage is a far more common phenomenon in digital designs than its analog counterpart which is, in fact, only partially true. The reason for this belief is because of the fact that digital circuits are almost always designed with minimum channel lengths which have a direct impact in the significant increase in horizontal electric field in the channel region of MOS transistors. In digital circuits, HCI can introduce critical timing problems in different circuit blocks of a bigger system level design. In case of properly designed analog circuits, hot carrier degradation does not usually impose a big threat in the long run. However, transconductance of some devices in analog circuits might be extremely critical for its proper functionality. Some notable effects of HCI on analog circuit performance can be found in [24], [25], [26]. Therefore, for analog circuits, effect of HCI related circuit failure depends on individual devices rather than circuit blocks. HCI can be
significantly decreased by reducing the horizontal electric field i.e. increasing the width of individual devices which is typically accompanied by additional parasitics. For a fixed transistor length, the primary factor causing hot carrier degradation is obviously the drain to source voltage, $V_{DS}$.

However, some other factors also play a limited role in this degradation mechanism. For a particular process, the design parameters that can influence the HCI process include gate signal’s slope and ratio of transistor width and associated load capacitance [5].

### 2.3.2 HCI reliability requirement for the proposed design

Unlike TDDB there is no strict foundry specified design guideline for HCI reliability since it heavily depends on transistor width and device usage in a particular circuit. Again, in current CMOS generations, standard Lightly Doped Drain (LDD) structures on all SLV devices significantly reduce HCI related degradations. However, as a general guideline, the maximum allowable $V_{DS}$ is considered to be somewhat restricted within the operating voltage of 1.8 volts. Therefore, in the proposed design, $V_{DS}$ for all transistors have been kept under this limit. Again, to lessen the HCI effect, lengths of all the devices are made at least 2 times the minimum allowed channel length. Also, the functionality of the charge pump circuit does not critically depend on any MOS transistors transconductance. Therefore, HCI related degradation is expected to be the minimum in the proposed design and is considered to have an extremely small effect on the circuit performance.
2.4 Ways to avoid VSR reliability issues

The most obvious way to avoid the abovementioned VSR reliability issues is to use HVT CMOS devices. The advantage of using HVT CMOS devices is that little or no modification in existing circuit designs is needed. For typical applications, the HVT devices that are used in addition to the SLV CMOS process have thicker gate oxides. This thicker gate oxide enables MOS devices to operate at higher supply voltages but only up to a certain level which is typically less than twice than the standard operating voltage limit. For example, the 1.8 V 0.18 μm CMOS process used in the proposed design have a high voltage option of 3.3 volts. As expected, additional process steps are required for this option incurring additional costs which can rise as high as 10% [27].

For more demanding applications like inkjet printers and automotives, Smart Voltage eXtensions (SVX) are used with standard low voltage processes without introducing additional process steps. SVX has been successfully implemented in 0.5 μm CMOS technology without additional process steps [28]. However, with SVX, circuit layout becomes increasingly complex. Again, SVX is known to be accompanied by reduced breakdown voltage for PMOS transistors [29]. Also, this technique is not yet available for current CMOS generations.

The other solution is to use SLV CMOS devices. The idea is to divide the voltage stresses among several transistors. However, considerable changes in circuit design have to be introduced. In many situations, these changes make the new design considerably slower. The other obvious limitation of this method is the maximum allowable voltage stress in such designs is strictly limited by the junction breakdown voltage of NMOS and PMOS transistors. Some design examples of HVT circuits using
SLV CMOS devices can be found in [7], [30], [31], [32], [33], [34]. However, there are no known charge pump circuits designed with a modern SLV CMOS process at the time of this writing. It is assumed that numerous physical limitations of SLV CMOS processes are the main reasons behind this.

2.5 Summary of design guidelines

As indicated before, the proposed charge pump design is based on the third concept. The restrictions to avoid VSR reliability issues are also indicated in the previous sections. All the restrictions are summarized here again for simplicity. The following guidelines are strictly maintained throughout the design phase:

1. $V_{GS}$ and $V_{GD}$ have to be kept equal to or less than 1.8 volts for steady state condition to reduce TDDB. Unwanted voltage spikes must be kept within 2 volts ($\approx 10\%$) for a short duration.

2. $V_{DS}$ must be kept within 1.8 volts when the associated device is switched ON and channel lengths should be made sufficiently long to absorb transients in order to contain HCI.

3. $V_D/V_S$ for NMOS transistors should be kept within the breakdown voltage specified by the foundry (3.5-4 volts) to eliminate the possibility of junction breakdown.

4. $V_B$ of PMOS transistors must be contained within the foundry specified limit (6.5-7 volts) of junction breakdown voltage between associated N-well and substrate.
2.6 Conclusion

A number of reliability simulators are available at present out of which Berkeley Reliability Tools (BERT) is probably the most widely accepted one. It can simulate HCI and TDDB related degradation as well as electromigration. However, the lifetime of the proposed charge pump circuit was not verified by any reliability simulator. It will be seen in the following chapters that the proposed circuit satisfies all the foundry specified standard VSR reliability requirements in the design specified Monte Carlo analysis with ease and hence, is expected to have a reasonable lifetime.
Chapter 3

Conventional charge pump designs

3.1 Introduction

Charge pump circuits are essentially dc-dc converters used to produce on-chip voltages higher than the supply voltage. Higher voltage level is basically obtained by charging and discharging capacitors. They are widely used in programming E²PROMS, driving electrostatic actuators, analog switches in switch capacitor systems, LCDs, in dynamic gate biasing [35] and in numerous other applications requiring higher than the regular supply voltage. Current submicron devices can also be used to interface with standard high voltage logic with the help of charge pump circuits.

In this chapter, the evolution and improvement of charge pump circuits with their summarized working principle will be discussed. A range of ideas including the very first voltage multiplier to a number of modern CMOS charge pump structures are included in this discussion.

3.2 Working principle of charge pumps

The basic working principle of charge pump circuits can be best described by the simple schematic as shown in Fig. 3.1. This structure can generate a voltage twice than its regular supply voltage, VDD. Clocks $\Phi_1$ and $\Phi_2$ are non overlapping signals. During $\Phi_1$,
switches $S_1$ and $S_3$ are closed and capacitor $C$ is charged to $V_{DD}$. During $\Phi_2$, $S_1$ and $S_3$ are opened, $S_2$ is closed and node $A$ connects to $V_{DD}$ while the capacitor maintains its charge during $\Phi_1$. In other words without a load,

During $\Phi_1$, charge across $C$ is $V_{DD} \cdot C$

During $\Phi_2$, $(V_{OUT} - V_{DD}) \cdot C = V_{DD} \cdot C$

which gives, $V_{OUT} = 2V_{DD}$

![Figure 3.1: Schematic of a voltage doubler (2VDD) circuit.](image)

When a load $R_{LOAD}$ is connected at the output node as shown by the dotted line, a smoothing capacitor is also used in parallel which helps the output voltage to remain stable. For a particular frequency, the output ripple voltage is controlled by the time constant of $C_{OUT}R_{LOAD}$.

### 3.2.1 Cockcroft-Walton Multiplier

Voltage multiplication technique was first proposed and implemented by Cockcroft and Walton [36], [37] in 1930s to generate a steady potential of 800 kV for an experiment investigating atomic structure. Thermionic rectifiers and capacitors were used to generate this dc voltage. The switches are operated according to non overlapping signals
$\Phi_1$ and $\Phi_2$ as shown. The capacitors $C_1, C_2, C_3, C_A$ and $C_B$ are considered to be of equal size for simplified analysis. $C_1$ is always charged to VDD. During $\Phi_1$, $C_A$ is also charged to VDD. During $\Phi_2$, the top plate of $C_A$ will be pushed to 2VDD potential level and will be connected to the top plate of $C_2$. Hence $C_2$ and $C_A$ will be connected in parallel. After charge sharing; voltage across them will be VDD/2. In the next $\Phi_1$, $C_2$ and $C_B$ will share charges and voltage across them will be VDD/4. At the same time, $C_A$ will charge to VDD again. Therefore, the output node will be gradually charged to a potential close to 3VDD level. It is quite evident that this structure can be further extended.

![Figure 3.2: Schematic of Cockroft-Walton multiplier](image)

However, this design cannot be realized in IC technology because the on-chip capacitors are limited to a few pFs with a relatively large parasitic capacitance. In fact, successful operation of this circuit structure heavily relies on the ratio of the charging capacitance and associated parasitics. In addition, the output impedance of the multiplier increases rapidly with the number of multiplying stages [38].
3.2.2 Dickson Charge Pump

The Dickson charge pump [38] overcomes the limitations of Cockcroft-Walton multiplier and can be effectively implemented in earlier generations of IC technology replacing thermionic rectifiers with diodes. The operating principal of Dickson circuit closely resembles that of Cockcroft-Walton multiplier. However, this configuration ensures better and more efficient multiplication even with the presence of relatively large parasitic capacitance as the nodes in the diode chains are coupled with the inputs via capacitors unlike Cockcroft-Walton multiplier. Fig. 3.3 clearly points it out.

\[\text{Figure 3.3: Comparison between Cockcroft-Walton multiplier (top) and Dickson charge pump (bottom).} \]

In practice, the Dickson charge pump can be easily implemented in modern CMOS processes using diode connected MOS transistors instead of diodes. Such an
implementation in NMOS is shown in Fig. 3.4. The voltage fluctuation at each pumping node is virtually identical and can be defined as [39]:

\[
\Delta V = V_{DD} \cdot \frac{C}{C + C_s} - \frac{I_{Load}}{f_{osc} \cdot (C + C_s)}
\]  

(3.1)

where \( C \) is the pumping capacitance, \( C_s \) is the parasitic capacitance associated with each pumping node, \( f_{osc} \) is the frequency of the non overlapping clocks \( \Phi_1 \) and \( \Phi_2 \) and \( I_{Load} \) is the load current.

Figure 3.4: NMOS implementation of Dickson Charge Pump. The presence of forward diode voltage drop should be noted.

The voltage pumping gain of a charge pump \( G_V \), for the \( N^{th} \) pumping stage is defined as [39]:

\[
G_V = V_N - V_{N-1}
\]  

(3.2)

where \( V_N \) and \( V_{N-1} \) are the steady state lower voltage at \( N^{th} \) and \( (N-1)^{th} \) node. Now, for Dickson charge pump, \( G_V \) can be written as [39]:
where $V_{Th}$ is the threshold voltage of the MOSFET of the last stage of any two stages considered and is modified due to body effect in a typical NMOS implementation. It should be noted that $G_v$ does not depend on the aspect ratios of the MOS transistors unless a small W/L ratio prevents the node voltages to settle down within the operating clock cycles.

Obviously, for the circuit to function properly, the relationship $\Delta V - V_{Th} > 0$ must be satisfied. It is clearly seen that, for lower supply voltages, the pumping gain of this circuit configuration decreases due to threshold voltage drop which turns to worse due to body effect. This makes the Dickson charge pump virtually unsuitable for modern low voltage submicron CMOS processes. Efforts to reduce this inherent problem have been made in numerous works. Some notable designs based on Dickson charge pump can be found in [40], [41], [42] and [43].

However, this problem can be completely eliminated if the threshold voltage, $V_{Th}$, is removed from the voltage pumping gain equation. MOS charge pumps using Charge Transfer Switches (CTS's) proposed by J. Wu and K. Chang [39] offers an excellent solution to this problem.

### 3.2.3 Charge Transfer Switch (CTS) Charge Pump

This charge pump uses MOS transistors with proper ON/OFF sequences, referred to as CTS's instead of diodes or diode connected transistors which inevitably introduces a
forward voltage drop at each pumping node. Figure 3.5 shows the ‘New Charge Pump’ (NCP-1) using CTS’s with static backward control [39], [44].

MD1 - MD4 are diode connected MOS transistors setting up the initial voltages at the pumping nodes. MS1 - MS4 are the charge transfer switches and are controlled by the higher voltage swings at the pumping nodes of their respective next stages. It is clearly evident that CTS’s will only work if they can be turned ON/OFF at the designated clock phases such that they will push charge only in one direction. Therefore, the lower voltage level at any pumping node is equal to the higher voltage level at the previous node. The voltage pumping gain for this configuration thus becomes:

\[ G_V = V_N - V_{N-1} = \Delta V \] (3.4)

Therefore, this configuration gives better gain compared to Dickson charge pump eliminating the \( V_{Th} \) term. It can be shown that, for proper operation of this circuit configuration, the following relation must be satisfied [44]:

![Figure 3.5: Four stage charge pump with static CTS's (NCP-1). The absence of forward diode voltage drop is notable [39]. Transistor names are shown in bold.](image)
where $V_{Th}$ is the threshold voltage of the CTS MOS transistor of the last stage of any two stages under consideration. Therefore, this circuit is more suitable for low voltage operation than the Dickson circuit.

However, in this circuit configuration, the CTS’s cannot be completely turned off when intended because the relationship $2\Delta V < V_{Th1}$ can never be met if the operating condition $2\Delta V > V_{Th}$ is met, where $V_{Th1}$ is the threshold voltage of the CTS MOS transistor of the first stage of any two stages considered and $2\Delta V$ is the Gate-Source voltage of the associated CTS MOS transistor. Therefore, charge leakage will occur from the nodes with higher voltages to the nodes with lower voltages.

Better pumping performance can be obtained by adding extra pass transistors in the NCP-1 circuit. This new circuit is called ‘New Charge Pump -2’ (NCP -2) \[39\] and is shown in Fig. 3.6.

Figure 3.6: Four stage charge pump with dynamic CTS’s (NCP-2) [39]. Transistor names are shown in bold.
The function of these pass transistors is to apply dynamic control to the CTS’s such that they turn OFF completely when required and still be able to turn them ON easily by the ‘backward control voltage’ as in NCP-1. The operating conditions for the New Charge Pump with dynamic CTS’s (NCP-2) can be shown as [39]:

\[
2\Delta V > V_{thp} \quad (3.6)
\]

and \[ 2\Delta V > V_{thN} \quad (3.7) \]

where \( V_{thp} \) is the threshold voltage of the PMOS transistors and \( V_{thN} \) is the threshold voltage of CTS MOS transistor of the last stage of any two stages under consideration. Both of the conditions can be simultaneously met in this circuit arrangement. Therefore, charge leakage can be stopped by dynamic control of charge transfer switches and thereby increasing the circuit efficiency. However, in both NCP-1 and NCP-2, MDO is a diode connected transistor which causes an undesirable forward voltage drop. In a bid to improve voltage pumping gain and circuit efficiency, several charge pump designs have evolved from NCP-1 and NCP-2 out of which [45] and [46] are worth noting.

### 3.2.4 High efficiency Charge Pump using Level Shifters

A new charge pump structure utilizing level shifting circuits [47] offers higher efficiency than the conventional charge pump structures. Fig. 3.7 shows the schematic of this charge pump.

CLKA and CLKB are non overlapping clocks. CLKA_D and CLKB_D are delayed signals of CLKA and CLKB respectively and are used to turn the charge transfer MOS
transistors (M1 to M4) ON or OFF at the point when CLKA and CLKB change their states. The gate voltages of these MOS transistors are controlled by level shifter circuits LS1 to LS4. Charge from VDD is transferred in order to C1, C2, C3 and CLoad to produce a stepped up output voltage of 4VDD. This circuit structure has the feature that the required breakdown voltage in charge transfer MOS transistors is reduced from 4VDD for conventional charge pumps to 2VDD resulting in reduced impedance. This allows the circuit to supply higher currents and increase its efficiency [47].

Charge leakage problem has been handled by delayed clock signals CLKA_D and CLKB_D which ensure the signals that turn ON the charge transfer MOS transistors are delayed relative to the timing with which the pumping nodes (N1 to N3) are switched.
ON. This arrangement reliably prevents charge leakage significantly increasing voltage gain and circuit efficiency.

### 3.2.5 High efficiency cross-coupled Charge Pump

This charge pump structure is based on a simple clock booster circuit with two cross-coupled NMOS and two charging capacitors. Two PMOS transistors are used as serial switches which compare between two voltages and pass the highest voltage to the output node. The circuit schematic is shown in Figure 3.8 [48].

Nodes A and B swings between VDD and 2VDD alternately. At any instant, the node with higher voltage is connected to the output smoothing capacitor $C_{\text{Load}}$. In this way, 2VDD output is produced. High efficiency can be achieved if the switches have low ON resistance. Clearly, this configuration can be stacked to generate higher voltages.

![Figure 3.8: 2VDD charge pump based on cross-coupled NMOS transistors. $\Phi_1$ and $\Phi_2$ are non-overlapping clock signals [48].](image)

Based on this configuration, several other designs have been put forward. Area efficient charge pumps are proposed in [49] and [50], a multi value charge pump is presented in [51] while a high efficiency voltage doubler has been designed in [35].
3.3 Conclusion

Over the years, numerous charge pump structures have been designed for different applications. Only a few of them have been discussed here. Most of these designs are basically offshoots of the Dickson charge pump which try to eliminate its inherent disadvantages for modern low voltage CMOS processes. However, as pointed out before, virtually all the designs require HVT CMOS devices for practical implementation. Efforts on designing charge pumps with SLV CMOS process have not been hard enough mainly because of the numerous physical limitations of low voltage CMOS devices. To the knowledge of the author at the time of writing this thesis, the proposed design is the first attempt to design and implement a fully integrated HVT charge pump with a modern SLV CMOS process.
Chapter 4

Circuit design and considerations

4.1 Introduction

The proposed design is a fully integrated charge pump and is based on an NMOS cross-coupled structure from [48] and [52]. This design has been chosen because of its high efficiency and voltage gain. The chapter begins with discussions on potential VSR reliability issues of this design when the basic voltage doubler cell is stacked to generate an output voltage of four times the VDD supply voltage (4VDD). Then the design issues of the proposed charge pump are analyzed which are followed by reliability and functionality requirements of different circuit blocks. Finally, design of the on-chip clock generator ends this chapter.

4.2 Analysis on high efficiency cross-coupled charge pump

As previously pointed out, the proposed design is based on a conventional charge pump structure as shown in Fig. 3.8. A complete circuit schematic of this cross coupled structure is presented in Fig. 4.1. The basic principle of operation is quite evident from the node voltages shown by the right. Two complementary clock signals CLKA and CLKB swing from 0 to VDD. Therefore, INA and INB signals are also complementary and swing from VDD to 0. During steady state operation of the charge pump, node VA
CIRCUIT DESIGN AND CONSIDERATIONS

and VB alternately swing from VDD to 2VDD. When node VA is at 2VDD, M1_2 is
turned ON and the potential at node VB equals to VDD as C1_2 charges fully from the
supply voltage. During this time, M1_1 is switched OFF and M1_3 is turned ON which
allows C1_1 to share charge with the output capacitor CLoad at node 2VDDOUT.

![Diagram](image_url)

Figure 4.1: Complete schematic of High efficiency cross-coupled 2VDD charge pump [52]. Node names are shown in bold (Left). Voltage waveforms at different nodes are also shown (Right).

Therefore, the output voltage at node 2VDDOUT rises gradually and finally reaches
close to twice the VDD supply (2VDD). The output ripple voltage depends on the time
constant CLoadRLoad as expected. Charging capacitors C1_1 and C1_2 are typically off-
chip capacitors to supply a large current. However, for smaller loads, these capacitors
can be fabricated on-chip. Since the output receives charge in both the half cycles from
C1_1 and C1_2 alternately, this structure is also known as dual-cell doubler. High
efficiency is ensured by low ON resistance of the PMOS serial switches M1_3 and
M1_4. Fig. 4.2 shows the simulation of output voltage at node 2VDDOUT. As
expected, like all other charge pump designs, the output voltage of this circuit
configuration never reaches a steady 2VDD potential because of the load current and
charge sharing between the output capacitor and the charging capacitors.
Timing relationships between voltages at nodes VB, VA, INB and INA are shown in Fig. 4.3. Charge delivered by C1_1 and C1_2 to the node 2VDDOUT is clearly seen in VA and VB waveforms as their potential gradually decrease after reaching 2VDD level.

Figure 4.3: Simulation waveforms at node VB, VA, INB and INA.
4.2.1 Cascaded voltage quadrupler (4VDD) design

The voltage doubler or 2VDD charge pump can be stacked with similar circuit blocks to produce higher output voltage. In this situation, the 2VDD output of the first stage acts as the regular supply for the second stage, then 4VDD output of the second stage works as the supply voltage for the third stage and so on. Fig. 4.4 shows a typical example of 4VDD charge pump [49]. CLKC and CLKD are complementary clocks but they swing from 0 to 2VDD. Therefore, node INC and IND alternately swing from 2VDD to 0. Finally, node VC and VD swing from 4VDD to 2VDD. PMOS serial switches M2_3 and M2_4 turn ON alternately to charge the output node 4VDDOUT to 4VDD potential.

Figure 4.4: 4VDD charge pump by stacking two 2VDD charge pumps [49]. Node names are shown in bold.
Fig. 4.5 shows simulation of voltage waveforms at node 2VDDOUT and 4VDDOUT.

VB, VA, VD and VC node voltages and their timing relationships are shown in Fig. 4.6.
4.2.2 VSR reliability issues in 4VDD design

Like other conventional charge pump designs, the 4VDD design presented in the previous section requires HVT CMOS devices. However, if, designed with SLV CMOS devices, a number of VSR reliability issues cannot be avoided.

As stated in Chapter 2, as a rough guideline, $V_{GS}$ and $V_{GD}$ must be contained within the operating voltage limit to minimize gate oxide damage. Again, to minimize the effect of damage due to hot carriers, $V_{DS}$ should be kept within the limit of operating voltage when the associated device is in saturation. And finally, the voltage between drain/source to substrate junction of NMOS transistors should be kept within the 3.6 volts limit to avoid junction breakdown.

To start with, the MOS transistors in the drivers (inverters) connected to the bottom plates of C2_1 and C2_2 have a potential gate oxide breakdown problem since they need clock signals of 0 to 2VDD swing. In addition to TDDB reliability issue, they will face severe transient hot carrier damage because of the high $V_{DS}$ when they are saturated.

Again, from Fig. 4.6, VC and VD are complementary signals swinging from 2VDD to 4VDD voltage levels. This causes a 2VDD stress across the gate oxide of M2_1 and M2_2. There will also be transient hot carrier damage since their $V_{DS}$ will always swing from 0 to 2VDD. And finally, these MOS transistors will also face junction breakdown between source and substrate.
The PMOS serial switches M2_3 and M2_4 will 2VDD gate oxide stress. These transistors will also experience transient hot carrier damage. Fig. 4.7 presents the \( V_{GS} \) and \( V_{DS} \) stress of M2_1, M2_2 and \( V_{GS} \) of M2_3 and M2_4 MOS transistors.

![Figure 4.7: \( V_{GS} \) and \( V_{DS} \) stress of MP2_1, MP2_2, M2_3 and M2_4 in the conventional 4VDD design.](image)

Therefore, it is quite evident that all the MOS transistors in the second stage of the 4VDD charge pump will face severe reliability issues if the circuit is designed with an SLV CMOS process.

A careful analysis shows that most of the VSR reliability problems are caused by the 2VDD to 4VDD swing of nodes VC and VD. A reduced swing of 2VDD to 3VDD (hence, 1VDD voltage stress in MP2_1, MP2_2, M2_3, M2_4) offers better reliability in TDDB and hot carrier induced damages. However, some reliability problems still remain and will have to be solved by careful circuit design. Hence, a 3VDD output is more feasible considering the numerous physical limitations of an SLV CMOS process.
4.3 Requirements and initial analysis of 3VDD charge pump

By careful design, the second charge pump stage can be implemented to step up the voltage only by 1VDD instead of 2VDD. This avoids excessive gate oxide stress and hot carrier damage in M2_1, M2_2, M2_3 and M2_4 as well as in the drivers of the charging capacitors as the voltage difference between node VC and VD remains within 1VDD at any instance.

However, since VC and VD are complementary signals swinging from 2VDD to 3VDD, the junction breakdown problem still persists in M2_1 and M2_2 as the voltage between their source and substrate reaches 3VDD in each period. A straightforward way to avoid this is to use PMOS transistors instead of NMOS transistors because of the flexibility of PMOS transistor's substrate connection. But unlike cross-coupled NMOS transistors, this newly introduced PMOS transistor pair MP2_1 and MP2_2 (Fig. 4.8) will need precise control signals to switch ON and OFF for successful and efficient circuit operation.

With this scenario in mind, it can be seen that in the steady state condition, MP2_1 and MP2_2 have a virtually constant 2VDD connection with their source while their drain terminals have voltages swinging between 2VDD to 3VDD. Successful circuit operation requires MP2_1 and MP2_2 to switch OFF when their respective drain voltages are at the higher potential i.e. 3VDD and to switch ON when their respective drain voltages are at the lower potential i.e. 2VDD. In other words, the gate control signals of MP2_1 and MP2_2 should be at 3VDD when their respective drain voltages are at 3VDD and at 1VDD when their respective drain voltages are at 2VDD. Precise timing of gate signals eliminates any potential VSR reliability issues.
Therefore, the gate control signals for MP2_1 and MP2_2 should alternately swing from 1VDD and 3VDD and should have minimum timing mismatch with VC and VD node voltages.

![Diagram of 3VDD charge pump design](image)

**Figure 4.8: Initial circuit structure of the proposed 3VDD design.**

### 4.4 Basic 3VDD charge pump design

In this section, construction of different circuit parts of the main charge pump is discussed. It includes the generation of control signals as well as the basic charge pump cell design issues. A complete circuit diagram is also presented.
4.4.1 High Voltage Tolerant (HVT) push-pull booster

The construction of the control signals swinging between 1VDD to 3VDD is divided into two different parts. At first, a clock signal swinging between 0 to 2VDD is generated. This clock signal is then 'pushed' upward by 1VDD which produces the desired control signal. The initially constructed 0 to 2VDD complementary signals should have similar timing characteristics of node voltages VC and VD. Moreover, the circuit topology should consume minimum amount of energy. The HVT push pull circuit designed in an SLV CMOS process in [7] offers an attractive solution. A simplified schematic diagram of this design is shown in Fig. 4.9.

The pull down part of the circuit works as follows. The PMOS transistors MLP1 and MLP2 shown inside the dotted rectangle compare the voltage between nodes OUTPUT and P and connect the higher voltage to the gate of ML3. The two NMOS transistors MLN1 and MLN2 work in a similar way and connect the lower voltage to the gate of ML4 after comparing the voltages at nodes Q and OUTPUT. Therefore, during a pull down event, when the OUTPUT falls below VDD, the gate of ML3 switches to VDD and keep ML3 turned ON hard facilitating a fast pull down. On the other hand, The NMOS transistors MLN1 and MLN2 also compare the voltages between nodes OUTPUT and Q and connect the gate of ML4 to the lower voltage between (VDDL-VDD) and node voltage at OUTPUT. Therefore, during pull down, ML4 switches OFF and ML3 switches ON providing a fast circuit response. The pull up event is similar to the pull down event. The "break before make" arrangement prevents any shoot-through current. During operation, the circuit does not violate any VSR reliability requirement. From now on, this circuit will be referred as HVT push-pull booster to avoid confusions.
In the proposed design, VDDH for this HVT push-pull booster circuit is 2VDD. Hence, the floating voltage source of (VDDH-VDD) volts can be replaced by a simple VDD potential. The HVT 'break before make' block (which is typically implemented by an SR flip-flop) and the inverter combination connected to the gate of ML6 generates a clock signal swinging between VDDH and VDD and is in phase with CLK signal. Since voltages at nodes VA and VB swing alternately between 1VDD to 2VDD, this control signal can be tapped off these nodes of the first charge pump cell. Adjustment of the aspect ratios of ML1-ML6 prevents any possibility of shoot through current. It will be seen later that this HVT push-pull booster will drive small capacitors and hence, does not require a high current carrying capability. Therefore, a careful designing avoids both shoot-through current and ensures the 0 to 2VDD signals with the required timing characteristics.
4.4.2 Gate control signal generation

The HVT push-pull booster generates 0 to 2VDD signal. A capacitor and diode combination can be used to 'push' this signal to produce the required control signal swinging between 1VDD to 3VDD. Fig. 4.10 shows the schematic of this arrangement.

Figure 4.10: HVT push-pull booster and diode-capacitor combination to generate 3VDD/1VDD gate control signal at node U. Node names are shown in bold.

For example, in Fig. 4.10, the voltage at node OUTPUT swings between 0 to 2VDD (0 to 3.6 V). When the voltage at this node becomes 0, the associated diode chain turns on and charge the capacitor $C_{\text{Left}}$ such that the top plate is charged by 1VDD (1.8 V) only. When voltage at node OUTPUT becomes 2VDD, the top plate of capacitor $C_{\text{Left}}$ is pushed up by 2VDD voltage. Hence, voltage at the top plate of $C_{\text{Left}}$ (node U) will swing between 1VDD to close to 3VDD (1.8 to 5.4 V). The associated voltage waveforms will be presented in chapter 5. The diode chain is realized by diode connected MOS transistors. The aspect ratios of these transistors are tailored to meet the VSR reliability requirements of MP2_1 and MP2_2 (Fig. 4.8).
4.4.3 PMOS substrate connections

For a PMOS transistor to work properly without leakage, its substrate must be connected to its highest potential. The drains of MP2_1 and MP2_2 in Fig. 4.8 swing between 2VDD to 3VDD while their sources are always connected to 2VDD. Therefore, the substrates of MP2_1 and MP2_2 can only be connected to the output node which, during steady state, should stay close to 3VDD potential. However, during the startup, voltages at nodes VC and VD should be significantly higher than that of node 3VDDOUT. This might forward bias the junctions of MP2_1, MP2_2, M2_3 and M2_4 temporarily facilitating a shorter rise time for the output voltage at node 3VDDOUT. As mentioned before, after this transient condition, these junctions should no longer remain forward biased as node voltage 3VDDOUT gradually increases and crosses the node voltage at 2VDDOUT allowing the associated MOS transistors to function properly.

Figure 4.11: Simulation of 3VDD design showing relationship between node voltages VC and 3VDDOUT. During start-up, node voltage VC goes as high as 0.8 volts higher than that of node 3VDDOUT (Inset1). In steady state, it drops to 0.06 Volts (Inset2).
Simulation of the proposed 3VDD design supports this argument. It is clearly seen from Fig. 4.11 that during start up, voltage at node VC goes as high as 0.8 volts higher than that of node 3VDDOUT. On the other hand, during steady state operation, the peak voltage at node VC is only 0.06 volt higher than voltage at 3VDDOUT node which is extremely small to forward bias the associated junction and hence, disrupt the intended functionality of M2_1. As expected, the same argument is valid for MP2_2 and node VD of Fig. 4.8.

4.4.4 Complete circuit design

The complete charge pump circuit is divided into separate smaller blocks. There are two different charge pump cells out of which, the first one producing a 2VDD output is similar to the conventional design. As discussed earlier, the second charge pump, which is responsible for stepping up the output to 3VDD level, has been modified. Control signals for successful operation of the charge pump are generated with the help of HVT push-pull booster and diode-capacitor arrangement. As shown by the dotted lines, the substrates of the PMOS transistors in the second charge pump cell as well as in the HVT blocks are connected to the node 3VDDOUT. The complete charge pump design is presented in Fig. 4.12.
4.4.4.1 Transistor dimensions

Aspect ratios of different transistors in this design are extremely important to ensure VSR reliability. The aspect ratios of the transistors of main charge pump cells ensures reasonable output voltage while that of the transistors in the push-pull booster circuits prevent any voltage spike potentially threatening to VSR reliability.

Table 4.1 enlists the corresponding widths, lengths and aspect ratios of the transistors shown in Fig. 4.11. Dimensions of the transistors of the auxiliary circuits can be found in the extracted net list which is included in the CD.
**Table 4.1: Transistor dimensions of the charge pump circuit shown in Fig. 4.12.**

<table>
<thead>
<tr>
<th>Transistor name</th>
<th>Width; W (μm)</th>
<th>Length; L (μm)</th>
<th>Aspect Ratio; (W/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1_1, M1_2</td>
<td>1.2</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td>M1_3, M1_4</td>
<td>4.8</td>
<td>0.4</td>
<td>12</td>
</tr>
<tr>
<td>DRL1_P, DRR1_P</td>
<td>4.8</td>
<td>0.4</td>
<td>12</td>
</tr>
<tr>
<td>DRL1_N, DRR1_N</td>
<td>2.4</td>
<td>0.4</td>
<td>6</td>
</tr>
<tr>
<td>MP2_1, MP2_2</td>
<td>19.2</td>
<td>0.4</td>
<td>48</td>
</tr>
<tr>
<td>M2_3, M2_4</td>
<td>4.8</td>
<td>0.4</td>
<td>12</td>
</tr>
<tr>
<td>DRL2_P, DRR2_P</td>
<td>4.8</td>
<td>0.4</td>
<td>12</td>
</tr>
<tr>
<td>DRL2_N, DRR2_N</td>
<td>2.4</td>
<td>0.4</td>
<td>6</td>
</tr>
<tr>
<td>ML6, MR6</td>
<td>1.2</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td>ML5, MR5</td>
<td>1.2</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td>ML4, MR4</td>
<td>1.2</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td>ML3, MR3</td>
<td>0.8</td>
<td>0.4</td>
<td>2</td>
</tr>
<tr>
<td>ML2, MR2</td>
<td>0.8</td>
<td>0.4</td>
<td>2</td>
</tr>
<tr>
<td>ML1, M21</td>
<td>0.8</td>
<td>0.4</td>
<td>2</td>
</tr>
<tr>
<td>D1, D2, D3, D4</td>
<td>4.8</td>
<td>0.4</td>
<td>12</td>
</tr>
<tr>
<td>MLN_1, MLN_2</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>MLP_1, MLP_2</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>MRN_1, MRN_2</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>MRP_1, MRP_2</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
</tr>
</tbody>
</table>

These dimensions were at first derived from [49] for driving a load resistor of 200 kΩ to 300 kΩ with an output load current of 20 μA. However, the final values presented in table 4.1 were quite different from the optimum values obtained by simulation as the modeling of the two stage charge pump circuit did not take the charge leakage (especially in M1_1, M2_1, MP2_1 and MP2_2) into consideration.
M1_1 and M2_1 are designed to have relatively small aspect ratio to minimize any leakage current going back from node VA to the supply voltage VDD during a 2VDD voltage level at that node and M1_1 is turned OFF (and so is for node VB and M1_2) [49]. DRL1_P, DRL1_N, DRL2_P, DRL2_N, DRR1_P, DRR1_N, DRR2_P, DRR2_N are designed to push up and pull down the bottom plates of the charging capacitors effectively within half of the operating clock frequency. MP2_1 and MP2_2 have been made sufficiently large to charge capacitors C2_1 and C2_2. Finally, the PMOS serial switches M1_3, M1_4, M2_3 and M2_4 are designed to offer very small ON resistance so that nodes 2VDDOUT and 3VDDOUT can be charged efficiently without any unwanted voltage drop across them. However, as pointed out before, these transistor dimensions have been chosen to supply a 20 μA load current only. For higher current, the transistor dimensions in the charge pump cells and in the drivers have to be changed according to the requirement.

4.5 Auxiliary circuit designs

This section deals with various aspects of the on-chip clock generator. It includes a brief discussion on current starved ring oscillator, supply independent current reference and clock divider.

4.5.1 On-chip clock generator

The proposed integrated charge pump consists of an on-chip clock generator which is turned ON/OFF by a control signal. The frequency of the clock generator is designed to be relatively independent of the nominal supply voltage, VDD. A voltage independent
current source provides supply independent current to a current starved oscillator which sets up the initial clock frequency. A frequency divider is then used to produce two complementary clock signals (INVERTED and NON_INVERTED) for the charge pump. Fig. 4.13 shows a block diagram of the clock generator. A provision for external clock has been kept in this design as well. The internally generated clock or the external clock will be fed to the frequency divider depending on the input control signal. This arrangement is such that, when the external clock is chosen as the input to the frequency divider, the ring oscillator is turned off.

![Block diagram of on-chip clock generator](image)

**Figure 4.13:** Block diagram of on-chip clock generator. Node names are shown in bold.

### 4.5.2 Current starved ring oscillator

Ring oscillators are the easiest solutions to on-chip clock generation. In its simplest form, it consists of an odd number of cascaded inverters, with the output of the cascade being fed back to the input of the inverter chain. In this configuration, the oscillator frequency is completely dependent on the inherent inverter time delay and is therefore not externally controllable. If the delay of a single inverter with a capacitive load equal
to its input capacitance is $t_p$, then, the oscillator shown in Fig. 4.14 (top) will have a period of $2 \times 5 \times t_p$ provided all the inverters are of same size. It is possible to control this ring oscillator by simply adding a NAND gate in the inverter chain as shown in Fig. 4.14 (bottom). In this situation, when the oscillator operates, a HIGH signal is needed to one of the inputs of the NAND gate so that it behaves as an inverter. Understandably, an odd number of inversions are required as shown in Fig. 4.14 (bottom).

![Diagram of ring oscillator with 5 inverters (top) and with 4 inverters and a NAND gate (bottom).](image)

However, to obtain a low frequency in the range of a few MHz, a large number of inverter stages are required. For example, the 1.8 V 0.18 μm low voltage CMOS process that have been used in this work requires 31 stages of standard inverters for an oscillation frequency of 417.63 MHz. Therefore, a simple ring oscillator will require a large number of stages to produce an initial frequency of 5 MHz. A ring oscillator with current starved inverters presents an attractive solution to this problem.

In a current starved ring oscillator, the current carrying capability of each inverter is controlled by a pair of current sources. Therefore, a much lower frequency can be easily obtained with only a few stages of inverters by controlling the current sources which, in turn, control the delay of the inverters. Fig. 4.15 (top) shows the basic circuit
arrangement. The current sources are controlled by a supply independent current reference circuit. In many applications, the reference current, $I_{\text{Ref}}$ is varied to obtain a wide range of oscillation frequency out of the current starved ring oscillator. However, in the proposed design, the reference current will be kept constant in order to minimize the variation in operating frequency with supply voltage variation.

![Figure 4.15: Current starved ring oscillator for on-chip clock generation. The basic arrangement is shown in the top. The circuit design shown in the dotted area in the top is shown in a more elaborate way at the bottom.](image)

### 4.5.3 Supply independent current reference

The design of the CMOS current reference is based on a widely known bipolar circuit. A simplified CMOS version of this design is shown in Fig. 4.16 [53]. However, this circuit takes care of the temperature and process variations only. The two PMOS transistors MCL2 and MCR2 form a current mirror with a gain of
(MCR2_AR/MCL2_AR) where, MCR2_AR and MCL2_AR define their respective aspect ratios. Again, the two NMOS transistors form another current mirror with a gain of (MCL1_AR/MCR1_AR) provided that $I_{Ref}$ is so small that the voltage across the resistance $R$ can be neglected. MCL1_AR and MCR1_AR are the aspect ratios of MCL1 and MCR1 respectively. Now, these two current mirrors form a closed loop, where the loop gain is the product of their gains. This loop gain is chosen higher than unity such that the current in both the branches increases until they reach an equilibrium state and the gain is only reduced by the voltage drop $V_R$ across resistance $R$ [53]. If the NMOS transistors are in weak inversion region, the voltage across the resistor $R$ can be defined by [54]:

$$V_R = U_T \cdot \ln \left( \frac{MCR1_{AR} \cdot MCL2_{AR}}{MCL1_{AR} \cdot MCR2_{AR}} \right)$$

(4.1)

Where, $U_T$ is the thermal voltage and is defined by $U_T = \frac{kT}{q}$.

![Figure 4.16: Conventional CMOS current reference with resistor [53].](image-url)
For the proposed design, it is required that the operating frequency stays close to 2.5 MHz regardless of supply variations. This requires a supply independent current supply for the current starved ring oscillator. By simply adding more stacked transistors, this circuit can be made almost voltage independent for a range of around 1.5 volts to 2.1 volts. Fig. 4.17 shows the schematic of the current reference used in the design. The aspect ratios of the MOS transistors have been chosen such that the required resistance is smaller and at the same time, the current remains relatively independent of the supply. Like the conventional current reference, a startup circuit consisting of D_C1, D_C2, D_C3, D_C4 and D_CS MOS transistors is added to ensure its proper operation. This ensures the node STARTUP does not stay at s0V when VDD is applied thereby avoiding a possible deadlock during circuit startup.

![Figure 4.17: Proposed supply independent current reference circuit. The startup circuit is shown inside the dotted rectangle. Substrate connections are shown in thin dotted lines. Node names are shown in bold.](image-url)
4.5.4 Clock divider

The T or ‘toggle’ flip-flop has been used as the clock divider. It changes its output on each clock edge producing an output clock with half the frequency of the input clock. It has been constructed from a master-slave J-K flip-flop by connecting both of its inputs to HIGH. The output is a pair of complementary clocks with a 50% duty cycle and half the frequency of the input clock regardless of its duty cycle. This is extremely advantageous for proper operation of the charge pump circuit. The rise and fall time of the signals are adjusted by the last two NAND gates according to the requirement of the circuit. Fig. 4.18 shows the gate level schematic diagram of the clock divider.

![Gate level schematic of frequency divider (by 2). Node names are shown in bold.](image)
Chapter 5

Simulation results

5.1 Introduction

Pre-layout simulations of different circuit parts of the fully-integrated charge pump are included in this chapter. Generation of clock and gate control signals and different node voltages are presented at first. Then the output voltage and circuit efficiency with fixed and different load conditions and with different supply voltages are included. Finally, Monte Carlo (MC) simulation focusing on VSR reliability issues concludes this chapter.

5.2 On-chip clock signal

The first sub-section deals with the simulation results of the supply independent current reference and its performance comparison with the conventional current reference circuit [53] which is specifically designed to be process and temperature independent. This is followed by the current starved ring oscillator and the frequency divider output voltage waveforms.

5.2.1 Supply independent current reference

As specified before, the proposed current reference structure is designed to be supply independent. The simulation result presented in Fig. 5.1 supports this claim.
A closer view of Fig. 5.1 is presented in Fig. 5.2. It is seen that with a supply variation from 1.7 to 2.15 volts, change in current in the conventional reference is 363 nA/V, while it is only 8.4 nA/V in the proposed design.

Figure 5.2: A close-up view of the supply dependence of reference current in the conventional and proposed design.
Figure 5.3 shows the start up circuit pulling up the node voltage from 0 volts and hence, is able to start the circuit without any difficulty. Again, a close-up of the initial transient is shown in the inset.

5.2.2 Current starved ring oscillator

Fig. 5.4 shows the current starved ring oscillator output. The ring oscillator needs only 4 current starved inverters and one current starved NAND gate to produce an initial frequency of 5 MHz. Node names are assigned from Fig. 4.14.

5.2.3 Frequency divider

Fig. 5.5 shows the input clock to the frequency divider and its output waveforms at nodes INVERTED and NON_INVERTED. The output signals are of 2.5 MHz with a
rise and fall time of around 1 ns. The input signal to the frequency divider is OSC_OUT with a frequency of 5 MHz.

Figure 5.4: Clock signals at different nodes of the current starved ring oscillator. Node names are assigned from Fig. 4.14.

Figure 5.5: Input and output voltage waveforms of the frequency divider. Node names are assigned from Fig. 4.11.
5.3 Gate control signal

As discussed in section 4.3.3, the HVT push-pull booster produces a 0 to 2V_DD signal which is pushed upwards by 1V_DD potential using a diode-capacitor combination (D1, D2, C_LEFT and D3, D4, C_RIGHT) to create the required 1V_DD to 3V_DD gate control signal.

Generation of this control signal can be easily understood from Fig. 5.6. Node P in Fig. 4.11 corresponds to node OUTPUT in Fig. 5.6. The input clock signal at node INVERTED swings from 0 to V_DD (0 to 1.8 V). The voltage at node VB swings between V_DD to 2V_DD (1.8 to 3.6 V). As seen from Fig. 4.11, these two node voltages are applied to gates of ML1 and ML6 respectively. The output signal at node OUTPUT from the corresponding push-pull booster circuit block swings between 2V_DD to 0 (3.6 to 0 V). Finally, the diode-capacitor combination is used to push this signal up by 1V_DD (1.8 V) at node U. This signal is used as the gate control signal of MP2_1.

Figure 5.6: Simulation waveforms at nodes INVERTED, VB, OUTPUT and U. Node names are assigned from Fig. 4.11.
5.4 VSR reliability issues

This sub-section is devoted to VSR reliability issues, particularly on vulnerable MOS transistors. A quick look at different node voltages of the 3VDD charge pump in Fig. 4.11 shows that MP2_1, MP2_2, M2_3 and M2_4 are the most vulnerable transistors as they deal with voltage levels as high as 3VDD. The diode-capacitor combinations (e.g. D1, D2 and C_{Left}) are designed to minimize the steady state as well as transient gate oxide stress on MP2_1 and MP2_2 such that the timing characteristics of node voltages U and V are very close to that of nodes VC and VD. However, it was not possible to perfectly match the rise and fall time of the P and Q node voltages in Fig. 4.11 mainly because of the stacked MOS devices in HVT push-pull boosters. As a result, some small and narrow voltage spikes are observed in V_{GD} waveform in Fig. 5.7. But the voltage spikes were contained within 1.9 volts in worst case situations and are believed not to have any significant effect on VSR reliability of MP2_1 and MP2_2 transistors.

Figure 5.7: Simulation of V_{GS}, V_{GD}, V_{DS} of MP2_1 and V_{DS} of M2_3. All the voltages satisfy typical VSR reliability requirement by staying below the 1.8 V limit. Transistor names are assigned from Fig. 4.11.
On the other hand, MOS transistors in the first charge pump cell do not face any VSR reliability problems because the maximum gate oxide stress on M1_1, M1_2, M1_3 and M1_4 is 1VDD. The HVT push-pull booster in [7] is basically designed such that the voltage stress is divided among the MOS transistors avoiding any typical VSR reliability concerns. The associated transistor dimensions are carefully chosen to avoid any potential short-circuit current while maintaining virtually same rise and fall time at nodes U and V with nodes VC and VD respectively (Fig. 4.11).

5.5 Output voltage

This section includes simulation results of the output voltage with fixed load, with different loading conditions and with different supply voltages. Circuit efficiency with different load and voltage gain with different supply voltages are also included. All these simulation results are performed on the specific charge pump circuit designed for a 200 kΩ to 300 kΩ resistive loads with an external 150 pF smoothing capacitor in parallel. The aspect ratios of the transistors of the charge pump circuit are presented in Table 4.1.

5.5.1 Output voltage with fixed load

The voltages at nodes 3VDDOUT and 2VDDOUT of the 3VDD charge pump are presented in Fig. 5.8. It is clearly seen that initially the voltage at node 2VDDOUT rises faster than that of node 3VDDOUT. Once the HVT blocks starts to produce the gate control voltages, rise of voltage at node 2VDDOUT slows down a little. 3VDDOUT node voltage rises initially because of forward biased drain-substrate junctions of the
PMOS transistors of the second stage of the charge pump and as well as of HVT push-pull booster circuits. Once these junctions get reverse biased, this node voltage continues to rise smoothly as the usual operation of the charge pump takes over.

Figure 5.8: Simulation of 2VDD and 3VDD voltages at nodes 2VDDOUT and 3VDDOUT. The ripple voltage is shown inset.

5.5.2 Output voltage with different load conditions

Fig. 5.9 shows the voltage at node 3VDDOUT with different loads ranging from 100 kΩ to 500 kΩ. From the simulation, it is quite evident that the voltage does not improve much at lower loads. Therefore, a reduced efficiency at lower loads is no surprise. The charging capacitors in this design are implemented by Metal Insulator Metal (MIM) capacitors. Though the capacitance per area for MIM capacitors is extremely large, it is found from simulation that the parasitic takes away nearly 10% of its average charging current in every cycle. This contributes to a significant reduction in efficiency which becomes quite clear at lower load conditions. The other contributor to lower output
voltage is the ON resistance of the PMOS serial switches which has been specifically designed for a 20 μA load current supply. With higher load currents, the voltage drop across them limits the maximum output voltage. An approximate equivalent circuit schematic of a typical MIM capacitor (modeled from TSMC spice files defining devices in the process) has been presented in Fig. 5.10. The component values of the model are roughly calculated for a maximum sized MIM capacitor of $30\mu m \times 30\mu m$.

![MIM Capacitor Schematic](image)

Figure 5.10: Schematic model of a MIM capacitor. Values are indicated for a maximum sized (30 μm X 30 μm) capacitor. An array of 49 such capacitors have been used to layout each charging capacitor of around 45 pF. Values are not exact.
Fig 5.11 shows simulation results of a 40 pF MIM capacitor. The top curve shows the current taken by the top plate of the MIM capacitor while the bottom curve shows the current to the ground node. Clearly, the average parasitic current is around 10% of the total charging current.

Figure 5.11: Simulation of currents of a 40 pF MIM capacitor shows nearly 10% of the charging current (top) is wasted through the parasitic components (bottom). Averages of both the currents are measured in each half cycle.

Fig. 5.12 shows the efficiency (in terms of charge transfer from VDD to load) of the 3VDD charge pump circuit (Fig. 4.11) with different load conditions. The total charge taken by the circuit from VDD and the total charge provided to the output by the circuit have been integrated over a specific time to calculate the circuit efficiency. The power consumption of the auxiliary circuits (Current reference and Ring oscillator) has not been taken into account since the circuit can also run from an external source. Higher efficiency in higher load conditions can be achieved by redesigning the dimensions of the transistors and size of charging capacitors.
5.5.3 Output voltage with different supply voltages

This 3VDD charge pump design can effectively multiply voltages with even a supply voltage of 1.2 volts virtually keeping the voltage gain constant. Simulation result of the output voltage with different supply voltages is presented in Fig. 5.13.
Fig. 5.14 shows the variation in voltage gain with supply voltage variation. Though the simulation has been run for supply voltages as low as 1.2 V, it must be kept in mind that the current source that has been designed for clock generator circuits starts to operate effectively from 1.6 V.

5.6 Monte Carlo (MC) simulation results

It is widely known that MC simulation selects process variables that have a known range of values but an uncertain value at any particular situation/instant. Due to its statistical nature, MC simulation should indicate any possibility of VSR reliability violation.

Fig 5.15-5.16 shows MC simulation results of \( V_{GS} \) of MP2_1 with default process variations (with both DEV and LOT variations). As indicated before, MP2_1 and MP2_2 are the most vulnerable to VSR reliability lifetime problems. The associated gate oxide stress as well as gate to drain voltage must stay within the 1.8 V limit.
Figure 5.15: First six runs of Monte Carlo simulation of $V_{GS}$ of MP2_1 showing the gate oxide stresses are within 1.8 V limit.

Figure 5.16: Last five runs of Monte Carlo simulation of $V_{OS}$ of MP2_1 shows the gate oxide voltage stresses are within 1.8 V.

Clearly, there is no violation of VSR reliability requirement for $V_{GS}$ in MP2_1 (and in MP2_2). All the voltage difference stays within the limit of 1.8 V. Fig. 5.17 and 5.18 shows the MC simulation of $V_{GD}$ of MP2_1 which reiterates the same fact.
Therefore, VSR reliability restrictions are not violated in any of the Monte Carlo simulations runs due to process variations in the proposed charge pump topology.
Finally, MC simulation of the output node 3VDDOUT is presented in Fig. 5.19 which shows the final output voltage remains virtually same in all the runs.

![Voltage at node 3VDD in 10 Monte Carlo simulation runs showing little change in the final output voltage.](image)

MC simulation result for $V_{DS}$ of MP2_1 and $V_{DS}$ of M2_3 are presented in appendix A due to their relative insignificance. It is also found that in MC simulations, operating frequency changes are very small and does not have any notable change in the circuit efficiency and voltage gain. MC simulation results on operating clock signals are also included in the same appendix.
Chapter 6

Layout considerations and post layout simulation

6.1 Introduction

A brief discussion on Metal Insulator Metal (MIM) capacitors is presented at the beginning of this chapter which follows post layout simulation results as well as relevant discussions. Layout of the whole design is presented in Appendix B. The complete layout GDS file is also included in the accompanying CD.

6.2 MIM capacitors

MIM capacitors offer an excellent and extremely compact solution to on-chip capacitors in modern CMOS processes. The capacitance per unit area for MIM capacitors is around 1 fF/μm² which is more than 20 times larger than the usual metal-metal layer capacitances. The parasitic capacitance is relatively small but it takes around 10% of total charging current as seen by Fig. 5.11. High capacitance is obtained by incorporating a new metal layer in between the top 2 metal layers of a particular process. This new metal layer is known as Capacitor Top Metal (CTM) layer and is placed very close to the capacitor’s bottom plate, resulting in a high capacitance/unit area. The top view (top) and front view (bottom) of a typical MIM capacitor layout is shown in Fig. 6.1.
The dielectric used in MIM capacitors is a PECVD oxide layer of around 35-40 nm thickness. The leakage current is typically very low for a bias voltage of less than 9-11 volts for this particular range of oxide thickness. The process used in this design is a standard 1.8 V 0.18 μm 6 metal layer process. Hence, the top two metal layers are metal6 (M6) and metal5 (M5). As seen from Fig. 6.1, the CTM layer CTM5 is very close to the metal5 (M5) layer separated by a thin dielectric. VIA5 is used to connect the CTM5 layer with M6 layer. Clearly, capacitance is formed between CTM5 and M5 layer. Fig. 6.2, 6.3 and 6.4 shows some MIM capacitor layouts. The particular design supports MIM capacitors of area up to 30μm × 30μm. Therefore, to realize a capacitor of 40pF, an area of 210μm × 210μm (≈ 44pF) is required. This is laid out as an array of 49 maximum sized capacitors (7×7).
Figure 6.2: An array of 49 maximum sized MIM capacitors giving a total capacitance of 44 pF.

Figure 6.3: A single MIM capacitor cell of a capacitance close to 1 pF.

Figure 6.4: A close up view of Fig. 6.2 shows M5 and M6 layer. Via5 are seen on M6 layers which connect it with the CTM5 layer below.
6.3 Post layout simulation

In this section, post layout simulation results of various node voltages including the output at node 3VDDOUT and 2VDDOUT are presented at first. VSR reliability issues and associated voltage waveforms are then included.

6.3.1 Current starved ring oscillator

Fig. 6.5 shows the post layout simulation output of the current starved ring oscillator. Node names are different from the ones assigned in Fig. 4.14. OSC_1, OSC_2, OSC_3, OSC_4 has been renamed to OSC_NAND, OSC_1, OSC_2 and OSC_3 respectively. The start up circuit was also found to operate flawlessly. However, the value of the resistance in the current reference had to be adjusted from 45 kΩ to 35 kΩ to achieve the desirable oscillation frequency.

Figure 6.5: Post layout simulation of different node voltages of the current starved ring oscillator.
6.3.2 Frequency divider

Fig. 6.6 shows the input and output of the frequency divider. The outputs INVERTED and NON_INVERTED are used to drive the charge pump as well as the HVT push pull booster circuit blocks. The rise time and fall time of these signals are close to 1 ns. Since the operating frequency of the charge pump is 2.5 MHz, it is obvious that the frequency of the signal OSC_OUT is 5 MHz.

![Waveform Diagram]

Figure 6.6: Post layout simulation of input and output voltages of the frequency divider. Node names are taken from Fig. 4.11.

6.3.3 Gate control signal

Fig. 6.7 shows the voltage waveforms associated with generation of gate control signal at node U. Node voltage INVERTED and VB are applied to gates of ML1 and ML6 of the HVT push-pull booster. The resulting voltage waveform at node OUTPUT is a signal swinging from 0 to 2VDD (0 to 3.6 V). The diode-capacitor combinations D1, D2, C_{Left} (and D3, D4, C_{Right}) are used to push this 0 to 2VDD signals up by 1VDD (1.8
V) at node U (and at node V). Voltage signals at nodes U and V are then used as the gate control signals for MP2_1 and MP2_2.

![Voltage Waveforms](image)

Figure 6.7: Post layout simulation of voltage waveforms associated with generation of gate control signal at node U.

6.3.4 VSR reliability issues

It has been previously indicated that the most vulnerable transistors to VSR reliability are MP2_1, MP2_2, M2_3 and M2_4. Fig. 6.8 shows $V_{GS}$, $V_{GD}$ and $V_{DS}$ of MP2_1 and $V_{DS}$ of M2_3. Clearly, all the voltage waveforms remain within 1.8 volt limit and hence do not violate any of the VSR reliability restrictions. The voltage spike on $V_{GD}$ of MP2_1 is also successfully restricted to 1.9 volts ($\approx 105\%$). It can be concluded from post layout simulation that, a reasonable circuit lifetime can be expected.
6.3.5 Output voltage

The voltages at nodes 3VDDOUT and 2VDDOUT (in Fig. 4.11) are shown in Fig. 6.9. The node voltages show similar characteristic to pre-layout simulation as expected. As seen, the ripple voltage is affected by the presence of capacitive couplings. Finally, the output voltage is dropped from 5.1 volts in pre-layout simulation to 5.03 volts in post layout simulation. However, the effect of the moment (at 2.5 μs) when the forward biased junctions of PMOS transistors MP2_1, MP2_2 become reverse biased (indicated in circle) is very pronounced on the 3VDDOUT node voltage in Fig. 6.9 unlike Fig. 5.8.
6.4 Conclusion

All the post layout simulation results conform to the ones obtained by the pre-layout simulation and the complete circuit with the integrated clock generator works flawlessly. Finally, as it is clearly seen, all the standard VSR reliability requirements are satisfied with ease.
Chapter 7

Conclusion

7.1 Chapter structure

In this chapter a summary of the achievements on this work is presented which is followed by a brief discussion on the limitations of the proposed design. Potential applications of this design are then discussed. Finally, possible avenues of future improvements of this design end the core of the thesis contents.

7.2 Achievements

In this work, a high efficiency on-chip charge pump circuit has been successfully designed in an SLV CMOS process. The circuit structure is based on the conventional charge pump design from [48] and [52]. However, the basic design cannot be implemented in an SLV CMOS technology. The proposed topology effectively solves this problem. The associated VSR reliability restrictions have not been violated in the design. Therefore, an acceptable level of lifetime and reliability can be reasonably expected from this circuit topology.

In comparison with Fig. 4.4, the proposed design occupies about 108% of real estate excluding MIM capacitors. However, in Fig. 4.11, additional circuits are needed as it is impractical to use extremely big resistors (as illustrated in [49] for simplicity) to create
efficient 0-2VDD signals which will cover more than that real estate covered by HVT
circuit blocks. The main difference between the two arrangements is the real estate
occupied by MIM capacitors. MIM capacitors cover an extremely large area. On the
other hand, use of internal MIM capacitors also means no ESD protection is necessary
and the charge pump is fully integrated with fewer pins/input connections avoiding a
frequently encountered problem in big designs.

This design is based on TSMC 1.8 V 0.18 μm 6 Metal CMOS process. The layout
measures 600 μm × 630 μm with the four charging capacitors implemented by MIM
capacitors. Pre layout and post layout simulation results of the complete design with
integrated clock generator indicate no violation of VSR reliability restrictions. Design,
simulation and layout have been carried out with the TSMC design kit from Mentor
Graphics Corporation. The complete layout has been extracted and extensively
simulated and checked for final tape out. However, implementation was suspended to
effectively utilize the total chip area.

This specific charge pump design is based on supplying a load current of 20 μA. With a
load resistance of 250 kΩ (and 150 pF smoothing capacitor in parallel) and a clock
frequency of 2.5 MHz, the output voltage reaches to 5.12 V in steady state condition.
The efficiency of the charge pump circuit itself is measured to be around 77%.

As pointed out before, almost all the conventional charge pump designs are based on
costlier HVT CMOS devices in order to avoid VSR reliability problems. The proposed
topology can be completely implemented with cheaper SLV CMOS processes. This
fully integrated charge pump is strongly believed to be an attractive alternative to charge pumps based on HVT CMOS devices for low and moderate load currents.

7.3 Design limitations

This section concentrates on various design limitations of the proposed charge pump structure. Identifying these limitations is extremely crucial for future improvement of the proposed topology.

7.3.1 ESD protection and external capacitors

The proposed charge pump design with an SLV CMOS process can not use external capacitors instead of the MIM capacitors C1_1, C1_2, C2_1 and C2_2. This is due to the inability of implementing ESD protection at nodes VA, VB, VC and VD. The simplest possible ESD protection scheme is shown in Fig. 7.1. Protections can be implemented with diodes or diode-connected MOS transistors at the node which is to be protected from positive or negative voltage spikes. However, a range of protection elements are commonly used in a modern scheme [56]. Clearly, a scheme based on the one shown in Fig. 7.1 can not be implemented for a successful ESD protection of nodes VA, VB, VC and VD. This is due to the fact that VA and VB alternately swing from 1VDD to 2VDD while VC and VD alternately swing from 2VDD to 3VDD.
When the circuit is operating, a successful ESD protection scheme for nodes VA and VB should operate only after the associated node voltage crosses the 2VDD potential level. Similarly, protection scheme for nodes VC and VD should work only after the associated node voltage crosses the 3VDD voltage level when the circuit operates. Again, when the circuit is not operating, then this requirement will change. Clearly, in this situation, all the ESD protections at these four nodes should be activated as soon as the associated node voltage crosses VDD potential. Stacking of diodes or similar protection devices is not feasible as this arrangement will make the whole protection scheme too slow to respond in an ESD event. Also, it will not provide any ESD protection for voltages below 2VDD (for nodes VA and VB) or 3VDD (for nodes VC and VD) during the times when the circuit is not operating. Therefore, only an unconventional ESD protection scheme with two different levels of protection might allow using external capacitors to increase the charge pumps current delivering capacity. Clearly, this design can not be used for high load applications unless suitable ESD protections at nodes VA, VB, VC and VD are incorporated.
7.3.2 Junction breakdown voltage

An extension of this design with an output voltage of 4VDD has been presented in the appendix C. The structure is expected to work properly in an SLV 1.8 V 0.18 μm CMOS process without violating any VSR reliability constraint as long as the foundry specified junction breakdown voltage between N-well of PMOS transistors and substrate is over the maximum output voltage of the circuit. However, this limitation is quite obvious and is common to all HVT design based on any SLV CMOS processes.

7.4 Potential applications

As mentioned before, this design is based on a load current of around 20 μA for an output voltage of 5.12 V. Therefore, it can be used to interface with standard 5V logic. It might also be possible to implement a complete HVT 5V I/O in SLV CMOS process using this design since clock signals of different voltage levels are readily available in different nodes of the charge pump. However, due to the requirement of on-chip charging capacitors, the topology can only be used to drive low or medium loads (e.g. dynamic gate biasing). For different applications that require such loads, this fully integrated charge pump topology can be used effectively as a cheap alternative to conventional charge pumps designed with costlier HVT CMOS devices.

7.5 Future works

In this design, the supply independent current source helps keeping the voltage gain of the charge pump almost constant. Therefore, the output voltage decreases with decrease in supply voltage. With lower supply voltage, increasing the frequency of the on-chip clock generator can help increasing the voltage gain and keep the output voltage almost
constant. Implementing such a feature is highly desirable for the circuit components which rely on the output of the charge pump.

Efficiency of this design can be significantly improved if the charging capacitors can be made external. This is due to the fact that about 10% of charging currents are wasted through the parasitic components of MIM capacitors. However, as discussed in section 7.3.1, suitable and dynamic ESD protection must be incorporated for external capacitors to protect the gate oxides of MP2_1, MP2_2, M2_3 and M2_4. Designing such an unconventional ESD protection remains the most significant challenge in the improvement of this circuit topology.
Bibliography


Appendix A

More Monte Carlo simulation results

This appendix includes some more Monte Carlo simulation results. Fig. A.1 and Fig. A.2 show MC simulation results of $V_{DS}$ of MP2_1 transistor while Fig. A.3 and A.4 shows MC simulation results of $V_{DS}$ of M2_3. Clearly, VSR reliability restrictions have not been violated in any of the simulation runs.

This appendix also includes MC simulation result of the clock signal at node INVERTED. The result demonstrates that the generated clock frequency remains relatively stable.

![Graph of first six runs of MC simulation of $V_{DS}$ of MP2_1.](image)

Figure A.1: First six runs of MC simulation of $V_{DS}$ of MP2_1.
Figure A.2: Last five runs of MC simulation of \( V_{DS} \) of MP2_1.

Figure A.3: First six runs of MC simulation of \( V_{DS} \) of M2_3.
Figure A.4: Last five runs of MC simulation of V_{DS} of M2_3.

Figure A.5: First six runs of MC simulation on clock signal at node INVERTED.
Figure A.6: Last five runs of MC simulation on clock signal at node INVERTED.
Appendix B

3VDD charge pump layout

Layout of different parts of the 3VDD charge pump circuit is included in this appendix. This complete layout of the 3VDD charge pump circuit is shown in Fig. B.1. The layout measures $600\mu m \times 630\mu m$. The MIM capacitors C1_1, C1_2, C2_1 and C2_2 are placed on four corners with dimensions of $280\mu m \times 280\mu m$. The rest of the circuit is placed between the two MIM capacitor groups. The Supply Independent Current Reference (SICR) is the first circuit block from left. The Current Starved Ring Oscillator (CSRO) is placed between SICS and the charge pump and HVT cells as shown. Layouts of the SICR and CSRO with clock divider are shown in Fig. B.2. and Fig. B.3. Layout of charge pump cells and HVT circuit are also presented in Fig. B.4, Fig. B.5 and Fig. B.6.
Figure B.1: Complete 3VDD charge pump layout with integrated clock generator
Figure B.3: Layout of Current Starved Ring Oscillator
Figure B.4: Layout of the charge pump cells
Figure B.5: Close up view of a part of MP2_1 and MP2_2 layout.
Figure B.6: Layout of the HVT push - pull booster blocks.
Appendix C

4VDD HVT charge pump design

The 4VDD charge pump structure is based on the proposed 3VDD design. Fig. C.2 shows the circuit diagram of this charge pump. The third charge pump cell increases the output voltage by 1VDD only. Gate control signals W and X are generated with the help of diode-capacitor combinations as before. Clearly, voltages at nodes W and X swing from 2VDD to 4VDD alternately. The working principals of MP3_1, MP3_2, M3_3 and M3_4 are similar to MP2_1, MP2_2, M2_3 and M2_4 respectively. Fig. C.1 shows the voltage waveforms at nodes 2VDDOUT, 3VDDOUT and 4VDDOUT.

Figure C.1: Simulation of 2VDD, 3VDD and 4VDD voltages at nodes 2VDDOUT, 3VDDOUT and 4VDDOUT.
In this design, the HVT push-pull I/O block has been re-used to generate additional control signals. This is because of the fact that these control signals need a 2VDD swing just like control signals U and V. Diode chain D5, D6 (and D7, D8) causes a 1VDD voltage drop across it. Hence, the lower voltage level of node voltage W and X is 2VDD. This voltage level is then pushed by 2VDD to produce the desired 4VDD voltage level. Fig. C.3 shows the control signals at nodes U, V, W and X.
Figure C.3: Gate control signals at nodes U, V, W and X. The node names are assigned according to Fig. A.2.

It is clearly seen from Fig. C.4 that VSR reliability restrictions have not been violated in MP3_1, MP3_2, M3_3 and M3_4 transistors.

Figure C.4: V_{GS}, V_{GD}, V_{DS} of MP3_1 and V_{DS} of M3_3. All the waveforms satisfy typical VSR reliability requirements.