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Fabricating Atomically-Abrupt, Surface-Gated Devices in Silicon

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SCHOOL OF PHYSICS

A thesis submitted in fulfilment of the requirements for the degree
Doctor of Philosophy

September, 2011

Declaration of Authorship

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Abstract

This thesis demonstrates the successful development of surface-gated, highly phosphorus-doped single electron transistors, defined by scanning probe lithography and low-temperature silicon molecular beam epitaxy. In order to fabricate these devices, a custom ultra-high vacuum technique was developed to grow silicon dioxide as a gate dielectric at low-temperatures to prevent thermal diffusion of the buried STM patterned dopants. This technique combined atomic oxygen generated using an RF plasma source with a coincident flux of sublimated silicon to grow silicon dioxide at temperatures down to $\sim 160^{\circ}C$ at growth rates of $\sim 0.3 nm.min^{-1}$. Using aluminium electrodes deposited on the dielectric, aligned to our buried STM-patterned dopants, we were able to form atomically-abrupt, surface-gated single electron transistors.

We performed chemical and structural analyses of the low temperature oxide using STM, TEM, XPS, and ellipsometry. These analyses indicated the oxide had low sub-oxide content and a sharp interface with the silicon substrate ($< 1nm$) comparable to high quality thermal oxide control samples. In addition there were no observable crystal defects induced within the underlying silicon, known to enhance dopant diffusion. However, we observed a high density of macroscopic surface defects ($> 1.25 \times 10^{-12} cm^{-2}$) — believed to arise from spitting of silicon particles from the Si cell. These defects created leakage paths in C-V and MOSFET devices and, despite reducing the device size to $\sim 2 \times 10^{-4} cm^2$, inhibited electrical optimisation of the oxide. Nevertheless, electrical characterisation of the oxide was possible for several samples and indicated a trap density of $N_{it} < 4.3 \times 10^{11} cm^{-2}$, consistent with that of un-annealed thermal oxide control samples ($N_{it} < 3 - 6 \times 10^{11} cm^{-2}$).

The low temperature UHV silicon dioxide was then incorporated into a surface gated single electron transistor with ~ 200 P donors, whose small size ($< 1 \times 10^{-8} cm^2$) reduced the likelihood of overlap with macroscopic defects. The results were compared to an in-plane gated SET of the same size, which did not have a surface gate. The surface gated SET showed gating up to electric fields of $1 MV.cm^{-1}$ — exceeding the range of all-epitaxial in-plane gates by around one order of magnitude ($< 0.2 MV.cm^{-1}$). Using the surface gate, we were able to tune the number of electrons on the dot by $\sim 160e$, compared to $30e$ using a comparable in-plane gated device. Low-frequency noise measurements showed similar charge noise using the two gating schemes ($\sigma_{Q_d} = 0.5\%e$ surface gated vs. $0.2\%e$ in-plane gated), however there was severe hysteresis ($4000e$) in the gate action of the surface gated device. These results emphasise the greater tunability afforded by surface gated devices but highlight the need for further improvement of the low temperature dielectric.

Acknowledgements

Normally people use this space to wax lyrical about the exhilarating and rewarding experience as a PhD student. Those of you taking the time to read this know better. Alas, there are many people I would like to thank for making my experience bearable.

Firstly, I would like to thank my PhD supervisor, Michelle. You always believed I could do it, and at times I was less convinced. Thank you for all your effort and positivity over the years, it would have been impossible without you.

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Next I must pay homage to the ghosts of PhD students past: Johnson, Toby, and Frank. Alas, we hardly knew ye. Without your ridiculously hard work, nothing in this thesis would have been possible. Your theses have been holy books to us all. It has been difficult living up to your legacy, but I am glad to have followed in your footsteps.

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In loving memory of my father

List of Publications

D.L. Thompson, W.R. Clarke, M.Y. Simmons. Strong spin-orbit interactions and weak antilocalization in highly disordered p-channel silicon MOSFETs. *In preparation.*

D.L. Thompson, W.R. Clarke, M.Y. Simmons. Determining the underlying disorder potential of percolating metals in disordered 2D systems. *In preparation.*

D.L. Thompson, W.C.T. Lee, S. Shamim, A. Ghosh, M.Y. Simmons. Charge noise in doping-defined SETs. *In preparation.*

W.C.T. Lee, S.R. McKibbin, D.L. Thompson, K. Xue, N. Bishop, M.S. Carroll, M.Y. Simmons. Introduction of strain into atomically precise Si device fabrication. *In preparation.*

W.C.T. Lee, N. Bishop, D.L. Thompson, K. Xue, J. Gray, S. Han, G. Celler, M.S. Carroll, M.Y. Simmons. Thermal processing of strained SOI for atoimcally precise Si device fabrication. *In preparation.*

B. Weber, S. Mahapatra, H. Ryu, S. Lee, A. Fuhrer, T. C. G. Reusch, D.L. Thompson, W.C.T. Lee, G. Klimeck, L.C.L. Hollenberg, M.Y. Simmons. Ohm's law survives to the atomic scale. *Science*, 335(6064):64–67, 2012.

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M.Y. Simmons, F.J. Ruess, W. Pok, D.L. Thompson, M. Fuechsle, G. Scappucci, T.C.G. Reusch, K. Johnson Goh, S.R. Schofield, B. Weber, L. Oberbeck, A.R. Hamilton, F. Ratto. Atomically precise silicon device fabrication. *Proceedings of the 7th IEEE International Conference on Nanotechnology*, pages 907–910, 2007.

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Abbreviations

AFM	Atomic force microscope
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapour deposition
ITRS	International technology roadmap for semiconductors
MBE	Molecular beam epitaxy
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
OED	Optical emission detector
PECVD	Plasma enhanced chemical vapour deposition
RF	Radio frequency
RMS	Root-mean-square
RT	Room-temperature
RTA	Rapid thermal anneal
SET	Single electron transistor
Si**:**P	Silicon doped with phosphorus
STM	Scanning tunnelling microscope
STS	Scanning tunnelling spectroscopy
SUSI	Silicon sublimation source
TEM	Transmission electron microscope
UHV	Ultra-high vacuum
UV	Ultra-violet
XPS	X-ray photoelectron spectroscopy

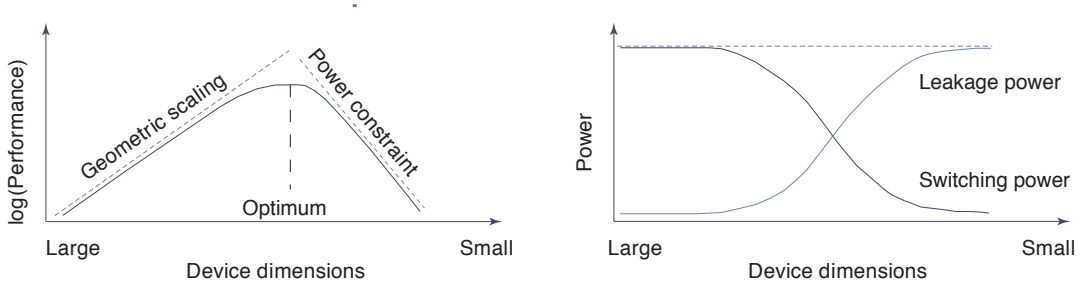
Chapter 1

Introduction

The proliferation of consumer electronics in the mid-20^{th} century sparked a technological revolution, underpinned by the rapid and unrelenting miniaturisation of metal-oxide-semiconductor (CMOS) transistors. Scaling CMOS transistors in this way simultaneously improved their switching speed and reduced their switching energy (as shown in Fig. 1.1(a), reproduced from [1]), making the integrated circuits they formed more computationally capable while dissipating less heat per operation. Heat dissipation is predicted to be one of the key hurdles in continued CMOS scaling, as increased leakage currents (Fig. 1.1(b)) within these ever-smaller devices becomes unmanageable. Each new generation of CMOS technologies aims to extend or circumvent these barriers to scaling, while simultaneously reducing the cost of each component on a chip. This approach has permitted ever more sophisticated circuits to be made over the past five decades, boosting performance through architectural enhancements (depicted in Fig. 1.2(a)), as first published by Gordon Moore in 1965 [2]. Moore's publication showed the cost per transistor decreasing throughout the 1960s, and the resultant growth in the number of components on a chip. This trend has since been dubbed 'Moore's law', and it continues to the present day [3].

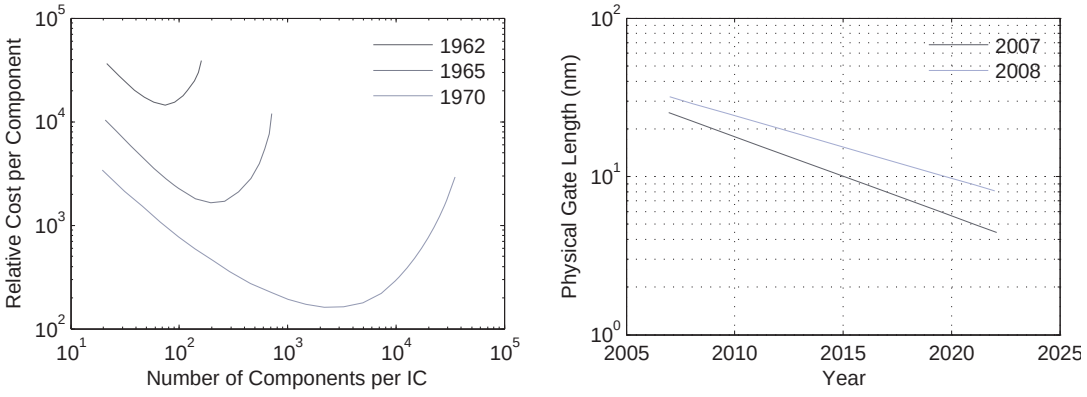
Each new generation of CMOS technologies presents new challenges to continued scaling, tracked by the International Technology Roadmap for Semiconductors (ITRS) [5]. Over the past decade, Moore's law has become increasingly difficult to achieve; Fig. 1.2(b) shows revisions made to the ITRS scaling projections in 2008 as progress slowed [4], where the projected date to reach $10nm$ gate lengths was delayed from 2015 to 2020. For decades, transistors have been scaled according to simple geometric rules, which required source and drain extensions to become shallower, and doping profiles to become increasingly abrupt [6]. In 2009, the ITRS predicted that conventional doping techniques like ion-implantation would cease to achieve sufficiently shallow junctions beyond 2014 [5]. In addition, the ordering and line-edge roughness of doped regions was predicted to play an increasingly important role at gate lengths below $10nm$ [7–9].

It has been suggested that scaling trends may continue for six further CMOS technology nodes, with gate dimensions approaching $5nm$ [4]. As devices approach this scale, continued scaling faces many fundamental physical limits, including the discrete, atomistic



(a) (b)

Figure 1.1: Impact of scaling on CMOS performance and power dissipation. (a) There is an exponential gain in performance as devices are scaled to smaller dimensions with simple geometric (constant field) scaling. The improvement in performance is however limited by power constraints, which gives an optimal device size for peak performance. From Ref. [1]. (b) The static power dissipation of a device increases with scaling, as a result of enhanced leakage currents. The dynamic power of a device decreases with scaling as a result of favourable shifts in the ratio of device capacitance to channel resistance. From Ref. [1].



(a) (b)

Figure 1.2: Scaling trends of CMOS devices. (a) Placing many components on a single chip reduces the cost per component, effectively scaling down fixed costs related to packaging and bonding. Beyond a critical level of integration, the circuit complexity has a severe impact on device yield, increasing the relative cost per functional chip. With improvements to the manufacturing process over time, the optimum number of components on a chip has increased exponentially. From Ref. [2]. (b) Prior to 2008, the ITRS scaling projections were based on devices scaling by a factor of 0.71 every three years. In 2008, this was expanded to 3.8 years. As a result, the projected date to reach physical gate lengths of $10nm$ was delayed from 2015 to 2020. From Ref. [4].

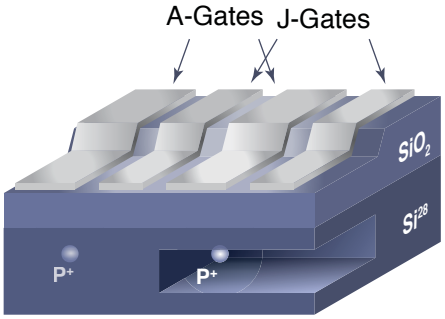


Figure 1.3: Phosphorus-in-silicon nuclear spin qubits. In the original quantum computing architecture proposed by Kane [10], quantum information is encoded into the spin-state of phosphorus nuclei, which are placed in an isotopically pure crystal of spin-free ^{28}Si. Quantum information is exchanged between neighbouring phosphorus atoms using electron-mediated coupling of the nuclear spins. From Ref. [15]

nature of dopants and semiconductor interfaces [8]. However, at these limits new device architectures may emerge with unique applications. In particular, there has been great interest in the quantum nature of semiconductors—specifically in the form of spintronics, single-electron circuits, and solid-state quantum computing [10–14].

Figure 1.3 depicts a solid-state quantum computing architecture in silicon, first proposed by Kane in 1998 [10]. In this architecture, phosphorus donors are placed in isotopically pure ^{28}Si, spaced $\sim 20nm$ apart. Quantum information is represented by the nuclear spin state of the phosphorus nuclei. The advantage of this arrangement is that silicon-28 has zero nuclear spin, allowing the spin of the phosphorus nuclei to remain unperturbed long enough to perform quantum computations. The phosphorus nuclei can exchange spin information with conduction electrons in a controlled way via the hyperfine interaction. The strength of this interaction is proportional to the electron density at the nucleus, which is tuned in Kane's architecture using A-gates situated above each donor. Intervening J-gates are then used to tune the overlap of the conduction electrons with neighbouring donors, which creates tuneable electron-mediated nuclear-spin coupling. The exponential decay of the electron wavefunction overlapping adjacent donors means that coupling between nuclear spin states is exponentially sensitive to their separation. Atomic-scale control in manufacturing is therefore essential for this system to succeed, despite progress recently made towards gating schemes that are somewhat tolerant to donor straggle [16, 17]. Recently this scheme has been adapted by the Centre for Quantum Computation and Communication Technology to consider electron spins rather than nuclear spins of the P atoms [13, 18] with results demonstrating favourable T_1 times

of $\sim 6sec$ [19]. Over the past decade, a complete atomic-scale fabrication scheme has been developed within our group based on the use of a scanning tunnelling microscope (STM) to pattern a single atomic layer of hydrogen as a resist on the silicon surface, in which P dopants are incorporated into the sample using a gaseous dopant source and encapsulated using low temperature molecular beam epitaxy (MBE) [20–23].

Molecular beam epitaxy provides excellent control over the growth of crystalline materials and the resultant interfaces formed within heterogeneous crystal structures. MBE systems are becoming increasingly prevalent in semiconductor processes to fabricate ultra-high mobility devices, particularly for communications applications. Maskless lithographic techniques, such as electron beam lithography, have long surpassed the resolution of optical lithography. Although maskless techniques have been traditionally hampered by low throughput and between-wafer variance, the push for deterministic doping may soon render them economically feasible [24].

In the original quantum architecture proposed by Kane, surface gates are used to control the hyperfine interaction between donors and their bound electrons, and through them the exchange coupling between donors. Kane proposed that silicon dioxide would make a suitable dielectric, but that in the long term it might be necessary to reduce disorder in the system by using epitaxial systems, such as Si-$SiGe$. Several groups are pursuing MOS based quantum dot architectures, tuned to the single electron limit, for use as qubits [25–27], indicating that using silicon dioxide as a dielectric is a realistic approach. Indeed, ^{28}Si and ^{16}O are both zero spin isotopes, and thus a SiO_2 dielectric is a good dielectric to prevent dephasing of P electron spins. Alternatively, Tucker *et al.* have suggested using doped in-plane gate electrodes in quantum electronic devices in which the silicon substrate itself is used as a dielectric [11]. Although this approach has the advantage of maintaining crystallinity of the device [23], it is ultimately limited by the low breakdown field strength of silicon ($< 1MV.cm^{-1}$ [28]). Whilst we have recently demonstrated the use of such STM patterned all-epitaxial in-plane gates, ultimately we will need maximal control of donor states. To this end, in this thesis we aim to demonstrate the incorporation of a low-temperature UHV compatible silicon dioxide dielectric into the atomic-scale fabrication scheme to enable surface-gating of STM-patterned devices.

Thesis outline

This thesis describes the extension of our STM-fabrication scheme in pursuit of surface gated atomic-scale devices. In Chapter 2 we give a theoretical overview of the concepts needed to understand our experimental results. We begin by discussing the use of silicon

as a substrate for nano-scale devices and low-dimensional systems, particularly when δ-doped with phosphorus. We then discuss silicon dioxide as a dielectric for silicon-based devices, focusing on Hall bar MOSFETs, which we use in this thesis as test devices for the oxide, based on the interaction between oxide charges and the mobility of carriers within the induced interface charge. Finally, we discuss the theory of single electron transistors, and the variety of excited states that may be visible within the transport spectroscopy of such devices.

In Chapter 3 we describe the development of a low-temperature oxidation process compatible with the STM fabrication scheme, developed as part of this thesis. In this chapter we describe the decision process that led to using a silicon sublimation source in combination with an oxygen plasma source to form silicon dioxide at low-temperature under ultra-high vacuum. We then describe the development of a dedicated oxide growth chamber attached to our custom STM-SEM system for the low temperature silicon dioxide growth. Next, we describe the chemical and structural analyses of the oxide using STM, TEM, ellipsometry and XPS, where we were able to show that the oxide was indistinguishable from a high quality thermal oxide in terms of sub-oxide content and sharpness of the interface with the silicon substrate, with no visible defects within the oxide. However, we observed a high density of macroscopic surface defects ($> 1.25 \times 10^{-12} cm^{-2}$) using an optical microscope, which we attribute to spitting of silicon particles from the silicon sublimation source. Finally, we performed electrical measurements of the oxide quality, using Hall-bar MOSFETs to assess the mobility of the induced 2DEG. From these measurements we calculate the density of parasitic charges and estimate that the interface trap density is $N_{it} < 4.3 \times 10^{11}.cm^{-2}$, compared with $N_{it} < 3 - 6 \times 10^{11} cm^{-2}$ for un-annealed thermal oxide control samples.

Chapter 4 details the design and analysis of a $\sim$200 donor in-plane gated STM-patterned SET, used to assess the stability and noise of the in-plane gating scheme developed within our group. In this chapter we first give an overview of the current state of the art in silicon SETs, and then discuss previous STM-patterned SETs made within our group. We then describe the design of an in-plane gated SET as a control device to compare with surface gated devices, and how this device was fabricated. Next we describe the electrical performance of this in-plane gated device, including a study of the signatures of tunnel-coupled and capacitively-coupled traps in the transport spectroscopy. Finally, we perform a magnetic field dependence to characterise the excited state features visible in the transport spectroscopy of this device.

In Chapter 5 we demonstrate how we can use the low temperature UHV compatible silicon dioxide dielectric to make a surface-gated STM-patterned SET of a comparable size

to the in-plane gated SET, with ∼200 donors. We perform stability and noise analyses on this device and compare it with the in-plane gated device discussed in Chapter 4. From this we provide a systematic comparison of the performance of the in-plane and surface gating schemes for STM-patterned devices. This chapter concludes with some recommendations for future STM-patterned devices based on the advantages and limitations of each gating architecture.

In Chapter 6 we provide conclusions of the work presented in this thesis, and recommendations for future work based on the progress we have made.

Chapter 2

Theoretical Review

2.1 Introduction

The inversion layer of silicon MOSFETs has been used to explore low-dimensional physics for several decades, an extensive review of which was conducted by Ando *et al.* in 1982 [29]. Since that time, $GaAs$ has become the preferred material system for studying quantum transport phenomena due to continued advancements in the purity and mobility of $GaAs/AlGaAs$ heterostructures. However, much of the knowledge gained from $GaAs$ systems is now relevant to silicon-based devices, especially as quantum effects play an increasingly important role in industrial semiconductor devices.

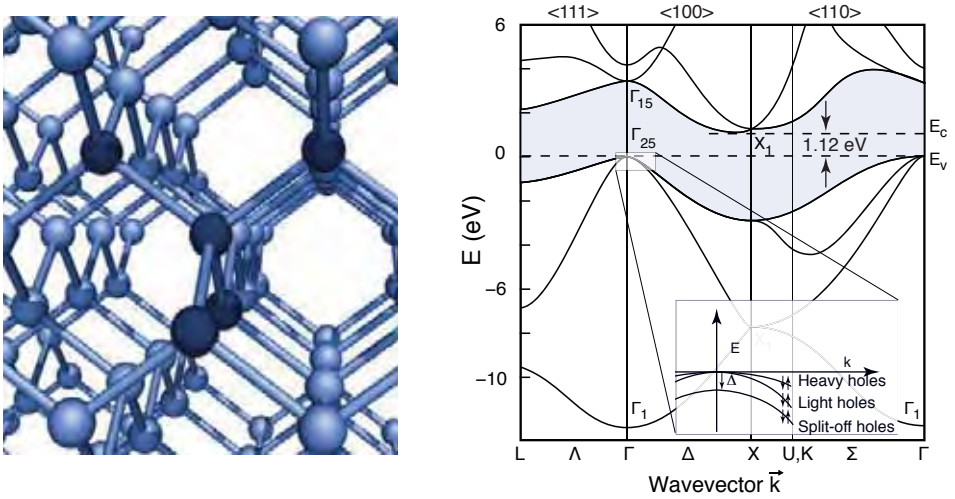
In this chapter we review the relevant theoretical concepts needed for this thesis. We begin with a brief introduction to the electronic and chemical properties of Si and SiO_2, and then discuss the operation of MOS devices. Finally, we discuss the physics of nanoscale surface-gated devices, focussing on transport and noise in single electron transistors.

2.2 Silicon as a basis for quantum electronic devices

Electronic structure of bulk silicon

Silicon is one of the most abundant elements on earth, and accordingly, one of the most commonly used semiconductors. The devices in this thesis are all fabricated on silicon substrates, and for this reason here we discuss the pertinent physical and electronic properties of silicon for our devices, with emphasis on the crystal properties and the resultant band structure.

Silicon atoms have four valence electrons, which form a tetrahedral covalent bond structure in crystalline silicon, as shown in Fig. 2.1(a). This bonding arrangement gives silicon an indirect band gap of $\sim 1.12eV$ at room temperature, as shown in Fig. 2.1(b), with six-fold degeneracy of the conduction band minimum, and four-fold degeneracy of the valence band maximum.

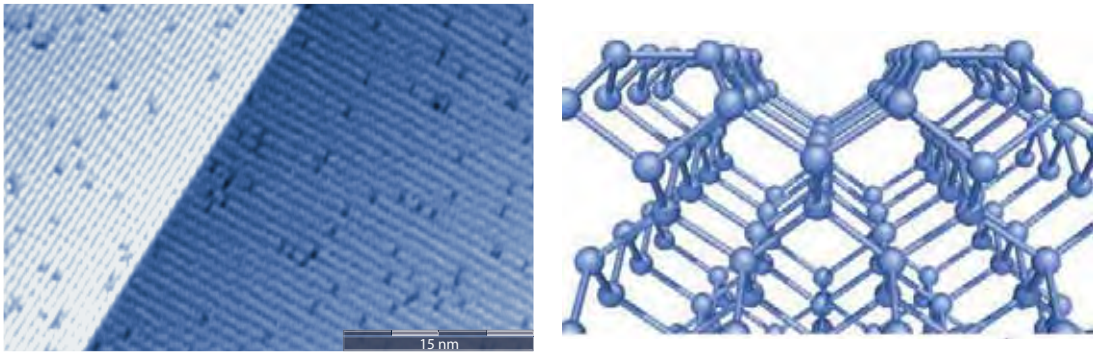


(a) (b)

Figure 2.1: Crystal structure and band structure of crystalline silicon. (a) Silicon forms a tetrahedral covalent bond structure in crystalline silicon. From Ref. [30]. (b) The tetrahedral bond structure gives crystalline silicon an indirect band gap, with a six-fold degenerate conduction band minimum and a four-fold degenerate valence band maximum. From Ref. [31]

The valence band maxima at the Γ point are p-like states, which are affected by spin-orbit coupling phenomena that are not present in the s-like states of the conduction band minima. Without consideration of spin, the valence band maximum would be three-fold degenerate ($l = 1$). When we include spin, the spin-orbit interaction splits this degeneracy into a four-fold degenerate state with total angular momentum $j = 3/2$ and a two-fold degenerate split-off state with $j = 1/2$ situated at an energy $\Delta = 44meV$ below the $j = 3/2$ states. The four degenerate states at the Γ point have both differing vertical components of the total angular momenta, and differing spins — designated as spin-up and spin-down light holes ($m = \pm 1/2$), and spin-up and spin down heavy holes ($m = \pm 3/2$). The split-off bands have $m = \pm 1/2$, resulting in the valence band structure shown schematically in the inset of Fig. 2.1(b).

The spin degeneracy of all bands is broken in a magnetic field by the Zeeman effect, giving an energy splitting of $E_z = \pm s_z g \mu_B B$, where s_z is the vertical projection of the particle spin ($\pm 1/2$), g is the gyromagnetic ratio ($\sim$2 in silicon), B is the magnetic field, and μ_B is the Bohr magneton $\mu_B = \frac{q_e \hbar}{2m_e}$. The conduction and valence band degeneracy can also be broken by confining carriers to a two or one-dimensional quantum well, which breaks the band symmetry.



(a) (b)

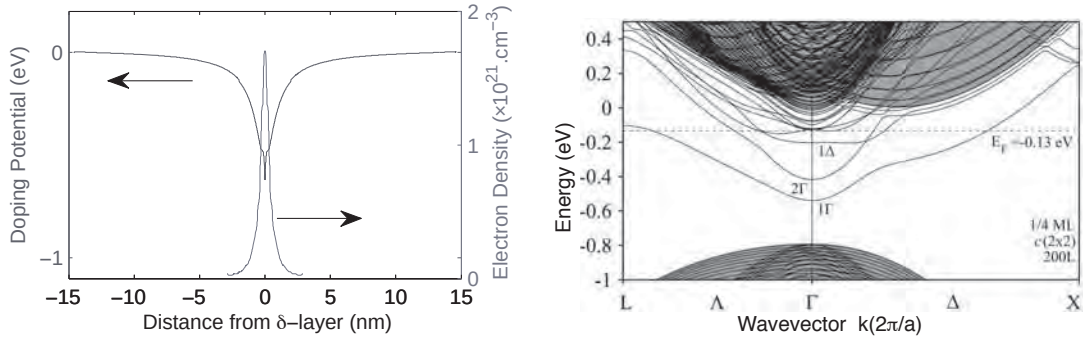
Figure 2.2: The Si(001) 2×1 surface reconstruction. (a) Filled state STM image of the (2×1) reconstruction of the silicon surface taken at $V_{tip} = -2.1V$ and $I_{tip} = 0.75nA$. (b) Ball and stick model showing the buckling of the surface atom bonds to form dimer rows. Reproduced from Ref. [30]

The proximity of the light-hole, heavy-hole and split-off bands causes a strong non-parabolicity in these bands around $k = 0$, making an effective mass approximation invalid in this region of k-space. Since the valence band states are a result of spin-orbit coupling, their spin degeneracy is also split by an external electric field via the Rashba effect, in which the asymmetry of the nuclear potential in the presence of an external electric field alters the degree of spin-orbit splitting created by this potential [32].

The Si (100) surface

Silicon atoms within a (100) plane of crystalline silicon form covalent bonds with the two neighbouring atoms in the plane immediately above, and two bonds with atoms in the plane below. Atoms at the surface in the (100) orientation therefore have two unsaturated bonds extending out from the bulk. In a vacuum, the lowest energy configuration is for the surface to reconstruct so that these dangling bonds mate with those of adjacent surface atoms. This forms silicon dimers bound by a strong σ bond (Si-Si), with the small amount of overlap between the remaining dangling bonds giving rise to an additional weak π bond. The lowest energy configuration is for the dimers to transfer charge from one atom to another, buckling the dimer on the surface, though this charge transfer occurs dynamically between the two atoms, making the effect invisible unless the sample is cooled to cryogenic temperatures and we resolve only the averaged structure. This relatively unstable and high-energy bond configuration makes the silicon surface highly reactive.

In practice the cleaving of the silicon surface is often slightly misaligned with the (100)



(a) (b)

Figure 2.3: Electron confinement in δ-doped silicon (a) The Coulomb potentials of ionised donors in the δ-doped layer combine to form a sharp potential well, confining the conduction electrons within this layer to a width of $\sim 2nm$. Adapted from [33]. (b) Density functional theory modelling of the δ-doped system shows that the Fermi level of the δ-layer is offset by $130meV$ from the conduction band edge of bulk silicon. From [33]

orientation (e.g. 0.2°), giving rise to a terraced structure on the surface in which the dimer rows are oriented in one direction on the upper terrace, and at a perpendicular orientation on the lower terrace; this effect is shown in the scanning tunnelling microscope image of Fig. 2.2(a), in which the upper terrace is brighter. To relate this image to the crystal structure, Fig. 2.2(b) shows the rows of dimers (upper most atoms) separated by a vertical step, it is these protruding rows that are visible in Fig. 2.2(a). The vertical step from one terrace to the next is determined by the separation between each monolayer, which is $a/4$ where $a = 5.43\mathring{A}$ is the lattice constant, giving $1.36\mathring{A}$. The lateral separation between dimer rows occurs across the diagonal of a unit cell, giving a separation of $\sqrt{2}a = 7.68\mathring{A}$.

Delta-doped silicon

Doping silicon with phosphorus gives an excess of free (extrinsic) electrons, created when the donors are ionised. If the donor atoms are arranged with sufficient density ($> 10^{13}.cm^{-2}$) in a single atomic plane (i.e. a δ-doping profile), the extrinsic electrons are confined to the Coulomb potential generated by the ionised phosphorus nuclei. This δ-doped system has been studied extensively by our group [34–40], and modelled using density functional theory by Carter *et al.* [33], giving the electron concentration profile shown in Fig. 2.3(a), with the associated band structure shown in Fig. 2.3(b). The full-width half-maximum of the electron density is less than one nanometre ($x = 0.67nm$), extending to $2nm$ for $\rho = \rho_{max}/10$ [33]. From the band diagram in Fig. 2.3(b), we see that the δ-layer Fermi level is $130meV$ below the bulk conduction band edge, giving several occupied sub-bands at equilibrium (1Γ, 2Γ, and the four-fold degenerate 1Δ). For this reason, the δ-doped

system remains highly conductive at cryogenic temperatures, and the interface it forms with the silicon bulk can be treated as a Schottky contact.

2.3 Silicon dioxide as a gate dielectric

Growth of silicon dioxide

Silicon dioxide forms naturally when silicon is exposed to an oxygen-containing ambient. The reaction between oxygen and silicon occurs readily at room temperature; however the formed oxide is typically limited to 1–2nm thick as the newly-formed oxide layer inhibits further oxidation. For this reason, silicon dioxide is typically grown in a furnace at high temperatures in order to diffuse oxygen through the formed oxide (typically 800–1000°C), in accordance with the Deal-Grove model [41]. Despite the existence of several crystalline forms of silicon dioxide — including quartz, cristobalite, and tridymite — there are no crystalline configurations with a lattice constant compatible with silicon. As a consequence, the oxide that forms on silicon is amorphous. As such, defects within the oxide can form because of localised non-stoichiometry during the formation of silicon dioxide.

Oxide defects

The nomenclature of silicon dioxide defects is based on their location and behaviour within the oxide, illustrated in Fig. 2.4:

Oxide trapped charge arises from traps distributed throughout the oxide, typically caused by radiation damage, that can be populated or depopulated by charge flowing through the oxide.

Fixed oxide charge is the constant (typically positive) charge that builds up within the oxide near the Si–SiO_2 interface as a result of non-stoichiometry of the oxide in this region.

Interface trapped charge refers to charge traps at the interface that populate/depopulate based on the local chemical potential at the surface.

Mobile ionic charge refers to mobile ions (typically light group-I ions such as K^+ and Na^+) that drift through the oxide under an applied electric field.

Oxide defects interact with charge carriers in semiconductor devices, particularly those confined to the silicon/silicon-dioxide interface, which has a detrimental impact on device

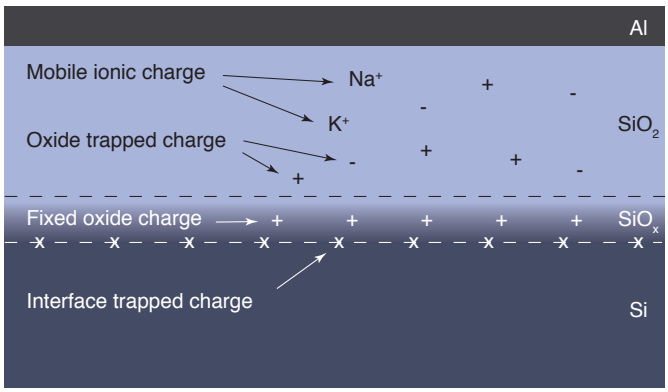


Figure 2.4: Parasitic charges within a silicon dioxide layer on a silicon substrate. The lattice constant of crystalline silicon is incompatible with all crystalline forms of silicon dioxide, so that all silicon dioxide layers formed on a silicon substrate are amorphous. This causes many parasitic charges to form within the oxide at the interface with the silicon substrate. Adapted from Ref. [42, pg. 129]

performance through Coulombic scattering and carrier trapping/de-trapping processes. Interface trapped charge and mobile ionic charge contribute to the device capacitance (though the effect of the ionic charge is transient); whereas fixed oxide charge and oxide trapped charge manifest as an offset in the effective gate voltage.

Oxide defects can be minimised under controlled growth conditions using high-temperature ($> 900°C$) post-oxidation annealing in an inert ambient (minimising fixed oxide charge), in combination with low-temperature annealing in the presence of hydrogen (minimising interface trapped charge). Importantly, both defects are less prevalent when the oxide is formed on the $Si(100)$ surface [43, 44], which is the crystal orientation used for devices in this thesis. To minimise mobile ionic charge, it is imperative that oxides are formed in a clean environment, in particular free of light metal ions such as Na^+ and K^+.

Under optimised growth conditions, and following post-oxidation and post-metallisation anneals, it is possible to form gate oxides with an interface trap density of $N_{it} \simeq 10^{10}.cm^{-2}.eV^{-1}$ and a fixed oxide charge on the order of $N_f = 10^{10}.cm^{-2}$, with negligible oxide trapped charge and mobile ionic charge [42, pg. 128–131].

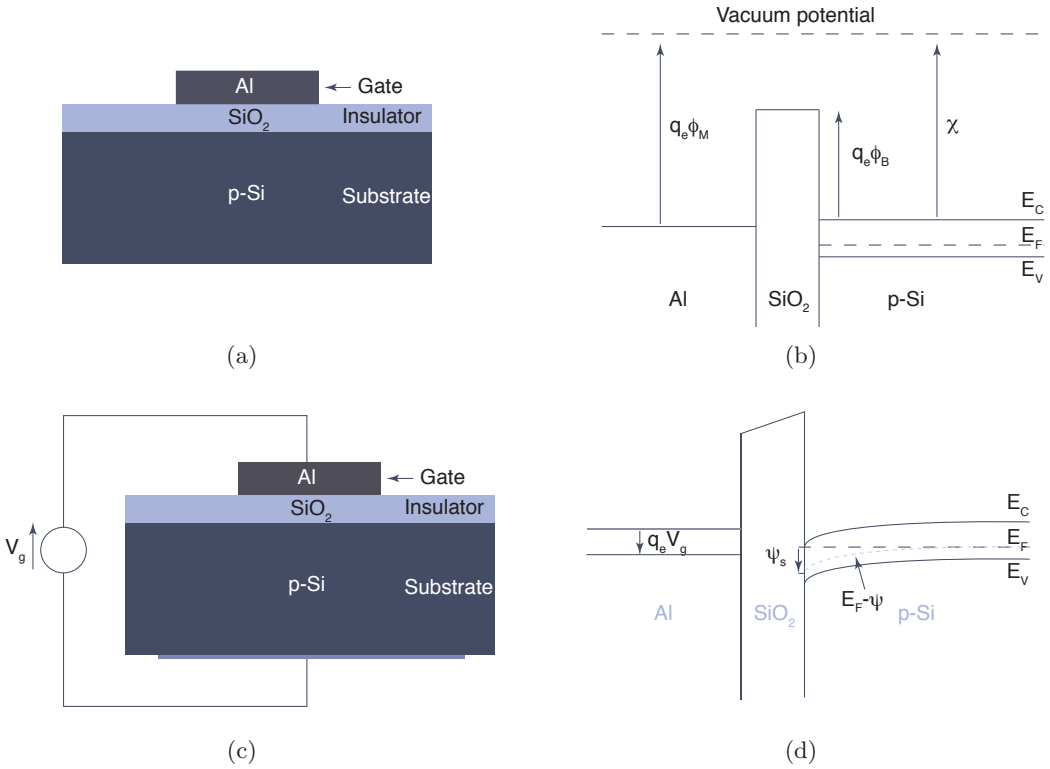


Figure 2.5: Inducing a space charge at the silicon/silicon-dioxide interface. (a) Profile view of a simple MOS system comprising an aluminium gate patterned on silicon dioxde on a silicon substrate. (b) The associated band diagram of (a) at flat-band conditionss. (c) Circuit used to induce a space charge at the Si–SiO_2 interface. (d) Band diagram showning the bending of the silicon bands under the application of a gate bias.

2.4 Metal-oxide-semiconductor devices

2.4.1 MOS capacitors

Inducing a space charge in MOS devices

The simplest metal-oxide-semiconductor device is the MOS capacitor, which consists of two electrodes, at least one of which is a semiconductor, separated by a dielectric; an example of which shown in profile in Fig. 2.5(a), with the associated band diagram shown in Fig. 2.5(b). The conductance band offset between the p-Si electrode and the SiO_2 insulator generates a potential barrier, preventing the flow of charge; the value of this barrier, ϕ_B, is determined by the respective material work-function (ϕ) and electron affinity (χ), measured relative to the vacuum potential.

Applying a positive bias to the surface gate, as shown in Fig. 2.5(c), generates an electric field within the SiO_2 layer, which creates a proportional field at the interface

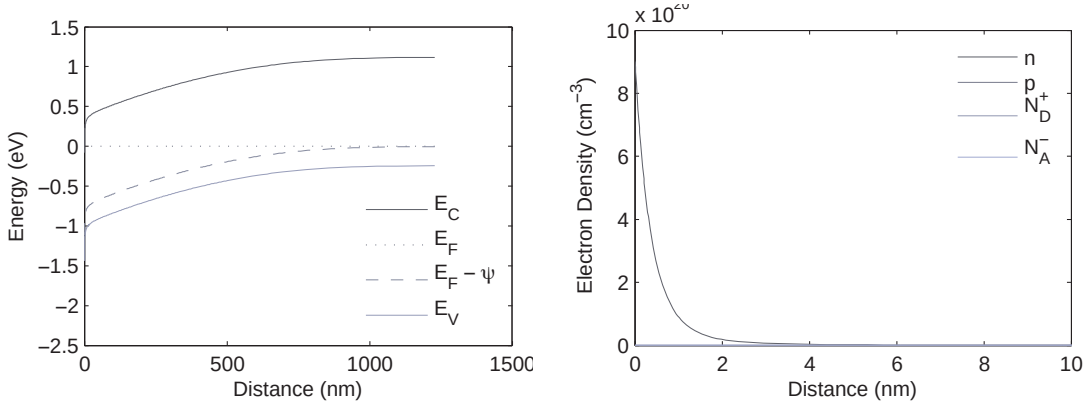
with the silicon substrate (scaled by the insulator/substrate dielectric constant). This field redistributes charges within the substrate so that the field is eventually nullified deep within the substrate bulk, as shown in Fig. 2.5(d). The resultant deviation of the silicon bands, ψ, from their equilibrium value at position x is given by Poisson's equation

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{e}{\epsilon_s}\left(N_D^+ - N_A^- + p - n\right), \tag{2.1}$$

where e is the charge of an electron, ϵ_s is the permittivity of silicon, and N_D^+, N_A^-, p, and n are the ionised donor and acceptor concentrations, and free hole and electron concentrations, respectively, which are themselves dependent upon ψ through the Fermi distribution (see e.g. [42, pg. 133]). We can thus solve numerically for ψ as a function of x, which gives the associated band bending for a given applied field. We show the results of a numerical simulation in Fig. 2.6(a) for a p-type substrate (B-doped to $10^{15} cm^{-3}$). From this model we see that when $\psi \simeq +E_g/2$, the surface goes into inversion, in which there is an excess of free electrons at the interface, as shown in Fig. 2.6(b) ($n > N_D^+ - N_A^- + p$); similarly when $\psi \simeq -E_q/2$, the surface will go into accumulation, in which case there is an excess of free holes at the surface ($p > N_D^+ - N_A^- - n$). In both cases, excess charge carriers near the Si–SiO_2 interface create a conductive two-dimensional layer. In the intermediate case ($\psi \simeq 0$) the system is in charge equilibrium ($N_D^+ - N_A^- + p - n = 0$), giving few free charge carriers at the interface; in this condition the silicon gives an insulating 'depletion capacitance' that acts in parallel with the oxide capacitance. By intentionally forcing the interface into accumulation, depletion, or inversion using the surface gate, we can tune the density of charge carriers at the Si–SiO_2 interface.

Quantifying the density of oxide charges using a MOS capacitor

For a p-type substrate, holes are generated by ionising acceptors, a process that occurs rapidly ($\tau = 1ps$ to $1\mu s$), so that the substrate can be treated as permanently in thermodynamic equilibrium. Conversely, when the surface is biased into inversion, free electrons are generated from thermal or optical excitation of electron-hole pairs, which adds a frequency-dependence to the capacitance of the MOS structure. We can measure the frequency-dependent capacitance of the structure as a function of the applied DC gate bias under quasi-static (QS) conditions and at high frequency (HF). An example C-V measurement of this type is shown in Fig. 2.7(a) for a circular capacitor with a radius of $265\mu m$, using a p-type substrate and nominally $50nm$ thermally-grown oxide, which has undergone a post-metallisation anneal. The measurement was conducted in collaboration with Dr. Greg Ten Eyck of Sandia National Laboratories.



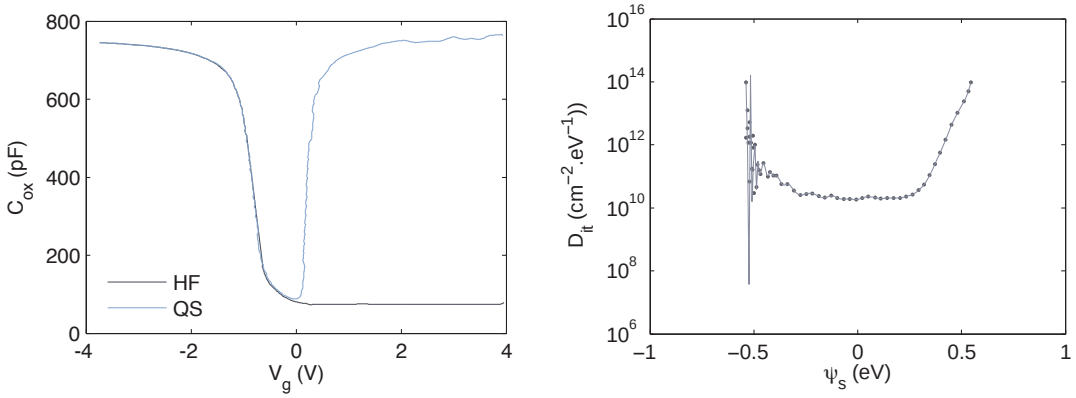
(a) (b)

Figure 2.6: Simulation of induced carrier density in a MOS system (a) Induced band bending under the action of an applied gate voltage (b) Induced carrier density corresponding to the band diagram shown in (a).

When the MOS capacitor is biased into accumulation (left side of Fig. 2.7(a)), charging and discharging of the MOS capacitor occurs via majority carriers, which are able to respond sufficiently quickly to match the high-frequency excitation.

As the gate of the MOS capacitor is swept towards $-0.5V$, the carriers at the silicon/silicon-dioxide interface begin to deplete. This creates a region between the interface and the bulk that is nearly free of charge carriers, which acts as an insulator in series with the gate capacitance, causing the total capacitance of the structure to drop. As the capacitor is further biased towards inversion ($\sim 1V$), the depletion region narrows and the QS capacitance returns to the previous value. However, now that the structure is inverted, conduction is dominated by minority carriers. These carriers must be generated by thermal or photon scattering events (which create an electron-hole pair), which occur relatively infrequently, depending on the temperature or illumination of the substrate. As such, the minority carrier response time is not sufficient to match the AC excitation, so that the interface remains essentially depleted for the HF measurement.

In the region between accumulation and inversion, the slowly-generated minority carriers play little role in substrate conduction; however, there are comparatively faster interface traps within this region that contribute to the measured capacitance. There is still a time-delay associated with charge transfer to the trap, which causes a discrepancy between the HF and QS curves [43]. One can therefore extract a measure of the interface trap capacitance in the depletion and weak inversion regime by subtracting the HF



(a) (b)

Figure 2.7: C-V Measurements of the oxide (a) C-V measurements of a thermal oxide control sample show the expected behaviour; the quasi-static capacitance drops when the structure is biased into depletion and the HF capacitance remains at or below the depletion capacitance in the inversion region. (b) Calculated interface trap density as a function of surface potential from the C-V measurements in (a).

capacitance from the QS measurement.

$$C_{it} = \left| \left(\frac{1}{C_{QS}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right| \tag{2.2}$$

Scaling this capacitance by the gate area and the elemental charge (assuming that a trap consists of a single electronic state) therefore gives a measure of the interface trap density (D_{it}) as a function of the gate voltage (V_g)

$$D_{it}(V_g) = \frac{C_{ox}}{eA} \left(\frac{C_{QS}(V_g)}{C_{ox} - C_{QS}(V_g)} - \frac{C_{HF}(V_g)}{C_{ox} - C_{HF}(V_g)} \right). \tag{2.3}$$

The corresponding surface potential can be calculated from the gate voltage by subtracting the flat-band voltage and the potential drop across the oxide. In this way we can calculate the interface trap density as a function of the surface potential within the band gap.

The minute differences between the HF and QS curves of Fig. 2.7(a) is visually imperceptible at the plotted scale, but it is this difference that gives the measured interface trap density shown in Fig. 2.7(b); as a consequence, the sensitivity of C-V measurements is limited to around $D_{it} = 10^9 cm^{-2}.eV^{-1}$. The measurements shown in Fig. 2.7(b) indicate a mid-gap trap density of $D_{it} \simeq 3\text{–}5 \times 10^{10}.cm^{-2}.eV^{-1}$.

Both HF and QS measurements of capacitance are sensitive to leakage through the oxide. In the case of the QS measurement, the curve is constructed from the gate charging current and therefore shows a large offset when the gate leakage current is comparable to

the capacitor charging current. The HF measurement extracts the capacitance from the portion of the AC gate current that is 90° out of phase with the AC excitation voltage. Since the leakage current of a MOS structure increases exponentially with the applied bias, the leakage creates harmonics of the applied AC signal in the capacitor leakage current, which contribute to the measured current 90° out of phase with the AC excitation. This effect is small, and as a consequence, alterations to the HF curve are more subtle and so the measured HF capacitance is more reliable than the QS value. As we will show in Chapter 3, the C-V measurements of our samples were hindered by leakage through the oxide, which prevented us from extracting a reliable measurement of the interface trap density.

2.4.2 Classical transport through long channel MOSFETs

The long channel approximation

We can inject a current into the induced layer of MOS systems using source and drain leads. When the source and drain are spaced sufficiently far apart ($> 1\mu m$), there is little capacitive coupling between them, and we can approximate the device as a long-channel MOSFET. In the long-channel approximation at low source-drain biases, we can treat the induced two-dimensional layer at the Si–SiO_2 interface as a uniform sheet of charge of density n_s with a fixed effective mobility μ_{eff}. In this way, we can calculate the expected resistance of the induced layer as

$$R_{sd} = \frac{L}{W}\mu_{\text{eff}} n_s \tag{2.4}$$

where L and W are the length and width of the induced region, respectively. The induced carrier density scales in proportion to the applied gate bias, as for any capacitor, but here there is an offset in the induced carrier density determined by the 'threshold voltage', which is the applied gate voltage at which the structure begins to invert or accumulate, according to the relation

$$n_s = C_{ox}(V_g - V_t) \tag{2.5}$$

where C_{ox} is the capacitance of the gate per unit area, V_g is the gate voltage, and V_t is the threshold voltage. In reality, the mobility also varies with the applied gate voltage — firstly as induced carriers screen out Coulombic scattering centres (increasing the mobility), and then as carriers are drawn closer to the interface (decreasing the mobility through surface-roughness scattering). When the carrier density is sufficient for free carriers to shield the

Coulombic scattering centres, the mobility increases. The 'critical density' at which the increase begins gives an estimate of the interface trap density of the oxide, since interface traps act as Coulombic scatterers. We use this effect in Chapter 3 to quantify the density of interface traps in our oxide.

2.5 Single electron transistors

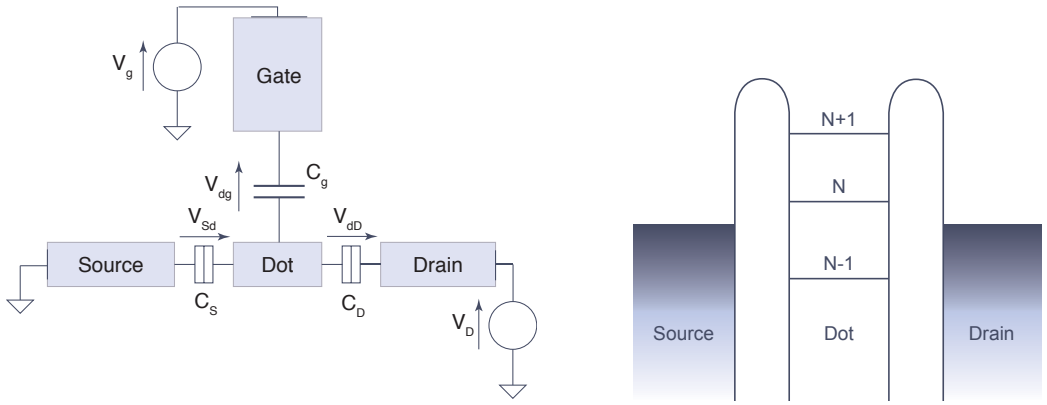
In Chapter 4 and Chapter 5 we analyse the electrical characteristics of STM-patterned single electron transistors. A single electron transistor is a three terminal device in which electrons pass sequentially between two terminals (from source to drain), and this flow can be controlled over several orders of magnitude simply by applying a small charge to the third (gate) terminal. Discrete electronic states arise within a single electron transistor (SET) as a consequence of Coulombic repulsion between like charges confined within a very small metallic island, carefully placed between the source and drain electrodes. Importantly, we can accurately model the energy of these single particle states using the 'constant-interaction model', in which the various conductive elements within the device are treated as metallic, the capacitive coupling between them remains fixed, and the energy separation between electronic states on the island is constant. In this section we first describe the constant interaction model, and then discuss corrections necessary to account for quantum phenomena in our atomic-scale devices. In particular, we discuss the behaviour expected in our ∼200 donor quantum dots, which are connected to 1-D source and drain leads. Several different excited state spectra are observed in these devices, and here we describe how to distinguish between these effects.

2.5.1 Classical energy quantisation in single electron transistors

The constant interaction model

Let us first consider the canonical single electron transistor shown in Fig. 2.8(a), which consists of an isolated metallic dot that is capacitively coupled to a metallic gate, and tunnel-coupled to metallic source and drain electrodes (the intervening regions are insulating). Tunnel-coupling is achieved when the geometric separation between two conductors is small enough for electrons to tunnel through the intervening insulator, but not close enough for Ohmic conduction to occur.

Figure 2.8(b) shows the band diagram of an SET including the source, dot, and drain



(a) (b)

Figure 2.8: Canonical model of an SET consisting of gate, source, and drain electrodes coupled to a central dot. (a) Schematic of a canonical SET layout, showing capacitive coupling between the gate and dot, C_g, and tunnel-coupling between the source and drain reservoirs and the dot (C_S and C_D). (b) Schematic band diagram of a canonical SET showing a continuum of states in the source and drain reservoirs and discrete states within the dot.

electrodes. The source and drain electrodes are treated as metallic reservoirs, with a uniformly distributed density of states filled to the Fermi level. The dot is also treated as metallic, but here the small size of the dot gives it a very small capacitance, and so Coulombic repulsion between like charges on the dot results in an appreciable separation in energy between each electronic state (because $\Delta E \propto 1/C$). In this section we quantify this energy separation and the necessary gate and drain voltages required to populate the dot states.

Consider the case when the tunnel barriers are infinitely resistive, preventing the electron occupancy of the dot from changing. We may induce a continuously-variable potential on the dot via capacitive coupling to the gate, source, and drain electrodes; for example, if we apply a drain bias V_D (with the gate grounded), some of this potential energy will be dropped across the dot-drain gap (V_{dD}), and the remainder across the parallel combination of the source-dot and dot-gate gaps (since the source and gate are grounded, and thus in parallel). The source-dot and dot-gate voltages must be equal and opposite, according to the sign conventions shown in Fig. 2.8(a) ($V_{Sd} = -V_{dg}$), such that:

$$V_D = V_{dD} + V_{Sd} = V_{dD} - V_{dg} \tag{2.6}$$

The relative magnitude of these voltages is determined by the capacitor divider rule, which states that the fraction of the voltage dropped between two circuit nodes is given by the capacitance between all other nodes, relative to the total capacitance,

$$V_{dD} = V_D \frac{C_S + C_g}{C_\Sigma}; \quad V_{Sd} = -V_{dg} = V_D \frac{C_D}{C_\Sigma} \tag{2.7}$$

where we have introduced the notation $C_\Sigma = C_D + C_S + C_g$. Equally, we could apply a bias to the gate with the source and drain grounded, giving

$$V_{dg} = V_g \frac{C_S + C_D}{C_\Sigma}; \quad V_{Sd} = -V_{dD} = V_g \frac{C_g}{C_\Sigma} \tag{2.8}$$

Thus, by the principle of superposition, for an arbitrary gate or drain bias we have (see e.g. [45])

$$\begin{aligned} V_{dg} &= V_g \frac{C_S + C_D}{C_\Sigma} - V_D \frac{C_D}{C_\Sigma} \\ V_{Sd} &= V_g \frac{C_g}{C_\Sigma} + V_D \frac{C_D}{C_\Sigma} \\ V_{dD} &= -V_g \frac{C_g}{C_\Sigma} + V_D \frac{C_S + C_g}{C_\Sigma} \end{aligned} \tag{2.9}$$

The total charge induced on the dot from each of these external electrodes is given by $Q_x = C_x V_{dx}$ for $x = S, D, g$, so that the total dot charge is

$$\begin{aligned} \Delta Q_d &= \Delta Q_S - \Delta Q_D - \Delta Q_g \\ &= C_S \left(\Delta V_g \frac{C_g}{C_\Sigma} + \Delta V_D \frac{C_D}{C_\Sigma} \right) ... \\ &\quad -C_D \left(-\Delta V_g \frac{C_g}{C_\Sigma} + \Delta V_D \frac{C_S + C_g}{C_\Sigma} \right) ... \\ &\quad -C_g \left(\Delta V_g \frac{C_S + C_D}{C_\Sigma} - \Delta V_D \frac{C_D}{C_\Sigma} \right) \\ &= 0 \end{aligned} \tag{2.10}$$

Note that, by the sign convention we have chosen for the voltages in Fig. 2.8(a), ΔQ_S is positive whereas ΔQ_D and ΔQ_g are negative. From Eq. 2.10 we see that although the dot has a continuously variable potential using V_D and V_g, the total number of electrons on the dot must remain constant, since there is no path for electrons to pass to or from the dot. Suppose now that we give the source and drain tunnel barriers some finite resistance, such that electrons can flow into and out of the dot. We define the number of electrons on the dot at equilibrium ($V_{g,D} = 0$) as N_0, and the number of electrons on the dot under

all other conditions as N. The presence of non-equilibrium charges on the dot induces a potential difference between the dot and each of the three terminals (when $V_{g,D} = 0$), given by

$$V_{dg} = -V_{Sd} = V_{dD} = \frac{e(N - N_0)}{C_\Sigma} \tag{2.11}$$

There a few things to note here: (1) the difference in sign between V_{Sd} and $V_{dg,dD}$ is a continuation of our sign convention; (2) the potential difference arises from the classical capacitor relation $V = Q/C$, where here $Q = -e(N - N_0)$; (3) a finite potential is induced only when we change the electron occupancy from the equilibrium condition (i.e. $N \neq N_0$); (4) this charge buildup is negative relative to the source terminal, since it consists of N electrons, which have a negative charge. Considering Eq. 2.9, the voltage of the dot relative to ground (V_{Sd}, since the source is always grounded) for finite gate and drain biases is therefore

$$V_{Sd} = V_g \frac{C_g}{C_\Sigma} + V_D \frac{C_D}{C_\Sigma} - \frac{e(N - N_0)}{C_\Sigma} \tag{2.12}$$

Since we have formed an accumulation of like charges, there will be an inherent repulsion between these charges, which requires that some finite amount of energy is paid to place an additional electron on the dot. Under the constant interaction model, we model the dot potential for N electrons using Eq. 2.12 as

$$\begin{aligned} \mu_d(N) &= -eV_{Sd}(N) + \mu_d(N_0) \\ &= -\frac{e}{C_\Sigma}\left(C_g V_g + V_D C_D - e(N - N_0)\right) + \mu_d(N_0) \end{aligned} \tag{2.13}$$

where $\mu_d(N)$ is the dot potential, $\mu_d(N_0)$ is its value at equilibrium, and both of these potentials are defined as the potential energy of an *electron*, which has negative charge thus inverting it's sign for positive voltages. The potential difference between the N and $(N + 1)$ electronic states on the dot is thus

$$\begin{aligned} \mu_d(N+1) - \mu_d(N) &= \frac{e^2(N + 1 - N_0)}{C_\Sigma} - \frac{e^2(N - N_0)}{C_\Sigma} \\ &= \frac{e^2}{C_\Sigma} \end{aligned} \tag{2.14}$$

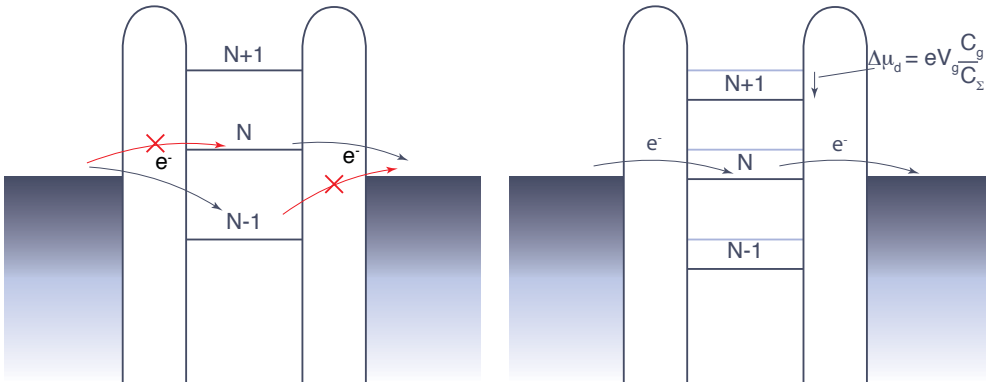
We refer to this as the charging energy, E_c, of the dot, though it differs from the classical definition of the energy, E_{Cl} required to charge a capacitor, which is given by

$$\begin{aligned} E_{Cl} &= \frac{1}{2}C_\Sigma V_{Sd}^2 \\ \text{where } V_{Sd} &= -\frac{e(N-N_0)}{C_\Sigma} \\ \Rightarrow E_{Cl} &= \frac{e^2}{2C_\Sigma} \end{aligned} \tag{2.15}$$

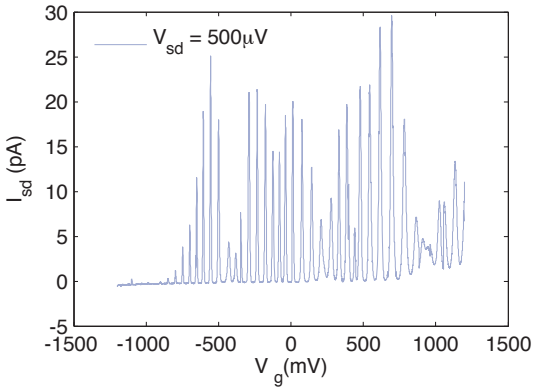
for the first electron ($N - N_0 = 1$). The reason we define the charging energy $E_c = \frac{e^2}{C_\Sigma}$ using the potential difference between electronic states is that it is a convenient unit when considering the necessary conditions for transport through the dot, as expressed by Kouwenhoven *et al.* [46, pg. 368]. Let us now consider electron transport through the dot in what is known as the 'linear response regime', where $eV_D \ll E_c$. In this case, the dot potential is

$$\mu_d(N) \simeq -\frac{e}{C_\Sigma}\left(C_g V_g - e(N-N_0)\right) + \mu_d(N_0) \tag{2.16}$$

where the source and drain potentials are $\mu_S = 0$, $\mu_D = -V_D$. Here we shall assume that $N_0 = (N-1)$, giving the band diagram shown in Fig. 2.9(a). Notice that in general $\mu_d(N_0) \neq 0$, so with the gate voltage grounded, the dot potential does not equal the source potential. In the case shown in Fig. 2.9(a), there is no way for the electron in the $(N-1)$ state to tunnel out to the drain, since it does not have enough energy as shown by the right-side red arrow, and there is no way for a source electron to tunnel into the N state, since the source electrons do not have enough energy, shown by the left-side red arrow. Thus, under this condition, no current will pass through the dot — an effect known as Coulomb blockade. Now, according to Eq. 2.16, it is possible to add an arbitrary potential $\Delta\mu_d$ to the dot using the gate bias V_g, and so we can tune the level N to be at the same energy as source and drain, as shown in Fig. 2.9(b). In this case, electrons can tunnel sequentially from the source to state N, and from this N state to the drain, allowing a source-drain current to flow. If we increase the gate further still, the state N is no longer in resonance, and the current is again blockaded. As we continue to increase the gate voltage, each time we pull a state $(N+1, N+2, N+3, ...)$ into resonance with the source and drain terminals, a current flows. If we plot the source-drain current (I_{SD}) versus the gate voltage (V_g) we see a series of sharp peaks in the current, which occur when the energy level on the dot is in resonance with source and drain; and because of Coulomb blockade, we see no current elsewhere. This is shown in Fig. 2.9(c); note the peaks have a

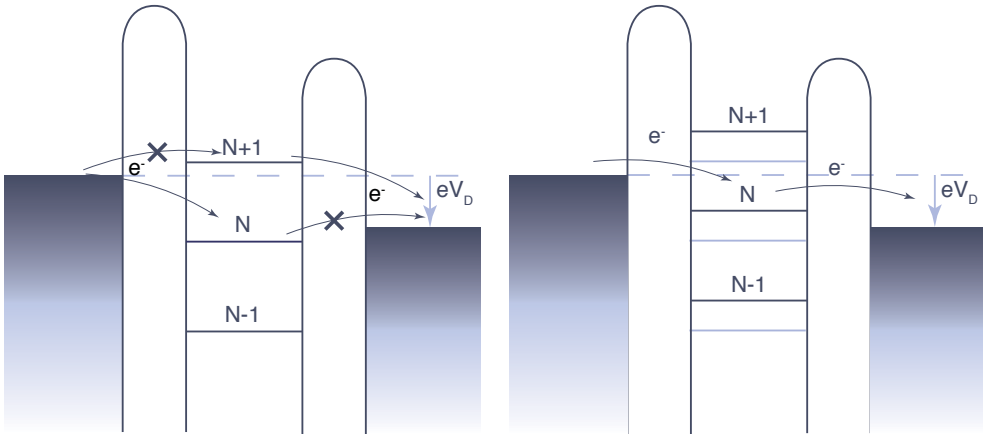


(a) Blockaded (b) Resonance

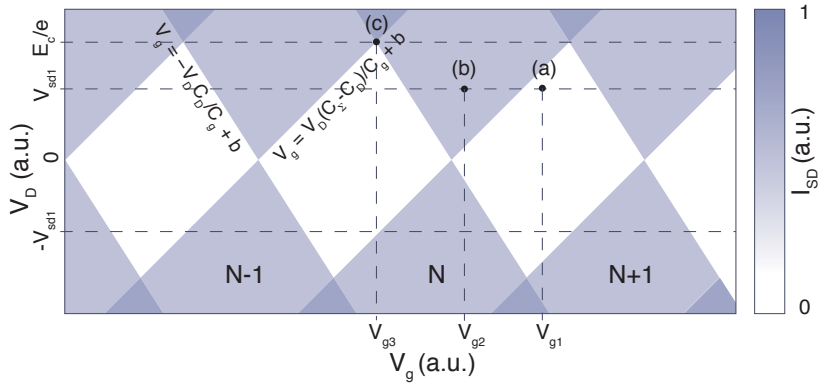


(c)

Figure 2.9: Conditions for Coulomb blockade within an SET at zero source-drain bias. (a) If the energy level of the dot is not in line with the source and drain reservoirs, conduction from the source to the N state is blockaded (left red arrow) and conduction from the $N-1$ state is blockaded (right red arrow), preventing current flow through the device. (b) If an appropriate shift in the dot potential $\Delta\mu_d$ is applied via the gate, the N state can be brought into resonance with the source and drain reservoirs, allowing conduction through the device. (c) As the gate is swept, there are discrete resonances in the device conductance corresponding to the gate voltages at which the dot levels are in resonance with the source and drain reservoirs.



(a) Blockade (b) Conduction



(c)

Figure 2.10: Conditions for Coulomb blockade within an SET with a finite source-drain bias. (a) Again we see blockade of current through the device if there is not a dot energy level situated between the source and drain potential. (b) Using the gate, we can pull the dot level within the source-drain bias window, allowing conduction through the device. (c) If we map the range of gate and drain biases that allow conduction through the device, we form diamonds in the gate-drain bias space known as Coulomb diamonds.

finite width for reasons we discuss in the next section.

Now let us consider the case when we apply an appreciable drain bias V_D, as shown in Fig. 2.10. We see the same regions of blockade, where no electrons can tunnel into or out of the dot states, as shown in Fig. 2.10(a); however if we change the gate voltage, there are now a range of drain biases over which the state N will be situated between the source and drain potential, allowing a current to flow. This range is given by

$$-eV_D = \mu_D \leq \mu_d(N, V_g) \leq \mu_S = 0 \tag{2.17}$$

Tuning the gate so that the dot potential is at the source potential ($\mu_d = \mu_S = 0$) for the equilibrium occupancy ($N = N_0$) gives

$$\begin{aligned} 0 &= -\frac{e}{C_\Sigma}\left(C_g V_g + V_D C_D\right) + \mu_d(N_0) \\ \Rightarrow V_g &= -V_D \frac{C_D}{C_g} + \frac{C_\Sigma}{eC_g}\mu_d(N_0) \end{aligned} \tag{2.18}$$

Similarly, setting the dot potential to the drain potential ($\mu_d = \mu_D = -eV_D$) for the equilibrium occupancy ($N = N_0$) gives

$$\begin{aligned} -eV_D &= -\frac{e}{C_\Sigma}\left(C_g V_g + V_D C_D\right) + \mu_d(N_0) \\ \Rightarrow V_g &= V_D\left(\frac{C_\Sigma - C_D}{C_g}\right) + \frac{C_\Sigma}{eC_g}\mu_d(N_0) \end{aligned} \tag{2.19}$$

thus there is a window within which conduction will occur, which increases linearly with V_D, given by

$$\begin{aligned} \Delta V_g &= V_D\left(\left(\frac{C_\Sigma - C_D}{C_g}\right) - \left(-\frac{C_D}{C_g}\right)\right) \\ &= V_D\frac{C_\Sigma}{C_g} \end{aligned} \tag{2.20}$$

At a finite drain bias (which we must apply to force current to flow), the peaks in source-drain current therefore have a finite width, which increases with the drain bias. If we replicate these gate sweeps at many drain voltages, we can form a 2-D plot of the source-drain current as a function of both the applied drain bias V_D, and the gate bias V_g; an example of this is shown in Figure 2.10(c). As a consequence of the variation in the peak width, the Coulomb blockaded regions (where there is no current) form diamonds in the 2-D plot, commonly referred to as Coulomb diamonds. The two operating points shown schematically in Fig. 2.10(a) and Fig. 2.10(b) are indicated on this 2-D plot with the labels (a) and (b), respectively. The equations defining the regions of conduction, set out in Eq. 2.18 and Eq. 2.19, are shown for the ($N_0 = N-1$) dot state. The constant b in these equations is the gate voltage corresponding to a resonance for $V_D = 0$. This is given by the final term in Eq. 2.18 and Eq. 2.19, which at the $(N-1)$ transition is $(C_\Sigma/eC_g)\mu_d(N-1)$.

What we see from the 2-D map in Fig. 2.10(c) is that there is a particular V_D beyond which the conduction of the N and $(N-1)$ states begin to overlap, labelled as point (c). Physically, this point corresponds to the precise drain bias at which both the N and $(N-1)$ states are within the V_D bias window, therefore here we have $\mu_d(N-1) = \mu_D$ and $\mu_d(N) = \mu_S = 0$. This value of V_D corresponds precisely to the separation between energy

levels on the dot, defined previously as E_c. We can check this condition analytically by introducing the electron occupancy into Eq. 2.18 and Eq. 2.19:

$$\begin{aligned} 0 &= -\frac{e}{C_\Sigma}\left(C_g V_g + V_D C_D - e(N - N_0)\right) + \mu_d(N_0) \\ \Rightarrow V_g &= -V_D\frac{C_D}{C_g} + \frac{e}{C_g}(N - N_0) + \frac{C_\Sigma}{eC_g}\mu_d(N_0) \end{aligned} \tag{2.21}$$

and

$$\begin{aligned} -eV_D &= -\frac{e}{C_\Sigma}\left(C_g V_g + V_D C_D - e(N - N_0)\right) + \mu_d(N_0) \\ \Rightarrow V_g &= V_D.\left(\frac{C_\Sigma - C_D}{C_g}\right) + \frac{e}{C_g}(N - N_0) + \frac{C_\Sigma}{eC_g}\mu_d(N_0) \end{aligned} \tag{2.22}$$

Now we can look for the point at which $\mu_d(N-1) = -eV_D$ and $\mu_d(N) = \mu_S = 0$ by setting $(N - N_0) = N$ in Eq. 2.21 (the left side of the N conductance window), and $(N - N_0) = (N - 1)$ in Eq. 2.22 (the right side of the $(N-1)$ conductance window); and equating the two (since we are looking for the point of coincidence in V_g).

$$\begin{aligned} -V_D\frac{C_D}{C_g} + \frac{e}{C_g}(N) + \frac{C_\Sigma}{eC_g}\mu_d(N_0) &= V_D.\left(\frac{C_\Sigma - C_D}{C_g}\right) + \frac{e}{C_g}(N-1) + \frac{C_\Sigma}{eC_g}\mu_d(N_0) \\ \Rightarrow 0 &= V_D\frac{C_\Sigma}{C_g} - \frac{e}{C_g} \\ \Rightarrow V_D &= \frac{e}{C_\Sigma} \qquad (2.23) \\ \Rightarrow \mu_D = -eV_D &= -\frac{e^2}{C_\Sigma} = -E_c \qquad (2.24) \end{aligned}$$

the negative sign arises because we have pulled the drain potential below the reference (ground) energy. Using this result, we can thus say that the apex of the Coulomb diamond gives the sum capacitance C_Σ directly, and the charging energy of the dot.

Similarly, we can extract the gate capacitance from the change in gate voltage between dot transitions with $V_D \simeq 0$, where the dot is in resonance with the source and drain. For this we can use either Eq. 2.21 or Eq. 2.22, and evaluate the difference in V_g. Using Eq. 2.21:

$$\begin{aligned} \Delta V_g &= \left(-V_D\frac{C_D}{C_g} + \frac{e}{C_g}(N - N_0) + \frac{C_\Sigma}{eC_g}\mu_d(N_0)\right) \\ &\quad - \left(-V_D\frac{C_D}{C_g} + \frac{e}{C_g}((N-1) - N_0) + \frac{C_\Sigma}{eC_g}\mu_d(N_0)\right) \\ &= \frac{e}{C_g} \end{aligned} \tag{2.25}$$

Thus, the period of the Coulomb blockade peaks is inversely proportional to the gate capacitance.

Necessary conditions for Coulomb blockade

Since there is an inherent variance in the time that an electron resides on the dot, there will be an associated uncertainty in the electron's energy, according to Heisenberg's uncertainty principle

$$\Delta E \Delta t > \frac{\hbar}{2} \tag{2.26}$$

where ΔE is the uncertainty in the energy of the electron and Δt is the uncertainty in the time for which the electron remains in this state. In order to resolve the spacing between discrete energy levels on the dot, we require the uncertainty in the electron energy to be less than the separation between dot states ($\Delta E \ll E_c$). As a lower limit on Δt, we can use the time constant for charging and discharging of the dot $\Delta t > \tau = R_t.C_\Sigma$, where R_t is the effective resistance of the tunnel barrier. From these requirements of energy and time scales, we find

$$\begin{aligned} \Delta E \Delta t \simeq E_c.\tau &\gg h > \hbar/2 \\ \Rightarrow \frac{e^2}{C_\Sigma}.R_t.C_\Sigma &\gg h \\ \Rightarrow R_t &\gg h/e^2 \end{aligned} \tag{2.27}$$

which is to say that the resistance of the tunnel barrier around the operating point must be greater than the resistance quantum $h/e^2 = 25.8k\Omega$, if we are to resolve the discrete energy spectrum of the dot. This effect is known as lifetime broadening of the electron energy. In fact, we can express this tunnelling resistance in terms of the tunnelling rate Γ of electrons through the dot. We can then expect lifetime broadening to alter the width of the Coulomb blockade peak according to the relation [47, pg. 17]

$$\frac{I_{SD}(\delta)}{I_{SD_{peak}}} = \frac{(h\Gamma)^2}{(h\Gamma)^2 + \delta^2} \tag{2.28}$$

where $V_D \simeq 0$ is constant, $\delta = \frac{eC_g}{C_\Sigma}\left(V_g - V_{g_{peak}}\right)$ is the deviation in the dot potential μ_d from the resonance condition induced by the change in gate voltage $\left(V_g - V_{g_{peak}}\right)$, and $I_{SD_{peak}}, V_{g_{peak}}$ are the current and gate voltage at the Coulomb blockade peak, respectively. In addition to lifetime broadening, we also see thermal broadening of the electron energy, in which thermal excitations create a Boltzmann distribution of electron energies, that

prevent Coulomb blockade unless

$$k_B T \ll E_c \tag{2.29}$$

where k_B is Boltzmann's constant, and T is the electron temperature. In practice, we cannot easily achieve electron temperatures below $100mK$, so we require a charging energy greater than $E_c \simeq 90\mu eV$ (using a factor of 10 to satisfy the strong inequality). For the condition $h\Gamma \ll k_B T \ll E_c$, the Coulomb blockade peak has a finite width as a consequence of thermal broadening, given by [47, pg. 15]

$$\frac{I_{SD}(\delta)}{I_{SD_{peak}}} = \frac{\delta/k_B T}{\sinh(\delta/k_B T)} \tag{2.30}$$

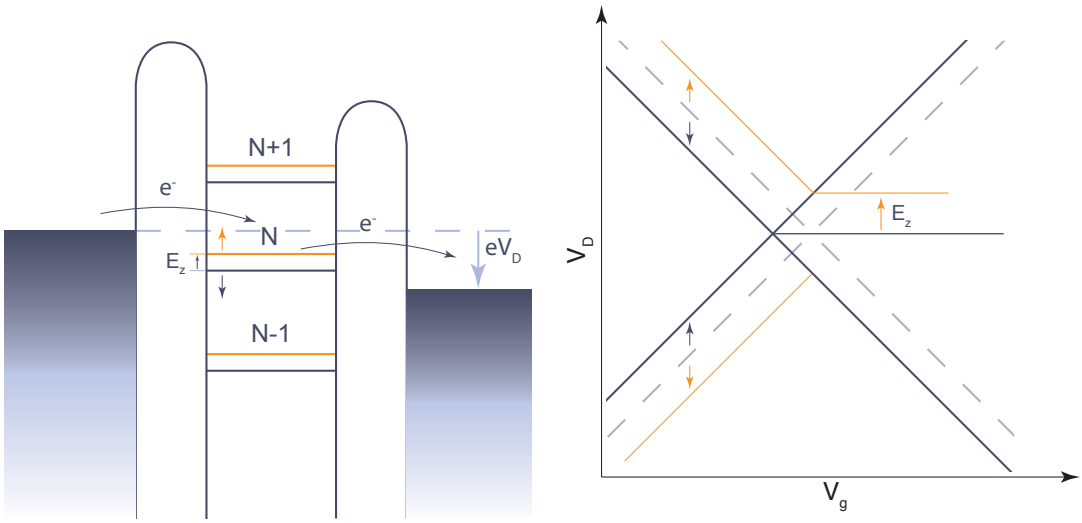
using the previously defined symbol notation. We will use this relationship between broadening of the electron energy levels and the electron temperature to determine the electron temperature of our sample in Chapter 4.

2.5.2 Transport through excited states in quantum dots

In addition to the classically-separated electronic states that occur within a single electron transistor, it is possible to see additional 'excited' states in the transport spectroscopy (i.e. the 2-D map of I_{SD} vs. $V_{D,g}$), which typically manifest as a step-change in the current through the device, arising from the additional conductance channel permitted by the excited state [48]. We refer to these levels as excited states because they are not generally the lowest-energy empty state on the dot, but they still contribute to conduction through the device. These excited states arise from quantum effects within the dot (or leads), and manifest as step-changes in the device current as a function of V_g and V_D, running parallel to the Coulomb diamond edge, as discussed by Escott *et al.* [48], whose review forms the basis for this discussion. The types of features we see in this 'excited state spectroscopy' are generally divided into the following categories:

Spin excited states

Spin excited states arise when we apply a magnetic field to the system, which causes Zeeman splitting of the electronic states on the dot (and the leads) by an energy of $E_z = \pm s_z g \mu_B B$, where s_z is the projection of the particle spin in the direction of the magnetic field ($\pm 1/2$), g is the gyromagnetic ratio ($\sim$2 in silicon), B is a magnetic field applied to the sample, and μ_B is the Bohr magneton $\mu_B = \frac{e\hbar}{2m_e}$. To see any spin split features in the stability plot, as illustrated in Fig. 2.11, at dilution refrigerator temperatures ($> 100mK$),



(a) (b)

Figure 2.11: Zeeman splitting of the ground state in a quantum dot. (a) In the presence of a magnetic field, the ground state of a quantum dot will split into two states, giving a lower-energy ground state that is in this case stricly occupied by spin-down electrons, and a second excited state that is strictly occupied by spin-up electrons. Note that the ground and excited states will not be populated simultaneously. (b) If we take a 2-D map of the differential conductance through the dot (dI_{SD}/dV_D), we see lines demarcating the regions of conduction through the ground state, with an additional line running parallel to the Coulomb diamond edge, corresponding to a step change in the conductance made possible by the spin excited state.

we require $E_z \gg k_B \times 100mK \simeq 8.6\mu V$. If we take $100\mu V$ as the minimum resolvable energy separation to satisfy this strong inequality (such that $E_z = \pm 50\mu V$), we are only likely to see clear Zeeman splitting in fields of

$$\begin{aligned} B &> \frac{E_z}{s_z g \mu_B} \\ &> \frac{50 \times 10^{-6} eV}{1/2 \times 2 \times \mu_B} \\ &\simeq 0.86T \end{aligned} \tag{2.31}$$

which we can easily reach with the measurement apparatus used in this thesis ($B < 8T$). At this limit of the magnetic field ($8T$), we should see a splitting between peaks of $\sim 930\mu V$. We use the Zeeman effect in Chapter 4 to isolate the spin-degenerate ground state in our STM-patterned quantum dot.

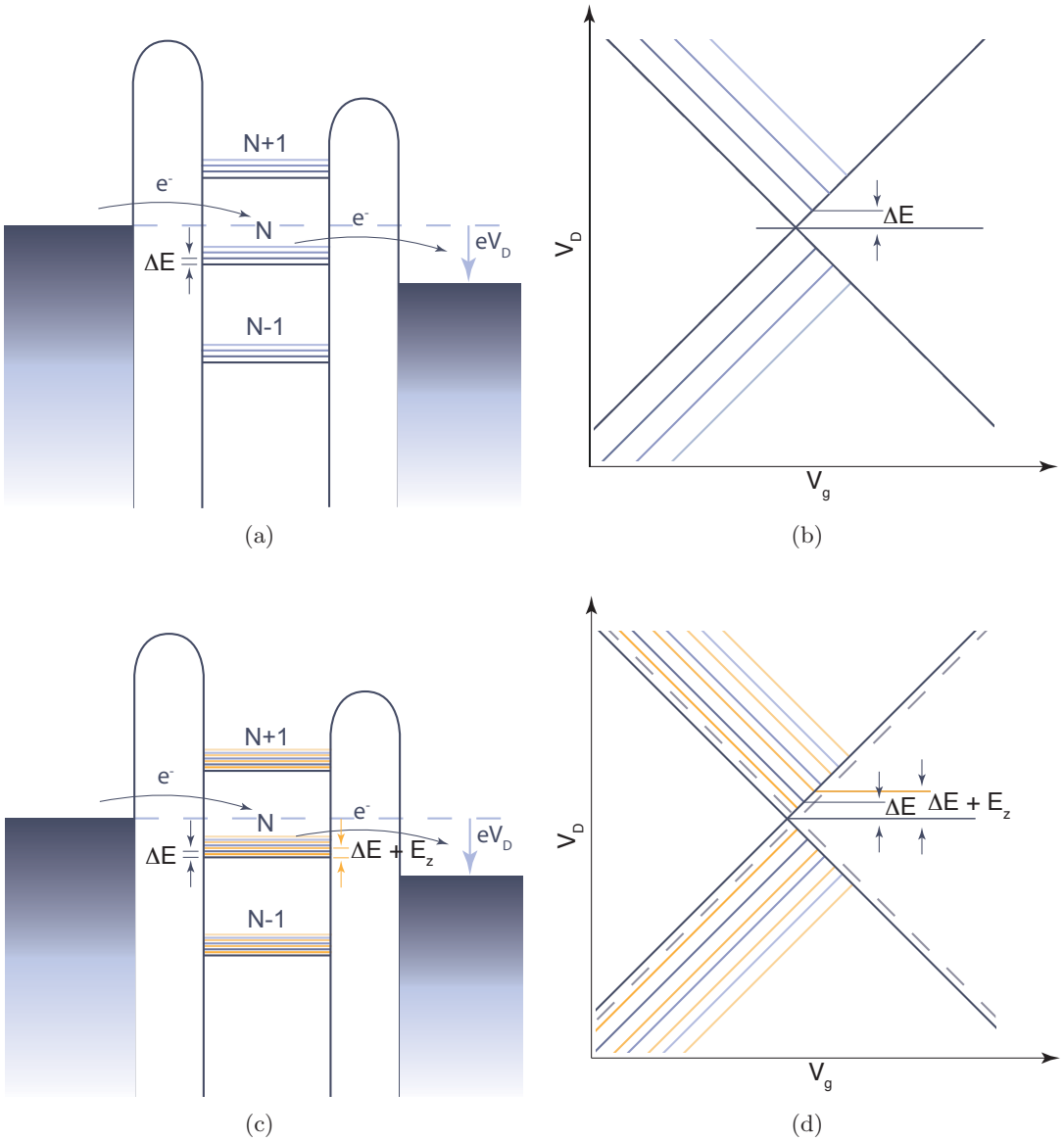


Figure 2.12: Effect of a magnetic field on orbital excited states in an SET (a) In the presence of orbital excited states, there may be multiple states around the N^{th} charge-separated level accessible by conduction electrons. (b) The orbital excited states appear as lines in the differential conductance running parallel to the Coulomb diamond edge. (c) In the presence of a magnetic field, the orbital excited states will split. (d) The splitting of the excited state energy levels causes a doubling of all the excited state lines in the stability plot.

Orbital excited states

Orbital excited states are generated from the geometric confinement of the electron wavefunction, the simplest model for which is the 'particle in a box' model seen in most introductory physics courses. For a two-dimensional box with area A, we expect an energy level spacing of [47, pg. 6]

$$\Delta E_{orb} = \frac{2}{\pi}\frac{\hbar^2\pi^2}{g_s g_v m^* A} \tag{2.32}$$

where $g_{s,v}$ are the spin and valley degeneracy of the electronic states, respectively, and $m^* = 0.28$ is the transport effective mass of electrons in our δ-doped systems, calculated using $m^* = 3(2/m_t + 1/m_l)^{-1}$ from [49]. For our δ-doped silicon devices, the spin degeneracy is $g_s = 2$, the valley degeneracy is within the range[1] $g_v = 1$–6, and the devices we have patterned in this thesis have an area $A \simeq 5.4nm \times 23nm$, giving a minimum energy separation of

$$\begin{aligned} \Delta E_{orb} &= \frac{2}{\pi}\frac{\hbar^2\pi^2}{12 \times 0.28 \times (5 \times 10^{-9})^2} \\ &= 1.3meV \end{aligned} \tag{2.33}$$

which is within the measurable range of devices presented in this thesis ($kT < E_{orb} < E_c$).

For non-trivial dot shapes (e.g. roughened or asymmetric sidewalls of the dot potential profile), the particle in a box approximation is poor, although the confinement levels themselves may still be of the same order of this calculated energy. As shown in Fig. 2.12, under an applied magnetic field, each of the orbital excited states will split by the Zeeman energy.

Valley excited states

The conduction band minimum of bulk silicon is comprised of six degenerate bands, resulting from the symmetry of the crystal structure in the six orthogonal directions of the cubic unit cell. The degeneracy of these bands is broken when we break the symmetry of the crystal potential, typically by confining the electron wavefunction to an n-dimensional well, for $n \leq 2$. This is precisely what happens when we create a δ-doped layer of phosphorus in silicon to pattern our atomic-scale devices. If we assume the doping density of the STM-patterned regions is approximately equal to the value measured in large-area Hall bars (0.25–$0.3ML$), the average separation between the donors is less than the Bohr radius

[1] The valley degeneracy is generally broken by the confinment of carriers to a potential well, so we can only place an upper and lower limit on the expected valley degeneracy, as discussed in the 'valley excited states' section presented next.

of $a_B = 2.5nm$ [50]. As such, the electronic states are distributed throughout the δ-doped layer. Modelling of the δ-doped band structure by Carter *et al.* using density functional theory showed that there were three partially occupied sub-bands (1Γ, 2Γ, and four nearly degenerate 1Δ bands). Fuechsle *et al.* (from our group) have shown that it is possible for the upper 1Δ sub-band to split when the δ-doping is confined in the x and y-directions using STM-lithography [23]. The resultant separation between valleys is determined by the sharpness of the confinement potential, which is $\sim 1.1eV.nm^{-1}$ for our δ-doped system [23]. For Fuechsle's dot containing $\sim$7 electrons, a self-consistent calculation of the electron wavefunctions, assuming a homogenous distribution of the donor charge, showed that it was possible for an energy separation on the order of $100\mu eV$ to arise between the four nearly degenerate 1Δ bands [23]. However, Fuechsle *et al.* conclude that it was not possible for valley excited states alone to explain the excited state spectrum of their quantum dot; the remaining excited states were attributed to variations in the density of states of the source and drain leads.

Density of states in the leads

The SETs fabricated for this thesis have source and drain leads that are confined vertically to $\sim 2nm$ as a consequence of the δ-doping profile [33], and laterally to 5–$7nm$ as part of tailoring the tunnel gap geometry to achieve the desired tunnel barrier transparency. These dimensions are comparable to the Fermi-wavelength of carriers within the δ-doped system (2–$3nm$ [51]), and so we can expect to see confinement effects within the leads similar to the orbital excited states present within the dot [52].

Based on a particle in the box approximation, for infinitely sharp barriers in the doping profile we expect the separation between these lead states not to be uniform — the level spacing should increase in proportion to n at the n^{th} eigenstate. As such, there is not one characteristic level spacing that we can attribute to this effect. The level spacing is however, constant for a parabolic potential well, with a separation in energy of [31]

$$\Delta E = \frac{\hbar}{g}\sqrt{\frac{8V}{m^*}}\frac{1}{L} \tag{2.34}$$

for valley degeneracy g as previously defined, and a potential well height of V over the lateral extent L. For a lead width of $5nm$ and a barrier height of $\sim 100meV$ [33], this corresponds to a constant energy spacing of $\sim 7meV$ [31].

Since the gyromagnetic ratio of the leads and dot tend to be approximately equal, applying a magnetic field to the device splits the lead and dot energy levels equally, as shown in Fig. 2.13. As such, the resonant features arising from the density of states

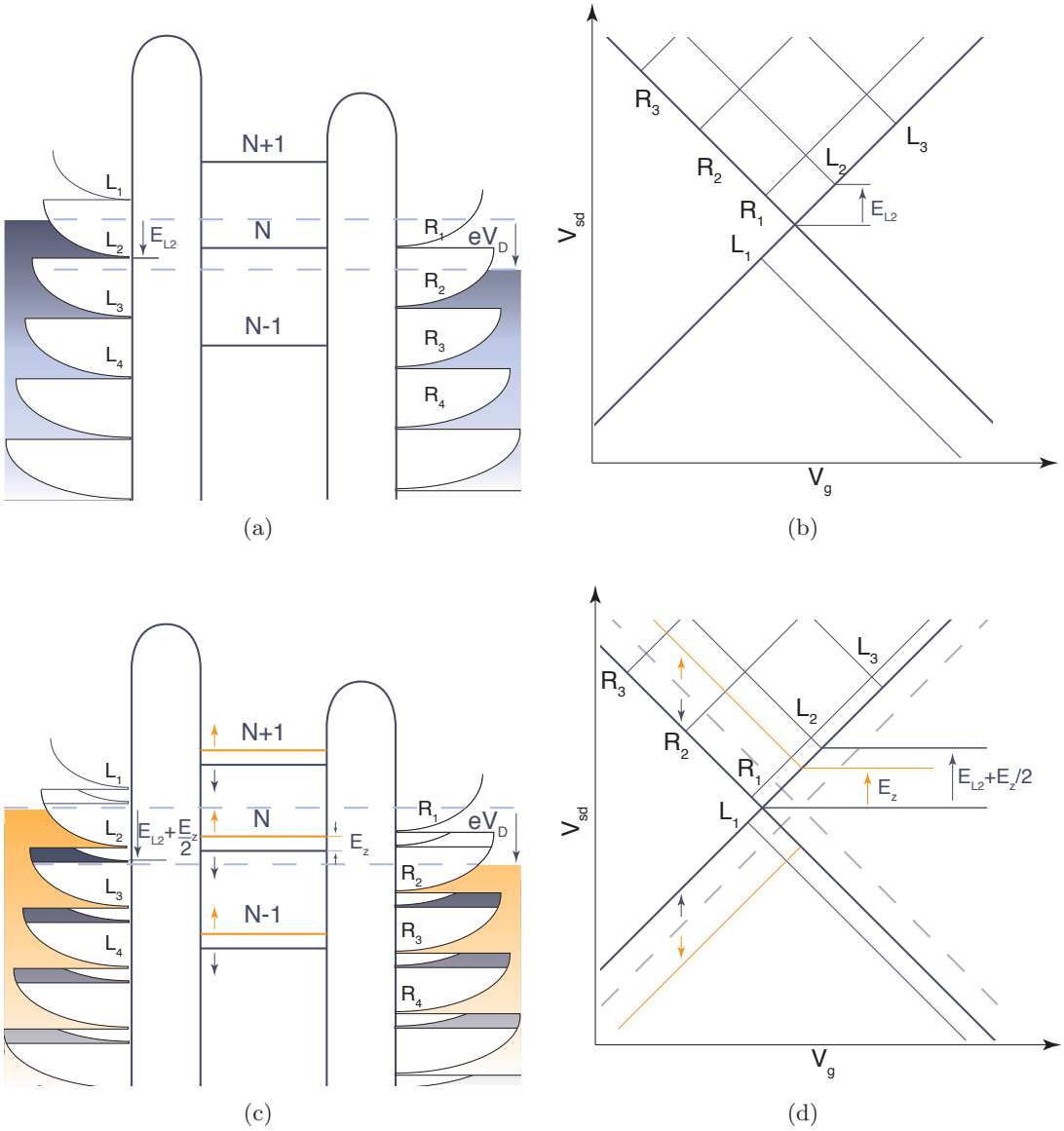


Figure 2.13: Effect of magnetic field on resonances arising from density of states in SET leads. (a) If the leads of the quantum dot are sufficiently narrow to cause quantisation of the energy levels in the leads, at some drain and gate biases we will see resonant features in the conductance, (b). (c) Under an applied magnetic field, the dot and lead states typically split by the same amount so that the energy splitting of the lead states is not visible, and so the resonant features in the stability plot remain unchanged (d) except for the Zeeman shift of the ground state of the dot.

fluctuations in the leads do not move (or split) under an applied magnetic field — though the splitting of the ground state of the dot causes the diamond edge to move relative to the lead DOS lines.

In Chapter 4, we use these differences between the variety of excited states present in quantum dots to isolate the cause of the resonant features in the transport spectroscopy of our quantum dot.

2.5.3 Noise in quantum dots

Finally in order to compare the electrical quality of quantum dots with and without the low temperature UHV SiO_2 dielectric developed in this thesis we will describe the theoretical background for the noise measurements conducted in Chapter 4 and Chapter 5. Any measurement of electron transport will include an inherent noise component, which is visible as a non-deterministic fluctuation in the measured sample conductance. This noise component arises from a variety of physical processes, most importantly sample drift, Johnson noise, random telegraph noise, and $1/f$ noise. To distinguish between the different sources of noise, we assess the deviation of the conductance from its steady-state value, $\delta\sigma(t) = \sigma(t) - \langle\sigma\rangle$, the magnitude of this fluctuation relative to the applied bias, and the frequency composition of the conductance noise, expressed in the form of its power spectral density. Here we first introduce the concept of power spectral density, and how it may be calculated from a series of measurements in the time domain, and then will discuss each of the mentioned sources of noise.

Power spectral density of stochastic signals

The time-averaged power of a randomly fluctuating potential $v(t)$ across a resistor is

$$P = \lim_{T\to\infty} \frac{1}{TR} \int_{-T/2}^{T/2} |v(t)|^2 \, .dt \tag{2.35}$$

where P is the power (W), R is the resistance (Ω), and T is the period over which the integral is performed (s). Since the potential is random, it is by definition aperiodic, as such there is no convenient interval over which we can calculate the integral, hence we calculate the integral over the limit $T \to \infty$. By Parseval's theorem [53], the net power of a time-series is equal to the net power of its Fourier transform

$$\int_{-\infty}^{\infty} |v(t)|^2 \, .dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |V(\omega)|^2 \, .d\omega \tag{2.36}$$

which, when restricted to a finite period, gives

$$\int_{-T/2}^{T/2} |v(t)|^2 .dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |V_T(\omega)|^2 .d\omega \tag{2.37}$$

where $V_T(\omega) = \mathscr{F}\{v(t).\text{rect}(t/T)\}$, is the Fourier transform of the time series $v(t)$ windowed by a rectangular function.

Thus we can say

$$\begin{aligned} P &= \lim_{T\to\infty} \frac{1}{TR} \int_{-T/2}^{T/2} |v(t)|^2 .dt \\ &= \lim_{T\to\infty} \frac{1}{TR} \frac{1}{2\pi} \int_{-\infty}^{\infty} |V_T(\omega)|^2 .d\omega \\ &= \frac{1}{2\pi} \int_{-\infty}^{\infty} S_v(\omega).d\omega \end{aligned} \tag{2.38}$$

where $S_v(\omega)$ is by definition the component of the signal power of frequency ω. From this we can say

$$S_v(\omega) = \lim_{T\to\infty} \frac{|V_T(\omega)|^2}{RT} \tag{2.39}$$

such that, following the treatment of Stremler [53],

$$\begin{aligned} \mathscr{F}^{-1}\{S_v(\omega)\} &= \frac{1}{2\pi} \int_{-\infty}^{\infty} \lim_{T\to\infty} \frac{|V_T(\omega)|^2}{RT} e^{j\omega\tau}.d\omega \\ &= \lim_{T\to\infty} \frac{1}{2\pi RT} \int_{-\infty}^{\infty} V_T^*(\omega) V_T(\omega) e^{j\omega\tau}.d\omega \\ &= \lim_{T\to\infty} \frac{1}{2\pi RT} \int_{-\infty}^{\infty} \left(\int_{-T/2}^{T/2} v^*(t) e^{j\omega t}.dt \right) \left(\int_{-T/2}^{T/2} v(t_a) e^{-j\omega t_a}.dt_a \right) .e^{j\omega\tau}.d\omega \\ &= \lim_{T\to\infty} \frac{1}{RT} \int_{-T/2}^{T/2} v^*(t) \int_{-T/2}^{T/2} v(t_a) \left[\frac{1}{2\pi} \int_{-\infty}^{\infty} e^{j\omega(t-t_a+\tau)}.d\omega \right] .dt_a.dt \\ &= \lim_{T\to\infty} \frac{1}{RT} \int_{-T/2}^{T/2} v^*(t) \int_{-T/2}^{T/2} v(t_a).\delta(t-t_a+\tau) dt_a.dt \\ &= \lim_{T\to\infty} \frac{1}{RT} \int_{-T/2}^{T/2} v^*(t).v(t+\tau).dt \end{aligned} \tag{2.40}$$

where this last result is commonly known as the Wiener-Khinchin theorem, which relates the power spectral density to the autocorrelation function of the signal $v(t)$; that is to say, we can compute the power spectral density of $v(t)$ by calculating the Fourier transform of its autocorrelation function. In general, it is more instructive to express the power spectral

density relative to the mean square power, in the form

$$PSD_{Norm}(\omega) = \frac{S_v(\omega)}{\langle v^2 \rangle} \tag{2.41}$$

which gives the signal power contributed at each frequency, and eliminates any dependence on the sample resistance, R.

Since it is impossible to numerically calculate the Fourier transform of an infinitely long series, it is common to use the algorithm developed by Welch [54], which computes the power spectral density (PSD) over many short interval of the signal, and generates the final PSD from the average of each interval's PSD. Note that, in general, these intervals may overlap. The principle advantage of this approach is a reduction in the memory required to perform the computation, since we are only required to hold a small portion of the signal in memory along with the average PSD, which is updated as each interval is processed.

Johnson noise

Johnson noise is caused by thermal fluctuations in the distribution of carriers within a sample, which manifests as a fluctuating voltage across the sample, even in the absence of an applied bias [55, 56]. The resultant deviation of the sample voltage from its equilibrium value, $\delta v(t) = v(t) - \langle v \rangle$, has a Gaussian distribution function. The power spectrum of Johnson noise is flat, which is to say that fluctuations of all frequencies occur with equal probability. The magnitude of Johnson noise is proportional to the temperature and the sample resistance, according to the relation

$$< v^2(t) >= 4k_B T R \Delta f \tag{2.42}$$

where v is the noise voltage, k_B is Boltzmann's constant, T is the temperature, R is the sample resistance, and Δf is the bandwidth over which the average is taken. Thus we can distinguish Johnson noise from other noise types based on the fact that it (a) occurs without an applied bias, (b) has a Gaussian distribution from the mean value, and (c) is uniformly distributed across all frequencies.

Random telegraph noise and $1/f$ Noise

If the current passing through a device switches discontinuously between two discrete states, often referred to as a random telegraph signal (RTS), the power spectrum of the current will have a signature shape, consisting of a flat (frequency-independent) noise level,

transitioning at a corner frequency to a power-law relationship given by

$$\frac{S_v(\omega)}{v^2} = \frac{A\tau_z}{1+\omega^2\tau_z^2} \tag{2.43}$$

where A is a proportionality constant, and τ_z is the time constant associated with changing between the two states, giving a corner frequency of $f_c = 1/2\pi\tau_z$. From this we see that the power spectral density will fall with frequency as $1/f^2$ for $f \gg f_c$.

When scaled to large dimensions, most semiconductor devices are influenced by many concurrent RTS events, each with a different time constant and magnitude. Typically we find that there is an exponential decay in the number of RTS events with increasing frequency — resulting in the time constants of these RTS fluctuations being uniformly distributed in $\log(f)$. In this case, the resultant power spectral density will fall with frequency as $1/f$, giving the prevalent $1/f$ noise seen in most semiconductor devices [57].

Chapter 3

Development of a Low-Temperature, UHV-Compatible Oxide for Atomic-Scale Devices

Fabricating devices in silicon with atomic precision is a challenging problem; at such minuscule scales thermally activated diffusion can alter the arrangement of dopants over length-scales comparable to the device dimensions. To overcome these challenges, our group has developed a unique low-temperature fabrication strategy that uses STM-lithography to pattern dopants with atomic precision in a pristine ultra-high vacuum environment [20, 58, 59]. In this chapter we describe the extension of this fabrication scheme to include a means of surface-gating atomic-scale devices.

3.1 Introduction

In 2004, our group developed a process to fabricate atomic-scale devices using STM-lithography, which has since been used to demonstrate atomic-scale tunnel gaps, wires, and in-plane gated quantum dots [22, 23, 60–64]. These devices have shown interesting electron transport phenomena (such as electron tunnelling, weak and strong localisation, and Coulomb blockade) and open the way for complex atomic-scale circuits, which may ultimately lead to a scalable implementation of a solid-state quantum computer.

The functionality of atomic-scale circuits is greatly enhanced using gates to control the flow of conduction electrons. In most semiconductor devices this is achieved by covering the semiconductor with a dielectric and capping the dielectric with a surface gate that, when biased using an external potential, changes the conductivity of the device. However, adding surface gates to STM-patterned devices is non-trivial. It requires additional process steps, including growing a high quality oxide, aligning the surface gates to the buried STM patterned layers, and ensuring good Ohmic contact to the buried dopant layer. In this chapter, we describe the overall requirements of these new process steps, and introduce the techniques we have developed to implement them.

3.2 Compatible dielectrics for STM-patterned devices

Adding surface gates to buried STM-patterned devices requires that we deposit the dielectric at a low temperature to prevent thermally activated diffusion of the dopants. In addition, the deposition process itself should ideally be compatible with the ultra-high vacuum environment in which we fabricate devices to prevent contamination of the interface, while retaining key properties of the material as a gate dielectric. These properties include low leakage currents, low interface trap densities, and high gate selectivity. Here we quantify these requirements, beginning with our thermal budget.

3.2.1 Dielectric requirements for STM-patterned devices

Low temperature deposition of the dielectric

To find a suitable dielectric, we must first quantify the thermal budget available for processing STM-patterned devices. Conventional dielectrics like thermally grown SiO_2 are formed at high temperatures to achieve practical oxidation rates ($> 600°C$), but such high temperatures are untenable for our process. To establish the available thermal budget, we must therefore quantify the expected thermally activated dopant diffusion. Phosphorus diffuses through silicon via both silicon vacancies and interstitials, where the dominant mechanism is determined by the concentration of strain and defects during the doping process [65]. In contrast to conventional doping techniques like ion-implantation and in-diffusion, our STM-fabrication scheme uses gas-phase doping of the silicon surface, which induces minimal strain or defects. In this process, the reactive silicon surface is exposed to phosphine gas (PH_3) at room temperature, which adsorbs to the surface. The sample is subsequently annealed at low temperature ($350°C$) for $1min$ to incorporate the phosphorus atoms from the adsorbed PH_3 into the silicon substrate. As it is energetically favourable for dopants to remain at the surface, there is little diffusion of the dopants into the bulk during this anneal. The initial doping profile using this technique is therefore atomically abrupt, and may be modelled as a δ-function. Following incorporation of the dopants, the device is encapsulated with crystalline silicon using molecular beam epitaxy at $\sim 250°C$. Throughout the epitaxial growth, segregation can occur, giving rise to an exponential decay of the doping profile towards the newly formed surface. As each layer of silicon is deposited, a fraction of the dopants incorporate into the underlying silicon ($n_s \times p_{inc}$), while the majority of dopants preferentially float to the new surface ($n_s \times (1 - p_{inc})$). Under this process, encapsulating with N monolayers of silicon reduces the surface concentration

to

$$n_{surf} = n_s \times (1 - p_{inc})^N . \tag{3.1}$$

$$\Rightarrow p_{inc} = 1 - \left(\frac{n_{surf}}{n_s}\right)^{\frac{1}{N}} \tag{3.2}$$

Our group have studied the segregation of donors during the silicon growth using an STM to count dopants on the surface [34]: After a 5 monolayer MBE growth ($5ML \times 0.136nm/ML = 0.68nm$), it was found that $n_{surf}/n_s = 25\%$, from which we see using Eq. 3.2 that

$$\Rightarrow p_{inc} = 1 - (0.25)^{\frac{1}{5}} = 0.24 \tag{3.3}$$

Which is to say that 24% of dopants incorporate into the lattice as each new layer of silicon is deposited, giving an exponential decay in the dopant profile with a decay length of $0.58nm$ [34]. We show a numerical model of this segregation in Fig. 3.1: Starting from the δ-doping profile in Fig. 3.1(a), the dopants segregate during the MBE growth with $p_{inc} = 0.24$, leading to the dopant profile shown in Fig. 3.1(b). In this same experiment, the diffusion of dopants was subsequently quantified by annealing the sample in six $5s$ increments at successively higher temperatures (conducted in $\sim 50°C$ steps from $350°C$ to $600°C$). STM images from this study are shown in Fig. 3.2(a). Here bright protrusions correspond to P dopants that have reached the surface. The relative surface concentration n_{surf}/n_s measured from these images is shown in Fig. 3.2(b), plotted as a function of the anneal temperature. We can fit this data using a numerical model that accounts for both segregation (from Eq. 3.3) and diffusion using Fick's law

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}. \tag{3.4}$$

The temperature dependence of this fit arises from the diffusion coefficient D, which was used as a fitting parameter to match the experimental data in Fig. 3.2(b). The results of this numerical modelling are shown in Fig's 3.1(c) and 3.1(d), in which we see the dopants spread out during the anneal in an approximately Gaussian profile. Note that those dopants that reach the surface are pinned there, as this is energetically favourable.

Based on the calculated diffusivity $D(T)$ from this experiment, we can establish an upper temperature limit for depositing our dielectric to prevent diffusion of the dopants out of the STM patterned layer. For this, we use Fick's law to estimate the re-distribution

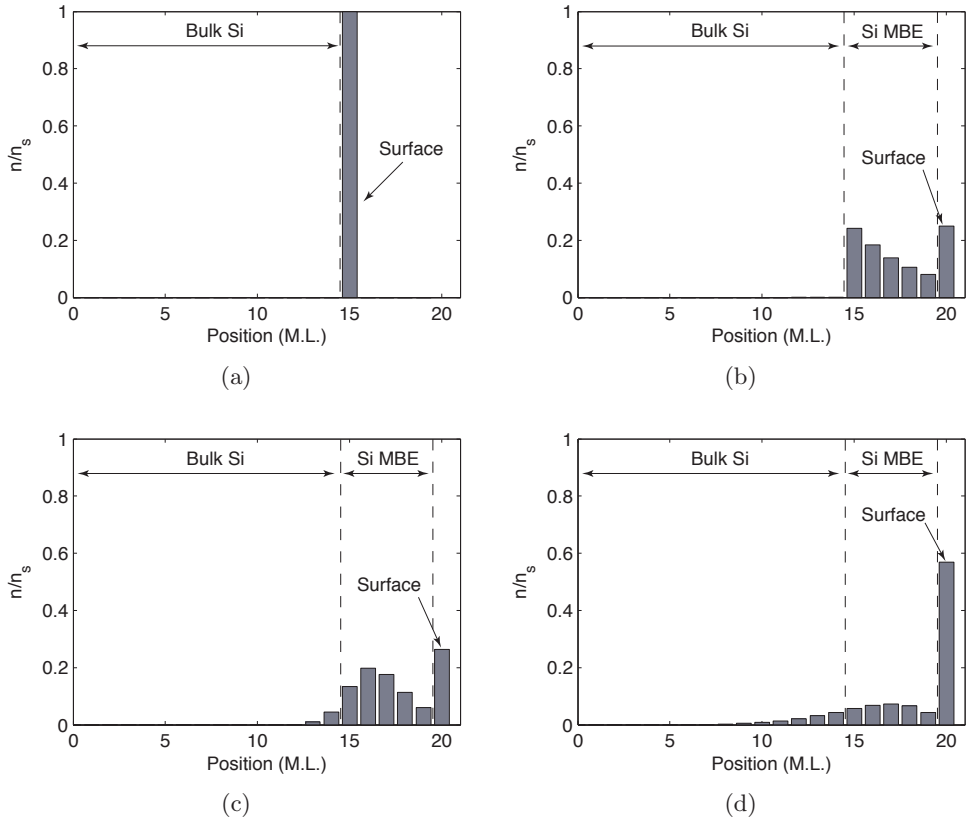
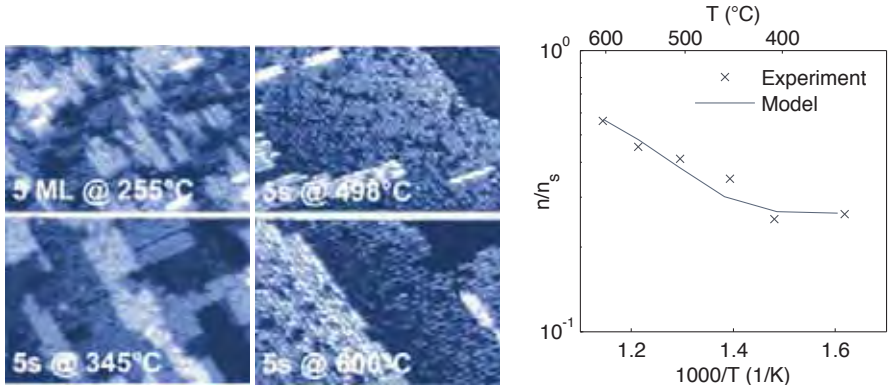


Figure 3.1: Modelling thermal diffusion of Si:P δ-layers. (a) We begin with bulk silicon, upon which the dopants are placed. The doping concentration n is plotted relative to the starting concentration n_s, giving $n/n_s = 1$ at the starting surface. (b) After encapsulating the sample with 5 monolayers of MBE-grown silicon, the dopants segregate throughout the deposited silicon layer, leaving $\sim$ 25% of dopants floating on the final surface. (c) After subsequently annealing the sample for $5s$ at $350°C$, the dopants diffuse throughout the Si; those that reach the surface are pinned there and tend not to diffuse back into the bulk. (d) After five subsequent $5s$ anneals at $\sim 50°C$ increments between 350 and 600, the majority of dopants ($\sim$ 60%) have diffused to the surface.

of dopants during the growth of a low-temperature dielectric

$$n\left(x,t\right) = \frac{n_s}{\sqrt{\pi Dt}}.\exp\left(-\frac{x^2}{4Dt}\right), \tag{3.5}$$

where n is the density of dopants at position x after time t, starting from an initial number of dopants n_s. We aim to keep the diffusion depth to less than one lattice site ($x \simeq 0.5nm$) to maintain atomic-scale precision of our STM-patterned dopants. Since this diffusion profile decays exponentially into the substrate, we must specify a characteristic length for the diffusion depth — here we use the junction depth (x_j), which is the location at which the diffused dopants are equal in concentration to the substrate doping ($n = n_D$).



(a) (b)

Figure 3.2: STM study of segregation and diffusion of δ-doped Si:P reproduced from Oberbeck *et al.* [34] (a) STM images of a δ-doped $Si{:}P$ sample with a $5ML$ encapsulation of silicon after annealing for $5s$ at temperatures of $255°C$, $345°C$, $498°C$, and $600°C$. (b) Experimental value of phosphorus concentration in the silicon surface (crosses) from the study shown in (a), with a numerical model fitting this data (solid line)

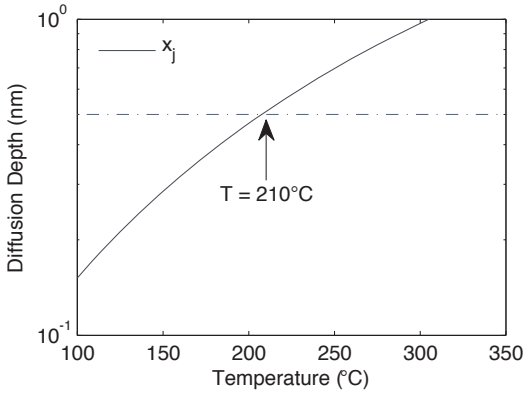


Figure 3.3: Predicted thermal diffusion of Si:P δ-layers while depositing a dielectric. Diffusion predicted by Fick's law for a 3hr oxidation as a function of temperature using the diffusivity, D extracted from Fig. 3.2(b). The plot shows the junction depth (x_j, solid line), where the density of diffused dopants is equal to the substrate doping. The dashed line shows our limit of $x_j \simeq 0.5nm$, one lattice site.

As an example of the expected diffusion when depositing a low-temperature dielectric, Fig. 3.3 shows the diffusion depth calculated using Eq. 3.5 while growing the dielectric over a period of three hours for temperatures ranging from $100°C$ to $350°C$. Note that the temperature and diffusion time are linked, so that a longer period may be accommodated by reducing the growth temperature, or *vice versa*. Here we choose $3hrs$ as a representative figure from the growth process discussed later in this chapter, which has a growth rate of $\sim 0.2nm.min^{-1}$ for the oxide thickness of $30nm$ used. As an input to Eq. 3.5, we use the density of our δ-doping $n_s \simeq 2 \times 10^{14} cm^{-2}$ [66] and the equivalent 2-D density of our substrates $n_D \simeq 3 \times 10^{10} cm^{-2}$ (the bulk doping is $N_D \simeq 5 \times 10^{15} cm^{-3}$). The trend plotted in Fig. 3.3 indicates that, if we are to restrict the diffusion length to less than one lattice site when depositing the dielectric ($x_j < 0.5nm$), we must limit the growth temperature to $\sim 210°C$. At a growth temperature of $300°C$, the diffusivity increases, which increases the junction depth to two lattice sites over a $3hr$ growth ($x_j \simeq 1nm$). From this example, we can see that it is possible to maintain atomic precision in our devices by limiting the substrate to $210°C$ for a $3hr$ growth; though we could tolerate a growth temperature of $300°C$ over this period for most practical applications. We set 210–$300°C$ for $3hrs$ as our thermal budget for the deposition process; let us now quantify the remaining requirements of the process, and the dielectric it forms.

Ultra-high vacuum deposition environment

The STM fabrication scheme is conducted entirely within an ultra-high vacuum environment, which minimises the inclusion of extraneous contaminants within the device. As part of this scheme, the STM tip is used to remove selected regions of atomic hydrogen on the silicon surface, exposing the reactive silicon surface below. The reactive Si regions lithographically defined by the STM tip are exposed to a small quantity of background gaseous species within the vacuum chamber during the lithographic process (which typically takes around $12hrs$). The low background pressure in the UHV chamber ($10^{-11} mbar$) ensures that these background species rarely strike the exposed surface. The species themselves are predominantly molecular hydrogen, hydrocarbon fragments, water, and permutations of their constituent atoms, which adsorb when striking the surface at room temperature with probabilities ranging from 10^{-9} for molecular hydrogen to ~ 1 for atomic oxygen and water [67–69]. Mass spectrometry analysis of the background gaseous species shows that the pressure is dominated by molecular hydrogen. As such, we find experimentally that the exposed sample surface accumulates negligible adsorbates throughout the lithographic process at this pressure.

Maintaining ultra-high vacuum conditions of $10^{-11}mbar$ requires strictly regimented cleanliness and operating procedures, and continuous pumping using both ion pumps and titanium sublimation pumps. The ultra-high vacuum this generates is the cleanest possible environment for atomic-scale device fabrication. As such, it is important to find a dielectric that is compatible with our UHV fabrication environment.

Tolerable leakage of the dielectric for atomic-scale devices

For reliable operation of our STM-patterned devices, we need to minimise the small leakage currents that flow through the dielectric from surface gates. This is necessary in the Kane architecture, for example, because leakage currents passing through the dielectric may decohere the quantum state of the qubit [70]. To quantify the tolerable leakage of surface gates in Kane's architecture, consider a gate with an area of $5 \times 20nm$ situated above a donor. We conservatively assume that each electron passing through the dielectric causes unrecoverable spin decoherence. Maintaining a coherence time greater than $100ms$ under these conditions would require a leakage current density of $J \leq 1.6 \times 10^{-6} A.cm^{-2}$ (1 electron per $100ms$ over an area of $5 \times 20nm$). For the operational fields required, this may be achieved with relative ease using a SiO_2 layer $5nm$ thick.

As a further example, STM lithography has been used to fabricate single electron transistors that operate with a source-drain current of 10–$100pA$ [22]. Gate leakage in these devices must be kept below $10pA$ if we are to maintain a useful signal-to-noise ratio. In this case, an SET gate of $1000\times1000nm$ would require a leakage current density of $J < 1 \times 10^{-3} A.cm^{-2}$, which is trivial to achieve with SiO_2 thicknesses in excess of $5nm$.

Leakage through a dielectric is a consequence of electron tunnelling, where an incident electron wave-function decays exponentially within the dielectric, emerging with some finite amplitude on the other side. For homogeneous dielectrics, Fowler-Nordheim and direct tunnelling dominate gate leakage. Direct tunnelling occurs in thin insulators at low fields, see Fig. 3.4(a), in which an electron tunnels directly from the silicon conduction band to the gate metal. For thicker insulators, Fowler-Nordheim tunnelling occurs through the triangular tip of the barrier [71, 72]. The tunnelling current is exponentially sensitive to both the barrier height (ψ_B) and the thickness of the insulator (t_I). The height of the potential barrier is determined by the offset between the silicon and dielectric conduction bands, which is a property inherent to the dielectric material itself. The thickness of the insulator is more easily controlled, as it is determined by the deposition process. The key to minimising leakage is therefore to deposit a sufficiently thick dielectric that forms a large potential barrier with the substrate (e.g. $t_I > 5nm$ of SiO_2, where $\psi_B = 3.2eV$).

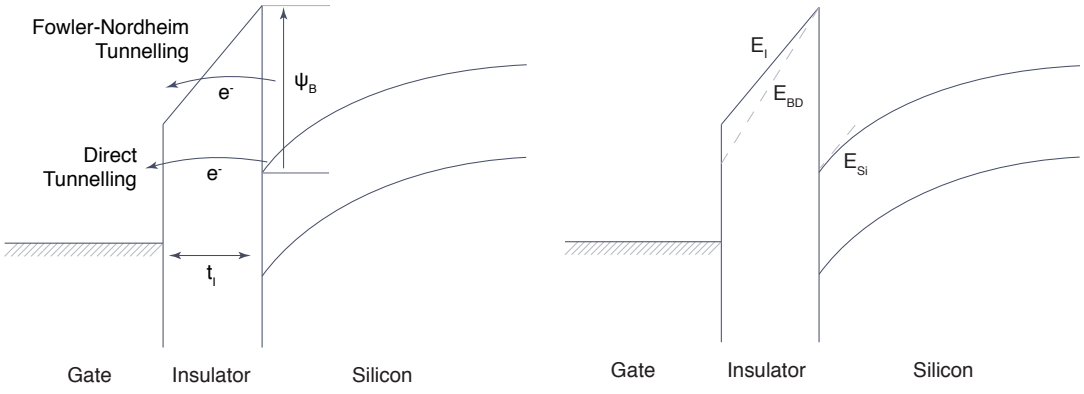


Figure 3.4: Band diagram depiction of breakdown and leakage in dielectrics. (a) The offset between the insulator and silicon conduction bands prevents direct conduction of carriers through the insulator. However, electrons may tunnel through the potential barrier formed. At high fields, electron tunnelling is dominated by Fowler-Nordheim processes, where electrons tunnel through the triangular tip of the potential barrier. At low fields and sufficiently thin insulators, the current is dominated by direct tunnelling. The magnitude of the tunnelling current is exponentially sensitive to the height of the barrier (ψ_B) and the thickness of the insulator (t_I). (b) Applying a bias between the silicon substrate and the gate electrode generates an electric field within the insulator – shown here as the slope of the insulator's conduction band, E_I. When E_I exceeds the breakdown field strength of the insulator, E_{BD}, there is a physical, often irreversible rearrangement of atoms within the insulator. This leads to high leakage between the gate and silicon substrate.

In addition to the tunnelling current, there is an upper limit on the electric field that may be applied to an insulator before it breaks down, at which time a large leakage current flows. The field at which this occurs is known as the breakdown field strength (E_{BD}), shown in Fig.3.4(b); when the slope of the insulator's conduction band (E_I), exceeds E_{BD}, the dielectric breaks down. This process is often irreversible, following a breakdown event the leakage current increases by several orders of magnitude. For this reason, materials are chosen with a breakdown field strength greater than the maximum electric field intended for the device. As an example, the breakdown field of silicon dioxide is $\sim 10 MV.cm^{-1}$, which exceeds the fields used for devices presented in this thesis by an order of magnitude.

Tolerable trap density of the dielectric for atomic-scale devices

The interface between a dielectric and a semiconductor is often disordered, which prevents a small number of atoms at the interface from satisfying their desired bond structure, and creates dangling bonds that trap charge. For single electron transistors, and eventually

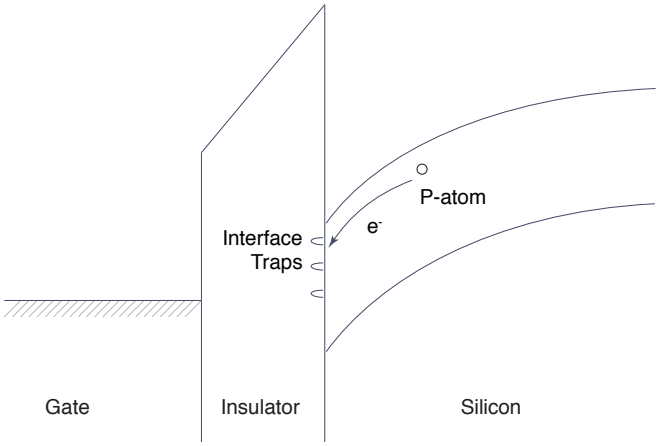


Figure 3.5: Band diagram depiction of the interaction between interface traps and a buried donor. The interface between a silicon substrate and the gate insulator is rarely perfect. Interface traps from dangling bonds at the interface are unable to form a covalent bond with surrounding atoms. This trap affects nearby electrons, either by trapping them or by altering their conduction path through Coulombic or spin-scattering.

solid-state quantum computers, it is important that the interface is relatively free of traps, since they perturb spins within the device. This perturbation can manifest as Coulombic or spin scattering of the carrier, or as physical trapping of the conduction electron, as shown in Fig. 3.5. Trapping and de-trapping events near an SET result in a shift in the local chemical potential, causing a shift in the operating point of the SET. If the SET is used as a sensitive electrometer, as with spin-to-charge readout schemes in quantum computing, it may be tuned to a Coulomb blockade resonance. Any major change in the SET potential would shift the SET off resonance, preventing it from detecting charge. Furthermore, charge traps may have an associated spin that can affect electron transport, which is particularly important for spin-qubits.

Charge trapping events are dominated by traps at the silicon-insulator interface, since the influence of a trap buried more than a few nanometres into the insulator is minimised by the intervening dielectric material. The key to minimising trapping and de-trapping events is therefore to reduce the areal density of interface traps (N_{it}), though one typically measures the density of interface traps as a function of the surface potential (D_{it}), since it is simpler to extract using capacitance-voltage techniques. The relationship between the two is

$$N_{it} = \int_0^{E_g} D_{it}(E).dE, \tag{3.6}$$

where E is the energy of the trap relative to the valence band maximum. The integral

is performed over the entire band gap, up to the conductance band minimum (where $E = E_g$). Although D_{it} describes a distribution of traps as a function of energy, D_{it} figures are typically quoted as the corresponding value of the distribution at mid-gap ($E = E_g/2$). Furthermore, since the band gap of silicon is approximately $E_g \simeq 1eV$, the magnitude of D_{it} in $cm^{-2}.eV^{-1}$ is of the same order as N_{it} in cm^{-2}. For silicon dioxide on silicon substrates, the interface trap density typically ranges from $D_{it} = 10^{12}.cm^{-2}.eV^{-1}$ for an unoptimised oxide to $D_{it} = 10^{10}.cm^{-2}.eV^{-1}$ after thermal annealing in a hydrogen-containing ambient (∼5%), although values as low as $D_{it} = 10^{9}.cm^{-2}.eV^{-1}$ have been reported by Reed *et al.* [44] by optimising the anneal temperature, time and gate metal.

A trap situated more than $100nm$ away from the path of conduction electrons is statistically unlikely to affect electron flow, provided that the intervening substrate is non-conducting and there are no metallic elements capacitively coupling the device to the trap. A mean distance between traps in excess of $100nm$ implies an areal interface trap density of $N_{it} < 10^{10}cm^{-2}$, which has been achieved with highly-optimised SiO_2 processes [44].

Required gate selectivity in atomic scale devices

The phosphorus donors patterned with STM lithography are encapsulated with epitaxially-grown silicon, which buries them below the silicon surface (Fig. 3.6(a)). When the patterned donors are positioned $20nm$ below the surface, the interaction of donors with traps at the interface is minimal [10]. In the Kane architecture, the distance to the metallic gates situated above each donor affects the gate selectivity. As an example, Fig. 3.6(a) shows a simplified schematic of the electric field produced by surface gates in the Kane architecture: The field produced by each gate affects neighbouring donors. If the gates are moved physically further from the donors (either by increasing the depth of the silicon or the thickness of the insulator), the selectivity of the gate decreases. A simplification of this effect is shown in Fig. 3.6(b). The gate selectivity influences the rate at which neighbouring donors inadvertently undergo a spin rotation while addressing a qubit. To improve selectivity, we must either decrease the distance between the gate and donor, or increase the magnitude of the applied field.

Pakes *et al.* have studied how device geometry and gate voltages affect gate selectivity in the Kane architecture [73]. They report that a $5nm$ layer of silicon dioxide requires $\sim 0.5V$ applied to the gate in order to achieve the desired error rate of neighbouring spin flips (without using a back-gate). Beyond an oxide thickness of $15nm$, the associated reduction in gate selectivity requires an electric field that exceeds the breakdown field strength of silicon dioxide. For this reason, the insulator used within the Kane architecture

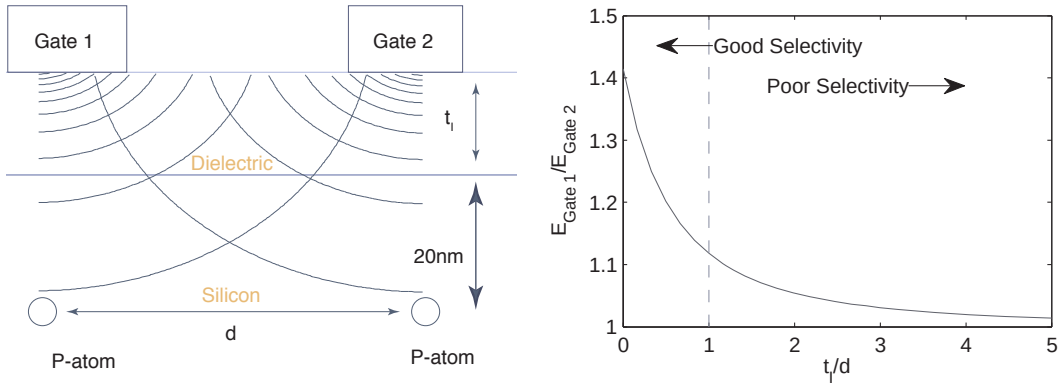


Figure 3.6: Selectivity of top-gates as a function of dielectric thickness (a) Side profile of the electric field produced by adjacent gates. (We note that there is ideally a step change in the magnitude of the electric field at the Si–insulator interface according to Maxwell's equations, which has been omitted for clarity). (b) Relative electric field induced at the left P-atom in (a) with varying insulator thickness, t_I. When the thickness of the insulator exceeds the separation between donors, d (such that $t_I/d > 1$), the selectivity of gates to their respective donors is poor.

must be physically thin. This may be mitigated by bringing the donors closer to the interface, but this approach is only practicable with low interfaces state densities; for example, Clarke *et al.* have shown that donors become electrically inactive when brought within $8nm$ of the native oxide [74] — however, the interaction between donors and the silicon surface is part of an ongoing investigation within our group. For this reason, the ultimate goal will be to develop a process that is able to fabricate a suitable dielectric that is less than $\sim 15nm$ thick, to make it compatible with the Kane architecture. For the initial proof of principle surface-gated STM patterned quantum dots presented in this thesis however, we do not place an upper limit on the dielectric thickness.

Summary of the dielectric requirements for STM-patterned devices

The targeted performance of the low-temperature UHV-compatible dielectric is summarised in Table 3.1. Some of these requirements are trivial to achieve — for instance, the breakdown field strength — while most will be very challenging, requiring compromise to find the best low temperature dielectric. Having established the requirements of the dielectric for STM-patterned devices, let us now consider which gate dielectrics are most appropriate.

Table 3.1: Ideal performance of the low-temperature UHV dielectric for atomic-scale devices.

Property	Symbol	Target Value
Breakdown field strength	E_{BD}	$\geq 1 MV.cm^{-1}$
Leakage current density	J	$\leq 10^{-6} A.cm^{-2}$ at $0.5 MV.cm^{-1}$
Interface trap density	D_{it}	$\leq 10^{10} cm.^{-2}.eV^{-1}$
Oxide thickness (for selectivity)	t_{ox}	$\leq 15nm$
Growth chamber base pressure	p_{base}	$\leq 10^{-10} mbar$
Thermal budget	T_{budg}	210–300°C for $3hrs$

3.2.2 Review of low temperature dielectrics

Table 3.2 lists a series of materials and techniques used to form gate dielectrics in silicon devices, including high-κ dielectrics, silicon dioxide, and—at the upper margins of the thermal budget—Si-$SiGe$ heterostructures. We will now review these alternatives with reference to the requirements set out in the previous section. We can immediately see that few techniques satisfy our calculated temperature limit for a $3hr$ growth (210–300°C). While it is possible to accommodate higher temperatures by growing the dielectric faster, we can safely rule out those techniques highlighted in bold ($T \geq 600°C$) as the necessary growth time is around one minute, which exceed the growth rate of every tabulated technique for insulator thicknesses of $t_I > 5nm$. Of the remaining techniques, let us consider the most appropriate material for our application.

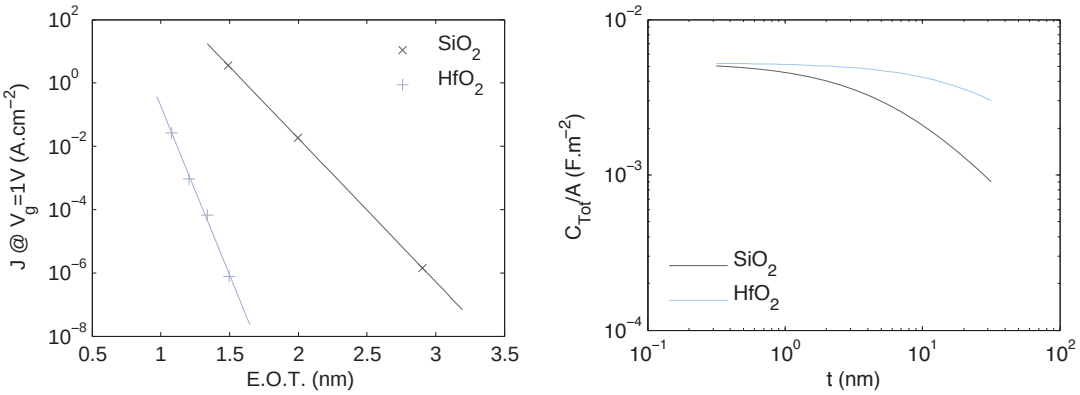
High-κ dielectrics

Further scaling of CMOS technology requires continued improvements in the gate capacitance of MOSFET devices, which has recently necessitated a switch to high-κ gate dielectrics. The semiconductor industry has selected HfO_2 as their preferred high–κ dielectric since it represents a good compromise between dielectric constant, gate leakage, and interface state density, as described by Wilk [95] and Robertson [96]. While alternative high-κ materials such as La_2O_3 perform better against these criteria, they are incompatible with CMOS manufacturing processes (La_2O_3 is hygroscopic).

In high-κ materials, one typically expresses the leakage with respect to the equivalent oxide thickness (EOT) so that the leakage curve is scaled according to the equivalent-field

Table 3.2: A summary of different dielectrics on silicon. Several of the listed techniques satisfy the calculated thermal budget for the atomically-precise fabrication scheme. The growth methods are abbreviated as follows: chemical vapour deposition (CVD), plasma-enhanced chemical vapour deposition (PECVD), molecular beam epitaxy (MBE), thermal oxidation using a liquid (wet) or gas (dry) oxidant, plasma-generated atomic oxygen (Atomic O), and ultra-voilet light assisted oxidation using ozone (UV + O_3). The temperature specified as 'RT' for atomic oxygen refers to room temperature.

Material	ψ_B eV	Growth Method	T °C	D_{it} $cm^{-2}.eV^{-1}$	Source
High-κ Dielectrics					
Al_2O_3	2.8	Dry thermal	**800–1100**	1×10^{11}	[75]
$SrTiO_3$	0	MBE	**850**	$1–6 \times 10^{11}$	[76]
HfO_2	1.4	CVD	400–550	$1–6 \times 10^{11}$	[77]
ZrO_2	1.5	CVD	400–550	$1–6 \times 10^{11}$	[78]
La_2O_3	2.3	Dry thermal	400–500	3×10^{10}	[79]
Si_3N_4	2.4	PECVD	60	$1–3.5 \times 10^{11}$	[80]
Heterostructures					
Si–SiGe	0.05–0.2	CVD, MBE	350–**750**	N/A	[81–85]
Silicon Dioxide					
SiO_2	3.2	Dry thermal	**1000**	$\sim 2 \times 10^9$	[44]
		Wet thermal	**900**	$0.3–1 \times 10^{11}$	[86]
			600	3.4×10^{11}	[87]
		PECVD	350	5×10^{11}	[88]
			250	3×10^{10}	[89]
			30	6.3×10^{11}	[90]
		UV + O_3	300	2×10^{11}	[91, 92]
		Atomic O	RT	2×10^{11}	[93]
			RT	1×10^{11}	[94]



(a) (b)

Figure 3.7: Relative tunnelling current density and capacitance of SiO_2 and HfO_2. (a) Measured leakage current density of HfO_2 and SiO_2 as a function of the equivalent oxide thickness (scaled by the dielectric constant). After Ref. [96]. (b) This figure shows the effective capacitance of both SiO_2 and HfO_2 with a $20nm$ layer of silicon between the oxide and the patterned device. The silicon layer limits the total capacitance, which minimises the capacitance gains of high-κ materials..

produced by SiO_2. For the Kane architecture however, there is the additional constraint that the dielectric must ultimately be thin ($\sim 5nm$) if we are to achieve the required gate selectivity. However an HfO_2 layer must be over three times thicker than SiO_2 to achieve the same leakage current density as SiO_2. As a consequence, the applied gate voltage must be larger by almost an order of magnitude to achieve the same error rate in neighbouring spin flips, meaning that high-κ materials may actually lead to greater leakage currents for the same qubit fidelity. Moreover, virtually every form of high-κ dielectric has a high density of interface traps—typically an order of magnitude greater than SiO_2—and has atomic species with a non-zero nuclear spin, which will adversely affect the operation of spin qubits. In addition, high-κ dielectrics are also typically more challenging to grow, so there is little benefit of high-κ dielectrics for STM-patterned devices in their current form, particularly for a practical implementation of electron spin qubits in silicon.

Silicon/silicon-germanium

In Kane's original article outlining a solid-state quantum computer, he indicated that Si–$SiGe$ heterostructures may be required if we are to achieve sufficiently low levels of disorder, in preference to SiO_2 [10]. Figure 3.8 shows an example Si–$SiGe$ heterostructures one might use to confine conduction electrons to a potential well, adapted from the review of Si–$SiGe$ heterostructures by D.J. Paul [85], which shows a potential barrier of $\psi_B = 200meV$ formed at the hetero-interface. To make Si–$SiGe$ heterostructures in a manner

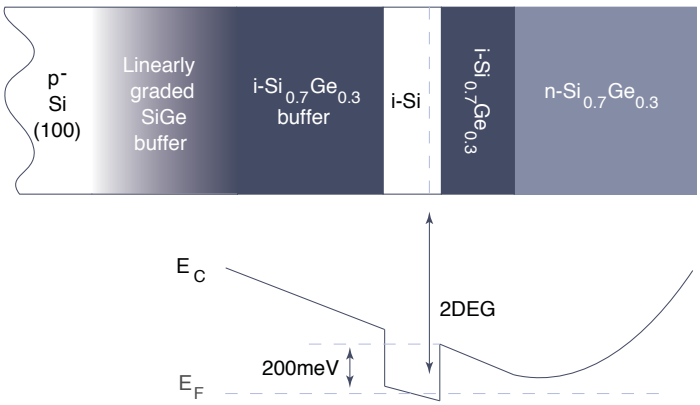


Figure 3.8: Potential Si-SiGe heterostructure for Si:P qubits. This heterostructure starts from a p-type silicon substrate, upon which a graded $SiGe$ is grown, where the atomic fraction of Ge increases linearly from 0% to 30% (Ge is represented here as dark blue, Si is white). Upon the graded buffer layer, a constant composition buffer layer is grown with 70% Si and 30% Ge. This is covered with a layer of intrinsic silicon that is capped with another constant-composition $SiGe$ layer, and finally a doped $SiGe$ cap. The lattice mis-match between the constant composition buffer layers and the intrinsic silicon layer between them strains the intrinsic silicon and creates a band discontinuity, which appears as a potential well in the band diagram. Adapted from Ref. [85]

compatible with STM lithography, we need to pattern our phosphorus dopants within the intrinsic silicon layer ($i - Si$ in Fig. 3.8). We could then use Schottky surface gates to induce, for example, single electron transistors for charge sensing in a manner similar to those published by the group of Eriksson *et al.* [97].

To maintain the clean, ultra-high vacuum environment required by the STM-fabrication scheme, it would be necessary to grow these Si–$SiGe$ heterostructures with molecular beam epitaxy (MBE). Several groups have successfully grown Si–$SiGe$ heterostructures using MBE, for example see the MBE-grown Si–$SiGe$ FETs of Mack *et al.* [83], or the quantum cascade structures of Zhao *et al.* [84]. Typically, $SiGe$ growth is carried out at temperatures of 500–600°C, which is at the upper margins of the thermal budget we have calculated for minimal phosphorus diffusion. However, Zhao have recently demonstrated MBE $SiGe$ growth on virtual substrates at 350°C, with growth rates of $0.02nm.s^{-1}$. If we assume the required gate stack is $\sim 100nm$ thick, it could be grown in $90min$ using this technique, which is within range of our thermal budget at this temperature ($x_j = 0.75nm$). However, growing at such low temperatures leads to defects or dislocations in the crystal growth that may act as charge traps. Additionally growing graded $SiGe$ buffers requires precise control of the growth parameters and continual calibration of the growth process

(both *in situ* and *ex situ*) using, for example, X-ray diffraction (XRD) measurements. A critical issue we must also consider is how the reduction in disorder is offset by the inevitable increase in gate leakage one sees when using a *Si–SiGe*–Schottky gate stack, since the strain-dependent barrier formed at the *Si–SiGe* interface typically lies within the range of 50–200meV [85] compared with $\sim$3.2eV of SiO_2. As a consequence, we do not pursue *Si–SiGe* in this thesis. However parallel efforts within our group are seeking to develop a suitable process window for growing epitaxial *SiGe* in a manner compatible with our STM-fabrication scheme.

Silicon dioxide as a low temperature dielectric

Silicon dioxide has been widely used as a dielectric in semiconductor devices for over 50 years since the barrier it forms with silicon is very high (3.2eV, see Table 3.2), and the interface between silicon dioxide and silicon is typically sharp ($< 1nm$) and relatively free of traps ($D_{it} \simeq 10^{10} cm^{-2}.eV^{-1}$). Indeed, this has been a large part of silicon's popularity as a semiconductor since the mid-twentieth century.

The growth of silicon dioxide on silicon is straight-forward; it only requires the supply of oxygen to the substrate because the reaction between silicon and oxygen occurs readily at room temperature. The oxidation rate is described by the Deal-Grove model [41], and has been shown to decrease as the oxide forms so that the oxide terminates at $\sim$2nm after several days at room temperature. The Deal-Grove model attributes the slowing of the growth to the increase in the time required for oxygen to diffuse through the oxide as it forms [41]. Creating oxide layers of a practical thickness for a gate dielectric ($t_I \geq 5nm$) has therefore traditionally required heating the substrate to high temperatures ($T > 800°C$), to promote diffusion of oxygen through the oxide layer.

Over the past two decades, there has been a shift towards the use of silicon-dioxide in a variety of temperature sensitive applications, in particular for thin film transistors used in liquid crystal displays [89, 93, 98–108]. Consequently, a number of techniques are being developed to deposit silicon dioxide at low temperatures, some of which are within the thermal budget of the STM-fabrication scheme. These low-temperature alternatives are more challenging to grow than conventional furnace processes, and tend to form lower quality dielectrics. As such, it is challenging to achieve the desired interface trap density of $D_{it} \simeq 10^{10} cm^{-2}.eV^{-1}$, but as shown in Table 3.2, several groups have achieved results in this range using low-temperature SiO_2. The remaining requirements set out in this chapter — in particular, growth temperature, UHV compatibility, gate leakage, and gate selectivity — are more likely to be achieved using SiO_2 than with the other materials we

have discussed.

Selecting SiO_2 as our preferred candidate for the low-temperature dielectric

Silicon dioxide represents a good compromise between simplicity and performance. It forms a large potential barrier with the silicon substrate, giving low leakage currents. It also produces high quality interfaces, especially compared to that of high-κ materials, while remaining physically thin, as required by gate selectivity constraints of the Kane architecture. As such, silicon dioxide was selected as the preferred material system for this study, although high-κ dielectrics and Si–$SiGe$ heterostructures will be developed in parallel as part of a long-term strategy within our group, especially as their respective growth processes continue to improve.

3.2.3 Review of low temperature techniques for depositing SiO_2

In traditional thermal oxidation processes, the diffusion of oxygen through the oxide is driven by heat. Low-temperature oxidation techniques must therefore compensate for an inherent lack of thermal energy. This energy can be supplied chemically using alternative oxidants, as with atomic layer deposition, or electrically, as with anodic oxidation. However, in the majority of cases, energy is supplied in the form of electromagnetic radiation; such techniques include plasma-enhanced chemical vapour deposition, ultra-violet light and ozone, and plasma-generated atomic oxygen. Here we explore techniques for growing low-temperature oxides and assess their compliance with the requirements set out previously in this chapter.

Atomic layer deposition

Atomic layer deposition (ALD) is used to deposit substances step-wise in single atomic layers, typically through exposure to alternating gaseous species. After an initial surface preparation, the surface is exposed to a reactant that binds to the surface and leaves a functional group exposed, to which a second reactant may bond. The second reactant binds to the new surface, leaving a functional group to which the first reactant may bond. An ALD material is deposited through a sequence of many such exposures to the precursor gases.

Klaus *et al.* have developed an ALD technique to grow SiO_2 on Si that uses sequential half reactions of $SiCl_4$ and H_2O, with a pyridine (C_5H_5N) catalyst [98]. The two half

reactions proceed according to the reactions

$$SiOH^* + SiCl_4 \rightarrow SiOSiCl_3^* + HCl \tag{3.7}$$

$$SiCl^* + H_2O \rightarrow SiOH^* + HCl, \tag{3.8}$$

where the asterisks denote the surface species. Using these two half-reactions, Klaus *et al.* were able to grow oxide layers at room temperature in a vacuum ($< 200mTorr$). However, the electrical performance and interface trap densities of the oxides formed were not reported. This technique is therefore capable of producing oxides within our thermal budget, but without knowing the electrical performance of the oxides it forms, nor whether we could adapt the technique to ultra-high vacuum growths, we decided not to pursue this strategy.

Anodic oxidation

Anodic oxidation is the process of oxidising a substance through electrochemical processes. The use of anodic oxidation to grow silicon dioxide appears in scientific literature as early as 1957 [99]. More recently, anodic oxidation has been studied by Clark *et al.* as a means of producing ultra-thin oxides for MOS devices at low temperatures [100]. Clark *et al.* fabricated oxides using aqueous solutions of NH_4OH, thus avoiding contamination associated with more traditional reactants containing potassium [109] that have deleterious effects on the reliability of gate oxides. However, Clark's oxides only became stoichiometric after a post-oxidation anneal at temperatures in excess of $700°C$. After annealing their oxides at this temperature, they were able to achieve interface trap densities of $D_{it} \simeq 4 \times 10^{10}.cm^{-2}.eV^{-1}$ [101]. It was not possible to measure the as-grown oxides because the hysteresis and leakage characteristics were too poor to record a quasi-static C-V curve. Therefore, although anodic oxidation is a practical means of growing oxides at low temperature, the oxide films formed are not viable gate dielectrics without performing a high temperature anneal ($700°C$ for $\sim 10min$) that exceeds our thermal budget ($x_j \simeq 2nm$). Furthermore, the use of aqueous solutions to grow the oxide is not compatible with our ultra-high vacuum fabrication scheme.

Plasma enhanced chemical vapour deposition

Applying an alternating electromagnetic field to a conductive material induces eddy currents that generate local heating. The degree of heating is determined by the magnitude and frequency of the applied field. For high frequencies and fields, the material may

reach sufficient temperatures to dissociate into its constituent ions, forming a plasma. This process is frequently used in the semiconductor industry for a process known as plasma-enhanced chemical vapour deposition (PECVD). In the case of PECVD, the electromagnetic field is typically supplied at radio-frequencies (e.g. 13.56MHz), which enables efficient coupling of the RF energy to the source materials [110]. In the case of PECVD-grown silicon dioxide, the source materials are typically gases such as SiH_4, and O_2 or N_2O.

Batey *et al.* were among the first to optimise PECVD-grown silicon dioxide to a sufficient extent that it could be used as a gate dielectric [111]. They grew SiO_2 films using SiH_4 and N_2O in a ratio of 1:125 to achieve stoichiometric oxides. The plasma was exposed to silicon substrates held at low temperatures ($275°C$). Batey *et al.* found a He carrier gas was necessary to reduce the pre-cursor gas flow rate sufficiently to produce robust oxides able to withstand electric fields in excess of $5MV.cm^{-1}$. The electrical quality of the as-grown oxide was similar to that of thermally grown oxide before annealing: $D_{it} \simeq 1 \times 10^{12}.cm^{-2}.eV^{-1}$. After a post-metallisation anneal at $400°C$ for $30min$ this reduced to $D_{it} \simeq 4 \times 10^{10}.cm^{-2}.eV^{-1}$.

More recent changes of source gas, for example to tetraethylorthosilicate (TEOS), have produced gate oxides with as-deposited trap densities in the range $D_{it} \simeq 9 \times 10^{10}.cm^{-2}.eV^{-1}$ at a growth temperature of $250°C$ [89]. PECVD is thus able to produce high-quality gate dielectrics at temperatures within the thermal budget we have calculated. However, once again traditional PECVD is not strictly UHV compatible, as the growth occurs at relatively high pressures ($\sim 1Torr$).

Ultraviolet light and ozone

When ozone strikes a silicon surface it dissociates into molecular O_2 and atomic-O. Atomic O diffuses more readily through an oxide than molecular oxygen, which enhances the oxidation rate. The process can be augmented by irradiating the system with UV light to generate more O_3 from the excess molecular O_2. Ozone gas has been used to oxidise silicon by several research groups [102–107]. Kazor *et al.* used locally-generated ozone to oxidise silicon at atmospheric pressure [102]. They found the oxidation rate to be ∼75 times that of molecular O_2 at a substrate temperature of $550°C$, and that the first ten Angstroms of oxide were indistinguishable from that of thermal oxides using FTIR and ellipsometry. These findings agree with more recent FTIR experiments conducted by Cui *et al.* [103]. Cui also performed electrical analysis (C-V) of the formed oxide and found an interface trap density of $D_{it} \simeq 3.7 \times 10^{11}.cm^{-2}.eV^{-1}$, which is around one third of their molecular

oxygen control samples grown under the same conditions. Nishiguchi *et al.* reported the use of a similar process to produce gate oxides with $D_{it} \simeq 5 \times 10^{10}.cm^{-2}.eV^{-1}$ at $400°C$ [107]. At this temperature Nishiguchi's process is able to grow oxides of $t_I > 5nm$ within $30min$, which is within our calculated thermal budget ($x_j \simeq 0.4nm$). However, the process itself occurs at atmospheric pressure, which is incompatible with our UHV fabrication scheme.

Atomic oxygen generated by an oxygen plasma

As an alternative to PECVD, an RF field may be applied to oxygen gas to produce a plasma that consists of highly energetic oxygen ions and neutral oxygen radicals. These energetic species are more chemically reactive than molecular oxygen [112, pg. 5]. As stated for ozone oxidation, atomic oxygen diffuses more readily through an oxide as it forms. As a consequence, plasma-generated atomic oxygen is able to rapidly oxidise a silicon substrate at room temperature.

Engstrom *et al.* have extensively studied the use of oxygen plasmas to oxidise silicon [68]. Engstrom's apparatus consisted of a plasma source that generated atomic oxygen remotely from the sample, thus preventing bombardment of the sample with radiation from recombination events within the plasma that can damage the oxide. Engstrom *et al.* reported that below a temperature of $900K$, the growth proceeded by a layer-by-layer mechanism, with an initial chemisorption saturation dose of approximately four monolayers. Engstrom *et al.* were able to grow oxides down to a temperature of $110K$; their XPS data indicated that oxides grown at such low temperature where not stoichiometric.

Majamaa *et al.* have also grown oxides using a remotely ionised plasma in a vacuum ($2 \times 10^{-5}mbar$)[93]. They were able to demonstrate good electrical performance, with un-annealed interface trap densities of $D_{it} \simeq 3 \times 10^{11}.cm^{-2}.eV^{-1}$ at room temperature. Their growth was performed step-wise, adding $1nm$ of oxide per $10min$, which is well within our calculated thermal budget for a $5nm$ oxide ($x_j = 0.1nm$). Moreover, this process is compatible with an ultra-high vacuum system, since the maximum pressure (only required during growth) is $2 \times 10^{-5}mbar$, which would allow the apparatus to idle at UHV pressures ($\sim 10^{-11}mbar$).

Summary of process selection

Table 3.2 summarises each of the low temperature SiO_2 deposition techniques we have discussed. Each technique is a viable candidate for producing SiO_2 gate dielectrics at low temperature. Of the listed methods, we have elected to use plasma-generated atomic-oxygen in this thesis since it has been proven to grow SiO_2 under conditions compatible

Table 3.3: Low temperature techniques for depositing silicon dioxide. The temperature value 'RT' refers to room temperature.

Growth	T °C	D_{it} $cm^{-2}.eV^{-1}$	p_{growth} mbar	Source
ALD	RT	–	0.3	[98]
Anodic	RT–700	4×10^{10}	N/A	[99–101]
O_3 & UV	300–550	5×10^{10}–4×10^{11}	∼1000	[102–107]
PECVD	250–600	5×10^{10}–1×10^{11}	1.3	[89]
Atomic O	RT	3×10^{11}	3×10^{-5}	[93, 108]

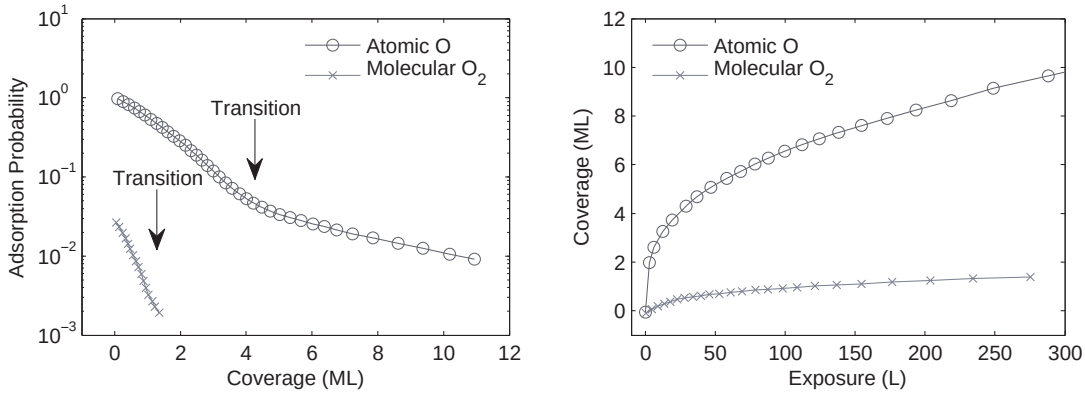
with an ultra-high vacuum environment ($p_{growth} = 3 \times 10^{-5} mbar$), and to produce comparatively low interface trap densities at room temperature ($D_{it} = 3 \times 10^{11} cm^{-2}.eV^{-1}$) [93].

3.2.4 Plasma-assisted growth of silicon dioxide in ultra-high vacuum

Engstrom *et al.* have studied the use of a remotely-ionised oxygen plasma to oxidise silicon in a vacuum [68]. When exposed to a silicon substrate, atomic oxygen adsorbs more readily to the surface than molecular oxygen, as shown in Fig. 3.9(a). Incident atomic oxygen adsorbs to the bare silicon surface with almost 100% probability, compared with ∼3% for molecular oxygen.

As the surface becomes saturated with oxygen, the incident oxygen must diffuse through the oxide to reach the substrate below, which leads to a transition in the adsorption probability (shown in Fig. 3.9(a)). Engstrom *et al.* also found that diffusion occurred more readily for atomic oxygen. This is shown in Fig. 3.9(b), in which the net coverage of atomic oxygen is an order of magnitude greater than that of molecular oxygen after an exposure of 250 monolayers. Using atomic oxygen as an oxidant therefore aids the speed and extent to which silicon oxidation progresses, particularly at low temperatures. This is an important factor in minimising the time required to deposit the dielectric, and thus the out-diffusion of dopants in our devices.

In 1998, Majamaa *et al.* used an RF oxygen plasma source to grow silicon dioxide at room temperature of sufficient quality for gate dielectrics [93]. Their study showed that using the oxygen flux alone, it was impractical to grow silicon dioxide layers thicker than $1nm$. Their solution was to use a layered growth mechanism in which the silicon surface



(a) (b)

Figure 3.9: Adsorption probability and diffusion of atomic and molecular oxygen. (a) Neutral atomic oxygen adsorbs to the bare silicon surface with almost 100% certainty. Under identical conditions, molecular oxygen adsorbs to the surface with approximately 3% probability. After a coverage of four monolayers of oxide, the adsorption probability of atomic oxygen transitions between a 'fast' and 'slow' mechanism. This transition occurs at approximately one monolayer for molecular oxygen. From Ref. [68] (b) Atomic oxygen adsorbs more readily to a silicon surface than molecular oxygen, so that an oxide of several monolayers forms rapidly when exposed to atomic oxygen. After an oxide forms, the diffusion of oxygen species through the oxide to the underlying silicon substrate is also much faster for atomic oxygen so that after a surface is exposed to $300 M.L.$ of each oxidant, an oxide formed with atomic oxygen is almost an order of magnitude thicker. From Ref. [68]

was first oxidised using the oxygen flux, upon which a 6Å layer of silicon was deposited. The deposited silicon layer was subsequently oxidised. Using several such layers, oxides were generated with more practical thicknesses of $5nm$ with good initial interface trap densities ($D_{it} = 3 \times 10^{11} cm^{-2}.eV^{-1}$).

Several authors have also reported room-temperature growth of silicon dioxide without the need for a layered growth process using a coincident flux of silicon and atomic oxygen [94, 113]. Under such conditions, Molinari were able to reach an oxide thickness of $200nm$ at $100°C$ with a growth rate of $1Å.s^{-1}$ [113]. Using a layered or co-deposited growth process decouples the growth temperature from the thickness of the oxide. As such, thick oxides ($t_I > 5nm$) may be formed without the need for significant substrate heating. This is beneficial for STM patterned devices, as gate leakage currents can be kept to a minimum using thicker oxides without exceeding the strict thermal budget imposed by dopant diffusion constraints.

The oxide deposition scheme presented in this thesis has been divided into two stages, as shown in Fig. 3.10. First, the surface of the silicon is exposed to the plasma-generated atomic oxygen, Fig. 3.10(a). This creates an oxide on the order of 0.5–1nm thick. This

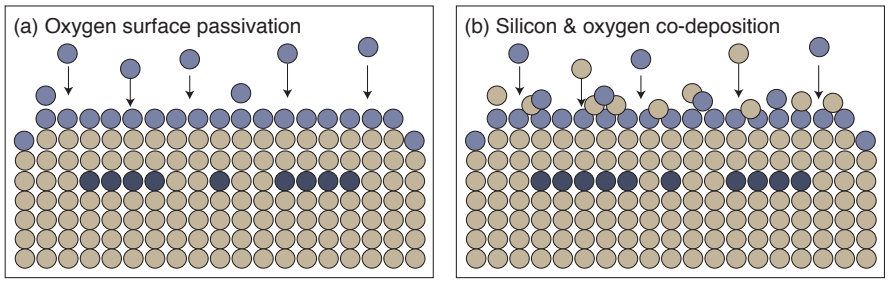


Figure 3.10: Depositing a low-temperature oxide on an STM-patterned device. (a) The surface of the silicon encapsulation layer is first passivated by exposure to a flux of atomic oxygen. This passivation layer forms the interface between the silicon substrate and the oxide to be deposited. Growing this layer using only atomic oxygen will provide interfaces similar to those of Majamaa *et al.* (b) The passivated surface is then buried by a thick oxide layer, which is deposited using a coincident flux of oxygen and silicon.

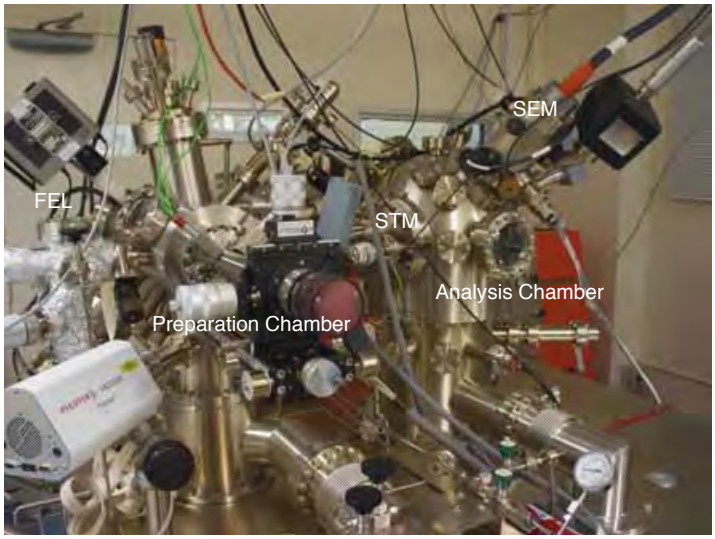


Figure 3.11: Custom multiscan STM-SEM system used to fabricate STM-patterned devices. The system is composed of a fast-entry load lock (FEL) (far left), preparation chamber (left), and analysis chamber (right). The analysis chamber includes an SEM and STM with the same focal point.

layer defines the interface between the oxide and the silicon substrate, which is expected to generate interfaces similar in quality to that achieved by Majamaa *et al.* [93].

The second stage in the oxidation process is to co-deposit silicon and oxygen to grow a thick, uniform layer of silicon dioxide, as shown Fig. 3.10(b). This stage proceeds until the desired oxide thickness is reached. The two-stage process we have developed requires independent control over the flux of silicon and atomic oxygen. To achieve this, a dedicated ultra-high vacuum chamber was designed for this thesis and integrated into the STM system.

3.2.5 UHV STM-SEM and oxidation system

A custom multi-scan STM-SEM system used to fabricate devices for this thesis was manufactured by Omicron NanoTechnology GmbH, and installed in our laboratory in 2002. In 2005 we added an additional chamber to the original system, designed to grow a low temperature oxide under UHV on STM-patterned samples. The resultant system comprises several interconnected UHV chambers, with the three main chambers being the analysis chamber, preparation chamber, and the oxide chamber. All three chambers were equipped with Varian Star Cell ion pumps and titanium sublimation pumps to maintain an ultra-high vacuum of 2–5 $\times$ $10^{-11}mbar$, measured using an ion gauge. The operation of the oxide chamber will be described in greater detail in the next section, here we focus on the analysis and preparation chambers.

Preparation chamber

The preparation chamber is used to prepare the samples for imaging or patterning with the STM. All samples are loaded into the preparation chamber via a fast entry load-lock (FEL), which is a very small volume chamber in which samples from the clean room are placed and pumped down to high vacuum ($\sim 10^{-6}mbar$) using a Pfeiffer turbo-molecular pump. The sample are then moved from the FEL to the preparation chamber.

The preparation chamber itself consists of a heated sample stage that is used to bake all volatile adsorbates from the sample (e.g. water) after they are loaded into the system. The sample manipulator allows us to pass current directly through the silicon sample to heat it to the high temperatures required to give the desired Si (001) surface reconstruction. The preparation chamber also includes a phosphine dosing system used to expose the sample to phosphine gas for sample doping. There is also a hydrogen cracker, used to crack molecular hydrogen into atomic hydrogen by passing it over a hot ($1400°C$) tungsten filament. Finally, there is a SUSI 63 silicon sublimation cell from MBE Komponenten, which is used for epitaxial growth of silicon on the STM-patterned device.

Analysis chamber

The analysis chamber consists of a scanning tunnelling microscope (STM) and a scanning electron microscope (SEM) in a single chamber. The SEM focal point is the sample stage when positioned for STM imaging. Under this arrangement, it is possible to precisely locate the tip at a desired point on the sample surface. The system also includes an optical positioning readout mechanism to track the tip location with a precision of $\sim 10nm$. This

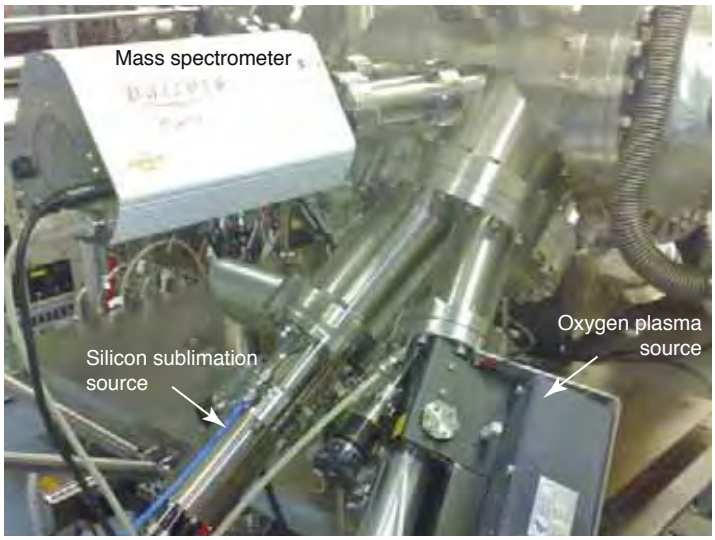


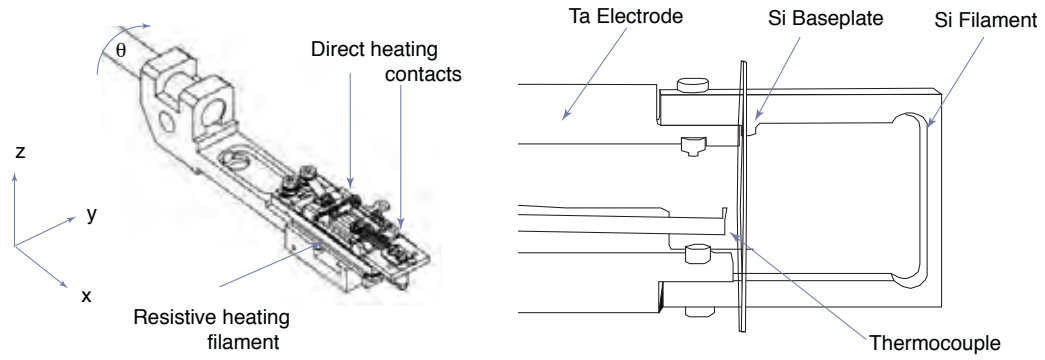
Figure 3.12: Custom oxide chamber used to form a low temprature oxide in UHV. The oxide chamber is composed of a silicon sublimation source (lower left) and an oxygen plasma source (lower right), both focused at the sample manipulator in the centre of the chamber.

chamber is used to image and pattern hydrogen terminated silicon surfaces with the STM tip. The location of the tip relative to etched registration markers in the sample is recorded using the SEM, which allows us to locate the STM-patterned device once the sample has been removed from the UHV system.

3.3 UHV oxide chamber

3.3.1 Design of the UHV oxidation chamber

We have developed a technique to deposit silicon dioxide at low temperatures in a UHV environment. This technique is based on oxidising the surface of the silicon sample with a flux of atomic oxygen. As the surface is oxidised, more silicon is deposited on the sample, slowly forming the oxide through the co-deposition of silicon and oxygen rather than diffusing oxygen into the silicon substrate. The flux of atomic oxygen is generated with an oxygen plasma source. The silicon flux is generated using a silicon sublimation source. Both sources are contained within a dedicated oxidation chamber, which is attached to the ultra-high vacuum STM system used to fabricate STM-patterned devices. This oxide chamber is shown in Fig. 3.12. Here we will describe the oxidation chamber, including both the atomic oxygen and silicon sources, and the parameters used to form the low



(a) (b)

Figure 3.13: Sample manipulator and silicon source. (a) The sample manipulator can be moved in all three spatial dimensions to put it at the point of coincidence of the oxygen and silicon flux. The manipulator can be rotated about the x-axis to shield it from the oxygen and silicon sources as necessary. The manipulator includes two mechanisms to heat the sample: A resistive tungsten element placed below the sample holder, and electrical contacts to pass a current through the sample itself, heating it directly. (b) The silicon is sublimated from a high-purity silicon filament, bolted to water-cooled tantalum electrodes. A silicon base plate and surrounding shroud (not shown) are used to shield the filament from any non-silicon parts. A thermocouple is used to measure the filament temperature.

temperature oxide. The oxide chamber is composed of three major components: A sample manipulator, a silicon sublimation source, and an RF plasma source.

Sample manipulator: The sample manipulator has three degrees of freedom to control the position of the sample (x, y, z), shown in Fig. 3.13(a), which allows the sample to be aligned to the point of coincidence of the oxygen and silicon flux. The manipulator can also be rotated about the x-axis, θ in Fig. 3.13(a), enabling the sample to be rotated directly into the oxygen and silicon flux, or rotated away from the flux when the growth is finished. The manipulator includes two heat sources to set the sample temperature: a resistive heating element is placed below the sample holder, which may be used to heat the sample through radiation and conduction; the sample holder is also designed to pass a current through the sample and heat it directly. The manipulator includes a thermocouple to measure the sample temperature, and the chamber includes a viewport aligned so that the sample temperature may be measured with a pyrometer.

Silicon source: The silicon source is a SUSI 63 silicon sublimation cell from MBE Komponenten, shown in Fig. 3.13(b). It consists of a high-purity silicon filament, supported by water-cooled tantalum electrodes. Current is passed through the silicon

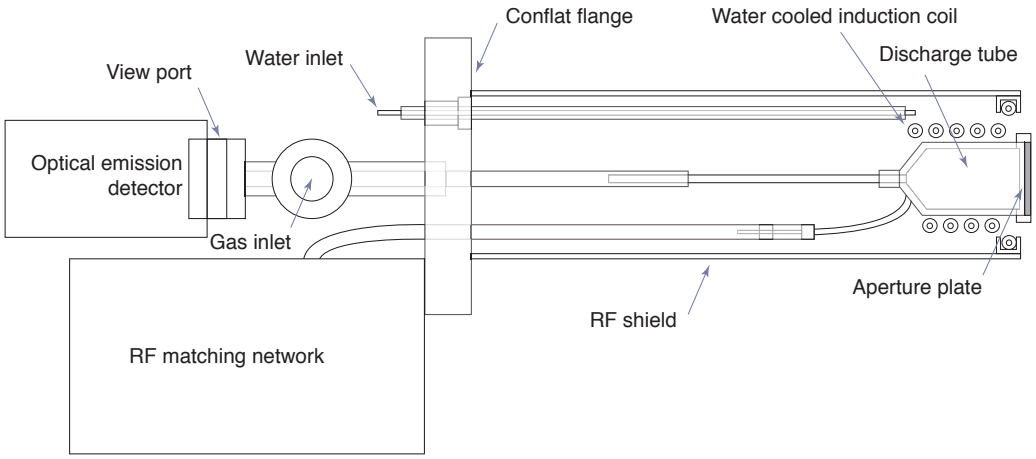
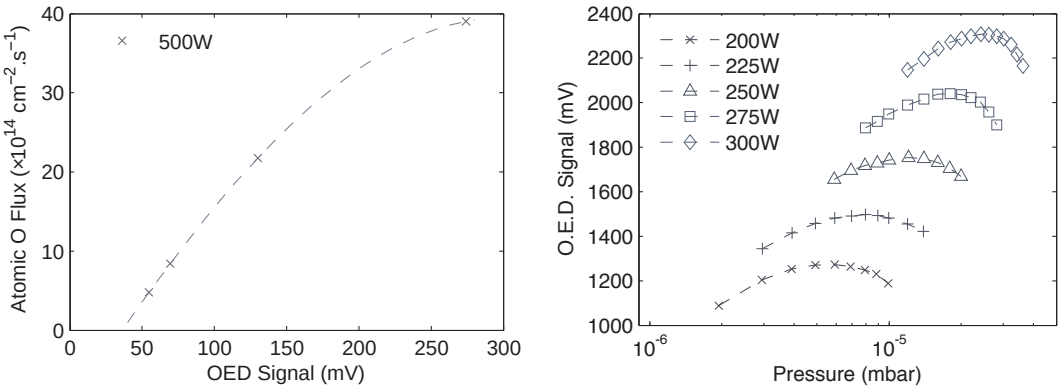


Figure 3.14: RF oxygen plasma source. Oxygen gas is fed via a needle valve into an alumina discharge tube. The operating pressure is controlled by the porosity of an alumina aperture plate. A water cooled coil is wound around the discharge tube to supply electromagnetic radiation required to excite the plasma. The RF energy is supplied from an RF source via a matching network, tuned to give maximum power to the plasma. The atomic content of the plasma is measured optically using an optical emission detector, which is in direct line of sight with the plasma. The entire source is enclosed in a shield to contain the RF radiation. Figure adapted from Ref. [114]

filament until it sublimates. The filament is surrounded by a silicon shield (not shown) and base plate to prevent elements other than silicon sublimating onto the sample. The silicon source also includes a thermocouple to monitor the filament temperature.

Oxygen plasma source: The oxygen plasma is generated with an HD-25 RF atom source from Oxford Applied Research. A schematic of this source is shown in Fig. 3.14. An alumina discharge tube and aperture plate are used to contain the plasma. A water-cooled RF coil is wound around the alumina tube, which supplies RF power up to a maximum of 600W from a Dressler Cesar 600W RF power supply. Charged particles exiting the discharge tube are deflected away from the sample using high-voltage ($500V$) deflection plates, allowing only neutrally-charged atomic oxygen to strike the sample. The intensity of the plasma is measured with an optical emission detector (OED). A needle valve is used to feed high-purity (99.9999% pure) oxygen gas into the discharge tube.

The chamber uses both an ion pump and a titanium sublimation pump to maintain a base pressure of 3–5 $\times$ $10^{-11}mbar$, making this process truly UHV-compatible. During oxide deposition, pumping is performed by a turbo molecular pump, since these are more



(a) (b)

Figure 3.15: Using the optical emission detector to measure the atomic oxygen flux. (a) At low pressures, the atomic oxygen flux is approximately proportional to the optical emission detector signal. Reproduced from Ref. [114]. (b) Our calibration of the system showed that, for a given RF power the atomic content of the plasma increases with pressure, until the flow rate reaches a critical value where the RF energy is not efficiently coupled to the discharge. The atomic oxygen content increases almost linearly with the applied RF power

efficient at the pressures used during the deposition process ($\sim 10^{-6} mbar$). The chamber also has a liquid nitrogen cooling shroud, which continuously cryopumps the chamber.

3.3.2 Generating a coincident flux of O and Si

Oxygen flux

The flux of atomic oxygen is controlled by the RF power applied to the oxygen source and the flux of oxygen gas passing into the discharge tube; from an initial characterisation, we have elected to operate at a chamber pressure of $2\text{–}9 \times 10^{-6} mbar$ with an RF power of $200\text{–}500 W$, tuned to optimise the plasma intensity as measured using the optical emission detector. The measured optical emission intensity increases monotonically with the generated flux of atomic oxygen (Fig. 3.15(a)) [114]. Figure 3.15(b) shows the relationship we have measured between the OED signal, the chamber pressure, and the applied RF power. The OED signal increases with pressure, before peaking at a power-dependent value. Beyond this peak, the coupling of RF energy to the plasma becomes inefficient and the atomic content begins to drop.

Based on Langmuir's relation between pressure and surface dose, and the knowledge that the oxygen flux from the plasma source contains ∼30% atomic oxygen [114], a lower

limit on the oxygen flux may be defined as

$$\Gamma_O[ML.s^{-1}] = 30\% \times 1.325 \times 10^6 \times P[mbar] \tag{3.9}$$

so that within our pressure range of 2–9 $\times 10^{-6} mbar$, $\Gamma_O = 0.8$–$3.6 ML.s^{-1}$, which is to say that the surface is dosed with one monolayer of atomic oxygen approximately every $1.25s$.

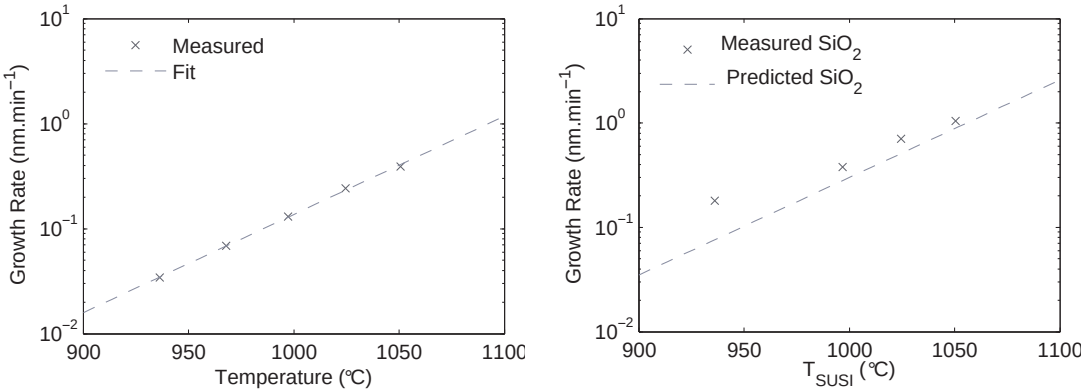
Silicon flux

To measure the flux (and therefore the growth rate) from the silicon source, we evaporated silicon at filament temperature of $935°C < T_{SUSI} < 1055°C$ for $3hrs$ onto a silicon substrate and measured the resultant layer thickness using a profilometer. Transmission electron microscopy of the deposited silicon shows epitaxial growth [31, pg. 67] (i.e. the deposited silicon is crystalline). Since the silicon that is deposited is crystalline, we can extract the flux by scaling the measured thickness by the height of one monolayer of crystalline silicon ($0.136nm$). Figure 3.16(a) shows the measured growth rate of Si from this calibration, giving a silicon flux of $\Gamma_{Si} = 0.001 ML.s^{-1}$ for $T_{SUSI} = 900°C$ and $\Gamma_{Si} = 0.1 ML.s^{-1}$ for $T_{SUSI} = 1100°C$.

We note that the temperature values presented here are likely to underestimate the actual filament temperature, since an Arrhenius fit to the measured temperature dependence of Γ_{Si} gives an energy barrier of $2.97eV$ for the sublimation energy of Si, which is less than the stated literature value of $4.1eV$ [115]. This difference is attributed to the silicon base plate of the SUSI shielding the SUSI thermocouple from silicon filament. Using this fact, we could calibrate the thermocouple reading of the sublimation source, but the temperature itself is not important for the following discussion, so we only describe the silicon sublimation rate relative to the measured filament temperature.

Generating a coincident flux of oxygen and silicon

For our process, we wish to use the silicon dioxide layer as a gate dielectric, and so we need to ensure that the SiO_2 layer is stoichiometric (free of traps), which requires that each silicon atom is matched with two oxygen atoms. Ensuring stoichiometry of the silicon dioxide requires the relative flux of silicon and oxygen to be sufficiently oxygen-rich for the deposited silicon to oxidise. Figure 3.9(b) indicates that, as a conservative estimate, $100ML$ of oxygen will be more than sufficient to fully oxidise one monolayer of silicon, which is achievable using the range of Γ_{Si} and Γ_O we have calculated.



(a) (b)

Figure 3.16: Calibrating the flux of the silicon and silicon dioxide. (a) The growth rate of silicon deposited on the sample increases exponentially with the temperature of the silicon sublimation source. (b) The growth rate of SiO_2 also increases exponentially with the silicon filament temperature. However, the growth rate is significantly higher than expected from the measured silicon flux.

To calibrate the process, we have grown oxides on the order of $35nm$ thick over a $3h$ period, which requires an oxide growth rate of $0.2nm.min^{-1}$. For a stoichiometric oxide, 45% of this thickness is comprised of silicon [43, pg. 647]. This corresponds to a silicon sublimation rate of $0.09nm.min^{-1}$ ($0.65ML.min^{-1}$), which we can achieve using $T_{SUSI} = 975°C$. According to the stated $100ML$ of oxygen exposure per monolayer of silicon, this would require an oxygen pressure of

$$P = \frac{100 \times 0.65ML.min^{-1}}{30\% \times 1.325 \times 10^6[mbar^{-1}.s^{-1}] \times 60[s.min^{-1}]} \simeq 2 \times 10^{-6}mbar \tag{3.10}$$

Figure 3.16(b) shows the oxide growth rate of samples grown without substrate heating under a pressure of $2 \times 10^{-6}mbar$, as a function of the SUSI temperature. The dashed line in this figure is the predicted growth rate of the oxide based on the silicon growth rate shown in Fig. 3.16(a), where the predicted oxide thickness is 2.2 times the measured silicon thickness for a stoichiometric oxide. However, the measured growth rate (crosses) is higher than the expected growth rate (dashed trace) — by as much as $\sim$2 at $T_{SUSI} = 935°C$ — indicating that the material density is either lower than that of a thermally grown oxide, or that the sublimation rate of the silicon source changes in the presence of the oxygen plasma. In the next section we explore this phenomenon in more detail, and describe the processes that contribute to it.

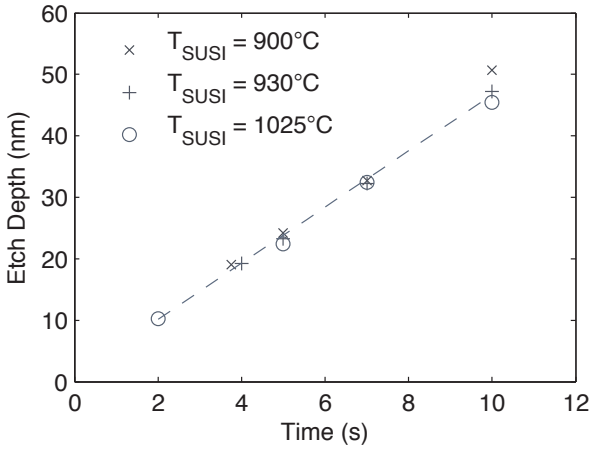


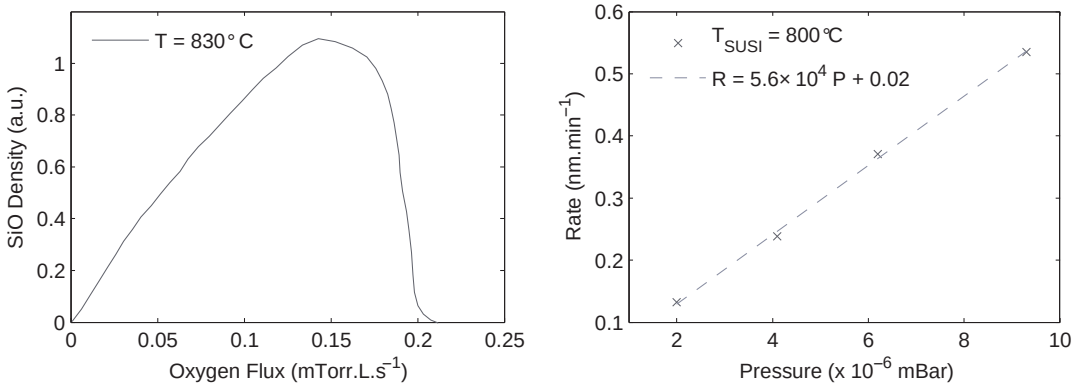
Figure 3.17: Assessing the density of the low-temperature oxide using hydrofluoric acid. The etch rate of three samples, each grown at four different currents has been plotted. All samples have an etch rate approximately four times higher than that of a thermal oxide, indicating that they are less dense than thermal oxides. All three samples have approximately the same etch rate, indicating that the low oxide density is not the cause of the higher than expected oxide growth rate.

3.3.3 Controlling the oxide stoichiometry using the O and Si flux

Oxide density

From the oxide growth rate calibration in Fig. 3.16(b), we see the oxide growth rate is higher than expected, particularly at low temperatures. This might be the result of the oxide grown at these temperatures not being stoichiometric. To establish whether this is indeed the case, we exploit the fact that the density of an oxide affects its chemical properties; in particular, Besser *et al.* have shown that the etch rate of silicon dioxide using hydrofluoric acid is exponentially sensitive to the oxide density [116]. According to their results, an oxide 30% less dense than a thermal oxide has an etch rate more than 25 times higher.

Figure 3.17 shows the etch rate of three different oxide samples grown with silicon filament temperature ranging from $930°C$ to $1050°C$. The average etch rate is $4.6nm.min^{-1}$, which is approximately four times higher than that of a thermal oxide, indicating that the oxide is indeed less dense than thermally-grown samples but only marginally so. The density change indicated by Fig. 3.16(b) predicts samples grown at $930°C$ to be considerably less dense than those grown at $1050°C$. However this is not evident from the etch rate results, since all the three samples in Fig. 3.17 have approximately the same etch rate. This indicates that the low oxide density is not the only source of the deviation in the oxide growth rate.



(a) (b)

Figure 3.18: Active oxidation of silicon in the presence of an oxygen flux. (a) If a silicon sample is held above the silicon monoxide desorption temperature, the presence of a low-pressure oxygen flux actively oxidises the sample. This process produces silicon monoxide and etches the silicon surface. Beyond a critical, temperature-dependent flux the sample begins to passively oxidise. At this flux the rate of silicon monoxide desorption drops. Reconstructed from Ref. [117]. (b) The growth rate shows a strong linear dependence on the pressure the oxide chamber. This is consistent with the oxygen ambient in the chamber actively oxidising the silicon filament, where the incident oxygen is the rate limiting reactant. The offset in the measured pressure-dependent rate is consistent with the expected sublimation rate of silicon from the filament at this current in absence of the monoxide desorption mechanism.

Interaction between O and Si sources

During the low-temperature oxidation, the oxide chamber is filled with oxygen, which was not present when calibrating the silicon source. The presence of the oxygen ambient oxidises the SUSI filament and when the silicon filament is heated it forces any adsorbed oxygen to desorbs faster than it is replaced. The desorption favours sublimation in the form of silicon monoxide, according to the chemical reaction

$$SiO_{2(s)} + Si_{(s)} \rightarrow 2SiO_{(g)} \tag{3.11}$$

which results in etching of the silicon filament. This process has been studied by Walkup *et al.* in which the silicon monoxide desorption rate was found to be approximately proportional to the oxygen flux incident upon the silicon surface [117]. The results of Walkup's study are shown in Fig. 3.18(a); the SiO desorption in Walkup's study increased almost linearly with the oxygen flux, up to a critical point of $0.15 mTorr.L.s^{-1}$. At this point, the silicon begins to passively oxidise, where oxygen adsorption dominates over the desorption process and a protective oxide forms that prevents further SiO desorption.

Figure 3.18(b) shows the pressure dependence of our oxide growth rate using a SUSI filament temperature of $\sim 800°C$. There is a strong linear correlation between the oxide growth rate and the oxygen pressure. The offset in this trend of $0.02 nm.min^{-1}$ is consistent with the growth rate expected solely from sublimated silicon, in the absence of the SiO desorption mechanism.

From this data we conclude that, when the oxygen plasma is running, the total silicon sublimation rate consists of temperature-dependent Si sublimation and pressure-dependent SiO sublimation in the form

$$R_{Si} = 5.6 \times 10^4 P + 8.02 \times 10^{10} \times e^{-\frac{2.97e}{k_B T_{SUSI}}} \tag{3.12}$$

for the growth rate R_{Si} in $nm.min^{-1}$, oxygen pressure P in $mbar$, and SUSI temperature T_{SUSI} in K. Adding these two mechanisms produces a good fit to the expected oxide growth rate, as shown in Fig. 3.19, which is much better than that of Fig. 3.16(b). The theoretical trend matches the measured data extremely well, indicating that the concurrent sublimation of SiO during the silicon dioxide growth is likely to be the cause of the growth rate discrepancy in Fig. 3.16(b).

The sublimation of SiO from the silicon source places an upper limit on the ratio between the oxygen and silicon flux of

$$\begin{aligned} \frac{R_{SiO_2}}{R_{Si}} &= \frac{0.3 \times 1.325 \times 10^6 ML.s^{-1}.mbar^{-1}}{5.6 \times 10^4 nm.min^{-1}.mbar^{-1} / 0.136 nm.ML^{-1} \times 1/60 min.s^{-1}} \\ &= \frac{3.9 \times 10^5 ML.s^{-1}.mbar^{-1}}{6.8 \times 10^3 ML.s^{-1}.mbar^{-1}} \\ &= 57.9 \end{aligned} \tag{3.13}$$

From the study of atomic oxygen surface dose versus oxide growth shown in Fig. 3.9(b), exposing each monolayer of silicon to $\sim$60 monolayers of oxygen puts us at the cusp of the transition to the diffusion-limited regime of oxide growth (beyond a coverage of $5ML$). As such, we expect the deposited silicon to be fully oxidised during the co-deposition process provided that the silicon sublimation rate is dominated by the SiO sublimation mechanism. For this, we must keep the silicon filament temperature to $T_{SUSI} \leq 930°C$. The only remaining means of improving the ratio beyond this limit to improve the oxide stoichiometry is to periodically interrupt the silicon flux using a mechanical shutter. Verifying that the present flux of oxygen is sufficient to fully oxidise the deposited silicon requires chemical and structural analyses, which we conduct in the following section.

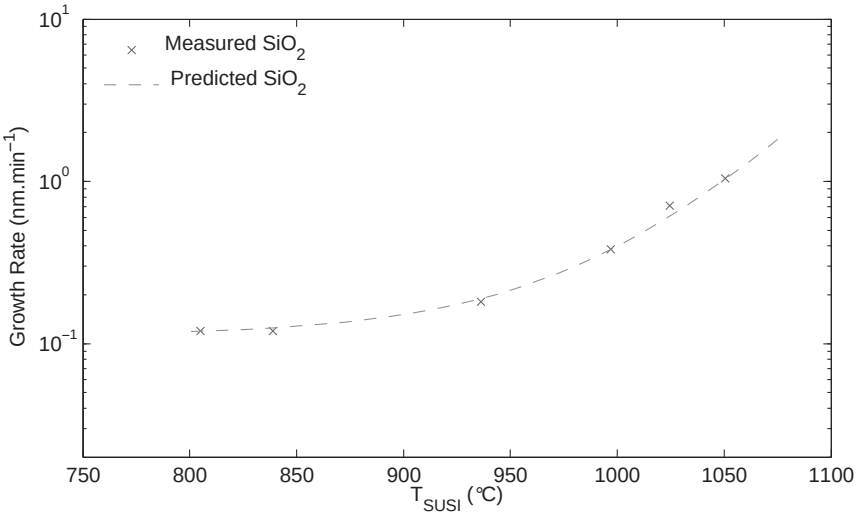


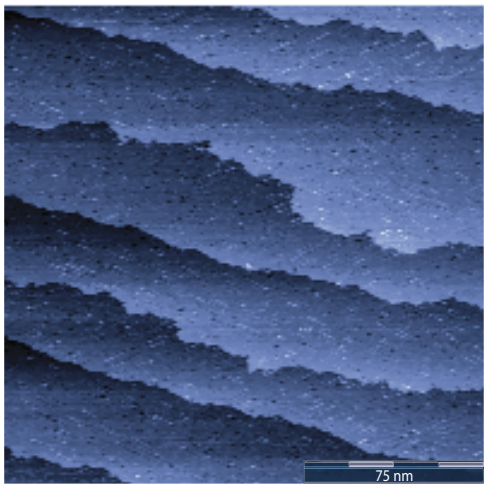
Figure 3.19: Corrected SiO_2 growth rate due to sublimation of SiO from the silicon source. The growth rate of the oxide was measured at low silicon filament currents, where the sublimation rate is dominated by the SiO desorption mechanism. The growth rate clearly saturates. Adding the expected growth rate from the SiO and Si sublimation mechanisms generates a predicted growth rate curve that matches the experimental values perfectly.

3.4 Chemical and structural analyses of low-temperature UHV oxide

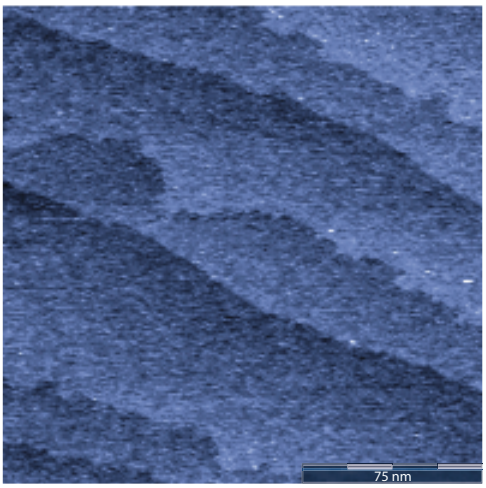
Silicon dioxide has been used almost exclusively as the gate insulator in CMOS processes for several decades. As a consequence, the performance of silicon dioxide as a dielectric and the interface it forms with silicon have been studied extensively. These studies have generated valuable insight into the chemical and structural properties of high-quality gate oxides. Here we apply a variety of techniques to analyse the chemical and structural properties of the low-temperature, UHV-grown silicon dioxide we have developed.

3.4.1 STM/STS of a silicon surface oxidised with atomic oxygen

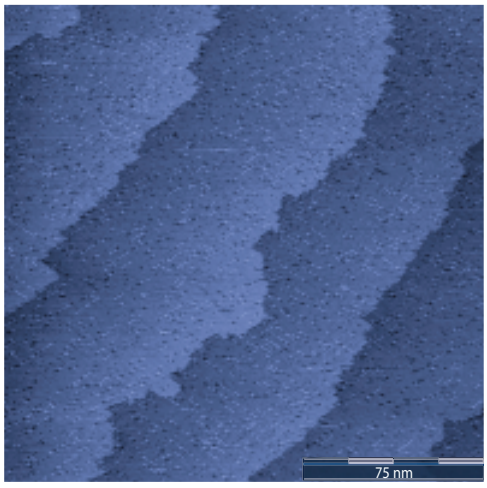
The oxide deposition system is attached to the scanning tunnelling microscope, used to fabricate devices, through a network of ultra-high vacuum chambers. This allows the silicon sample to be transferred between the two chambers without exposing it to atmospheric contaminants. With this setup it is possible to study the silicon surface using the STM before it is oxidised, and if the deposited oxide is sufficiently thin, to image the resultant surface after the sample is oxidised.



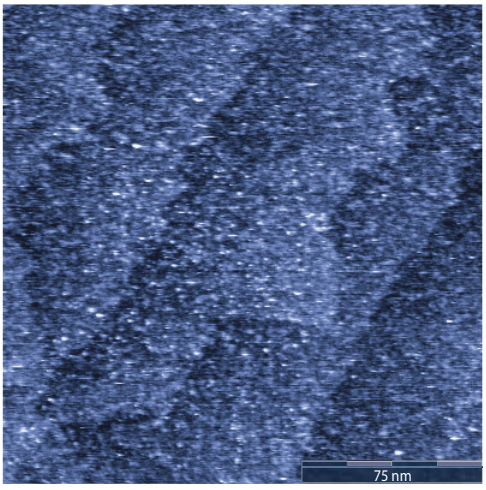
(a) Filled state STM image of silicon surface before exposure to atomic oxygen ($V = -2.3V$, $I = 0.75nA$)



(b) Filled state STM of silicon surface after 5min exposure to atomic oxygen at $2.0 \times 10^{-6} mbar$ with $RF = 200W$ and no substrate heating ($V = -1.8V$, $I = 0.18nA$)



(c) Filled state STM image of silicon surface after re-flashing the sample ($V = -2.3V$, $I = 0.75nA$)



(d) Filled state STM of silicon surface after 60min exposure to atomic oxygen at $2.0 \times 10^{-6} mbar$ with $RF = 200W$ and no substrate heating ($V = -1.8V$, $I = 0.18nA$)

Figure 3.20: STM images of the passivation of silicon Si(100) 2×1 with atomic oxygen. (a) The starting silicon surface shows atomically-flat terraces typical of the flash-anneal surface preparation technique. (b) After exposing the surface to atomic oxygen for $5min$, the surface is visibly roughened and step edges become blurred. (c) The re-flashed surface looks like a standard silicon surface, with the addition of a small increase in the number of dimer vacancies (black spots) that typically occurs when a surface is re-flashed. (d) After exposing the surface to atomic oxygen for $60min$, the surface looks rougher still. The atomic terrace structure is preserved, indicating that the oxide thickness is still less than several monolayers thick.

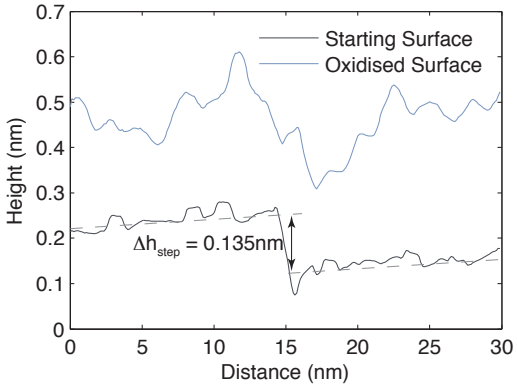


Figure 3.21: STM line profiles of oxidised silicon surface after exposure to atomic oxygen. The lower trace shows a line profile over a step-edge on the clean silicon surface of Fig. 3.20(a). The RMS roughness of this starting surface is $51pm$, averaged over the whole image. The upper trace shows a line profile over a step-edge on the oxidised surface of Fig. 3.20(b). The RMS of this oxidised surface is $100pm$, averaged over the whole image. The step edge of the oxidised surface is less distinct, both as a result of roughness and because the oxide masks the order of the underlying substrate.

Several authors have studied the growth kinetics and electrical properties of silicon dioxide using a scanning tunnelling microscope [118–122]; measuring an oxidised surface with an STM requires the oxide to be thin so that an appreciable tunnel current will flow. The tunnel current measured by an STM is a function of the density of states in the tip and sample, the barrier height for the tunnelling process, and the tip-sample bias [123].

In normal (topographic) imaging with an STM, the tunnel current is regulated by a control loop that adjusts the tip-sample spacing to maintain a constant tunnel current as the tip rasters across the surface [124]. The deviation of the tip during constant current imaging is therefore a convolution of the conductivity and topography of the sample surface.

Figure 3.20(a) shows an image of a starting silicon surface using constant-current imaging. This surface was prepared by chemically cleaning the sample and performing an *in-situ* flash-anneal to $1100°C$, as described in Sec. 4.3.2. There is a regular set of diagonal lines passing through the image, demarcating edges of atomically-flat terraces of silicon atoms. This is the result of a slight mis-cut ($\leq 0.2°$) of the silicon wafer from the intended [001] crystal orientation.

Figure 3.20(b) shows the effect of exposing the surface in Fig. 3.20(a) to the atomic oxygen plasma for $5min$ ($\sim 600L$). The terraced structure of the silicon surface persists after oxidation, indicating that an oxide forms through a wetting process, rather than nucleating from defects. Line profiles over the step-edges are shown in Fig. 3.21. The step edges of the starting surface are roughened and blurred after the oxide forms. The

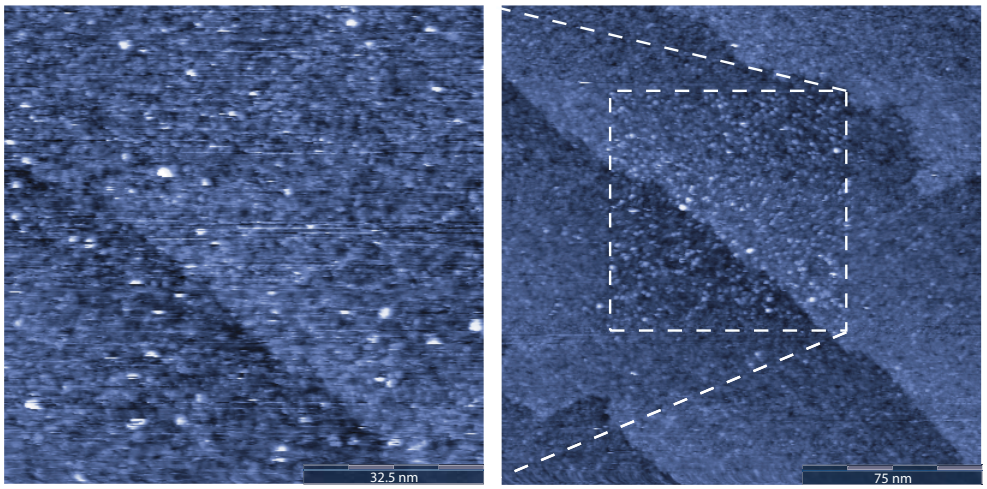


Figure 3.22: Damage caused to the oxide by imaging with an STM. The left image shows an area on the surface that was scanned several times with the STM tip. The right image shows the effect this repeated scanning has on the the oxide surface. The scanned region is visibly brighter and multiple bright spots occur, indicative of weak points in the oxide after stress-induced break down.

conformance of the oxidised surface to the initial terraced structure indicates that the oxide is not thicker than 1–2nm, given that there is expected to be no crystalline oxide species [125]. The surface is visibly rougher after oxidation, with an RMS roughness of 100pm, compared with 51pm of the starting surface (averaged over the images shown in Fig. 3.20). This is consistent with previous studies of thin oxides with an STM [126].

After oxidising the sample for five minutes, the oxide was cleaned using a flash-anneal before performing the next exposure experiment. Figure 3.20(c) shows the resultant surface after the flash anneal. It is comparable to that of Fig. 3.20(a). This cleaned silicon surface was then exposed to the atomic oxygen flux for 60min, giving a surface dose of approximately 7000L of atomic oxygen. The resultant surface is shown in Fig. 3.20(d). Once again, the surface is visibly roughened by the oxidation, and the terraced structure of the surface remains visible. This image shows a higher density of bright protrusions than that of Fig. 3.20(b), which is attributed to the increase in contrast between the insulating and conducting regions on the surface as the oxide becomes thicker.

Imaging oxidised surfaces may also lead to stress-induced leakage of the oxide [126, 127]. This effect is shown in Fig. 3.22, in which a 100nm frame was repeatedly scanned with the STM (3 times) to stress the oxide (shown left). Zooming out to a 200nm scan frame (shown right) highlights the damage caused by repeated scanning. The area stressed by repeated scanning is visibly brighter and rougher, consistent with local stress-induced leakage caused by the STM tip. As a consequence of this stress-induced leakage, it is

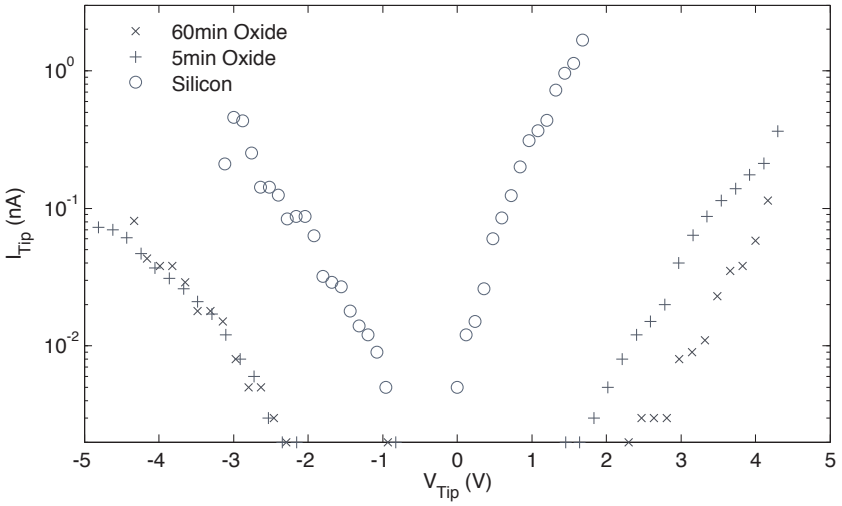


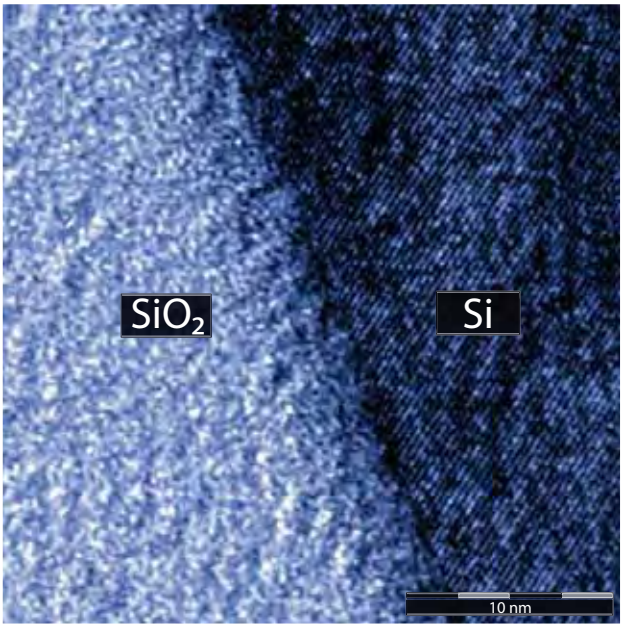
Figure 3.23: Scanning tunnelling spectroscopy of the low temperature oxide. The conductivity of the bare silicon surface is dominated by the π and π^* orbitals that are generated by the 2×1 surface reconstruction. Tunnelling through the oxide occurs into the silicon conductance and valence band as the π and π^* surface state are passivated by the oxide. The magnitude of the tunnelling current passing through the oxide is reduced as a result of the increase in the tunnel barrier width.

difficult to quantitatively compare the topographical roughness of oxidised surfaces using STM.

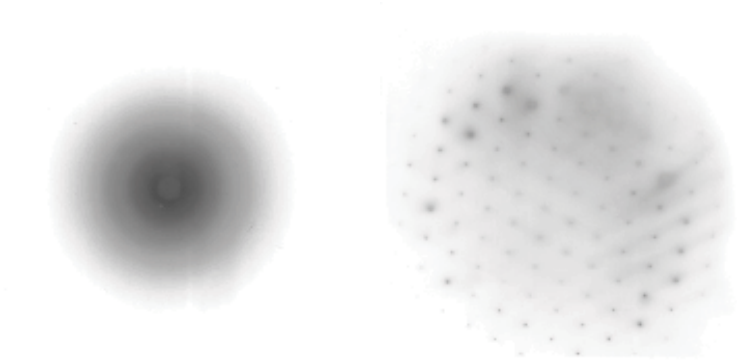
To distinguish between the surface conductivity and topography, it is possible to probe the electrical characteristics of the surface by sweeping the tip-sample voltage at a fixed tip height. Performing this scanning tunnelling spectroscopy (STS) across the surface gives an indication of the overlap between the energy-dependent local density of states in the tip and the sample. Figure 3.23 shows the average of STS spectra taken over a $200nm$ area on the bare silicon surface, and surfaces oxidised for $5min$ and $60min$.

Tunnelling to the bare silicon surface occurs predominantly into the π and π^* surface states formed by the (2×1) surface reconstruction [128]. The energy gap between these states is considerably narrower than the band gap of the silicon bulk ($0.5eV$ vs. $1.1eV$), and they are centred closer to the valence band of the bulk. When the surface is oxidised, the π and π^* surface states are passivated. As a result, STS of the oxide probes the bulk conductance and valence band states of the substrate [126]. The additional barrier to tunnelling formed by the presence of the oxide decreases the magnitude of the tunnel current.

The resulting STS data in Fig. 3.23 therefore indicates that the surface is passivated by the atomic oxygen flux, and that an insulating layer of oxide has formed. Thus we conclude that the atomic oxygen flux is capable of oxidising the silicon surface, and that



(a)



(b) (c)

Figure 3.24: Transmission electron micrograph of the interface between the deposited low-temperature oxide and the silicon substrate. (a) The silicon substrate (right) shows an ordered crystal structure. The silicon dioxide layer (left) shows no ordering, as a result of the amorphous nature of SiO_2. The interface between the silicon and oxide is abrupt and flat, with a mean interface roughness less than $1nm$. (b) Electron diffraction pattern formed by electrons passing through the oxide (left of (a)), which shows no ordering of the diffracted electrons — i.e. the oxide is amorphous. (c) Electron diffraction pattern formed by electrons passing through the silicons substrate (right of (a)), which shows strong ordering of the diffracted electrons, indicating that the substrate is still crystalline.

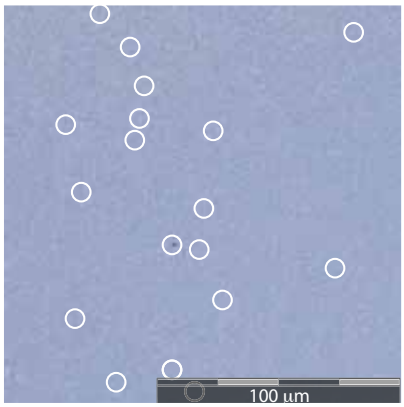


Figure 3.25: Optical microscopy of macroscopic defects in the oxide. Optical image showing macroscopic defects (highlighted with circles). With the density of macroscopic defects shown in this frame, it is likely that any gate electrode larger than $100\mu m$ will overlap with a macroscopic defect in the oxide.

this process essentially saturates after $5min$ exposure of the sample to the oxygen flux. Based on these results, all oxide samples have been fabricated using an exposure to the oxygen flux for $20min$ to produce the initial surface passivation shown in Fig. 3.10(a).

3.4.2 TEM of the low-temperature UHV oxide

A transmission electron microscope passes a focussed beam of electrons through a thin sample. Using a focused ion beam, it is possible to mill a vertical cross-section of a silicon/silicon-dioxide sample that is less than $100nm$ wide. This cross-section can be imaged under a transmission electron microscope. Electrons scatter off atoms in the sample as they pass through, forming an image that shows the location and ordering of atoms.

Figure 3.24 shows a TEM image of a $\sim 80nm$ sliver milled from a UHV-grown low-temperature oxide. This cross section shows the interface between the silicon substrate and the low-temperature oxide. The silicon substrate (right of image) shows an ordered, regular crystal structure. The oxide (left of image) shows a disordered, amorphous, homogeneous structure. The interface between the two materials has a roughness of less than $1nm$.

3.4.3 Optical analysis of macroscopic defects in the low-temperature UHV oxide

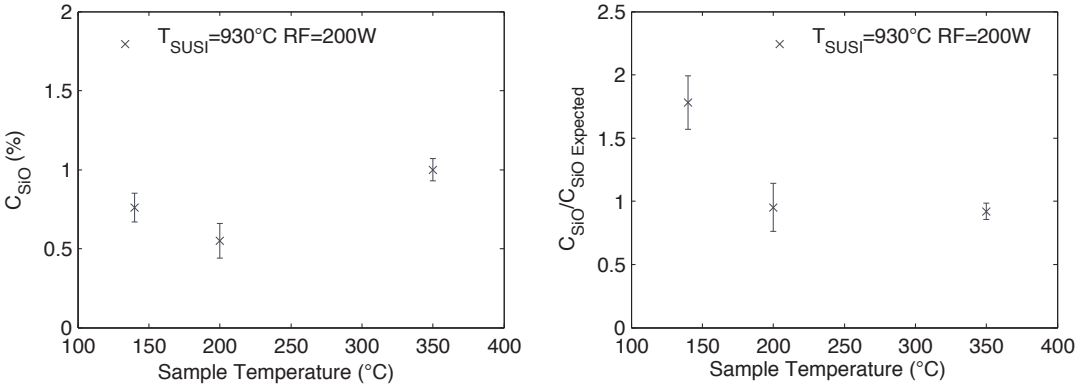
After growing many test oxide samples, we noticed the samples had particles on the surface after they were removed from the UHV system. These particles could not be removed using

ultrasonic agitation, or using a full chemical clean (App. A), and appeared to be embedded in the oxide itself. An image of the particles present on the surface is shown in Fig. 3.25. The density of defects ($\sim 1.25 \times 10^{-12}.cm^{-2}$) did not appear to change across the many samples fabricated, regardless of the growth conditions. When the oxygen source was not used and silicon was grown on the sample epitaxially, the particles were still present. The formation of particles within MBE-grown silicon is known to arise from silicon films forming on the chamber wall and flaking off into the path of the silicon flux, or from silicon particulates 'spitting' from the silicon source itself [129]. Flaking is reduced by the use of liquid nitrogen cooling shrouds, and the effects of spitting can be minimised by placing the silicon source below the sample so that the heavy silicon particulates do not reach it [129]. Both techniques are employed in the design of our UHV oxide chamber, however it may be possible that silicon particulates are still arriving at the sample. Alternatively, the particles may be forming during the growth itself, however this seems unlikely given that they did not change in size or density across the range of growth parameters used to make the samples we have studied. Work continues on tracing and eliminating the source of these macroscopic defects in the oxide; however, they were sufficiently sparsely distributed across the sample surface that some devices would successfully avoid overlapping with a defect. As such, in parallel we began studying the use of the oxide as a gate dielectric. To be a successful gate dielectric, the oxide must be stoichiometric. Several techniques allow direct measurement of the ratio between silicon and oxygen in the formed oxide. To measure the composition we have used ellipsometry and XPS.

3.4.4 Ellipsometry of the low-temperature UHV oxide

When a linearly polarised beam of light is directed at the surface of a dielectric, elliptically polarised light may be reflected. The extent of the elliptical polarisation is dependent upon the material type and its thickness [130]. The degree of elliptical polarisation can be measured with an ellipsometer. This instrument directs two orthogonally polarised beams of light at the sample. The relative phase shift and complex amplitude of the reflected beam may be used to determine the sample refractive index and thickness.

The absorbance and refractive index of a sample are material dependent. As such, an ellipsometer may be used to determine the composition of an oxide [131]. For this study, the sample was modelled as a homogeneous mixture of silicon monoxide in a silicon dioxide matrix. The concentration of silicon monoxide was used as a fitting parameter for the measured ellipsometry data.

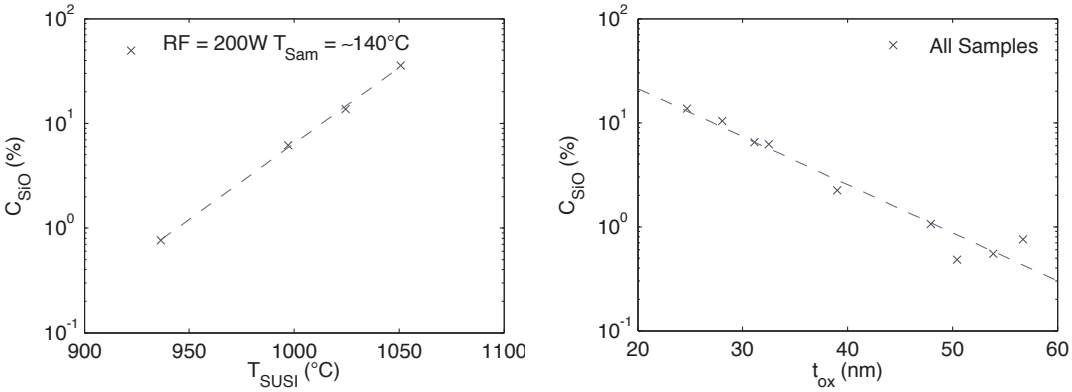


(a) (b)

Figure 3.26: Measuring the composition of the oxide as a function of the sample temperature using ellipsometry. (a) These samples were grown with a SUSI temperature of $930°C$, a chamber pressure of $2 \times 10^{-6} mbar$, and an RF power of 200W. (b) Here the measured concentration of SiO relative to that predicted by the sample thickness is plotted against the sample temperature. There is a monotonically decreasing trend, but the errors associated with this method prevent drawing any definitive conclusion about the effect of substrate temperature.

Figure 3.26(a) shows the measured concentration of SiO from the ellipsometry model as a function of sample temperature during growth. The three samples shown in this figure were grown with an RF power of $200W$, a SUSI temperature of $930°C$ and a chamber pressure of $2 \times 10^{-6} mbar$. The lowest temperature sample was grown without actively heating the substrate, where radiative heating from the silicon and oxygen sources generated a sample temperature of 130–$140°C$. The error bars displayed for each data point are the specified error from the model fitting process. From this data there is no clear trend in the concentration of silicon monoxide as a function of the silicon dioxide growth temperature, which is unexpected since higher temperatures should enhance the diffusion of atomic oxygen through the formed oxide, increasing the oxygen content of the oxide.

Figure 3.27(a) shows the effect of the SUSI temperature on the measured concentration of SiO. For these samples the RF power was held at $200W$, the chamber pressure was kept at $2 \times 10^{-6} mbar$, and the samples were grown without substrate heating. There is a clear exponential trend in the concentration of measured SiO with the SUSI temperature. This is what we expect intuitively, since a higher flux of silicon would reduce the ratio of atomic oxygen to silicon flux during the oxide growth. However, the SUSI temperature during growth is coupled to the final oxide thickness through changes in the silicon sublimation rate. To ensure that the relationship shown in this figure is dominated by the SUSI temperature, and not the final oxide thickness, we plot the concentration of



(a) (b)

Figure 3.27: Measuring the composition of the oxide as a function of the SUSI temperature and thickness using ellipsometry. (a) These samples were grown with a chamber pressure of $2 \times 10^{-6} mbar$, while the sample was not actively heated. The sample temperature during growth was $130 - 140°C$. (b) This figures shows samples grown with substrate temperatures in the range $130 - 350°C$, RF powers in the range $200 - 500W$, SUSI temperatures in the range $930 - 1050°C$. The implied concentration of silicon monoxide detected using ellipsometry appears to be more sensitive to the thickness of the oxide than any other parameter varied in this study.

SiO in all samples as a function of the oxide thickness in Fig. 3.27(b). There is a clear exponential correlation between the oxide thickness and the measured concentration of silicon monoxide. The only deviation from this trend occurs at concentrations below 1%, which is the expected detection limit of the apparatus. This indicates that the majority of the results presented here are dominated by the thickness of the oxide. One possible explanation for this is that diffusion of oxygen from the incident flux of atomic oxygen continues throughout the oxidation process, allowing the stoichiometry of the as-deposited oxide to improve as the growth proceeds.

If we compensate for the effects of the oxide thickness, we can isolate the effect of the other process parameters. Figure 3.26(b) shows the relative concentration of SiO from the temperature-dependence study of Fig. 3.26(a) when scaled by the thickness trend shown in Fig. 3.27(b). The measured concentration of SiO now shows a monotonically decreasing trend with temperature, indicating that increasing the sample temperature during the growth does in fact improve the oxide stoichiometry. This is consistent with our model of atomic oxygen diffusing through the as-deposited oxide throughout the oxide growth. We therefore conclude that increasing both the growth temperature and time will improve the stoichiometry of the oxide by allowing the atomic oxygen to diffuse down into the formed oxide layer. To investigate this further, the composition of the oxide can also be measured with X-ray photoelectron spectroscopy.

3.4.5 XPS of the low-temperature UHV oxide

X-ray photoelectron spectroscopy measures the energy spectrum of emitted photoelectrons generated when a sample is bombarded with mono-energetic X-ray radiation [132]. The kinetic energy of the emitted photoelectron (KE) is a function of the starting energy of the X-ray ($h\nu$), the binding energy of the state from which the photoelectron is emitted (BE), the surface potential ($q\phi$), and the spectrometer work function (ψ_s):

$$KE = h\nu - BE - \psi_s - q\phi_s \tag{3.14}$$

The binding energy of an electron is determined by the chemical species within the sample and their bonding arrangement. In the case of silicon dioxide, these bonding arrangements include silicon bound to four oxygen atoms, four silicon atoms, or any permutation in between [133, 134]. The XPS spectrum therefore gives an indication of the ratio of silicon atoms in each oxidation state.

Figure 3.28 illustrates the XPS spectrum of a silicon dioxide layer as it forms, showing the sub-oxide species present close to the interface where the silicon is bound to less than four oxygen atoms. The labels Si^{n+} refer to XPS peaks associated with a silicon atom bound to n oxygen atoms. The incident X-ray penetrates a finite depth into the sample. As a consequence, the XPS spectra of thin oxides typically show a Si peak associated with the silicon substrate. It has been shown that this peak is dominated by the substrate rather than the oxide using angle-resolved XPS spectra [135, pg. 93], where the silicon peak was observed to subside when the angle of incidence of the X-ray was shallow, because the X-ray would only probe the surface species.

XPS spectra also typically show a depth-dependence of the oxide composition. Close to the silicon substrate, the oxide contains a higher percentage of sub-oxides. This is attributed to the statistical process by which oxygen diffuses into the silicon substrate. In the study by Watanabe *et al.* [134] shown in Fig. 3.28, the oxide grows from $0.6nm$ (upper frame) to $1.7nm$ (lower frame) and the ratio between the stoichiometric oxide peak Si^{4+} and sub-oxide peaks $Si^{n+}, n \leq 3$ improves. It is also possible for the composition to be non-stoichiometric in the oxide bulk. This can occur in thermal oxides because the oxygen must diffuse through the outer-most layer of oxide to reach the silicon substrate below. This occurrence of sub-oxide species near the Si–SiO_2 interface is consistent with our ellipsometry study, where thinner samples contained a higher proportion of sub-oxide species (since a higher proportion of the oxide was nearer to the interface).

Figure 3.29 shows the XPS spectra of two nominally $5nm$ low-temperature oxides grown in the UHV oxide chamber, where one sample was grown without substrate heating

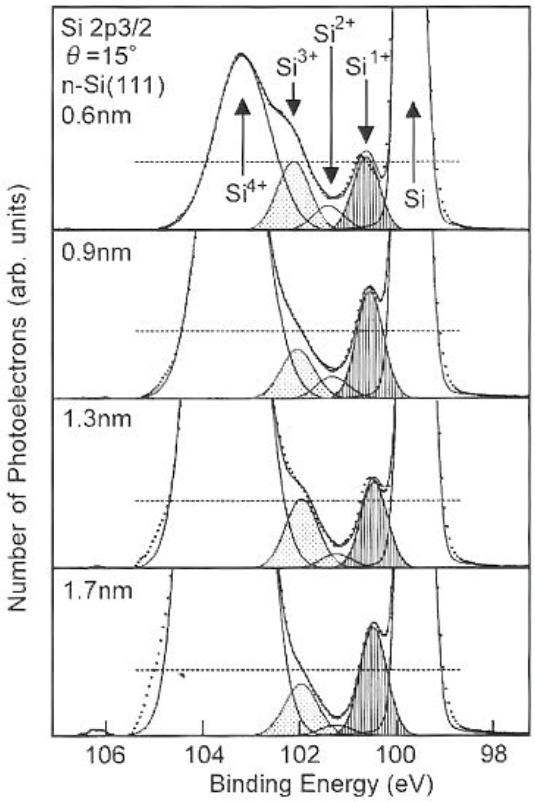


Figure 3.28: XPS spectra of oxides containing un-oxidised silicon. The XPS spectrum of an oxide around the Si $2p$ peak is composed of five distinct peaks. Here they are labelled Si^{n+} where n corresponds to the number of oxygen atoms the silicon atom is bound to. The ratio between the amount of fully oxidised silicon (Si^{4+}) and the sub-oxide species ($Si^{n+}, n \leq 3$) improves as the oxide grows thicker. From Ref. [134].

and the other was grown at $350°C$. For comparison, we have also shown the results for a high-quality nominally $5nm$ thermal oxide grown at $800°C$ followed by a $1000°C$ RTA. The spectra shown were recorded after each sample was sputtered with argon for $10s$ to remove surface contaminants.

The results show the presence of an Si^{4+} peak centred around $104eV$ for all samples, consistent with a stoichiometric oxide. In addition, there is a doublet peak at $\sim 99.2eV$ and $\sim 99.8eV$, corresponding to the Si^0 bonding state that arises from the silicon substrate. This substrate peak is visible in these samples because XPS probes $\sim 15nm$ into the sample, and the oxides shown here were only $5nm$ thick. The relative Si^0 peak height of each sample differs because of the minute differences in thickness of the three samples after they were each cleaned using argon sputtering. The splitting of the Si^0 peak is attributed to shifting of the $2p_{1/2}$ and $2p_{3/2}$ energies in the valence states of the silicon substrate atoms once ionised (the splitting of the Si^0 peak is not visible in Fig. 3.28 because the two

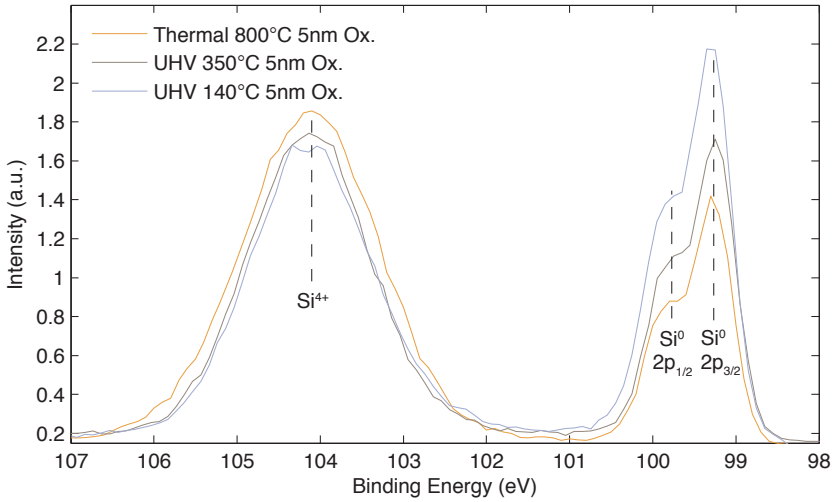
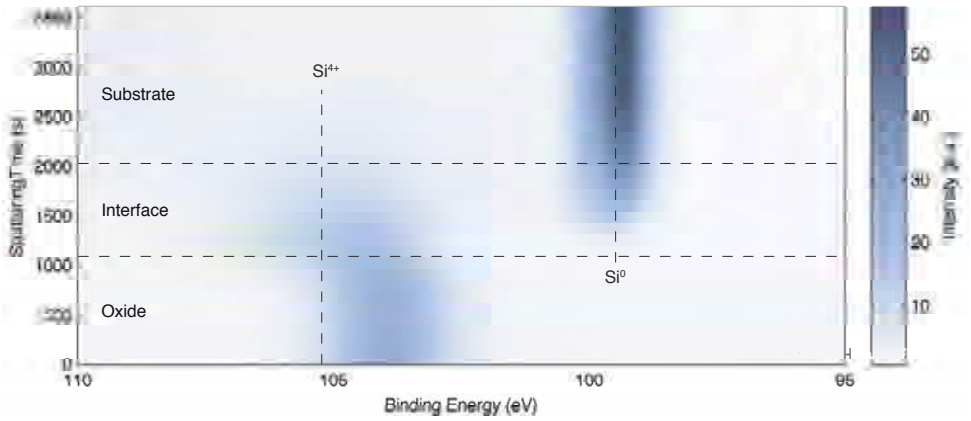


Figure 3.29: XPS spectra of low-temperature UHV oxides compared to a high quality thermal oxide. XPS spectra are shown for nominally $5nm$ UHV oxides grown with a pressure of $3.5 - 5.5 \times 10^{-6} mbar$, a SUSI temperature of $703 - 710°C$, and with substrate temperatures of $140°C$ and $350°C$. A high-quality thermal oxide grown at $800°C$ is shown as a reference. The three spectra have the same qualitative shape, though the Si^0 peak heights differ. This is attributed to the respective sample thicknesses after argon sputtering. There are no discernible sub-oxide peaks in the spectra.

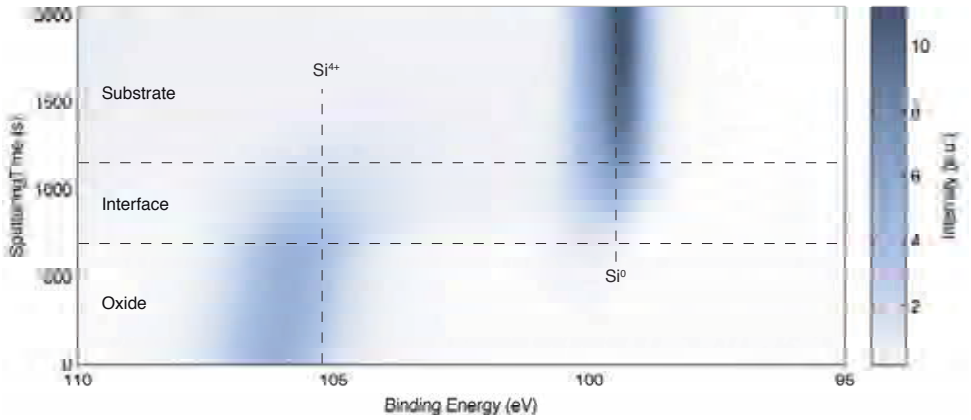
peaks have been combined in post-analysis, as is common practice). The expected energy splitting of the $2p_{1/2}$ and $2p_{3/2}$ peaks is $0.61eV$ with a relative intensity of $2:1$ [136], which is consistent with the measured spectra of our samples in Fig. 3.29.

There are no resolvable sub-oxide peaks for any of the samples in Fig. 3.29, which is typical of gate oxides in which the magnitude of sub-oxide peaks falls below the detection limit of the instrument [136], corresponding to $\sim$0.2 in the arbitrary intensity scale for the measurement apparatus used for Fig. 3.29. That is, the sub-oxide content of our oxide is below the detection limit of the apparatus. We note however that XPS is most sensitive to the sample surface, so that photoelectrons emitted by sub-oxides nearer to the interface are attenuated by the intervening oxide bulk [137]. Another way of assessing charges within the oxide however has been suggested by Iwata *et al.* [136]. Iwata's method takes advantage of the fact that charges present in the oxide alter the surface potential $q\phi_s$, and thus according to Eq. 3.14, the measured photoelectron binding energy. Irradiating an oxide with X-rays is known to produce positive charges within the oxide [135]. Sputtering a sample with argon ions also leads to a build up of positive charge. Through this mechanism, irradiating or sputtering a thick oxide sample produces a large shift in the measured binding energy.

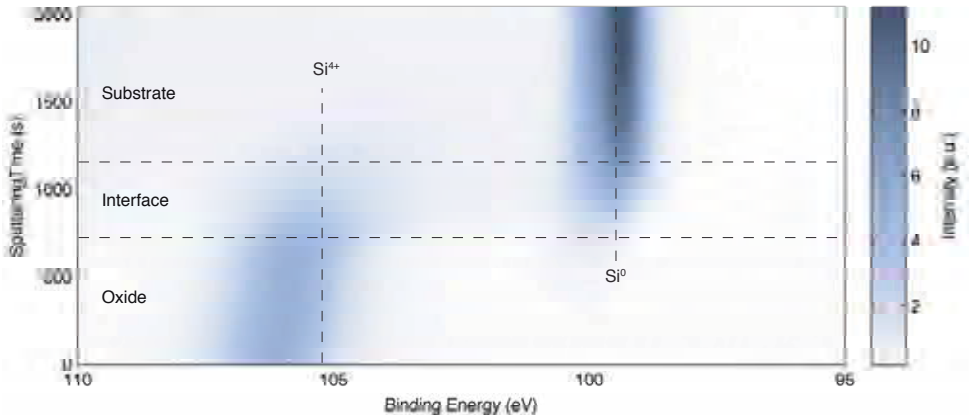
To perform this measurement on our samples, we grew nominally $35nm$ oxides and measured the shifting of the Si^{4+} peak in the XPS measurements. Figure 3.30(a) shows



(a) **800°C Thermal**



(b) **350°C UHV**



(c) **140°C UHV**

Figure 3.30: Depth-dependent XPS spectra for low-temperature UHV oxides compared to a high-quality thermal oxide. The depth-dependent spectra were recorded by argon sputtering the sample in $10s$ increments between XPS measurements. (a) This sample is a high-quality $40nm$ thermal oxide grown at $800°C$ followed by a $1000°C$ anneal. (b) This sample is a UHV-grown oxide deposited at a sample temperature of $350°C$, a pressure of $\sim 5 \times 10^{-6} mbar$, at a SUSI temperature of $\sim 705°C$. (c) This sample is a UHV-grown oxide deposited at a sample temperature of $\sim 140°C$, a pressure of $\sim 4 \times 10^{-6} mbar$, at a SUSI temperature of $\sim 710°C$.

depth-dependent XPS spectra of a $35nm$ thermal oxide grown at $800°C$ in the presence of dichloroethylene and annealed to $1000°C$. Dichloroethylene is used as a getterer of positive charges in the growth of high-quality oxides, and is used here as a reference for oxides without positive charges. The spectra are displayed as a $2D$ map with the intensity versus binding energy relationship, similar to that shown in Fig. 3.29, plotted as a function of argon sputtering time. The Si^{4+} peak is located at an energy of $104eV$ on the starting surface (zero etching time). As the oxide is sputtered, the peak undergoes a slight shift to lower energies, consistent with a reduction in the oxide charge.

The Si/SiO_2 interface is reached after $1000s$ of sputtering, at which point the peak spreads into a broad band centred at $105 \pm 1eV$. It is this interface region that gives spectra similar to that shown in Fig. 3.29, where both the Si^{4+} and Si^0 peaks are visible and there is an asymmetry of the Si^0 peak that arises from the $2p_{1/2}$ and $2p_{3/2}$ valence band states. As the sample is sputtered further, the Si^{4+} peak gradually fades, leaving only the Si^0 peak of the substrate at $\sim 99.5eV$.

Figure 3.30(b) shows XPS spectra of a $35nm$ UHV oxide grown at $350°C$ as a function of the sputtering time. The degree of oxide charging is more pronounced in this sample. After the first $10s$ of sputtering to clean the sample the Si^{4+} peak has already shifted to $105eV$. The Si^{4+} peak then shifts lower in energy with sputtering time, eventually occupying the same $105 \pm 1eV$ spread at the Si–SiO_2 interface as the thermal oxide sample shown in Fig. 3.30(a). The increase in the initial Si^{4+} binding energy, and the more dramatic shift of this peak with sputtering than the thermal oxide, indicate a greater amount of positive charge distributed throughout the oxide.

Figure 3.30(c) shows XPS spectra of a $35nm$ UHV oxide grown at $\sim 140°C$ at different sputtering depths. This sample shows a slightly more pronounced trend in the Si^{4+} peak shift, terminating in a nominally identical manner to the thermal oxide and $350°C$ sample at the interface.

Based on this study, it appears the low-temperature oxide contains a greater percentage of positive charges after sputtering than the high quality thermal oxide. This might be comprised in part by oxide trapped charge [42, pg. 129]. Studies of thermal oxide samples indicate that oxide trapped charge can be minimised with an anneal. None of the UHV-grown oxides presented in this chapter were annealed, which may explain the large quantity of distributed positive charge indicated by the XPS results. However, there is no discernible difference between the XPS spectra of the low-temperature oxide and the thermal oxide at the Si–SiO_2 interface. We therefore conclude from the XPS results that there is no direct evidence of sub-oxide species within the oxide, but the depth dependence does imply the presence of oxide trapped charge, particularly for oxides grown at lower

temperatures.

3.5 Electrical characterisation of the low-temperature UHV oxide

Since we are going to use the oxide as a dielectric in nanoscale devices, the electrical performance of the oxide is its most important characteristic. As a consequence we have designed simple MOS test structures to characterise the oxide before using the oxide on STM-patterned devices. With these test structures we can assess the leakage characteristics of the oxide, and measure the expected density of traps. A number of different test devices are typically used to quantify the performance of a gate oxide. Here we will use two of the most common: MOS capacitors and Hall bar MOSFETs.

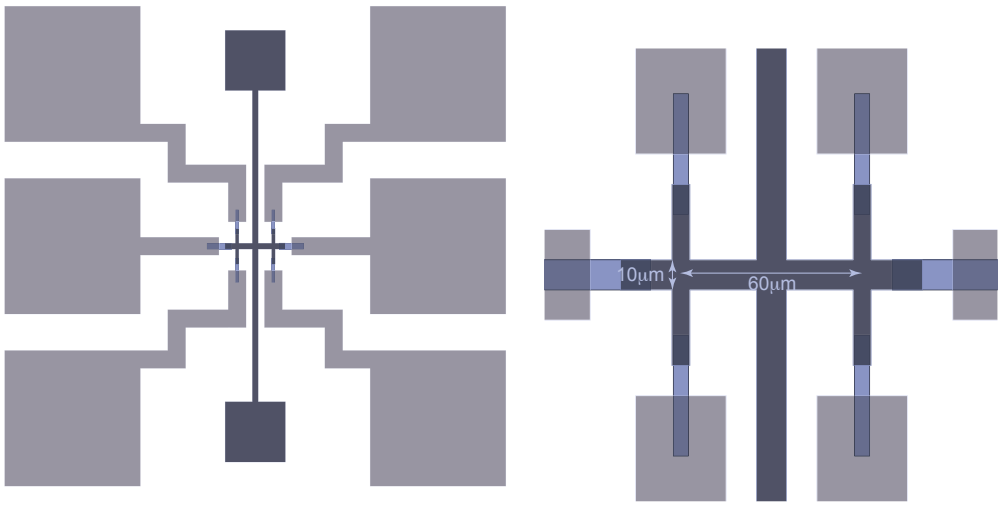
3.5.1 Design of electrical test devices

C-V capacitors

A MOS capacitor is constructed of a lightly doped substrate that is covered with a gate oxide, which is usually capped with a circular gate electrode. MOS capacitors can provide valuable information about the leakage current density, breakdown field strength, and—using C-V measurements—interface trap density and fixed oxide charge. However, C-V measurements are intolerant to leakage through the oxide and as a result, we will see the high defect densities present in our low temperature UHV oxides affected the quality of the C-V measurements.

Typically, reducing the leakage through a homogeneous oxide requires increasing the oxide thickness. To mitigate the associated drop in device capacitance, the gate area must be scaled proportionally. However, by making the gate area larger, there is a greater probability that the gate metal will overlap with the defects causing Ohmic shorts through the oxide. The minimum device capacitance, set by the C-V measurement apparatus, was specified as 50–100pF, where higher capacitances give more reliable measurements. We chose to target 75pF. The minimum oxide thickness for reliable operation during preliminary studies was $\sim 30nm$. Using this thickness, we knew that we needed to have gates with a radius of

$$r = \sqrt{C_{ox} \frac{t_{ox}}{\pi \epsilon_0 . \kappa_I}} \simeq 150 \mu m \tag{3.15}$$



(a) Full device (b) Close-up

Figure 3.31: Hall bar MOSFET design (a) The Hall bar MOSFET induces a 2DEG in the shape of a Hall bar using an aluminium gate electrode (dark grey). Electrical contact is made to the induced 2DEG using phosphorus doped regions, which overlap with the highly-doped source-drain contacts (blue-grey). Ohmic contacts are made to the doped regions using aluminium (light grey). (b) A close-up of the Hall bar showing the device dimensions: The gate electrode induces a 2DEG that is $10\mu m$ wide by $80\mu m$ long. Hall probes are used to contact the 2DEG with a longitudinal separation of $60\mu m$.

Another important factor in the design of MOS capacitors for C-V measurements is that, ideally we would place a thick field oxide under the capacitance probe to prevent mechanical punch-through of the oxide during the measurement. However, the high-temperature flash-anneal used to clean the samples when loading them into the UHV system prevents the use of a thick field oxide, because the field oxide sublimates from the sample during the flash. As a consequence, it was necessary to place the capacitance probe directly on the C-V gate electrode. This required a thick layer of metal for the gate structure ($> 100nm$), to prevent mechanical punch-through of the oxide during measurement. In this study, aluminium was used as the gate metal, although C-V measurements may be conducted with many gate metals provided that the metal work-function is properly calibrated.

Hall bar MOSFETs

Inducing a two-dimensional electron gas (2DEG) in the shape of a Hall bar allows the mobility and carrier density of the induced 2DEG to be measured directly. The carrier density is controlled by the effective capacitance of the gate structure, which is offset by the depletion and trap capacitances. The mobility of the 2DEG is determined by scattering mechanisms. At room temperature these mechanisms include phonon scattering from

the substrate, surface roughness scattering at the silicon-oxide interface, and Coulombic scattering from charges near the 2DEG, including charge traps and substrate dopants. At low temperature ($\leq 4.2K$), phonon scattering has virtually no effect on the mobility.

To assess the quality of the oxide, Hall bar MOSFET measurements were carried out at $4.2K$ (liquid helium temperature), as all STM-patterned devices fabricated for this thesis will be measured at cryogenic temperatures to prevent thermal broadening of carrier energies (especially for single electron transistors). The devices presented here are accumulation mode MOSFETs with an N^+-N-N^+ structure, to mimic devices patterned with STM-lithography. The substrates used for these devices are only lightly doped ($\sim 10^{15} cm^{-3}$), and become non-conductive at cryogenic temperatures. As such, the substrate effectively acts as an insulator until gated into accumulation [138].

Because of defects causing Ohmic shorts through the oxide, we aimed to make the Hall bar MOSFETs as small as possible in order to avoid overlap of the gate metal with a defect. The contacts of the Hall bar MOSFET were fabricated using furnace in-diffusion. This in-diffusion was conducted at high temperatures ($950°C$), and it was therefore necessary to dope the source and drain regions prior to depositing the low temperature oxide (so that we could fairly test the oxide without exposing it to high temperatures). Performing the source-drain in-diffusion before oxidation does mean however that the in-diffused regions were present during the $\sim 1100°C$ flash anneal performed for $1min$, which is used to clean the samples after loading them into the UHV system. For this reason, the in-diffused regions had to be well separated, since phosphorus is able to diffuse $\sim 2\mu m$ during such an anneal. As such, the Hall bar MOSFETs were designed with in-diffused regions separated by at least $5\mu m$. Under this constraint, the Hall bar MOSFET channel was designed to be $10\mu m$ wide. To give reliable Hall data, the length-to-width ratio of a Hall bar is required to be to be $\sim$ 6:1; as such, the MOSFET channel was designed to be $60\mu m$ long (from one Hall contact to the next). A plan view of the Hall bar MOSFET design is shown in Fig. 3.31.

As with the C-V test structures, the flash anneal made it impossible to use a thick 'field oxide' over the silicon substrate; consequently, the bonding of wires from the device to the chip package had to be performed on top of the low-temperature oxide. Although the gate bond pads were physically far from the active device region, the absence of a field oxide meant that the induced 2DEG formed with the gate extended all the way to the bond pads. For this reason, any mechanical punch-through during bonding would short the gate to the 2DEG below. Several schemes were trialled to prevent this issue, including depositing very thick gate metal ($\sim 1\mu m$), but ultimately we settled on depositing a thick layer of poly-methyl methacrylate (PMMA) under the bond-pad lead. This reduced the

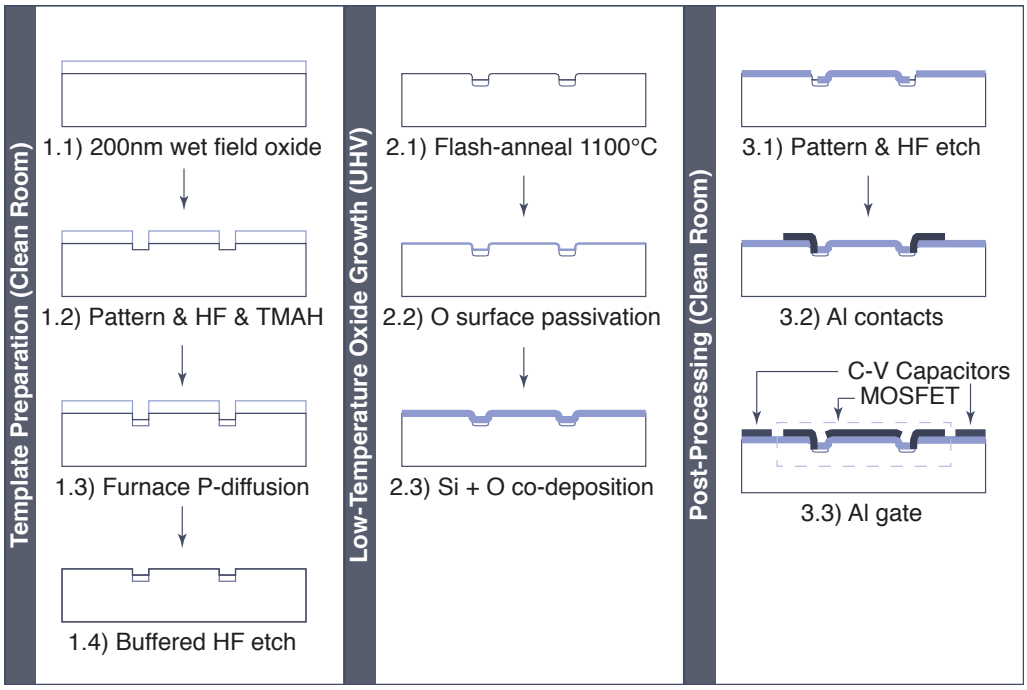


Figure 3.32: Fabrication strategy developed to electrically characterise low-temperature UHV dielectric using Hall bar MOSFETs and C-V capacitors. Hall bar MOSFET and C-V capacitor structures are patterned on every sample. Template wafers are prepared in a cleanroom, where source-drain regions are patterned using furnace in-diffusion. This requires the use of a $200nm$ field oxide to mask (1.1) against the diffusion process. The mask is patterned and etched using EBL, HF and TMAH (1.2). This etches the pattern slightly into the silicon substrate, so that the metal contacts may be aligned to the in-diffused regions. The P dopants are then diffused into the sample (1.3). The field oxide is then removed (1.4). The samples are then loaded into UHV and cleaned using a flash-anneal to $1100°C$ (2.1). The oxide is then deposited in two stages: the surface is first passivated using the atomic-oxygen source (2.2); the bulk of the oxide is then grown by co-depositing oxygen and silicon to reached the desired oxide thickness (2.3). The sample is then removed from UHV and metal contacts (3.1, 3.2) and gate electrodes (3.3) are patterned on the sample using EBL through a lift-off process.

capacitance of the bond-pad lead enough to prevent a 2DEG forming between the bond-pad and the device, isolating any leakage through the bond pad from the device itself.

Since the in-diffused regions were fabricated before depositing the gate dielectric, we required etched alignment markers in the substrate to align the metallic contacts and the gate to the in-diffusion regions. We achieved this by simply etching the source-drain regions by $\sim 50nm$ using tetra-methyl ammonium hydroxide (TMAH) before performing the in-diffusion.

3.5.2 Fabrication of electrical test devices

Both C-V capacitors and Hall bar MOSFETs were formed on all oxide samples. The fabrication process developed for these samples is shown in Fig. 3.32. The first stage of this fabrication process is to grow a $200nm$ wet field oxide, which is used as a mask for the in-diffusion process. This oxide is grown in a furnace at $1000°C$ for $1hr$ using high-purity (99.9999%) oxygen gas passed through deionised water held at $95°C$. This introduces water vapour into the oxidation process, increasing the growth rate.

Using electron beam lithography (EBL), the pattern of the source-drain regions is etched into the wafer using a buffered oxide etch (15:1 NH_4F:HF) and then a silicon etch (TMAH). Phosphorus is then diffused into the exposed silicon substrate at $950°C$ for $30mins$, giving a phosphorus doped silicon layer $\sim 1\mu m$ deep. The field oxide is then removed using a buffered oxide etch.

The sample is then loaded into the UHV system, and outgassed overnight at $400°C$. The sample is then flashed-annealed to $1100°C$ for $1min$, followed by a $10s$ anneal at $1100°C$. This forms atomically flat terraces on the silicon surface. At this point, the sample is imaged using the STM to ensure that it is clean. The sample is then transferred under UHV to the oxidation chamber.

In the oxide chamber, the sample is first exposed to the flux of atomic oxygen for $20min$, passivating the surface with a thin oxide. The shutter to the silicon sublimation cell is then opened, co-depositing silicon and oxygen. For the samples presented in this section and the STM-patterned devices in Chapter 5, the oxide growth rate was 0.2–$0.3nm.s^{-1}$, using a SUSI filament temperature of $930°C$. The plasma source was held at $350W$, using an oxygen pressure of $2.0 \times 10^{-6}mbar$. The samples were grown to a thickness of 28–$53nm$.

The oxidised samples are then removed from UHV. Windows are etched into the oxide to make contact to the in-diffused regions using EBL and buffered oxide etch. Aluminium contacts are then deposited, overlapping with the in-diffused regions. The contacts are typically given a forming gas anneal at $350°C$ for $15min$ to ensure good contact between the aluminium and doped silicon. An aluminium gate is then deposited to define the Hall-bar 2DEG, along with aluminium discs to form C-V capacitors. Approximately half of the devices receive no anneal of the gate metal, while the other half are annealed in forming gas at $350°C$ for $20min$; this permits assessing the as-grown oxide against the annealed oxide.

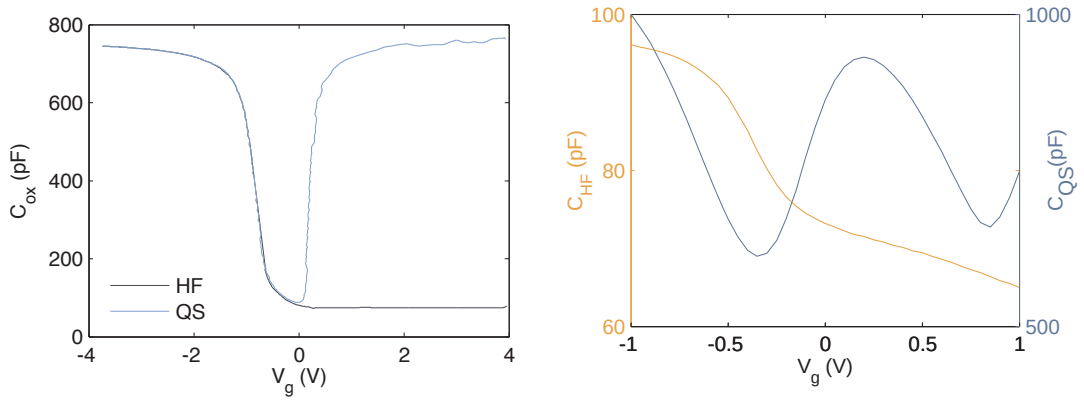


Figure 3.33: C-V Measurements of the oxide (a) C-V measurements of a thermal oxide control sample show the expected behaviour; the quasi-static capacitance drops when the structure is biased into depletion and the HF capacitance remains at or below the depletion capacitance in the inversion region. (b) C-V measurements of the low-temperature UHV oxide show a large offset in the QS capacitance, and the HF curve fails to saturate in the accumulation or inversion regimes. This is characteristic of large leakage currents through the oxide.

3.5.3 C-V measurements

Figure 3.33(a) shows C-V measurements conducted on a thermal oxide control sample, replicated here from Fig. 2.7(a) in the theory chapter of this thesis. In the region between accumulation and inversion, minority carriers play little role in substrate conduction. Any charge traps at or near this energy level therefore contribute to the measured capacitance. There is a time-delay associated with charge transfer to the trap, which causes a discrepancy between the HF and QS curves [43], as discussed in Sec. 2.4.1. Note that the interface trap density calculated is very sensitive to any imperfections in the capacitance measurements. For example, the slight but finite difference between the HF and QS curves of Fig. 3.33(a) gives a mid-gap trap density of $D_{it} \simeq 3\text{–}5 \times 10^{10}.cm^{-2}.eV^{-1}$. Both HF and QS measurements of capacitance are sensitive to leakage through the oxide. In the case of the QS measurement, the curve is constructed from the gate current. One can therefore expect large offsets in the measured capacitance when the gate leakage current is comparable to the capacitor charging current. Alterations to the HF curve are more subtle, and as a consequence the measured HF capacitance is more reliable. The HF measurement extracts the capacitance from the portion of the AC gate current that is 90° out of phase with the AC excitation voltage. When the capacitor leakage current is linearly proportional to the applied AC bias, the measured HF capacitance is unaffected by leakage. However, the leakage current of a MOS structure increases exponentially with

the applied bias. This creates harmonics of the applied AC signal in the capacitor leakage current, which contribute to the measured current 90° out of phase with the AC excitation. As a consequence, both HF and QS measurements are affected by gate leakage.

Figure 3.33(b) shows typical C-V measurements from a low-temperature UHV oxide test sample. The intended capacitance of the test structure was $\sim 75pF$. The mean value of QS capacitance curve is an order of magnitude greater than this; it also does not exhibit the expected QS capacitance shape. The HF curve shows capacitances of the right order, but it does not saturate in the inversion or accumulation regions. The unexpected shape of the QS and HF curves is attributed to gate leakage. This behaviour was consistent across all ∼100 MOS capacitors measured, which included both n-type and p-type substrates, post-oxidation annealed and as-grown samples, and post-metallisation annealed and as-deposited samples.

The high leakage of these samples can easily be understood by the overlap of the large area capacitor gate metal with the macroscopic defects on the sample surface shown in Fig. 3.25. The density of these defects on the surface is found to be $\sim 1.25 \times 10^{-12} cm^{-2}$. Given the required size of the capacitor structure ($150\mu m$ radius), it was not possible to avoid overlap between the capacitors and these defects. Smaller capacitors were fabricated using shadow-mask evaporation (to avoid potential oxide damage caused by EBL) that were only $100\mu m$ in diameter. However, these devices showed similar results. It was concluded that we would be unable to quantify the electrical quality of the low-temperature UHV oxide using C-V methods. However, we were able fabricate Hall bar MOSFETs that were significantly smaller than the C-V test structures.

3.5.4 Hall bar MOSFET measurements

Figure 3.34(a) shows a gate leakage curve of a working Hall bar MOSFET. The vast majority of these samples ($> 85 - 95\%$) did not work, instead showing an Ohmic short of the gate to the substrate. This was again attributed to macroscopic defects on the oxide surface, where some working samples were able to avoid overlap with a defect.

The traces shown in Fig. 3.34(a) are taken from a sample fabricated with the as-grown oxide, and a sample that has undergone a post-metallisation anneal for $20min$ in forming gas ($95\%N_2 : 5\%H_2$) at $350°C$. To be clear, the two samples were not completely identical before annealing; the only difference being that the oxide of the annealed sample was $53nm$ thick, whereas the oxide of the as-grown sample was $37nm$ thick.

The tunnelling current density of the annealed oxide is

$$J = \frac{20 \times 10^{-12} A}{\sim 2 \times 10^{-4} cm^2} = 1 \times 10^{-7} A.cm^{-2} \tag{3.16}$$

Here we assume leakage occurs over the entire area of the gate, including the bond-pads, since a 2DEG is also induced in this area. Since the MOSFET is an accumulation-mode N-type MOSFET, the Fermi level sits within a few tens of mV from the conduction band at $4.2K$; almost the entire gate voltage is therefore dropped across the oxide. Under this assumption, the electric field within the oxide at the maximum gate voltage is

$$E = \frac{5V}{53 \times 10^{-7} cm} \simeq 1MV.cm^{-1} \tag{3.17}$$

When can therefore verify that the annealed sample shown here meets the breakdown field ($\geq 1MV.cm^{-1}$) and leakage requirements ($J \leq 1 \times 10^{-6} A.cm^{-2}$ at $0.5MV.cm^{-1}$) as specified in Table 3.1 of Sec. 3.2.1.

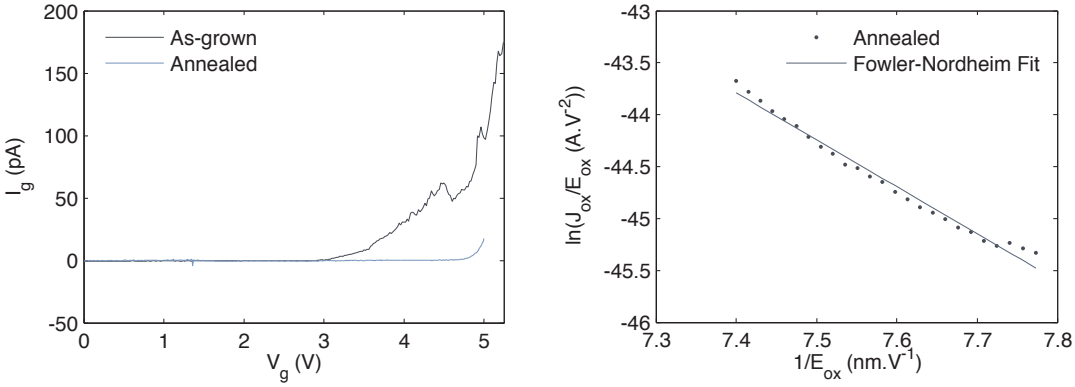
Figure 3.34(b) shows a fit to the leakage curve of the annealed sample using an oxide effective mass of $m^* = 0.5 \times m_e$, and a barrier height of $\psi_B = 2.9eV$ with the Fowler-Nordheim fitting formula [72]:

$$J = q_e^3 E^2 / 8\pi h \psi_B e^{-4(2m^*)^{1/2} \psi_B^{3/2} / 3\hbar q_e E} \tag{3.18}$$

This is similar to the stated literature value of $m^* = 0.4 \times m_e$ and $\psi_B = 3.2eV$ [139, pg. 232]. Leakage data of similarly thick thermal oxide samples made for this thesis do not show any measurable leakage ($< 10pA$) up to gate biases of $15V$. It is therefore clear that the low-temperature UHV oxide leaks more than a thermal oxide of the same thickness.

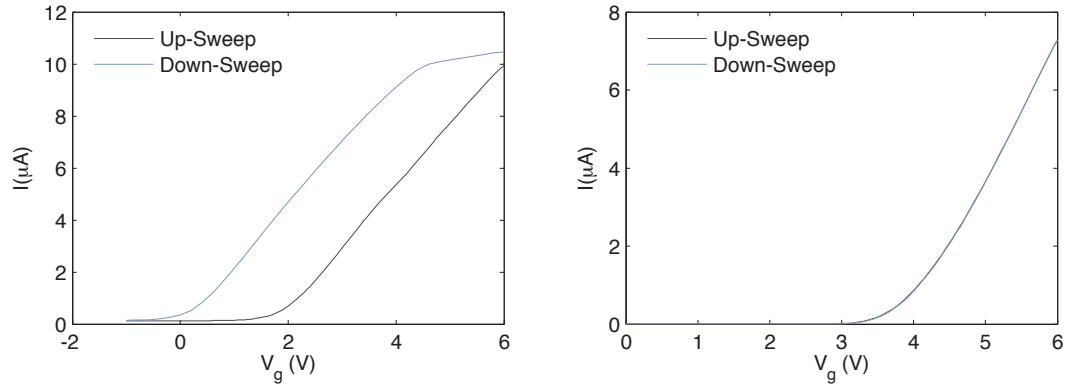
Figure 3.35 shows the gating action of the two samples shown in Fig. 3.34. Figure 3.35(a) shows hysteresis in the gating action of the as-grown sample. This hysteresis was present in all as-grown low temperature UHV samples measured. Figure 3.35(b) shows the gating action of the annealed sample. The annealed samples were the only samples to show no perceptible hysteresis in the gating action: the up-sweep and down-sweep in this figure are virtually identical.

The threshold voltage of the annealed sample is higher than that of the as-grown sample. The difference cannot be attributed solely to the increase in oxide thickness ($53nm$ vs. $37nm$). It is likely that the difference is caused by the anneal, since the presence of hydrogen during the anneal is known to passivate dangling bonds when atomic hydrogen permeates through the formed oxide to bind with the unsaturated bonds of the silicon atoms [44].



(a) (b)

Figure 3.34: Gate leakage current of the as-grown oxide. (a) This is the gate leakage current measured for a N^+-N-N^+ MOSFET before conducting any other measurements on the device. For this device there are some minor resonances in the gate leakage curve that are not reproducible. This may be the result of trapping and detrapping events changing the potential landscape within the oxide, or it might be indicative of electromigration of atoms within the oxide. Based on this measurement we set an upper limit on the gate voltage of $5.0V$, which keeps the leakage current below $100pA$. (b) This is the gate leakage of the annealed sample plotted on a Fowler-Nordheim diagram. The fit gives an effective mass of 0.5 times the free electron mass, and a barrier height of $2.9eV$, both of which are similar to the stated literature values.



(a) Un-annealed (b) Annealed

Figure 3.35: Hysteresis in the UHV oxide and the effect of a post-metallisation anneal. (a) The hysteresis measured in the gate transconductance is indicative of trapped charge within the as-grown UHV gate oxide. (b) This sample was grown under similar conditions to that of Fig. 3.35(a), and then annealed at 350°C for $20min$ in forming gas ($95\%N_2 : 5\%H_2$). The hysteresis is eliminated, but the threshold voltage has drastically increased.

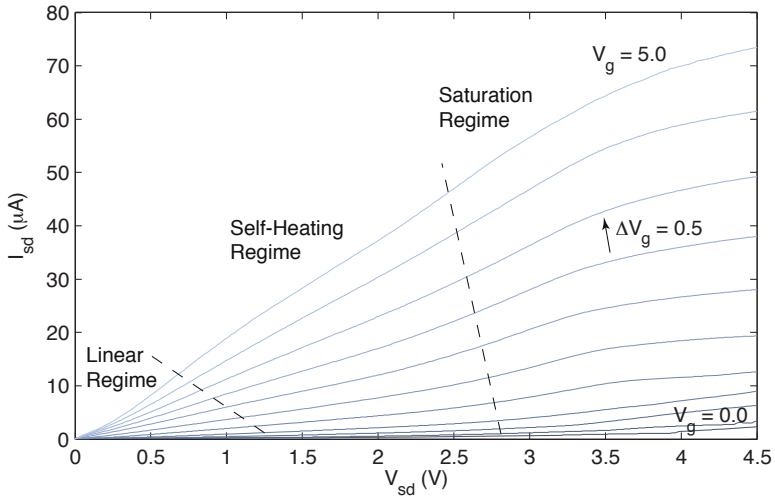


Figure 3.36: Current-voltage curves of a Hall bar MOSFET with a low-temperature UHV gate oxide. These curves were recorded from an N^+-N-N^+ MOSFET structure. This device acts as a MOSFET only because the substrate carriers freeze-out at low temperatures. This creates a small potential barrier between source and drain. The low temperature measurement and small potential barrier create subtle changes to the I-V curves. At an intermediate source-drain bias (e.g. $2.0V$ for $V_g = 5.0V$) there is a downward curvature in the I-V curve in a section of the curve that is typically straight. This is a result of localised heating within the pinch-off region, which generates intrinsic carriers that pull the local fermi level closer to mid-gap, which causes the channel resistance to go up. In the high source-drain bias region, impact ionisation of the substrate in the pinch-off region begins an avalanche breakdown of the substrate and so the I-V curve continues to increase where it would typically saturate.

Figure 3.36 shows source-drain current-voltage measurements of the as-grown sample, with gate voltages ranging from 0 to $5V$. The traces match the generally expected shape of a linear increase in current with source-drain voltage until the channel pinches off, where the current begins to saturate. There are some subtle variations to standard MOSFET I-V data. There is a slight downward curvature in the linear conduction region. This is attributed to self-heating of the MOSFET channel [140], which creates both intrinsic carriers and phonons. The intrinsic carriers pull the local chemical potential closer to mid-gap. Since this is an accumulation mode MOSFET, this reduces the gate-substrate bias, making the channel more resistive. At higher source-drain biases ($> 2 - 3V$), the channel current continues to increase with source-drain voltage. This is attributed to impact ionisation of extrinsic carriers within the substrate, which are ordinarily frozen out at $4.2K$ [138]. This manifests in a similar manner to breakdown of the silicon substrate, with current eventually increasing exponentially with source-drain bias. In this figure, the effect is most pronounced at low gate biases ($V_g \leq 1.5V$) as a MOSFET pinches off at lower source-drain biases in this gate range.

To now, all of the data discussed could equally have been collected from traditional three-terminal MOSFET structures. Figure 3.37 shows data collected in which we exploit the Hall bar shape of the induced 2DEG. The y-axis of this plot shows the measured mobility of the MOSFET channel. The x-axis shows the measured carrier density. The carrier density is measured directly using Hall resistance measurements, in which a perpendicular magnetic field passing through the 2DEG is swept, the associated bias induced across the Hall bar is inversely proportional to the 2DEG carrier density:

$$n_s = \frac{1}{e}\frac{I_{sd}}{V_{Hall}}.B \tag{3.19}$$

Where e is the electron charge, I_{sd} is the source-drain current, V_{Hall} is the voltage across the width of the Hall bar at magnetic field B.

The mobility is calculated from the device conductivity:

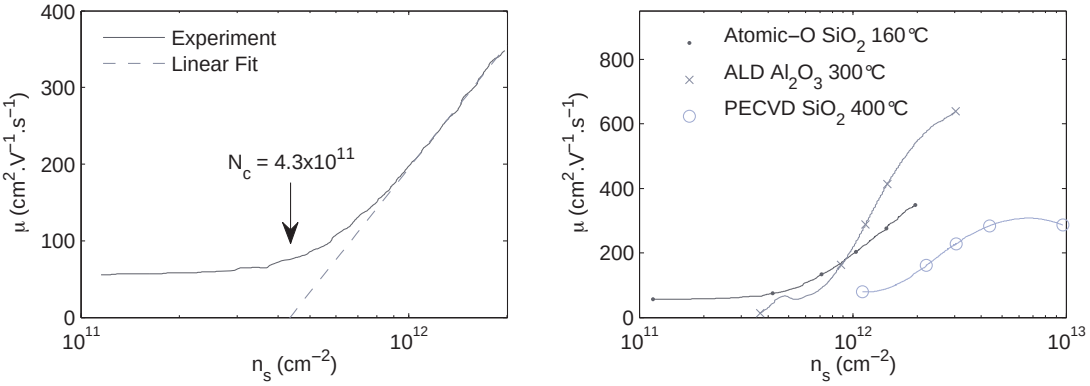
$$\mu = \frac{L}{W}\frac{I_{sd}}{V_{sd}}\frac{1}{n_s e} \tag{3.20}$$

Where L and W are the length and width of the Hall bar, respectively, and V_{sd} is the source-drain voltage.

In the carrier density range shown in Fig. 3.37 ($n_s = 0.1$–$2 \times 10^{12} cm^{-2}$), the mobility increases as a power law of the carrier density in the high-density region. At low densities the mobility is dominated by Coulombic scattering, where conduction electrons are perturbed as they pass near charge centres within the substrate or at the interface. These charge centres are likely dopants in the substrate, interface traps, or fixed oxide charge near the interface. As the carrier density increases, these charge centres are shielded by carriers, and their effect on the sample mobility becomes less pronounced. As a result, the sample mobility increases. The turning point in the mobility/carrier-density curve corresponds to the point at which carriers begin to screen out the Coulomb potential of charges. This is likely to require multiple carriers per charge centre, but as a conservative estimate we assume a one-to-one ratio. We refer to this turning point as the 'critical density', after Das Sarma *et al.* [141]. The critical density of the sample should therefore be proportional to the combined 2-D density of charge centres at the interface, which is composed of

$$N_c = A \times \left(N_{it} + N_D^+ + N_{FO}\right) \tag{3.21}$$

Where A is a constant that defines the number of free carriers necessary to shield the potential of each charge centre, N_{it} is the areal density of interface traps, N_D^+ is the 2-D density of ionised dopants at the interface, and N_{FO} is the equivalent 2D density of fixed



(a) (b)

Figure 3.37: Critical density in the mobility/carrier-density curve. The Hall bar structure can be used to measure the carrier density of the MOSFET as a function of the gate voltage. Increasing the gate voltage increases the number of carriers in the induced 2DEG. The free carriers act to shield any Coulombic scattering potentials near the 2DEG, increasing the effective device mobility with increasing carrier density. The point of equivalence, below which the mobility essentially saturates, is the critical density. This critical density is proportional to the number of charge centres that actively scatter conduction electrons in the 2DEG.

oxide charges that have an effect on the 2DEG.

The critical density of the (un-annealed) sample from Fig. 3.35(a) has been determined from the mobility measurement shown in Fig. 3.37(a) as $N_C \simeq 4.3 \times 10^{11}.cm^{-2}$. If there is one free carrier to shield the effects of a charge centre from the 2DEG, and assuming that the charge centres present are composed entirely of interface traps, this implies an upper limit on the areal density of interface traps of $N_{it} \simeq 4.3 \times 10^{11}.cm^{-2}$. However, the true number is likely to be several-fold lower because more than one electron would be required to properly shield the Coulomb potential of each trap unless that electron is captured by the trap itself. For comparison, McCamey *et al.* have shown a critical density of $1-2\times10^{11}.cm^{-2}$ for a high-quality thermal oxide [142]. McCamey also studied the critical density of ALD-grown Al_2O_3 and PECVD grown SiO_2 at low temperature, the results of which are shown in Fig. 3.37(b). The trace from Fig. 3.37(a) is overlaid on McCamey's data in Fig. 3.37(b) for comparison. The low-temperature UHV oxide compares favourably to both of McCamey's samples, despite the lower growth temperature. It is not yet clear how the measured critical density of our low-temperature oxide might translate to a density of electrically active traps for atomic-scale devices (D_{it}). However, the measured critical density is in line with the expected interface trap density for the plasma-grown oxide.

After a post-metallisation anneal, many of the Hall bar samples began to leak through the gate before the 2DEG was induced, and we have therefore not been able to extract the

Table 3.4: Measured performance of the dielectric for atomic-scale devices.

Name	Symbol	Target Value	Success
Breakdown field strength	E_{BD}	$\geq 1MV.cm^{-1}$	Yes
Leakage current density	J	$\leq 10^{-6}A.cm^{-2}$ at $0.5MV.cm^{-1}$	Yes
Interface trap density	D_{it}	$\leq 10^{10}cm.^{-2}.eV^{-1}$	TBD
Oxide thickness (for selectivity)	t_{ox}	$\leq 15nm$	Yes*
Growth chamber base pressure	p_{base}	$\leq 10^{-10}mbar$	Yes
Growth temperature	T	$\leq$ 210–300$^{\circ}C$ for $3hrs$	Yes

* Performance not assessed at this thickness, but theoretically achievable using this technique

critical density after a post-metallisation anneal. Our experience so far indicates that yield issues are dominated by macroscopic defects within the oxide. For this reason, small (i.e. atomic-scale) devices are likely to exhibit substantially better yields, since the probability of a small device overlapping with a defect is negligible.

3.6 Chapter summary

This chapter described the development of a low-temperature silicon dioxide deposition technique, commensurate with the thermal budget of atomic-scale devices patterned with STM-lithography. The gate oxide requirements for atomic-scale devices were quantified, and compared to a variety of materials and techniques used to deposit gate dielectrics.

Silicon dioxide was selected as the preferred material system for use as a dielectric based on its performance in published literature, its high barrier ($3.2eV$), and the simplicity and compatibility of the techniques used to deposit it at low temperature in UHV. An ultra-high vacuum oxide deposition chamber was designed to grow low-temperature silicon dioxide, which proved capable of depositing thick silicon dioxide layers down to temperatures of $140^{\circ}C$.

Structural and chemical testing of the low-temperature oxide indicated that it was indistinguishable in composition and structure from a high-quality thermal oxide using XPS and TEM. However, a higher than expected etch rate in hydrofluoric acid was observed, consistent with the formation of a low density oxide. In addition, signatures of

oxide trapped charge were visible via XPS, which appeared to improve with higher growth temperatures.

The electrical quality of the low-temperature oxide was assessed using capacitance-voltage measurements and Hall bar MOSFETs. These samples showed large leakage currents through the oxide, which were attributed to the presence of macroscopic defects in the oxide bulk visible with optical microscopy. The density of these defects was $\sim 1.25 \times 10^{-12}.cm^{-2}$; giving one defect on average every $8000\mu m^2$. With the C-V capacitors used to measure the interface trap density having an area of $100,000\mu m^2$, many of the C-V capacitors leaked. However, with an area of just $20,000\mu m^2$, including the gate bond pads, the smaller area Hall bar MOSFETs were less affected by leakage, which allowed us to determine the critical density from the carrier mobility, giving an indication of the interface trap density.

Table 3.4 lists the performance of the oxide measured in this chapter against each of the requirements for a scalable quantum computing architecture. In regions unaffected by macroscopic defects, it is clear that the oxide meets all but two of the requirements: Firstly, although we achieved an as-grown density of interface traps of $N_{it} < 4.3 \times 10^{11}.cm^2$ and anticipate this is likely to reduce after a forming gas anneal [44], we have been unable to characterise the annealed oxide due to the high density of macroscopic defects in the oxide. Secondly, while it is possible to achieve oxide thicknesses down to one monolayer, we have not optimised the growth at a thickness of $15nm$. This will be the subject of further work.

The macroscopic defects observed in optical microscopy seem inherent to the fabrication process; work continues towards minimising or eliminating them. It is not yet known whether result from spitting of the silicon sublimation source or if they are are inherent to the low-temperature oxide itself. However, the sparse nature of their distribution implies that they will have negligible impact on the yield of atomic-scale devices, especially where the gate area is no more than $1\mu m$ across.

Chapter 4

Fabricating In-Plane Gated, STM-Patterned SETs

In 2009, Fuhrer *et al.* made the first STM-patterned single electron transistor (SET). This device used phosphorus-doped silicon gates patterned in the same plane as the source and drain regions to control a 4000 donor dot [22]. This in-plane gating scheme showed exceptional stability, with only three charge rearrangements over a 24 hour period. In addition to the proposed use of quantum dots as qubits [143], quantum dots configured as single electron transistors are extremely capable charge detectors [144] and are particularly sensitive to charge noise. In this chapter we have adapted the design by Fuhrer *et al.* to create a quantum dot with ∼200 donors. This device will be used to quantify the noise and stability of STM patterned epitaxial gate architectures. We use this SET to compare the electrical stability of the in-plane gating scheme with the metallic surface gates discussed in Chapter 5.

4.1 Introduction

The conductance of an SET is controlled with a gate, in an analogous way to MOSFETs, but the response is highly non-linear because of a small conducting island situated between the source and drain. Electrons on the island repel one another with such force that it is difficult to add an electron without first emitting one to the drain; under this condition, electrons tunnel sequentially between the source, island, and drain. Since an electron can only pass to the drain if it is energetically favourable, we can prevent conduction through the device by lowering the island potential using the gate. This condition is known as Coulomb blockade.

The clearest example of Coulomb blockade was first observed in silicon quasi-1D wires in 1989 by Scott-Thomas *et al.* [145], though the effect was visible in earlier devices [146]. In Scott-Thomas's study, a MOSFET inversion layer was confined to a width of $25nm$ using a double gate structure. The high mobility samples had a mean free path of 100nm, such that the lateral confinement created quasi-1D channels. However, instead of seeing

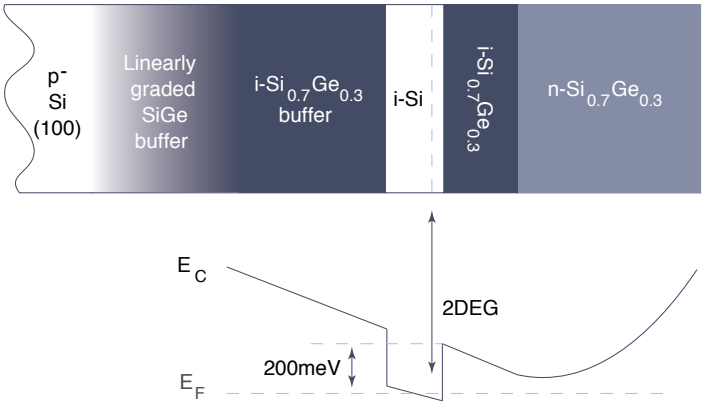


Figure 4.1: A Si–SiGe heterostructure used for making single electron transistors. Using a linearly graded SiGe buffer it is possible to form a SiGe layer whose lattice constant is sufficiently large to strain an intrinsic silicon layer, making a potential well separated from the doped capping layer. The dopants in this capping layer give their electrons to the well, making a high-mobility 2DEG. Adapted from Paul *et al.* [85]

the expected 1-D behaviour, Scott-Thomas *et al.* observed peculiar oscillations in the device conductance. Over the next three years, many papers attempted to explain these fluctuations, most notably Sols *et al.* [147], Averin *et al.* [148], Meir *et al.* [149], and Beenakker *et al.* [52, 150], eventually leading to the review of the so-called 'single electron transistor' by Kastner in 1992 [151]. The operating principles of single electron transistors detailed within these and later references [46, 47] are summarised in Section 2.5 of this thesis. We begin this chapter with an overview of the state of the art in silicon-based SETs and go on to describe two in-plane gated SETs fabricated within our group. Following this we outline the design, fabrication, and analysis of an in-plane gated SET, which we use to quantify stability and noise. This analysis focusses on the excited state spectroscopy — including signatures of coupled traps — and the noise and stability of the SET evident within electrical transport measurements.

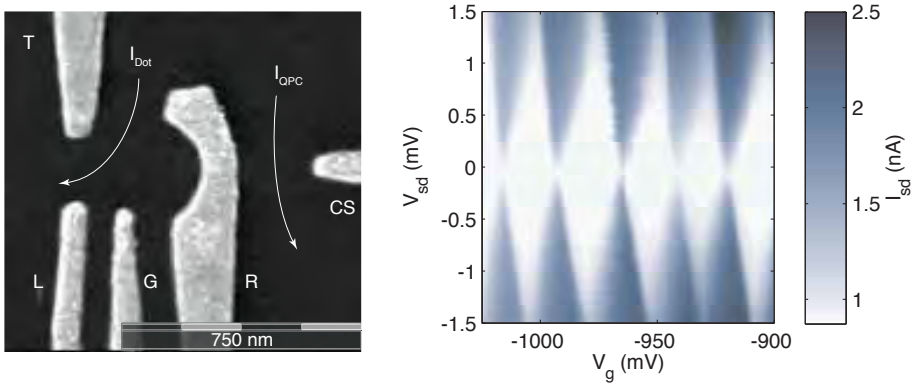
4.2 Review of single electron transistors in silicon

4.2.1 Gate-defined SETs in silicon

There have been many electrostatically-defined single electron transistors published in the scientific literature, particularly using MOSFET inversion layers [25–27, 145], and heterostructures of $GaAs$–$AlGaAs$ [46, 152–154] or Si–$SiGe$ [97, 155–162]. Quantum confinement within such zero-dimensional systems forms quantum dots that, when reduced to the few electron limit, may be used as spin qubits [143]. One of the aims of our group is to make a phosphorus-in-silicon spin qubit because of the long electron spin coherence time in silicon [10, 13, 19]. As a consequence, we review a selection of state of the art few-electron silicon-based SETs.

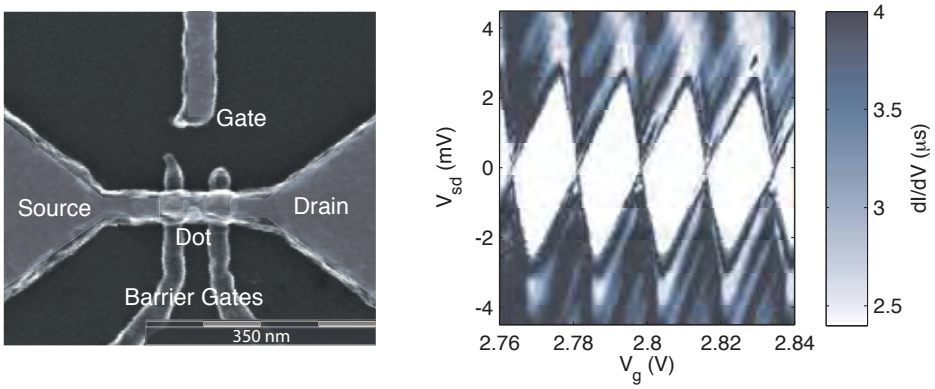
Si–SiGe SETs formed by electrostatically depleting a 2DEG

The doped capping layer of a Si–$SiGe$ heterostructure causes local band bending that can be exploited to induce a 2DEG in a strained silicon layer; as an example we show the heterostructure described by D.J. Paul in Fig. 4.1 [85]. The extrinsic electrons from the doped capping layer pass to the well and form a 2DEG. The isolation of the 2DEG from the dopants via the $Si_{0.7}Ge_{0.3}$ spacer results in high carrier mobilities (e.g. the highest mobilities recently reported are $1.6 \times 10^6 cm^2 V^{-1}.s^{-1}$ [163]), since carriers are unperturbed by scatterers or charge traps. This epitaxial system is an excellent environment for making single electron devices, but fabricating devices from Si–$SiGe$ heterostructures requires lateral confinement of the 2DEG. Lateral confinement is typically achieved either by etching through the 2DEG or by localised depletion of the 2DEG using gates — both of which have been successfully demonstrated by the group of Eriksson *et al.* [97, 157, 161, 162]. An example of localised depletion from the Eriksson group is shown in Fig. 4.2(a) [161]. There is a high mobility 2DEG below the entire area shown in this figure (black region), which can be depleted with surface gates (light grey areas, labelled T, L, R) to form an isolated quantum dot. The device in Fig. 4.2(a) also has a charge sensor in the form of a quantum point contact, defined and tuned using the charge sensor (CS) gate. Simmons *et al.* were able to use this sensor to verify that the dot was emptied to the last electron, well beyond the detection limit of transport spectroscopy. Figure 4.2(b) shows the transport spectroscopy of this dot in the many electron regime, where we clearly see Coulomb blockade diamonds — regions in the gate-drain voltage space where there is no conduction through the device — with a charging energy of $1.6meV$. In 2009, Simmons *et al.* used



(a) (b)

Figure 4.2: A gate-defined SET in Si-SiGe. (a) SEM image of the device, showing the gate structure used (light grey areas) to deplete the underlying 2DEG (dark regions). A quantum point contact, defined using the CS gate, is used to detect the occupancy of the dot. (b) The stability diagram of this device shows regular Coulomb blockade diamonds in the many electron regime. Using the quantum point contact, Simmons *et al.* were also able to prove they depleted the dot to the last electron [161].



(a) (b)

Figure 4.3: SET in a MOSFET inversion layer. (a) SEM image of an induced SET, formed by the inversion layer of a MOSFET. The two barrier gates pass under the global MOSFET top-gate, which are used to form tunnel barriers between source, dot, and drain. (b) The stability plot of this device shows extremely sharp, regular diamonds when populated with many electrons. [26]

a modified version of this gating scheme to form a double quantum dot with tuneable dot-dot coupling [162] — an important step towards controllable silicon spin-qubits.

Induced SETs in Si using MOS structures

In addition to the localised depletion of heterostructure 2DEGs, it is possible to induce quantum dots using MOS gates [25–27, 145]. Figure 4.3(a) shows such a device fabricated by Angus *et al*, which uses a global (butterfly-shaped) top gate to simultaneously induce the source, dot, and drain, patterned over thin aluminium barrier gates used to form the tunnel barriers [26]. The barrier gates and top gate are isolated by a thin layer of aluminium oxide, formed by oxidising the barrier gates using an oxygen plasma; the nearby finger gate is used to tune the dot potential. With this architecture, Angus *et al.* were able to see clear Coulomb blockade diamonds with a charging energy of $2.5meV$, and excited state lines running parallel to the CB diamond edge (see Fig. 4.3(b)) separated in energy by $\sim 200\mu eV$. With this structure, the transparency of the tunnel barriers is variable, allowing an appreciable current to be maintained through the dot even as it is depopulated towards the last electron. This device architecture was later improved upon by Lim *et al.* [164], who added a third gate to give independent control of the density of states in the source and drain leads. Using this device, Lim *et al.* were able to push the occupancy of the dot down to what appeared to be the last electron. Using a similar scheme Morello *et al.* recently fabricated a $Si{:}P$ qubit, where a single donor was implanted into the substrate between the gate electrode and SET island [19]. Using this device, Morello *et al.* were able to preferentially load and empty an electron from the donor based on the electron spin. They measured a spin lifetime of $\sim 6sec$, significantly longer than the gate control pulses required for a physically realisable quantum computation scheme [165].

4.2.2 Doping-defined silicon SETs

Implated Si:P SET

In 2006, Hudson *et al.* fabricated an SET by implanting P into a silicon substrate capped with a thin gate oxide [166]. The sample was then annealed at $1000°C$ for $5s$ to remove the implantation damage, and aluminium source, drain, and barrier and side gate electrodes were deposited using EBL. The device contained $\sim 600e$ on the SET island, which could be tuned by several tens of electrons. The device had a charging energy of $415 \pm 66\mu eV$, and a small gate lever arm of $C_g/C_\Sigma = 0.0036$, because the side-gate electrodes were situated far from the dot ($>100nm$). The charging energy of this device varied greatly throughout the gate range, and the Coulomb blockade was aperiodic. This was attributed to capacitive coupling to either charges at the Si–SiO_2 interface, or donors migrating during the high-temperature RTA used to anneal out the implantation damage.

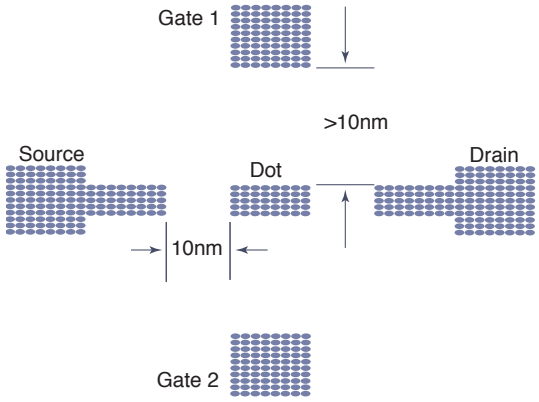


Figure 4.4: Theoretical proposal for a planar SET formed by dopants. This is the design of the SET proposed by Tucker *et al.* conisting entirely of dopants in a single atomic plane, compatible with the STM fabrication scheme.

STM-patterned SETs

In 2000, Tucker *et al.* proposed the concept of a planar single electron transistor consisting of 2-D sheets of dopants that could be made with STM lithography (Fig. 4.4) [11]. To determine a suitable geometry for such devices, Tucker *et al.* estimated the electron wavefunction would extend $\sim 4nm$ into the substrate from the patterned donors, based on the calculated Bohr radius[1]

$$\begin{aligned} a_B &= \frac{4\pi\hbar^2}{m^* e^2} \\ &= 3.3nm. \end{aligned} \tag{4.1}$$

Tucker *et al.* proposed spacing the tunnel barriers $\sim 10nm$ apart to achieve an appropriate degree of tunnel coupling. The design also includes in-plane gates, which are spaced further than $10nm$ from the dot to minimise gate leakage.

Since Tucker's original concept, our group has developed the technology to realise this architecture and demonstrated several such all-epitaxial SETs. In Tucker's original design it was hoped that the dopants would be ordered, but extensive studies by our group have shown this not the be the case [30]. The first such device that our group fabricated consisted of a large SET containing approximately 4000 electrons on the central dot [22]; more recently a small SET has been produced, estimated to contain 7 electrons [23]. These devices are at the geometric extremes of SET dimensions: The larger device is dominated by classical charging behaviour, while the smaller device clearly shows quantum

[1] In an earlier paper [167], Tucker *et al.* used a directionally averaged value of the effective mass, giving $a_B = 2.5nm$. The value calculated here is based on the electron travelling only in the $\langle 100 \rangle$ plane, with $m^* = 0.19m_0$.

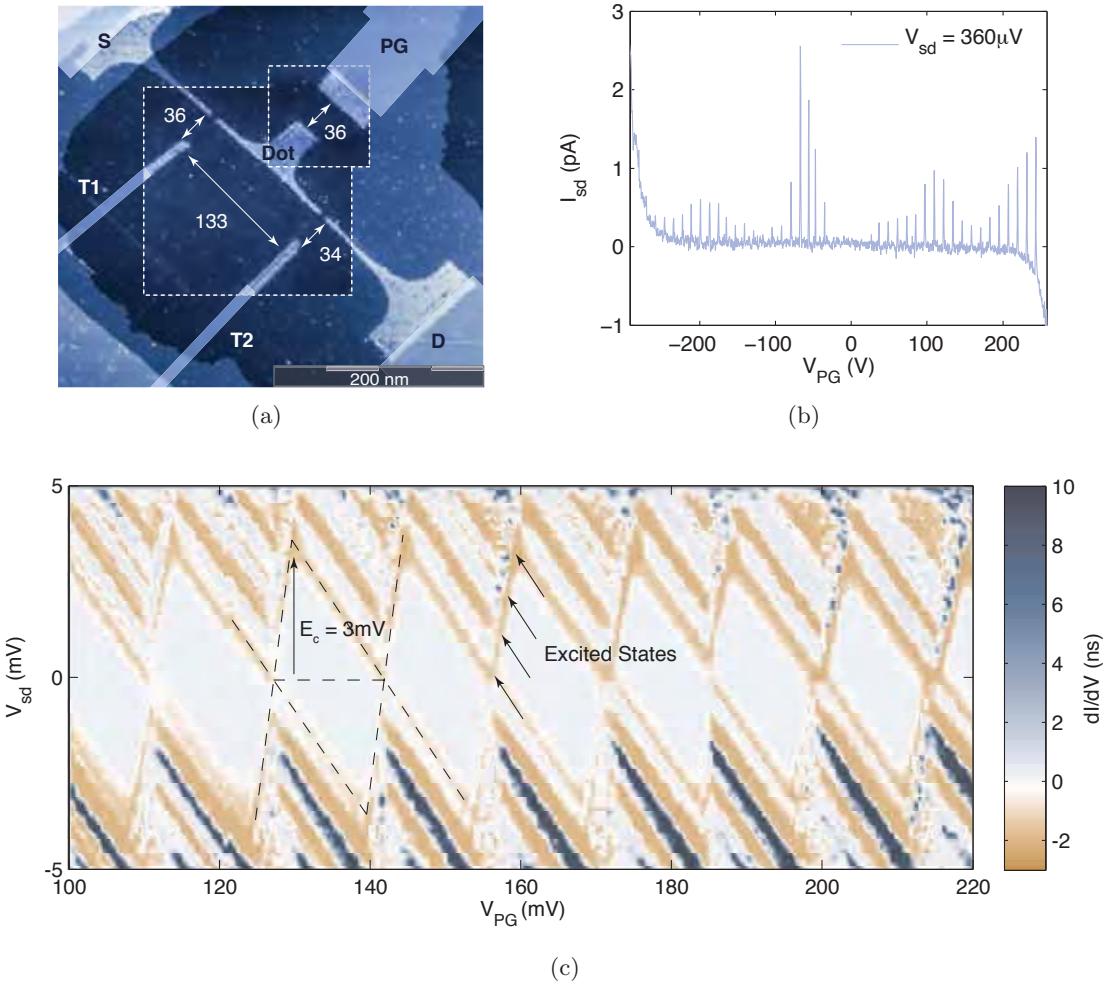


Figure 4.5: 4000 donor SET fabricated by A. Fuhrer *et al.* [22] with STM lithography. (a) An STM image of 4000 donor silicon SET immediately after patterning the hydrogen resist, but before dosing the sample with phosphine. (b) Sweeping the plunger gate (PG in (a)) at a small source-drain bias shows many sharp Coulomb blockade peaks. (c) Plotting the differential conductance of the device as a function of source-drain bias, we find a charging energy of $\sim 3eV$, and many excited state lines. [22]

confinement effects. Here we describe these two devices in greater detail to give context for the single electron transistors made for this thesis.

Classical (4000e) all-epitaxial SET

The large all-epitaxial SET published by Fuhrer *et al.* is shown in Fig. 4.5(a); the bright areas in this image demarcate lithographically exposed silicon in the hydrogen resist. Following this, the surface was dosed with PH_3 gas and subsequently encapsulated with epitaxially-grown silicon, creating 2-D sheets of phosphorus within the patterned regions.

The 2-D sheets of donors formed by this process are metallic at cryogenic temperatures ($< 70K$) — whereas the lightly doped substrate is insulating — giving an isolated quantum dot that is tunnel-coupled to the source and drain. Electrons tunnel from the source in the upper left of Fig. 4.5(a) to the dot, then to the drain in the lower right. There are three in-plane gates, labelled PG, $T1$ and $T2$. The broad plunger gate (PG) electrode is strongly capacitively coupled to the dot. The two remaining gate electrodes alter the transparency of the source and drain barriers, and were made as thin as possible to minimise coupling to the dot. The device resistance is dominated by transport through the source-drain tunnel barriers, which have since been optimised by a systematic study of tunnel gaps conducted within our group by Pok [168]. The tunnel gap dimensions of this device ($8nm \times 4nm$) give a peak conductance of $<10nS$, which minimises lifetime broadening of the electron energy enough to see clear Coulomb blockade resonances in the device conductance (Fig. 4.5(b)). Based on the geometry of the device and the doping density of the STM-fabrication scheme, we expect approximately 4000 phosphorus atoms, and therefore 4000 electrons on the dot at equilibrium (all leads grounded). Using the plunger gate, it is possible to alter this number by $\sim 50e$, as shown in Fig. 4.5(b) where each peak corresponds to a transition in the number of electrons on the dot. At the extremities of the plunger gate range, the gate leakage exceeds the source-drain current, masking all further transitions.

Figure 4.5(c) shows the stability plot of the $4000e$ SET, where the differential conductance is plotted as a function of the drain and gate biases. At zero source-drain bias there are clear diamonds of zero conductance, where conduction is prohibited by Coulomb blockade. From the vertical (source-drain) extent of the blockaded regions, we find an addition energy of $E_c \simeq 3meV$, which remains constant over each the shown transitions. This is expected when the single-particle energy spacing, ΔE, from quantum confinement within the dot is much less than the classical charging energy, E_c, from Coulombic repulsion, so that the energy required to add an electron to the dot, E_{add}, is

$$E_{add} = E_c + \Delta E \tag{4.2}$$

$$\simeq E_c \iff E_c \gg \Delta E. \tag{4.3}$$

In this 2-D map we see lines of constant differential conductance running parallel to the Coulomb diamond edges, which are characteristic of changes in the number of electronic states participating in conduction — so-called 'excited states'. There are resonant features in this plot separated in energy by 250–$500\mu eV$, which show both positive and negative differential conductance, indicating that excited states are moving both into and out of

the bias window.

Escott *et al.* have given a detailed review of the variety of such resonant features expected in the conductance of single electron transistors [48]. In this 4000 electron dot, we expect contributions from spin excited states, valley excited states, and density of states variations in the leads. These different excited states are described in more detail in the theory section of this thesis (Sec. 2.5). To distinguish between the forms of excited states, we can apply electric or magnetic fields to the device and watch the excited state lines shift. Given the complexity of this device, an alternative method of studying the excited states is to downscale the size of the SET island to increase the energy level spacing. The effects of downscaling have been studied by Füchsle *et al.* who have fabricated a $7e$ in-plane gated SET using the same technique as that of Fuhrer *et al.*; at this scale the SET can be legitimately called a 'quantum dot' since the geometric confinement of electrons is shorter than their phase coherence length.

Quantum ($7e$) all-epitaxial SET

The quantum dot fabricated by Füchsle *et al.* is shown in Fig. 4.6(a); it consists of 5–6nm wide source and drain leads separated from the dot by tunnel gaps of 9.2–10nm [31]. The dot area is $\sim 4 \times 4nm$, from which Füchsle *et al.* estimated $7e$ on the dot at equilibrium [31]. This was determined from the size of the desorbed hydrogen resist where, by counting the sites visible in the STM image with three adjacent exposed dimers required for incorporation of donors into the substrate [169], we can estimate the number of P atoms likely to incorporate into the substrate. There are two in-plane gates (G1 and G2), separated from the dot by $44nm$ and $57nm$ respectively, where the second in-plane gate is used to increase the effective gate range. The gate G1 is also offset towards the drain, so that it affects the drain barrier more than the source, giving control over the relative tunnel barrier transparency.

Figure 4.6(b) shows the stability plot using gate G1, with G2 left floating [31]. The addition energy of the dot increases as the dot is depopulated, reaching approximately $E_{add} \simeq 50meV$ at $V_{G1} = -800mV$. This is because the single-particle level spacing is sufficiently large at these dimensions to make $E_{add} = E_c + \Delta E$ increase as the electron population is reduced. We can also see excited state lines running parallel to the diamond edges. Füchsle *et al.* published a detailed analysis of the excited state spectrum of this dot in 2011, in which the excited state lines at low drain biases are attributed to valley excited states within the dot, where the sharp wall of the confinement potential ($\sim 1.1eV.nm^{-1}$) causes a splitting of the degenerate Δ-bands within the doped regions. Their numerical

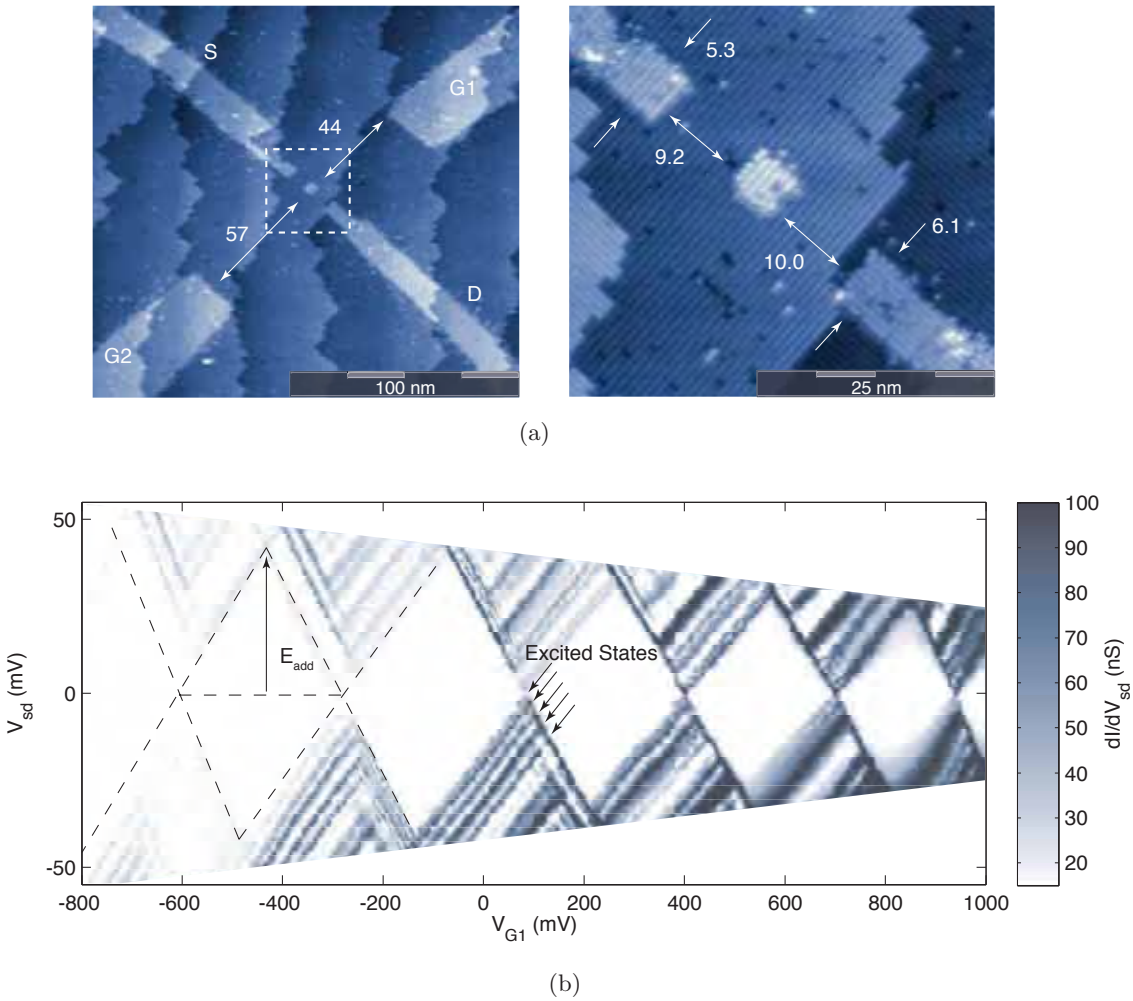


Figure 4.6: Few electron SET fabricated by Füchsle *et al.* [31] with STM lithography. (a) The few-electron SET was made with a cross structure, where current passes from source to drain (upper left to lower right) via thin leads, and two broad gates (G1 and G2) are used to tune the dot potential. (b) The stability diagram using only gate G1 (G2 is floating) shows many excited state lines and diamonds that grow in size as the electron number is reduced.

modelling of this system predicted splitting of the valley-degenerate Δ-states of the same order as the excited state line spacing. The excited state lines seen at high biases (extending to $50meV$) were attributed to the strong lateral confinement of carriers within the leads, giving rise to additional 1-D density of states fluctuations.

Both the quantum dot of Füchsle *et al.* and the SET of Fuhrer *et al.* showed incredible stability, and very low noise. This is attributed to the all-epitaxial in-plane gating scheme, where the substitutional dopants form all the conducting regions of the device and are buried in the silicon substrate using MBE-grown silicon. In this chapter we design a single

Table 4.1: Comparison of occupancy, charging energies and lever arm for few-electron silicon quantum dots.

Type	E_c (meV)	Occupancy (e)	Lever Arm $\alpha = C_g/C_\Sigma$	Ref.
SiGe	1.6	1–30	∼0.10	[161]
	4.0	30–150	0.02	[158]
	4.0	∼25	0.17	[159]
Si-MOS	2.5	10–100	0.20	[26]
	6	1-40	0.21	[164]
Si:P	0.415±0.066	∼600	0.0036	[166]
	3	∼4000±25	0.27	[22]
	25-44	∼7±3	0.07–0.10	[23]

electron transistor at an intermediate scale between that of Füchsle *et al.* and Fuhrer *et al* (a few hundred electrons), which we then use to study the performance of the in-plane gating scheme. There are several reasons for this choice: If the SET is too small then we would see quantisation effects with well defined single particle levels. If the dot is too large we enhance capacitive coupling to everything nearby. Ultimately, to optimise sensitivity to noise and instability of this system we need an intermediate-scale device.

4.2.3 Comparison between silicon quantum dots

Table 4.1 outlines the silicon based SETs we have discussed, extending from the many-electron regime (∼4000e) down to single electron devices. We can clearly see the strong lever-arm $\alpha = 0.2$ offered by the surface-gated Si-MOS devices, which is an indication of the geometric advantage of surface-gating schemes through enhanced capacitive coupling between the gate electrode and the dot. The charging energies quoted for each device is that at equilibrium. The 'charging energy' quoted for Füchsle's device [23] (last line in the table) does however include effects from single-particle level spacing, since these are present in its equilibrium state. We also note that the in-plane gate coupling of Fuhrer's device of $\alpha = 0.27$ is greater than the surface-gating schemes. This is because of the small gate separation used in this device, which also gave a comparatively small gate range. We

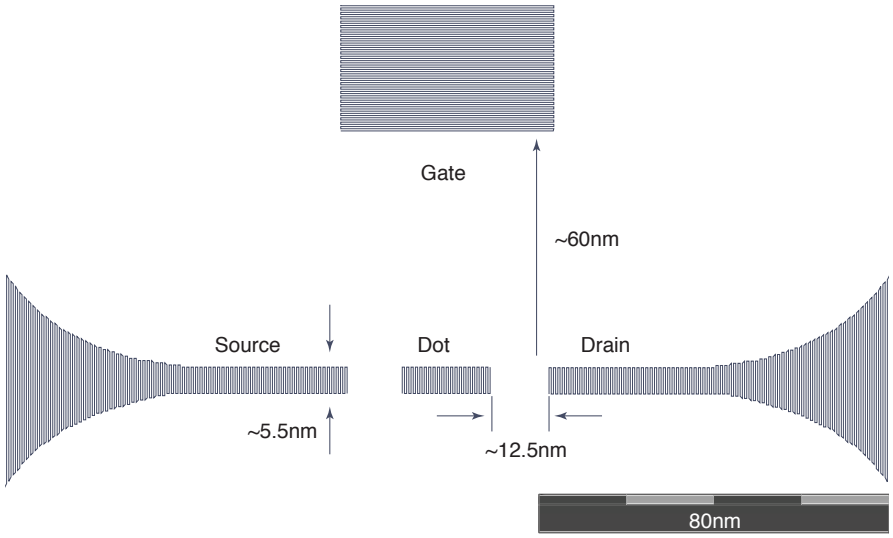


Figure 4.7: STM lithography pattern for the in-plane gated ~200 donor quantum dot in this thesis. This line-diagram shows the raster pattern traced by the STM tip when patterning the in-plane gated dot. The pattern is adjusted as needed on the day to account for the linewidth of the writing process.

discuss this trade-off between gate leakage and capacitive coupling in more detail in the design of the in-plane gated SET presented in the next section.

4.3 Fabricating in-plane gated, STM-patterned SETs

In this section we describe the design and analysis of an intermediate scale in-plane gated SET, used throughout this chapter to assess the performance of the in-plane gating scheme. We first describe the design and numerical modelling processes used, and then describe the fabrication process required to make it. Finally we present electrical transport results from this device and perform a detailed analysis of its stability and noise.

In this section we describe the design of our in-plane gated STM-patterned SET. The purpose of this device is to quantify the stability and noise of the in-plane gating scheme, and ultimately to compare this performance with surface-gated devices. For this reason, we must fabricate a single electron transistor that satisfies the typical usage requirements of STM-patterned SETs, while being sufficiently sensitive to the performance of the gate that it can be used to distinguish between the in-plane and surface gating scheme.

4.3.1 Designing an in-plane gated SET

The STM-patterned devices published by Fuhrer and Füchsle were fabricated using an Omicron variable-temperature STM. The SETs fabricated for this thesis however were made using a custom STM system that incorporates a scanning electron microscope — used to align the STM-patterning with surface gates — and the dedicated UHV oxide chamber developed for this thesis. The complexity of this system affects the resolution of the STM; specifically, the presence of an SEM precludes the use of magnetic damping of the STM stage, increasing the amount of vibration-induced noise in the STM images. Despite these challenges, we have made an in-plane gated SET with a lithographic line edge roughness of a single dimer row, proving that this custom system is capable of fabricating atomically-abrupt devices.

We have chosen to make this device slightly larger than Füchsle's dot to avoid quantisation effects and to account for the patterning tolerance of our custom STM/SEM system. To improve coupling between the in-plane gate and the dot, we have elongated the dot and widened the gate. To simplify the fabrication process greatly, we have also opted to use a single gate, since it is not our intention to deplete the device to the last electron. With these constraints in mind, we have developed the STM lithography pattern shown in Fig. 4.7. This figure shows the exact raster pattern followed by the STM tip while patterning the device (each of the depicted regions is formed by a single line that zig-zags back and forth). While writing, the pattern was scaled as necessary to compensate for the finite line width of the tip. The gate has been placed $60nm$ from the dot, approximately equal to the $57nm$ of gate G2 in Füchsle's dot, to maximise the gate range. The gate leakage current is exponentially sensitive to separation, whereas the capacitance is only proportional, so maximising the gate separation tends to improve the gating range. As we show in the next chapter, this is sufficient to make tunnelling from the gate negligible, with the dominant form of leakage being the breakdown of the substrate at fields beyond $0.2MV.cm^{-1}$. With a gate separation of $60nm$, this corresponds to a gate range of

$$V_g \leq \pm 0.2MV.cm^{-1} \times 60nm = \pm 1.2V \tag{4.4}$$

We have chosen to make the gate broader than that used in Füchsle's dot, since this improves capacitive coupling without any tangible effect on gate leakage — however, this approach offers diminishing returns for gate widths beyond the gate separation, so we have set the width to $60nm$. We tapered the source and drain lead to maintain a minimum separation of $70nm$ to the gate, while maximising the conductivity of the leads. The leads of the SET were designed to be $5.4nm$ wide (7 dimer rows) at their tips to mitigate

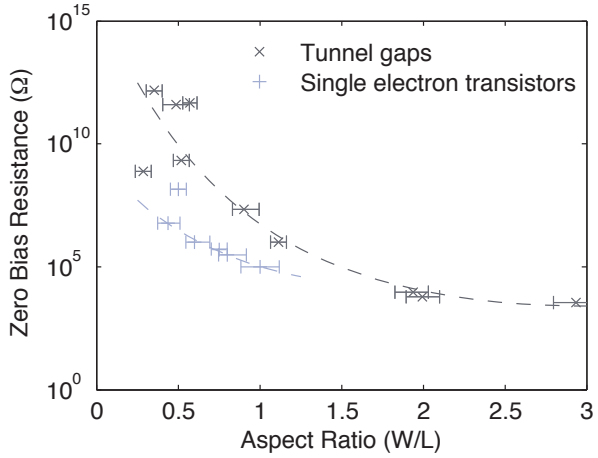


Figure 4.8: Previous studies of resistance versus aspect ratio for tunnel gaps and single electron transistors. This curve shows the relationship between the zero-bias resistance of tunnel gaps with respect to the aspect ratio of the gap from by Pok [168, pg. 83]. We also show data for several STM-patterned SETs made within our group, where we see the resistance is lower than that of tunnel gaps for all aspect ratios.

uncertainty introduced by the line-edge roughness of the patterned area (∼1 dimer row). Using this lead width, the tunnel barriers were designed to be $\sim 12.5nm$ wide, based on the systematic study of STM-patterned tunnel gaps conducted by Pok [168]. From Pok's study this aspect ratio of 0.44 gives a zero-bias resistance on the order of 1–$10G\Omega$ for tunnel gaps [168, pg. 83]; however, empirically we see SETs consistently show lower resistances than tunnel gaps of similar dimensions, as shown in Fig. 4.8. As such, we expect the zero-bias resistance to be on the order of $10M\Omega$.

In summary, we have now designed the basic geometry, the gate width and separation, the lead width and tunnel gap dimensions, and the shape of the source drain leads. Finally, to ensure reasonable capacitive coupling to the gate, we have designed the dot to be $\sim 20nm$ long, giving a dot area of $108nm^2$, which corresponds to a maximum of $250e$ on the dot (when multiplied by the measured sheet density of Hall bar calibration samples [66]). The number of electrons on the dot is not vital for this experiment, except to ensure that the device is representative of those actually used for charge sensing applications. This device is indeed very similar to an SET currently being used as a charge sensor in an ongoing program within our group to make a coupled SET/single-donor system for measurement of the electron spin relaxation time, T_1 [170]. Having designed our SET, now we describe the process used to fabricate it.

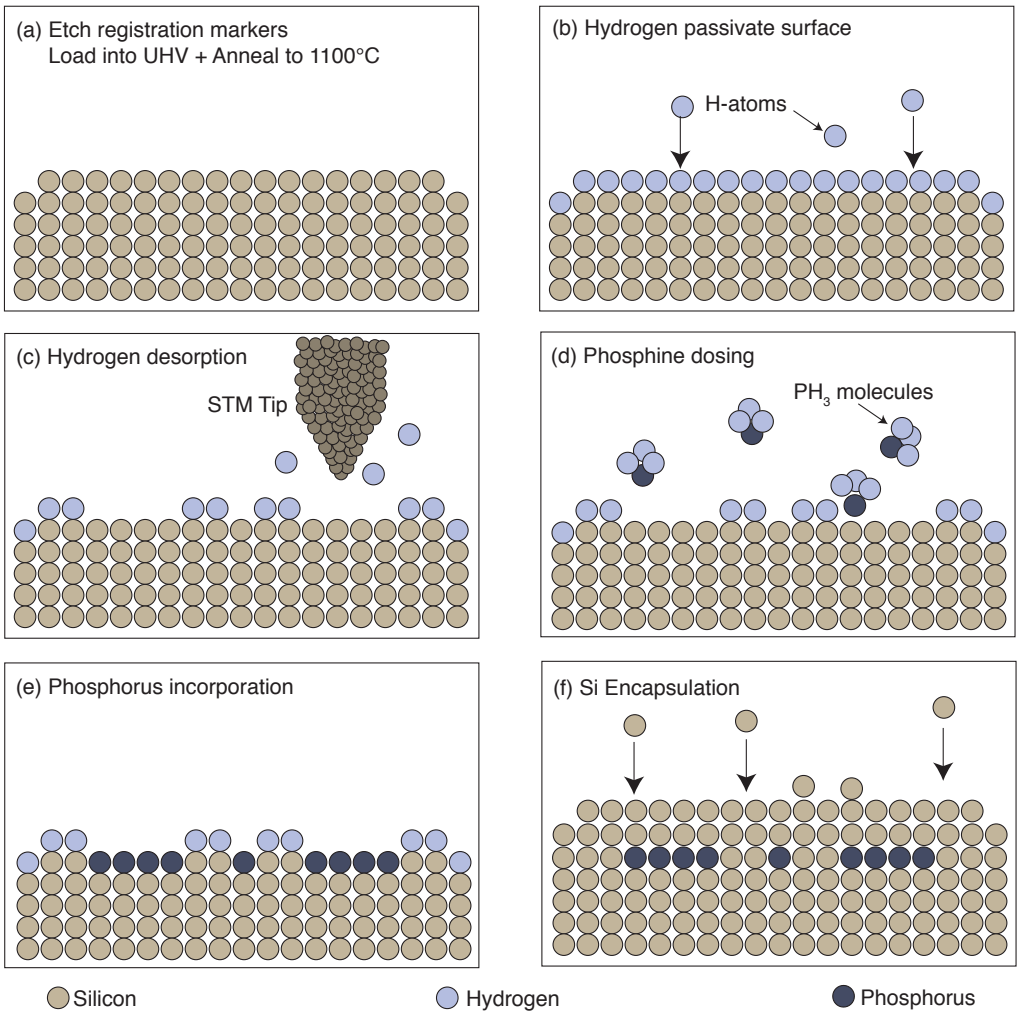


Figure 4.9: Fabricating precision planar single electron transistors with STM lithography. (a) Registration markers are etched, and the sample is flash-annealed. (b) The bare silicon surface is exposed to a flux of atomic hydrogen, used as a resist. (c) The STM tip is used to desorb hydrogen. (d) The sample is dosed with phosphine gas, which adsorbs to the reactive silicon surface. (e) The sample is annealed to incorporate the phosphorus dopants into the lattice. (f) The STM patterned dopants are then encapsulated with epitaxial silicon by MBE.

4.3.2 STM-fabrication scheme

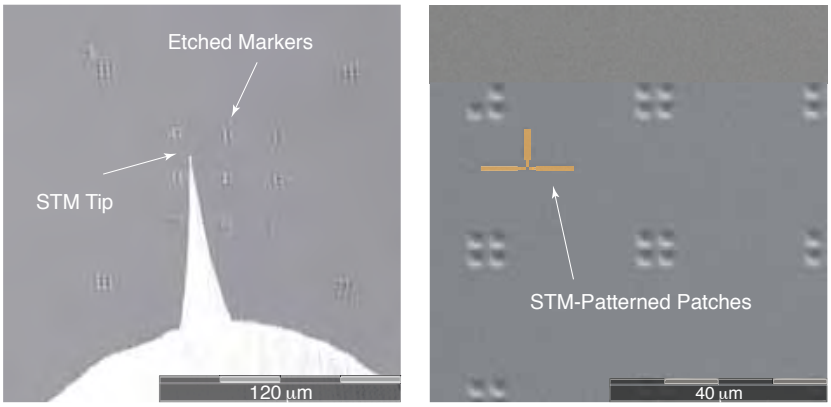
The STM fabrication scheme developed within our group is illustrated in Fig. 4.9. In this section, we describe the fabrication scheme used to fabricate the in-plane gated device for this chapter.

Alignment markers

The STM fabrication scheme outlined in Fig. 4.9 begins by patterning alignment markers into the silicon substrate to align each of the lithographic steps, shown in Fig. 4.9(a). The UHV surface preparation technique used to form atomically-flat terraces for STM-lithography requires heating the sample to extreme temperatures ($>1100°C$, as described in the next section and in Ref. [171]); this precludes the use of alignment markers in a field oxide layer, as used in some traditional semiconductor processes, since silicon dioxide evaporates from the silicon surface at temperatures above $600°C$ in a vacuum of $< 10^{-10}mbar$ [172]. Metallic alignment markers have been used in more contemporary processes but they are incompatible with our system because they contaminate the silicon surface during the surface preparation — preventing the sample from developing the desired (2×1) surface reconstruction. The solution developed within our group by Rueß *et al.* [20] was to etch alignment markers into the substrate itself, which does not contaminate the sample. Since the markers are formed by the substrate, they survive the high temperature anneal. However, as the surface reconstructs it smoothes out the etched markers, limiting the alignment accuracy of this scheme to $\sim 100nm$. The patterning is performed by writing the desired marker shape onto a $50nm$ thermally grown oxide on the sample surface using EBL, which is then etched with a $90s$ emersion in buffered hydrofluoric acid (15:1 NH_4F (40%w/w):HF (49%w/w)), and $\sim 3hrs$ in tetra-methyl ammonium hydroxide (20% TMAH). The oxide is then removed with a buffered hydrofluoric acid etch. After etching alignment markers into the substrate, the wafer is chemically cleaned (see App. A), and loaded into the ultra-high vacuum environment where the surface is prepared for STM-patterning.

Surface preparation

The UHV surface preparation technique consist of a series of anneals designed to achieve atomically-flat terraces [171]. In this process, adsorbates are baked from the sample for $\sim 12hrs$ at $400°C$ in ultra-high vacuum ($p_{base} \simeq 5 \times 10^{-11}mbar$), after which the sample is ramped rapidly over $<30s$ to $1100°C$, where it is held for $1min$ before ramping back to $400°C$. This anneal is then repeated for $5s$, after which the sample is cooled slowly from $900°C$ at $1°C.s^{-1}$ down to $280°C$. This anneal process sublimates the native silicon oxide from the sample surface, removing SiC from the surface [173, pg. 64] and leaving a flat and relatively defect free surface [171]. The second $5s$ anneal and slow cool-down are used to let the silicon surface atoms move freely to form smooth, defect free terraces of silicon on the surface with a (2×1) reconstruction.



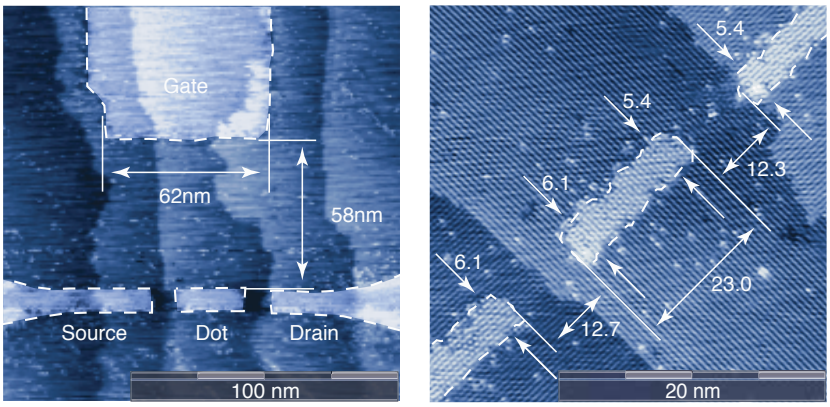
(a) (b)

Figure 4.10: Locating the STM-patterned device with the SEM. (a) In this image we show the etched registration markers used to find the STM-patterned device, where we record the location of the STM tip at the beginning and end of each contact patch (the tip is the sharp bright protrusion coming from the bottom of the image) (b) By comparing images at the end of the patterning process, we can outline the location of the STM-patterned contact patches, which we then use to align evaporated surface aluminium contacts.

When the sample temperature stabilises at $280°C$, it is exposed to a flux of atomic hydrogen at a pressure of $5 \times 10^{-7} mbar$ for $6min$, corresponding to a dose of over 100 Langmuirs, which passivates the surface with a monolayer of hydrogen. The atomic hydrogen flux is generated by passing molecular hydrogen over a hot ($1400°C$) filament. The sample temperature used during this step is optimised to give complete passivation of the surface, where exactly one hydrogen atom is bound to each silicon surface atom. If the sample temperature is too low during the hydrogen passivation, the atomic hydrogen flux can actually etch the silicon surface [174]. If the sample temperature is too high, the hydrogen begins to desorb from the surface [175]. After the sample is terminated with a monolayer of hydrogen, it is transferred to the analysis chamber for patterning.

STM-lithography

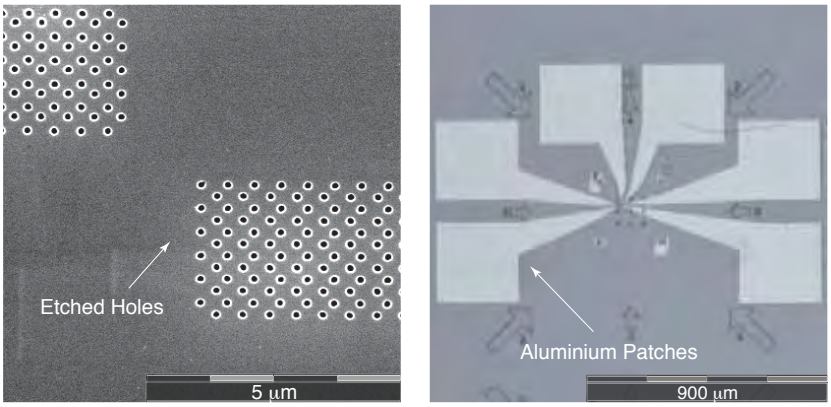
The use of an STM tip to desorb regions of hydrogen from a silicon (100) surface was first demonstrated by Lyding *et al.* in 1994 [174]. Since then, our group has refined the STM lithography scheme over many years [20, 21, 58]. To perform STM lithography, the STM tip is positioned at the outer edge of one of the four square regions demarcated by the central nine etched alignment markers, using the SEM to monitor the tip location, as shown in Fig. 4.10(a). The tip is then brought into tunnelling contact with the sample and conditioned by holding the tip-sample current constant ($\sim 800pA$) while pulsing the



(a) (b)

Figure 4.11: STM images of the in-plane gated quantum dot. (a) The large scale STM image of the device immediately after patterning (this is a $150 \times 150nm$ frame) showing the final gate separation and width of $58nm$ and $62nm$, respectively; only $2nm$ from the targeted dimensions. (b) Using the STM we can see the device with dimer-row resolution, where the dimer rows are separated by $0.768nm$, which we can use to calibrate the scale of both this image and that in (a). The line edge roughness of the device is less than one dimer row.

tip voltage ($-10V \leq V_{tip} \leq 10V$). Once satisfied with the stability and resolution of the tip for both writing and imaging, the tip is moved to the centre of the alignment markers, where the precise location of the tip is noted relative to the markers using the SEM. The tip is then re-engaged and the surface is imaged with the tip to ensure that the surface is completely saturated with hydrogen and free of defects. After this, the device is patterned into the hydrogen resist by passing a pre-defined pattern file to the STM control software, which rasters the pattern across the surface using a large tunnelling current (3–$15nA$), at slightly higher biases than used while imaging (3–$6V$) at a tip speed of less than $100nm.s^{-1}$. Under these conditions, the hydrogen desorbs from the surface primarily via multi-vibrational excitations that break the Si–H bonds by inelastic tunnelling from the tip [176], which gives the greatest patterning precision. An STM image of the pattern in the hydrogen resist is shown in Fig. 4.11. Once satisfied with the STM-patterning of the active device region, the source, drain, and gate electrodes are extended out into large area contact patches ($800nm \times 3000nm$), which are required to make contact to the device using EBL-defined metallic electrodes, as indicated with the orange overlay in Fig. 4.10(b). At this stage, we typically use lower currents and higher voltages (3–$6nA$, 6–$8V$), so that hydrogen depassivation occurs via field emission; this allows us to draw the tip further from the surface so that the desorption process is less affected by mechanical vibrations and we can speed the tip raster speed to $800nm.s^{-1}$.



(a) (b)

Figure 4.12: Making electrical contact to the STM-patterned devices (a) Using EBL and reactive ion etching, we define small ($\sim 200nm$) holes in the silicon to perforate the STM-patterned contact patches, giving better contact between the STM-patterned device and the metallic leads. (b) Using EBL and a lift-off process, we deposit aluminium contacts over the etched holes to contact the device.

Doping and encapsulating

After patterning, the sample is exposed to phosphine gas at a pressure of $1.1 \times 10^{-9} mbar$ for $30min$, which adsorbs to the exposed silicon regions defined with the STM tip with a sticking coefficient of ~ 1 [177]. After the phosphine dosing process, the phosphorus atoms from the PH_3 molecules are incorporated into the sample using a short anneal ($1min$ at $350°C$). During this process the phosphorus atom moves into the substrate to occupy a substitutional lattice site [178].

The presence of the hydrogen resist on the surface during this anneal prevents lateral diffusion of the dopants across the surface, and since it is energetically favourable for the dopants to sit at the surface rather than in the bulk, little diffusion occurs into the substrate itself [179]. The sample is then encapsulated with MBE-grown silicon using a silicon flux from a silicon sublimation source, which deposits silicon at a rate of $\sim 0.1nm/min$ for $3hrs$, forming a 20–$25nm$ layer of silicon over the device. During this growth, the sample is held at a temperature of $250°C$ which gives the best compromise between the highest crystallinity of the MBE grown silicon with the lowest segregation of the patterned dopants [35].

Depositing metallic source, drain, and gate electrodes

The sample is then removed from UHV and electrically contacted in a clean room. All cleanroom processing was performed in the Semiconductor Nanofabrication Facility, at the

University of New South Wales. This facility has a class AS 3.5 cleanroom (equivalent to ISO class 5). The specific parameters used for all cleanroom processing are outlined in App. A. All patterning performed in the cleanroom was conducted using electron beam lithography (EBL), where an FEI XL30 scanning electron microscope was used to write the pattern into the resist under the control of the Nanometer Pattern Generator System (NPGS) software program by JC Nabity Lithography Systems.

To contact the devices, we first pattern the intended contact regions with a mesh of $200nm$ diameter holes using EBL, as shown in Fig. 4.12(a). These contact holes are then etched into the silicon substrate using a custom-built reactive ion etching system (RIE) using a mixture of CHF_3 and CF_4 gases (each set to a flow rate of 10sccm with a mass flow controller) at a chamber pressure of $14Pa$ for $5min$. This process perforates the STM-patterned contact patches with $200nm$ diameter holes that are 55–$75nm$ deep, which gives good areal contact between the metallic electrodes and the phosphorus-doped silicon [31].

Aluminium source and drain electrodes are then patterned with EBL, overlapping with the perforated STM-defined patches, as shown in Fig. 4.12(b). Before depositing the contact metal, we perform a $2min$ ash of the resist in a Denton PE-250 oxygen plasma asher, to remove any residual resist from the patterned areas, and then do a $10s$ chemical etch in hydrofluoric acid (49%HFw/w diluted 10:1 with deionised water), to remove any native oxide on the silicon. After this, we deposit $\sim 80nm$ thick aluminium contacts using a Kurt J. Lesker thermal evaporator at a pressure of $5 \times 10^{-6} Torr$, lifting off the unwanted metal by immersing the sample in 1-methyl-2-pyrrolidone (NMP) for several hours, then rinsing the samples with acetone and isopropanol.

For the devices presented in this thesis, no post-metallisation anneal was performed. After depositing the metallic leads — which terminate in large-area bond pads — the device is cleaved and glued to an IC package using polymethyl-methacrylate, and the bond pads are bonded to pins on the IC package using a Karl Suss semi-automatic aluminium wedge bonder.

4.3.3 Electrical transport properties of the in-plane gated SET

Measurement setup

All devices presented in this thesis were initially characterised at $4.2K$ to check that the device contact resistance was acceptable ($< 100k\Omega$) and that the device behaved as expected before spending time to load it into the dilution refrigerator. The measurements

at $4.2K$ were conducted by immersing the sample into a dewar of liquid helium using a custom dipping stick, where the sample is placed in a 20 pin package at the lower end of the stick, which is immersed in the helium dewar, and electrical contact to these pins are accessible outside of the dewar from a breakout box at the top end of the dipping stick. This rig is equipped with a $2T$ superconducting magnet to apply a magnetic field perpendicular to the sample for magnetic field dependent measurements.

The majority of the milli-Kelvin measurements presented in this thesis were performed on a Kelvinox K100 $^3He/^4He$ dilution refrigerator made by Oxford Instruments, located within our research centre. The Kelvinox dilution refrigerator is housed in a copper shielded room, where all power passing into this room is filtered, and the instrument communications are passed into the room using an optical isolator. The noise measurements presented in the next section were recorded on an American Magnetics dilution refrigerator at the Indian Institute of Science. All electrical measurements of the samples using an AC bias were conducted using Stanford Research System SR830 lock-in amplifiers for both sourcing and sensing the device current. All DC measurements were conducted using Yokogawa 7651 DC sources to apply gate and drain voltages, where the source-drain current was sensed using a DL Instruments 1211 current preamplifier with a gain of 10^7 to $10^9 V/A$, connected to a HP 34401A digital multimeter. The devices were connected to the instrumentation via BNC cables, with in-line $1M$–$100nF$–$1M$ RC filters used on the gate leads, and $1.7k\Omega$–$100nF$–$1.7k\Omega$ RC filters on the drain lead. All instruments were linked via the GPIB interface to a desktop computer running LabVIEW routines to acquire the data.

Transport measurements of the in-plane gated device

The gate leakage of our device (with a $58nm$ gate separation) is shown in Fig. 4.13, juxtaposed with a comparable trace from the 4000 donor dot (with a 36nm separation) by Fuhrer [22]. The bias voltage was applied to the gate with both the source and drain contacts grounded. The measured current shows a sharp increase at $\pm 1.5V$, consistent with breakdown of the silicon substrate. The leakage of the plunger gate from the 4000 donor SET of Fuhrer *et al* shows a much smaller range of $\pm 0.4V$, as expected from the narrower gate-dot separation. Since breakdown dominates the leakage of our device (as we show in the next chapter), there would have been no benefit in patterning the gate further from the dot, since the gate field can never exceed the breakdown field strength of silicon.

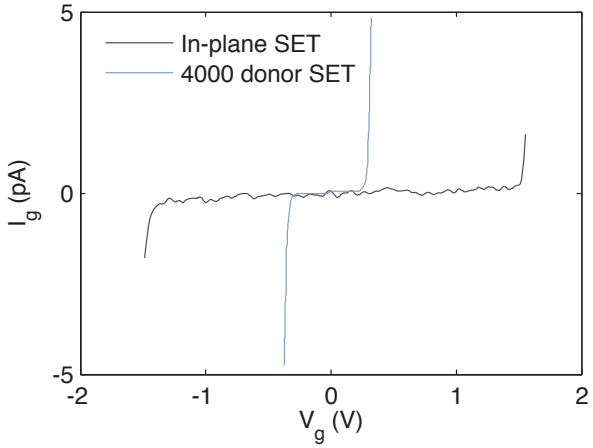
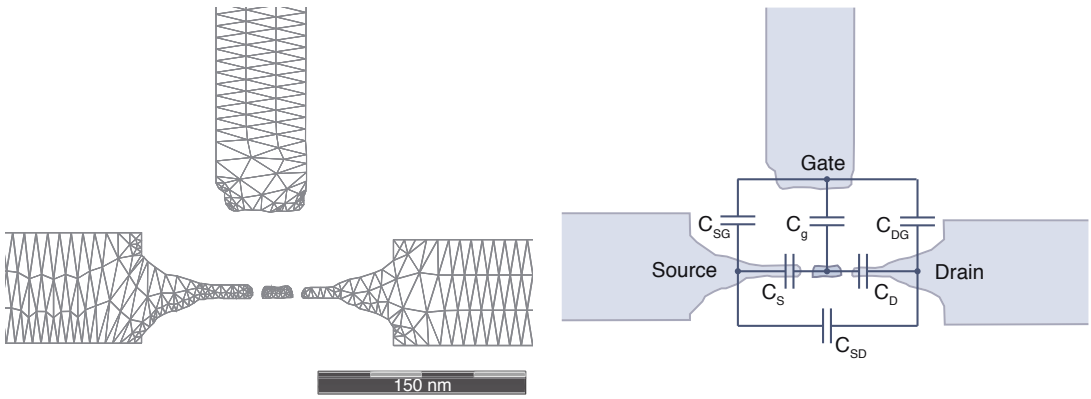


Figure 4.13: Comparison of the in-plane gate leakage for the ∼200 donor dot and the 4000 donor dot. The in-plane gate does not begin to leak until $V_g = \pm 1.5V$, at which point the current turns on abruptly. For comparison, we show the in-plane gate leakage of Fuhrer's plunger gate, which leaks much sooner because it is closer to the dot ($36nm$ vs $58nm$).



(a) (b)

Figure 4.14: Wireframe model of in-plane gated device for capacitance modelling. (a) Using the STM image shown in Fig. 4.11(a) and the scale calibration in Fig. 4.11(b), we have extracted the precise geometry of the STM-patterned area (we also include the large STM-patterned contact patches, whose inner edges are visible in this figure). We use this geometry to form a wireframe for finite element analysis capacitance modelling. (b) The capacitance between STM patterned regions can be approximated by lumped capacitances, as labelled in the figure.

From Fig. 4.11, the approximate area of the dot (SET island) is

$$A = 23 \times 5.5nm = 126nm^2. \tag{4.5}$$

If we assume the same carrier density as measured from Hall bar control samples ($\sim 1.5 \times 10^{14} cm^2$ [66]), this implies a total number of electrons on the dot at equilibrium of

$$\begin{aligned} N &= A \times n_s \\ &= 126 \times 10^{-18} \times (1.5) \times 10^{18} \\ &= 189. \end{aligned} \tag{4.6}$$

Where A is the dot area and n_s is the sheet density of dopants. However, statistical studies of phosphorus incorporation within small lithographically-defined regions show lower levels of doping than for large scale Hall bars [31]; we can therefore safely estimate an upper limit of 200 electrons on the dot at equilibrium.

Figure 4.14(a) shows a wireframe model of the dot, constructed from the STM image shown in Fig. 4.11. We use this wireframe to calculate the expected capacitive coupling between the various elements of the dot using the program FastCap [180]. We have dilated the STM patterned area by $\sim 2nm$ to account for the Bohr radius of the dopants. Similarly, the vertical thickness of the δ-layer is modelled as $2nm$, in accordance with the modelling of Carter *et al.* [33]. Given that the STM-patterned regions are highly degenerately doped, we model them as metals. The intervening regions of silicon are doped below the metal-insulator transition, and so become insulating at measurement temperatures ($\sim 150mK$–$4.2K$). For this reason, we treat the silicon lattice as a perfect insulator with a dielectric constant of $\epsilon_r = 11.9$ (bulk silicon). The effect of the insulating substrate can be modelled as lumped capacitances between the patterned dopant regions, as illustrated in Fig. 4.14(b). The source, drain, and gate leads are all connected externally to either DC sources or ground, so we can neglect the effect of the capacitive coupling between them. Here we focus on the capacitive coupling between each lead and the dot. From the device geometry shown in the wireframe model and the silicon dielectric constant, we can model the expected capacitance between each lead and the dot using the finite element analysis fast field solver, FastCap [180]. The results of this simulation are shown in Table 4.2. The symbol C_Σ corresponds to the 'sum capacitance' of the device — literally the sum of all capacitances terminating at the dot. The source-dot and drain-dot capacitances (C_S and C_D, respectively) are equal, and together dominate the sum capacitance of the device ($C_S + C_D = 8.2aF$). As expected intuitively, the gate capacitance is smaller than that of

Table 4.2: Capacitance between degenerately doped regions of the in-plane gated SET. The capacitance values are presented in units of atto Farads. The device was modelled as metallic conductors in a dielectric substrate with a dielectric constant of $\epsilon_r = 11.9$. The conducting regions were modelled as $2nm$ thick to account for the Bohr radius of electrons around the phosphorus donors.

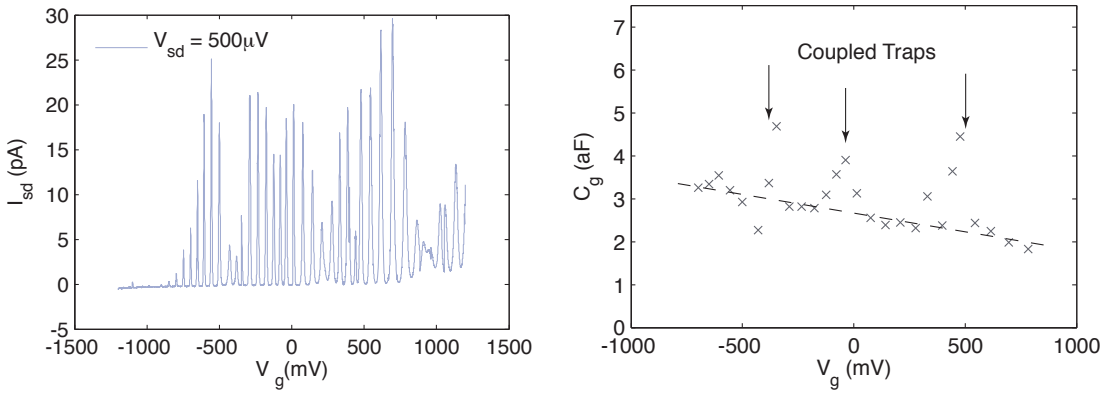
(aF)	C_Σ	C_D	C_g	C_S
Simulation	11.8	4.1	1.7	4.1
Experiment	11.8	4.7	2.4	4.7

the source and drain, because the gate lead is ∼5.5 times further away; this is compensated by the greater size of the gate electrode, making the gate capacitance 40% of the source and drain capacitances. Note that here, the values C_D, C_S, and C_g do not sum to C_Σ, since FastCap also solves for the capacitive coupling of the dot to the ground plane. We can use these modelling results to calculate the expected response of the dot under an applied gate and drain bias. In the following discussion we rely heavily on the equations found in the theory section of this thesis (Sec. 2.5). A sum capacitance of $C_\Sigma = 11.8aF$ implies a charging energy of

$$\begin{aligned} E_c &= \frac{e^2}{C_\Sigma} \\ &= \frac{e^2}{11.8aF} \\ &= 13.6meV \end{aligned} \tag{4.7}$$

This quantity defines the required change in the dot potential to add another electron to the dot, which we can apply to the dot using the gate. Any change in the gate potential is coupled to the dot by a proportion determined by the capacitor divider rule, from which we can expect the gate to add or remove an electron from the dot every time the gate potential changes by

$$\begin{aligned} \Delta V_{gate} &= \frac{C_\Sigma}{C_g} E_c/e \\ \Delta V_{gate} &= \frac{11.8aF}{1.7aF} \times 13.6mV \\ &= 94.4mV \end{aligned} \tag{4.8}$$



(a) (b)

Figure 4.15: Coulomb blockade oscillations using the in-plane gate at 4K. (a) The Coulomb blockade sweep at $4K$ shows clear, distinct blockade peaks that vary slowly in height and width. (b) The separation between successive peaks of the CB sweep gives the capacitance of the dot for that transistion, which decreases with gate voltage, indicating that the dot is dilating. There are three peaks in this trend, which we attribute to coupled traps, discussed in the next section.

Accordingly, with a gate range of $\pm 1.2V$, we can expect to tune the number of electrons on the dot by

$$N = \frac{\pm 1200mV}{94.4mV} = \pm 13. \tag{4.9}$$

In this way we can expect that, with a small source-drain bias ($V_{sd} \ll E_c/e = 13.6mV$), the conductance of the device should be virtually zero (blockaded) except at discrete points spaced $\sim 95mV$ apart in gate voltage. Figure 4.15(a) shows a plot of the source-drain current with a drain bias of $400\mu V$, recorded by sweeping the gate potential with the sample at a temperature of $4.2K$. This trace clearly shows regions of Coulomb blockade separating sharp peaks in the current; however there are already 15 peaks within a gate range of $0 \leq V_g \leq 1V$. This implies a peak spacing of $\sim 67mV$. Compared with the expected peak space of $94.4mV$, this gives a gate capacitance of

$$\begin{aligned} C_g &= \frac{\Delta Q_d}{\Delta V_g} \\ &= \frac{15e}{1.0V} \\ &= 2.4aF \end{aligned} \tag{4.10}$$

The measured peaks are broad towards the positive gate bias limit, reducing in both width and height as we progress towards negative gate biases. This is consistent with the gate altering the potential profile of the tunnel barriers that isolate the dot from the source

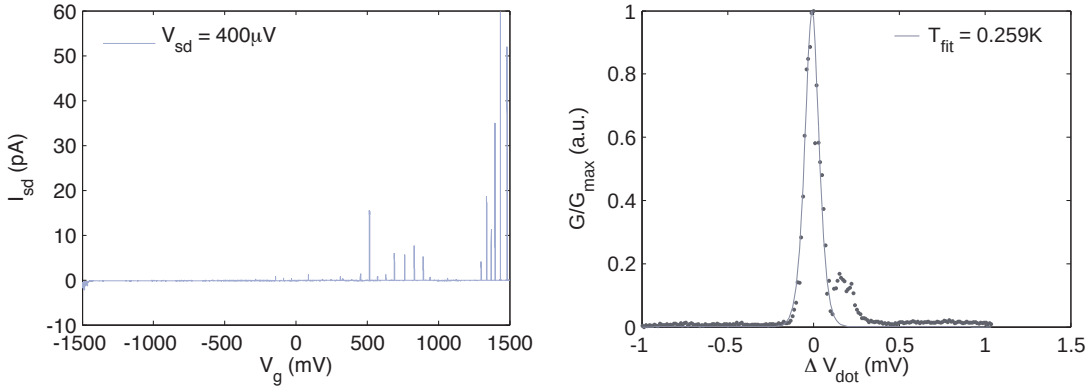


Figure 4.16: Coulomb blockade oscilations using the in-plane gate at base temperature. (a) As we cool the sample to base temperature, the CB peaks become significantly sharper and smaller. The peak height varies by more than that expected with temperature indicating that the tunnel barrier heights also change with temperature. (b) Fitting the CB peak centred at $V_g = 691.4mV$ with the theoretical thermally-broadened relationship (see [150]), gives an electron temperature of $259mK$.

and drain leads; specifically, the tunnel barriers are pulled up as we take the gate to more negative biases. The small height of these tunnel barriers ($\sim$100meV [33, 168]) means that any minor variations in the barrier potential are likely to have a large effect on the device current. As a consequence of this change in the barrier profile with gate bias, we must be careful about calculating the gate capacitance from the number of peaks over a given range, since the gate also influences the confinement geometry of the dot. From Fig. 4.15(b), when we calculate the capacitance purely from the spacing between successive peaks, we see the capacitance clearly reduces with increasing positive gate voltage, as expected when the barriers become shallower. There are also some distinct aberrations in this capacitance trace, which we attribute to switching of the dot potential under the action of nearby capacitively coupled traps — we discuss this phenomenon in greater detail later in this chapter.

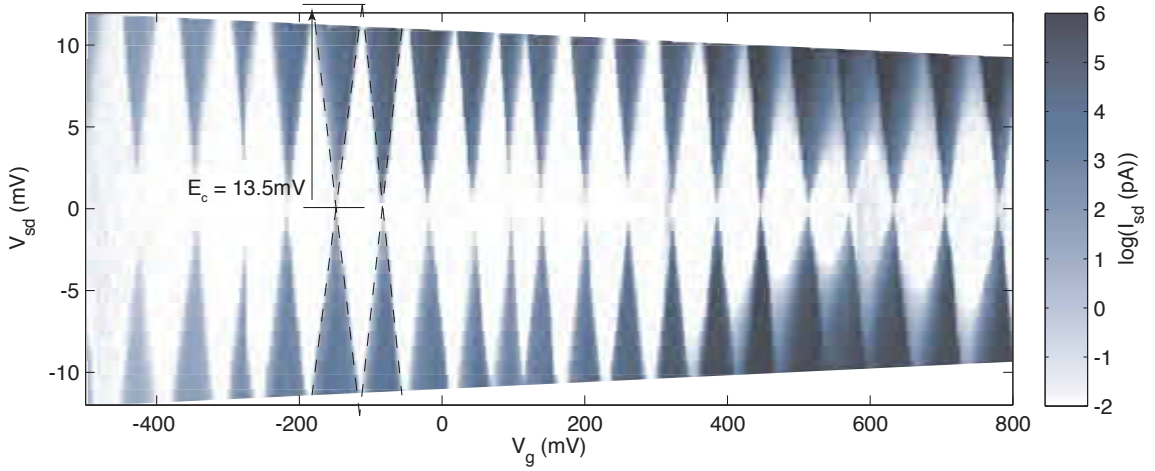
Figure 4.16(a) shows the same sweep as Fig. 4.15(a), but taken at the base temperature of a dilution refrigerator. The peaks become narrower at this temperature and the height of each peak is reduced significantly. This narrowing of the peaks reflects a reduction in the thermal energy of carriers within the dot. The decrease in the peak magnitude is indicative of a change in the transparency of the tunnel barriers, which is expected as temperature-dependent band bending of the tunnel barriers becomes sharper. Figure 4.16(b) shows a close-up view of the plot in Fig. 4.16(a), centred around $V_g = 691.4mV$. The trace shows a central peak with a strong side-lobe that is caused by a coupled trap, to be discussed

in detail later in this chapter. The central peak has a finite width that is commensurate with an electron temperature of $T \simeq 259mK$ using the fitting formula [150]

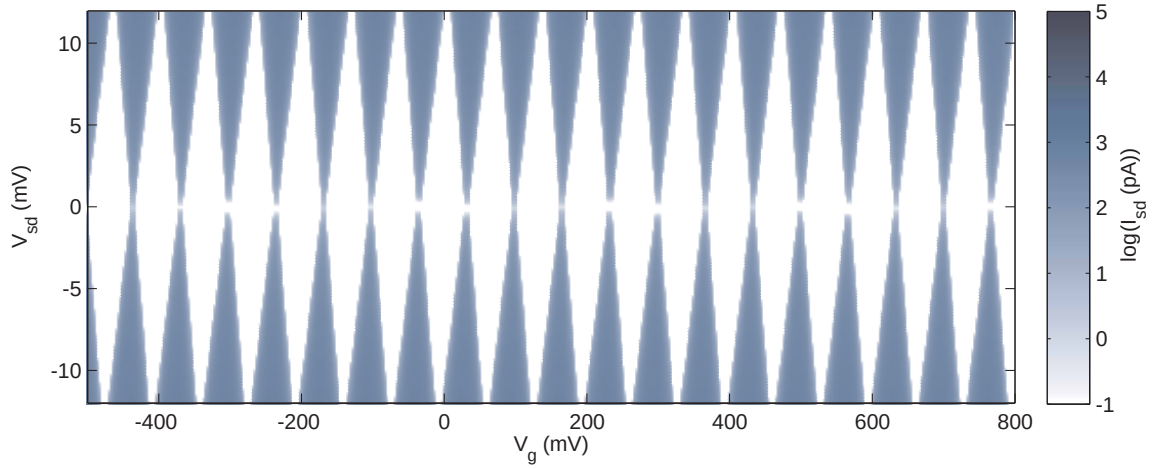
$$\frac{I_{sd}(\delta)}{I_{sd_{peak}}} = \frac{\delta/k_BT}{sinh(\delta/k_BT)} \tag{4.11}$$

where $\delta = \frac{eC_g}{C_\Sigma}\left(V_g - V_{g_{peak}}\right)$ is the deviation in the dot potential μ_d from the resonance condition induced by the change in gate voltage $\left(V_g - V_{g_{peak}}\right)$, and $I_{sd_{peak}}$, $V_{g_{peak}}$ are the current and gate voltage at the Coulomb blockade peak, respectively. This electron temperature of $259mK$ is consistent with the results of Füchsle, who measured an electron temperature of $260mK$ on this dilution refrigerator [31]. However, because of the strong non-linearity of the tunnel gaps, we had to apply a drain bias of $V_{sd} = 400\mu V$ to see an appreciable current, which is greater than the thermal energy, and is therefore likely to contribute to the peak width.

Figure 4.17 shows a 2-D map of the device current as a function of the source-drain and gate voltages. The measured current is shown on a log scale to reveal the faint current passing through the device near $V_g = -400mV$, which is around three orders of magnitude lower than that at $V_g = 800mV$ due to the tunnel barriers becoming more opaque under the action of the gate. Below the measured stability plot, we show the theoretical (classical) conductance through the dot, simulated using the single electron simulation software SIMON [181] using values of $C_D = C_S = 4.1aF$ and $C_g = 2.4aF$, extracted from the experimental stability diagram. When we compare the measured and simulated results, we see that there is a variation in the size of the Coulomb diamonds within the measured data that is not present in the simulation, and furthermore that the measured diamonds do not close — that is, there is zero conduction at $V_{sd} = 0$. We attribute both effects to capacitive and tunnel-coupled traps, which we address explicitly in the next section. From the measured stability plot, we find the charging energy is approximately $E_c = 13.5meV$, which gives a sum capacitance of $C_\Sigma = e/13.5meV = 11.8aF$. Since the diamonds are approximately symmetric in the V_{sd} axis, we can say $C_S \simeq C_D$; therefore, using the measured value for the gate capacitance $C_g = 2.4aF$, we have $C_S \simeq C_D = (C_\Sigma - C_g)/2 = 4.7aF$. We compare the modelled and experimental capacitances in Table 4.2. As previously noted, the FastCap model makes different assumptions about the sum capacitance of the dot — specifically the contribution of the dot capacitance from the ground plane — and so the numbers do not match perfectly. However, the values are generally in good agreement, indicating that the patterned device behaves as designed. This confirms our understanding of the critical device parameters and allows us to predictably pattern quantum dots of known E_c and α.



(a) Measurement



(b) Simulation

Figure 4.17: Experimental and theoretical stability diagrams at base temperature. (a) The stability diagram of the in-plane gated device shows that the majority of diamonds have a charging energy of 12–13.5meV. Smaller diamonds observed are attributed to compression of the blockaded region due to the population of nearby traps as the gate is swept. (b) We have modelled the expected stability diagram of the device using the program SIMON [181]. This program only accounts for classical charging effects, not excited states within the dot or leads, but provides a very good match to the experimental data.

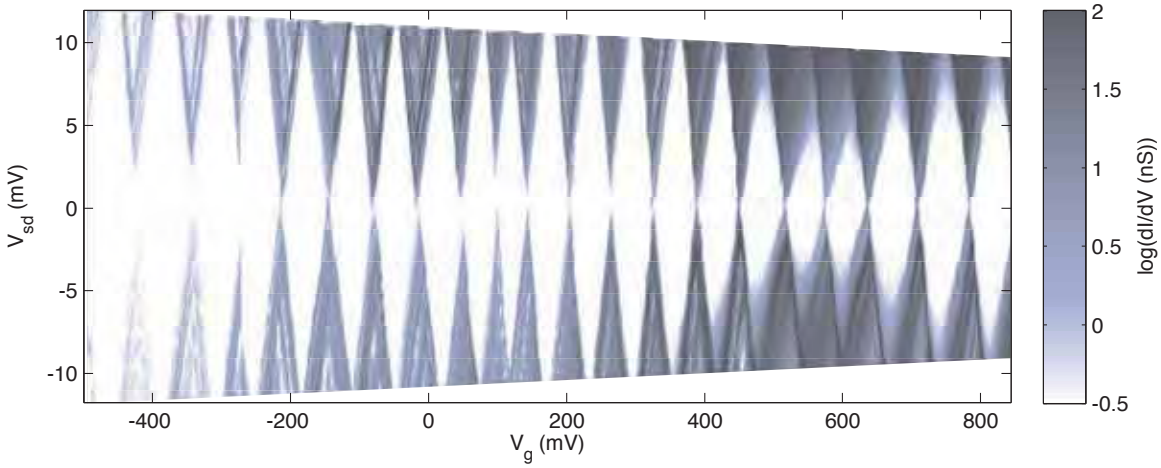


Figure 4.18: Excited states of the in-plane gated SET. The differential conductance of the stability diagram makes it much easier to observe the excited states.

We can also see fine structure in the measured stability plot, which is easier to see when we calculate the differential conductance of the device (dI/dV_{sd}). This is shown in Fig. 4.18 for the large-scale stability plot shown in Fig. 4.17(a). As with the SETs of Fuhrer and Füchsle [22, 23], we attribute the fine structure observed to excited states within the dot and 1-D leads. In the next section, we describe the appearance of resonant features in the excited state spectrum consistent with a tunnel-coupled trap, which also neatly explains why our Coulomb blockade diamonds do not close.

4.4 Coupling between traps and STM-patterned SETs

4.4.1 Shifting of the Coulomb diamonds

A variety of mechanisms cause resonant features in the differential conductance of an SET; many of which were discussed in the review by Escott *et al.* [48]. Included among these, Escott briefly describes the effect of tunnel-coupled traps, which causes both resonant features and an 'opening' of the Coulomb blockade diamonds, where no conduction is seen at zero source-drain bias. In this section we describe the effect of tunnel coupled traps based largely on the work of Pierre *et al.* [182]. First let us consider the most simplistic case of a trap capacitively coupled to an SET.

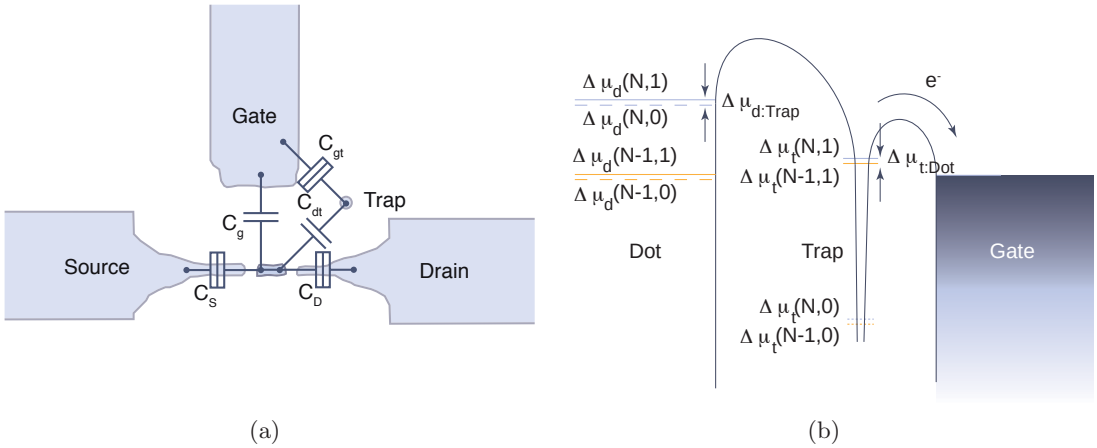


Figure 4.19: Switches in the dot potential from capacitive coupling to traps. (a) Here we model switches as traps capacitively coupled to the dot and tunnel coupled to the gate, with no interaction from the source and drain. (b) The splitting of the dot and trap energy levels occurs via capacitive back-action between the dot and trap.

Capacitive coupling between traps and an SET

A trap near to an SET will cause a sudden switch in the dot potential ($\Delta\mu_{d:Trap}$) as the trap populates or depopulates. This is a consequence of the capacitive coupling between the trap and dot (C_{dt}, see Fig. 4.19(a)), according to the relation [182]

$$\Delta\mu_{d:Trap} = \frac{e^2}{C_t}\frac{C_{dt}}{C_\Sigma} \tag{4.12}$$

where C_t is the self-capacitance of the trap. Populating the trap with an electron *increases* the dot energy level, since electrons on the dot are repelled by the trapped electron. Equally, a change in the occupancy of the dot increases the trap potential by $\Delta\mu_{t:Dot} = \Delta\mu_{d:Trap}$, which is to say, the back-action affects the dot and trap equally. The modification of the trap and dot levels caused by their coupling is shown in Fig. 4.19(b). Filling the trap increases the dot level from $\mu_d(N,0)$ to $\mu_d(N,1)$, where the separation between these two states is given by $\Delta\mu_{d:Trap}$ in Eq. 4.12. If the gate potential is swept so that at some gate voltage it is energetically favourable for the trap to fill, the change in occupancy of the trap causes a sudden shift of the Coulomb diamonds, as shown in Fig. 4.20(a), where the diamond translates discontinuously in the V_g axis at the point demarcated by an orange line. In more complex cases the trap may be tunnel-coupled to the gate, so that electrons tunnel freely between the gate and trap. In this tunnel-coupled state, the trap is able to constantly empty and fill, continually switching the dot potential back and forth by $\Delta\mu_{d:Trap}$. This continual switching in the dot potential has the effect of doubling all

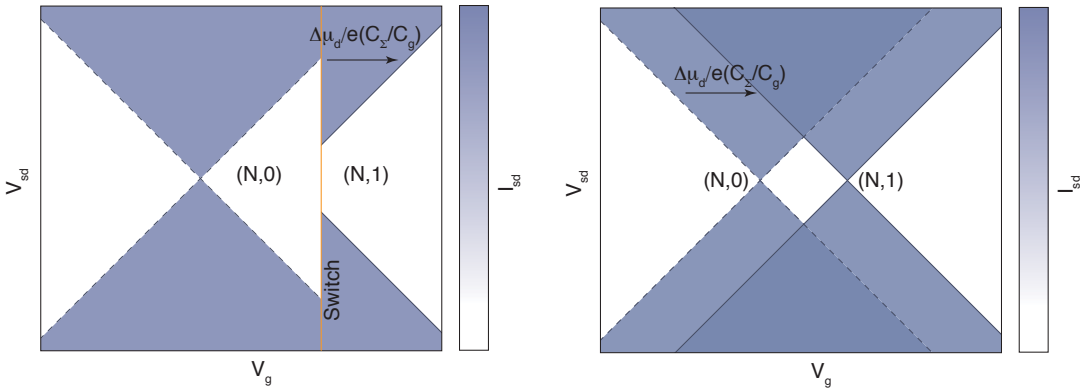


Figure 4.20: Schematic stability plot showing the effects of a capacitively coupled trap. (a) Under the action of a trap that fills suddenly, the stability plot translates discontinously in V_g. (b) When the trap state is unstable, both configurations of the transitions (N,0) and (N,1) are visible concurrently.

features in the transport spectroscopy, including the diamond edges. This effect is shown in the stability diagram of Fig. 4.20(b). This additional trap-induced state on the dot can therefore also double any excited state lines in the transport spectroscopy.

We show experimental evidence of both effects in our device later in this section. Now let us explore the case where the trap is tunnel-coupled to the dot and a lead, as modelled by Pierre *et al.*

Tunneling between the trap and dot, leading to an unstable trap state

Pierre *et al.* have shown that it is possible for a trap to be tunnel coupled to both the dot and drain, as shown in Fig. 4.21(a). In this situation, we see both a doubling of the Coulomb diamonds and an effect that causes the diamonds to 'open' — that is, we see no conduction at $V_{sd} = 0V$ on a transition. This effect is clearly visible in the transport spectroscopy of our in-plane gated dot, indicating that we indeed have a tunnel-coupled trap in our system. A full derivation of the conditions leading to the diamonds opening is presented in App. B; let us briefly describe the effect here.

In Pierre's model, the capacitance between the trap and gate is small relative to the self capacitance of the trap, so that sweeping the gate affects the dot far more than the trap. However, even if we disregard C_{gt}, the trap potential is directly linked to the dot potential, and therefore indirectly coupled to the gate. Consider transport through the $\mu_d(N,1)$ level on the dot with the trap level situated above the dot and drain: The $\mu_d(N,1)$ state is inaccessible until the dot or drain potential are raised above the trap level,

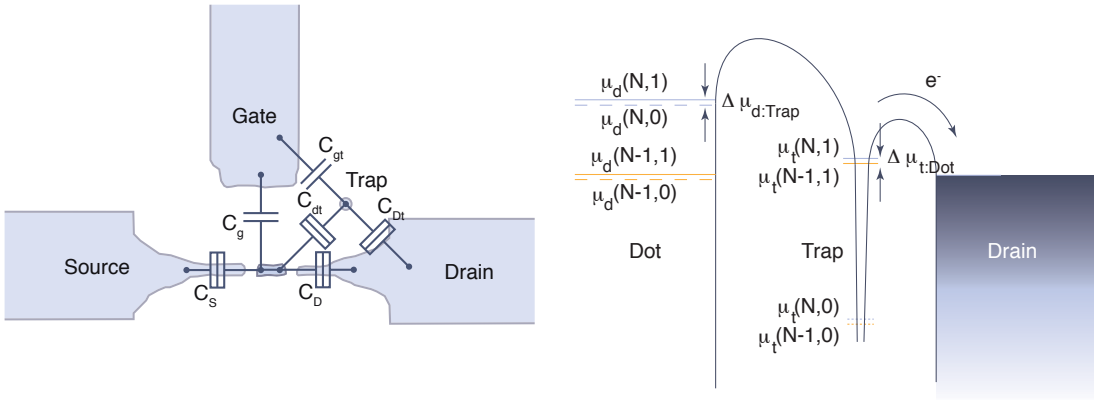


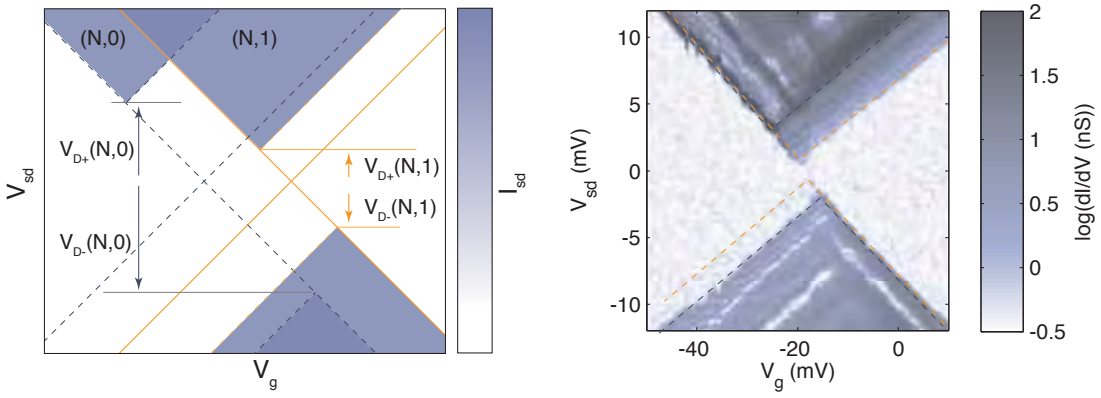
Figure 4.21: Modelling the interaction between the dot and a tunnel-coupled trap. (a) We can model a tunnel-coupled trap offset closer to the drain than the source as a dot in parallel with the drain barrier, which is also affected by the gate potential. (b) The capacitive coupling between the trap and dot causes a splitting of both the trap and dot energy levels (by an equal amount).

populating the trap. Similarly, we see no conduction through the $\mu_d(N,0)$ state unless the trap is empty, which can only occur if either the drain or the dot potential are lower than the trap. Thus, to see conduction through either the $\mu_d(N,0)$ or $\mu_d(N,1)$ states, we must first apply a sufficient bias to the drain. As we derive in App. B, the required bias to see conduction through the $\mu_d(N,1)$ state with $\mu_d = \mu_S$ is

$$V_D < \frac{-X}{1-\frac{C_{Dt}}{C_t}} \quad \text{or} \quad V_D > X\frac{C_t}{C_{Dt}} \tag{4.13}$$

where V_D is the drain bias (here the source voltage is zero, so $V_D = V_{sd}$), and X is the potential difference between the trap state $\mu_t(N,1)$ and the source. The trap will be weakly coupled to the gate, so X varies with V_g — that is, each Coulomb blockade diamond opens by a different amount. We show a schematic of the opening of a Coulomb blockade diamond in Fig. 4.22(a). In Fig. 4.22(b) we show a single Coulomb diamond of our in-plane gated device, from which we can see that indeed the diamond does not close. We have superimposed orange and blue dotted lines on this figure to highlight features that are consistent with filled and empty states of a tunnel-coupled trap, respectively. In this data, the difference between $\mu_d(N,0)$ (blue) and $\mu_d(N,1)$ (orange) is very small, making the translation in the V_g axis between these two states difficult to resolve. This implies that the trap is not strongly coupled to the dot in this device ($C_{dt} \ll C_t$).

Let us now apply this model to the stability diagram shown in Fig. 4.23(a). We can clearly see the Coulomb blockade diamonds do not close. Based on the understanding just



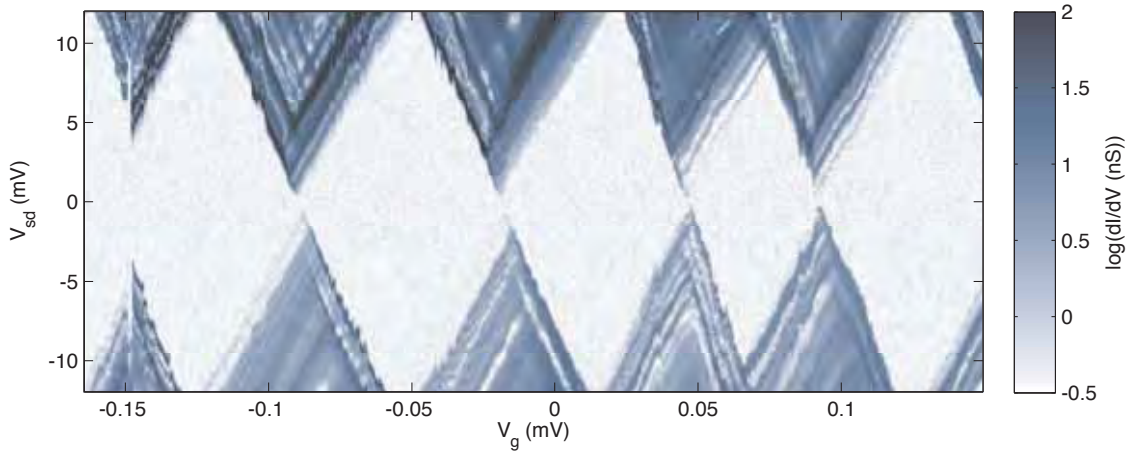
(a) (b)

Figure 4.22: Schematic stability plot showing the effect of a tunnel-coupled trap. (a) In the presence of a tunnel-coupled trap, we should see every dot level doubled in the stability diagram, separated in the gate voltage axis by $\Delta/e(C_\Sigma/C_g)$. The dot-trap interaction prevents conduction through either state at zero source-drain bias. (b) Experimental differential conductance showing this opening of the diamonds visible for the in-plane gated device.

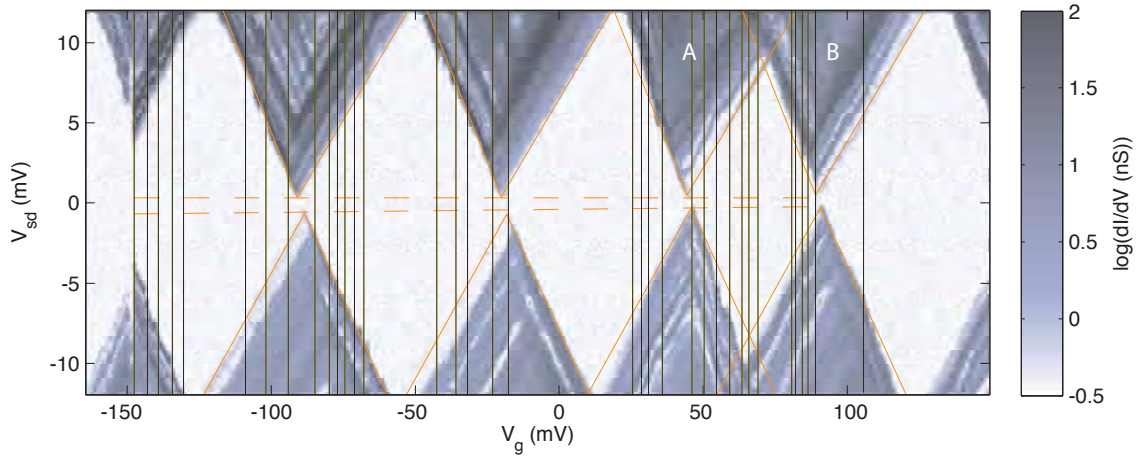
described, we have generated an overlay of the CB diamonds for a filled and empty trap, shown in Fig. 4.23(b) and Fig. 4.23(c), respectively. Here the filled trap states are outlined in orange, and the empty trap states are outlined in blue. We have also indicated what appear to be minor switching events with fine vertical black lines. Note the concentration of switching events around $25mV < V_g < 100mV$, which appear to compress together the neighbouring diamonds labelled A and B. This compression of the CB diamonds makes it difficult to locate the filled and empty state features precisely; in addition, the shift in the V_g axis between the filled and empty states is less than the thermal broadening, limiting our sensitivity to their separation. Based on this overlay, we can now analyse the degree of coupling to the trap.

We see the splitting of the orange overlay decreases with gate voltage. The lower portions of diamonds move up at a rate of $2.2 \times 10^{-3} V/V$, whereas the upper diamonds are essentially flat. From Eq. 4.13, we expect the upper diamond to shift by

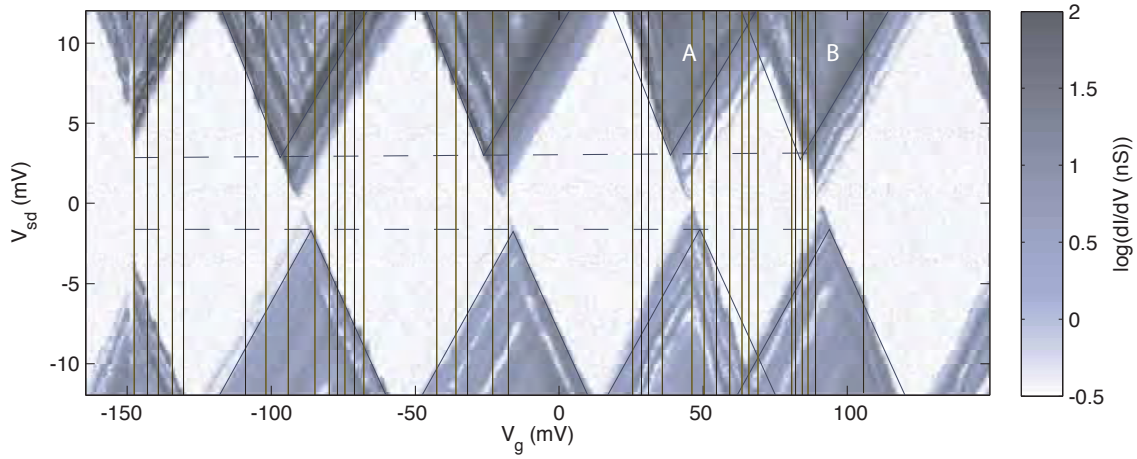
$$V_{D+} = -\left(V_g \frac{C_{gt}}{C_t} + X_c\right) \frac{C_t}{C_{Dt}} \tag{4.14}$$



(a)



(b)



(c)

Figure 4.23: Signs of a tunnel-coupled trap in the stability plot of the in-plane gated device. (a) The experimental stability plot showing diamonds that do not close. (b) The same plot overlayed with switches in μ_d (black), and features associated with a filled tunnel-coupled trap (orange). (c) Overlay of features associated with an empty tunnel-coupled trap (blue).

where X_c is the constant offset in the trap potential at equilibrium. The derivate of this equation with respect to V_g is given by

$$\begin{aligned} \frac{dV_{D+}}{dV_g} &= -\frac{C_{gt}}{C_{Dt}} \\ &\simeq 0V/V \end{aligned} \tag{4.15}$$

where in the last step we account for the fact that the upper portions of the diamonds do not shift with V_g. Similarly, for negative drain biases, we expect the offset to decrease according to the relation

$$V_{D-} = -\left(V_g \frac{C_{gt}}{C_t} + X_c\right) \frac{1}{1 - \frac{C_{Dt}}{C_t}} \tag{4.16}$$

so that the slope of this equation with respect to V_g is

$$\begin{aligned} \frac{dV_{D1-}}{dV_g} &= \frac{C_{gt}}{C_t - C_{Dt}} \\ &\simeq 2.2 \times 10^{-3} V/V \quad \text{from Fig. 4.23(b)} \\ \Rightarrow C_{gt} &\simeq 2.2 \times 10^{-3} C_{dt} \end{aligned} \tag{4.17}$$

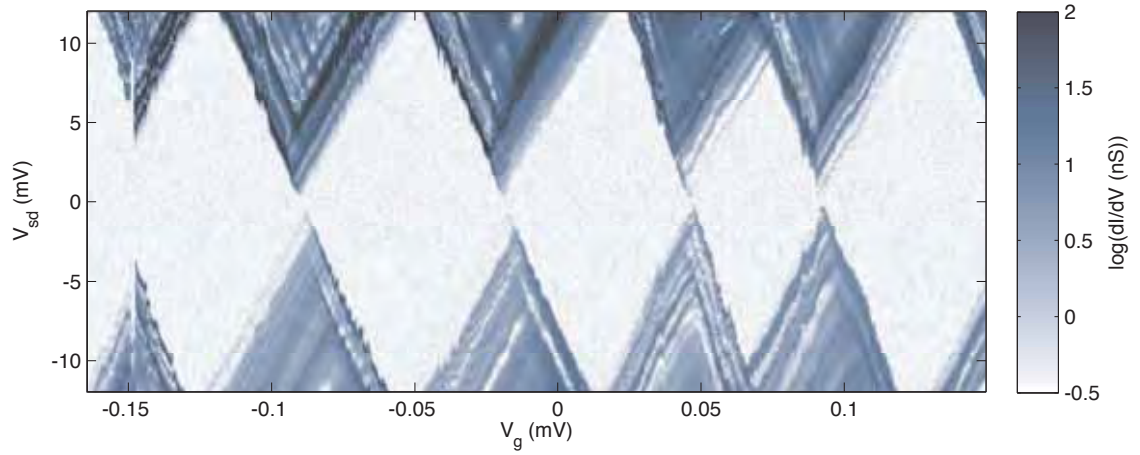
Finally, the translation of the diamonds in the V_g axis as the trap fills is given by

$$\begin{aligned} \Delta V_g &= \frac{\Delta\mu_{d:Trap}}{e} \frac{C_\Sigma}{C_g} \\ &= \frac{e^2}{C_t} \frac{C_{dt}}{C_\Sigma} \frac{1}{e} \frac{C_\Sigma}{C_g} \\ &= \frac{eC_{dt}}{C_t.C_g} \\ &\ll 0.5mV \end{aligned} \tag{4.18}$$

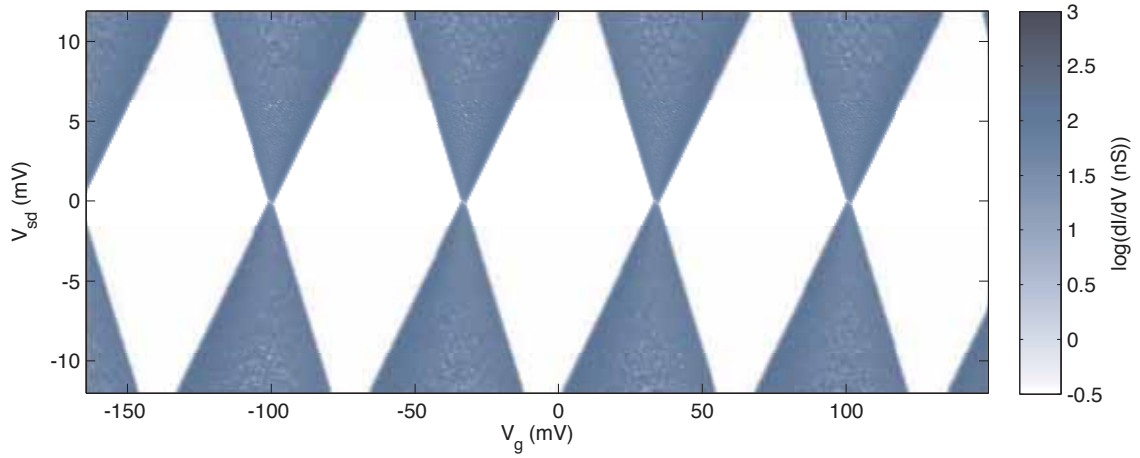
where we set $V_g = 0.5mV$ as our measurement resolution in the gate voltage axis due to thermal broadening of the electron energy levels. From Eq. 4.18 we can determine the ratio of capacitive coupling from dot to trap versus the self capacitance of the trap.

$$\begin{aligned} \frac{C_{dt}}{C_t} &\ll 0.5 \times 10^{-3} \frac{C_g}{e} \\ &\ll 0.5mV/77mV = 6.5 \times 10^{-3} \end{aligned} \tag{4.19}$$

The implications of this are that the trap is only very weakly coupled to the dot, making up <1% of the trap's sum capacitance; furthermore, from Eq. 4.17, the coupling C_{gt} is about three orders of magnitude smaller than C_{dt}. From this result, we can make



(a)



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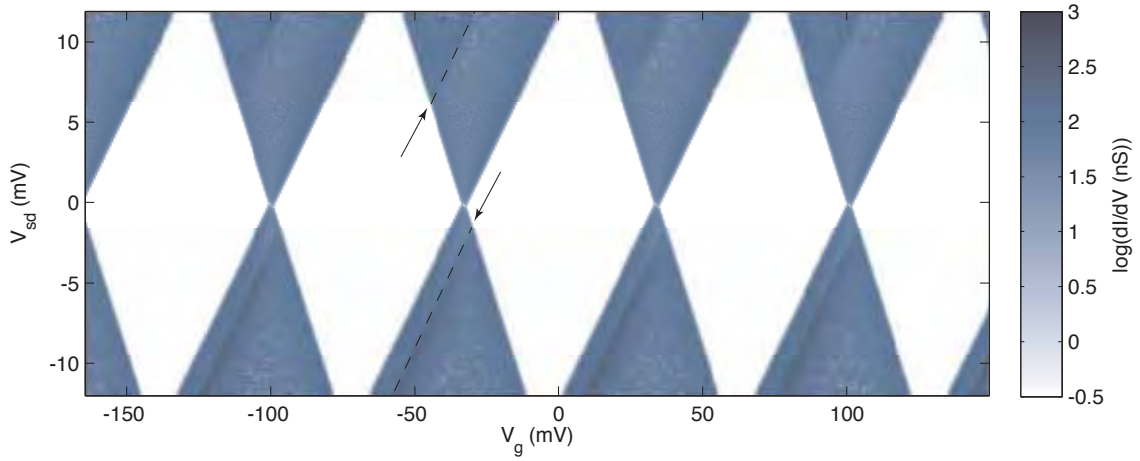


(c)

Figure 4.24: Modelling the stability plot of the in-plane gated quantum dot with a tunnel coupled trap. (a) Experimental stability plot showing diamonds that do not close with replicated diamonds. (b) Simulated stability plot without a tunnel-coupled trap. (c) Simulated stability plot with a tunnel coupled trap with replicated diamonds.

the approximation that $C_t \simeq C_{Dt}$, which is to say that the trap is most strongly coupled to the drain. However, we cannot extract the value of this sum capacitance, C_t, without first knowing the drain voltage at which multiple electrons occupying the trap, which we cannot see from this data. We have modelled the expected (classical) transport response of our dot both with and without a coupled trap in Fig. 4.24(b) and Fig. 4.24(c), respectively. The coupled trap diagram was modelled by setting $C_t = 20aF$, from which we get $C_{dt} = 0.13aF$ and $C_{gt} = 0.0003aF$. In general, this modelled stability diagram is in good agreement with the experimental data, with lines running parallel to the diamond edge in the stability map, as highlighted with black dashed lines in Fig. 4.24(c). These results highlight that we have a tunnel-coupled trap in our device in agreement with previous studies [182].

4.4.2 Switching of the in-plane gating action caused by capacitive coupling with nearby traps

In the stability plot of Fig. 4.23(b), there is clear evidence of switching in the dot potential, which we have highlighted with fine vertical black lines. In this section, we perform a detailed analysis of these switching events using the simple capacitively coupled trap model from Fig. 4.19(a), and discuss the implications of these switching events for STM-patterned SETs.

The magnitude of the switch in the V_g-axis is proportional to C_{dt}/C_t. To cause a measurable shift of the Coulomb blockade peaks, we require the trap to be sufficiently close to the dot. From this effect, the SET itself can be used as a crude indicator of the location of traps. Probing the state of traps using an SET is only possible when the dot is biased on a Coulomb blockade peak, so we can see it measurably affect the device current. In addition, traps may be coupled to one another, sometimes through the dot itself. In this situation, the occupancy of traps in the surrounding substrate becomes a complex many-body system. Without any certainty or control of the trap potential, switching events are therefore only visible when the trap population-depopulation energy happens to coincide with a Coulomb blockade peak.

In this device, switching events appear to occur at random. We have therefore built up a statistical data set of switching events to quantify the degree of switching. For this, we have performed several experiments in which we continually swept the gate across several Coulomb blockade peaks at a fixed source-drain bias; the results of such an experiment at $4K$ are shown in Fig. 4.25(a). The data was recorded in one direction only ($V_g : -0.5V \rightarrow +0.5V$), to eliminate any hysteresis in the gate action.

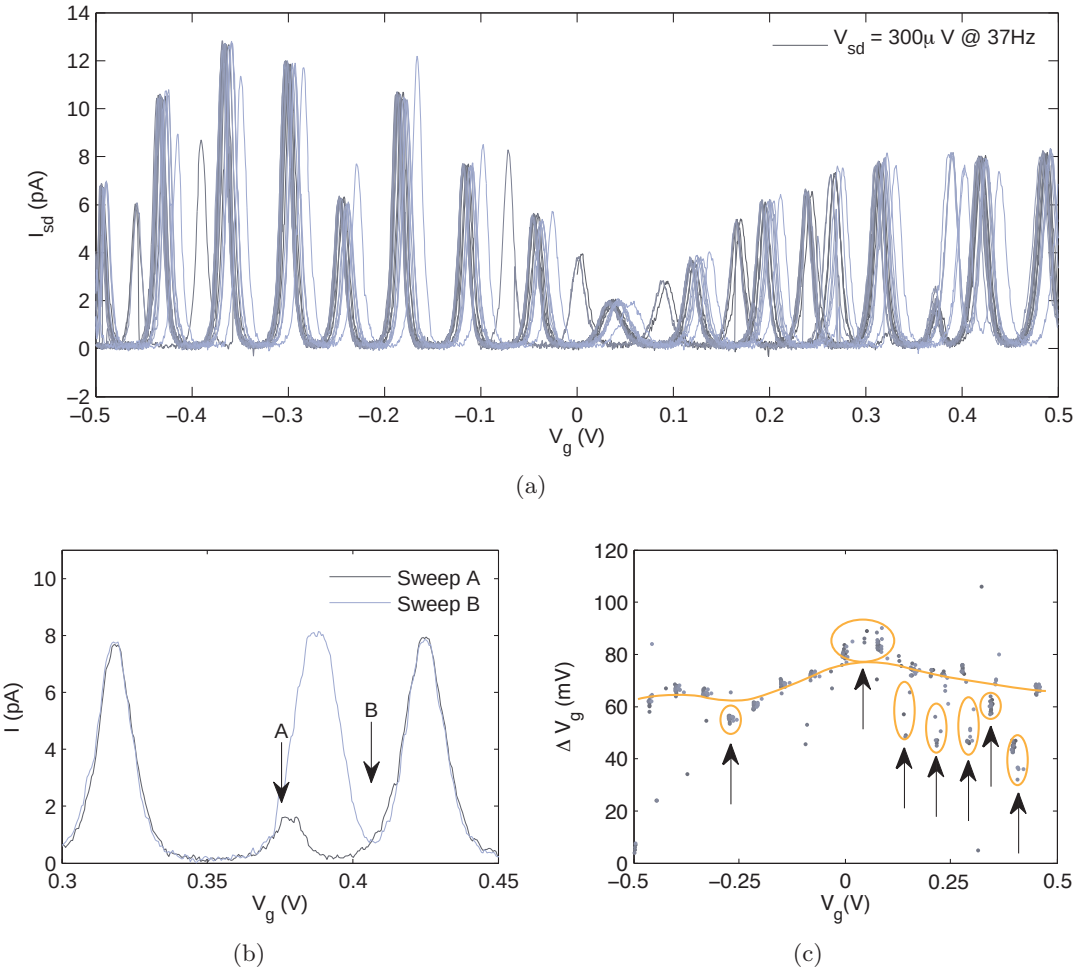


Figure 4.25: Observation of multiple switching events in the Coulomb blockade oscillations at 4.2K. (a) 20 CB sweeps taken over the same range at the same drain bias sweeping from negative to positive gate voltages. (b) Close-up view of two clearly visible switches in the peak location at $V_g = 0.38V$. (c) Mapping the separation in gate space between successive CB peaks as a function of V_g.

Perhaps the first and most obvious observation from Fig. 4.25(a) is that smaller peaks appear to coincide with regions of frequent switches. A clear example of this is the peak at $V_g = 0.38V$. We show this peak in greater detail in Fig. 4.25(b). In the majority of sweeps this peak is sharp and small in amplitude — an example of which is Sweep A. However, sometimes we see the trace develop into a full-height Coulomb blockade peak, as shown in Sweep B. The implication is that in the majority of sweeps, the gate action is consistently switching at point A, where $V_g = 0.38V$ — causing a sudden translation in the V_g-axis to the other side of the peak. In Sweep B of Fig. 4.25(b), the trace develops into a full-height peak before the gate action clearly undergoes a switch at point B, indicating

that there has been a shift in the effective trap potential. It is clear at this magnified scale that when a switch occurs, there is a distinct change in the peak spacing. This gives an objective measure of both the location and magnitude of switching events. We have plotted the peak spacing as a function of V_g in Fig. 4.25(c), from which we can see that the peak spacing undulates slowly across the whole gate range, where this slow variation is inversely proportional to the peak magnitude. This is a direct indication of the link between the dot capacitance and the device conductance. Fuhrer *et al.* explain in the supplementary information of their 2009 paper [22] that this phenomenon is consistent with chaos within the quantum dot. Under this model carriers within the dot scatter off the confinement walls, forming chaotic coherent paths within the dot that evolve with the gate potential [183]. This causes both the tunnelling probability and capacitive coupling to the chaotic electron cloud to vary with gate voltage, giving rise to changes in the peak height and spacing. However, from Fig. 4.25(c) we clearly see distinct clustering of the peak spacing that is not consistent with the slow undulation of chaos within the dot, indicated with arrows. It is this consistent switching of the Coulomb peak location that we attribute to traps. The switching affects the peak located at $V_g = 0.38V$ most, which is the transition we focussed on in Fig. 4.25(b). Here we see that ΔV_g varies between $30mV < \Delta V_g < 45mV$, which is less than the expected peak spacing indicated by trend line ($\Delta V_g \simeq 65mV$). This indicates that there is a trap that consistently causes a negative shift in the dot potential, where $-35mV < \Delta V_{g:Trap} < -20mV$. The scatter of points around $\Delta V_g = 30mV$ is attributed to the interaction between multiple traps. The most consistent cluster of points occurs at $\Delta V_g = 45mV$, where that the trap is causing a shift in the peak location of $V_{g:Trap} = -20mV$. Scaled by the expected peak spacing, this implies

$$\begin{aligned} \frac{C_{dt}}{C_t} &= \frac{\Delta V_{g:Trap}}{\Delta V_{g:Gate}} \\ &= \frac{20mV}{65mV} \\ &= 0.3 \end{aligned} \tag{4.20}$$

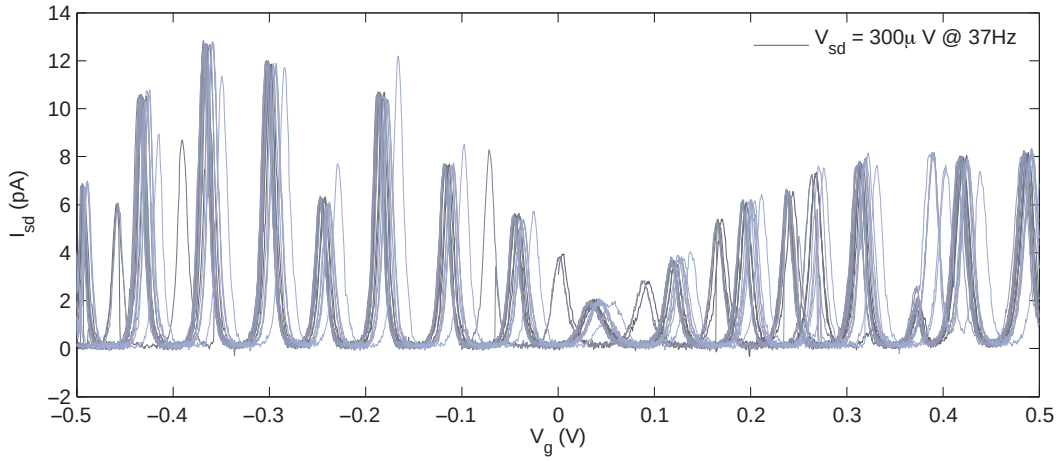
Which indicates that, for the most strongly-coupled trap, the trap is more strongly capacitively-coupled to the gate than the dot ($C_{gt} = 70\%C_t$, $C_{dt} = 30\%C_t$). Given the relative dimensions of the gate and dot, we cannot say from this whether the trap is physically closer to the gate, since the gate is much larger. However, the fact that the shift in the gate voltage axis is negative indicates that the trap is depopulating as the gate transitions past $V_g = +0.38V$ [48]. Depopulation of the trap acts as a positive addition

to the effective gate voltage, so the same peak occurs at a lower gate voltage. As the gate becomes more positive an electron will be attracted towards it, and so it becomes likely that we see an electron pass from the trap to the gate at this potential, and not from the trap to the dot. The fact that the switch occurs so consistently indicates that the tunnel coupling is relatively strong, since it only requires the trap potential to fall between the gate and dot, without any measurable transience waiting for the trap to empty.

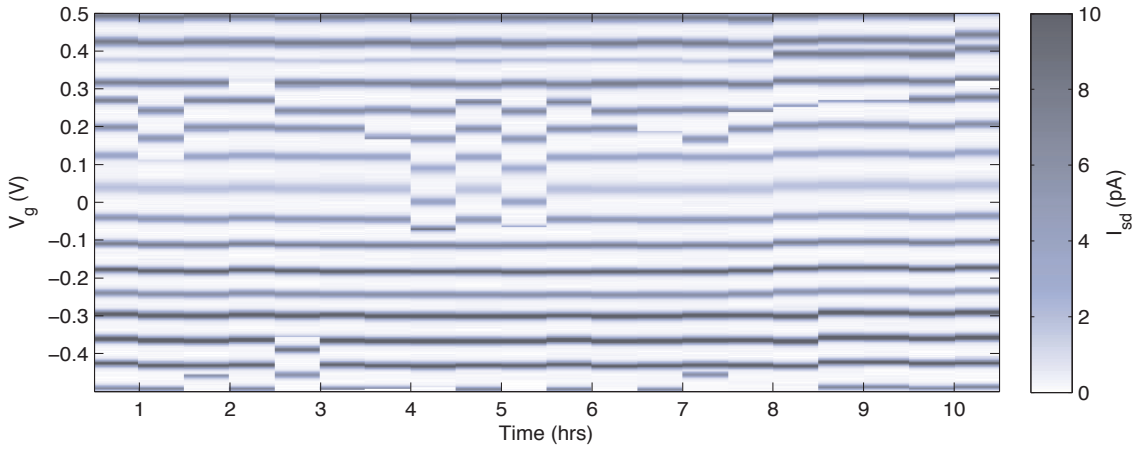
The gate sweeps were recorded at regular intervals, so the data also includes transient information about the switching events. To better illustrate this, we show the data as a 2-D map in Fig. 4.26(b); here the x and y-axes of the 1-D plot in Fig. 4.26(a) translate to the y and z (colour) axes, respectively. On the new x-axis we now plot the time at which each sweep was taken. Switching events clearly stand out in this map as discontinuities in an otherwise periodic pattern. We have indicated the location of all switching events with orange lines in Fig. 4.26(c). This map shows that on all gate sweeps, a consistent switch (instantaneous shift in the gate voltage axis) is visible in the regions marked 'a', 'c', and 'd'; an occasional switch in region 'e', and an inconsistent switch within the region marked 'd'. We conclude that what therefore looked like many switching events scattered throughout the gate range can be attributed to five traps.

First let us focus on the strongest switch at $V_g = 0.38V$ (described previously), which is highlighted as the range labelled 'a' in Fig. 4.26(c). This switch is consistent throughout the whole map, only showing an offset at $8hrs$ and $10hrs$, where all peaks undergo a similar shift. This global shift of all peaks is indicative of the interaction between traps, causing an independent shift in the dot potential. The fact that this global shift does not repeatedly occur at a particular gate voltage indicates that it is either weakly coupled to the gate, or simply that the tunnel rate to it is extremely low. There are two much weaker global shifts at $2.5hrs$ and $9.5hrs$, which are less well coupled to the dot.

Next we cooled the sample to base temperature to see the temperature dependence of the switching events. The data from this experiment is shown in Fig. 4.27; again we see a slow undulation in the peak separation that is inversely proportional to the peak height, consistent with chaos within the dot (Fig. 4.27(a) c.f. Fig. 4.27(c)). There is also generally less scatter in the peak separation at this temperature relative to 4K — the only clear indication of switching occurs between the peaks at $V_g = -0.2V$ and $-0.15V$, highlighted in the zoomed image of Fig. 4.27(b). As shown in Fig. 4.27(c), the magnitude of this switch is extremely consistent $\Delta V_g = 48 \pm 2mV$ (indicated by the arrow at $Vg = -0.175V$). The first striking feature in the 2-D map show in Fig. 4.27(d) is the dramatic increase in the drift decay constant over that seen at 4K (Fig. 4.26(b)) — which is to say that it takes approximately $6hrs$ for peaks in this map to settle to a consistent location, drifting



(a)



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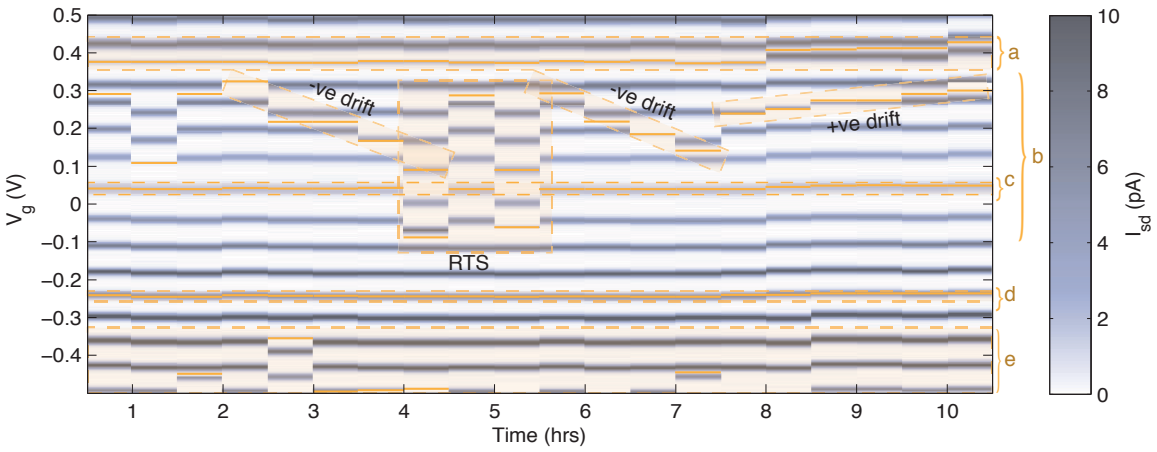
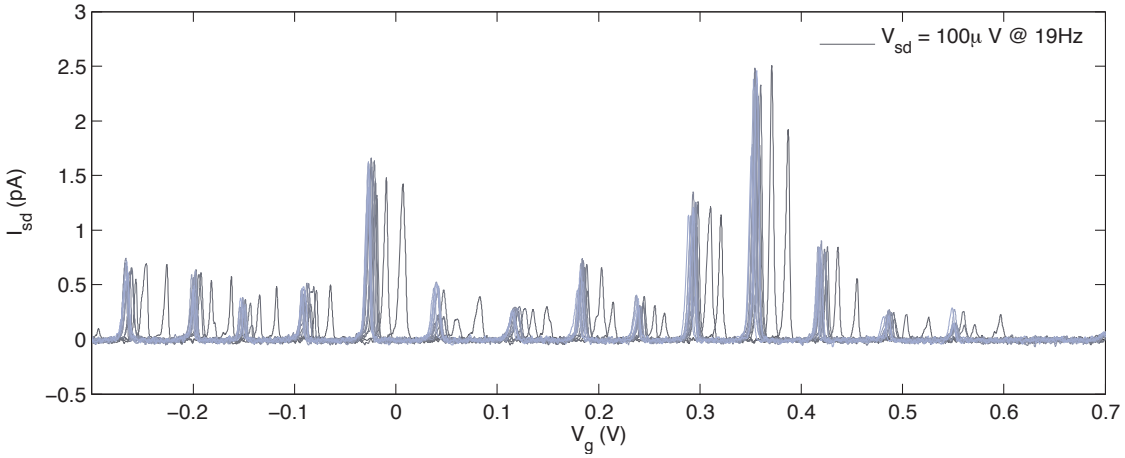
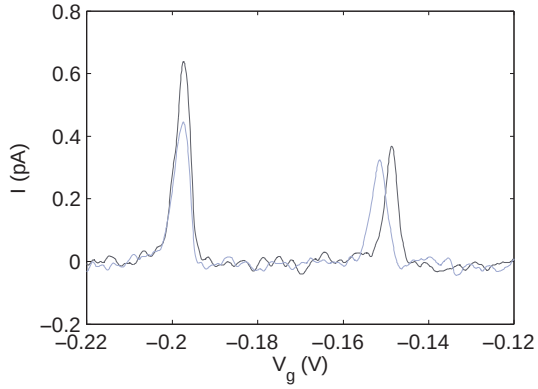


(c)

Figure 4.26: Mapping the location of switching events in the in-plane gated quantum dot as a function of time at 4K. (a) 20 CB sweeps taken over the same range at the same drain bias sweeping from negative to positive gate voltages. (b) Switching events on a 2-D time versus gate voltage map. (c) An overlay showing the location of switches, highlighting different trends.



(a)



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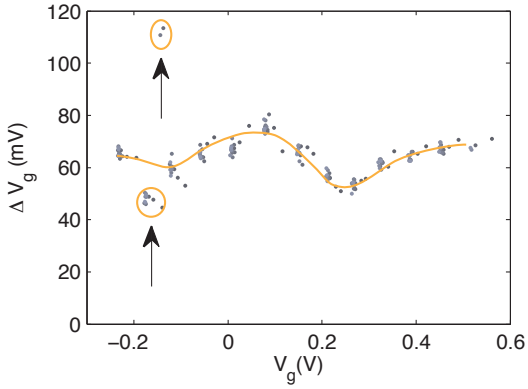

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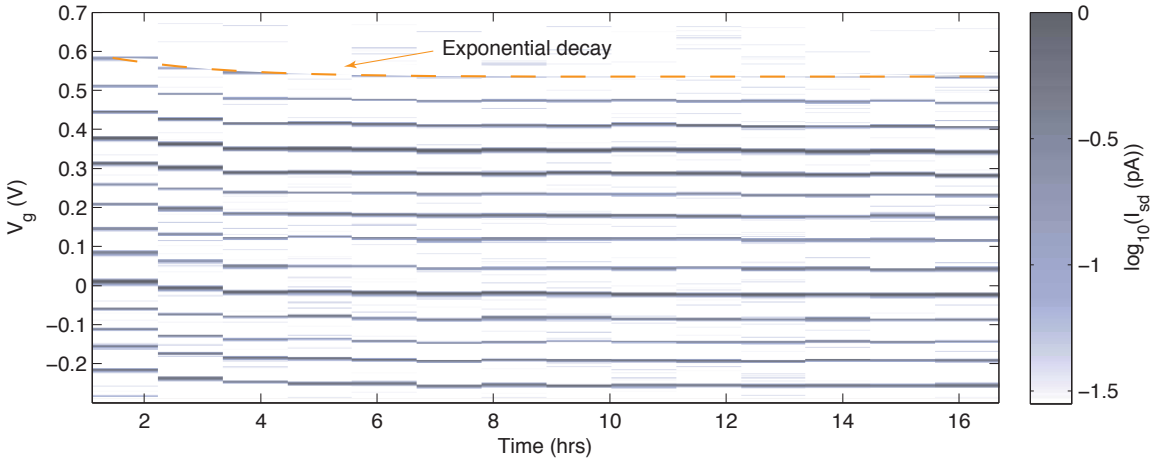


(d)

Figure 4.27: Mapping the location of switching events in the in-plane gated quantum dot as a function of time at base temperature. a) 15 CB sweeps taken over the same range at the same drain bias sweeping from negative to positive gate voltages. (b) Close-up view of a clearly visible switches in the peak location at $V_g = -0.18V$. (c) Mapping the separation in gate space between successive CB peaks as a function of V_g. (d) A 2-D time versus gate voltage map showing the peak drift as a function of time.

according to a first-order exponential with time. The second notable feature is that the number and magnitude of switching events dramatically reduces. Otherwise, there are really no significant transient events, with the exception of slight universal shifts at $4.7hrs$, $6.7hrs$, and $12.2hrs$.

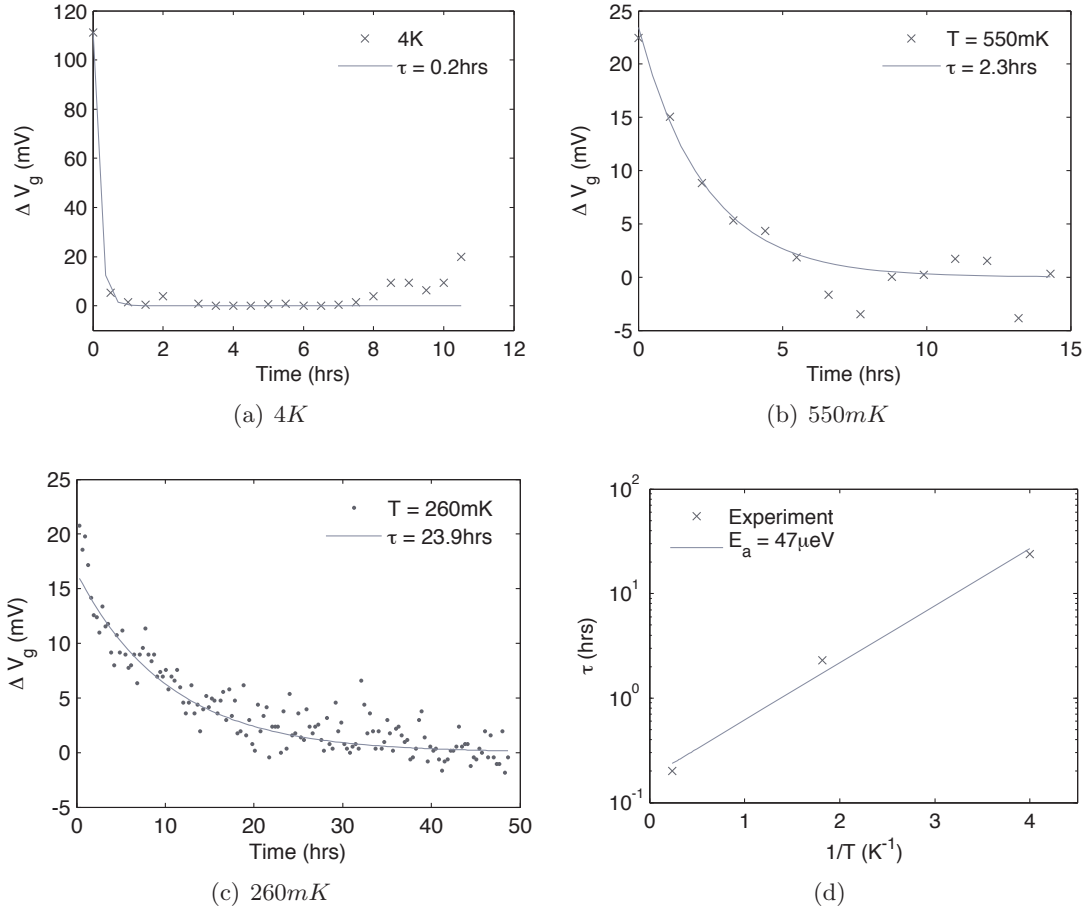
The fact that the peak spacing is also proportional to the peak magnitude at base temperature indicates that the beating effect is not thermally activated. This is consistent with our model of chaotic electron wavefunctions within the dot. In contrast to the beating pattern, the reduction in the number of switching events with temperature indicates that the interaction between the dot and traps is thermally activated, and so the traps must be very shallow (at $4K$, $k_BT = 370\mu V$). Shallow traps might include donors (e.g. background doping of the substrate) under the influence of an electric field from the substrate, and traps at the Si–SiO_2 interface.

Charge offset drift in STM-patterned SETs

Drift in the operating point of single electron transistors is a common phenomenon across all material systems, since SETs are inherently capacitively coupled to their surroundings. Therefore, any minor fluctuations of charge in the surrounding substrate give a corresponding change in the SET operating point. In particular, if the operating point drifts away from a peak, into the Coulomb blockade regime, the SET will no longer sense charge.

The time dependence recorded while studying switches in the previous section showed the location of the Coulomb blockade peaks drift over time, where the rate of this drift changed with temperature. We have extracted the mean peak drift as a function of time in Fig. 4.28 at both $4K$ and the base fridge temperatures of the two fridges used to measure this device. The fridge used within our research centre has a base temperature of $\sim 260mK$, and the fridge used for noise/switching measurements at the Indian Institute of Science has a base temperature of $\sim 550mK$ calculated by fitting the Coulomb blockade peaks. The peak drift was calculated by finding the point of maximum correlation of the $t = 0hrs$ sweep with each successive sweep thereafter. These line traces show an exponential decay of the drift, with a larger time constant at lower temperatures.

The lowest-temperature trace was recorded by sweeping the gate voltage back and forth over five Coulomb blockade peaks for two days on the fridge in our research centre, intended to verify that the device had settled before recording the magnetic field dependence described at the end of this chapter. There is a large scatter in each of these traces because of the switching events described in the previous section, and so the time constant extracted in each case is only accurate to within $\pm 20\%$. With this uncertainty in mind, we



(a) $4K$ (b) $550mK$

(c) $260mK$ (d)

Figure 4.28: Drift decay constant of the in-plane gated device as a function of temperature. (a) Shift in the peak location at 4K recorded by calculating the point of greatest correlation of each CB sweep with the $t = 0$ sweep. (b) Peak drift at $\sim 550mK$. (c) Peak drift at $\sim 260mK$. (d) Plotting the drift time contant of the in-plane gated device as a function of temperature gives an energy barrier of $47\mu eV$ from the Arrhenius fit.

plot the drift time constant as a function of temperature in Fig. 4.28(d). The Arrhenius fit shown indicates a very low barrier to thermal activation ($47\mu eV$). As a consequence of this temperature dependence, the time constant approaches one day at a temperature of $260mK$, which is only modestly cold by dilution refrigerator standards. If we extend this Arrhenius plot out to the temperatures required for quantum computing applications ($T < 100mK$) [10], we find that we would require several days for the drift to settle.

Given the presence and severity of switching events, and the fact that switches appear to be randomly distributed in magnitude, it seems likely that drift is caused by the population/depopulation of many weakly coupled traps in response to changes in the gate potential, where there is an inherent transience associated with transport to the trap. Given the energy barrier against generating intrinsic carriers ($\sim E_g/2$ for an un-doped

substrate), it is unlikely that the trap is populating or depopulating from random local thermal recombination or generation events. Also, since the generation of intrinsic or extrinsic carriers should in principle have a minimum energy barrier equal to the donor ionisation energy, it is unlikely that the temperature dependence is caused solely by the generation of new carriers. We therefore believe this barrier reflects the energy, on average, required to populate nearby traps from tunnelling or thermionic emission — if only those close enough to actually influence the dot potential.

From this analysis, we have a better understanding of the frequency and nature of switching events expected for in-plane gated devices. Specifically, though we do see the effects of five traps over a gate range of $\Delta V_g = 1V$ at 4K, we see only one such switch at base temperature. From this and the drift results, we conclude that the interaction between the dot and traps is thermally activated. Furthermore, if we select an appropriate gate range, we can avoid these large-energy switching events at base temperature. In the next section, we assess fluctuations in the dot potential with greater resolution in energy and time by measuring charge noise.

4.5 Charge noise of the in-plane gated SET

As the STM-fabrication scheme discussed in this thesis is unique to our group, here we give the first systematic analysis of noise in such STM-patterned devices. In this section we review the initial measurements of low frequency noise in δ-doped $Si{:}P$ Hall bars, conducted in collaboration with the group of Arindam Ghosh at the Indian Institute of Science. We then give a brief description of previous noise measurements in silicon quantum dots, and finally present the measured conductance noise in our STM-patterned SET.

4.5.1 Review of noise in δ-doped Si:P and SETs

Noise in semiconductor devices

Flicker noise is a type of noise present in all macroscopic semiconductor components; it differs from thermal (Johnson) noise in that its power spectrum is not uniformly distributed in frequency — the flicker noise power spectrum decays in proportion to $1/f$ — hence its alternate name of $1/f$-noise. Many physical processes may lead to flicker noise, for example contact noise [184], mobility fluctuations [185], or fluctuations in the number

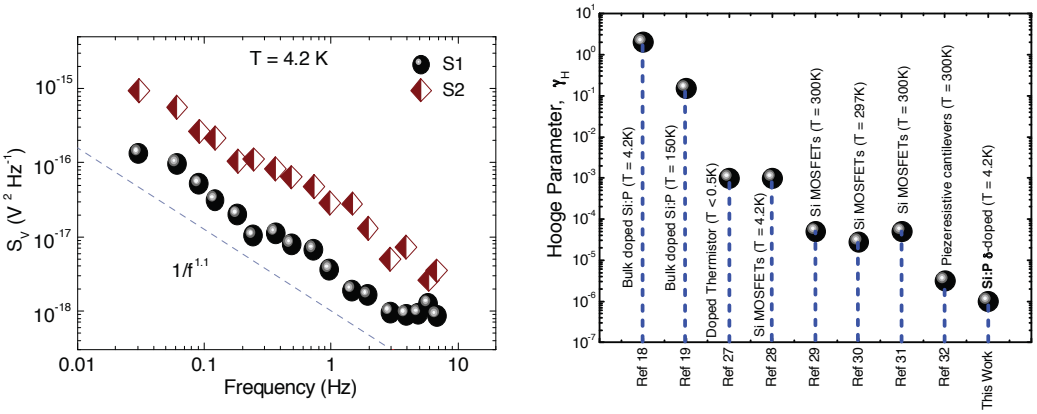
of carriers [186]. Each process gives a $1/f$ power distribution, and so it is not possible to correlate the presence of $1/f$ noise with a single process. For example when a trap continually populates and depopulates, it causes the device current to switch back and forth between two fixed values — commonly referred to as a random telegraph signal (RTS). A random telegraph signal has a power spectral density $S(f)$ given by (see [57, pg. 374]):

$$S(f) = \frac{2(\Delta I)^2 \tau}{4 + (2\pi f \tau)^2} \tag{4.21}$$

where ΔI is the fluctuation in the current between the filled and empty trap states, and τ is the period of the RTS (here we assume a 50% duty ratio). From this relationship, we see that the power spectral density of a single coupled-trap is proportional to $1/f^2$. Therefore, a single dominant fluctuator does not yield the $1/f$ spectrum of flicker noise. However, there are several experimental examples where the number of fluctuators within the device was scaled up [187–190] — typically by increasing the size of the test devices — showing an unambiguous evolution of the power spectrum from $1/f^2$ to $1/f$, indicating that the capture and emission of carriers from traps does in fact cause $1/f$ noise. Mathematically, to construct $1/f$ noise from many constituent RTS ($1/f^2$) spectra requires the time constants of all RTSs to be uniformly distributed in $\log(f)$; in most cases this is satisfied by the thermal broadening of carrier energies, where traps far from the Fermi level are populated exponentially infrequently because of the scarcity of carriers with sufficient energy. Given its frequency dependence, flicker noise typically dominates over other forms of noise at very low frequencies (e.g. $1mHz$).

As part of a collaboration with Assistant Professor Arindam Ghosh at the Indian Institute of Science (IISc), the noise of Si:P δ-doped Hall bar samples grown at UNSW was measured at the IISc using an AC four-probe Wheatstone bridge technique [192–194]. Here an AC bias was applied to a Wheatstone bridge incorporating the sample, and the current was measured using a high-frequency data acquisition card. The results of this work are shown in Fig. 4.29 from the publication of Shamim *et al.* In Fig. 4.29(a) we see that at $4.2K$ the noise has an approximately $1/f$ distribution. Figure 4.29(a) shows the magnitude of the flicker noise in these δ-doped layers, which is characterised by the power spectral density, S_v. The noise is very low compared to other doped silicon systems (Fig. 4.29(b)) [191]. Since the δ-doping and contacting process of these samples is identical to our STM-patterned devices, we know that the contacts and STM-patterned leads in our devices contribute little to the noise of our STM-patterned SETs.

As we will show, we can attribute the majority of noise in our devices to fluctuations in the dot potential. The physical source of fluctuations in traditional semiconductor



(a) (b)

Figure 4.29: Flicker noise in our δ-doped Si:P system. (a) At $4.2K$ the power spectral density of the noise in Si:P δ-layers show a $1/f^{\alpha}$ dependence, where $\alpha = 1.1$. (b) The Hooge parameter (a measure of the noise independent of sample geometry and applied bias) is less in these δ-doped Si:P layers than many other silicon based devices. Both the figures and the cited references are from the work of Shamin *et al.* [191].

devices — e.g. capture and emission of carriers from nearby traps— would also give rise to fluctuations in the dot potential of our device. We have shown when addressing both tunnel-coupled and capacitively-coupled traps that each causes small shifts in the dot potential as they capture and emit electrons. However, so far we have only addressed discrete traps, where the population of a single trap causes the effective dot potential to switch discontinuously between the $\mu_d(N,0)$ and $\mu_d(N,1)$ states. In the next section, we show $1/f^{\alpha}$ noise within our dot arising from the ensemble average of many such coupled traps.

Noise in single electron transistors

Noise is an important consideration in the operation of SETs because these devices are exceptionally sensitive to their surrounding environment. This is particularly significant for proposed applications of SETs in which they are biased at the point of maximum transconductance — halfway down a CB peak — amplifying the effects of noise many times over. Several research groups have studied noise in SETs [195–204], with Zimmerman *et al.* being most prolific [200, 205–209]. The types of noise witnessed in SETs include Johnson noise, flicker noise, RTSs, large amplitude switches in the charge offset, transient decays in the charge offset, and low-frequency drift in the charge offset. We note that Zimmerman *et al.* frequently use 'drift' to describe random fluctuations in the charge offset after the device equilibrates for many weeks, where these fluctuations are not consistent with flicker

noise; in the following discussion we avoid using the term drift in this way because it conflicts with our usage in the previous section when describing the transient decay of the charge offset as the device equilibrates.

It is simple to distinguish between Johnson noise, flicker noise, and RTSs because of the frequency-dependence of their power spectra. Transient drift and switches, on the other hand, are simpler to see in the time series data — we therefore note the importance of studying noise in both the time and frequency domains, especially because switches, for example, have the same $1/f^2$ power spectrum as an RTS. Given that we have already studied transient drift and switches in the previous sections, here we focus on flicker noise and RTSs. These types of noise arise from the same physical processes — flicker noise is commonly understood to be the result of many concurrent RTS events [57] — and so we can reasonably expect the presence of both $1/f$ noise and RTSs. As such, we can expect the power spectra of SET noise to show a $1/f^{\alpha}$ relationship, where $1 \leq \alpha \leq 2$ varies according to the dominance of discrete fluctuations.

4.5.2 Conductance noise in STM-patterned SETs

The conductance of an SET is defined by the resistance of the leads, the transparency of the tunnel barriers, and the location of electronic states within the dot. In this section, we will isolate the dominant source of noise in our devices. We see from the work of Shamim *et al.* [191] that the noise of our 2-D Si:P δ-layers is exceptionally low, implying that any visible fluctuations in the SET conductance are unlikely to arise from the STM patterned leads. We therefore focus on fluctuations arising from either the tunnel barriers or the dot potential. We know the transparency of tunnel barriers changes under an applied gate bias, indicating that they are sensitive to fluctuations in the local chemical potential. Similarly, we know the conductance of the dot is strongly dictated by the gate potential. The question is therefore which element dominates — the dot or the barriers — in the presence of a fluctuating potential? Here we address this question, and explore the nature of the potential fluctuations.

Discerning between fluctuations in the tunnel barriers and the dot

To discern between noise in the dot potential and barriers, here we model both cases to compare their behaviour. A quintessential Coulomb blockade peak is shown in Fig. 4.30(a) (labelled 'ideal') for the thermally-broadened regime ($T = 250mK$). Any fluctuations in the dot potential randomly shift this peak in the μ_d axis, as shown in the example trace

labelled 'Noisy $\Delta\mu_d$', in which we have added Gaussian noise to the dot potential. Since any noise in μ_d causes a horizontal shift of the ideal curve, the conductance at the centre of the peak varies little, since $dG/d\mu_d$ is flat in this region, so the noisiest part of the curve occurs mid-way down the Coulomb blockade peak. A comparable shift in the barrier potential, in contrast, would alter the conductance at the centre of the peak more than anywhere else, as shown in Fig. 4.30(b). This is because, in the thermally-broadened regime, the magnitude of the conductance fluctuations varies in proportion to the peak height. Using this distinction, we can isolate the source of noise in an SET.

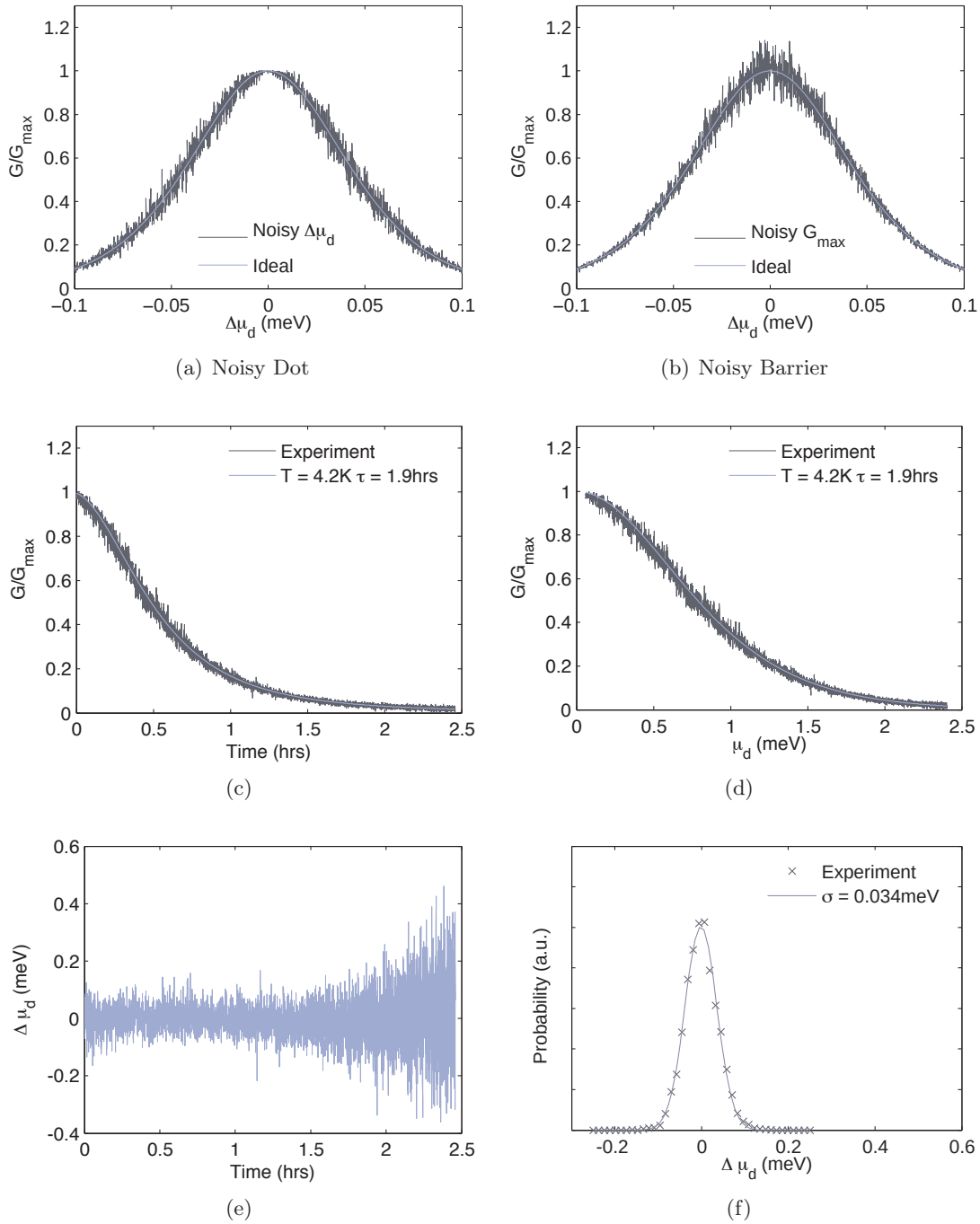
Given that low frequency fluctuations dominate 1/f noise, to assess the variance in conductance throughout the CB peak we needed to sweep the gate very slowly. In practice, we found the peak to drift faster than our desired ramp rate, so it was simpler to leave the gate voltage at a constant value, initially set at the top of the peak, and observe the drift. Figure 4.30(c) shows one such time sweep. We can translate this drifting time-series into an equivalent Coulomb blockade sweep by fitting a first-order exponential to the drift, where the dot potential shift changes the device current according to the thermal broadening relation, so that

$$\begin{aligned} \Delta\mu_d &= \Delta_{mag} e^{-t/\tau} \\ \frac{\Delta G}{G_{max}} &= \frac{\Delta\mu_d / k_B T}{\sinh(\Delta\mu_d / k_B T)} \end{aligned} \tag{4.22}$$

where Δ_{mag} is the magnitude of the drift in the dot potential $\Delta\mu_d$. The fitting parameters for this system of equations are the decay time constant τ, the drift magnitude Δ_{mag}, and the temperature T. We set $T = 4.2K$ in the following analysis to match with experimental conditions.

We show a fit using this formula in Fig. 4.30(c). We note that the drift time constant of this fit ($\tau = 1.9hrs$) is longer than that measured in the switching analysis at 4.2K ($\tau = 0.2hrs$), which we attribute to the fact that in the switching analysis the gate was swept back and forth, forcing nearby traps to populate and depopulate. Here however we must wait for the population events to occur. The calculated dot potential from this fit was used to plot Fig. 4.30(d), from which it is clear that the noise is greatest mid-way down the peak, not at the centre of the peak ($\mu_d = 0$). We thus conclude that the noise more closely resembles fluctuations in the dot potential (Fig. 4.30(a)) than noise in the tunnel barriers (Fig. 4.30(b)). The dominant source of noise in our device is therefore fluctuations in the dot potential.

Using the fit in Fig. 4.30(d), it is possible to translate the conductance noise to an equivalent deviation in the dot potential (we simply divide by the slope of the fit). The



(a) Noisy Dot

(b) Noisy Barrier

(c)

(d)

(e)

(f)

Figure 4.30: Differentiating between noise in the dot potential and tunnel barriers. (a) CB profile in the presence of noise in the dot potential. (b) Modelled CB profile in the presence of fluctuations in the barrier transparency. (c) Experimental CB sweep taken as a function of time. (d) Translation of the CB time sweep in (c) to the equivalent dot potential. (e) Extracting the fluctuations in the dot potential as a function of time. (f) Probability distribution of the dot potential.

implied deviation in the dot potential is shown in Fig. 4.30(e), which shows that the noise is uniform up to $\sim 1.5hrs$. Beyond $1.5hrs$ the (constant) background noise, which grows because we scale by the inverse of the fit slope, swamps any fluctuations caused by the dot potential. We show the probability distribution of $\Delta\mu_d$ in Fig. 4.30(f), calculated from Fig. 4.30(e) up to $\sim 1.5hrs$. Here we see the fluctuations in dot potential are Gaussian distributed, with a standard deviation of $\sigma = 0.034meV$. Since the fluctuations are Gaussian in nature, we may attribute the noise to a multitude of uncorrelated charging events [57, pg. 420].

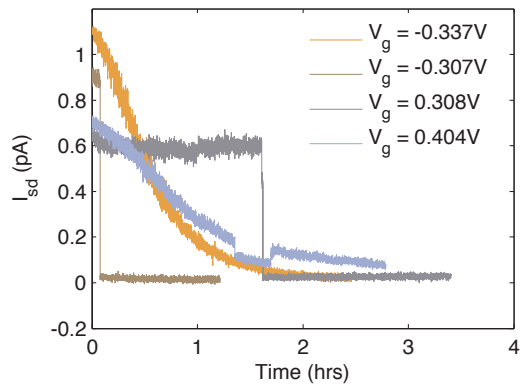
Using the method described in this section, we are now equipped with a means of quantifying the charge noise in our SET, which we address in the next section as a function of the gate potential at different temperatures.

Measuring fluctuations in the dot potential

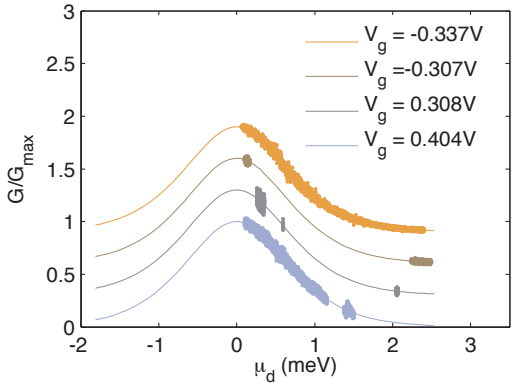
We saw in the previous section that noise in STM-patterned SETs is dominated by fluctuations in the dot potential, where these fluctuations have a Gaussian distribution, implying that they are caused by many uncorrelated fluctuators. To further isolate the source of these fluctuations, here we study the SET noise in detail, focussing on the influence of the gate voltage and device temperature. For this we have taken several time sweeps similar to that of Fig. 4.30(c) on different Coulomb blockade peaks, as shown in Fig. 4.31(a). Since we consider different CB peaks, each sweep has a different starting current and consequently, each trace has a different signal to (background) noise ratio. The peaks were chosen to coincide with the regions labelled 'a', 'b', 'd', and 'e' in Fig. 4.26(c) to provide further information about the switching events.

First, let us describe why these traces have such different shapes: As a consequence of rapidly driving the gate voltage from $-0.5V < V_g < 0.5V$ for many hours during the switching study, and then ramping the gate to the voltage used for the first trace ($V_g = 0.404V$), we observed considerable drift throughout the first measurement. We see a random telegraph switch at $2hrs$, which lasts for $45min$. This switch magnitude ($\Delta\mu_{d:Trap} = 0.5meV$), is consistent with the switching study (Fig. 4.25(b)) indicating that the observed switching events has a transient random telegraph nature.

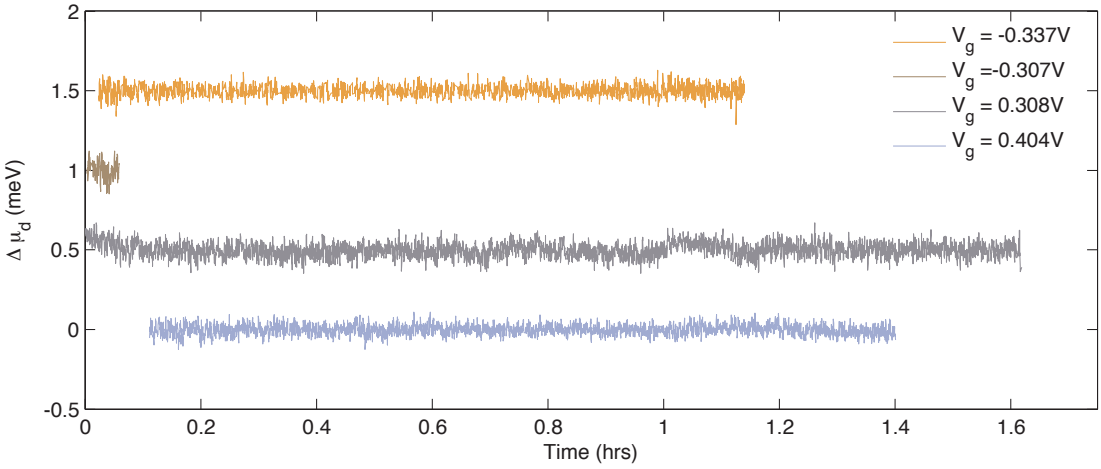
Next we moved the gate to $V_g = 0.308$, which was close enough to the first gate voltage that we initially saw very little drift; then at $\sim 1.6hrs$ the dot undergoes a severe switch, taking it into what appears to be full blockade. The magnitude of this switch is again consistent with that witnessed in the switching study (Fig. 4.25, $\Delta V_{g:Trap} > 10mV$). The move to the next peak ($V_g = -0.337V$) was a very large step in gate voltage, and



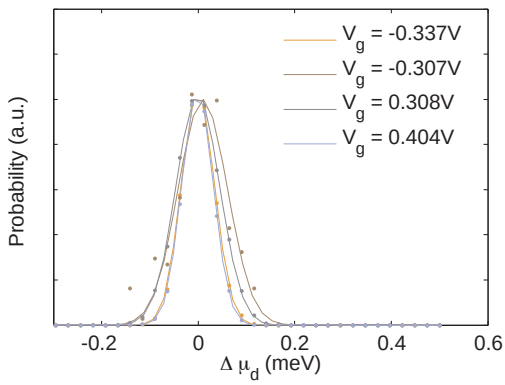
(a)



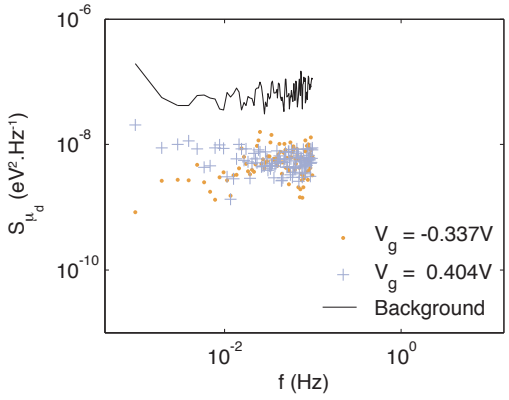
(b)



(c)



(d)



(e)

Figure 4.31: Conductance noise of the in-plane gated SET at 4K. (a) Measured SET current with time for four different gate voltages showing noise in the current. (b) Mapping the time series data in (a) to the equivalent dot potential. (c) Using the trace in (b) to extract the dot potential as a function of time. (d) Probability distribution of the dot potential at each gate voltage from (c). (e) Power spectral density of (c) calculated for each time sweep.

Table 4.3: Standard deviation of dot potential compared over the gate voltage range at base temperature and 4K. (a) Results form $4K$ study shown in Fig. 4.31. (b) Base temperature results shown here for comparison, which are discuss later in this section.

(a) $4K$		(b) Base	
V_g (V)	σ_{μ_d} (meV)	V_g (V)	σ_{μ_d} (meV)
0.403	0.032	0.373	0.026
0.308	0.045	0.232	0.023
-0.307	0.034	-0.282	0.028
-0.337	0.051	-0.425	0.015

consequently we again see severe drift in this trace. The final trace ($V_g = -0.307V$) shows minimal drift because it was such a minor change in gate voltage. This final trace undergoes a severe switch within 5–10min, going into full blockade.

Using the method discussed in the previous section, we can map the current to the dot potential. We show this mapping in Fig. 4.31(b). Here we have forced all traces to use the same drift time constant ($\tau = 1.9hrs$) and temperature ($T = 4.2K$); allowing only the magnitude of the switch in μ_d to change, and the magnitude of the drift Δ_{mag}. We assume that the drift restarts after a switching event. Again, the difference between the ideal and measured curve gives a measure of the conductance noise, from which we can calculate the noise in the dot potential using

$$\Delta\mu_d = \left(\frac{G_{Exp} - G_{Fit}}{G_{max}}\right)\left(\frac{dG_{Fit}/G_{max}}{d\mu_{d:Fit}}\right)^{-1} \tag{4.23}$$

When performing this calculation, we neglect all points outside of $0.1meV < \mu_d < 1meV$, since the peak becomes flat outside of this region and the background noise dominates over any noise in the dot potential. Whilst this is fine for most traces it does not leave many viable data points for the $V_g = -0.307V$ trace. The result of converting from fluctuations in conductance to fluctuations in the dot potential is shown in Fig. 4.31(c). The traces have been offset by $0.5meV$ in the y-axis for clarity. The most striking feature of this figure is that, despite the obvious variations in current between successive time sweeps, and the conditions under which they were recorded, the fluctuation in dot potential are remarkably similar. To demonstrate this quantitatively, we show the probability distribution of each

trace in Fig. 4.31(d). The standard deviations of each trace are tabulated in Table 4.3(a). The fits of $V_g = 0.404V$ and $V_g = -0.337V$ take up a wide range of μ_d values because of the inherent drift, and consequently these two traces give a more reliable conversion from ΔG to $\Delta\mu_d$. The resultant probability distribution functions of these two traces are very similar, despite being at the two extremes of the studied gate voltage range; their standard deviations differ by only ∼5%. Based on this result, we conclude that the magnitude of the fluctuations in dot potential varies little within the studied range of gate voltage at $4K$. To further understand the nature of the fluctuations in dot potential, we can look at the power spectral density (PSD) of these fluctuations.

The power spectral density of a signal is a measure of the component of that signal's power that occurs at a given frequency. Mathematically, the power spectral density is calculated from the Fourier transform of the autocorrelation function of the signal, as described in greater detail in Sec. 2.5.3. As mentioned in the introduction to this section, we expect the power spectral density of the noise in an SET to have a $1/f^{\alpha}$ frequency dependence, where $1 < \alpha < 2$ is determined by the dominance of discrete switching events. Figure 4.31(e) shows the power spectral density of the dot potential versus time traces shown in Fig. 4.31(c). For clarity we have included only the $V_g = 0.404V$ and $V_g = -0.337V$ traces in this figure—where we have the most data points—but the PSD of the $V_g = -0.307V$ and $V_g = 0.308V$ sweeps are qualitatively identical. In addition, we also estimate the background noise by plotting the power spectral density of the $V_g = -0.307V$ trace for $\mu_d > 1meV$, where we expect fluctuations in the dot potential to be dominated by the background noise. We see in Fig. 4.31(e) that all of the PSD curves are essentially flat over the frequency range shown, with only a slight upturn at the low frequency points; there are not enough points at these lower frequencies to reliably confirm any frequency dependence in the power spectra. Note that even the 'background' trace turns up at low frequency, reflecting the fact that it includes $1/f$ noise arising from the dot, which should dominate at low frequencies. We conclude therefore that the measurements shown here are largely dominated by frequency-independent background noise. As further evidence of this claim, we note that the average PSD of each curve is inversely proportional to the starting current of the respective time series, which occurs because we normalise the background noise to the starting current and thus reduce the effective contribution of the constant background noise signal.

Figure 4.32 shows a set of time sweeps taken at the base temperature of the dilution refrigerator. At these temperatures, the magnitude and location of the CB peaks has changed (e.g. see Fig. 4.25(a) cf. Fig. 4.27(a), where there is an average reduction in the peak current of ∼6 times and shift in the peak location of $\sim 60mV$). To get reliable

measurements, we therefore had to change the gate voltages used to record the time series data, but we kept them as close as possible to the measurements taken at $4K$. The current traces recorded at base temperature ($\sim 550mK$ on this fridge) are considerably noisier than their $4K$ equivalents. This is because of the change in the shape of the Coulomb blockade peak at this temperature; as the peak becomes sharper we see greater current fluctuations for a given change in the dot potential. We show the conversion of these sweeps to the equivalent fluctuations in the dot potential in Fig. 4.32(b), and the equivalent μ_d versus time traces in Fig. 4.32(c), where we have used a time constant of $\tau = 23.9hrs$ to fit the experimental drift. Figure 4.32(d) shows a histogram of the dot potential fluctuations for each of the gate voltages used. Again, we see Gaussian-distributed curves, with standard deviations independent of the gate voltage (tabulated in Table 4.3(b)); though here the curves show consistent side-lobes, indicative of many discrete switches in the dot potential.

When we plot the power spectral density of these base-temperature sweeps, we see a much clearer relationship with frequency, with the signal power dropping off in proportion to $1/f^{1.8}$. This indicates that the noise at this temperature is not dominated by frequency-independent background noise. This is likely a consequence of the background noise being thermally activated, indicating that it is Johnson noise (which scales in proportion to kT). As a consequence, here fluctuations in the device current are dominated by fluctuations in the dot potential. Furthermore, because the Coulomb blockade peaks are much sharper at base temperature than at 4K — giving large current fluctuations for a given change in the dot potential — any background fluctuations in the device current are less visible at this temperature. The exponent of the frequency dependence in the power spectral density (-1.8) is indicative of fluctuations caused by random telegraph switches in the time trace, as seen in the work of Zimmerman *et al.* [200]. We see these small-scale switches in Fig. 4.32(c). The frequency dependence of all traces consistently begins at a corner frequency of 2–$3mHz$, which is the characteristic frequency of the random telegraph switching, below this frequency the power spectral density is approximately flat.

To compare the noise characteristics of our device with those published by Zimmerman *et al.* we have tabulated the noise characteristics of each in Table 4.4. We show the base temperature results from this chapter, where we have scaled from fluctuations in the dot potential to fluctuations in the dot charge (S_{μ_d} to S_{Q_d}) by dividing by the square of the charging energy ($E_c{}^2$). We note that the power spectral density quoted here at $1Hz$ is a

[2]Note: Zimmerman *et al.* chose this sample because it was 'unusually noisy'. We have converted from the stated noise amplitude supplied in this paper in units of pA to units of e using the CB sweep of Fig.1(a) of this reference.

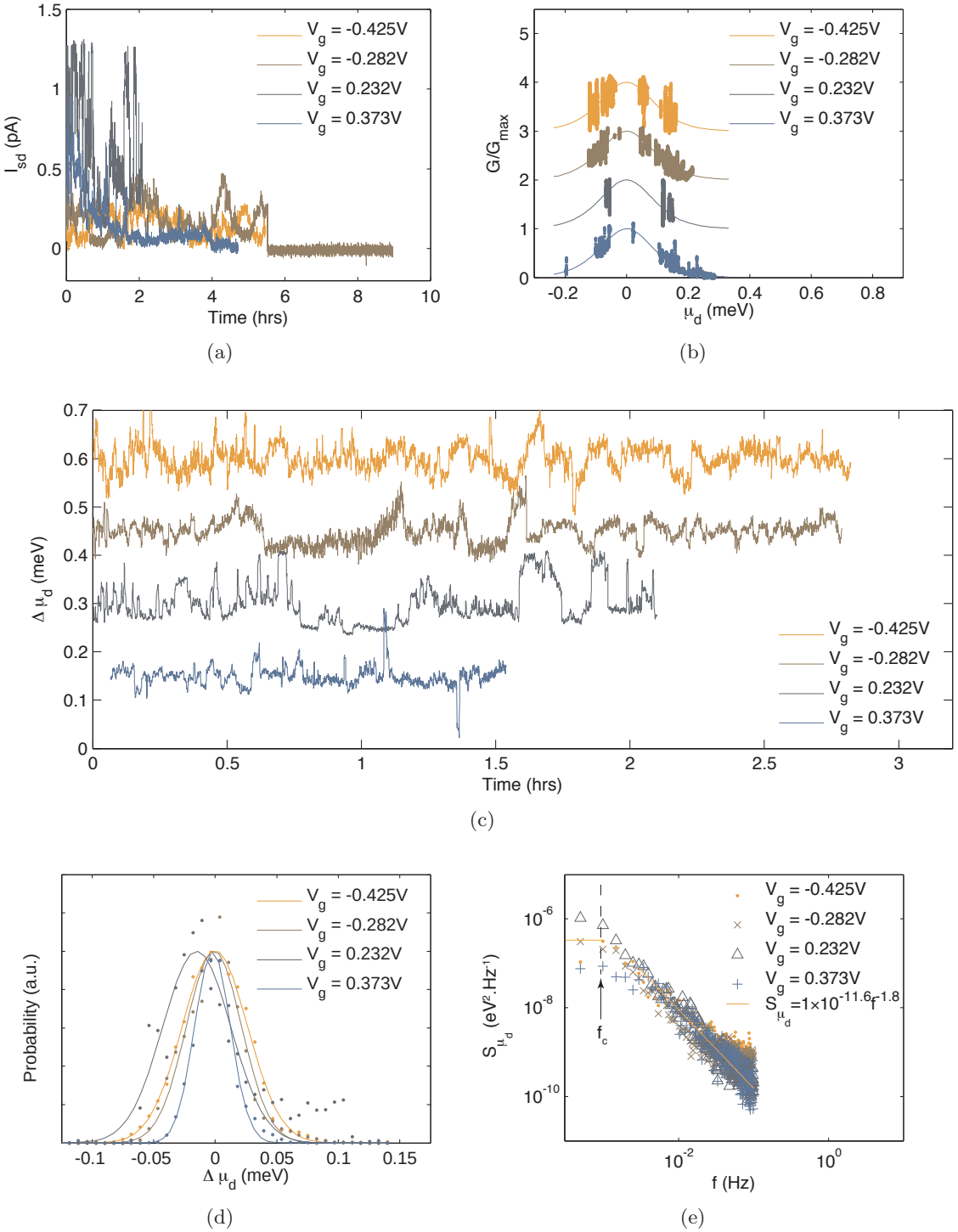


Figure 4.32: Conductance noise of the in-plane gated SET at base temperature. (a) Measured SET current with time for four different gate voltages showing noise in the current. (b) Mapping the time series data in (a) to the equivalent dot potential. (c) Using the trace in (b) to extract the dot potential as a function of time. (d) Probability distribution of the dot potential at each gate voltage from (c). (e) Power spectral density of (c) calculated for each time sweep.

Table 4.4: Comparing the noise performance of our in-plane gated device with literature. Here we show the standard deviation (σ_{Q_d}), power spectral density at $1Hz$ (S_{Q_d}), corner frequency of the power spectral density curve (f_c) and the slope of its roll-off (α where $S_{Q_d} = A/f^{\alpha}$) relative to Al-based SETs and Si-MOS based SETs measured by Zimmerman *et al.*

Architecture	σ_{Q_d} (e)	S_{Q_d}@1Hz ($e^2.Hz^{-1}$)	f_c (Hz)	α	Ref.
Al	∼0.2	∼0.03	1×10^{-2} to 5	∼2	[205][2]
Si-MOS	0.015	3×10^{-8}	∼7	∼2	[209]
Si:P	∼0.002	3.1×10^{-8}	$\sim 3 \times 10^{-3}$	1.8	This work

strong function of the corner frequency of the RTS spectrum[3]. A fairer comparison can be derived by calculating the integral of the power spectra, but this data is typically not given in the cited references. Based on the σ_{Q_d} and S_{Q_d} of our device, we expect the integrated noise power of our device to compare favourably to Zimmerman's Si-MOS sample.

In a later paper [209] Zimmerman highlights that Si-MOS SETs are consistently less noisy than aluminium SETs — at least in terms of low frequency charge fluctuations. From this comparison, we therefore conclude that the noise performance of our device appears equal or better than the Si-MOS based SETs of Zimmerman *et al*, which are among the best noise results of published SETs.

4.5.3 Possible sources of traps in STM patterned SETs

It is interesting to consider what might cause traps near the STM-patterned dot. In the fabrication process we have used, traps may be introduced from:

Random dopant incorporation due to incomplete hydrogen passivation: If the starting surface was not perfectly terminated, it might be possible for a PH_3 fragment to bind to any un-terminated regions in the resist. However we know that such depassivated regions would have to be at least three dimers in area for a P atom to incorporate into the surface [179]. We imaged the surface before patterning to ensure that the surface was fully terminated and so we can rule this out.

[3]For comparison, our peak PSD is $S_Q = 5.4 \times 10^{-3} e^2.Hz^{-1}$, compared to the Si-MOS sample of Zimmerman *et al.* where the peak is $S_Q = 3 \times 10^{-8} e^2.Hz^{-1}$, but the two were measured over different frequencies

Stray/unintentional desorption during STM lithography: Given the finite line width of the STM desorption process, it is possible that the surrounding regions of the STM-patterned area may be unintentionally desorbed. Again though, this only really remains an issue if three or more dimers are exposed. Whilst there is nothing to indicate this condition in the STM image of Fig. 4.11(b), it is not possible to completely rule this out for the regions around the large contact patches while patterning the source, drain, or gate extensions.

Surface diffusion of adsorbed donors during incorporation: Since the tunnel-coupled trap in this device is so strongly coupled to the drain, we expect it to be physically close to it. The incorporation of a spurious dopant might occur from a small amount of surface diffusion during the $350°C$ incorporation anneal if the hydrogen resist nearby was incomplete. This is unlikely however, as it would require the resist to be significantly compromised without the exposed regions being doped with PH_3 during the dosing process. We consider this case extremely unlikely.

Nearby substrate dopants: The silicon substrate is lightly doped to $\sim 5 \times 10^{15} cm^{-3}$ with phosphorus. During the high temperature anneal used to reconstruct the surface, phosphorus is known to evaporate form the surface [210]. However a substrate doping density of $10^{15} cm^{-3}$ corresponds to one dopant on average within a radius of $62nm$ from the dot, making this a statistically likely cause of switching events in this device.

Traps at the Si–SiO_2 interface: The $\sim 20nm$ of MBE-grown Si deposited on top of the STM-patterned device will form a native oxide at its surface once exposed to the ambient. This interface is known to have dangling bonds that act as traps with a density of $N_{it} = 10^{12} cm^{-2}$, spacing them on average $10nm$ apart. When combined with the vertical $20nm$ separation, interface traps are therefore likely to be within the vicinity of the device, but they are unlikely to be strongly coupled to the dot or drain.

Given the density of substrate dopants, the probable cause of the strongly tunnel-coupled trap and switching events is statistically likely to be the result of substrate dopants. Indeed, Ferguson *et al.* have shown that the degree of switching increases with increased substrate doping [202], so it is expected that substrate dopants will affect our devices. From this analysis though, we expect traps at the interface with the native oxide to dominate drift and charge noise.

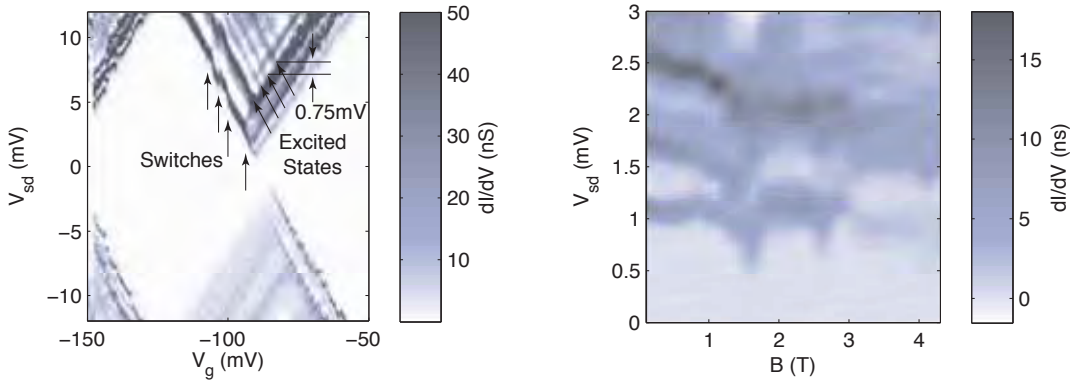


Figure 4.33: Studying the excited states of the in-plane gated SET in a parallel magnetic field at 260mK. (a) The excited state lines are clearly visible when we look in high resolution on a single transistion. (b) We can study the nature of the excited state lines by measuring how they evolve in a magnetic field. The measurement was plagued by constant switches in the dot potential shown by the arrows in (a).

4.6 Magnetic field dependence of the excited states within the in-plane gated SET

We have shown that some of the excited state features observed in the transport stability diagram of this dot are due in part to a tunnel coupled trap. To study these features in greater detail, we analyse how their location evolves under the application of a magnetic field. We show the excited state lines in detail for a single transition in Fig. 4.33(a). If the lines in the stability plot are due to spin degenerate excited states on the dot (e.g. confinement levels or orbital excited states), we would expect the excited state lines to split in a magnetic field due to the Zeeman effect by $2E_z = s_z g \mu_B B$, where E_z is the shift in energy of a given spin-state, $s_z = 1/2$ if the spin of an electron, $g \simeq 2$ is the g-factor for an electron in silicon, μ_B is the Bohr magneton and B is the magnetic field. If the excited states are due to the density of states of the leads, we expect the excited state lines to move from the ground state by an amount E_z (i.e. half of the Zeeman splitting), and for these features not to split in the magnetic field [211]. If the features are due to valley excited states, we expect that these states will move relative to one another in the magnetic field, with spin up and spin down electrons filling the available states according to Hund's rule — resulting in a complex evolution of the excited state lines [48]. As we calculated in Sec. 2.5, it is plausible that we will see orbital excited states ($\Delta E \simeq 1meV$), valley excited states ($\Delta E \simeq 100\mu eV$), and sharp density of states in the leads ($\Delta E \simeq 7meV$) within our

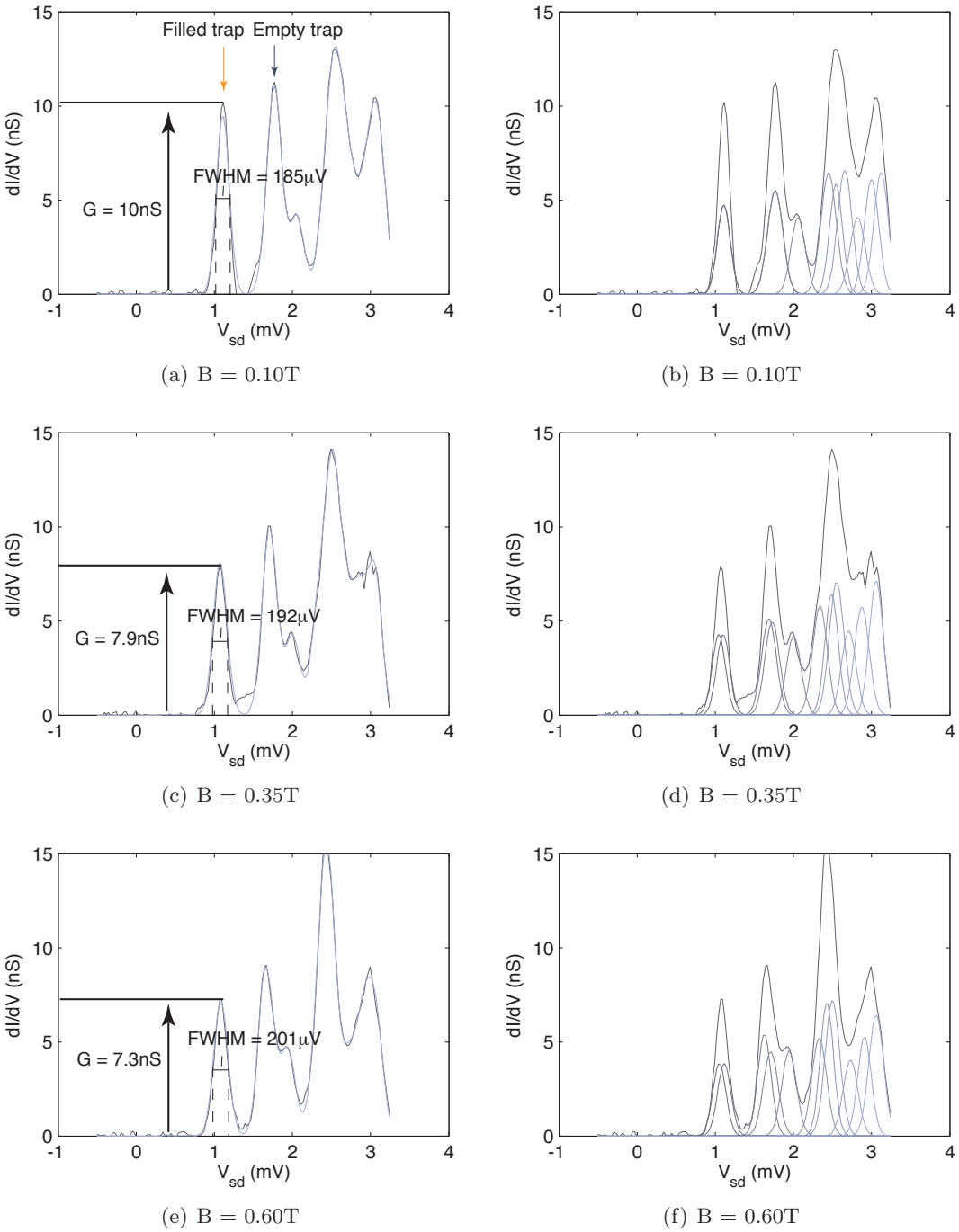
dot.

We have studied the evolution of the excited state spectra under an applied parallel magnetic field in Fig. 4.33(b) for a single cut through the map at $V_g = -166.9mV$. While there is a visible trend in the location of the resonances with B, the measurement is plagued by switching events. Up to $B = 0.8T$ the data seems relatively unaffected by switches (Fig. 4.35(a)), but here the degree of peak splitting is smaller than the line-width of the resonant features, because of thermal broadening of the electron energy. However, we can see the peaks evolve in this narrow range of fields ($0T < B < 0.8T$) by studying a line trace of each V_{sd} sweep in greater detail.

Figure 4.34 shows line traces of the differential conductance at three different fields ($B = 0.1,\ 0.35,\ 0.6T$). Since the dot is in the thermally-broadened regime under these conditions, we expect the excited states to be thermally broadened [150]. We can therefore fit each line trace with many such peaks of equal temperature, $T \leq 300mK$ (the fit is shown in light blue in the figures in the left column). We show the constituent peaks in the right-hand column. Here we have tried to maintain a reasonable variation in the relative conductance of each excited state ($\sigma_{ES} = 5 \pm 1.5nS$). Using this method we can accurately fit each line trace. We have to be careful when fitting the data around the sharp discontinuities in the $B = 0.35T$ trace at $V_{sd} = 3mV$ though, since this is more likely to be measurement or switching artefacts than the true excited state structure. We can see from this line-trace analysis that the peaks at $V_{sd} = 1.1mV$ and $V_{sd} = 1.8mV$ decrease in magnitude and increase in width with magnetic field, indicating that what appeared to be a single excited state with a conductance of $\sim 10nS$ was in fact two or more coincident states that have different magnetic field dependences (e.g. different spins). Further support for this is that the side-lobe at $V_{sd} = 2mV$ with conductance $\sim 5ns$ clearly moves to lower V_{sd} values at higher fields. Conversely, the peak at $V_{sd} = 2.6mV$ increases in magnitude with field, indicating that multiple states here are starting to merge.

Despite the fact that the device constantly switches during the magnetic field sweep, we can still assess the peak splitting of two closely spaced peaks. If the peaks are indeed simply split via the Zeeman effect, they should not move relative to one another following a switching event. In Fig. 4.35(b) we plot the splitting between the two states that we assert make up the $V_{sd} = 1mV$ peak. The trend line included in this figure labelled 'theory' is what we expect for Zeeman splitting[4] with a g-factor of 2. The point at $0.1T$ was set to $\Delta\mu_d = 0$ in the fitting process since this was our lowest field data point. Despite uncertainties introduced by the peak fitting process, the low resolution of this

[4]Note we translate from ΔV_{sd} to $\Delta\mu_d$ using the relation $\Delta\mu_d = \Delta V_{sd}\frac{C_D}{C_\Sigma} \simeq \frac{1}{2}V_{sd}$ since we have taken these traces at constant V_g.



(a) B = 0.10T (b) B = 0.10T

(c) B = 0.35T (d) B = 0.35T

(e) B = 0.60T (f) B = 0.60T

Figure 4.34: Decomposing the differential conductance into individual excited states. When we apply a magnetic field, the peaks at $V_{sd} = 1mV$ and $1.75mV$ reduce in magnitude and increase in width, indicating that they are beginning to split.

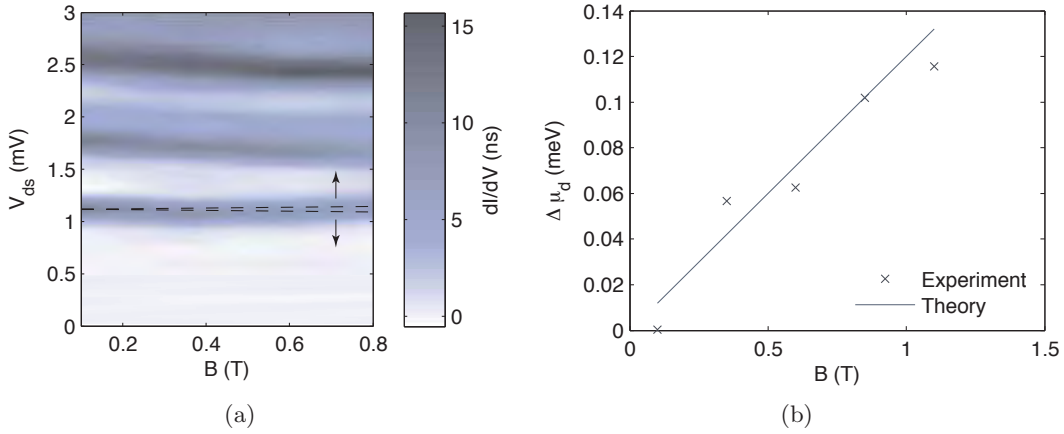
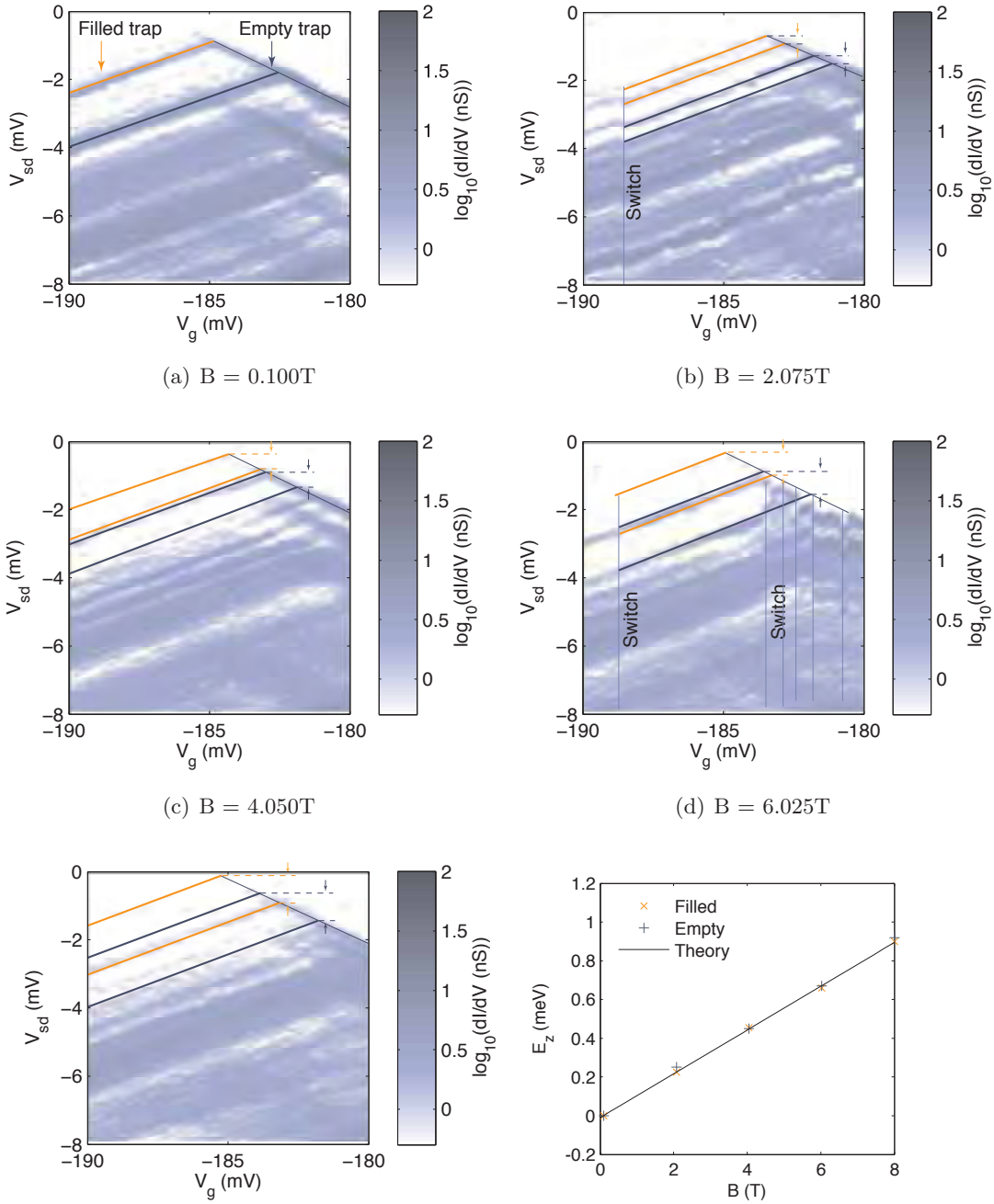


Figure 4.35: Assessing the magnetic field dependence at low fields. (a) Up to $B = 0.8T$ the switching is not as severe, and here we can see clear trends in the excited state lines with magnetic field. (b) By fitting thermally-broadened peaks to the differential conductance, we find the peak at $V_{sd} = 1mV$ Zeeman splits with $g = 2$.

measurement in the V_{sd} axis due to thermal broadening, and the obvious switching present in this measurement, we find good agreement between the experimental and theoretical trends. This would imply that the excited states we see are not due (solely) to variations in the density of states of the leads, which should not move at a constant V_g with an applied magnetic field [211]. In addition, there are clearly a multitude of peaks within the cluster at $V_{sd} = 2.5$–$3.5mV$, some of which may be stationary peaks. We also see one isolated peak at $V_{sd} = 2mV$ that moves in field without any clear splitting (changes in magnitude or width), it is likely a valley-split state. This is because valley split states should fill according to Hund's rule, which makes it favourable for electrons of a given spin to load the dot [48]. That is, this state at $V_{sd} = 2mV$ is only accessible to, say, spin up electrons. These results indicate that the excited states of this dot are caused by multiple different mechanisms.

To ensure that we are seeing Zeeman splitting, we took a stability map at several fields, as shown in Fig. 4.36. By taking a complete map of the transition, we can isolate Zeeman splitting of the excited state lines from drifting or switching of the dot potential. In this experiment, we can clearly see the ground state and first excited state visible at $B = 0.100T$ split at $B = 2.075T$. At $B = 4.050T$ we see the splitting double in magnitude, then at $B = 6.025T$ and $B = 8.000T$ we see the spin-split ground state and excited state lines cross. When we plot the spin-splitting as a function of magnetic field Fig. 4.36(f), we see the splitting of the ground state almost perfectly match the theoretical expectation for $g = 2$ (solid line).



(a) B = 0.100T

(b) B = 2.075T

(c) B = 4.050T

(d) B = 6.025T

(e) B = 8.000T

(f)

Figure 4.36: Searching for Zeeman splitting of the coupled trap. Here we map the splitting of the filled (orange) and empty (blue) states with magnetic field, with the original data in (a) to (e) and the plotted splitting in (f), showing clear evidence of Zeemen splitting of the first two resonances.

Now, from our analysis of tunnel coupling between the dot and a trap, the 'excited state' line seen here actually corresponds to a shift of the dot ground state as the tunnel-coupled trap empties. That is, it is transport through the ground state of the dot replicated in the stability plot by the filling of the nearby trap. As such, the splitting of the first two resonances in a magnetic field is not evidence of orbital or confinement excited states within the dot, since this is not a true excited state. We do not resolve any true excited state features that clearly split with magnetic field. If we refer this model back to the line trace excited state decomposition of Fig. 4.34, there we can also only clearly see the first and second peak (i.e. the ground state with a filled and empty trap, respectively) split in a magnetic field. There is therefore no clear evidence of splitting of excited states, though we can say that the ground state must be spin degenerate.

4.7 Chapter summary

In this chapter we described the design, fabrication, and analysis of a ∼200 donor in-plane gated, STM-patterned SET. The finished device had a line edge roughness of a single dimer with tunnel gap dimensions of $5.4nm \times 12.5nm$. Using FastCap capacitance modelling and the single electron transport modelling program SIMON, we modelled the device capacitance and conductance and found them in excellent agreement with our experimental data; for example, we calculated a theoretical charging energy of $E_c = 13.6meV$ and measured $E_c \simeq 13.5meV$ experimentally. At milli-Kelvin temperatures we observe excited states in the transport spectroscopy, separated in energy by $100\mu eV$–$750\mu eV$, consistent with the excited state features of STM-patterned SETs published by both Fuhrer [22] and Füchsle [23]. We observed clear evidence of spin splitting via the Zeeman effect in a magnetic field, but noticed that not all peaks split, indicating both the presence of valley splitting within the dot and states due to transport through the 1-D source and drain leads. This is consistent with previous reports where the high donor density in these planar STM-patterned $Si{:}P$ δ-layers caused electrons to occupy both the Γ and Δ bands of the δ-doped band structure so that the abrupt lateral confinement of the dopants caused valley splitting of the Δ bands, giving rise to energy separations down to $100\mu eV$, as observed in our device.

In addition to the observed periodicity in the Coulomb diamonds (differential conductance versus source-drain and gate voltages) we also saw additional diamonds offset in gate space. We were able to replicate these features using numerical modelling, assuming the presence of a tunnel-coupled trap near the SET. In particular we were able to match

the excited state energy levels and apparent opening of the Coulomb blockade diamonds at low V_{sd}.

For comparison with the UHV-oxide gated SET described in the next chapter, we measured the drift of the Coulomb blockade peak position, which we found to be thermally activated with an activation energy of $47\mu eV$, arising from thermal activation of nearby traps. We also studied the presence of switching in the Coulomb blockade peaks position, which we attribute to the presence of capacitively coupled background dopants in the substrate. The number and severity of these switching events dropped considerably when the sample was cooled from $4K$ to base temperature, resulting in only one visible switch at milli-Kelvin temperatures.

When we studied conductance noise of the SET, we found the source of the noise to most resemble fluctuations in the dot potential, attributed to interface traps or background dopants within the substrate. In studying this noise over a range of gate voltages and at $4K$ and base temperature, we found no correlation between the noise characteristics and the gate voltage, but the frequency-independent Johnson noise reduced at base temperature, lowering the mean noise power over the measurement bandwidth. This revealed a frequency dependence in the power spectral density of the noise at base temperature, proportional to $1/f^{1.8}$, indicating the presence of both discrete trapping events causing RTSs in the signal, and $1/f$ noise caused by many weakly coupled fluctuators. We found a standard deviation in the charge noise of $\sigma_{Q_d} = 0.002e$, which is comparable to silicon MOS based SETs studied by Zimmerman *et al.* [209]. These results demonstrate that we can make a planar SET with an $E_c = 13.5meV$ with very low charge noise. This device will be used in the comparison between in-plane gated SETs and the surface-gated devices discussed in the next chapter (Chapter 5).

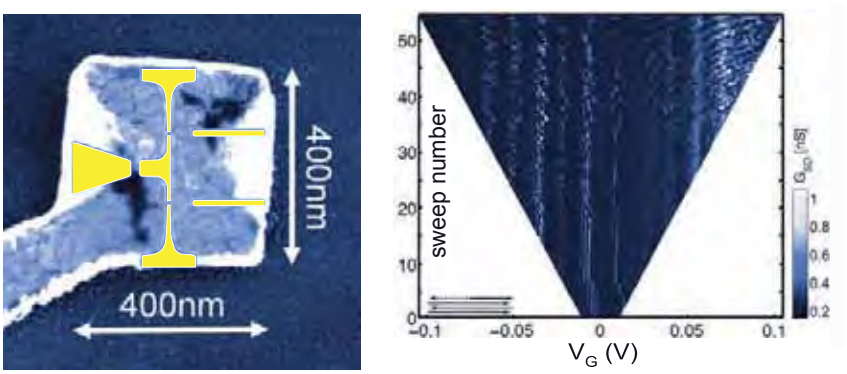
Chapter 5

Fabricating Surface Gated STM-Patterned SETs

In the previous chapter we demonstrated an atomically abrupt, highly phosphorus doped ∼200 donor single electron transistor in silicon. In this chapter we integrate the UHV compatible low-temperature oxide developed in Chapter 3 into the STM-fabrication process to form surface gates on a ∼200 donor STM-patterned SET. We then characterise its electrical performance and compare it systematically with the all-epitaxial SETs presented in Chapter 4. In particular, we address the gating range and the presence and severity of noise, hysteresis, and switching. From this study we make recommendations about the use of surface gates in future STM-patterned devices.

5.1 Introduction

In his original article describing a $Si{:}P$ solid-state quantum computer, Kane suggested using surface gates on either SiO_2 or $SiGe$ to control the location and overlap of electrons bound to the phosphorus nuclei for qubit control [10]. To this end, we have developed a low temperature strategy to fabricate atomically abrupt $Si{:}P$ devices with surface gates aligned to the buried STM patterned $Si{:}P$ device. We have chosen to use single electron transistors to compare the behaviour of surface gates with all-epitaxial in-plane gates, since SETs behave as very sensitive electrometers. Single electron transistors are used in quantum electronic circuits to sense the occupancy of an electronic state; for example, to act as charge sensors for the readout of spin-qubits using spin-to-charge conversion schemes [144, 212, 213]. However, for an SET to be used in such applications, we must first be sure that it is sensing the intended electronic state, and not the surrounding substrate or fluctuations within the SET itself. This noise in the SET readout may result from a number of sources including thermal fluctuations in the distribution of charge, shot noise arising from discrete electron tunnelling events [214], and charge noise resulting from changes in the occupancy of nearby crystal defects, impurities, or traps [197, 202]. For this reason, it is important to quantify the magnitude and type of noise present within



(a) (b)

Figure 5.1: Stability of a native oxide surface gated 4000e quantum dot from Fuhrer *et al.* [22]. (a) SEM image of the surface gate placed over the buried STM patterned device (on the native oxide and $\sim 20nm$ encapsulation layer). The shape of the STM-patterned device is overlayed in yellow in the SEM image (b) Conductance of the device (colour scale) over successive gate sweeps (vertical axis) with an increasing gate range (horizontal axis), showing a significant increase in the degree of switching/hysteresis as the gate range is extended.

an SET. In this chapter we characterise a single electron transistor with a surface gate on top of the UHV oxide developed in Chapter 3, and quantify the noise in this surface-gated device. Finally we highlight the comparative advantages of surface gates and all-epitaxial in-plane gates.

5.2 Surface-gating STM-patterned SETs via the native silicon oxide

Our group made the first STM-patterned nano-scale $Si{:}P$ device in 2004. Following this result we have created many devices [22, 23, 60–64], leading to a single electron transistor using the native silicon oxide as a dielectric, published in 2009 [22]. In parallel, as part of this thesis we have developed a UHV oxide and incorporated it into both simple tunnel gap devices [168] and more recently into an SET architecture [215]. In this chapter we describe the first surface-gated device using the native silicon oxide as a dielectric, made by Fuhrer *et al.* [22], and then the first surface-gated SET that used the low temperature silicon dioxide from this thesis as a gate dielectric. In order to directly compare the impact of the low temperature dielectric on the device performance, we then present the results of a very similar SET to that described in Chapter 4, but with surface gates patterned on

the low temperature dielectric.

5.2.1 Many electron (4000e), surface gated STM-patterned SET using the native silicon oxide

The $4000e$ SET fabricated by Fuhrer *et al.* described in the previous chapter was made using STM-patterned in-plane gates. After fully characterising the device at milli-Kelvin temperatures using these in-plane gates, an overall $400 \times 400nm$ surface gate was added to the device aligned over the buried SET, using the native oxide on the silicon encapsulation layer as a dielectric (see Fig. 5.1(a)). This native oxide has a high density of interface traps ($> 10^{12}.cm^2$), and Fuhrer *et al.* found the surface gate formed in this way to be generally unstable, showing enhanced switching and hysteresis in the gating action. Each switch was found to 'activate' once the surface gate was swept beyond a threshold voltage, so that sweeping the gate back and forth across a successively wider range generated greater instability in the Coulomb blockade sweep. This is illustrated in Fig. 5.1(b); as the swept range increased (proceeding vertically upwards through the diagram), the peak locations became increasingly unstable. This increased instability was often irreversible within a given cool-down of the device. Furthermore, the surface gate showed hysteresis in the gating action of $\sim 0.30e$. Fuhrer *et al.* attributed this instability and hysteresis in the device to the change in the occupancy of charge traps once the applied gate field exceeded a threshold value (on the order of $0.02MV.cm^{-1}$).

The capacitance between the surface gate and the dot was much higher than the in-plane gate ($C_{TG} = 64aF$ cf. $C_{PG} = 13.2aF$), illustrating the geometric advantage of the parallel-plate surface-gate geometry over the adjacent-plane geometry of in-plane gates. This allowed the dot occupancy to be changed by $\sim 500e$ using the surface gate, compared with the $\sim 50eV$ using the in-plane gate. This device therefore demonstrated the potential advantages of surface gates over in-plane gates in terms of gate range, but the instability and hysteresis introduced using the native oxide as a dielectric highlighted the superior stability of the in-plane gating scheme. In parallel with this experiment, as part of this thesis we developed a process to form a low temperature silicon dioxide layer as a gate dielectric, under controlled UHV conditions with minimal contamination, rather than forming a native oxide as a dielectric on the device.

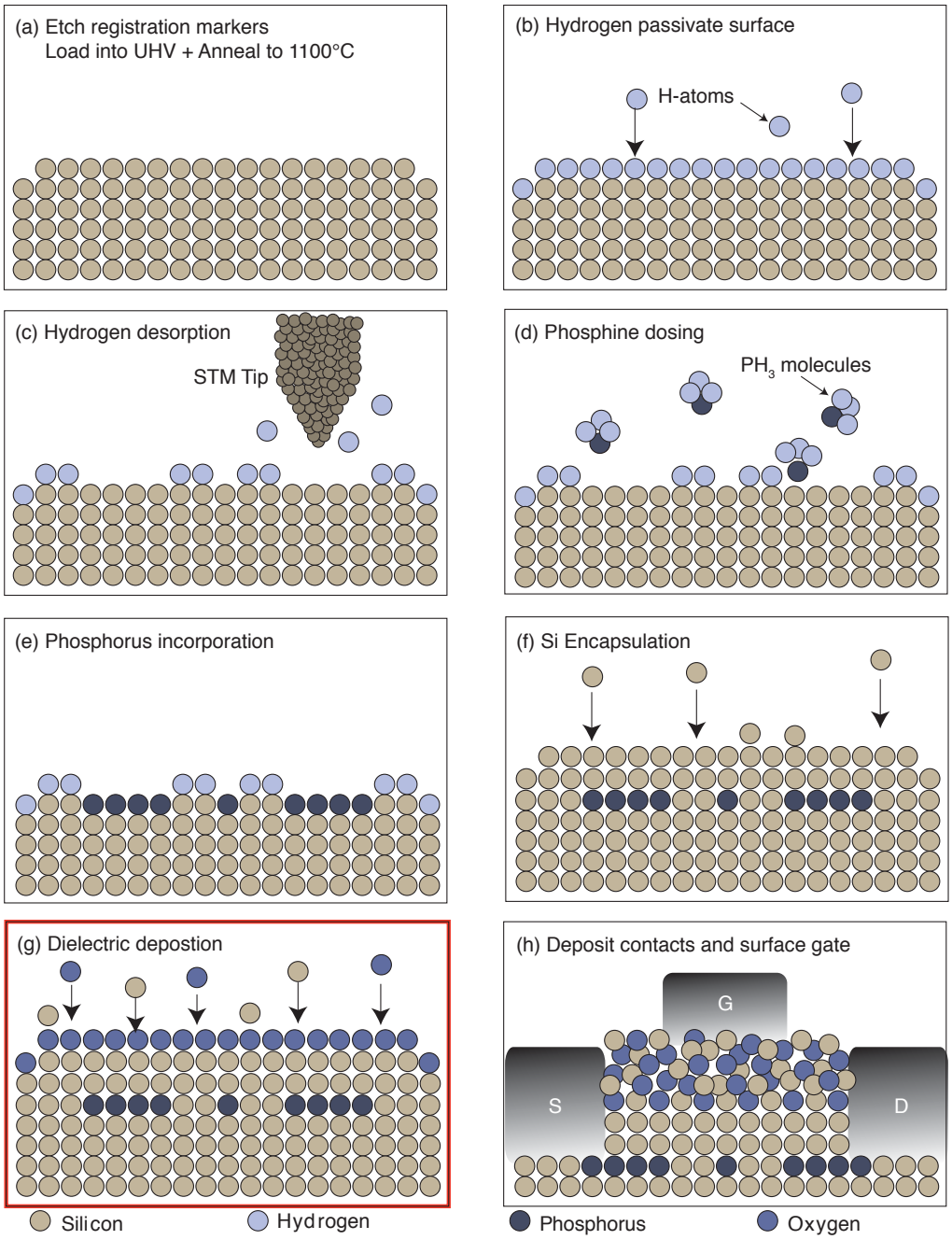
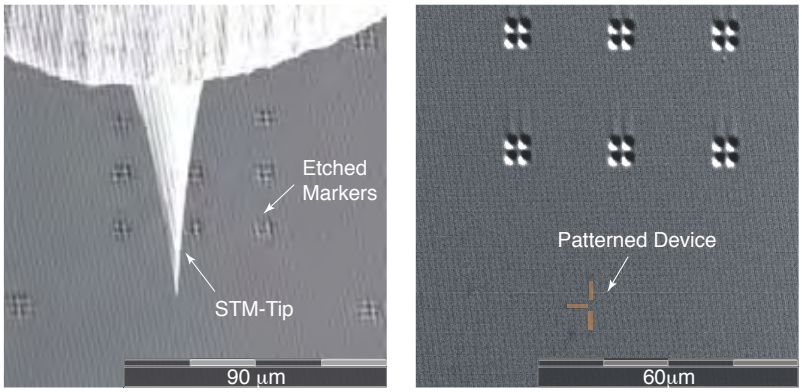


Figure 5.2: Incorporation of a UHV dielectric into the STM fabrication scheme. (a) Registration markers are etched, and the sample is flash-annealed. (b) The bare silicon surface is exposed to a flux of atomic hydrogen, used as a resist. (c) The STM tip is used to desorb hydrogen. (d) The sample is dosed with phosphine gas, which adsorbs to the reactive silicon surface. (e) The sample is annealed to incorporate the phosphorus dopants into the lattice. (f) The patterned dopants are encapsulated with silicon. (g) The encapsulated device is oxidised to form a gate dielectric. (h) Metallic gate electrodes are then deposited on the oxide using clean-room processing to complete the MOS structure.



(a) (b)

Figure 5.3: SEM image of the STM tip relative to the etched registration marker. (a) Positioning the tip relative to the etched registration markers in the silicon sample. (b) Location of the completed device (orange) relative to the registration markers.

5.3 Fabricating surface-gated STM-patterned devices

5.3.1 Modifying the STM-fabrication scheme to form surface gated devices

This thesis extends the STM-fabrication scheme developed within our group over the past decade to include metallic surface gates patterned by electron beam lithography (EBL) on a low-temperature silicon dioxide dielectric. Here we describe the fabrication process developed for surface gated devices, which includes a UHV oxide and a metallic surface gate electrode as shown in Fig. 5.2. We step through each stage of the fabrication process, but the discussion of steps identical to that of in-plane gated devices is limited to the process parameters used.

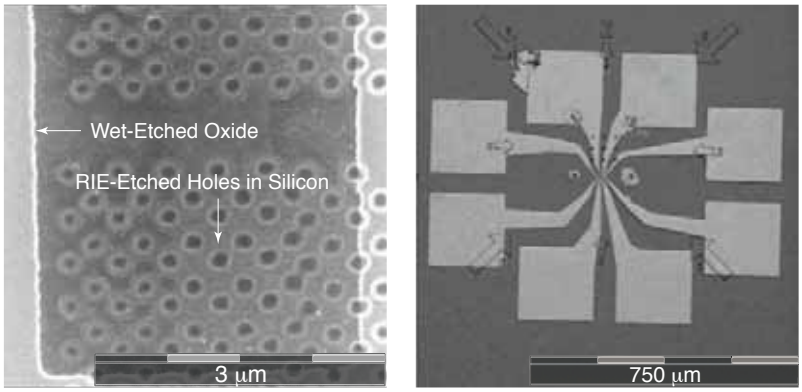
Alignment markers and surface preparation: The alignment markers for surface-gated devices are identical to those used for in-plane gated devices, fabricated by etching the same 1–10$\Omega.cm$ n-type (phosphorus doped) silicon substrates using tetra-methyl ammonium hydroxide (20%w/w TMAH) to give the desired alignment marker pattern. After etching alignment markers, the wafer is cleaned chemically (see App. A), and loaded into the ultra-high vacuum environment. Water adsorbates are then baked from sample for $\sim 12hrs$ at $400°C$, after which the sample is annealed at $1100°C$ twice, once for $1min$ and a second time for $5s$. The sample is then cooled slowly ($1°C.s^{-1}$) to $280°C$ and held at this temperature while exposed to atomic hydrogen for $6min$, passivating the surface with hydrogen.

STM lithography: Once moved to the STM chamber, the STM tip is conditioned by pulsing the tip voltage within the range $-10V \leq V_{tip} \leq 10V$. Once satisfied with the stability and resolution of the tip for both writing and imaging, the tip is moved to the alignment markers (Fig. 5.3(a)), where the precise location is noted relative to the markers. The device is then patterned in the hydrogen resist by passing the pre-defined pattern file to the STM control software. Finally, the source, drain, and gate electrodes are extended out to large area contact patches ($800nm \times 3000nm$), used to make contact to the device using EBL-defined metallic electrodes.

Doping and encapsulating the device: After patterning, the device is dosed with phosphine gas at a pressure of $1.1 \times 10^{-9} mbar$ for $30min$, after which the dopants are incorporated into the sample using a short anneal ($1min$ at $350°C$). The sample is then encapsulated with MBE-grown silicon by exposing it to a silicon flux of $\sim 0.1nm/min$ for $3hrs$ at $T_g = 250°C$, forming a $20nm$ layer of silicon over the device.

Depositing the low temperature oxide: It is at this stage that we have modified the existing fabrication process to form surface gated devices. The first step in making surface gates is to deposit the low-temperature dielectric developed in Chapter 3 onto the sample. For this, the device is transferred within UHV to the oxide chamber immediately after encapsulating the device with epitaxially-grown silicon. All surface gated STM patterned devices in this thesis were grown without substrate heating during the growth, to keep the diffusion of dopants to an absolute minimum. Radiative heating from the silicon and oxygen sources restricted the minimum steady-state temperature of the sample to $\sim 140°C$, measured using the manipulator thermocouple. The expected diffusion under these conditions for an oxide grown over $3hrs$ is $x_j < 0.3nm$. All oxides were grown using an oxygen pressure of $2.0–4.0 \times 10^{-6} mbar$, with an RF power of $350W$, and SUSI temperatures of $920°C$, resulting in a growth rate of $0.17nm.min^{-1}$. The samples were not given a post-oxidation anneal, both to restrict diffusion of the patterned dopants and to probe the performance of the as-grown oxide.

Depositing metallic source, drain, and gate electrodes: The sample is then removed from UHV and electrically contacted in a clean room. As described for the in-plane gated device, ordinarily we first pattern the doped contact regions with a mesh of $200nm$ diameter holes using EBL, which perforate the STM-patterned contact patches in a way that gives good contact between the metallic electrodes and the phosphorus-doped silicon. With a thick $50nm$ UHV silicon dioxide layer over the device however, we found it difficult to maintain the required definition of the EBL-defined holes. To overcome this we added an additional lithographic step to the process to chemically remove the oxide from the contact regions using a $15s$ immersion in buffered hydrofluoric acid (15:1 NH_4F



(a) (b)

Figure 5.4: SEM images of the UHV oxide surface-gated device during the clean-room post-processing steps. (a) Before depositing the Ohmic contacts, the oxide was first wet-etched from the ohmic regions to reveal the silicon substrate below, and then the silicon was etched with $200nm$ diameter holes to give reliable contact between the Al contact metal and the buried STM-patterned device. (b) Optical image of the completed device showing the contacts extending out to large area ($\sim 200\mu m \times 200\mu m$) bond pads, used to bond the device to the chip package.

$(40\%w/w)$:HF $(49\%w/w)$) before patterning the hole array. The wet-etched oxide and RIE-etched holes in the silicon are shown in Fig. 5.4(a). Using this method, we achieve reliable contact to the STM-patterned devices.

After locally removing the oxide and perforating the contact patches, metallic source and drain electrodes are patterned with EBL using the standard lift-off process described for the in-plane gated device ($\sim 80nm$ of Al), an example of which is shown in Fig. 5.4(b). Since we found it best to perform a quick chemical etch in hydrofluoric acid before depositing the contact metal (to remove any native oxide on the silicon), the source, drain, and in-plane gate contacts are deposited in a separate EBL step to the surface gate electrode. The surface gate electrode is then deposited using an additional EBL step with the same lift-off process. For the devices presented in this thesis, no post-metallisation anneals were performed; however, we have shown using MOSFETs in Chapter 3 that it is possible to anneal devices to further optimise the quality of the oxide. We have not annealed any of the oxides in this thesis, both to find the minimum diffusion of the STM-patterned dopants, and to assess the quality of the as-grown oxide. After depositing the metallic leads, which terminate in large-area bond pads, the device is cleaved and glued to an IC package using PMMA, and the bond pads are bonded to the package pins using an aluminium wedge bonder.

Using this same process, we have successfully fabricated several surface-gated STM-patterned devices, and routinely achieve reliable contact to these devices once they are removed from the UHV system. In this chapter we describe the surface-gated STM-patterned SETs made using this process.

Considerations in the design of surface gated STM-patterned devices

There are a number of considerations in the design of surface gated STM-patterned devices using the fabrication scheme outlined in the previous section, including the thickness of the oxide, the alignment accuracy of the gate electrode, and the length of the STM-patterned contact patches. Here we explore these design considerations in greater detail.

Thickness of the UHV oxide: The thickness of the UHV oxide affects the capacitive coupling of the gate, the selectivity of the gate, the gate leakage, and the diffusion of dopants during the oxide growth. In the devices presented in this chapter, the gate selectivity is not critical since a single surface gate is used. In addition, since the gate capacitance decreases in proportion to the oxide thickness, but the leakage decreases exponentially, we typically achieve a greater gating range using a thicker oxide. As such, the devices presented here each have a thick oxide. The growth parameters outlined in the previous section result in a growth rate of $\sim 0.17 nm.min^{-1}$, with a substrate temperature of 140–160°C from radiative heating from the silicon source. At these conditions, we can grow a $\sim 50nm$ oxide before reaching our tolerance on the diffusion of dopants ($x_j < 0.5nm$), which corresponds to an approximately $6hr$ growth. Each of the devices presented in this chapter therefore include a $50nm$ oxide grown under the conditions outlined in the previous section.

Alignment accuracy of the gate electrode: The alignment accuracy of surface gates for STM-patterned device is limited to $\sim 100nm$ by the resolution of the alignment markers etched into the silicon substrate. These alignment markers lose definition when the sample undergoes the high-temperature anneal used to form a clean Si (2×1) surface reconstruction, as silicon atoms on the surface both diffuse and sublimate from the surface during this anneal. With an alignment accuracy of $\sim 100nm$, the gate electrode must have a minimum size of $200nm$, to allow for misalignment of $\pm 100nm$ in either direction. For the devices presented in this chapter, the selectivity of the gate was not critical, so the gates were all patterned 1–2μm wide. We also etch the low temperature oxide away from the STM-patterned contact patches when depositing the aluminium surface electrodes. This process can lead to

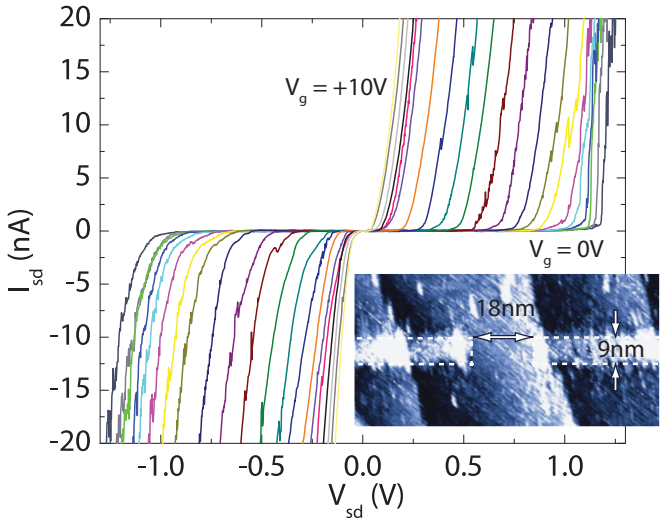


Figure 5.5: Surface-gated STM-patterned tunnel gap using the low-temperature UHV oxide. The STM-patterned tunnel gap fabricated by Wilson Pok [168] consists of $9nm$ wide source and drain leads separated by an $18nm$ gap (inset). The gap shows strongly non-linear I-V characteristics, and applying a positive bias to the surface gate reduces the zero-bias resistance of the device by three orders of magnitude.

some under-etch, and so we typically leave a $1\mu m$ separation between the surface electrodes and the gate. As such, we must ensure that the STM-patterned contact patches are several microns long (we use $> 5\mu m$) to generate sufficient contact area with the aluminium surface electrodes.

We have designed the STM-patterned devices presented in the next section with these considerations in mind. As such, each device has a $\sim 50nm$ low-temperature oxide formed at $\sim 140°C$ for $6hrs$, restricting the expected dopant diffusion to $x_j < 0.5nm$ (one lattice site). Furthermore, we have formed $5\mu m$ long STM-patterned contact patches to ensure that there is sufficient overlap with EBL-defined aluminium surface contacts.

5.3.2 Surface-gated STM-patterned tunnel gap

The UHV oxide developed for this thesis was used in collaboration with Wilson Pok to study surface gating of STM-patterned tunnel gaps [168]. As part of this study, we fabricated a device using the STM-SEM system described in Chapter 3 and the fabrication scheme outlined in the previous section. An image of the STM-patterned tunnel gap is shown in the inset of Fig. 5.5. The leads were patterned as $9nm$ wide $\sim 50nm$ long wires, separated by an $18nm$ tunnel gap. A $\sim 50nm$ thick UHV oxide was deposited on the device to act as a gate dielectric, capped with a $\sim 1\mu m$ wide aluminium gate electrode.

This surface gate had a range $-10.2V < V_g < 10.2V$ before the gate leakage reached $I_g = \pm 20pA$.

Figure 5.5 shows electrical transport results from this gated tunnel gap. The non-linear I-V curves are caused by tunnelling between the STM-patterned leads. The resonances in these traces are attributed to resonant tunnelling through unintentional dopants arising from stray desorption during the STM lithography process. For $V_g > 5.0V$ the zero-bias resistance of the device ($V_{sd} \simeq 0V$) decreases rapidly, changing from $\sim 5 \times 10^{11}\Omega$ at $V_g = +5.0V$ to $\sim 4 \times 10^{8}\Omega$ at $V_g = +10V$. Of the three surface gating methods used to gate the STM-patterned tunnel gaps in this study, including Schottky barrier gates and the native oxide, the low temperature UHV-grown oxide had the greatest impact on the tunnelling resistance of the device (1300 fold change in R_t, vs. 700 for native oxide and $\sim$4 for Schottky barrier). As such, this study demonstrated the wider gate range possible with the low-temperature oxide over alternative surface gating techniques. Following this study, we then began to use the oxide in STM-patterned single electron transistors.

5.3.3 Many electron (770e), surface gated STM-patterned SET using the low-temperature oxide

Among the first of the surface-gated STM-patterned devices fabricated was a $700e$ single electron transistor made in collaboration with Dr. William Lee [215], using the oxide developed for this thesis as a gate dielectric. This device was adapted from the design of the original device by Fuhrer *et al.* [22] in an attempt to reduce the number of donors on the central island from 4000 to $\sim$1000. One of our concerns in downscaling the central island was to maintain the capacitive coupling to the dot at smaller dimensions. To achieve this we used a curved gate geometry. The STM-patterning for this device followed the method outlined in the preceding section, starting from an n-type 1–10Ωcm silicon (100) wafer, into which registration markers were etched. The surface was then cleaned using the standard UHV annealing process, after which the surface was hydrogen terminated. The curved gate device architecture was then patterned into the hydrogen resist as shown in Fig. 5.6(a). There are four irregular lines passing vertically through the STM image, which are atomic steps on the silicon surface. In addition to these step edges, there are four bright regions that have been lithographically defined with the STM tip, labelled plunger gate (PG), source (S), drain (D), and dot. Based on the size of the patterned dot area and the donor density expected from the phosphine dosing process, we estimate approximately $700e$ on the dot at equilibrium.

Given the additional range anticipated using the surface-gate, it was not considered necessary to use two in-plane gates (a valid assumption, as we show later). As such, the single in-plane gate, source, and drain leads were angled around the dot in a way that minimised coupling between them. The in-plane gate was given a unique curved structure, increasing the capacitance between the gate and dot. The leads were patterned $8nm$ wide, terminating with $\sim 10nm$ tunnel gaps to the dot with the gate patterned at a radial distance of $38nm$ from the dot.

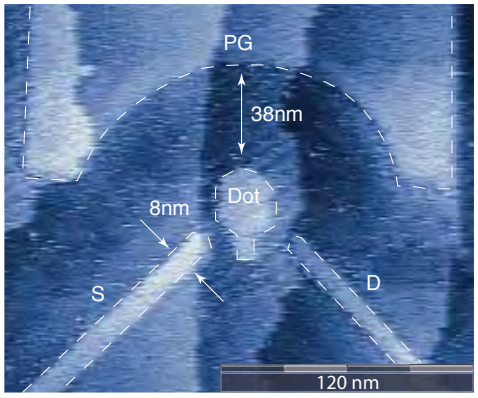
The $700e$ surface-gated SET was first characterised at $4K$ without the addition of a surface gate. A Coulomb blockade sweep of the dot from this measurement is shown in Fig. 5.6(b), taken using the in-plane gate. We see in Fig. 5.6(b) regular Coulomb blockade peaks spaced $35mV$ apart in the V_{PG}-axis, corresponding to an in-plane gate capacitance of

$$\begin{aligned} C_{PG} &= \frac{e}{\Delta V_{PG}} \\ &= 4.5aF \end{aligned} \tag{5.1}$$

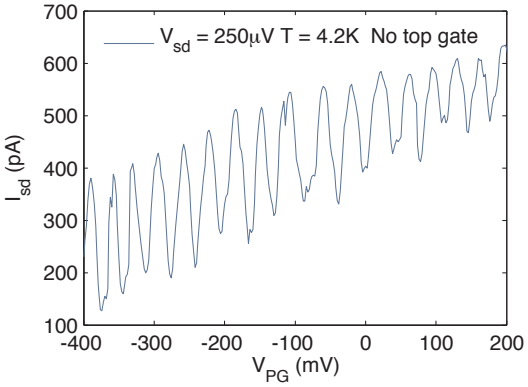
The source-drain conductance does not go to zero between peaks, indicating that we do not achieve full Coulomb blockade. The peak and valley conductance both drop as V_{PG} becomes negative, attributed to a change in the coupling of the source and drain tunnel barriers. The peak conductance is $\sim 0.1e^2/h$ at $V_{PG} = 0.2V$, from which we conclude that the dot conductance is likely affected by life-time broadening.

Following the initial characterisation, the device was removed from the measurement setup and a surface gate ($1.5\mu m \times 2.5\mu m$) was deposited over the buried STM-patterned dot. Figure 5.6(c) shows the resultant current through the device at $V_{sd} = 250\mu V$, sweeping the surface gate (V_{TG}), showing $\sim$160 Coulomb blockade peaks visible within the gate range ($-5.5V < V_{TG} < 2.5V$). Again we see the blockaded current does not go to zero until we apply a large negative bias. Both the peak and valley conductance reduce with gate voltage, which is consistent with the gate field making the tunnel barriers more opaque.

The conductance plot in Fig. 5.6(d) was taken using the in-plane gate while holding the surface gate at $V_{TG} = -5.5V$. Here we see the peak spacing has changed to $\Delta V_{PG} = 46mV$, indicating a slightly smaller gate capacitance of $C_{PG} = 3.5aF$, due to the additional capacitance between the surface gate and the dot. More interesting is the reduction in the valley conductance in the presence of the surface gate; by holding the surface gate at $V_{TG} = -5.5V$, the valley conductance is reduced to less than $10pA$ from the $100pA$ seen without a surface gate. This indicates that the surface gate can be used to control the transparency of the tunnel barriers, so that the dot can be tuned to give true Coulomb



(a)



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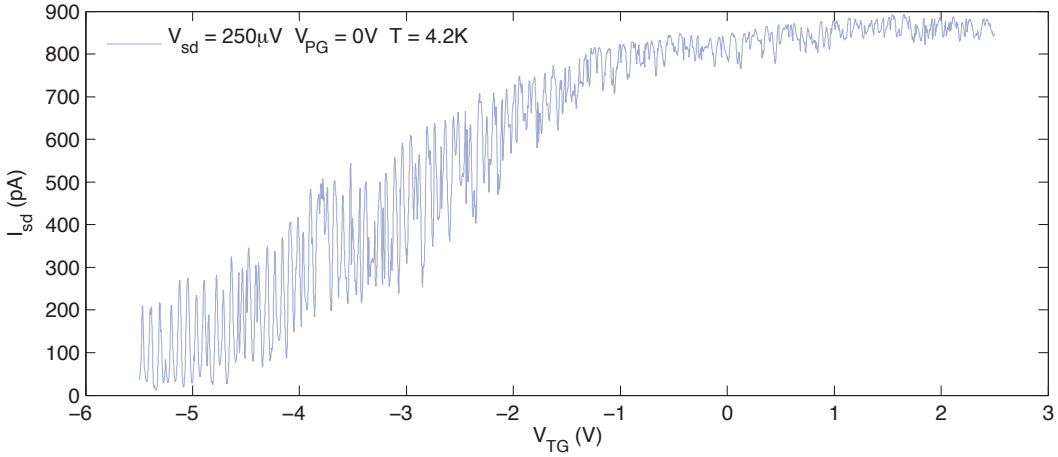

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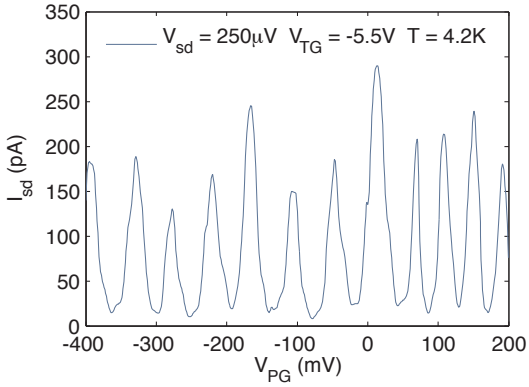

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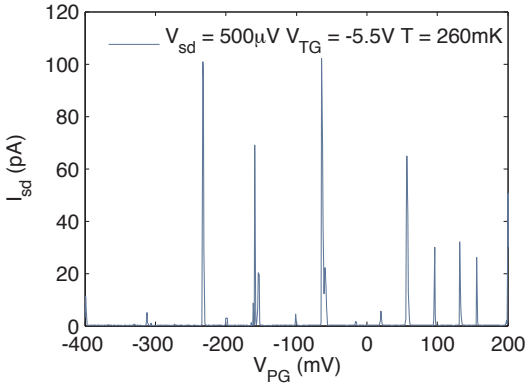


(e)

Figure 5.6: Transport characteristics of a 700e UHV oxide surface-gated STM-patterned SET. (a) Filled state STM image of the device (-3.1V, 0.3nA). (b) In-plane gate sweep at $4.2K$ before depositing the surface gate. (c) Surface gate sweep at $4.2K$ with the in-plane gate floating. (d) In-plane gate sweep at $4.2K$ after depositing the surface gate, which was held at $V_{TG} = -5.5V$. (e) In-plane gate sweep at $\sim 260mK$ with the surface gate at $V_{TG} = -5.5V$.

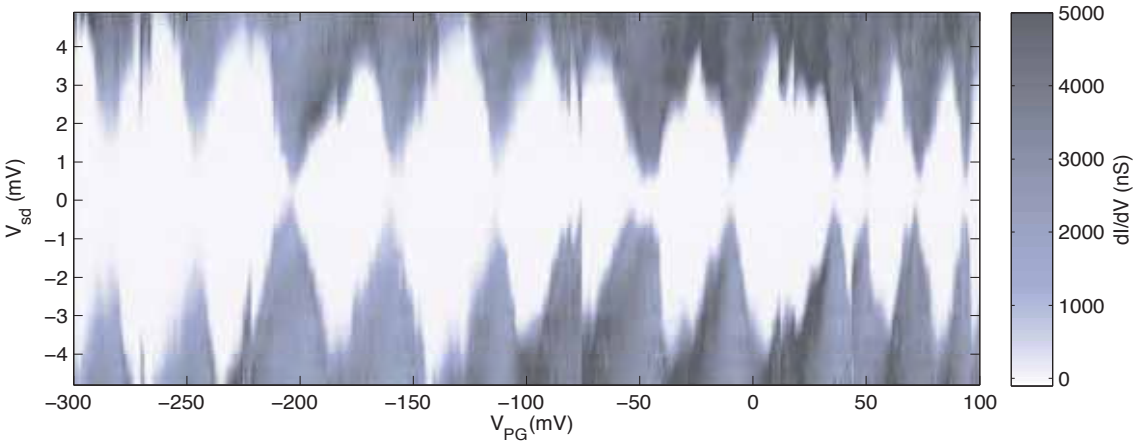


Figure 5.7: Stability plot of a 700e surface-gated STM-patterned SET. A stability plot of a surface-gated UHV dielectric SET using the in-plane gate to tune to dot potential ($V_{TG} = -5.5V$). There are many switches in the stability plot for each transition in the dot occupancy.

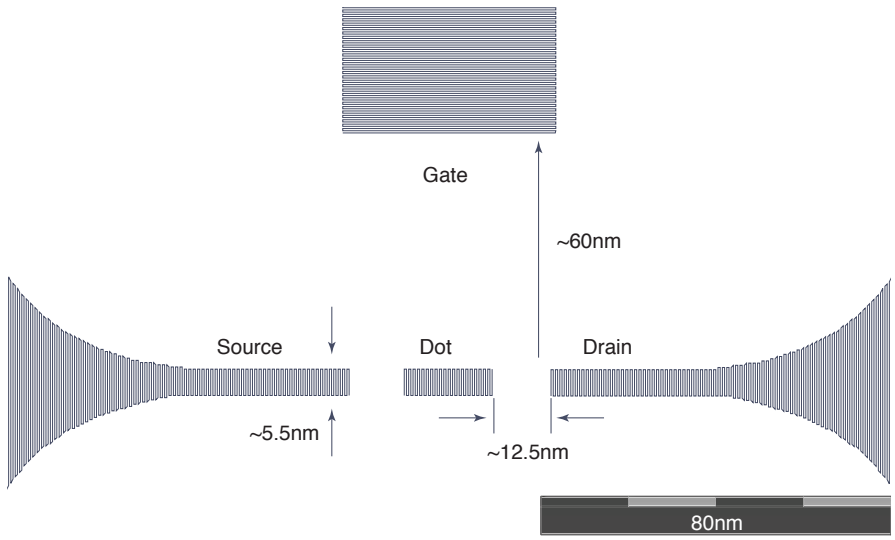
blockade.

When the sample was cooled to the base fridge temperature ($\sim 260mK$), the peaks narrowed and the valleys went into true blockade, with the current decreasing to $< 1pA$, as shown in Fig. 5.6(e). A stability plot of the device at base temperature is shown in Fig. 5.7, highlighting the large number of switches observed in the device, indicative of a high density of capacitively-coupled traps nearby. In order to fairly compare the behaviour of surface gated STM patterned devices to in-plane gated devices, we decided to make an SET of similar dimensions to the ∼200 donor in-plane gated SET of Chapter 4. We describe the design and electrical performance of this device in the next section.

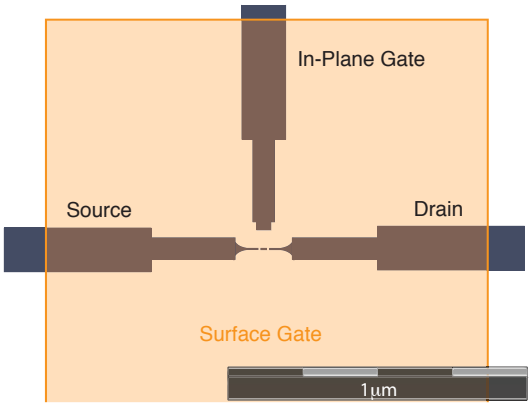
5.4 Fabricating a surface-gated SET for a systematic comparison with in-plane gated devices

5.4.1 Designing the surface-gated STM-patterned SET

In Chapter 4 we designed an in-plane gated SET specifically to test the noise and stability of the in-plane gating scheme, and found its noise to compare favourably to the best devices reported by Zimmerman *et al.* In this chapter we describe a surface-gated SET of comparable dimensions, using the low-temperature oxide developed in Chapter 3 as a gate dielectric. The purpose of this device is to measure the performance of the surface-gate



(a)



(b)

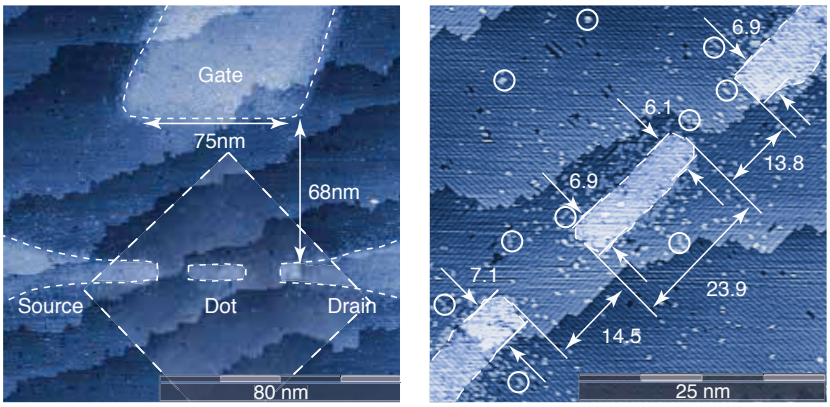
Figure 5.8: STM-lithography pattern of a ∼200e UHV oxide surface-gated SET. (a) The inner-most patterned region of the surface-gated device is nominally identical to that of the in-plane gated device in Chapter 4. (b) The central $1.5 \times 2\mu m$ of the STM-patterned device is covered with a global surface gate (shown in orange), deposited over a $50nm$ layer of the low-temperature oxide.

architecture relative to the previously-fabricated in-plane gated device. As such, we have used the same STM pattern file to generate the device, as shown in Fig. 5.8(a). That is:

Tunnel barriers with an aspect ratio of ∼0.45, and a width ∼$5.4nm$, tapering out to large contact patches.

Dot dimensions of ∼ $5.4nm \times 25nm$, giving ∼200 donors, and therefore ∼$200e$ on the dot at equilibrium.

An in-plane gate separated by ∼$60nm$ from the device, that is ∼$60nm$ wide.



(a) (b)

Figure 5.9: STM-image of the surface-gated SET. STM image of the surface-gated SET at a large scale (a), and a close-up (b), which has dimer-row resolution. From this high-resolution image we were able to calculate the precise device geometry.

In addition, this device also includes an $80nm$ thick aluminium global surface gate $\sim 1.5\mu m \times 2\mu m$ across (the outline of the gate is shown in orange in Fig. 5.8(b)). The surface gate is separated vertically from the device via the $20nm$ encapsulation layer and the $\sim 50nm$ low temperature oxide used as a gate dielectric. When depositing this oxide, we aimed to keep the deposition temperature as low as possible ($\sim 160^{\circ}C$) in order to minimise diffusion of dopants within the device. Since we know that the oxide quality improves when using higher deposition temperatures, or post-oxidation/post-metallisation anneals, it is known that these conditions give a worst-case measure of the oxide quality. However it demonstrates the lower limit of the thermal budget achievable with this technique. In the next section we describe the fabrication process used to make this device.

5.4.2 Fabricating the surface-gated STM-patterned SET

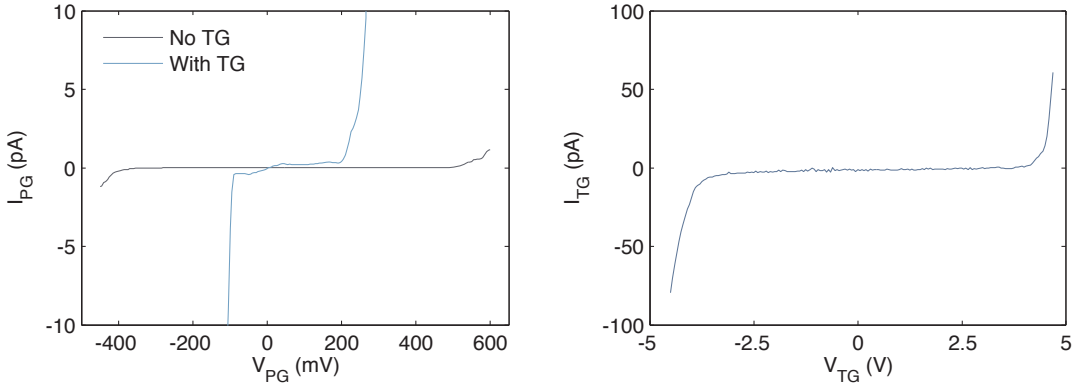
The fabrication of this surface gated ~ 200 donor SET follows the procedure outlined in Sec. 5.3.1. We began with the standard set of alignment markers and cleaned the sample both chemically and then in UHV using the anneal process. We then hydrogen terminated the sample and transferred it to the analysis chamber to pattern the device. The batch of tips used to fabricate this device retained a thin surface oxide after the tip conditioning process. This is common on the STM-SEM system because the tip cannot be annealed in-situ to remove the oxide. As such, we were forced to pattern the device close to the field-emission regime for STM-lithography (low current, high voltage), using a tip current of $3nA$ and a tip voltage of $6V$. This affected the precision of the STM lithography,

leading to a greater amount of stray desorption of the hydrogen resist around the intended pattern, as shown in Fig. 5.9(b). This is also the reason for the stray desorption visible in the STM-patterned tunnel gap (Fig. 5.5) and the curved gate 700e SET (Fig. 5.6(a)). We have highlighted several sites in the STM image of Fig. 5.9(b) where a PH_3 molecule might bind to the surface. Because of the change in the line-edge roughness, we also increased the tunnel gap dimensions to ensure that the tunnel gap aspect ratio would give the desired device conductance. As such, the tunnel gaps were patterned as $7.1nm \times 14.5nm$ and $6.9nm \times 13.8nm$, compared to $\sim 5.4 \times 12.5nm$ for the in-plane gated device. These dimensions correspond to a lead width to tunnel gap aspect ratio of 0.48 and 0.50, respectively compared to the aspect ratio of the in-plane gated device ($\sim$0.44). These tunnel gaps were therefore expected to be more transparent than the in-plane gated device in the previous chapter ($R_t \simeq 1M\Omega$ vs. $R_t \simeq 16M\Omega$, respectively, based on Fig. 4.8 on pg. 114).

The low temperature oxide was grown on the surface-gated SET without substrate heating. Radiative heating from the silicon and oxygen sources generated a steady-state sample temperature of $\sim 158^{\circ}C$, measured using the manipulator thermocouple. The oxide was grown at a pressure of $2.0 \times 10^{-6} mbar$, with an RF power of $350W$, and SUSI temperatures of $920^{\circ}C$, resulting in a growth rate of $0.17nm.min^{-1}$. The growth took $\sim 6hrs$ to reach the desired $50nm$ of oxide. The expected diffusion under these conditions is $x_j < 0.5nm$. The sample was then removed from UHV and contacted with aluminium surface contacts and a surface gate using the process outlined in Sec. 5.3.1.

5.4.3 Electrical transport characersitics of the surface-gated SET

The surface gated device has both an in-plane gate (of the same dimensions as the device presented in Chapter 4), and a surface gate that was formed using our low temperature oxide as a dielectric. Two key factors affect the gating action: the voltage range before the gate leaks, and the capacitance between the gate and the device. First, let us discuss the voltage range. The leakage characteristics of the in-plane gate with and without the surface gate are shown in Fig. 5.10(a). Interestingly, we see the gate range dramatically reduces after depositing the surface gate. We can attribute this to either the presence of the surface gate changing the tunnel-barrier/breakdown characteristics of the intervening region of silicon, or to a leakage path from the in-plane gate to the surface gate itself. We note that the maximum range of the in-plane gate in this device is $\sim$40% lower than that of the in-plane gated device in the previous chapter, despite being $\sim 10nm$ further away. This is likely to be the result of stray dopants in the intervening region of silicon separating the



(a) (b)

Figure 5.10: Gate leakage of the surface-gated SET. (a) Leakage of the in-plane gate both before and after the surface gate was added to the device. The in-plane gate begins to leak abruptly at $V_{PG} \simeq \pm 500mV$ before adding a surface gate, and $-100mV < V_{PG} < 200mV$ after adding the surface gate. (b) The surface gate has a range of $V_{TG} = \pm 4.5V$, and the leakage is observed to increase more slowly than that of the in-plane gate.

gate from the device (Fig. 5.9). Stray dopants affect both tunnelling and breakdown of the substrate: In tunnelling, the additional doping lowers the potential barrier, and creates Frenkel-Poole type tunnelling [139]. In breakdown, the presence of additional un-ionised donors accelerates the avalanche process by increasing the ease with which free carriers are generated [28]. We can see the dramatic difference between the in-plane gate range and that of the surface gate ($-3.7V < V_{TG} < 4.1$ @$I_{TG} = 10pA$), shown in Fig. 5.10(b). This is expected because we are applying the surface gate voltage across a $50nm$ layer of SiO_2, which has a much greater potential barrier than the in-plane gates ($3.2eV$ vs. $\sim 100meV$). Having established that the surface gate range is considerably larger, let us now look at the capacitive coupling. Theoretically, the capacitance of the surface-gating scheme has a geometric advantage, since the overlap area between the surface gate electrode and lateral dot is much greater than the in-plane gate, where the capacitive coupling only acts at the edges of atomic terraces. Let us now look at this geometric advantage in more detail.

From the close-up STM image of the device in Fig. 5.9(b), the device area is

$$\begin{aligned} A &= 6.9nm \times 23.9nm \\ &= 165nm^2 \end{aligned} \tag{5.2}$$

This dot is therefore $\sim$25% larger than that of the in-plane gated device from Chapter 4 ($126nm^2$). The expected number of donors on the dot, calculated from our calibrated

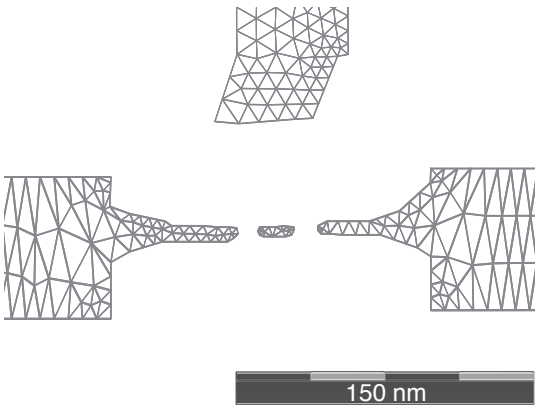


Figure 5.11: Wireframe model of the surface gated SET for capacitance modelling.

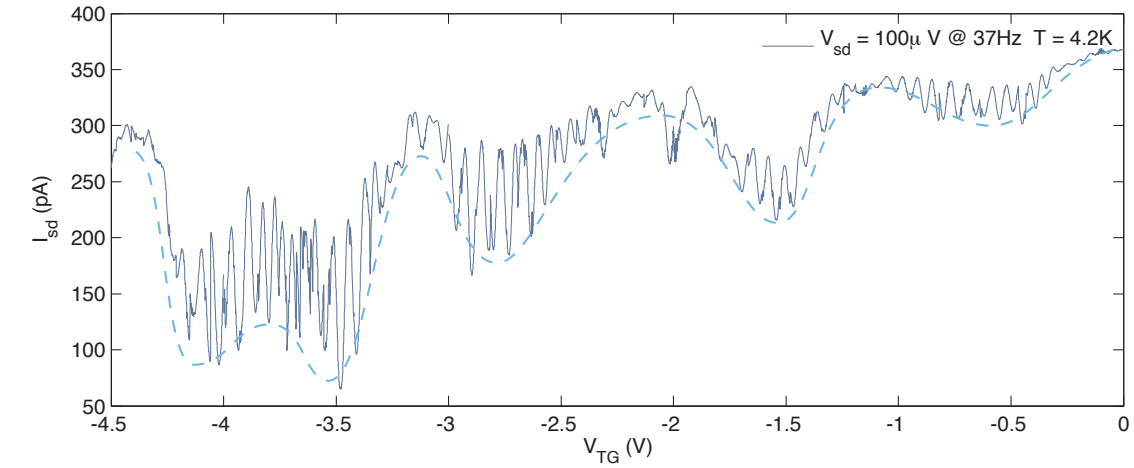
doping density of $1.5 \times 10^{14} cm^{-2}$, is therefore

$$\begin{aligned} N &= (165 \times 10^{-18} m^2).(1.5 \times 10^{18} m^{-2}) \\ &= 248 \end{aligned} \tag{5.3}$$

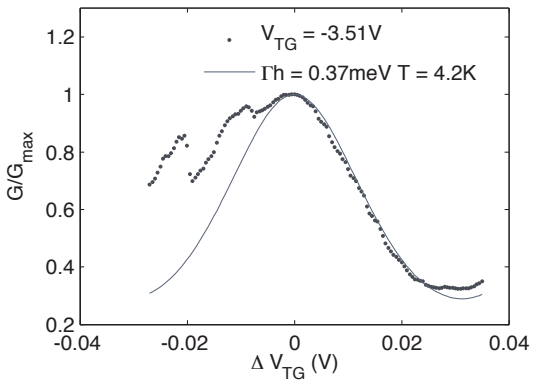
That is, we estimate that there will be approximately 250 donors within the dot, and that each donor will have a bound electron, giving an upper limit of $250e$ on the dot at equilibrium.

From the large-scale STM image of the device, we can accurately measure the size, shape, and separation of each of the conducting regions, which we have used to generate the wireframe model in Fig. 5.11 for modelling the coupling capacitances using FastCap. As with the in-plane gated device, we have extended the pattern laterally by $\sim 2nm$ to account for the Bohr radius, and we have used a modelled thickness of the δ-layer of $\sim 2nm$, in accordance with the modelling of Carter *et al.* [33]. The results of this capacitance modelling are shown in Table 5.1.

We have modelled the device using FastCap both before depositing the surface gate and afterwards, to establish the differences between this device and the in-plane gated device of Chapter 4 based solely on their fabrication, and those due to the presence of the surface gate. As a consequence of the greater separation in the patterning of the source and drain regions from the dot in this device, the source and drain capacitances of this device ($C_S = 1.6aF$, $C_D = 2.1aF$) are much less than that of the in-plane gated device ($C_S = C_D = 4.1aF$). There is also an asymmetry in the source and drain capacitances of the surface-gated device as a result of the different tunnel gap geometries after patterning. This was not seen in the in-plane gated device in the previous chapter, where the source



(a)



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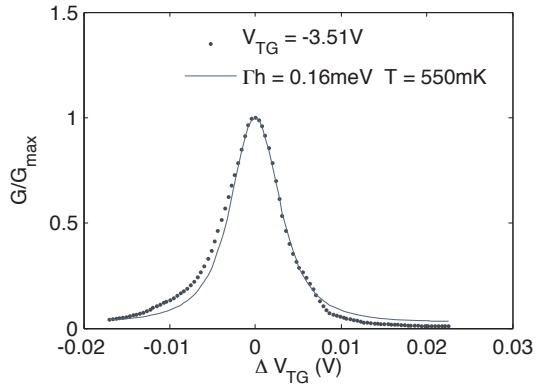

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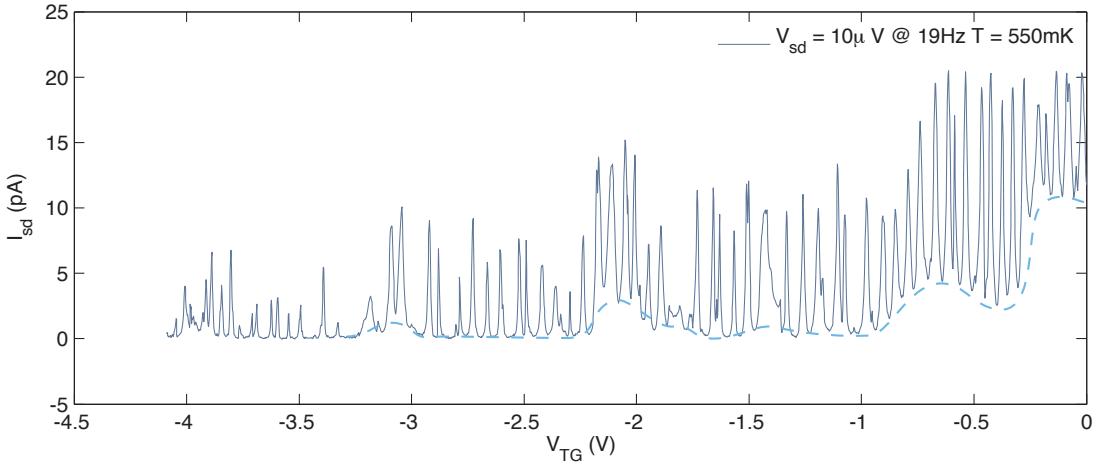


(d)

Figure 5.12: Measuring the device conductance as a function of the surface gate voltage. (a) Coulomb blockade sweep of the device at $4K$ using the surface gate showing a beating pattern in the peaks, where the valley conductance changes as a function of voltage (dashed line). (b) Close-up image of a blockade peak at $4K$ showing a fit to the peak shape with both electron temperature and lifetime broadening. (c) Close-up image of the same peak shown in (b) at the base fridge temperature ($\sim 550mK$). (d) Coulomb blockade sweep of the device at base temperature showing that the beating pattern in the peaks is retained.

Table 5.1: Capacitance of the surface gated SET from modelling and experimental measurements

(aF)	C_Σ	C_D	C_{PG}	C_S	C_{TG}
No Surface Gate					
Simulation	8.6	1.6	1.1	2.1	N/A
Experiment	< 64	–	4.2	–	N/A
With Surface Gate					
Simulation	8.7	1.0	0.5	1.5	3.3
Experiment	< 59	–	2.9	–	2.2

and drain tunnel gap dimensions were approximately equal.

Once the surface gate is added to the device, the sum capacitance of the dot increases — a consequence of the additional surface gate capacitance. The global surface gate also acts as a ground plane for each of the phosphorus-doped regions, so that the field lines emanating from each lead are shielded by the surface gate, lowering each of the capacitances C_D, C_{PG}, and C_S. As such, the effective lever-arm of the in-plane gate ($\alpha = C_{PG}/C_\Sigma$) more than halves in the presence of the surface gate.

Experimentally, we observed the in-plane gate gradually degrade once we had patterned a surface gate on the dielectric. As a consequence, we will focus solely on the action of the surface gate in the following analysis. A Coulomb blockade sweep at $4K$ using the surface gate is shown in Fig. 5.12(a). As with the surface gate of the $700e$ device, here we see many Coulomb blockade peaks within the accessible gate range (> 150 for $-4.5 < V_{TG} < 4.5$), with both the peak and valley conductance reducing as the gate voltage approached its negative limit. However, we also see a regular beating pattern in the peak and valley conductance (dashed blue line). This behaviour is similar to that reported by Hofheinz *et al.* shown in Fig. 5.13, with the same beating in both the peak and valley conductance. Hofheinz *et al.* explained this beating pattern by the presence of a tunnel-coupled trap between the lead and dot, with $C_{dt} \simeq C_{Dt}$ [216]. This model is identical to the tunnel-coupled trap system discussed in Sec. 4.4.1. Essentially, the premise is that, rather than a single trap state that causes the diamonds to open and close again once filled, the trap has multiple levels (that is, it is a dot in itself), and so the opening and closing of the diamonds repeats for each level of the unintentional dot, causing a beating of the blockade peaks and valleys [216]. This coupled trap may arise from several sources. It could be a single trap between the lead and dot arising from the incorporation of donors

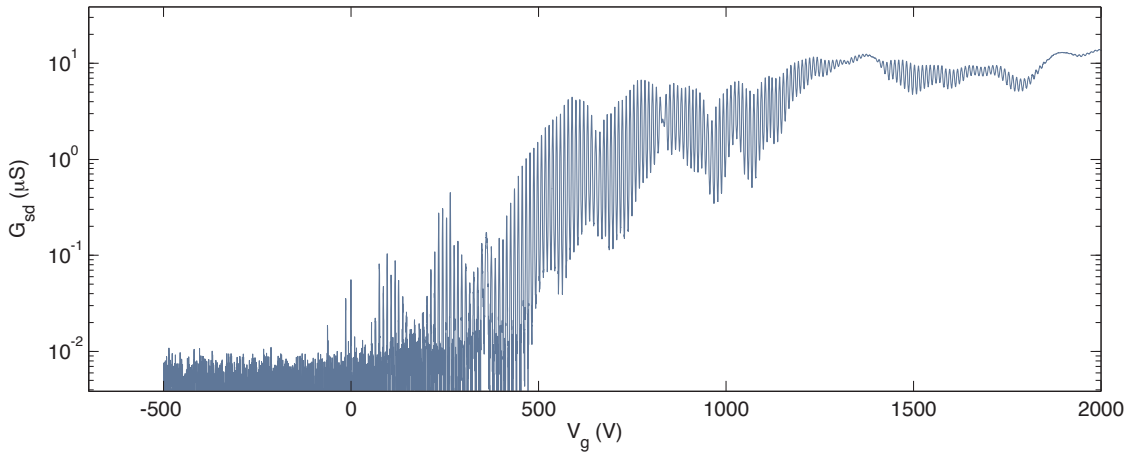


Figure 5.13: Beating of Coulomb blockade peaks reported by Hofheinz *et al.* Hofheinz *et al.* have reported a similar beating pattern in the Coulomb blockade peaks as seen in our surface-gated SET, showing periodic regions where the contrast between peak and valley conductance is reduced. Reproduced from [216]

from the stray desorption of the STM patterned regions (highlighted in Fig. 5.9). It could also be due to the source or drain lead breaking up into unintentional series-coupled dots. However, given the high doping density of our leads, and the number of sites for unintentional dopants to be incorporated into the sample highlighted in Fig. 5.9, we believe the effect is due to a coupled donor from stray desorption.

Further to the beating pattern of the Coulomb blockade peaks, we see a great many switches in the gate sweeps — in fact, often there are multiple switches on a single peak (e.g. Fig. 5.12(b)). This complicates the peak fitting process used to calculate the thermal and lifetime broadening of the peak. We can see from the blockade sweep that the peak conductance at $V_{TG} = -3.51V$ (one of the nodes of the beating pattern) is

$$\begin{aligned} G &= 200 \times 10^{-12}/100 \times 10^{-6} \\ &= 2\mu S \\ &\simeq 0.13\frac{e^2}{h} \end{aligned} \tag{5.4}$$

That is, the peak conductance is approximately one tenth of a conductance quantum (e^2/h), and so we expect the peak to be at least partially lifetime-broadened. In Fig. 5.12(b) we show a fit to this peak that includes both thermal broadening ($T = 4.2K$) and lifetime

broadening ($\Gamma h = 0.37meV$) according to the form

$$\begin{aligned} \frac{G(\Delta\mu_d)}{G_{max}}_{Life} &= \frac{(h\Gamma)^2}{(h\Gamma)^2 + \Delta\mu_d^2} \\ \frac{G(\Delta\mu_d)}{G_{max}}_{Therm} &= \frac{\Delta\mu_d/k_BT}{\sinh(\Delta\mu_d/k_BT)} \\ \frac{G(\Delta\mu_d)}{G_{max}}_{Total} &\simeq \frac{G(\Delta\mu_d)}{G_{max}}_{Life} * \frac{G(\Delta\mu_d)}{G_{max}}_{Therm} \end{aligned} \tag{5.5}$$

where the first equation accounts for lifetime broadening with a transmission rate of Γ through the dot, the second for thermal broadening with an electron temperature of T, and the final equation shows their combination through the convolution operator. Note that in Fig. 5.12(b) there is a finite valley conductance because we include the contribution from the adjacent peak (we add the G/G_{max} fit shifted in V_{TG} by the peak spacing). From Fig. 5.12(c), we see that both the thermal broadening and lifetime broadening of the Coulomb blockade peak decrease with temperature, where the latter ($\Gamma = 0.37meV \rightarrow 0.16meV$) is a consequence of the tunnel barriers becoming more opaque as the sample is cooled and the tunnel barrier potential profile becoming sharper.

In Fig. 5.12(d) we see that as the temperature is reduced to base ($\sim 550mK$), the peaks become narrower and we see a reduction in both the peak and valley conductance. In particular, here the valley (off-peak) conductance reduces to $\sim 0\mu S$, so that the device is truly in Coulomb blockade. The beating pattern in the Coulomb blockade peaks remains at base temperature, though there is a greater contrast between the peak and valley conductance because the lifetime and thermal broadening have decreased. There are still many switches in this trace — indicating that the switching process is active even at base temperature for this device.

We show stability plots of the device in Fig. 5.14, beginning with a map taken at $4K$ using the in-plane gate (before the surface gate was added to the device, Fig. 5.14(a)). In this map in particular, the Coulomb diamonds are indistinct, with the minimum conductance not reaching zero as expected under true Coulomb blockade. Also, the maximum conductance is more than an order of magnitude greater than that of the in-plane gated device, because of the lower tunnel barrier resistance. It was not possible to extract the charging energy from this map since the diamond edges are smoothed by the lifetime broadened electron energy levels. There are also many fine switches running vertically through the map that obfuscate the diamond edges, but we can estimate an absolute lower limit on the charging energy of $E_c = 1.5meV$ and what appears to be an upper limit of $4meV$. This is approximately one third that of the in-plane gated device ($E_c = 13.6meV$), despite

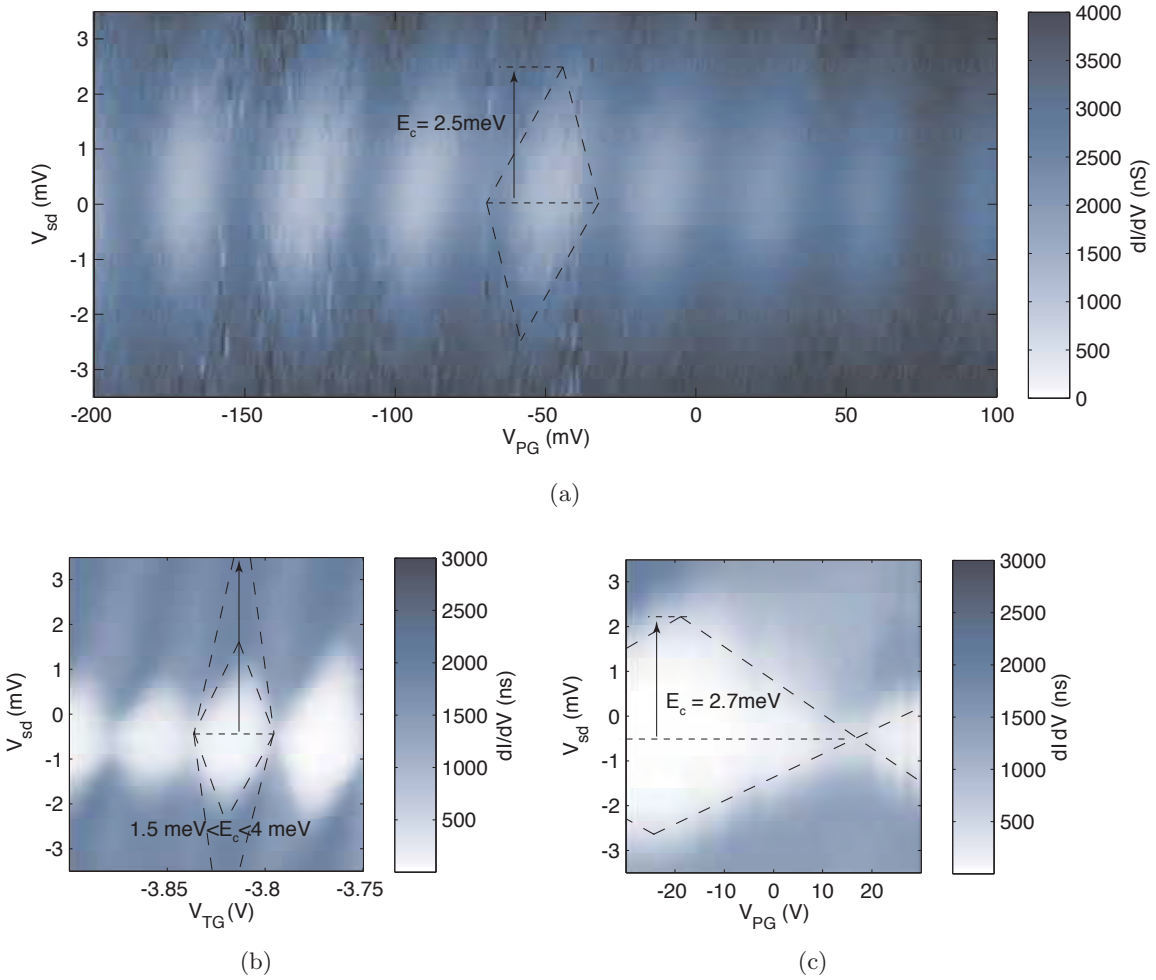


Figure 5.14: Stability plots of the surface-gated SET. (a) Stability plot taken using the in-plane gate at $4K$ before the surface gate was patterned on the device. (b) Stability plot taken using the surface gate at base temperature with the in-plane gate floating. (c) Stability plot taken using the in-plane gate at base temperature with the surface gate held at $V_{TG} = -4.3V$.

using the same file to pattern the device with the STM. However, we note that this is not a fair comparison because of the uncertainty in E_c from this measurement.

As we cooled the device to base temperature, the diamonds became truly blockaded, so that the diamond edges were sharper (Fig. 5.14(b), Fig. 5.14(c)). In Fig. 5.14(b) the Coulomb diamonds are changing in size with each transition, with the largest consistent with a charging energy of $E_c = 4meV$. We can also see in this figure that the mid-point of these diamonds actually occurs at a source-drain bias of $V_{sd} = -0.5mV$. This offset is similar to that seen in the devices of Hofheinz *et al.* [216], in which a tunnel coupled trap caused a doubling of the Coulomb diamonds in the stability map, where the vertical

shift is caused by coupling between the gate and the trap. The sum and gate capacitances extracted from these stability plots are shown in Table 5.1. The gate capacitance is more than double that modelled with FastCap, the charging energy is significantly less ($\sim 4meV$ vs. $18.6meV$), and the tunnelling resistance is less than half the designed value. There are a number of possible reasons for this, including:

Diffusion of dopants during the low temperature oxidation: We expect dopants to diffuse by $x_j < 0.5nm$ during the growth of the low temperature oxide. If the dopants were to diffuse significantly more during the growth, the phosphorus-doped regions could differ substantially from the patterned dimensions shown in the STM images of Fig. 5.9. In particular, if the dopants diffuse outwards from their patterned location, the capacitive coupling between each of the doped regions would increase. This would cause C_{PG}, C_{TG}, and C_{Σ} to increase, where the latter would account for the reduction in the charging energy. This would also account for the tunnel-barrier resistance of this device being lower than expected based on the trend between aspect ratio and zero-bias resistance discussed in the previous chapter (we expect $R_t \simeq 2M\Omega$, and we see $R_t < 500k\Omega$).

Tunnel coupling to an unintentional dot: As we discussed in the previous chapter, it is possible for the Coulomb diamonds to be replicated in gate space if the dot is tunnel-coupled to a nearby trap (or an unintentional dot). If the trap-dot and trap-drain capacitive coupling are approximately equal ($C_{dt} \simeq C_{Dt}$), the shifted Coulomb diamonds would be replicated at the mid-point of the original diamonds, effectively doubling the apparent gate capacitance, and halving the apparent charging energy. Given the beating pattern in the Coulomb blockade sweeps, it is apparent that we have some form of tunnel-coupled unintentional dot in this system. Furthermore, there are $\sim$10 visible locations in the STM image shown in Fig. 5.9(b) where an unintentional dopant may have incorporated into the surface, so this mechanism seems likely.

Asymmetry of the source-drain tunnel junctions: The dimensions of the source and drain tunnel junctions in this device are not equal. The relationship between the aspect ratio of the tunnel gap and the resistance of the tunnel gap shown in Fig. 4.36(e) on pg. 163 was derived empirically from devices in which the source and drain tunnel barriers were symmetric. The asymmetry in the tunnel gap dimensions of this device may therefore affect the tunnelling resistance which, through lifetime broadening of the electron energy, affects the shape of the Coulomb diamonds in the stability diagram.

Of course, these three mechanisms are not mutually exclusive, and we may be seeing them acting concurrently. This would account for the more than four-fold increase in gate capacitance between the simulated and measured plunger gate capacitance (without a surface gate). However, we know from the modelling results in the previous chapter that FastCap includes a capacitance component to ground when calculating the self-capacitance of the dot, so that $C_\Sigma \neq C_D + C_{PG} + C_S$. Therefore, we do expect some inherent discrepancy between the measured and simulated gate capacitance, even in the absence of dopant diffusion or tunnel-coupled traps. As such, we believe the smaller than expected charging energy is predominantly caused by a tunnel coupled trap, replicating the Coulomb diamonds at approximately the mid-point of the expected location of the diamonds in the stability plot, where diffusion of the dopants during the oxidation has decreased the charging energy of the dot.

5.5 Switching in the gating action of the surface-gated SET

In Sec. 5.4.3 we saw discontinuous changes in the effective gate potential of the surface-gated STM-patterned SET. In this section, we perform a detailed analysis of these switching events, and discuss their implications for surface-gated STM-patterned devices.

5.5.1 Interaction between traps and surface-gated SETs

To assess the stability of surface gated devices, we performed the same repeated gate-sweep experiment as performed on the in-plane gated device in the previous chapter. For this, we swept over approximately the same number of peaks (∼14). Note that this corresponds to a smaller range of electric fields than the in-plane gated device; therefore, if switching effects are indeed 'activated' by an electric field (see e.g. the supplementary information of Fuhrer *et al.* [22]), we must be careful about comparing the number of switches between devices. We chose to use the same number of peaks in preference to the same electric field because, in the end, this is a more relevant measure of gate performance in a quantum dot.

The results of this experiment at $4K$ are shown in Fig. 5.15(a). At first, the location of Coulomb blockade peaks in this plot appears substantially more random than for the in-plane gated device in Chapter 4. We show a narrower gate range ($-4.1V < V_g < -4.0V$) in Fig. 5.15(b), highlighting two Coulomb blockade peaks. Here we see multiple large switches within the swept range, indicating greater instability than for an equivalent sweep at $4K$

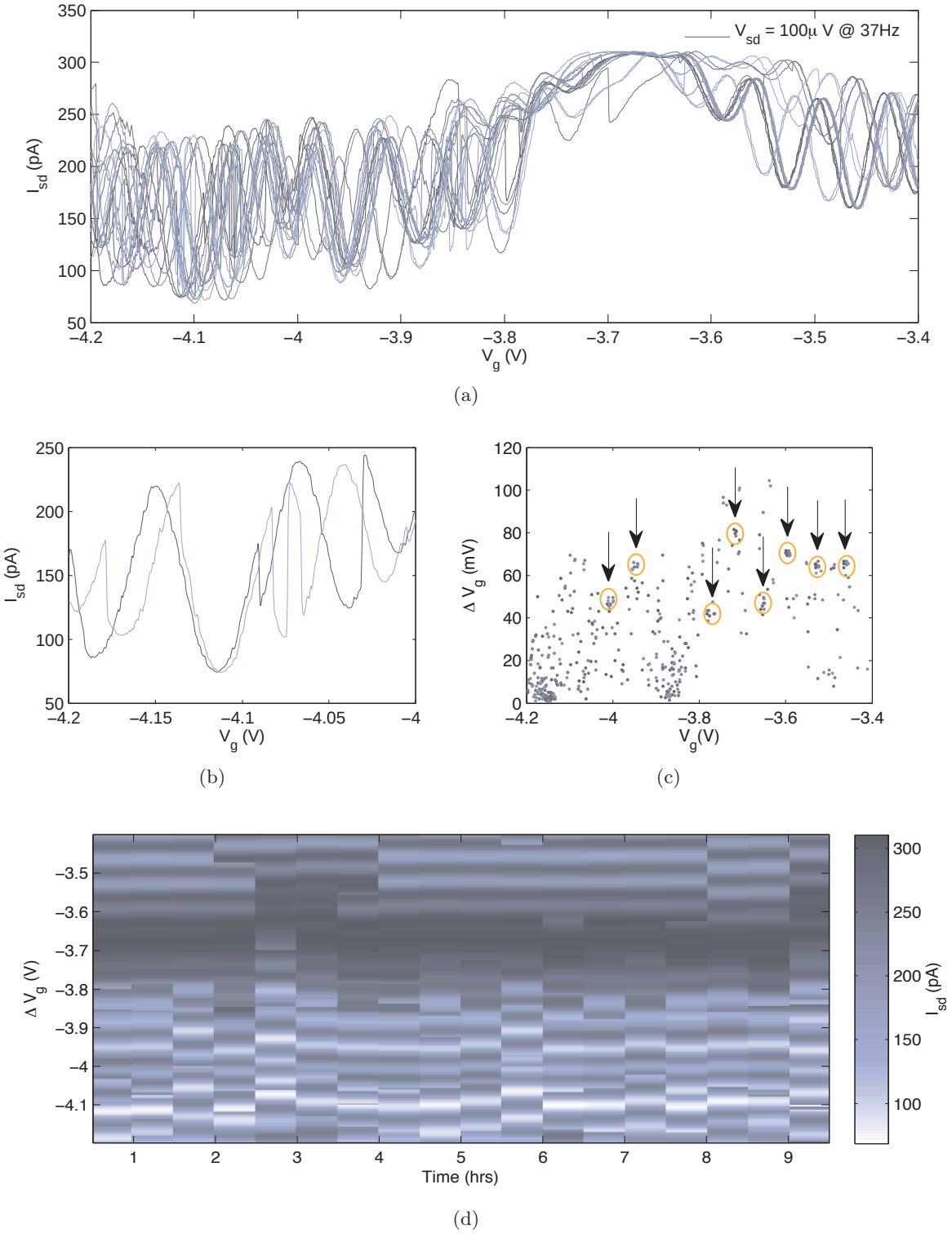
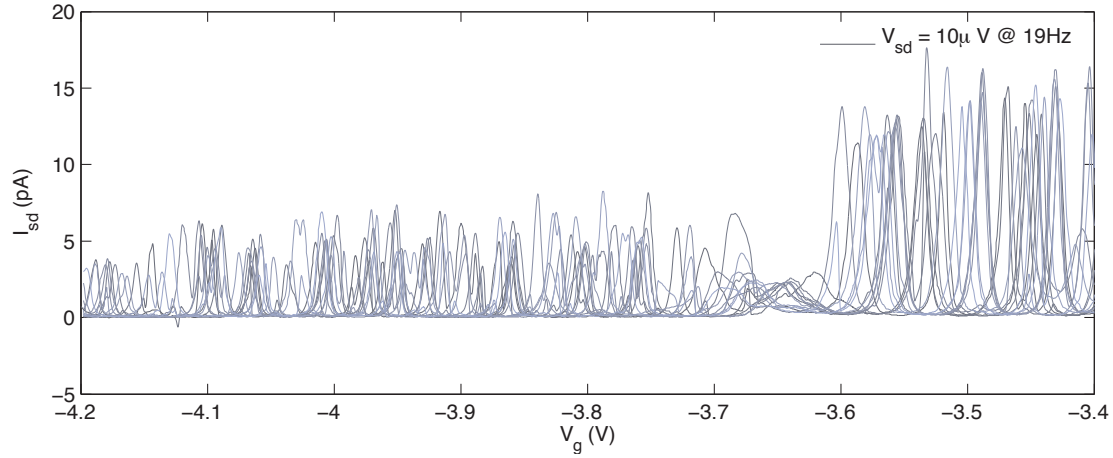
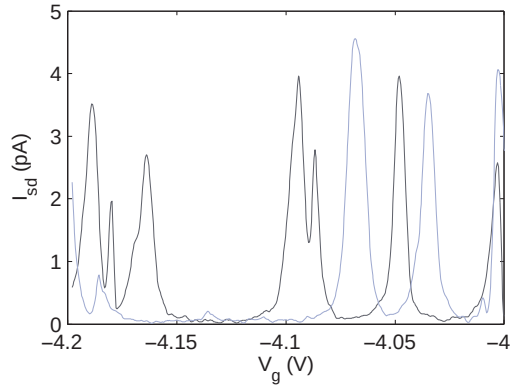


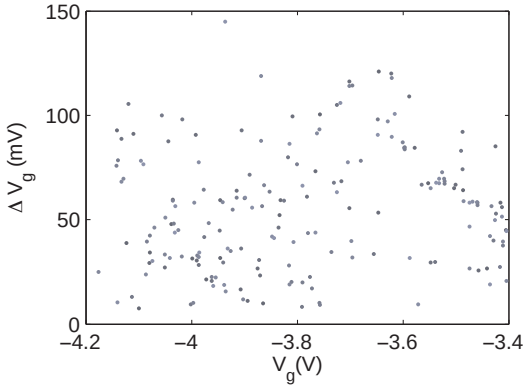
Figure 5.15: Measuring switches in the loction of the CB peaks of the surface gated device at 4K. (a) Multiple CB sweeps taken over the same surface gate voltage range at $V_{sd} = 100\mu V$. (b) Zoomed view of the CB sweep data showing several peaks with clear switches in the peak location. (c) Mapping the distance between successive peaks across the gate voltage range for each sweep. (d) Plot of the Coulomb blockade sweeps in (a) spread out in a 2-D map against the time each sweep was taken.



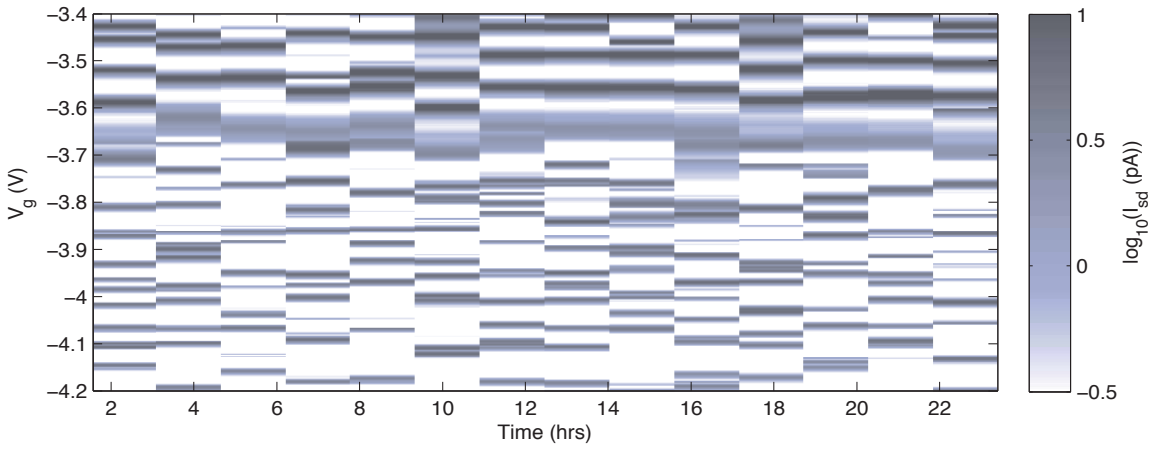
(a)



(b)



(c)



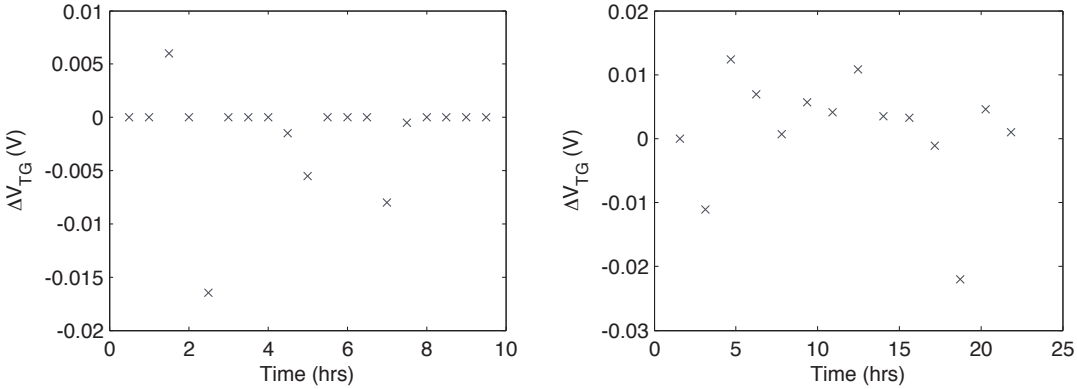
(d)

Figure 5.16: Measuring switches in the loction of the CB peaks of the UHV oxide surface gated device at base temperature. (a) Multiple CB sweeps taken over the same surface gate voltage range at $V_{sd} = 10\mu V$. (b) Close-up view of the CB sweep data showing several peaks with clear switches in the peak location. (c) Mapping the distance between successive peaks across the gate voltage range for each sweep. (d) Plot of the Coulomb blockade sweeps in (a) spread out in a 2-D map against the time each sweep was taken.

of the in-plane gated device. We show the switch magnitude as a function of the gate voltage in Fig. 5.15(c); the scatter between points in this figure is so high that we can only highlight those peaks that remain relatively *unaffected* by switches. Given that the applied gate field here is less than that used for the in-plane gate, we can safely conclude that the situation would only be worse at equivalent fields if indeed traps are 'activated' beyond a threshold field as Fuhrer *et al.* assert [22].

We present the same data as a 2-D map against time in Fig. 5.15(d), where we see a large scatter and drift in the location of switching events. We see an average of 10–12 switching events within a given sweep, compared with < 5 for the in-plane gated device. Furthermore, the magnitude of the switch in the gate voltage axis is greater in this device (as evident in Fig. 5.15(c)). There are no clearly correlated switching events visible in this map. For this reason, there are likely many weakly-coupled traps that populate with the changing gate potential. This is consistent with the increase in stray desorption seen in Fig. 5.9(b), which would lead to unintentional dopants in the substrate near the dot.

At base temperature (Fig. 5.16(a)) the CB peaks become sharper and separated, but still we see many switches and a large spread in the peak location. Again, we show a representative of the switching behaviour in Fig. 5.16(b), and plot the magnitude of the peak spacing in Fig. 5.16(c). Generally, we conclude that switching in the gating action appears more frequent (0.6 switches/peak) and more extreme ($\sim 0.8e$) in this device than the in-plane gated device reported in the previous chapter (0.06 switches/peak and $\sim 0.2e$) when measured at base temperature. The fact that the number of switching events does not decrease with temperature, as it did with the in-plane gated device in the previous chapter, is consistent with the conclusion of the previous chapter in which we attributed these switching events to nearby dopants. There was no visible stray desorption in the STM image of the in-plane gated device with the three adjacent dimers required for a donor to incorporate into the substrate. The dopants coupled to the in-plane gated device are therefore likely to be from background doping in the substrate, and therefore physically far from the device. As such, these substrate dopants are populated and depopulated by thermionic emission. In comparison, the surface-gated device in this chapter shows ~ 10 candidate sites in which an unintentional dopant might incorporate into the substrate. This number is also of the same order as the number of switches seen in this device per gate sweep. Furthermore, since these sites are close to the device, they can be populated and depopulated by tunnelling events, and therefore would not be affected by the device temperature. We therefore attribute the increased number of switching events in this device to the high density of unintentional dopants, as a consequence of stray desorption during the STM lithography.



(a) 4K (b) Base

Figure 5.17: Drift in the gate action of the surface gated SET over time. (a) At $4K$, there does not appear to be any discernable drift in the location of the blockade peaks. (b) At base temperature, there is even more uncertaintly in the location of the peaks over time, with no discerable drift.

Because we cannot anneal tips in the STM-SEM system, these unintentional dopants from stray desorption are common (see for example STM images of the surface gated tunnel gap in Fig. 5.5, and the curved-gate SET in Fig. 5.6(a)). However, work is underway within our group to develop a means of removing the oxide from the STM tips before loading them into the UHV system.

5.5.2 Charge offset drift in surface gated SETs

From the 2-D maps used in the switching study, there is no obvious overall drift in the Coulomb peak location. We have extracted the offset between each successive gate sweep numerically from both the $4K$ and base temperature 2-D switching maps, which we show in Fig. 5.17. There is no discernible trend at either temperature. Since drift is caused by an ensemble of many trapping and detrapping events far from the device, we concluded in Chapter 4 that drift was likely to be dominated by interface traps in the native oxide ($N_{it} > 10^{12} cm^{-2}$), which are both great in number and far from the device. We have shown in Chapter 3 that the interface trap density of the low temperature oxide is $N_{it} < 4.3 \times 10^{11} cm^{-2}$. It is therefore expected that drift should be lower in this device, as we find experimentally in Fig. 5.17. However, we must be mindful that any drift in this measurement may not be visible amongst the multitude of switching events arising from the higher density of unintentional dopants.

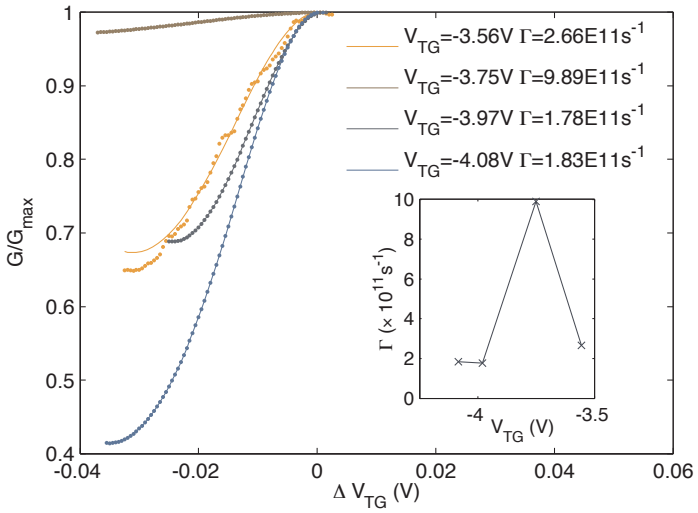


Figure 5.18: Determination of Γ for blockade peaks used for noise analysis at 4K. Here we show each of the Coulomb blockade peaks used in this noise analysis at $T = 4.2K$, where we varied Γ to fit each peak, with the Γ value used for each gate voltage shown in the inset.

5.6 Charge noise in the surface gated SET

In the previous chapter, we converted from noise in the device current to fluctuations in the dot potential using the shape of the thermally-broadened peak. In order to convert from the device current to the dot potential, we must know the peak shape precisely. In the surface-gated SET in this chapter, the peak shape varies considerably from peak to peak because of lifetime broadening of the electron energy. For this reason, here we have recorded a Coulomb blockade sweep of each of the blockade peaks to be used in the noise analysis, which we have fit using the thermal and lifetime broadening formulae of Eq. 5.5, as shown in Fig. 5.18 and Fig. 5.19. The transmission rate (Γ) through the dot at each gate voltage is shown in the inset of each figure, which was extracted from the fit to each peak. Note that at $4K$, the peak at $V_{TG} = -3.97V$ coincides with a maximum in the beating pattern of the peaks, so this peak is broader and flatter than the other peaks shown. As a consequence, any fluctuations in the dot potential give a smaller change in the device current on this peak. We have used these peak fits to convert from current to dot potential, and then to perform the same noise analysis as in the previous chapter. First we acquire the device current at a fixed drain bias at several Coulomb blockade peaks (Fig. 5.20(a) and Fig. 5.21(a)). Notably, there is also very little drift in any of these traces, which supports the claim made in the previous section that drift is minimal in this device because of the reduced interface trap density. In the time traces of Fig. 5.20(a) and

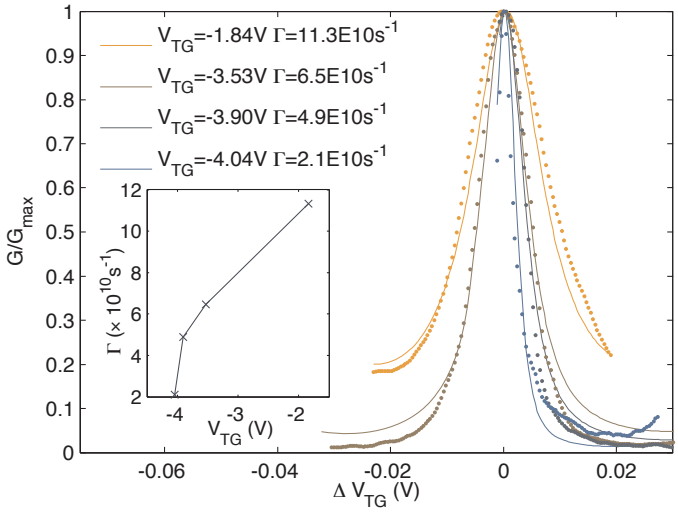


Figure 5.19: Determination of Γ for blockade peaks used in noise analysis at base temperature. Here we show each of the Coulomb blockade peaks used in this noise analysis at base temperature, where we have set $T = 550mK$ and varied Γ to fit each peak, with the Γ value used for each gate voltage shown in the inset.

Fig. 5.21(a), again we see fluctuations are larger in the base temperature data, since the base temperature peaks are sufficiently sharp that small deviations in the dot potential cause large variations in the device current. We also see a unique feature in the $4K$ data at $V_{TG} = -4.08V$ — there is a strong RTS with an amplitude of $\sim 4.5pA$ and a period of $\sim 5min$. This RTS is indicative of strong coupling to a nearby trap. Other than this single RTS, the time traces at $4K$ are very flat, with little visible drift and typically one switch throughout the measurement. For this reason, much of the data shown coincides with the apex of the Coulomb blockade peak — since the device did not drift away from this starting point throughout the measurement. As such, fluctuations in the dot potential have little influence on the device current, and the noise in the $4K$ sweeps especially are dominated by the background Johnson noise.

The fluctuations in the dot potential are shown in Fig. 5.20(b) and Fig. 5.21(b). Each peak has a unique shape because of the unique degree of lifetime broadening. The resultant time series of the dot potential (Fig. 5.20(c) and Fig. 5.21(c)) were used to calculate the probability distribution (Fig. 5.20(d) and Fig. 5.21(d)) and power spectral density (Fig. 5.20(e) and Fig. 5.21(e)). Again we see the power spectral density plots (Fig. 5.20(e) and Fig. 5.21(e)) show virtually no frequency dependence at $4K$, and a strong $1/f^{\alpha}$ dependence at base temperature where $\alpha = 1.7$. This indicates that frequency independent Johnson noise dominates the measurement at $4K$, which reduces with temperature (since it is caused by thermal fluctuations in the carrier distribution) so that a $1/f^{1.7}$ dependence

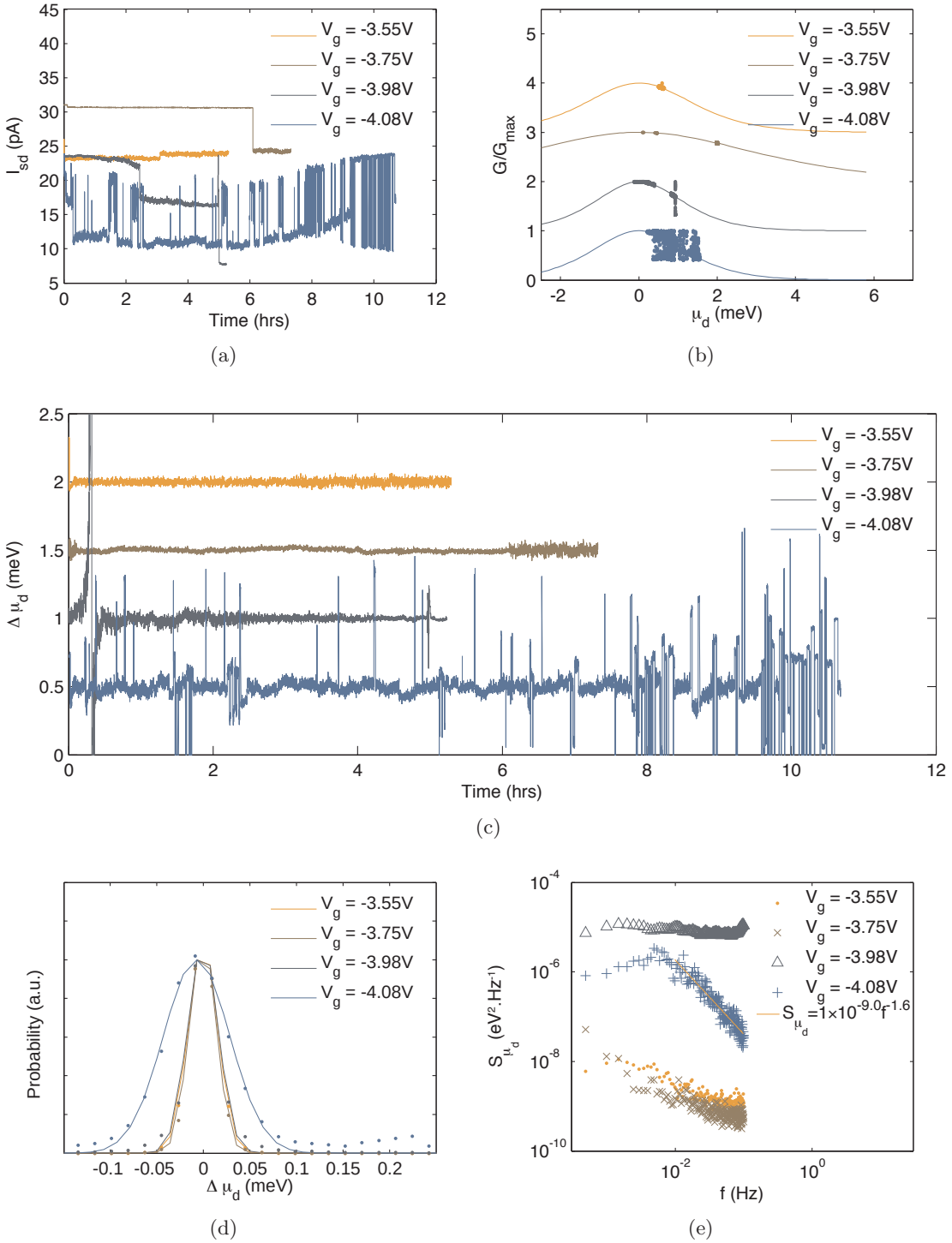


Figure 5.20: Conductance noise of the surface gated gated SET at 4K. (a) Measured SET current with time for four different gate voltages showing noise in the current. (b) Mapping the time series data in (a) to the equivalent dot potential. (c) Using the trace in (b) to extract the dot potential as a function of time. (d) Probability distribution of the dot potential at each gate voltage from (c). (e) Power spectral density of (c) calculated for each time sweep.

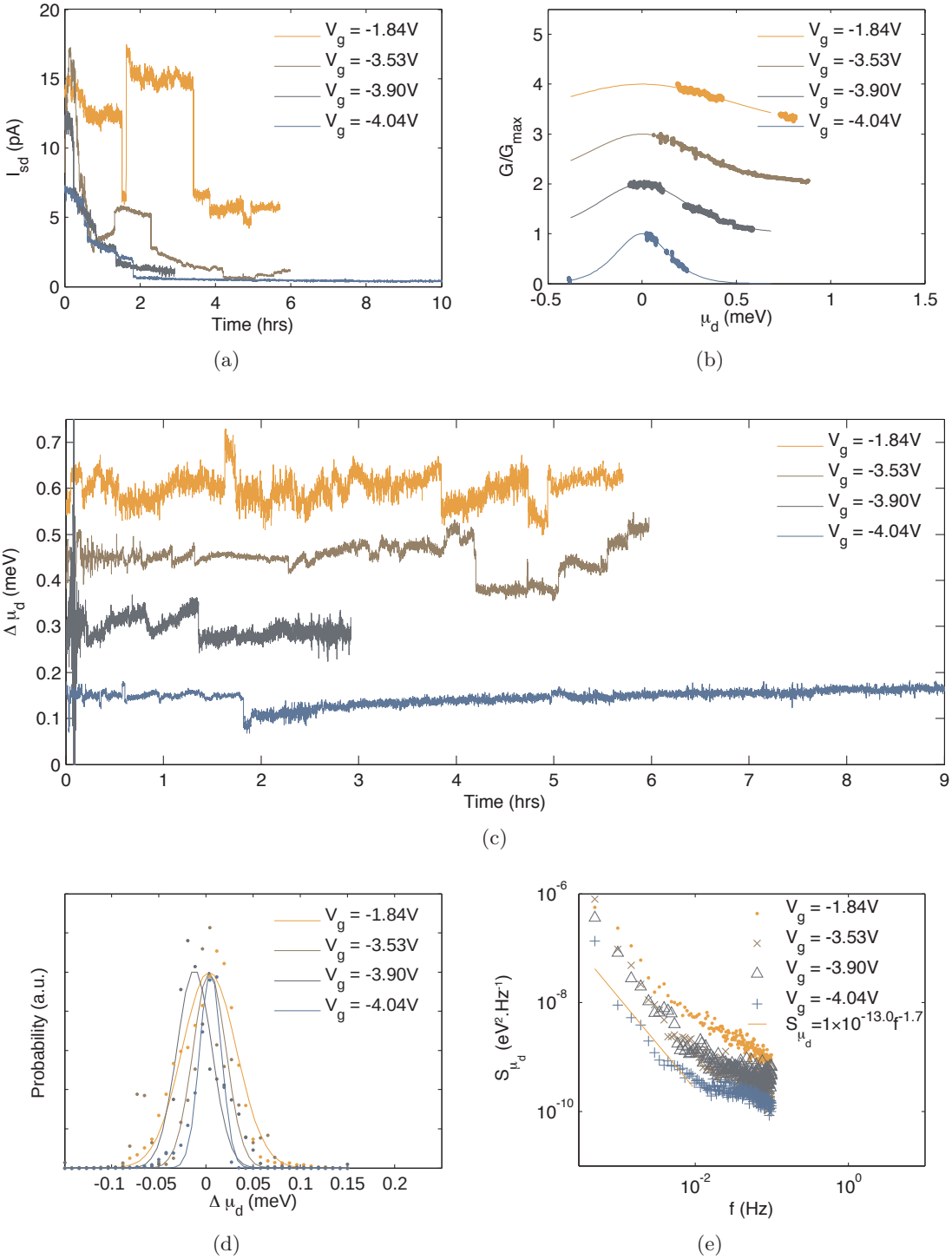


Figure 5.21: Conductance noise of the surface gated gated SET at base temperature. (a) Measured SET current with time for four different gate voltages showing noise in the current. (b) Mapping the time series data in (a) to the equivalent dot potential. (c) Using the trace in (b) to extract the dot potential as a function of time. (d) Probability distribution of the dot potential at each gate voltage from (c). (e) Power spectral density of (c) calculated for each time sweep.

Table 5.2: Standard deviation of surface-gated dot potential compared over the gate voltage range at base temperature and 4K (a) Results form $4K$ study shown in Fig. 5.20(d). (b) Base temperature results shown here for comparison, which are discussed later in this section.

(a) $4K$

V_{TG} (V)	σ_{μ_d} (meV)
-3.55	0.015
-3.75	0.015
-3.98	0.016
-4.08	0.085

(b) Base

V_{TG} (V)	σ_{μ_d} (meV)
-1.84	0.029
-3.53	0.017
-3.90	0.019
-4.04	0.013

is visible at base temperature. The one exception to this finding is the trace recorded at $V_{TG} = -4.08V$ at $4K$, where there is a very strong RTS in this signal ($> 50\%$ of device current) giving a strong frequency dependence in its power spectral density ($\alpha = 1.6$) even in the presence of Johnson noise.

The standard deviation in the dot potential is virtually independent of gate voltage and device temperature, as highlighted in Table 5.2(b). The notable exceptions to this (in particular at $4K$ and $V_{TG} = -4.08V$) are caused by a strong RTS in the signal, visible in the time trace of Fig. 5.20(a). Otherwise, the general insensitivity to gate voltage and temperature seems to indicate that the noise sources in this device are not thermally activated. That is, the noise in this device may be dominated by tunnelling to traps, not thermionic emission and capture of electrons from those traps, as was the case for the in-plane gated device. This indicates that the sources of noise in this device are physically close to it, especially for the fluctuator that causes the RTS, since it gives a very strong fluctuation in the device current ($> 50\%$). This RTS in particular is a good indication that charging of the unintentional dopants within the substrate has an inherent transience, contributing to the charge noise of the device.

Table 5.3 summarises the noise analysis of the in-plane gated device from the previous chapter and the surface gated device form this chapter (at base temperature). Again, we state the noise magnitude (both σ_{Q_d} and S_{Q_d}) as a fluctuation in the dot charge rather than the dot potential (σ_{μ_d} and S_{μ_d}), since this is a device-independent measure of charge noise, given that the charging energy differs between the two dots. From Table 5.3 we can see that, at the base fridge temperature, σ_{Q_d} of the surface gated device is larger (0.005e

Table 5.3: Comparing the noise performance of in-plane and surface gated devices. Here we show the standard deviation (σ_{Q_d}), power spectral density at $1Hz$ (S_{Q_d}), corner frequency of the power spectral density curve (f_c) and the slope of its roll-off (α where $S_{Q_d} = A/f^{\alpha}$) relative to the in-plane gated device of Chapter 4

Device	σ_{Q_d} (e)	S_{Q_d}@1Hz ($e^2.Hz^{-1}$)	f_c (Hz)	α
In-plane gated (Chapter 4)	∼0.002	3.1×10^{-8}	$\sim 3 \times 10^{-3}$	1.8
Surface gated (this chapter)	∼0.005	1.1×10^{-8}	$< 1 \times 10^{-3}$	1.7

vs 0.002e). From the value of σ_{Q_d} we conclude that the total noise magnitude is greater in this device over the measurement bandwidth used (which was the same for the two devices). The values of $S_{Q_d}@1Hz$ are also shown, where it would appear that the value of $S_{Q_d}@1Hz$ is much smaller in the surface gated device. However, we must be aware of the fact that the corner frequency of the surface-gated device PSD is lower ($< 1mHz$ vs $3mHz$), which forces down the value of S_{Q_d} at higher frequencies. The exponents of the respective frequency-dependences in S_{Q_d} for the two dots are approximately equal ($S_{\mu_d} \propto 1/f^{1.8}$ versus $S_{\mu_d} \propto 1/f^{1.7}$). From this power spectral density analysis we can conclude that the frequency dependence of the noise in the two samples is qualitatively the same, and quantitatively of the same order of magnitude. From this analysis we conclude that, despite the presence of nearby unintentional dopants in the substrate from stray desorption, the charge noise in the surface-gated device is not significantly different from the in-plane gated device in the previous chapter. This bodes well for the use of surface gates in STM patterned devices that are sensitive to charge noise, such as SETs used to probe the charge state of phosphorus qubits in a silicon substrate.

Having quantified the electrical performance of the surface-gated SET, and in particular the stability and noise of this device, in the next section we provide a summary of the key differences between in-plane gates and surface gates for STM-patterned devices.

5.7 Key differences between surface gated and in-plane gated STM-patterned devices

It is important to understand the relative advantages and limitations of in-plane gates and surface gates when designing STM-patterned devices, both in selecting the best gate

architecture for an application, and in quantifying the associated design constraints. Here we discuss the differences between gating architectures in the context of device design, highlighting their respective strengths. The measurements presented in this chapter emphasise several differences between the in-plane gated device of Chapter 4 and surface gated device of this chapter, here we focus on:

Gate range: Accounting for both the maximum electric field achievable and the consequences of exceeding this range.

Hysteresis and switching: Where there are non-deterministic or non-ideal contributions to the gate action that arise from traps and imperfections in the gate dielectric, or the surrounding substrate.

Fabrication differences: In which the fabrication process affects the distribution of dopants or the optimum placement of a gate.

It is important to consider the gate range in the design of STM-patterned devices to guarantee the gate has the desired effect; for example, to ensure there are visible charge transitions in the operation of an SET intended as a charge detector. Hysteresis and switching, on the other hand, are associated more with the reliability and reproducibility of a device, complicating the gating action with non-deterministic effects. Fabrication issues affect the design in an indirect way; while a given architecture may be favoured by the design process, eccentricities of the fabrication process itself can markedly affect these decisions. In this section we explore such differences and discuss their implications in the design of future devices.

5.7.1 Comparing the gating range of surface gates and in-plane gates

Figure 5.22 is a compilation of all published gate leakage data from STM-patterned quantum dots, including data from the 4000e dot published by Fuhrer (AF) [22], the top-gated device published by Lee (WL) [215], the $\sim$200e in-plane gated device (Chapter 4) and $\sim$250e surface-gated device (this chapter) discussed in this thesis, and the 7e dot published by Füchsle (MF) [23]. The in-plane (or plunger) gates (PG) are distinguished from the surface (or top) gates (TG). Note that the device of Füchsle *et al.* had two in-plane gates, labelled PG1 and PG2. We have excluded the in-plane gate leakage of Lee's device, since this was found to vary as a function of the surface gate, and will be described in greater detail later in this section. The most striking feature of this plot is that, with the exception of Fuhrer's in-plane gate (AF PG), all gates reach the accepted leakage (10pA,

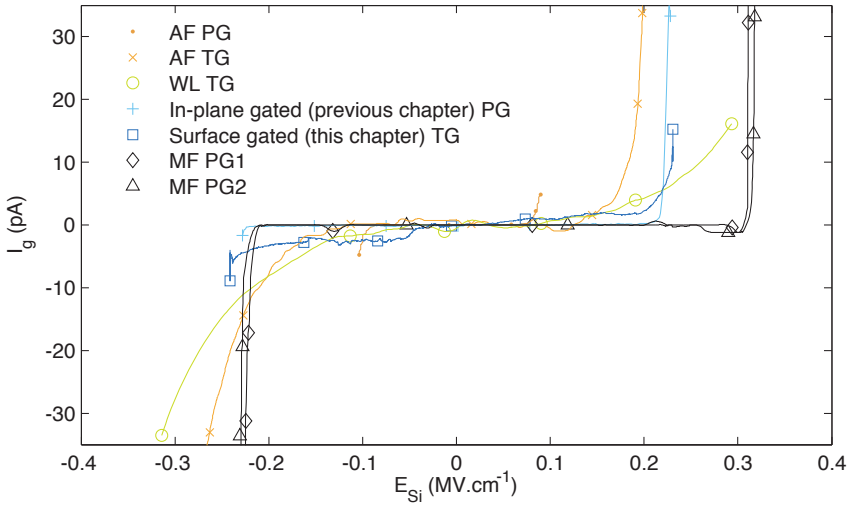


Figure 5.22: Comparing the gate range of all STM-patterned SETs. Here we show the gate range of all STM-patterned SETs, including both in-plane gates (labelled PG) and surface gates (labelled TG).

see Sec. 3.2.1) at similar electric fields (± 0.2–$0.3 MV.cm^{-1}$). To underline the significance of this result, let us explore the differences between the samples.

Constructing a geometry-independent comparison of gate leakage

The independent variable (x-axis) in Fig. 5.22 is the applied electric field, which we use in preference to the applied gate voltage because the induced electric field is a geometry-independent measure of the gate range. For in-plane gated devices, the electric field is simply calculated from the applied gate voltage divided by the gate separation. In this we neglect any voltage dropped across the metallic contacts and STM-patterned leads, since each STM-patterned lead is connected to two metallic contacts and the resistance between them is on the order of 5–$100k\Omega$, whereas the effective resistance implied by the gate leakage is $\gg 1G\Omega$. Calculating the induced field for surface-gates is more complex, since there is an intrinsic layer of silicon separating the device from the oxide that acts as a series capacitance. A simple series capacitor model gives

$$E_{Si} = V_g \frac{\kappa_{SiO_2}}{\kappa_{SiO_2} t_{Si} + \kappa_{Si} t_{SiO_2}}, \tag{5.6}$$

where E_{Si} is the electric field induced in the silicon, V_g is the applied gate voltage, $\kappa_{SiO_2} = 3.9$ is the dielectric constant of the oxide, $\kappa_{Si} = 11.9$ is the dielectric constant of silicon, t_{Si} is the thickness of the intrinsic silicon layer, and t_{SiO_2} is the thickness of

the oxide. To remove any dependence on device geometry, the leakage is best expressed in units of current *density* rather than raw current. This is not possible in Fig. 5.22 since the effective gate area is poorly defined for in-plane gates; in-plane gates apply an electric field to the device from the edge of 2-D sheets of dopants that sit in a single atomic plane, and therefore the distribution of the electric field is dominated by fringing effects at the edges of the gate. As such, we plot only the leakage current.

Qualitatively, the in-plane gates consistently show an abrupt change in current at a particular field ($-0.2MV.cm^{-1}$), which is consistent with breakdown of the substrate under an applied electric field rather than tunnelling through the substrate. There is some asymmetry in the breakdown field, particularly in MF PG1 and MF PG2, which have a negative and positive break down field of $-0.22MV.cm^{-1}$ and $0.33MV.cm^{-1}$. Based on the study by Pok [168, pg. 154], asymmetry in the leakage occurs in the presence of geometric asymmetries in the device. For this 7 donor dot we might therefore expect the relative asymmetry to be greatest, because it is the smallest of the dots. However, generally the leakage is insensitive to the separation between the gate and device beyond $\sim 45nm$, since the leakage is very similar for gate separations of $44nm$ (MF PG1) to $68nm$ (in-plane gated device from Chapter 4). This supports the claim that for in-plane gated devices, the leakage is caused primarily by breakdown rather than tunnelling, since tunnelling would be exponentially sensitive to the gate separation.

In-plane gate leakage mechanisms

The breakdown field in all devices is too small to be attributed to band-to-band tunnelling, which has little effect below $0.5MV.cm^{-1}$ (see, e.g. [217, Fig. 4]). Below $0.5MV.cm^{-1}$, avalanche breakdown dominates. At milli-Kelvin temperatures, the breakdown process is likely caused by impact ionisation of shallow donor states. Impact ionisation typically occurs above $0.1MV.cm^{-1}$ in silicon, when carriers gain enough kinetic energy from the applied electric field to generate an electron-hole pair ($E_i > E_g \simeq 1.1eV$) [42, Fig. 2.6]. In a substrate where carriers are frozen out at low temperatures however, carriers need only gain enough energy to ionise a donor ($E_i > E_d \simeq 45meV$ for $Si{:}P$). In support of this view, we also see impact ionisation of MOSFETs on these substrates at $4K$, which gives a pronounced step in the device current at high source-drain biases [218]. As such, we know impact ionisation is prevalent in our substrates at electric fields of $\sim 0.1MV.cm^{-1}$. In addition, in a similar way to substrate breakdown in these MOSFETs, breakdown of an in-plane gate has no lasting influence; the gating action is restored by returning the gate bias to an acceptable level.

When in-plane gates are brought closer to the device, Fowler-Nordheim tunnelling dominates. For example, the leakage current of Fuhrer's in-plane gate (AF PG) reaches $5pA$ at just $\pm 0.1 MV.cm^{-1}$, since the gate separation is small ($38nm$). This indicates that a gate separation of $\sim$50–60nm for in-plane gated devices is required to reach the breakdown electric field of the silicon substrate.

Surface gate leakage mechanisms

In contrast to in-plane gates, surface gates do not generally show the same abrupt upturn in current at $E_{Si} = 0.2 MV.cm^{-1}$. This implies that the oxide does not break down before reaching the accepted gate leakage threshold ($10pA$). The leakage we do see is dominated by tunnelling through the oxide, and is therefore proportional to the gate area. With a potential barrier of $>3eV$, surface gates can theoretically be patterned closer to the device than in-plane gates before tunnelling has an influence. This is important for example in the Kane architecture, where gate selectivity is key. However, we must scale the gate area to keep the leakage below the accepted threshold ($10pA$). All top gates presented in this thesis were large compared to the STM-patterned device (0.4–2μm on a side), although these dimensions were used deliberately as a precaution against mis-alignment of the gate. We could easily push the gate to smaller dimensions (say, $200nm$ on a side) given our alignment accuracy of $\sim$100nm. Since the gate leakage is proportional to the gate area, this would reduce the leakage up to 100-fold, so that we could operate the device at lower currents (e.g. $1pA$) without complications introduced by leakage from the gate.

The notable exception to tunnelling-dominated leakage through the oxide is highlighted by the leakage of the surface gated device introduced in this chapter ('Surface gate (this chapter) TG' in Fig. 5.22), where there is a step-change in leakage (to $\pm 2pA$) at a field of $\pm 0.075 MV.cm^{-1}$. This is consistent with the field required to induce an accumulation or inversion layer at the silicon-oxide interface. It seems therefore that the oxide in this device is leaking to the induced layer at this field, and it is actually the $\sim$20nm thick silicon layer that is acting as the primary gate dielectric. This is supported by the fact that, at an applied silicon field of $\sim 0.2 MV.cm^{-1}$, there is a sharp increase in the gate leakage, consistent with the breakdown of the silicon substrate rather than tunnelling through the oxide.

Further to leakage in the oxide, we have seen in earlier studies using C-V capacitors and MOSFETs that exceeding 2–3$MV.cm^{-1}$ causes permanent breakdown, which does not recover in the same way as an in-plane gate following a breakdown event. We have not pushed these valuable STM-patterned devices to such fields, but it is fair to expect a

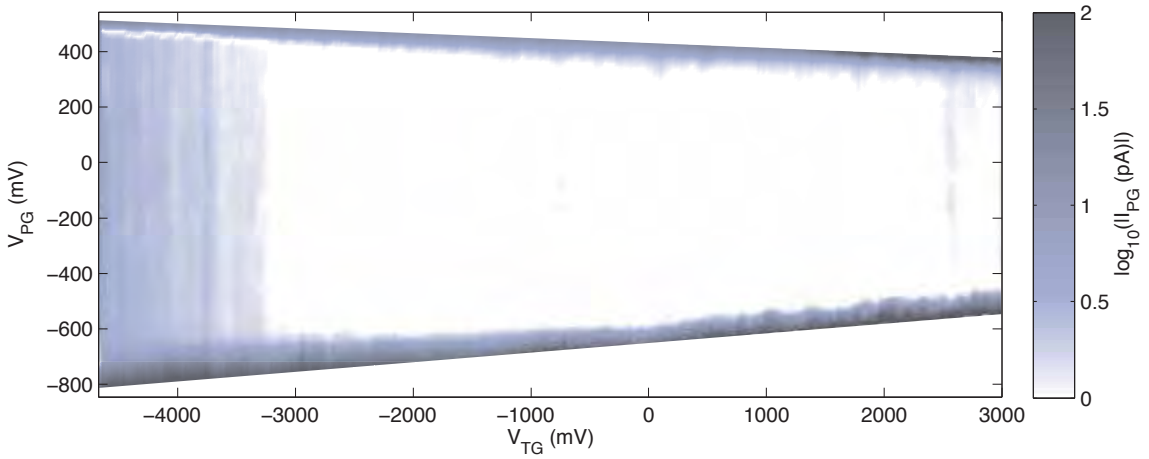


Figure 5.23: Leakage of in-plane gate of the 700e surface-gated SET in gate-gate space. Here we see the range of the in-plane gate increase as the surface gate is pushed to the negative limits.

similar breakdown field range. By the relation given in Eq. 5.6, this equates to a silicon field of 0.66–1$MV.cm^{-1}$. However, we know from the work of Majamaa *et al.* that oxides grown with the RF-generated atomic oxygen are robust to fields of 10$MV.cm^{-1}$ [93]. This implies that we can expect to further optimise the co-deposition method in the future to achieve higher quality oxides with a greater field range.

Interaction between surface gates and in-plane gate leakage

We have seen that a surface gate affects the transparency of the source-drain tunnel barriers. In a similar way, it also affects the leakage of the in-plane gate. The clearest example of this is shown in Fig. 5.23, where the gate leakage of the curved gated dot is plotted as a function of the surface gate and in-plane gate voltages [215]. The range of the in-plane gate clearly increases as we take the surface gate to more negative voltages. This is because negative surface gate voltages increase the barrier height of the in-plane gate, reducing the leakage current.

In addition to the maximum applicable field, the geometry of a gate also affects the gate action. In particular, maximising the effective gate area enhances capacitive coupling to the device. In this way, surface gates have a natural advantage in that they are more strongly coupled to the device, given their parallel-plate structure, compared to the edge-to-edge coupling of in-plane gates. A corollary of this is that, when a surface gate is added to the device, the capacitance of the in-plane gate can change considerably in the presence of the large surface gate capacitance. These geometric consideration will be

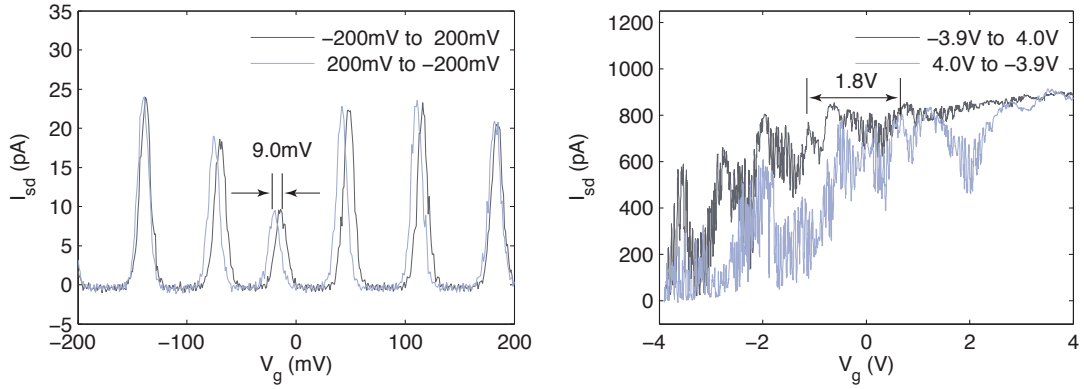
discussed further in a subsequent section; next we address how the presence of a surface gate introduces parasitic charges, affecting the stability of the dot.

5.7.2 Hysteresis and switching in surface gates and in-plane gates

Ideally the gate of an SET is perfectly capacitively coupled to the dot, so that any change in the gate potential affects the dot proportionally. Experimentally we often see a transient or non-deterministic offset in the dot potential, specifically in the form of switching and hysteresis. We attribute this to parasitic charges near the dot, where the population and depopulation of these charge centres leads to variations in the dot potential. Here we distinguish between switching and hysteresis, and discuss their respective causes.

Switching events in STM-patterned SET's

As the gate potential is swept, it is possible to make it energetically favourable for an electron to tunnel to or from a trap nearby. There is an inherent transience associated with this process, as the trap equilibrates with changes in the gate potential. In an identical manner to the charging of the dot, it is common for electrons to sequentially tunnel into the trap (e.g. from the gate), and then back out (to the drain, dot, or source leads in this example). Depending on the tunnelling rate to and from the trap, it is therefore possible to resolve discrete changes in the trap occupancy, where the trap changes, sometimes repeatedly, between the occupied and unoccupied states. Repeated changes in the trap occupancy manifest as random telegraph switching (RTS) in the device current. There are several examples of random telegraph switching throughout this thesis, where the trap occupancy seems to switch randomly between two states across a range of gate voltages. An RTS has a power spectral density that varies in proportion to $1/f^2$, whereas an ensemble of many such switching events gives a spectrum that varies with $1/f$. We have seen a mixing of these two effects in samples measured in this thesis, with the power spectral density changing in proportion to $1/f^{\sim 1.8}$. We have also seen discrete switches in the location of the Coulomb blockade peaks of both devices as the gates were swept across $\sim$14 Coulomb blockade peaks. Specifically, at base temperature we saw an average of 0.06 switching events in the in-plane gated device per Coulomb blockade peak, whereas there were 0.6 for the surface-gated device, attributed to the greater density of unintentional dopants in the surface gated device.



(a) (b)

Figure 5.24: Hysteresis in the gating action of the in-plane gated and surface-gated SETs. (a) Hysteresis of the in-plane gated SET from Chapter 4. (b) Hyseteresis in gating action of the surface-gated SET.

Hysteresis in the gating action of STM-patterned SET's

When many weakly-coupled traps are populated by the gate, the sum of their respective contributions may have a measurable effect on the dot potential. Crucially, as these charges are depopulated again by sweeping the gate in the opposite direction, they create hysteresis in the gate action. That is, the effective gate voltage is dependent upon the history of the applied gate voltages. Fuhrer *et al.* found hysteresis in the action of a global top-gate on their device. There, it was clear that traps at the interface were affecting the device. Fuhrer attributed the hysteresis and instability introduced with a top gate to the change in occupancy of charge traps, which appeared to be 'activated' when the applied gate field exceeded $0.02MV.cm^{-1}$. Zimmerman *et al.* suggest that the application of large amplitude gate pulses can help to train out noise/hysteresis seen at low gate voltages [200].

We saw hysteresis in the low temperature oxide using MOSFET test devices, which we were able to eliminate using a low temperature post-metallisation anneal. Annealing STM-patterned devices might therefore eliminate the gate hysteresis. The STM-patterned device in this chapter did not undergo a post-metallisation anneal to avoid any complications with diffusion of the patterned dopants and to assess the quality of the as-grown oxide. This resulted in a hysteresis of 40–50e in the gate action, as shown in Fig. 5.24, where the $\sim$0.1e hysteresis in the in-plane gated device of the previous chapter is shown for comparison. Future experiments are planned to anneal devices to verify that the anneal eliminates hysteresis in the low temperature oxide. The ideal temperature range for annealing out defects is 350–400$^{\circ}C$ [44]. Here we would have to keep the anneal time to $\sim 15min$ to keep the diffusion of dopants to less than one lattice site ($x_j = 0.5nm$).

5.7.3 Comparison between surface gate and in-plane gate fabrication processes

The addition of a surface gate to STM-patterned devices requires additional process steps. Each step may affect the device, depending on the process parameters used. As such, there are a number of considerations that we must take into account before choosing to use a surface gate on an STM-patterned device:

1. Given the enhancements made to our clean room post-processing by Füchsle *et al.* [219], surface gates may be patterned with a precision of $\sim 100nm$, where the gate itself has a minimum size of 20–$50nm$. In comparison, we can place in-plane gates with a precision of <2–$5nm$, including the piezoelectric drift one typically sees when using an appropriate scan-frame to achieve the desired dot-gate separation ($\sim 200 \times 200nm$). Furthermore, we can pattern in-plane gates that are just 2–3 dimer rows wide (1.5–$2.3nm$), which are metallic even at cryogenic temperatures [220]. However, we have established that a surface gating scheme will provide greater gate selectivity, since tunnelling through an oxide is less than tunnelling through the silicon substrate, allowing us to position surface gates closer to the device than in-plane gates.

2. After encapsulating the device with $20nm$ of MBE-grown silicon at $250°C$ for $3hrs$ ($0.1nm/min$), we must then deposit a low temperature oxide on the silicon encapsulation layer for surface gating. Though the device is kept at low temperatures throughout this process (typically <$160°C$), some diffusion of the patterned dopants is inevitable because elevated temperatures thermally activate diffusion (we estimate $x_j < 0.5nm$ from the model in Fig. 3.1 on pg.42). However, diffusion of the dopants is exacerbated by the process of oxidation, which is known to introduce defects at the surface that may propagate into the substrate and enhance dopant diffusion [221, 222]. We have seen evidence of unexpectedly high dopant diffusion in this chapter; specifically that the tunnel gap resistance of the surface gated device was less than expected from the aspect ratio study of Pok on pg.114 ($R_t \simeq 200k\Omega$ vs. $R_t = 1M\Omega$ theoretically).

3. Once removed from the UHV fabrication system, we must remove the UHV-grown oxide from areas where we intend to make Ohmic contact with the buried $Si{:}P$ STM-patterned electrodes. This may be done using a brief dip in hydrofluoric acid, or by increasing the time used for reactive ion etching of the contact holes. In this thesis, we trialled both but eventually elected to use hydrofluoric acid, since it does

not cause diffusion of patterned dopants, and does not damage the remaining oxide — both of which may be caused by radiation from the plasma during an RIE etch.

4. After depositing aluminium Ohmic contacts, a surface gate must be patterned on the device. This evaporation step is identical to that used when depositing the Ohmic contacts. As a consequence we are doubling the amount of thermal diffusion caused by radiative heating of the substrate when using a thermal evaporator (as we used), or the accumulation of radiation-induced defects generated within the gate oxide if using an electron-beam evaporator. However, the diffusion during a thermal evaporation is expected to be very little (x_j less than one monolayer) during the $\sim 2min$ required to deposit the aluminium gate electrode with an estimated sample temperature of $< 200°C$.

Based on these considerations, using surface gates on STM patterned devices will cause some thermal diffusion of the patterned dopants, though this should be immeasurably small according to our diffusion studies. Furthermore, surface gates cannot yet be placed with an alignment accuracy less than $100nm$, or with dimensions $< 20nm$. However, surface gates should provide an increased gate range, and/or improved gate selectivity.

5.7.4 Selecting between in-plane and surface gates in the design of future STM-patterned devices

Based on the two ∼200 donor STM patterned quantum dots presented in this and the previous chapter, the performance of the in-plane gating scheme and surface gating scheme are summarised in Table 5.4. The breakdown field using a surface gate is greater than that of the in-plane gating architecture ($> 1MV.cm^{-1}$ vs. $0.2MV.cm^{-1}$), but the surface gated device shown in this chapter proved that we may not always reach this limit, though this might be improved by a post-metallisation anneal. The frequency of switching events when sweeping the gate was an order of magnitude higher using the surface gate (0.6 switches per blockade peak vs. 0.06 switches), and the magnitude of those switches was approximately three times greater ($\sim 0.8e$ vs. $\sim 0.25e$). However, switching is believed to correspond to substrate donors and is not related to the gate architecture used. While the hysteresis in the surface gated device was more than two orders of magnitude greater than the in-plane gated device, we have shown using MOSFET test structures that this hysteresis can be eliminated using a post-metallisation anneal at $350°C$ in a hydrogen-containing ambient. Optimisation of the oxide using such anneals is an ongoing stream of development within our group. The charge noise of the surface gated device was similar —

Table 5.4: Summarising the gating performance of the in-plane and surface gate architecutres. Note that all values tabulated here were recorded at base temperature

	In-plane	Surface
Breakdown field($MV.cm^{-1}$)	0.2	> 1
Switch density (No./CB peak)	0.06	0.6
Av. switch magnitude (%e)	15–30	70–90
Hysteresis (%e)	12-15	4000-5000
Noise magnitude σ_{Q_d} (%e)	0.2	0.5

both qualitatively and quantitatively — to the in-plane gated device, indicating that the charge noise witnessed in these devices is not dominated by the gate architecture itself.

If the hysteresis can be annealed out of the low-temperature oxide and the macroscopic defects within the oxide can be avoided, either by changing the growth conditions or by moving the sample further from the silicon sublimation source during the oxide growth to minimise spitting from the silicon source, we can expect the breakdown field of the oxide to be consistently $> 3MV.cm^{-1}$. In this scenario, the surface gating scheme offers a larger gating range. It is possible that by annealing out the hysteresis we also reduces drift or charge noise within the device. It is also possible that by scaling down the size of the surface gate, we can reduce the gate leakage. Even if this is not the case, surface gates are still suited to global static control gates, used for example to pinch off the tunnel barriers of a quantum dot.

5.8 Chapter summary

The 4000 donor in-plane gated quantum dot published by Fuhrer *et al.* was the first study of surface gates on our STM-patterned devices, using the native oxide as a dielectric. The surface gate in Fuhrer's device showed greater instability and hysteresis than the in-plane gate, indicating that coupling to traps at the interface adversely affected the stability of the device. It was hoped that by replacing this native oxide with the low-temperature UHV oxide developed for this thesis we could minimise the instability of these surface gates. However, initial surface gated SETs made with the UHV dielectric showed many switching events [215]. To make a more direct comparison with the in-plane gating scheme,

we decided to make a $\sim 200e$ surface-gated device constructed with the same STM pattern file as the ~ 200 donor in-plane gated device in Chapter 4, using a $50nm$ low temperature oxide as a gate dielectric and a $1.5 \times 2\mu m$ global aluminium surface gate.

The surface gated device had a gate range of $\sim |V_{TG}| < 4.5V$, which remained constant over successive cool-downs. Because of the parallel-plate coupling of the surface gate to the device, it could tune the dot occupancy by more than five times that of the in-plane gated device in Chapter 4, changing the electron density by $\sim 150e$ compared to the $\sim 30e$ accessible using the in-plane gate structure from the previous chapter.

Experimentally, we found it difficult to accurately measure the charging energy of this surface gated SET, because all features in the stability plot were smeared out by thermal and lifetime broadening of the electron energy levels. We were able to extract an upper limit on the sum capacitance of $< 40aF$ (c.f. $8.7aF$ from numerical modelling). This discrepancy between the measured and modelled capacitances is attributed to two possible causes: thermally-activated diffusion of the STM-patterned dopants, or strong tunnel-coupling between the dot and a nearby trap. It seems plausible that both effects might act concurrently since there was a clear beating pattern in the Coulomb blockade sweep using the surface gate, indicative of a strongly tunnel-coupled trap, and the tunnel barrier resistance was less than expected ($R_t \simeq 200k\Omega$ measured versus $R_t > 1M\Omega$ expected) indicating diffusion of the STM-patterned dopants. Diffusion of the STM-patterned dopants was unexpected based on the diffusion calculations of Fig. 3.1 on pg. 42, which predicted that the growth conditions used would give a diffusion of $x_j < 0.5nm$.

Fitting the Coulomb blockade peaks with a combination of thermal and lifetime broadening fitting formulae indicated a lifetime broadening energy of $\sim \Gamma h = 0.16meV$ at base temperature, where the in-plane gate device of Chapter 4 showed no perceptible lifetime broadening when measured using the same experimental setup. This is a reflection of the greater transparency of the tunnel barriers in this device, which may be the result of either stray desorption altering the dimensions of the patterned device, or diffusion of the patterned dopants while growing the low temperature oxide. The tunnel barrier transparency seen in this device ($< 500k\Omega$) is consistent with a tunnel gap aspect ratio of ~ 0.6 rather the targeted 0.44 of the in-plane gated device. Furthermore, the capacitive coupling of the source and drain barriers appears to be more than double the modelled value, this implies that the δ-layer width is $\sim 4nm$ rather than the expected $2nm$. Both the capacitance change and tunnel barrier resistance change are therefore consistent with the dopants diffusing by $\sim 1nm$ during the growth of the low temperature oxide (~ 2 lattice sites).

We also witnessed many switches in the Coulomb blockade peaks of the surface gated

device, with approximately ten times more switches at base temperature in this device per Coulomb blockade peak than the in-plane gated device of the previous chapter (∼0.6 switches per peak, c.f. 0.06 for the in-plane gated device). We attribute these switches to unintentional dopants in the substrate from stray desorption during STM lithography, since the switching events did not reduce in magnitude or density at base temperature, indicating that the tunnelling to nearby dopants does not require thermal energy to occur. In contrast, switching was found to be thermally activated for the in-plane gated device, indicating that the coupled dopants in that device were further away and required thermionic emission over the potential barrier to populate and depopulate. The increased number of switches in the surface gated device is therefore not believed to be related to the low temperature oxide or the surface gate itself, but simply due to difference in the degree of stray desorption in the STM patterning.

We observed minimal drift in the surface gated device, either when sweeping over multiple peaks during the switching study or when sitting on a single peak during the charge noise study. In Chapter 4, we attributed drift to coupling of the dot potential to an ensemble of many distant traps, predominantly at the Si–SiO_2 native oxide interface. Since the interface traps density of the low temperature oxide is less than that of a native oxide ($N_{it} < 4 \times 10^{11} cm^2$ vs. $N_{it} > 10^{12} cm^2$), the reduction of drift in the surface gated sample is consistent with this model.

The charge noise of the surface gated device was comparable to that of the in-plane gated device: The standard deviation of the fluctuations in the dot potential was $\sigma_{Q_d} = 0.005e$, whereas the in-plane gated device showed $\sigma_{Q_d} = 0.002e$. This indicates that the total noise power is of the same order for the two devices over the measurement bandwidth used, and more importantly that the surface gating scheme does not significantly increase the charge noise in the device. This means that the surface gating scheme developed within this thesis is equally capable in sensitive applications — for example, to make SETs as electrometers for charge sensing in quantum computing architectures.

The power spectral density calculated for the two devices at base temperature (in the absence of Johnson noise) were similar, with the surface-gated device showing $S_{Q_d} = 1.1 \times 10^{-8} e^2.Hz^{-1}@1Hz$ and the in-plane gated device showing $S_{Q_d} = 3.1 \times 10^{-8} e^2.Hz^{-1}@1Hz$. The exponents describing the relationship between power spectral density and frequency were also similar, with the surface gated device showing $S_{Q_d} \propto f^{-1.7}$ and the in-plane gated device showing $S_{Q_d} \propto f^{-1.8}$. From this, we can conclude that the charge noise in both devices is dominated by a small number of fluctuators (which would give $S_{Q_d} \propto f^{-2}$), with some mixing with an ensemble of fluctuators (which gives $S_{Q_d} \propto f^{-1}$). As such, the noise in both devices appears to be dominated by a small number of nearby traps.

From this analysis we conclude that surface gates give a larger gating range as a consequence of the greater field that may be applied and the enhanced capacitive coupling of the gate to the device. Moreover, the charge noise in the device in the presence of surface gates is comparable to that of the in-plane gating scheme. The drift also appears to be lower, which indicates that drift in these STM-patterned SETs is linked to the density of interface traps. It may be possible that future optimisation of the oxide, particularly using post oxidation or post-metallisation anneals, may improve the hysteresis and charge noise, and as such this optimisation is an ongoing subject of investigation within our group.

Chapter 6

Conclusions and Future Work

This thesis presents a methodology to extend the atomically-precise fabrication scheme recently developed at UNSW to make atomically abrupt, *surface-gated* STM patterned Si:P devices. To this end, we have developed a low temperature, UHV-compatible method for depositing aluminium gate electrodes on a SiO_2 gate dielectric, aligned to buried STM-patterned dopants with minimal diffusion of the patterned donors. Silicon dioxide was selected as the preferred dielectric based on its high barrier ($3.2eV$), its previously published performance at low growth temperatures, and its compatibility with UHV technology.

In Chapter 3 we demonstrated a UHV silicon dioxide deposition system capable of forming silicon dioxide layers at growth temperatures down to $140°C$ at a growth rate as high as $0.3nm.min^{-1}$. Importantly using this system we were able to form silicon dioxide layers of the desired thickness for gating STM-patterned devices ($\sim 15nm$), within the calculated thermal budget ($\sim 210°C$ for $3hrs$) required to minimise diffusion of the patterned dopants to less than one lattice site ($\sim 0.5nm$). Structural and chemical analysis using both XPS and TEM of the low-temperature oxide showed that it was indistinguishable in composition and structure from a high-quality thermal oxide. However, we observed a higher than expected etch rate in hydrofluoric acid ($\sim$4 times that of thermal SiO_2), consistent with the formation of a low density oxide. Finally optical measurements of the surface revealed a high density of surface defects with a density of $\sim 1.25 \times 10^{-12}.cm^{-2}$. These defects are most likely due to spitting of silicon particles from the Si SUSI cell and were present on all samples.

Electrical characterisation of the oxide was hindered by the large leakage in these devices arising from the high density of surface defects. However using Hall bar MOSFETs we measured an upper limit on the interface trap density of $N_{it} = 4.3 \times 10^{11} cm^{-2}$ for the as-grown UHV oxide (without any post-oxidation or post-metallisation anneals). While we did observe hysteresis in the gate action, we showed that it could be eliminated using a $350°C$ post-metallisation anneal in forming gas ($95\%N_2$:$5\%H_2$). Once annealed in forming gas, devices were able to withstand electric fields of 2–$3MV.cm^{-1}$, exceeding the requirement of $1MV.cm^{-1}$ for STM-patterned devices.

In parallel with the characterisation of the oxide, we began using the silicon dioxide

layer as a dielectric on much smaller STM-patterned devices, where the overlap with surface defects would be less frequent. To incorporate the low-temperature oxide into STM-patterned devices, we had to modify the STM fabrication scheme. As part of this modification, we found the optimum thickness of the low temperature oxide that could be deposited without significant diffusion ($x_j < 0.5nm$) of the STM-patterned dopants ($t_{ox} = 50nm$), the required length of the STM-patterned contact patches to allow for any under etching of the oxide ($5\mu m$), and developed a process to reliably achieve contact to the STM-patterned device once it had been buried under the low-temperature oxide. This process was used to make surface gated STM-patterned tunnel gaps in collaboration with Pok [168], and a large scale surface gated SET in collaboration with Lee [215]. We then designed an STM-patterned ∼200 donor SET — the optimal size for single shot spin read-out. Such devices are currently under investigation within our group as a means of probing the charge states of individual donors. In this thesis, we utilised these STM-patterned ∼200 donor SETs as sensitive electrometers for comparing the charge noise of all-epitaxial in-plane gates with low-temperature SiO_2 surface gates.

In Chapter 4 we describe the design and analysis of a ∼200 donor in-plane gated, STM-patterned SET, fabricated using our custom-designed STM-SEM system. The device had a line edge roughness of a single dimer row with tunnel gaps of dimensions $5.4nm \times 12.5nm \pm 0.77nm$. Using the FastCap capacitance modelling program and the single electron transport modelling program SIMON, we found excellent agreement between modelled capacitance and experimental transport data. We observed a charging energy of $E_c = 13.6meV$ predicted theoretically and $E_c \simeq 13.5meV$ measured experimentally. At milli-Kelvin temperatures we observe excited states in the transport spectroscopy separated in energy by $100\mu eV$–$750\mu eV$, consistent with the excited state features of STM-patterned SETs published by both Fuhrer [22] and Füchsle [23], which contain 4000 and 7 donors, respectively. We observed clear evidence of spin splitting via the Zeeman effect in a magnetic field, but noted that not all peaks split, indicating both the presence of valley splitting within the dot and states due to transport through the 1-D source and drain leads (which were $\sim 6nm$ wide). This is consistent with previous reports where abrupt lateral confinement of the device caused valley splitting of the Δ bands, giving rise to energy separations down to $100\mu eV$. In addition to the patterned device showing Coulomb diamonds in the differential conductance, we also observed additional diamonds offset in the gate space. We were able to replicate these features with a numerical model of a tunnel-coupled trap near the SET. In particular we were able to match the offset of the Coulomb diamond edges and apparent opening of these diamonds observed at low V_{sd} with that expected for a tunnel coupled trap.

We then fabricated a surface gated STM-patterned SET incorporating the low temperature UHV SiO_2 dielectric with comparable dimensions to the in-plane gated device in Chapter 4. The device was observed to have a much higher conductance, which enhanced the lifetime broadening of the electron energy levels and made it difficult to extract the charging energy of the device and masked all excited states of the device in the stability map. It is likely that the increase in the device conductance is caused either by stray desorption during the STM lithography or by diffusion of the dopants when growing the low-temperature silicon dioxide gate dielectric. Preliminary calculations of the expected diffusion during this growth estimated that the donors would move by $< 0.5nm$. However for the transport data the capacitive coupling of the source-drain leads to the dot was more than double that of numerical modelling, whilst the tunnel gap resistance was less than half that expected from the tunnel gap aspect ratio relationship measured in previous devices. Both of these point to enhanced diffusion of dopants during the growth, closing the tunnel gap aspect ratio to $\sim$0.6 rather than the intended 0.44, with the vertical diffusion of the dopants causing the δ-layer width to approximately double (to $\sim 4nm$). Both effects are consistent with the dopants diffusing $\sim 1nm$ during the growth of the oxide ($\sim$2 lattice sites).

We characterised the stability and noise of the in-plane gated and surface gated device. As part of this process, we measured the drift of the Coulomb blockade peak position, which we found to be thermally activated for the in-plane gated device, with the population of nearby traps having an activation energy of $47\mu eV$. Given the probable causes of traps within this device, we expect the drift to be related to traps located at the Si–SiO_2 interface. Interestingly we did not observe such large drift in the surface gated device. This might be a consequence of the expected reduction in the number of interface traps when using the low-temperature oxide versus the native oxide used for the in-plane gated device ($< 4 \times 10^{11}.cm^2$ vs $> 10^{12}.cm^2$). It is however also possible that drift in this device was simply masked by a greater number of switching events caused by unintentional dopants incorporation from stray desorption during the lithography of this device. We studied these switching events in the Coulomb blockade peak position, which we attribute to the presence of capacitively coupled traps within the substrate, near to the dot itself. For the in-plane gated device, the number and severity of these switching events dropped considerably when the sample was cooled from $4K$ to base temperature, resulting in only one visible switch at milli-Kelvin temperatures, indicating that these traps were thermally activated, and therefore relatively far from the device. The surface gated device showed $\sim$10 times more switching events per Coulomb blockade peak (0.6 vs 0.06 for the in-plane gated device). We did not see a noticeable change in the number of switching events in

the surface gated device as we cooled the device to milli-Kelvin temperatures. This would indicate that the switching in this device was dominated by tunnel coupling to unintended donors from stray desorption, which are near to the dot. We do not believe that the greater number of switching events in the surface gated device can be attributed to the low-temperature oxide nor the surface gate itself.

When we studied conductance noise of the two different SETs, we found the nature of the noise to be consistent with fluctuations in the dot potential, most likely arising from interface traps, unintentional dopants from stray desorption, or background dopants within the substrate. By measuring fluctuations in the device current and correlating this to the dot potential over a range of gate voltages, we found no variation in the noise characteristics, indicating the number of active fluctuators did not change as we altered the gate voltage. The frequency-independent Johnson noise however reduced at base temperature, revealing a frequency dependence in the power spectral density of the charge noise at base temperature proportional to $1/f^{1.8}$ for the in-plane gated device, and $1/f^{1.7}$ for the surface gated device. This frequency dependence indicates the presence of both discrete trapping events causing RTSs in the signal, and of $1/f$ noise caused by many weakly coupled fluctuators. We found that the standard deviation in the charge noise was of the same order for the two devices, with $\sigma_{Q_d} = 0.002e$ for the in-plane gated device and $\sigma_{Q_d} = 0.005e$ for the surface gated device, both of which compare favourable to silicon MOS based SETs studied by Zimmerman *et al.* with a high quality gate oxide [209]. This is a very positive result, since the low charge noise in our STM patterned device will be an advantage for the more complex spin-qubit devices planned in the future. Furthermore, the similarity in the charge noise results of the surface-gated and in-plane gated devices indicates that the surface gating scheme will also be applicable to these spin-qubit devices.

6.1 Future work

Based on the results of this thesis, there are several interesting experiments that we should pursue in future, some of which are already underway within our group. Specifically, optimisation of the low temperature oxide to reduce the interface trap density and create stoichiometric SiO_2 using a post-metallisation anneal, and reducing the density of macroscopic surface defects. Further noise studies are underway of STM-patterned devices, and on the use of this low temperature UHV SiO_2 for STM-patterned FETs.

6.1.1 Optimisation of the low temperature oxide

We have shown that the low temperature oxide developed as part of this thesis is a suitable gate dielectric for atomic scale devices, but further optimisation is possible. The dominant problem remaining with the oxide is that of leakage. Specifically, we have found macroscopic defects within the oxide that we believe cause shorts through the oxide between the gate electrode and the silicon substrate. The most likely sources of these defects include:

Spitting of particles from the silicon sublimation source: The SUSI 63 silicon sublimation source from MBE Komponenten used to grow the low temperature oxide consists of a hot silicon filament that sublimates silicon onto the sample. Such sources are known to exhibit 'spitting' of particles, where non-uniformities in the shape or temperature distribution of the filament causes large particles to be emitted from the filament. These particles have been observed on silicon samples grown in the preparation chamber of the STM-SEM — with an identical silicon source — where there is no oxygen plasma source to complicate the silicon sublimation process. Generally, these spitting events are rare, since the silicon source is placed below the sample (pointing upwards) within the chamber such that large heavy particles projected from the silicon filament should fall away before reaching the sample. In the future, different silicon sources may be tried in which spitting is known to be less problematic.

Defects nucleating within the oxide itself: It is also possible that the observed macroscopic defects within the oxide are caused by the growth itself, where the silicon dioxide is not fully stoichiometric. If this is true then we would expect the growth conditions used to deposit the oxide to change the density or size of these defects, which we have not observed in any of the samples made for this thesis. As such, in future we will pursue a superlattice approach, in which a mechanical shutter is used to periodically interrupt the silicon flux and allow the atomic oxygen to diffuse further into the formed oxide between the deposition of silicon layers, such as that demonstrated by Majamaa *et al.* [93].

In addition to reducing the number of macroscopic defects, it may be possible to improve the oxide quality by promoting diffusion of the atomic oxygen into the formed oxide layer during the growth. We have shown using XPS and ellipsometry that higher growth temperature improves the quality of the oxide, and the best samples during the electrical measurements were grown using higher RF powers in the oxygen plasma source (which gives a larger flux of atomic oxygen). While it is clear that at the growth temperatures used

for the surface gated SET shown in this thesis ($\sim 160^{\circ}C$) we do retain the STM-patterned source, drain, and SET island, we did also see signs off diffusion of the dopants — with the tunnel barrier resistance and in-plane gate range were much lower than expected and the source-drain capacitances was much higher. At this temperature we did not expect to see any signs of diffusion ($x_j < 0.5nm$).

6.1.2 Further noise studies

In this thesis we showed the first noise studies performed on STM-patterned $Si{:}P$ devices. As part of this study we were able to quantify the charge noise and stability of STM-patterned SETs, where it was clear that the conductance noise within the SET arose from coupling of the SET island to nearby traps. Having learned how to perform these noise studies at the Indian Institute of Science, we can now go on to routinely measure noise in future STM-patterned devices. In particular, it would be interesting to see whether we can disentangle the effects of stray P incorporation and interface traps. As part of this study, the group aims to study the noise of devices with a much thicker encapsulation layer (e.g. $> 50nm$), to see whether we can minimise charge noise arising from traps at the silicon/silicon-dioxide interface. Finally, on future devices it will be interesting to anneal the oxide (e.g. $15min$ at $300^{\circ}C$ in forming gas), to see whether we can eliminate the gate hysteresis, and to see whether this reduces the charge noise or improves the stability of the device.

6.1.3 Using the low temperature oxide to make other novel devices

The greatest advantage of the surface gating scheme is the improvements it promises in both gate selectivity and gate density. These advantages will become more apparent as our group progresses towards quantum electron devices in which we must gate single dopant atoms to perform changes to the qubit state. A study has recently been completed within our group on the use of STM-lithography to pattern a single isolated P dopant and study the energy spectrum of this donor [31]. Scaling devices up to use multiple isolated donors is underway, towards the ultimate goal of forming spin qubit devices, where gate selectivity becomes critical. Combined with improvements to the alignment accuracy of surface gates — from the $\sim 100nm$ tolerance now achievable to the $\sim 5nm$ required — the optimisation of the low-temperature oxide developed as part of this thesis could provide the key to achieving the required selectivity to address these isolated donors individually.

In addition to these quantum electronic devices, the low temperature oxide developed as part of this thesis will allow us to explore additional surface-gated devices, such as atomic-scale MOSFETs, or MOSFETs in which the dopants are ordered within the channel or source-drain leads with atomic precision. This study is already underway within our group. This could provide insights into the operation of MOSFET devices that are not yet possible with industrial semiconductor processes, which may provide clues about how or when we will reach the ultimate limit of Moore's Law in CMOS scaling.

Appendix A

Clean Room Processes

A.1 Standard Processes

The clean room processes used in this thesis share many common sub-processes, which we present here in detail.

A.1.1 Wafer clean

The wafers were chemically cleaned using the following standard procedure:

1. 10 minutes in a mixture of sulphuric acid (96% w/w) and hydrogen peroxide (30% w/w), mixed in a ratio of 3:1, respectively. Hereafter denoted an 'SP clean'.
2. 10 minutes under flowing deionised water (all deionised water used has resistivity $> 18\text{M}\Omega.\text{cm}$). Hereafter referred to as a 'DI rinse'.
3. 10 minutes in a mixture of deionised water, hydrochloric acid (37% w/w), and hydrogen peroxide (30% w/w) in a ratio of 6:1:1, respectively. During this clean, the solution is held at $80°C$ on a hotplate. Hereafter, this will be called an 'RCA-2 clean', as it follows the specifications of the Radio Corporation of America's 'Standard Clean 2'.
4. 10 minute DI rinse

This standard clean leaves the sample with a thin oxide. When cleaning a sample before a furnace oxidation, this oxide was removed with a $10sec$ immersion in a solution of hydrofluoric acid (49% w/w) and deionised water in a ratio of 10:1, respectively, hereafter called 'HF 10:1'. When used to clean samples before loading them into UHV, the HF 10:1 etch was conducted mid-way through the DI rinse of step 2.

A.1.2 Electron beam lithography

All clean-room patterning of samples in this thesis used electron beam lithography (EBL) according to the following process:

1. The wafer was baked at 180°C for 10 minutes to remove any adsorbed water on the surface, and then allowed to cool for 2 minutes. A layer of 'A4' poly-methylmethacrylate (PMMA) was then spun on the wafer with the sample rotating at 5000 rpm for 60 seconds, which yields $\sim 170nm$ of resist.

2. The solvents were then baked from the resist at 180°C for 90 seconds.

3. A custom pattern was then written in the resist using an XL30 scanning electron microscope from FEI, with an electron dose of 170–3500$\mu C.cm^{-2}$, where the dose is adjusted to give the desired pattern definition.

4. The resist was then developed for $40sec$ in a 1:3 solution of MIBK and isopropanol, followed by a 20 second rinse in isopropanol.

5. After the required pattern was produced in the resist, it was placed in an oxygen-plasma with 50W forward power at $340mTorr$ for 2 minutes. This removes around twenty nanometers of resist, thus removing any residual resist within the developed-region.

Note that some process steps required a thicker layer of PMMA, for which we repeated the stated spin recipe to achieve the desired thickness using multiple layers.

A.1.3 Sample metallisation

All metal electrodes patterned on the sample (e.g. gates and Ohmic contacts) were deposited using a metal lift-off process, in which metal is deposited onto patterned PMMA and then the PMMA is dissolved, taking the undesired metal with it. The details of this process are as follows:

1. Lithography was first conducted according to the process in A.1.2, using a single layer of resist and including the $2min$ plasma ash to remove any residual resist.

2. The sample was then mounted on a glass slide using 'A5' PMMA on the back of the sample to temporarily glue it to the slide, which was then baked at 95°C for $5min$ so that the would PMMA set.

3. If depositing Ohmic contacts, the sample was then dipped in BHF 15:1 for $10sec$ to remove any native oxide on the exposed silicon. When depositing gates on an oxide, this step was skipped.

4. The sample was then mounted in a Kurt J. Lesker thermal evaporator, in which the desired source metal had been loaded into a clean tungsten crucible.

5. The evaporator chamber was then pumped down to $\sim 2 \times 10^{-6} Torr$ using a roughing pump and turbo pump.

6. The crucible temperature was then raised by passing a current through it, with the sample protected using a metal shutter, until the crucible had out-gassed and was evaporating the desired flux of the source metal, measured using a crystal monitor.

7. The sample shutter was then opened, depositing the desired thickness of metal, as measured by the crystal monitor.

8. The sample shutter was then closed and the crucible temperature was ramped down, with chamber pressure allowed to settle back down.

9. The chamber was then vented, and the sample and crucible removed

10. The sample was then placed in a heated mixture of n-methyl-2-pyrrolidone (NMP) at $80°C$, and left in this heated mixture for 1–$24hrs$ to dissolve the PMMA. After the PMMA had dissolved, the sample was bathed in acetone for $\sim 2min$ and rinsed with isopropanol for $1min$.

Note that if there were any problems removing the undesired metal, the sample was repeatedly rinsed in acetone or isopropanol, and sometimes returned to the NMP solution. In severe cases, a short burst of ultrasonic agitation (1–$2sec$) was used.

Appendix B

Tunnel coupling between a trap and a quantum dot

Simplistically, a trap in isolation near an SET causes a sudden switch in the dot potential every time the trap populates or depopulates. The physical link between the trap occupancy and the dot potential is the capacitive coupling between them (C_{dt}); the addition of an electron on the trap causes a change in the dot potential of

$$\Delta\mu_{d:Trap} = \frac{e^2}{C_t}\frac{C_{dt}}{C_\Sigma} \tag{B.1}$$

where C_t is the self-capacitance of the trap. Bringing an electron into the trap *increases* the dot level, since electrons on the dot are repelled by the trapped electron. Equally, a change in the occupancy of the dot increases the trap potential by

$$\begin{aligned}\Delta\mu_{t:Dot} &= \frac{e^2}{C_\Sigma}\frac{C_{dt}}{C_t} \\ &= \Delta\mu_{d:Trap}\end{aligned} \tag{B.2}$$

which is to say, the back-action affects the dot and trap equally. Filling the trap increases the dot level from $\mu_d(N,0)$ to $\mu_d(N,1)$, where the separation between these two states is given by $\Delta\mu_{d:Trap}$ given in Eq. B.1. Now let us consider the case when the trap is brought closer to the dot, so that electrons may tunnel freely into the trap. In this tunnel-coupled state, the trap may constantly empty and fill, continually switching the dot potential back and forth by $\Delta\mu_{d:Trap}$. This continual switching in the dot potential has the effect of blurring or doubling all features in the transport spectroscopy, including the diamond edges. This additional trap-induced state on the dot therefore appears as an excited state line in the transport spectroscopy, though it is only an excited state of the coupled dot-trap system, not the dot itself.

In a more complex scenario, the trap may be coupled to both the dot and the drain. In this situation, a curious thing happens as the dot potential is swept through the trap level, which is best described by breaking the process into a sequence of steps. Let us first assume that the capacitance between the trap and gate is much less than the trap self

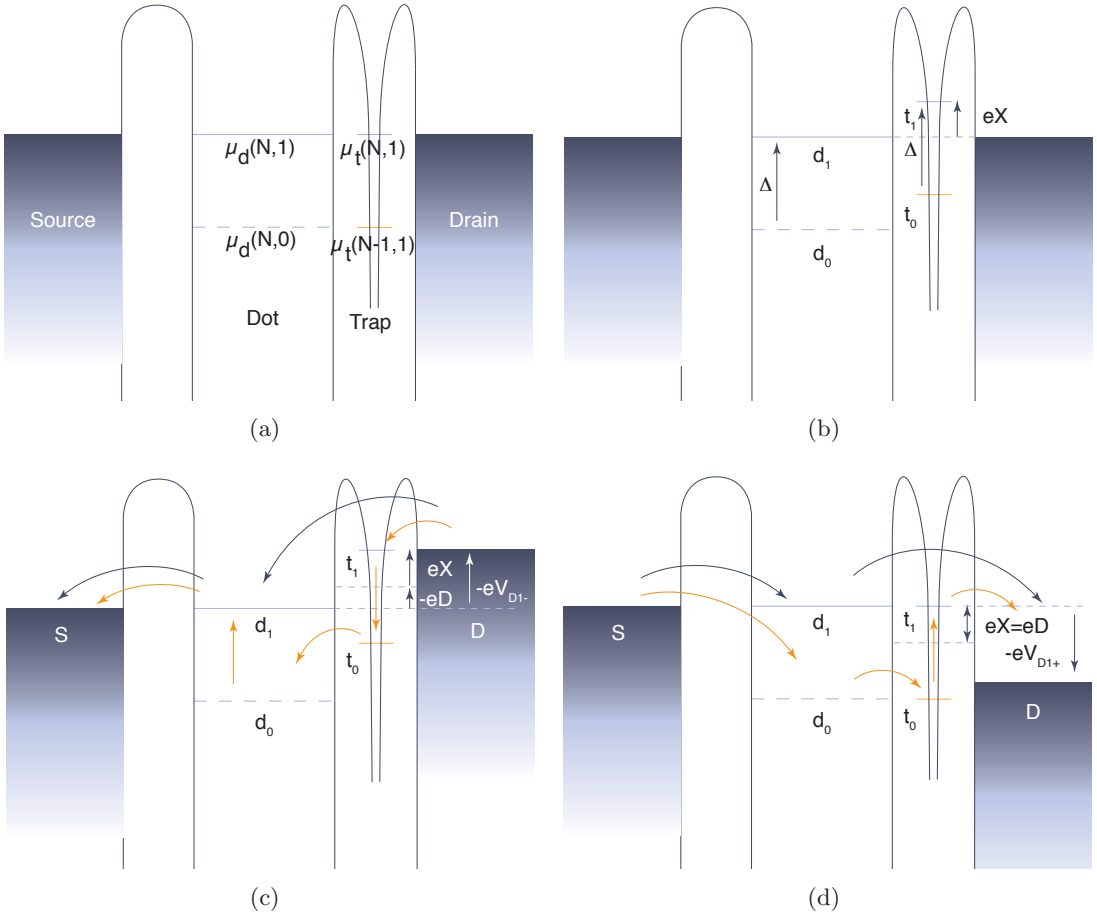


Figure B.1: Transport through a coupled dot-trap system. (a) We can represent the system as a dot with an additional dot situatued in the drain barrier, though tunnelling can still occur directly from the drain to the dot. (b) Simplified nomenclature of the energy levels for the following discussion. (c) Tracing the different paths traversed for an electron passing through state d_1 on the dot (blue arrows), and through the trap (orange arrows) with a negative drain bias. (d) Tracing conduction through the same states as in (c), but with a positive drain bias.

capacitance, so that sweeping the gate affects the dot more than the trap. Note that even if we were to disregard C_{gt}, the trap potential would be determined by the voltage divider formed by C_{dt} and C_{Dt}; as a consequence, the trap potential will still change with any variation in the drain or dot level — even those induced by the gate. Let us work through the simplified level diagram shown in Fig. B.1(a), where we focus only on transport through the $\langle N, 0\rangle$ and $\langle N, 1\rangle$ states of the dot-trap system (N is the number of electrons on the dot and 0/1 is the number of electrons in the trap). Note here that we expect tunnelling between the source, dot, and drain; and between the dot, trap, and drain. To depict this properly we would therefore need to invoke a third dimension in the level diagram; for

simplicity we present the dot and trap levels side-by-side. Since we will present several of these diagrams, we show a version that is simpler still in Fig. B.1(b), here we substitute $\mu_d(N,0) = d_0$, $\mu_d(N,1) = d_1$, $\mu_t(N-1,1) = t_0$, and $\mu_t(N,1) = t_1$. In this figure, we have also added an offset potential eX of the trap level t_1 from the zero-bias potential, since in general the trap and dot levels do not align with the source and drain. In the following discussion we assume that the coupling between the gate and trap is minimal, so that we can use the gate to compensate the dot potential, keeping it aligned with the source. Let us begin our analysis with the d_1 level of the dot. In the following discussion, all transport through the d_1 state is shown in solid blue arrows, whereas that through the d_0 state is shown in broken blue arrows, and that through the trap is shown in orange. Since the number of electrons on the dot N, is arbitrary for this discussion, let us set $N - 1 = 0$. We therefore have four possible states of the coupled dot-trap system: $\langle 0,0\rangle$, $\langle 0,1\rangle$, $\langle 1,0\rangle$, and $\langle 1,1\rangle$. From Fig. B.1(b), we see that we begin with the d_1 state at the source and drain potential, and the corresponding trap state t_1 above it. From this we can conclude that the system will initially have one electron on the dot and zero electrons on the trap: $\langle 1,0\rangle$. The dot state occupied is therefore the d_0 state, which is below the source and drain potential; thus, the dot is in Coulomb blockade and we see no conduction. With an electron on the dot, there is no way for the trap to populate unless we increase the drain potential (by decreasing the drain voltage). This is shown in Fig. B.1(c); once the drain potential reaches t_1, we can fill the trap, giving conduction through the d_1 state. Note that, since the trap is capacitively coupled to the drain, increasing the drain potential will increase the trap potential by a small amount, $-eD$, given by

$$-eD = -eV_{D1-}\frac{C_{Dt}}{C_t} \tag{B.3}$$

In order for the drain potential to reach t_1, we must therefore apply a drain bias of

$$\begin{aligned} D &= t_1 \\ -eV_{D1-} &= eX - eV_{D1-}\frac{C_{Dt}}{C_t} \\ \Rightarrow eV_{D1-}\left(1 - \frac{C_{Dt}}{C_t}\right) &= -eX \\ \Rightarrow V_{D1-} &= \frac{-X}{1-\frac{C_{Dt}}{C_t}} \\ &\simeq -X\frac{C_t}{C_{dt}} \end{aligned} \tag{B.4}$$

where, in the last step we make the approximation $C_t \simeq C_{Dt} + C_{dt}$. This means that we

should not expect conduction through the d_1 state without first applying a drain bias of $V_D = -X\frac{C_t}{C_{dt}}$. Which is to say, if $X > 0$, there is no conduction through this state at zero source-drain bias. Note that the trap will also periodically empty when the d_1 level empties to the source (i.e. when we are in the $\langle 0,1\rangle$ state). Transferring an electron from the trap to the dot then gives $\langle 1,0\rangle$. This state (d_0) is in blockade, and so we do not see conduction through the device until the trap fills again, giving $\langle 1,1\rangle$, which was our starting state. Conduction through the d_1 dot level therefore occurs via two pathways:

$$\begin{array}{lllll} \text{(A)} & \langle 1,1\rangle\rightarrow & \langle 0,1\rangle \rightarrow & \langle 1,1\rangle\rightarrow & ... \\ \text{(B)} & \langle 1,1\rangle\rightarrow & \langle 0,1\rangle \rightarrow & \langle 1,0\rangle \rightarrow & \langle 1,1\rangle \rightarrow \quad ... \end{array}$$

What this means is that, in pathway (B) the trap continually fills and empties, which is to say that the trap is in an astable state. Now let us analyse the system with a positive drain bias; we cannot pass current until we can fill the trap state, this time from the dot (Fig. B.1(d)). Since an electron can only ever be transferred between the dot and trap via the d_0 and t_0 states ($\langle 1,0\rangle \rightarrow \langle 0,1\rangle$), we must apply a large drain bias to pull t_0 down to d_0. As shown, this occurs precisely when $eX = eD$. This requires that we apply a drain bias of

$$\begin{aligned} 0 &= eX - eV_{D1+}\frac{C_{Dt}}{C_t} \\ \Rightarrow V_{D1+} &= X\frac{C_t}{C_{Dt}} \end{aligned} \tag{B.5}$$

Having established the conditions for transport through d_1, now let us analyse the d_0 level (Fig. B.2(a)). We must apply a finite negative drain bias to depopulate the trap before we can access this state; this time the trap must empty to the dot, which requires that $d_0 = t_0$. This occurs at a drain bias of

$$\begin{aligned} 0 = d_0 &= t_0 \\ 0 &= eX - eV_{D0-}\frac{C_{Dt}}{C_t} - \Delta \\ \Rightarrow V_{D0-} &= (X - \Delta/e)\frac{C_t}{C_{Dt}} \end{aligned} \tag{B.6}$$

Lastly, to see conduction through the d_0 state under a positive drain bias (Fig. B.2(b)), we must empty the trap into the drain before the d_0 state is accessible. For this we must

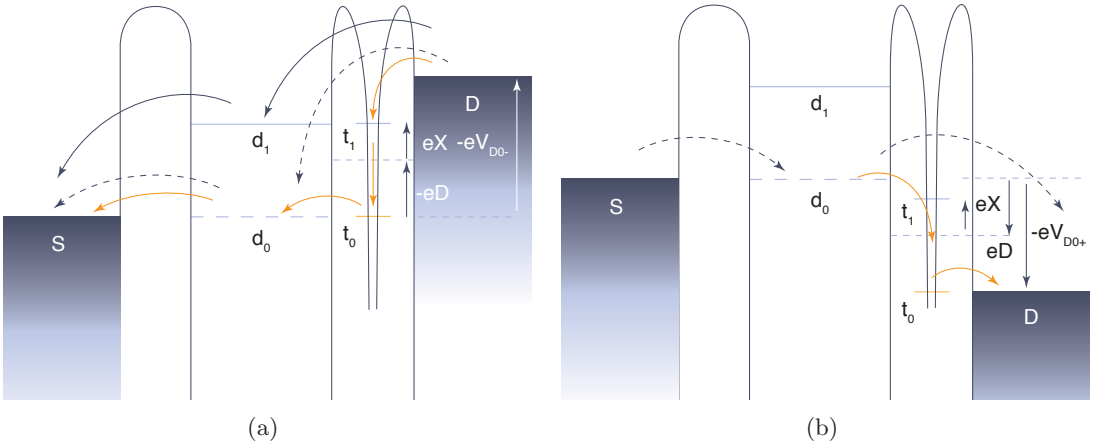


Figure B.2: Transport through lower-energy states of a coupled dot-trap system (a) Tracing the different paths traversed for an electron passing through state d_0 on the dot (dashed blue arrows), and through the trap (orange arrows) with a negative drain bias. (b) Tracing conduction through the same states as in (a), but with a positive drain bias.

apply a drain bias of

$$\begin{aligned} -eV_{D0+} &= eX - \Delta - eV_{D0+}\frac{C_{Dt}}{C_t} \\ \Rightarrow V_{D0+} &= \frac{(\Delta/e - X)}{1 - \frac{C_{Dt}}{C_t}} \\ &\simeq (\Delta/e - X)\frac{C_t}{C_{dt}} \end{aligned} \tag{B.7}$$

The resultant stability diagram of this system is shown in Fig. B.3. From this we see that the d_0 and d_1 transitions are translated in the V_g axis by $\Delta V_g = \Delta/e(C_\Sigma/C_g)$, and there is no conduction through either state at $V_{sd} = 0$.

Now, in addition to the arbitrary offset of the trap from the zero-bias level, the term X can be used to include any coupling between the gate and trap of the form:

$$X = V_g\frac{C_{gt}}{C_t} + X_c \tag{B.8}$$

Where X_c is the constant component of the offset potential. From this we can see that the opening of the CB diamonds (given by V_{D0-}, V_{D0+}, V_{D1-}, and V_{D1+}) changes with gate voltage. For example, at a gate voltage of $V_g = -X_c\frac{C_t}{C_{gt}}$, we have $X = 0$, so that $V_{D1+} = V_{D1-} = 0$; which is to say that the d_1 diamonds close at this voltage. Similarly, at $V_g = (\Delta - X_c)\frac{C_t}{C_{gt}}$, $X = \Delta$ and $V_{D0-} = V_{D0+} = 0$; such that the d_0 diamonds close at this gate voltage. From this analysis, we can therefore determine the relative capacitance

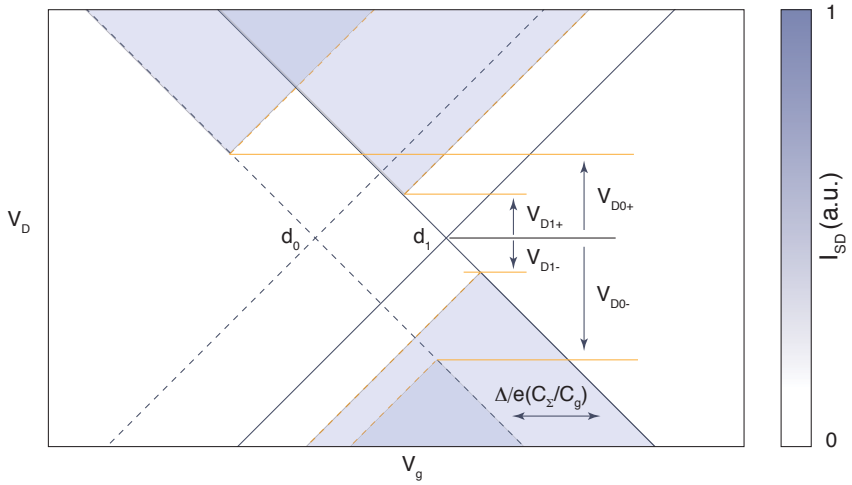


Figure B.3: Plotting the expected change to the stability diagram in the presence of a tunnel-coupled trap. In the presence of a tunnel-coupled trap, we should see every dot level doubled in the stability diagram, separated in the gate voltage axis by $\Delta/e(C_\Sigma/C_g)$. The dot-trap interaction prevents conduction through either state at zero source-drain bias.

of the trap to the gate, dot, and drain.

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