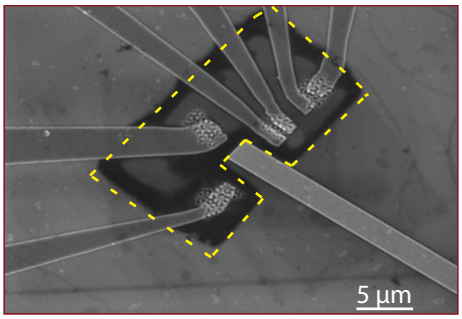
Surface Gated Atomically Precise Devices in Silicon



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In this thesis, the introduction of top gates over buried phosphorus donor devices in silicon patterned with the atomic precision of a STM is investigated. To achieve this a low temperature 200 ^{0}C ALD grown Al_2O_3 dielectric is introduced and a process strategy is developed to both contact the buried nanostructure and align surface gates to the devices.

The thesis describes the impact of the Al_2O_3 dielectric on the electrical properties of the buried nanostructure and successful efforts to maintain the integrity of the dielectric whilst contacting the buried donor layers in silicon. Dose rates are optimized for the EBL resist to contact the buried donor device. Moreover, with the optimization of the etch rate of the deposited Al_2O_3 to minimize the dielectric undercut, the top gate was successfully implemented on 3 types of donor based devices.

In the first device a 2D δ-layer, the implementation of top gate shows a effective gate range of -4 V to 4 allowing ~ 3% change in the carrier density of the highly doped ~10^{14} cm^{-2} δ-layer in silicon.

In the second device an Al_2O_3 dielectric and a top gate was integrated onto a precision STM-patterned SET. An increase in the overall tunability of the SET quantum dot was observed using the top gate owing to its large lever arm (~4 times that of the in-plane gate) with no significant reduction in the charging energy of the quantum dot. An enhanced gating range of -4 V to 4 V was observed for the SET quantum dot device. Additionally, the patterned top gated device demonstrated exceptional stability with the lowest noise and drift of all devices and a successful dynamic frequency response up to 1 MHz.

In the third device the top gate and an Al_2O_3 dielectric was incorporated into a precision STM-patterned 4 quantum dot device with the aim to capacitively couple two singlet-triplet qubits. Without the top gate the limited in-plane gate range did not allow any singlet-triplet inter-dot transitions in the gate space. However, after successful patterning of a top gate, two new inter-dot transitions were accessible in the gate range, with one of them being a singlet-triplet type inter-dot transition. An enhanced gate range of -4 V to 4 V was again observed for the top gate patterned on top of the 4 quantum dot.

In conclusion a successful integration of an Al_2O_3 dielectric on precision STM-patterned donor devices in silicon was demonstrated important for the continuing success of silicon based atomic electronics.

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Abstract

In this thesis, the introduction of top gates over buried phosphorus donor devices in silicon patterned with the atomic precision of a Scanning Tunneling Microscope (STM) is investigated. To achieve this a low temperature 200 ℃ ALD grown Al_2O_3 dielectric is introduced and a process strategy is developed to both contact the buried nanostructure and align surface gates to the devices.

The thesis describes the impact of the Al_2O_3 dielectric on the electrical properties of the buried nanostructure and successful efforts to maintain the integrity of the dielectric whilst contacting the buried donor layers in silicon. Dose rates are optimized for the EBL resist to contact the buried donor device. Moreover, with the optimization of the etch rate of the deposited Al_2O_3 to minimize the dielectric undercut, the top gate was successfully implemented on 3 types of donor based devices.

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In conclusion a successful integration of an Al_2O_3 dielectric on precision STM-patterned donor devices in silicon was demonstrated important for the continuing success of silicon based atomic electronics.

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Contents

1 Introduction **1**

2 Background: Importance of top gating precision donor devices **5**

2.1 Silicon 5

2.1.1 Si(100) 2×1 surface 7

2.2 Scanning Tunneling Microscopy based donor fabrication in silicon . . 8

2.2.1 Surface preparation for UHV devices 10

2.3 Delta-doped (δ-doped) layers in silicon fabricated in UHV 12

2.3.1 Electron transport in δ-doped layers in silicon 14

2.4 Planar-doped nanostructures in silicon patterned by STM 20

2.4.1 Ex-situ processing of planar STM patterned nanostructures . . 22

2.4.2 Electron transport in a donor quantum dot 24

2.4.3 The constant-interaction model 26

2.5 Quantum computing with quantum dots in silicon 30

2.5.1 Donor based quantum dots 32

2.5.2 Gate defined quantum dots in semiconductor systems 35

2.6 Incorporating an Al_2O_3 dielectric onto STM fabricated devices 41

2.7 Atomic Layer Deposition: Principles and Applications 42
2.7.1 Introduction to Atomic Layer Deposition 43
2.8 Growing Aluminum oxide (Al_2O_3) as a dielectric using ALD 45
2.8.1 Reaction pathways of Al_2O_3 growth using TMA & H_2O 46
2.8.2 Additional aspects of growing Al_2O_3 using TMA and H_2O . . 50
2.8.2.1 Surface treatment before ALD and number of cycles 50
2.8.2.2 Al_2O_3 growth temperature 53
2.8.2.3 Impact of purge time 54
2.8.2.4 Impact of TMA & H_2O dose rates 55
2.9 Characterization of Aluminum Oxide grown using ALD 55
2.9.1 Ellipsometry to measure thickness of ALD deposited Al_2O_3 layers 56

3 Integration of a top gate on a Al_2O_3 dielectric 58

3.1 Reproducible ALD deposited Al_2O_3 layers 58
3.2 Integrating ALD deposited Al_2O_3 into STM fabricated devices 61
3.3 Patterning Al_2O_3 to access buried nanostructures 64
3.4 Etching ALD grown Al_2O_3 layers 69
3.4.1 BHF for etching ALD grown Al_2O_3 71
3.4.2 BHF 1:10 solution as an etching agent for Al_2O_3 layers 74
3.4.3 BHF 1:15 solution as an etching agent for Al_2O_3 layers 78
3.5 Effect of O_2 plasma treatment on the etch success 80
3.6 Effect of temperature on the etch process 82
3.7 Summary of all etch tests 83

4 Electrical Characterization of Al_2O_3 top gated atomic precision devices 85

4.1 Integrating a top gate on a 2D Si:P δ-layer fabricated in UHV 86

4.1.1 Depositing Al_2O_3 using ALD on a Hall bar 88

4.2 Integrating a top gate on a planar STM-patterned SET 91

4.2.1 Capacitance modeling for the ALD SET device before and after top gate 96

4.2.2 Characterization of the ALD-SET device 97

4.2.2.1 Electrical characterization of the SET without a top gate 99

4.2.2.2 Electrical Characterization of the SET with a top gate patterned on an Al_2O_3 dielectric 103

4.2.3 Comparison of capacitance modelling with results 109

4.2.4 Dynamic frequency response of the top gate 110

4.2.5 Effective gate range of the in-plane and surface gates 114

4.3 Integrating a top gate on a 4 quantum dot device 116

4.3.1 Device characterization before the top gate 119

4.3.2 Device characterization after patterning the top gate 123

5 Conclusions and Future Work 129

References 132

Chapter 1

Introduction

Since the inception of quantum physics, physicists have unraveled some of the most extraordinary phenomenons in nature, such as wave-particle duality [1], entanglement of fundamental particles [2], and quantized nature of radiation [3]. Since the invention of transistor in 1947 [4], a quest has been undertaken to make computers better, faster and more powerful [5]. Moore′s Law is a self-fulfilling prophecy made by a pioneer in the field of microprocessors Gordon Moore in 1968 stating that number of transistors will double every 18 months leading to increase in computation power. This equates to bundling more transistors onto the chip which comes at a cost of scaling them down and making them smaller. Transistor operation consists of current flow through a channel between source and drain modulated using gate voltage. In the near future, transistor operation will be governed by a few electrons flowing in the channel taking the underlying physics in to the realm of quantum physics. Leakage current is a quantum phenomenon where electron or hole wavefunction decays exponentially within the dielectric emerging with some finite

amplitude on the other side of the dielectric. Scaling down transistor size causes an increase in the leakage current where charge carriers (either electron or hole) tunnel through an insulating region. Leakage is one of the important phenomenon limiting the computational power as the gate dielectric (SiO_2) becomes thinner [6]. In order to tackle the problem of high leakage currents, alternate gate dielectric layers have been investigated that have better performance in terms of having a high dielectric constant, with larger breakdown field strengths and larger leakage currents [6]. Alternate gate dielectric that have a high dielectric constant such as aluminum oxide, silicon nitride and hafnium oxide are currently used for semiconductor device fabrication to replace silicon dioxide as preferred gate dielectric [7, 8, 9].

Despite the increasing computational power there exists several classical problems that are computationally complex [10]. In 1982, Richard Feynman famously introduced the concept of simulating physics with the use of quantum systems [11]. Almost a decade later, major breakthroughs in the field of quantum computing were proposed with applications in prime factorization by Shor [12] and searching large unsorted databases by Grover [13, 14]. These novel applications of quantum computing coupled with error correction protocols developed by Steane [15] and Shor [16] made the experimental realization of a quantum computer a highly valued goal.

Information stored in digital logic circuits is in binary form, either 0 or 1. In quantum information processing, information is stored in a quantum bit or *qubit*. A qubit is a quantum two-level system which can have superposition of both 0 and 1 : $\alpha \mid 0 > + \beta \mid 1 >$, where $\mid \alpha \mid^2 + \mid \beta \mid^2 = 1$ [17]. Example of such systems are cavity quantum electrodynamic systems [18], atoms in optical lattice [19], ions in

electrostatic traps [20], ensembles of nuclear spins in a liquid [21], purely quantum optical approaches [22, 23] and solid state approaches [24]. Solid state systems across both semiconductor and superconductor approaches constitute a major class of architectures that have utilized advances in lithography techniques to help realize micron to nanoscale quantum computer architectures. This thesis concentrates on developing new gating techniques to implement on phosphorus donors in silicon - a leading atomic-scale contender for solid state quantum computation. In particular it focuses on implementing a Al_2O_3 gate dielectric to introduce surface gates on buried STM-patterned donor devices in silicon.

Chapter 2 discusses the background information required for introducing a low temperature dielectric into atomic precision donor architectures. It starts off by discussing the reconstruction of the silicon surface in a 2×1 (001) formation, the starting surface for patterning atomic precision devices discussed in this thesis. The STM hydrogen lithography technique is described for achieving atomic precision phosphorus doping of devices in silicon. Subsequently, the fabrication and electrical transport properties of 2D δ-doped and STM-patterned planar nanostructures in silicon are discussed. Quantum computing is then introduced for different semiconductor host systems including donor and gate defined quantum dots. Lastly, the principle of growing Al_2O_3 using Atomic Layer Deposition (ALD) is discussed with methods to characterize the deposited layer.

Chapter 3 concerns itself with the robust and reproducible implementation of the ALD deposited dielectric layer of Al_2O_3 for STM-patterned δ-doped and planar nanostructures. Two main parameters, namely the optimum dose rate and precision

etching time are discussed in detail for different cases highlighting the need for establishing a recipe to integrate the Al_2O_3 dielectric into STM-patterned devices.

Chapter 4 presents the electrical characterization of three types of devices fabricated in the UHV environment of the STM with an Al_2O_3 dielectric and top gate, namely a 2D Si:P Hall bar, a 3-terminal phosphorus doped quantum dot device and a 4-quantum dot device. Excellent electrical performance of all three sets of devices was shown before patterning a top gate. After dielectric incorporation the ability to "top gate" these devices is presented showing the robustness of the dielectric layer and the stability of gate operations. The results presented in this chapter confirm the uniform quality of the Al_2O_3 film and the successful integration of a low temperature (200 ℃) Al_2O_3 dielectric on atomic precision devices.

Chapter 2

Background: Importance of top gating precision donor devices

2.1 Silicon

Silicon is the 14th element in the periodic table and has four electrons in its outermost shell. Each silicon atom in a crystal shares four bonds with its neighboring atoms. Silicon crystallizes similar to diamond in a face-centered cubic (fcc) crystal lattice structure with the four covalent bonds taking tetrahedral positions at an angle of 109.28° as shown in Figure 2.1 (a). Silicon has a lattice spacing $a = 5.43$ Å and contains two atoms in each primitive fcc cell separated by $a/4$ in each dimension. With four electrons per silicon atoms in the valency, there are 8 electrons that can fill successive Brillouin zones.

The conduction and valence bands in silicon do not overlap and silicon forms an indirect band gap. The width of the forbidden energy gap in silicon equals to

1.12 eV at 27 ℃ making silicon a semiconductor as shown in Figure 2.1 (b). The

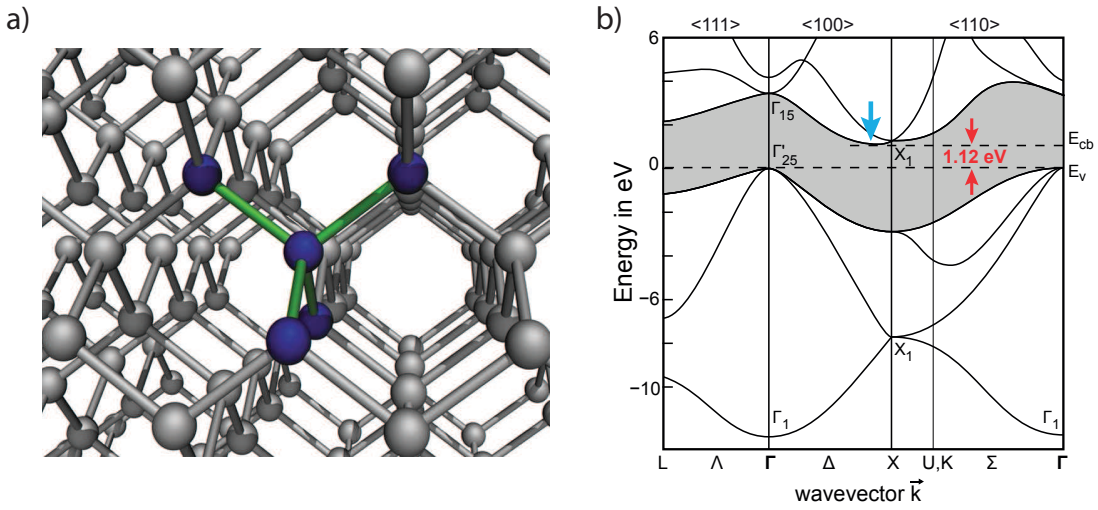

Figure 2.1: Silicon Crystal Structure. (a) Schematic of silicon bulk lattice structure showing each Silicon atom covalently bonded to four neighboring atoms in a tetrahedral geometry, (b) Corresponding band diagram between wave vector and energy in the [100] crystal direction. Blue arrow indicates minima of conduction band at k=0.85$\frac{2\pi}{a}$ which leads to 6 degenerate 'valleys'. Forbidden energy gap is shaded in gray with an indirect band gap of 1.12 eV at 27 ℃. Figure adapted from [25, 26]

conduction band minima in silicon occurs at $k = 0.85\frac{2\pi}{a}$ along the [100] crystal direction where $\frac{2\pi}{a}$ is the limit of the Brillouin zone. Due to the symmetry in the silicon crystal there are 6 [100] type directions giving six minima equivalents which are degenerate in energy and are called *valleys*.

Doping of silicon with impurities is performed in order to modulate its electrical properties. There are two kinds of dopant: acceptors and donors. Acceptors in case of silicon are boron, aluminum or other group III elements that have three electrons in their valence shell and accept an electron from silicon and thus provide holes for conduction. Donors in case of silicon are phosphorus, arsenic or other group V elements that have five electrons in their valence shell and provide an excess electron that can contribute to transport. Besides the type of dopant, also

the doping profile can vary. In this thesis, δ-doping is introduced to create active conducting structures. δ-doping of silicon is the process of introducing very narrow profile of dopant atoms in host semiconductor crystal. In this thesis δ-doping of silicon is performed by introducing high density ($n_s \approx 10^{14} cm^{-2}$) phosphorus within a single atomic 2D plane of silicon.

2.1.1 Si(100) 2×1 surface

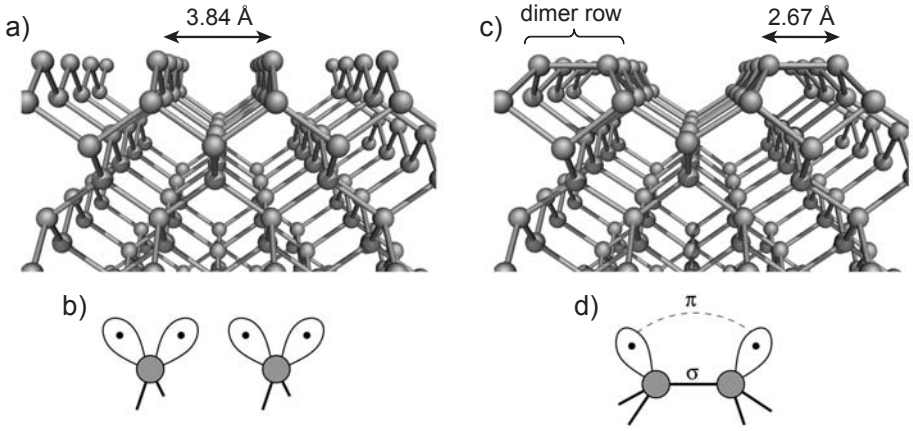

Figure 2.2: **Silicon(100) 2×1 surface reconstruction**. a) A bulk silicon crystal cut along (100) direction leads to a 1×1 surface which is energetically unfavorable. b) Silicon surface atoms in a 1×1 symmetry containing two valence electrons. c) Silicon dimer formation between two surface atoms leads to a 2×1 surface reconstruction which is stable. The pitch of parallel dimer rows is 7.68 Å. d). Surface silicon atoms in a dimer configuration are covalently bonded with a σ bond. The remaining dangling bond on the silicon atom in a dimer leads to formation of a weaker π bond. Figure adapted from [25].

In a bulk silicon crystal, the equilibrium position of each silicon atom is determined by forces exerted by all the other silicon atoms in the crystal resulting in a diamond-like fcc crystal structure. If the bulk silicon crystal is terminated along the (100) plane, then the forces holding the silicon crystal together are altered, changing the equilibrium position of the remaining silicon atoms. Most noticeably affected

are the surface atoms as these atoms are only experiencing forces from one direction. Silicon atoms at the surface in a 1×1 configuration are composed of a square array of silicon atoms as shown in Figure 2.2 (a). Each surface silicon atom has two valence electrons that are not participating in a covalent bond formation as shown in Figure 2.2 (b). The high number of dangling bonds present on the 1×1 surface makes the surface energetically unfavorable and results in a 2×1 reconstruction of the square lattice. In 2×1 surface reconstruction, silicon dimers are formed between two silicon atoms (bond length 2.67 Å) as shown in Figure 2.2 (c), thereby lowering the overall energy of the silicon surface. This leads to formation of weaker π bonds between the dimer row silicon atoms. 2×1 surface reconstruction reduces the number of dangling bonds by a factor of two and provides a high long-range order.

In this thesis, two types of devices are fabricated and studied on a 2×1 reconstructed Si(100) surface, namely δ-layer of phosphorus donor atoms in silicon and planar-doped nanostructures. Planar doped nanostructures are fabricated in UHV using the Scanning Tunneling Microscope (STM) hydrogen lithography, while δ-layers are fabricated in UHV environment of the STM. The phrase *donor atoms* will be used to refer to phosphorus donor atoms in silicon from now on.

2.2 Scanning Tunneling Microscopy based donor fabrication in silicon

The STM was invented by Gerd Binnig and Heinrich Rohrer at IBM Zurich in 1981 [27]. STM uses an atomically sharp metallic tip to scan across a sample [28]. When

a bias is applied between the tip and the surface, a very small current flows due to quantum tunneling of electrons in vacuum between the surface and the tip. The tip is scanned in the x-y plane while the tip height is controlled by a PID feedback loop such that the current remains constant. The height as a function of tip position gives a topographic image of the surface. Using this technique it is possible to image conducting surfaces such as silicon with atomic resolution and since then STM has become an essential tool to realize novel structures in science and nanotechnology [27].

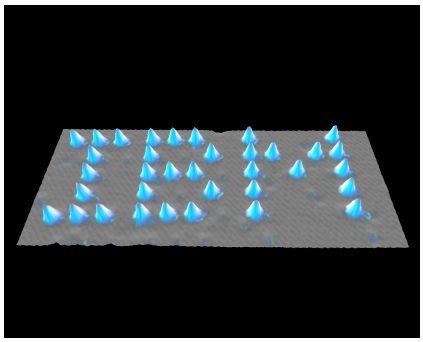

Figure 2.3: 35 Xenon atoms positioned on Ni surface to write IBM, using a STM tip by Eigler in 1990. Figure adapted from [29].

STM was first used by Eigler at IBM in 1990 to manipulate single atoms when he used a STM tip to pick up 35 Xe atoms and placed them on Ni surface to write IBM [29]. Figure 2.3 shows early demonstration of atomic manipulation by using on STM by for placing atoms on a metal surface. Achieving atomic manipulation in covalently bonded semiconductors was much more difficult. Four years later in 1994 Lyding first proposed to employ an atomic scale lithography strategy for patterning hydrogen terminated silicon surfaces by selectively desorbing hydrogen from the silicon substrate [30, 31]. This method has since been adapted by the Simmons group at UNSW to realize atomically precise devices in silicon using phosphorus

donors [32, 33]. The first step in this direction involved fabricating a conducting 2D Si:P monolayer in UHV to learn about the electrical properties and physics of epitaxial donor atoms incorporated in silicon. This was achieved by δ-doping of silicon in UHV using phosphine gas. Using δ-doped layers of donor atoms in silicon, important parameters such as the active carrier density n_s and mobility μ of the charge carriers in the 2-dimensional (2D) electron system were determined and studied extensively [34, 35]. The fabrication of devices with precision placed donors in silicon followed to utilize the promising aspect of STM hydrogen lithography to position individual atoms with angstrom level resolution. This is a critical aspect in realizing the Kane architecture for quantum computing that uses phosphorus donors in silicon as qubits [36], which will be discussed in greater detail in Section 2.6. First, the fabrication process used for engineering precision placed donor devices in silicon will be discussed. This consists of two parts: firstly, fabricating donor devices using STM lithography in UHV, and secondly, ex-situ processing of STM patterned devices using standard semiconductor processing techniques within the UNSW node of the Australian Nano Fabrication Facility (ANFF) in an ISO class 5 cleanroom facility.

2.2.1 Surface preparation for UHV devices

Two types of device fabrication strategies were performed in UHV in this thesis. They are, (i) 2D δ-doping of silicon layers with phosphorus and (ii) precision placing donor atoms in silicon using STM hydrogen lithography. The surface preparation in both the cases is similar after loading the sample into the UHV. However, the silicon sample used for STM hydrogen lithography is etched with registration markers that

are useful in both, STM lithography for patterning the device and also later in the cleanroom processing for successfully aligning ohmic contacts to the buried donor atoms in silicon [26]. These markers must be able to withstand the high temperature (∼1100 ℃) treatment performed during the surface preparation. Metal markers are not used on the silicon wafer because the presence of metal inside UHV will contaminate the STM chamber and the surface of the substrate. No registration markers are necessary for fabricating δ-doped layers in silicon.

Once the silicon wafer is mounted on a wafer holder and loaded in the UHV, it is outgassed at 350℃ for several hours using both indirect (heating the silicon wafer holder with the wafer mounted) and direct heating (heating the silicon wafer by passing a direct current through it) to remove adsorbents such as water. During the direct and indirect heating procedure, the silicon surface is protected by the native oxide layer. The silicon sample is then flash annealed to 1100 ℃ in order to remove the native oxide layer that was protecting the silicon surface from contaminants and is then slowly cooled to room temperature with a rate of (∼ 100℃/min) which eventually results in formation of a Si(001) -2 × 1 surface reconstruction as shown in Figure 2.2 (c).

Section 2.3 will present the fabrication procedure for the δ-layer in silicon using phosphine dosing to bring in the donor atoms in UHV and also provide an theoretical overview about the transport measurements performed at 4.2 K and device properties derived from those. Section 2.4 will discuss the fabrication of planar-doped nanostructures using STM hydrogen lithography which reduces the dimensionality of the active nanostructures to 0-D or 1-D, thereby requiring the framework of

quantum transport.

2.3 Delta-doped (δ-doped) layers in silicon fabricated in UHV

As mentioned in Section 2.1, δ-doping silicon will alter its electronic properties. In order to measure the electrical properties obtained after doping silicon, δ-layers were fabricated inside STM in the UHV environment of the STM.

Fabricating δ-doped devices in silicon

As discussed in Section 2.2.1, the surface treatment inside UHV results in a highly reactive 2 $\times$ 1 reconstruction of the silicon surface. A schematic outlining the important steps in fabricating of δ-layers in silicon is shown in Figure 2.4 (a). The next step in the fabrication of δ-layers in silicon is carried out by exposing the 2$\times$1 Si (001) surface to phosphine (PH_3) gas for 2 minutes at a chamber pressure of 2×10^{-7} mbar. Dosing the surface with PH_3 will continue until no reactive silicon sites are available. Figure 2.4 (c) shows an STM image of the silicon surface showing disorder coverage of Si:PH_x (x=1,2). The reason for Si:PH_x (x=1,2) is because phosphine gas after attaching to the reactive silicon surface dissociates into PH_2 and PH.

Full density functional analysis and silicon surface studies have been conducted to understand the dissociation pathways of how phosphorus incorporates into the silicon crystal [25]. Dissociation of PH_3 to P into the silicon crystal happens as phosphine successively looses hydrogen atoms before incorporating into the silicon

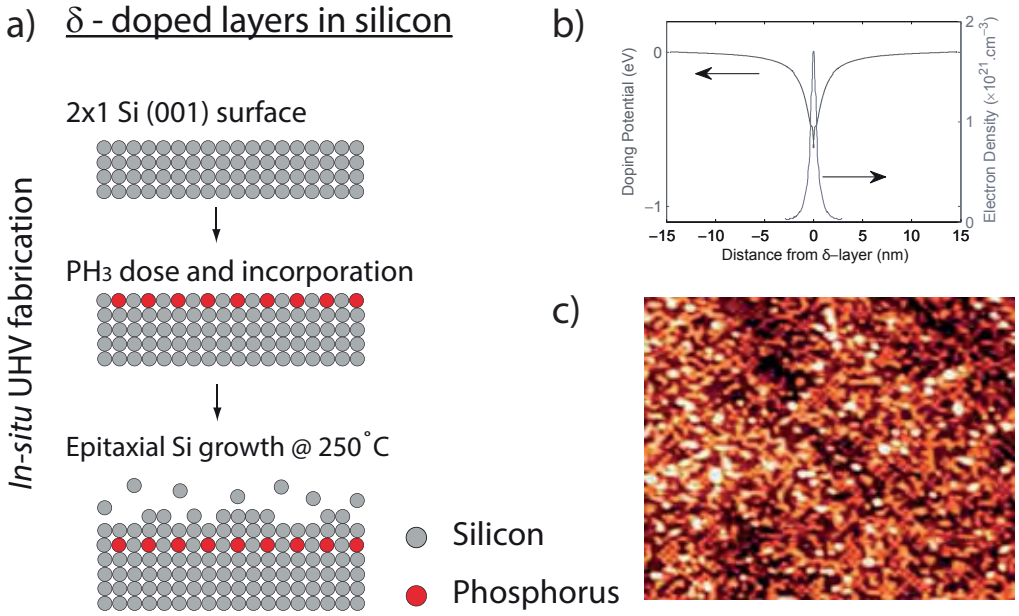

Figure 2.4: Delta doped device fabrication in UHV STM. a) Schematic of a δ-layer fabricated in UHV STM on silicon using PH_3 gas and encapsulated with silicon at 250 ℃. b) The coulomb potentials of donors incorporated in the δ-layers form a sharp potential well which confines the conduction electrons within a $\sim$ 2 nm wide layer vertically. Figure adapted from [37]. c) STM image showing a Si (100) 2×1 surface dosed with PH_3 gas. Figure adapted from [35].

crystal as shown in the following reaction.

$$PH_3 \rightarrow PH_2 + H \rightarrow PH + 2H \rightarrow P + 3H \rightarrow P \text{ (incorporated in the silicon crystal)}$$

The incorporation step of P atom into the top layer of the silicon surface is performed when the sample is annealed to ∼350 ℃ for 1 minute as shown in Figure 2.4 (a). This step results in the formation of Si-P hetrodimers where phosphorus replaces one silicon atom from the crystal lattice. To electrically activate the donors, the patterned structure is then encapsulated with epitaxially grown silicon as shown in Figure 2.4 (a) step 3 keeping the substrate temperature low at 250 ℃ which is chosen to so that the vertical integrity of doping profile is maintained by minimizing

donor diffusion [38, 39]. The target encapsulation thickness for all the devices is around 45- 50 nm.

2.3.1 Electron transport in δ-doped layers in silicon

For δ-doped layers in silicon, the classical Hall effect will be discussed and how magnetotransport measurements at 4.2 Kelvin are used to extract the active carrier density n_s and carrier mobility μ. The active sheet carrier density n_s in a δ-doped layer is defined as number of charge carrier per unit area that participate in transport. n_s of a system provides information about the level of doping in the conduction plane because unlike other systems, the plane of conduction is directly where the phosphorus dopants are present. Carrier mobility (μ) is a measure of the average velocity acquired by an electron when an external electric field **E** is applied in the plane of delta doped layer. The Si:P δ doped layer is a diffusive system where transport is controlled mainly by scattering from ionized phosphorus donors within the conduction plane. μ is important to quantify because it provides information about the electronic charge distribution present in Si:P channel.

Classical Hall Effect

The classical Drude model for conductivity [40] gives the conductivity σ, of a 2-dimensional (2D) layer of dopants as:

$$\sigma = \frac{n_s e^2 \tau}{m} \tag{2.1}$$

where σ is the conductivity, n_s is the active carrier density, e is the electron charge, τ is scattering time and m is the effective mass of the electron in silicon. The mobility of the electrons is a measure of the average velocity acquired when an electric field E is applied,

$$v = -\mu E, \tag{2.2}$$

where v is the average drift velocity of an electron. Using ohm's law, the current density, $\mathbf{j}$ is given by,

$$j = -n_s e v = \sigma E, \tag{2.3}$$

Using equation 2.2 and 2.3, the mobility μ can be expressed as

$$\mu = \frac{\sigma}{n_s e} = \frac{e\tau}{m}, \tag{2.4}$$

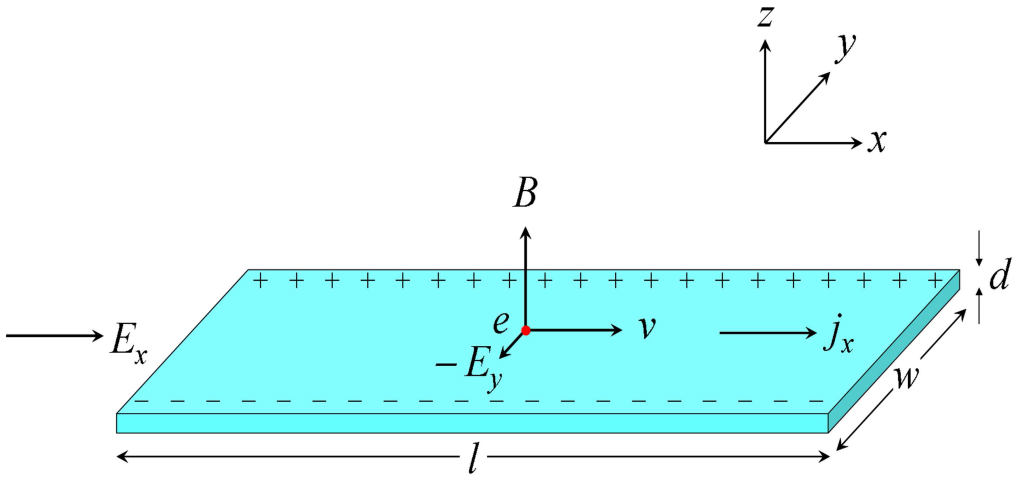

Figure 2.5: Classical Hall effect for a 2D system. Figure adapted from [34].

On the application of a magnetic field (B) perpendicular to the electron transport in x-direction, an electric field (E_y) is induced in the 2D conductor perpendicular to both the electron transport direction and applied magnetic field (classical hall effect

as shown in Figure 2.5). The resultant conductivity becomes a tensor quantity. Equation 2.3 thus transforms to

$$\begin{pmatrix} j_x \\ j_y \end{pmatrix} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ \sigma_{yx} & \sigma_{yy} \end{pmatrix} \begin{pmatrix} E_x \\ E_y \end{pmatrix}, \tag{2.5}$$

However, it is convenient to express equation 2.5 with resistivity tensor because in a typical magnetotransport measurement constant current is maintained and voltages in longitudinal and transverse direction are measured. Therefore, the relation looks like this

$$\begin{pmatrix} E_x \\ E_y \end{pmatrix} = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{pmatrix} \begin{pmatrix} j_x \\ j_y \end{pmatrix}, \tag{2.6}$$

Lorentz force acting on the electrons flowing in the x-direction with velocity v_x is balanced by the electric force in the y direction, E_y:

$$B_z v_x e = E_y e \tag{2.7}$$

where B_z is the applied magnetic field and e is the elementary charge of an electron.

Using equations 2.7 and 2.4, ρ_{xy} and ρ_{xx} can be derived as

$$\rho_{xy} = \frac{B}{n_s e} \quad , \quad \rho_{xx} = \frac{1}{n_s e \mu} \tag{2.8}$$

Thereby giving a relation between measurable quantities (ρ_{xx} and ρ_{xy}) and device properties of interest: the active carrier density and the mobility.

Magnetotransport measurements in δ-doped Si:P devices

The δ doped layers fabricated using in the UHV environment of the STM are processed into Hall bars to perform magnetotransport measurements and compute transport characteristics of the Si:P 2D electron gas. Hall bar mesas are defined using EBL with length L= 100 μm and width W = 20 μm. Mesas are then etched at a rate of $\sim$ 60 nm/minute using RIE. Aluminum bonds are made to the contact pads of the Hall bars establishing contact with the δ-layer. Hall bar measurements are performed at 4.2 K in a helium dewar. At such temperature scales, all the impurities from the bulk doping are frozen and transport can only occur through the δ-layer which is doped with phosphorus.

A typical magnetotransport curve for a Si:P δ-layer is shown in Figure 2.4 along with configurations for measuring experimentally accessible parameters R_{xx} and R_{xy} under the influence of an external magnetic field. R_{xx} is the longitudinal resistance and R_{xy} is the transverse resistance measured by induced voltages in longitudinal and transverse direction, respectively. R_{xy} gives the number of electrons contributing to conduction and R_{xx} is used to calculate the resistivity of the channel and mobility of electrons.

Performing electrical measurements on the Si:P δ-layers fabricated using the STM and patterned into Hall bars, one obtains $\mu \approx$ 10-100 cm^2 /V s and $n_s \approx 10^{14}$ cm^{-2} [34, 35]. It is worthwhile to compare this with n_s and μ for Si/SiGe based 2D electron system where typical $n_s \approx 10^{11}$cm^{-2} and $\mu \approx 10^4 - 10^5$ cm^2/V s. This clearly explains the reason for lower mobility in the Si:P δ-layers as they have much higher carrier density and as a consequence the current is flowing through the

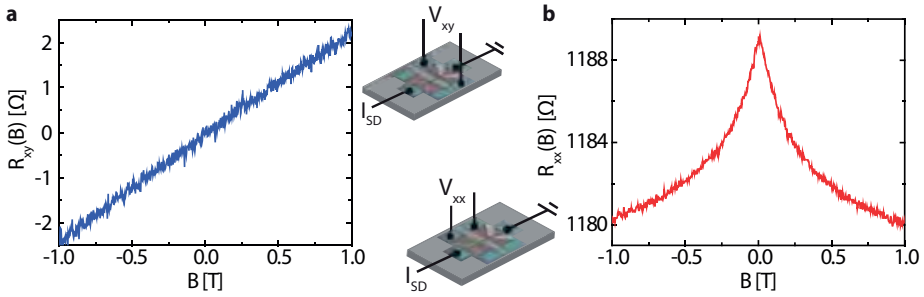

Figure 2.6: Typical magnetotransport measurement of a Si:P δ-layer at 4.2 Kelvin with $n_s \sim 2\times10^{14}$ cm^{-2}. (a) Hall trace of R_{xy} used to obtain carrier density, and (b) R_{xx} used to obtain resistivity and carrier mobility of electrons in a δ-layer. Figure adapted from [35].

disordered 2D doped layer. The linear dependence observed in Figure 2.6 (a) is the result of the Lorentz force balanced by the electric field perpendicular to the flow direction (Equation 2.7), while the result from Figure 2.6 (b) can be understood in the framework of weak localization which will be discussed in the following section.

Weak Localization

Negative magnetoresistance as shown in Figure 2.6 (b) is a typical characteristic of highly-diffusive systems where electron trasport takes place predominantly via ionized impurity scattering. In these systems, an effect called weak localization is observed which is a quantum mechanical effect that results in a negative magnetoresistance with increasing magnetic field B at low temperatures.

Consider the example shown in Figure 2.7 where an electron propagates from origin O in a highly disordered system by scattering at the labelled scattering centres. The path taken by the electron in the first case is shown with solid line while another complimentary path that can be taken by the electron is shown with dashed line. In both the cases the electron ends up at the starting position O which leads

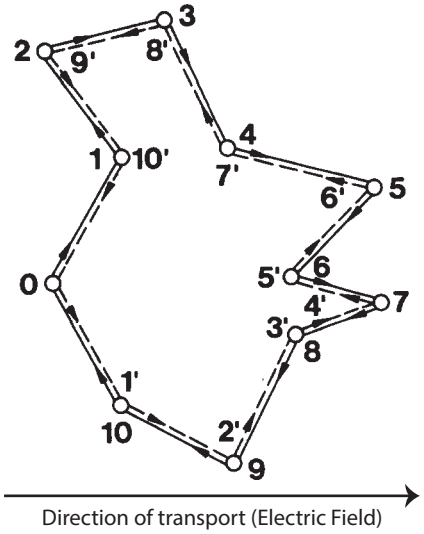

Figure 2.7: Diffusion path of an electron in a disordered system. The electron is propagating in both directions and in the quantum diffusion regime (such as a Si:P δ-layer) the probability to return to the starting position is twice as much because the amplitudes add coherently. Figure adapted from [41].

to constructive interference at the starting point (i.e. higher probability that the electron can be found after the series of scattering events again at the starting point rater than at, e.g. point 5) and increased resistance (lower conductivity) in the system. However, under the application of a perpendicular magnetic field, an electron propagating through the system acquires a phase and the observed interference is weakened or destroyed. This effect that leads to the increased resistance in the system is known as weak localization. Weak localization is experimentally demonstrated in the magnetotransport measurements for a Si:P δ-layer as shown in Figure 2.6 (b) where increasing the magnetic field leads to a decreased resistance in the system.

2.4 Planar-doped nanostructures in silicon patterned by STM

Introducing a 2D electron system of phosphorus donors into the silicon crystal enhances its electronic properties as discussed in Section 2.3 by using δ-doping. Interestingly further reduction in the dimensionality is achieved by patterning the δ-layer into 0-D quantum systems, known as quantum dots which are quantized in energy and charge. These zero-dimensional system are able to hold a fixed amount of charge and have discrete energy spectrum rendering their use in studying quantum phenomena.

STM hydrogen lithography

A silicon sample with etched registration markers undergoes the heating treatment specified in Section 2.2.1 resulting in a 2×1 Si (001) surface. In contrast to the 2D structures discussed in Section 2.3 where the reconstructed 2×1 Si (001) surface was directly exposed to phosphine, for performing the STM hydrogen lithography, the 2×1 Si(001) surface is exposed to atomic hydrogen (by cracking the hydrogen molecule) for 6 minutes at a chamber pressure of 5×10^{-7} mbar and at a substrate temperature of ∼350 ℃, which results in a hydrogen terminated Si(001) -2 × 1 surface as shown in Figure 2.8 (a).

STM lithography can then be performed on the hydrogen mask (comparable conceptually to EBL where one patterns a resist mask using a beam of electrons) by applying voltage to the tip of the STM which then selectively desorbs hydrogen [30]

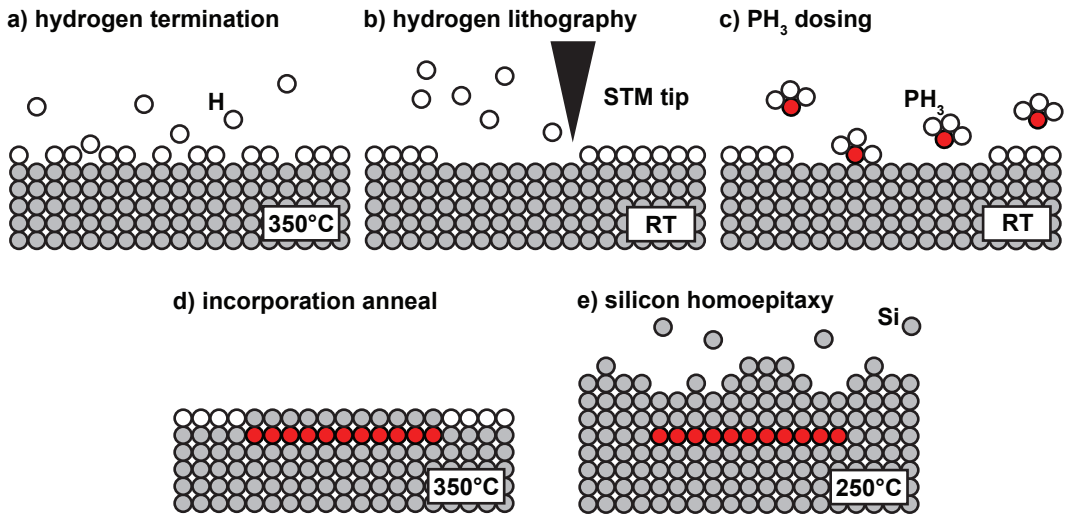

Figure 2.8: Schematic of atomically precise lithography and device fabrication process (a) Surface termination of silicon (100) 2x1 with monoatomic hydrogen to form an atomic scale mask, (b) Using tip of an STM to selectively remove hydrogen from desired areas, (c) Dosing the active areas of silicon using phosphine gas, (d) Incorporation of phosphorus into silicon lattice using an anneal at 350 ℃, (e) Epitaxially growing silicon over phosphorus at 250 ℃. Figure adapted from [42]

as shown in Figure 2.8 (b). There are two modes of hydrogen desorption, the low bias, high current mode where the desorption mechanism is due to inelastic electron tunneling which induces exictational-vibrational mode of the Si-H bond. And the high bias, low current mode where direct excitation of Si-H covalent bond removes the H [30]. STM fabricated devices consists of two types of structures: inner device structures (within 200x200 nm^2 scan area) and extension leads (few microns long) as shown in Figure 2.9 (a). For patterning the inner device structures, sub-nm precision is required and therefore the low bias (2-4 V) and high currents ($\sim$ 10 nA) mode is used to achieve precision in the desired pattern with minimum stray desorption (unwanted hydrogen desorption outside of the desired pattern). Patterning the extension leads is performed using a high bias (6-8 V) and low currents (3-4 nA) mode where higher stray desorption is not so vital. These extension leads are later used

for establishing ohmic contact with the buried nanostructures. After finishing the device patterning using STM lithography, processing is equivalent to the previously discussed fabrication of δ-layers with the difference being only that phosphine can only absorb to the patterned areas as shown in Figure 2.8 (c) and (d). Epitaxial silicon growth is then performed on the STM fabricated device as shown in Figure 2.8 (e).

2.4.1 Ex-situ processing of planar STM patterned nanostructures

After successful STM patterning and encapsulation, post processing is carried out in the cleanroom facilities at ANFF. In order to perform electrical measurements, ohmic contacts are aligned with the STM fabricated device underneath the encapsulation layer of silicon. This is a two step process where firstly holes are etched aligned to the ohmic contact pads on the STM patterned silicon surface and secondly metal is evaporated to establish contact with the buried planar nanostructures with a schematic depiction of the process as shown in Figure 2.9 (a).

First, the encapsulation thickness is measured using Atomic Force Microscope (AFM). Using the etched registration markers the exact location of the STM patterned device can be found. A pattern of holes with diameters of $\sim$ 150 nm and pitch $\sim$ 500 nm are aligned on top of the patterned device using EBL. To define the hole pattern, PolyMethylMethAcrylate (PMMA) A4 950 K (1 K= 1 Kilo Dalton = 1000 grams per mole) is spin coated on top of the silicon surface and baked at 180 ℃ for 5 minutes before performing EBL. After development, the hole pattern is

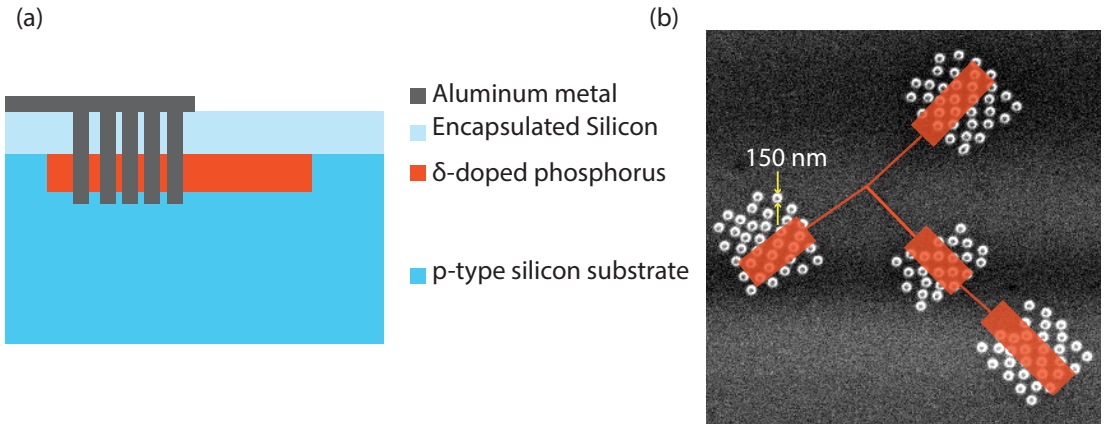

Figure 2.9: Cleanroom processing for contacting buried δ-doped STM patterned nanostructures. (a) Side view schematic showing RIE based etching method used for contacting δ-doped nanostructures in silicon by patterning holes using EBL. Holes are typically etched to $\sim$ 1.5-2 times the thickness of encapsulated silicon. Aluminum metal is evaporated in these etched holes to contact buried δ-doped nanostructures. (b) Top view image showing array of holes patterned using EBL aligned to the buried contacts of a quantum dot device patterned in STM using hydrogen lithography (STM pattern overlaid in orange). The holes are $\sim$ 150 nm in diameter with a pitch of $\sim$ 500 nm.

then etched down to the STM patterned device by Reactive Ion Etching (RIE) with CHF_3:SF_6 gas mixture at a 5 mTorr pressure and 40:20 sccm mass flow [26]. Etch rates obtained using this recipe are around 50-60 nm/minute. Figure 2.9 (b) shows the holes aligned on top of the STM fabricated planar nanostructures (overlaid in orange). The residual PMMA resist in the holes is removed using an O_2 plasma etch, followed by an acetone rinse in an ultrasonic bath followed by IPA clean. The mask for ohmic contacts is patterned over the etched holes using EBL with PMMA as a resist. A BHF 1:15 dip is performed before depositing metal to remove the native oxide. Aluminum metal is then deposited on to the substrate using a electron-beam metal evaporation with a deposition rate of 0.5 nm/sec with a final thickness of 80 nm. Lift-off is then performed by placing the substrate in a solution of N-methyl-2-pyrolidone (NMP) for 60 mins which removes PMMA with aluminum on top and

leaving the metalized ohmic contacts only.

2.4.2 Electron transport in a donor quantum dot

A single quantum dot in transport can be represented schematically as shown in Figure 2.10 (a). The metallic island forming the quantum dot in Figure 2.10 (a) is tunnel coupled to the source and drain terminals, allowing the flow of electrons from source via the island to drain. The metallic island is also capacitively coupled to the gate electrode which can be used to tune the potential of the island relative to the source and drain. At low temperatures, there is a significant energy cost

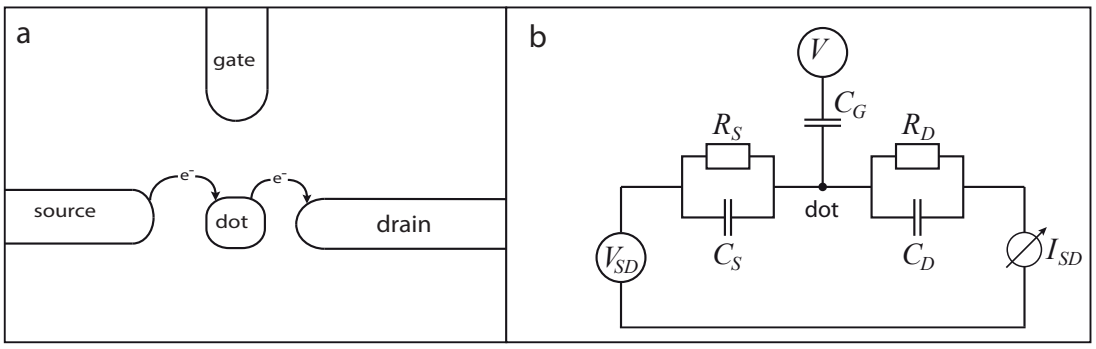

Figure 2.10: Quantum dot device in transport regime. (a) The quantum dot is tunnel coupled to source and drain terminals and capacitively coupled to a gate terminal. (b) A circuit diagram illustrating the quantum dot. Tunnel junctions are modeled as a resistor and capacitor network in parallel. The charging energy of the quantum dot is given by e^2/C_{tot}, where C_{tot} is the self capacitance of the quantum dot, $C_{tot} = C_{source} + C_{drain} + C_{gate}$.

for adding an electron to the quantum dot, compared to the thermal energy of the electrons, given by k_BT, which is called the charging energy E_C that results from the mutual repulsion between the electrons on the island. Until the charging energy is supplied, the quantum dot remains in a state where no current can flow. This is known as Coulomb blockade. Coulomb blockade can be observed experimentally if

the following two conditions are met [43].

1. First, the thermal energy of the quantum dot system must be lower than the charging energy of the quantum dot, $E_C \gg k_B T$. This condition can be satisfied by performing the experiments at cryogenic temperatures and reducing the size of the quantum dot such that the charging energy is significantly larger than the thermal energy. To illustrate this condition, a quantum dot with just one phosphorus donor atom is considered. The sum capacitance of a sphere can be used as an approximation for a single donor given by $C = 4\pi\epsilon_0 R$ where R $\sim$ 2.5 nm is the Bohr radius (neglecting additional capacitance resulting from the coupling to source, drain and gate electrodes)[44]. Since the donor quantum dot is embedded in crystalline silicon, it is safe to assume a dielectric constant of 11.7 for silicon and estimate the charging energy to be $\sim$ 49 meV. This energy corresponds to a temperature of 600 K which exceeds the typical measurement temperature of 4.2 K performed in this thesis by a very large amount.

2. Secondly, the tunnel coupling between the quantum dot and source and drain terminals has to be sufficiently weak to avoid any fluctuations in the number of electrons occupying the quantum dot during the measurement. This places a lower limit on the tunnel resistance that is required for the tunnel junctions for source and drain terminals, set by the Heisenberg uncertainty principle. The energy uncertainty must be smaller than the charging energy, $\triangle E \ll e^2/C_{tot}$, while $\triangle t$ can be estimated using the RC time constant from the circuit diagram in Figure 2.10 (b), $\triangle t \sim R_{source,drain} C_{tot}$. Now, for the energy uncertainty to

be much smaller than the charging energy there is a minimum value for the tunnel resistance, that is $R_{source,drain} \gg h/e^2 \approx 25.8$ kΩ.

The quantum dot shown in Figure 2.10 (a) is capacitively coupled to the gate electrode which can be used to change the electrochemical potential of the quantum dot island capacitively. Applying a voltage V_G to the gate electrode changes the electrostatic energy of the quantum dot in a continuous manner. Raising (lowering) the electrostatic energy of the quantum dot leads to an electron to tunnel off (on) the dot, thereby minimizing the overall electrostatic energy of the device. In Figure 2.11 a STM patterned quantum dot with a charging energy of ~ 7 meV is used and the gate voltage is varied for a fixed source drain bias of 2 meV. When the system is biased such that the electrochemical potential of the quantum dot is set between the 'bias' window of the source and drain electrochemical potential, the charge state of the quantum dot constantly fluctuates by one electron and current can flow resulting in a peak in the quantum dot current. Due to such operation, these kind of quantum dot devices are called a single electron transistor. The first instance of controlled single electron tunneling was observed in aluminum tunnel junctions in 1987 [45].

2.4.3 The constant-interaction model

A simple theoretical model that is used to describe the phenomenon of Coulomb blockade with a set of discrete energy levels is called the constant-interaction model [46]. This model is based on two assumptions, (a) the energy levels present in the quantum dot are discrete and independent of the number of electrons N occupying the dot, and (b) the interactions between all the terminals in the device with

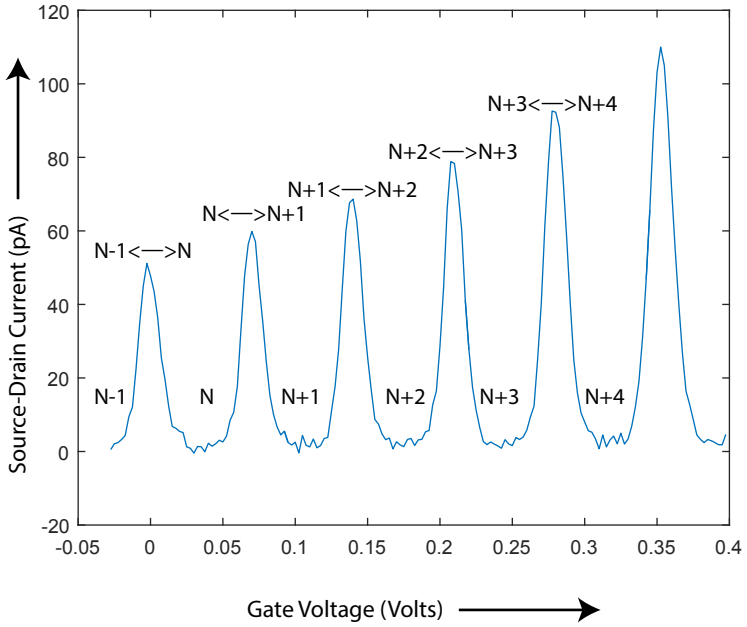

Figure 2.11: Experimental observation of Coulomb peaks observed in a STM patterned quantum dot with a charging energy of $\sim$ 10 meV. The figure shows periodic Coulomb peaks where each valley corresponds to the addition of an electron to the quantum dot by varying the gate voltage.

the quantum dot island are constant. The system can be fully described using a schematic diagram as shown in Figure 2.10 (b) with tunnel junctions modeled using resistor and capacitors in parallel. The total energy of the quantum dot with N electrons is given by

$$U(N) = \frac{[-(N - N_0)|e| + C_S V_{SD} + C_G V_G]^2}{2C_{tot}} + \sum_{i=1}^{N} \epsilon_i \tag{2.9}$$

where C_{tot} is total mutual capacitance between the dot and all electrodes, $C_{tot} = C_S + C_D + C_G$. In the case described using equation (2.9) it is assumed that a voltage V_{SD} is applied to the source terminal with the drain terminal grounded and V_G is applied to the gate electrode. N_0 is the number of electrons at zero voltage on the gate and source. The first part in equation (2.9) describes the electrostatic

energy calculated using the circuit shown in Figure 2.10 (b) and the second term is the sum of all filled single-particle energy levels. In order to describe experiments such as the quantum dot in transport where the number of electrons occupying the dot is constantly altered, it is easier to describe the process using electrochemical potential of the dot. The electrochemical potential μ_N is defined as the energy difference between the quantum dot occupied with N and N-1 levels filled with electrons is,

$$\begin{aligned}\mu(N) &= U(N) - U(N-1) \\ &= \frac{e^2}{C_{tot}}\left(N - N_0 - 1/2\right) - \left[\left(\frac{C_S}{C_{tot}}\right)eV_{SD} + \left(\frac{C_G}{C_{tot}}\right)eV_G\right] + \epsilon_N\end{aligned} \tag{2.10}$$

Equation 2.10 has terms $\frac{C_S}{C_{tot}}$ and $\frac{C_G}{C_{tot}}$ which are called *lever arms* and are used to convert the equivalent change in voltage applied on source and gate electrodes to a change in energy in the electrochemical potential energy of the SET.

For the quantum dot, the energy spacing between discrete levels is defined as the addition energy E_{add},

$$E_{add} = \mu_{N+1} - \mu_N = E_c + \triangle E_N \tag{2.11}$$

The addition energy is defined as the sum of charging energy plus the single-particle energy level spacing where $\triangle E_N = \epsilon_{N+1} - \epsilon_N$.

The energy diagram of a quantum dot depicting the alignment of its electrochemical potential with respect to the electrochemical potential levels of source and drain terminals is shown in Figure 2.12 (a). The source and drain terminals are filled

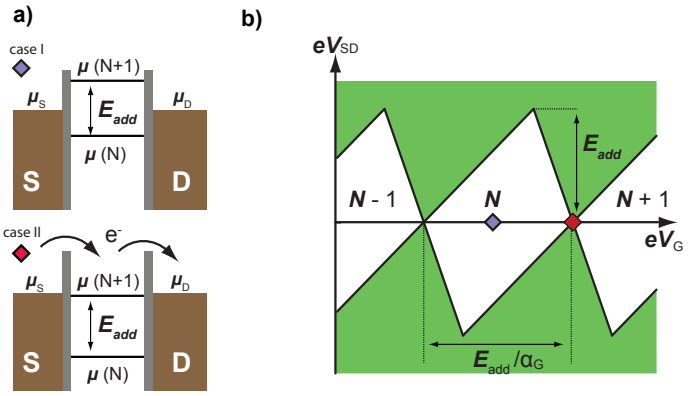

Figure 2.12: Coulomb Blockade and Coulomb Diamonds. (a) Low source drain bias energy level diagram of a quantum dot island connected to source and drain terminal through tunnel junctions. In case I, the system is in blockade and the quantum dot contains N electrons. In case II, the electrochemical potential of quantum dot is aligned with source and drain terminal, therefore current can flow. (b) Stability diagram of the quantum dot showing regions of coulomb blockade (inside the diamond shaped regions) obtained by sweeping the gate voltage with respect to source drain bias. Inside the diamond (shown as case I) the number of electrons on the quantum dot is fixed,leaving the system in blockade. However, in case II the electron number keeps oscillating between N and N+1 and current flows. The height of the coulomb diamonds along the eV_{SD} source bias axis directly corresponds to the addition energy, while along the gate voltage axis the lever arm α_G due to the capacitive has to be taken into account.

with electrons up to the electrochemical potential levels of μ_S and μ_D, respectively.

In case I, as shown in Figure 2.12 (a), there is no electrochemical potential of the SET aligned with μ_S and μ_D, thus the system remains in blockade and no current flows, which corresponds to the minima in the measurements of the coulomb blockade presented in Figure 2.11. Case II shows the condition where $\mu(N+1) = \mu_s = \mu_D$. This situation is achieved by changing the voltage on the gate electrode that brings the electrochemical potential level μ_{N+1} of the quantum dot in line with the source and drain electrochemical potentials. In this case, transport between source and drain terminals is allowed with the electron number on the quantum dot fluctuating between N and N+1, corresponding to the maxima in the quantum dot current in

Figure 2.11.

By increasing the source-drain bias (vertical axis on the stability plot in Figure 2.12 (b)) the charging energy of the quantum dot can be directly measured. Since the coulomb blockade suppresses charge flow as long as no electrochemical potential of the quantum dot is aligned between μ_S and μ_D, the maximum bias voltage where blockade is observed directly corresponds to the charging energy. Beyond this point, there is always at least one electrochemical potential level of the quantum dot within the bias window, allowing the flow of electrons independently of the gate voltage settings. The gate voltage between two coulomb peaks from Figure 2.8 (b) to add an extra electron can be calculated using equation 2.11.

$$\triangle V_G = V_G^{N+1} - V_G^N = \frac{C_{tot}}{eC_G}(\mu_{N+1} - \mu_N) = \frac{1}{e\alpha_G}E_{add}, \tag{2.12}$$

where $\alpha_G = \frac{C_G}{C_{tot}}$ is the lever arm of the gate electrode G which converts a change in voltage on gate G to a change in energy in the electrochemical potential of the quantum dot.

2.5 Quantum computing with quantum dots in silicon

In this chapter so far discussion about the fabrication and electron transport of δ-doped layers in silicon along with planar doped nanostructures that form 0-dimensional quantum dots has been done. Quantum dots presented in Section 2.4 have since been utilized in the few- and single-electron regime to realize Si:P based quantum dots for

single shot spin readout in quantum computing. This section presents the necessary requirements for an architecture to be utilized in quantum computing and then discusses various semiconductor based systems and their experimental implementation and achievements.

In 1998 Loss and DiVincenzo proposed the use of quantum dots to build a quantum computer using electron spin states, spin up ($|\uparrow\rangle$) and spin down ($|\downarrow\rangle$) [47]. At the same time Kane proposed using the electron and the nuclear spins of donor impurities in silicon to be used as a qubit for realization of a quantum computer [36]. The field of quantum computing was heavily impacted when DiVincenzo laid out the 7 key criteria for implementation of a quantum computer [48], which are:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state, such as their ground state
3. Long relevant decoherence times, much longer than the gate operation time
4. A 'universal' set of quantum gates to control each qubit and the coherent interaction between pair of qubits
5. A qubit-specific measurement capability
6. The ability to interconvert stationary and flying qubits
7. The ability to faithfully transmit flying qubits between specified locations

Semiconductor based systems using silicon have experimentally encoded quantum information in various forms such as charge state of an electron [49], spin state

of an electron [50], nuclear spin state of phosphorus [51], singlet triplet configuration of two electron spins [52] (orientation of spins in a two spin system), hybrid of spin and charge state of 3 electron spins [53]. In this thesis, focus will be on STM based donor quantum dot systems which use the proposals outlined by Loss & DiVincenzo [47] and Kane [36] for realizing a quantum computer.

2.5.1 Donor based quantum dots

Using a donor based architecture for quantum computation, one can realize two qubits with using one atom of phosphorus, namely the electron spin qubit and the nuclear spin qubit since phosphorus has a nuclear spin 1/2 [36]. Besides the so-called bottom-up approach pursued using STM fabrication discussed earlier in Section 2.4, there is also significant progress achieved in the top-down approach.

The top-down approach uses low energy ion-implantation of few to single phosphorus donors [54] with metallic gates and high quality oxides grown later. The disadvantage of this technique is that it does not provide high precision placement of phosphorus donors and only limited control over the number of donors implanted, because the implantation region is fairly large $30 \times 30\text{nm}^2$ [55]. However, to operate single spin qubits (electron and nuclear) in this architecture, atomic precision of location of phosphorus atom is not needed [56]. Electron spin readout of donor atom in silicon using ion implantation was carried out in 2010 [57]. Following this, an electron spin qubit in a device with $\sim$ 30 P donors was demonstrated in 2012 [50] and in the same device nuclear spin qubit in 2013 [51]. The coherence times of electron and nuclear spin qubit in donor using ion implantation have been further

improved to $\sim$ 1 second and $>$ 30 seconds, respectively [58]. Very recently, donor based qubits using ion implantation have also shown entanglement between the nuclear spin and the electron spin of a donor and violated bell's inequality with >96% fidelity [59].

Using the bottom-up fabrication approach atomically thin wires [60], single atom transistors [33], and the fabrication of single [61] and double quantum dot [62] have been demonstrated with atomic precision. Importantly, STM based lithography has shown precision placement of a single donor in silicon with 1 nm accuracy [33] and the ability to place individual atoms deterministically into the device, crucial for scalability. On top of that STM based donor qubits using an electron spin bound to a phosphorus atom have demonstrated high readout and initialization fidelity well above the fault tolerant level as required in quantum computation [63]. Dual spin readout of two electron spins coupled to two donor clusters has also been shown with exceptionally high fidelity [64]. The next major milestone for donor based architecture using STM lithography is the demonstration of one and two qubit gates, i.e. achieve coherent control of a single spin state and (where the strength of the STM approach comes into play) engineer coupling between two qubits.

Typically STM based devices use all epitaxial in-plane gates that are made of phosphorus doped silicon and patterned in the device with sub-nm precision to the qubits. As a consequence STM devices do not have a dielectric layer intentionally grown on them, but rather have a native oxide in form of SiO_2 as a dielectric formed during the ex-situ cleanroom processing. Despite exceptional stability of Si:P devices as compared to other implementations due to fixed device parameters by design (for

e.g. the tunnel rates) [69] the presence of a surface oxide might lead to decoherence in the system due to electrostatic fluctuations arising from movement of charges in the oxide layer or on the oxide semiconductor interface [65, 66]. The spin of an electron in donors is typically protected from charge noise due to the weak spin-orbit interaction but charge fluctuations at the interface could still be the cause of relaxation of spins in donors causing loss of information [65, 67]. Charge sensing in STM patterned quantum dots is achieved by employing a SET based quantum dot [68]. It is important to note that the distance between the Si/SiO_2 interface and the planar nanostructures (where the active device structures like donor quantum dot or charge sensors are formed) is given by the thickness of the encapsulated Si layer which is $\sim$ 50nm. Recently, low-frequency electrical noise studies of STM-patterned donor based devices showed that samples with a native oxide exhibited excellent stability better than any other nanostructured devices including carbon nanotubes[69]. However, when samples incorporated a poor quality grown low temperature SiO_2 dielectric in an attempt to add top gates, interface charges were identified as the major source of noise and electrostatic instability [69].

To tackle the problem of fabricating reproducible interfaces (rather than just a native oxide), in this thesis the use of Al_2O_3 dielectric is investigated. The donor based fabrication procedure using STM does not have a high thermal budget ($>$ 350 ℃) as this leads to dopant diffusion out of the lithographically patterned regions [70]. This constraint essentially limits the ability to grow high quality thermally grown SiO_2 as a dielectric on encapsulated silicon in the UHV (where T required is $>$ 600 ℃). However, growing a low temperature dielectric SiO_2 at $\sim$ 200 ℃ in UHV for STM

patterned devices was attempted [71]. The interface quality of the low temperature SiO_2 dielectric was poor and it produced an oxide with a very high defect density at the surface and a high interface trap density leading to large leakage currents [71]. Therefore, a suitable dielectric material compatible with the low STM device processing temperature is investigated and pursued in this thesis. To illustrate the use of dielectric in quantum electronic devices, different semiconductor qubit architecture are discussed that rely on the control of 2D conducting layers using electrostatic potentials applied using top gates which naturally need to deal with the interface quality.

2.5.2 Gate defined quantum dots in semiconductor systems

Another category of quantum dot architecture utilizing Loss and DiVincenzo criteria to use an electron spin for quantum computation is gate defined quantum dots. Gate defined quantum dots in general are mainly utilized using two approaches, first using gallium arsenide/aluminum gallium arsenide (GaAs/AlGaAs) based heterostructures and secondly using silicon/silicon germanium (Si/SiGe) based heterostructures.

Gate defined quantum dots in GaAs/AlGaAs were the first semiconductor quantum dot based system to fulfill 5 of the key criteria listed by DiVincenzo. They first showed spin readout of an electron spin [72], followed by controlled single qubit [73] and two qubit [74, 75] gate operations. Gated quantum dot systems have the flexibility of tuning multiple parameters such as tunnel rates and tunnel couplings between their nanostructures. However, GaAs/AlGaAs based quantum dots suffer

from constantly fluctuating magnetic field (also known as Overhauser field) caused by the nuclear spin isotopes of gallium (^{69}Ga, ^{71}Ga) and arsenide (^{75}As), each with a nuclear spin of 3/2 [76]. Their coherence times are heavily impacted from the hyperfine interaction between electronic spins and Overhauser field [77]. But, in recent years GaAs/AlGaAs based quantum dots have shown entanglement of two qubits [78] and extended the coherence time to 0.87 ms [79]. Owing to the faster gate operation time, large number of gates can be performed within the coherence keeping the GaAs/AlGaAs architecture still a promising candidate for realizing a quantum computer.

Gate defined quantum dot qubits in silicon can also be fabricated using Si/SiGe based heterostructures. There have been three experimental categories of realizing a Si/SiGe heterostructure. First is the modulation doped heterostructure [80] as shown in Figure 2.13 (a), the second is an undoped heterostructure [81, 82] as shown in Figure 2.13 (b) and the third is nanomembrane based Si/SiGe based heterostructure [83, 84] as shown in Figure 2.13 (e).

Modulation doped Si/SiGe heterostructures first realized the formation of quantum dots in 2007 using Schottky barriers [87] with electron spin readout demonstrated in 2011 [88]. Si/SiGe heterostructures grown using modulation doping have a high concentration of group V donor atoms which is a source of charge noise [80, 89]. As can be seen in Figure 2.13 (a), the phosphorus doped Si/SiGe layer is only about 20nm away from the strained Si quantum well where 2D electron system is formed at low temperatures. Charge noise arising from the donor region is critical to the stability of vertically placed 2D electron gas and has a degrading effect on

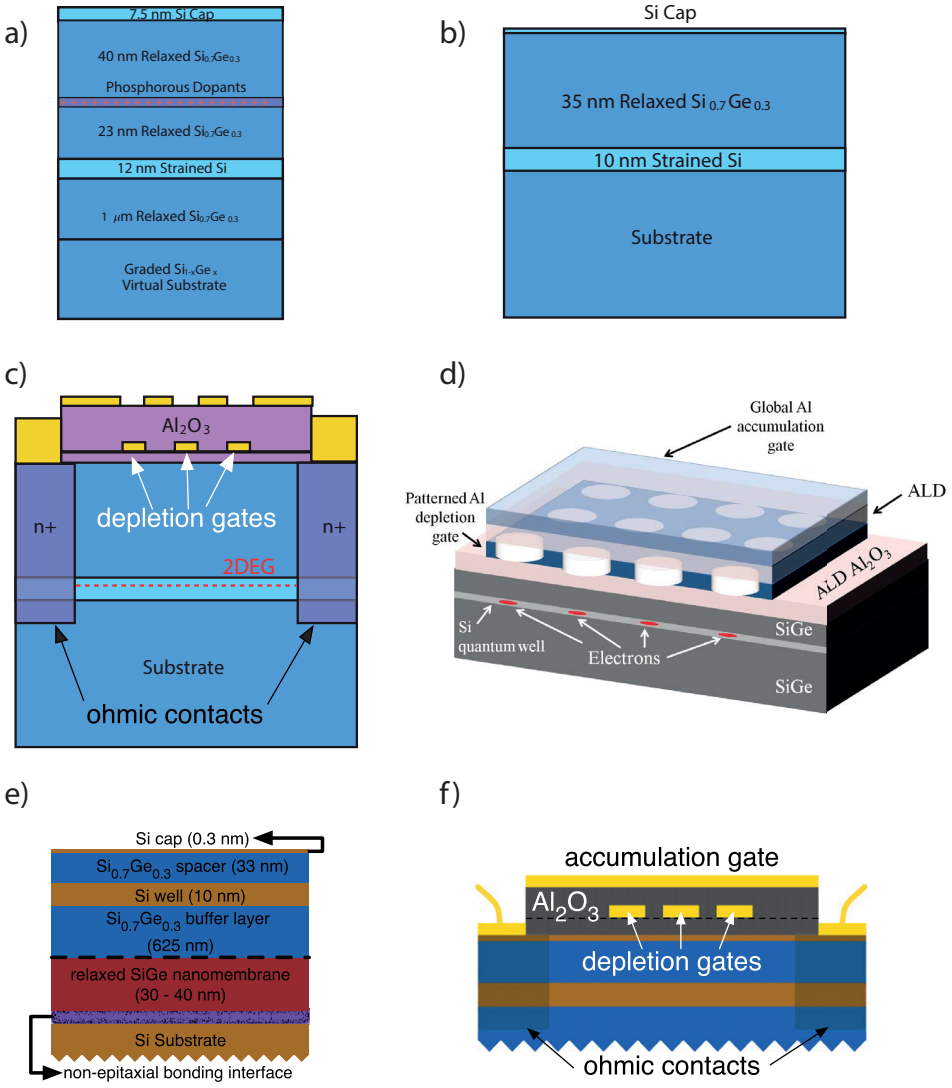

Figure 2.13: Gate defined quantum dots in silicon. (a) A typical modulation doped heterostructure [85]. b) A typical undoped heterostructure [85]. c) Schematic of the cross-section of a quantum dot device fabricated using an undoped Si/SiGe heterostructure. Depletion gates for defining gate defined quantum dots are patterned on top of Al_2O_3 grown dielectric which is deposited straight after growing the Si/SiGe heterostructure. Then, another layer of Al_2O_3 is deposited as an insulation layer between the depletion and accumulation gates which differ a lot in potential. The black solid line shows the boundary of two Al_2O_3 layers [85]. d) Schematic of a double gated undoped Si/SiGe heterostructure with circular depletion gates patterned on Al_2O_3. Additional layer of dielectric is deposited on top of depletion gates to pattern the global accumulation top gate. Red spots in the strained silicon quantum well region represent quantum dot formation by dual-gating the Si/SiGe heterostructure [86]. e) Schematic depiction of the undoped Si/SiGe heterostructure on a SiGe nanomembrane [84]. f) Schematic depiction of a cross-section of a device similar to c), but the heterostructure is grown on a SiGe nanomembrane [84].

the stable quantum dot system in the modulation doped Si/SiGe heterostructure. Additionally, the Schottky barrier formed between the metal and semiconductor was not sufficiently robust in Si/SiGe heterostructures [90]. A natural choice would be to implement higher temperature thermal oxides as dielectric for the gates, but it is not desirable for this system because it leads to strain relaxation and Ge diffusion into the strained Si quantum well [91]. Another option is to deposit an insulating gate oxide layer: generally, insulating layers deposited at lower temperature suffer from interface related defects and poor performance of the deposited oxide layers [92]. Low temperature plasma-enhanced chemical-vapor-deposition (PECVD) grown SiO_2 has relatively poor performance as well, leading to a large number of traps in the bulk oxide and at the interface between Si and SiO_2 [93]. Additionally, a slow response to the 2D electron system is observed when gating using this low quality dielectric owing to the large number of charge traps inside the SiO_2 [93].

A reduction in carrier density and mobility was reported for modulation doped Si/SiGe heterostructure upon exposure to air [94, 85]. The main cause for degradation was identified as the poor surface quality of silicon due to native oxide which results in formation of interface trap states between the semiconductor and oxide interface [94]. This effect was later reversed partially by performing a HF treatment or a forming gas anneal, but n_s and μ remain significantly lower as compared to initial measurements [94]. Thermal cycling of the samples was shown to return them to the degraded state where the carrier concentration and mobility are much lower [94]. Although, deposition of Atomic Layer Deposition (ALD) grown Al_2O_3 dielectric on modulation doped Si/SiGe heterostructure was demonstrated with negligible leak-

age current and high quality dielectric-semiconductor interface [93], an alternative undoped Si/SiGe architecture [81] was pursued owing to all the difficulties inherent in the modulation doped heterostructure for applications in quantum computing.

A typical high yield undoped Si/SiGe heterostructure is shown in Figure 2.13 (b). Without the presence of dopants to induce the conduction charge carriers, undoped heterostructures require an additional accumulation metal gate to capacitively induce charge carriers within the strained silicon quantum well. An Al_2O_3 dielectric grown using ALD was used for passivating the surface straight after the Si/SiGe heterostructure growth from CVD. A BHF dip was performed before depositing ALD grown Al_2O_3 in order to prevent any native oxide formation [85, 95]. Two sets of gates are employed to form stable quantum dot structures, namely depletion gates and accumulation gates. Depletion gates are patterned on top of ALD dielectric to confine electrons in quantum dots. Accumulation gates on the other hand are patterned on top of depletion gates with a layer of Al_2O_3 dielectric in between. A schematic of the two dual gated device architectures used in undoped Si/SiGe heterostructure is shown in Figure 2.13 (c) and 2.13 (d). In Si/SiGe the Overhauser noise is less pronounced due to presence of fewer nuclear spins. With early experimental demonstration of 2D electron systems [96], Coulomb blockade [97] and double quantum dots [82], undoped Si/SiGe architecture have demonstrated multiple designs of qubits including single spin qubit [98, 99, 100], charge qubit [101, 102, 103], singlet-triplet qubit [52], and a mixture of spin and charge qubit (called the Hybrid Qubit) [104, 105, 106]. Electron spin confined in a quantum dot patterned with a micromagnet demonstrated fault tolerant single-qubit gate fidelity of 99.6 %

[100] and coherence time of 400 μs [99]. In 2013, a charge qubit in a double quantum dot was measured with coherence time of picoseconds [102]. Two years later, a charge qubit in undoped Si/SiGe system showed coherent oscillations with a gate fidelity of 86% for standard process tomography and gate set tomography [103]. Additionally, undoped Si/SiGe heterostructure have demonstrated a new class of qubit called Hybrid Qubit combining spin and charge control of 3 electrons [53, 107]. In this architecture single qubit operations lasting 100 picoseconds were demonstrated with high gate fidelities of 85% for X and 94% for Z rotations [104] which were later improved to 93% and 96% for X and Z rotations, respectively [105].

Recently, undoped Si/SiGe based heterostrucutre were patterned on top of relaxed SiGe nanomembranes instead of graded SiGe layers because the presence of graded layers leads to misfit dislocations in a heterostructure [84]. These defects then introduce lateral strain, mosaic tilt and threading dislocations [84]. The use of Si/SiGe nanomembrane has led to a new way of confining electrons in a Si/SiGe heterostructures based quantum dots. The SiGe nanomembrane has no dislocations because it is grown below the critical thickness necessary for nucleation of misfit dislocations [84]. A typical layer sequence of undoped Si/SiGe based heterostructure grown on relaxed SiGe nanomembrane is shown in Figure 2.13 (e). The SiGe nanomembrane based approach also uses dual gated ALD dielectric architecture as shown in Figure 2.13. Using this approach formation of a high-quality and stable double quantum dots with wide inter-dot tunnel couplings without any instability caused by SiGe nanomembrane has been demonstrated [84].

A third category of gate defined quantum dots are silicon metal oxide semicon-

ductor (MOS) quantum dots. These quantum dots work similar to the conventional MOSFET device where an insulated gate controls the conductivity of the device. Si MOS quantum dots have a metallic gate fabricated on top of silicon substrate with a thin layer of thermal oxide serving as dielectric in the middle. The first demonstrations of silicon MOS quantum dot were in 2006 and 2007 where a single electron island was formed using depletion gates in a MOS transistor [108, 109]. In MOS quantum dots the two dimensional electron gas is formed at the interface of the oxide layer using potential barriers to deplete a quantum dot region using surface gates. Spin manipulation can be achieved by properly tuning the quantum dot so that it contains an extra spin 1/2 electron to realize single qubit operation. Similarly, two quantum dots can be coupled via the exchange interaction and a two qubit gate can be realized. Silicon MOS quantum dots have been successful in realizing fault tolerant single qubit operations [110] with coherence time of tens of milliseconds. Similarly, a two-qubit logic gate [111] in silicon was also realized in MOS based quantum dots for the first time using single and two-qubit operations as proposed by Loss and DiVincenzo.

2.6 Incorporating an Al_2O_3 dielectric onto STM fabricated devices

As discussed in Section 2.5, fabricating quantum dots using various semiconductor based approaches for applications in quantum computing is not a trivial task. The functionality of various quantum dot architectures is to perform electrical measure-

ments (such as spin readout, one qubit gate, two qubit gate) by using combination of gates, either patterned using Schottky barriers (for GaAs/AlGaAs and STM donor based devices) [73, 33] or by employing a multi-layered gate architecture by using a dielectric (for undoped Si/SiGe heterostructure and nanomembrane based undoped Si/SiGe heterostructure) [82, 84]. Based on the progress and encouraging results presented in Section 2.5 for adding dielectric to the Si/SiGe based heterostructures, it seems promising to investigate replacing the native oxide on STM fabricated donor devices with a ALD deposited Al_2O_3 dielectric for reproducible surface passivation and to add tunability by adding surface gates. The next section is going to introduce the principle of ALD technique and a recipe for integrating Al_2O_3 layer in the STM device fabrication.

2.7 Atomic Layer Deposition: Principles and Applications

Atomic Layer Deposition (ALD) is a Chemical Vapor Deposition (CVD) based technique where two gaseous reactants are alternatively pulsed in order to react with a solid substrate maintained at a suitable growth temperature. This process is repeated in a cyclic manner to produce thin inorganic layers with sub-monolayer thickness. This technique was independently developed in two places [7]. Firstly the less commonly acknowledged invention, occured in former Soviet Union during the 1960's by Professor Aleskovskii and colleagues where they presented their findings during a conference in 1965 and later published growth of thin films using ALD

in 1967 [112]. This technique developed in Russia was more commonly referred to as "Molecular Layering" with first experiments performed on high-surface area silicate substrates, and on single crystals to grow dielectric layers [7].

The more commonly acknowledged origin of ALD was in Finland invented by Suntola and colleagues [7]. Suntola along with his colleagues filed a patent for a technique under the name "Atomic Layer Epitaxy (ALE)" in 1974 [113]. This patent demonstrated growing ZnS using Zn/S_2, SnO_2 using Sn/O_2 and GaP using Ga/P_4 [113]. Later the same technique was used to grow thin films based on compound reactants and has led to numerous applications since the 1980's [7].

ALD since its inception has been used for variety of purposes including thin-film electroluminescent displays [114], mainstream integrated circuits (IC) applications [115], photovoltaics passivation [115], gate dielectric [115] and as catalysts to name a few. The future of ALD is not limited to the microelectronics or solar cell industry, but applications also span multiple industries as is evident by predicted 22% year over year growth in total market size for ALD based applications [115].

2.7.1 Introduction to Atomic Layer Deposition

The Atomic Layer Deposition (ALD) technique is based on sequentially dosing the substrate maintained at a particular growth temperature with precursors in gaseous form which leads to chemical reactions that are self-limiting in nature. Using ALD, conformal inorganic layers can be grown with nanometer level precision in growth direction. ALD of thin films using two precursors can be understood in these four simple steps

1. Self-terminated reaction of solid surface with the first gaseous precursor

2. Purging the unreacted precursors and gaseous by-products

3. Self-terminated reaction of the second gaseous precursor with the newly formed surface after first precursor

4. Purging the unreacted precursors and gaseous by-products

These four steps altogether make a *reaction cycle*. Steps 1,2 and 3,4 are referred to as the *half-reaction* of an ALD reaction cycle. Growth of desired material after finishing one reaction cycle is termed as Growth per cycle (GPC). GPC is different from *monolayer growth of material* per cycle which was often understood as the dominant growth mechanism during ALD growth [116, 117, 118], but is a wrong way of visualizing the whole ALD process.

One reaction cycle is schematically shown in Figure 2.14. The first step shows the reaction between the substrate surface and the gaseous precursor A. During the second step, all unreacted precursors A unable to react with the surface are purged along with the gaseous by-products generated from step 1 using an inert purging gas. In the third step, the gaseous precursor B reacts with the newly formed surface from step 2. Finally in the fourth step, the unreacted gaseous precursors and by-products after completion of the reaction from step 3 are purged. Reaction cycles are repeated until the desired thickness of material is grown.

Important parameters that are critical for growth in ALD are: the surface treatment before deposition, substrate temperature during growth, number of cycles and purge time. ALD is mainly a surface controlled process and relies on the self-

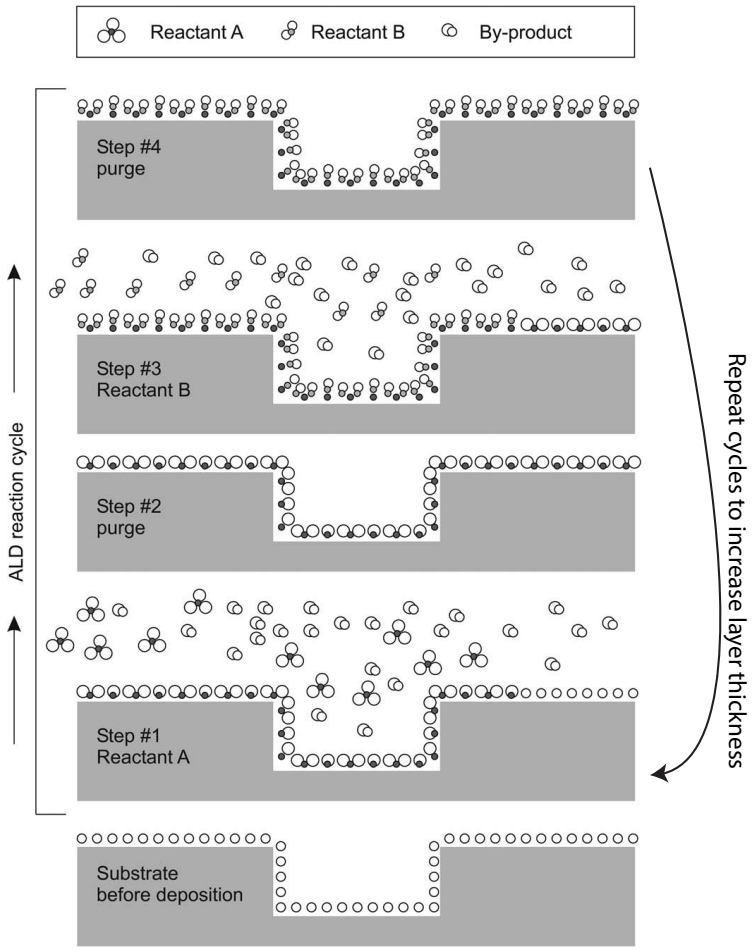

Figure 2.14: Schematic Illustration of one ALD reaction cycle. Figure adapted from [7].

terminating nature of the two half reactions as shown in Figure 2.14.

2.8 Growing Aluminum oxide (Al_2O_3) as a dielectric using ALD

One of the first experimental demonstrations that highlighted the use of ALD to grow Al_2O_3 on silicon (Si(100)) was conducted by Higashi and Fleming in 1989 at AT&T Bell Labs [119]. It was pointed in their study that using ALD to grow thin layer films was applicable to both crystalline and amorphous substrates, since the

chemistry on both would be similar. They conceived that using ALD grown Al_2O_3 layers would be useful in future generations of silicon integrated circuits. They concentrated on the use of Al_2O_3 as gate insulators and passivation layer, because this technique to grow conformal thin films at low temperature was excellent and would prevent "dopant redistribution and unwanted solid-state side reactions" [119]. They used Trimethylaluminum (TMA) and H_2O as precursors for growing Al_2O_3 on silicon substrates at temperature as low as 100 ℃ [119].

In this thesis the two precursors used are Trimethylaluminum (TMA) and H_2O because they are the most widely used precursors for growing Al_2O_3 using the ALD deposition method [7]. In the next section, the pathways through which TMA and H_2O react with a substrate to grow Al_2O_3 based on ALD are discussed.

2.8.1 Reaction pathways of Al_2O_3 growth using TMA & H_2O

The ALD reactor for depositing Aluminum oxide is a very simple apparatus consisting of a single chamber, heaters and valves which uses TMA and water as precursors which are sketched in Figure 2.15. TMA molecule consists of an aluminum atom (blue) with 3 methyl -(CH_3) (grey) groups attached, while the water molecule is depicted as oxygen (red) and hydrogen (grey). Only the aluminum and oxygen atoms will remain on the silicon surface at the end of the process.

The substrate on which the Al_2O_3 is grown is maintained at a particular growth temperature. The range of growth temperatures for Al_2O_3 varies from room temperature up to 350 ℃ with some experiments showing thin film Al_2O_3 growth at 500 ℃

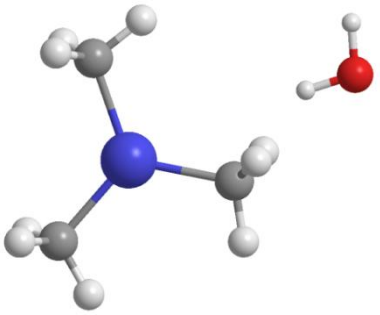

Figure 2.15: A schematic of TMA and water. Figure adapted from [120].

(using chlorine based precursors because TMA is not stable at temperature > 300 ℃ and dissociates) [121]. Growing Al_2O_3 at higher temperature impacts the growth rate and the quality of the film, which will be discussed later in Section 2.8.2. There are two different ways of operating the ALD system. In the first method, continuous flow of an inert carrier gas (N_2 in this case) is maintained with precursors (TMA & H_2O) cyclically injected in the gas stream whilst pumping the system continuously [120]. Alternatively, the precursors are pulsed in alternating steps and the system is purged with inert gas in between the precursor steps. The reactor that is used to grow thin films ALD layers in this thesis is a Savannah S200 by Cambridge Nanotech (Figure 2.16 (a)). Throughout this thesis the layers are deposited using the first method where TMA and H_2O are pulsed in alternating steps with N_2 purge in between. The base pressure of the system during Al_2O_3 growth is maintained at 0.26 Torr. A typical pressure profile inside the chamber during Al_2O_3 growth is shown in Figure 2.16 (b) showing the peak pressure inside the system at the time of TMA and H_2O pulses (duration of 0.015 s). The purge time between the precursor steps is 8 seconds, long enough to ensure that the system has pumped out all the by-products and unreacted precursors the from previous step removed, before pulsing the second precursor. If the purge time is too short, then the GPC increases

as both the precursors are present in gaseous phase simultaneously which leads to uncontrolled CVD type growth [122, 123].

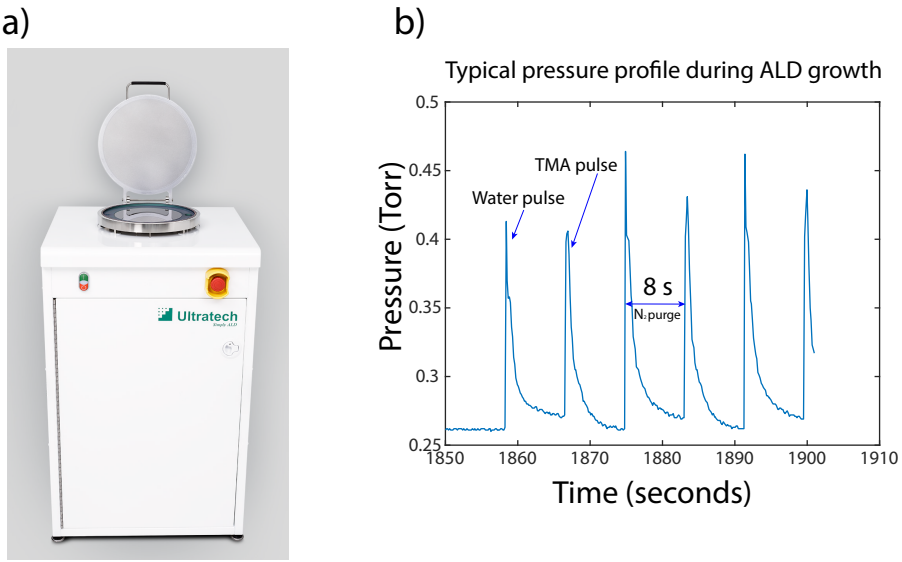

Figure 2.16: a) ALD reactor Savannah S200 by Cambridge Nanotech. Figure adapted from [120]. b) A typical pressure profile during growth of ALD based Al_2O_3 using TMA and H_2O as precursors. Purge time during the run is set to 8 seconds using N_2 gas. Base pressure during growth is 0.26 Torr.

The growth of Al_2O_3 using TMA and water is considered ideal for an ALD type processes because: (1) the reactants are highly reactive but are also thermally stable, and (2) most importantly the gaseous by-product, methane does not seem to interfere with growth [7]. The process of growing Al_2O_3 using TMA and water follows the overall stoichiometry presented below:

$$2Al(CH_3)_3(g) + 3H_2O(g) \rightarrow Al_2O_3(s) + 6CH_4(g) \tag{2.13}$$

The surface chemistry involved in this process is described using two successive

half reactions that are as follows:

$$||\mathrm{Al{-}OH} + \mathrm{Al(CH_3)_3}(g) \rightarrow ||\mathrm{Al{-}O{-}Al(CH_3)_2} + \mathrm{CH_4(g)} \tag{2.14}$$

$$||\mathrm{Al{-}CH_3} + \mathrm{H_2O}(g) \rightarrow ||\mathrm{Al{-}OH} + \mathrm{CH_4}(g) \tag{2.15}$$

The process is much more complicated at the beginning of the growth than it is shown using reaction 3.1-3.3. Depending on the surface treatment before growth (such as a HF treatment for silicon sample), deposition of Al_2O_3 during the first few cycles undergoes distinct initiation mechanisms which will be discussed later in Section 2.8.2. It is only after the first few cycles that the surface reaches a maximum number of sites available for incoming TMA molecules to bind during each reaction cycle. Only then the process is correctly identified by half-reactions 3.2 & 3.3. Moreover, it is evident from these two half reactions that the surface switches from methyl-terminated to hydroxyl-terminated and vice versa leading to Al_2O_3 growth.

Parameters used to grow Al_2O_3 thin films using ALD in this thesis are shown in Table 2.1. These include dose rates for TMA and H_2O, temperature of the substrate, number of cycles (always the same unless otherwise mentioned) and carrier gas flow rate.

Parameters used for growing Al_2O_3 using ALD		
TMA	Dose = 0.8 mg/pulse	Pulse time = 0.015 sec
H_2O	Dose = 0.7 mg/pulse	Pulse time = 0.015 sec
Carrier gas N_2	Flow = 20 sccm	Purge time = 8 seconds
Temperature	200 ℃	
Cycles	250 (unless otherwise mentioned)	

Table 2.1: Recipe parameters used to grow Al_2O_3 using ALD at ANFF, UNSW for this thesis.

2.8.2 Additional aspects of growing Al_2O_3 using TMA and H_2O

The parameters mentioned in Table 2.1 for growing ALD based Al_2O_3 have an influence on the nature of oxide grown and the reaction chemistry. Moreover, the surface treatment prior to growth also affects the film quality and alters the reaction chemistry. In this section, the influence of the growth parameters along with surface treatment will be discussed with relevance to growing Al_2O_3 on the silicon substrates. Extensive review of these parameters can be found in [7].

2.8.2.1 Surface treatment before ALD and number of cycles

ALD is a surface limited process where material is deposited with each reaction cycle and this is quantified using GPC. When the precursors are pulsed into the chamber for the first time, they encounter the bare substrate (hydrogen terminated silicon in this thesis) where the deposition will begin. Initially, during the first few cycles,

the precursors witness the growth surface changing constantly until the surface is covered only with ALD grown material.

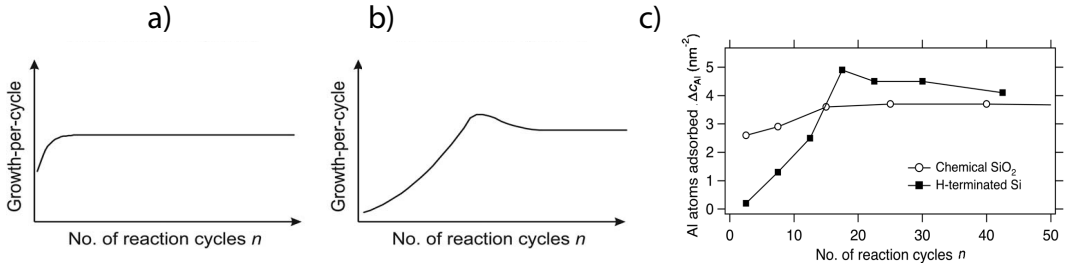

Figure 2.17: a) Dependency of the GPC on the number of reaction cycles showing substrate-inhibited type-1 growth. b) Dependency of the GPC on the number of cycles showing substrate-inhibited type-2 growth. c) Experimental confirmation of substrate-inhibited type-1 and type-2 growth mechanism observed in silicon surface covered with SiO_2 and hydrogen terminated silicon surface, respectively. Figure adapted from [7].

For the first few cycles of Al_2O_3 deposition using TMA and H_2O on silicon, there are two growth mechanism dominating the surface chemistry. These are substrate-inhibited type-1 growth (Figure 2.17 (a)) and substrate-inhibited type-2 growth (Figure 2.17 (b)) [7]. In both these cases GPC is initially lower in the first few cycles due to lower number of reactive sites available for TMA molecules to bind. Then GPC reaches a maximum and stays constant for type-1 growth whereas in type-2 growth GPC reaches a maximum before settling down for a constant GPC as a result of Al_2O_3 formation (thereby providing equal reactive sites for precursors in every subsequent reaction cycle). Using a silicon substrate with a SiO_2 layer present before deposition, substrate-inhibited type-1 growth is observed experimentally as shown in Figure 2.17 (c) [124]. Whereas, hydrogen terminated silicon surface exhibits substrate-inhibited type-2 growth as shown in Figure 2.17 (c) [125]. ALD layer growth in a substrate-inhibited type-2 mode happens as a result of Al_2O_3 island formation where TMA molecules bind with defects in the hydrogen terminated silicon

surface as shown in Figure 2.18 [125]. These Al_2O_3 islands then further catalyze the oxidation process of hydrogen terminated silicon to form reactive SiO_x species [125]. The presence of Al_2O_3 islands and reactive SiO_x species explains the reason for initial increase in the GPC observed for the hydrogen terminated silicon surface, which later becomes constant as a constant number of reactive sites are available due to Al_2O_3 deposition. However, the saturation thickness of SiO_x is found to be 0.15 nm [125].

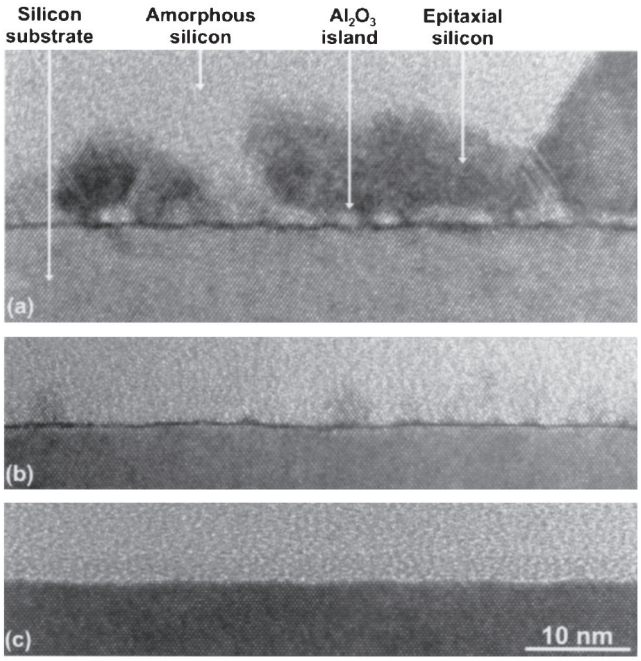

Figure 2.18: Cross-sectional Transmission Electron Microscope image for Al_2O_3 deposited on hydrogen terminated silicon at 300 °C showing three cases. a) 15 reaction cycles, b) 20 reaction cycles, and c) 30 reaction cycles. All the grown layers were then capped *in situ* silicon. Figure adapted from [125].

In this thesis all the ALD grown Al_2O_3 is deposited on hydrogen terminated silicon because the presence of native oxide on silicon is a dominant source of trap charges and low frequency noise which is deemed undesirable for quantum computing applications [69]. Prior to deposition, a 1:10 HF dip is performed on the silicon

substrate for 30 seconds followed by a 30 seconds rinse in DI water. The silicon surface is then blow dried using N_2 and transferred in a petri dish (within <1 minute) to be loaded into the chamber of the S200 system for ALD deposition. Performing the HF dip treatment and swift loading of sample in a closed container (such as a petri-dish) prior to deposition ensures a hydrogen terminated surface with <1Å growth of native oxide as shown by Okeda [126].

As can be seen from Figure 2.17 (c) and Figure 2.18 ALD deposition on hydrogen terminated silicon surface exhibits constant growth after first 25-30 cycles. However, the total number of cycles for depositing Al_2O_3 in this thesis is 250 which is much greater than 25-30 cycles ensuring that the growth of deposited Al_2O_3 is uniform.

2.8.2.2 Al_2O_3 growth temperature

ALD deposition during growth progresses when the incoming gaseous precursor molecules attach to the reactive surface OH groups. The main reaction mechanism is through ligand exchange where the methyl group in the TMA molecule react with -OH bond and methane is released. The reaction is then self-terminated due to steric hindrance from the methyl groups. Therefore, the concentration of surface OH group has an affect on the number of adsorbed species [7]. With higher deposition temperatures, the concentration of surface OH groups reduce and it is exactly this mechanism which is accounts for the decrease in the GPC at higher temperatures, as observed experimentally and shown in Figure 2.19.

In this thesis, all the ALD layers of Al_2O_3 are deposited on silicon substrate maintained at a temperature of 200 ℃. This temperature provides maximum OH surface concentration available and also compatibility with STM fabricated devices.

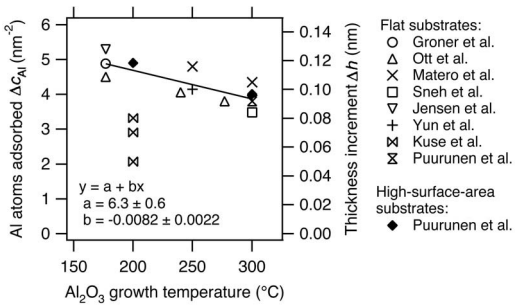

Figure 2.19: GPC in the ALD growth of aluminum oxide in steady growth regime. Figure adapted form [7].

It is also worth noting that during the cleanroom processing of the STM fabricated devices, the silicon wafer piece will be baked at 180 ℃ after Al_2O_3 deposition to harden the resist mask for EBL. Utilizing an Al_2O_3 growth temperature that is higher than the normal processing temperature is beneficial as extra heating of the grown ALD layer at a temperature lower than the deposition temperature should not have any effect the integrity of the thin film.

2.8.2.3 Impact of purge time

A sufficient dose of TMA and H_2O is necessary for saturating the surface, meaning that the pulse time has to be sufficiently long. Additionally, for the integrity of the ALD process the purge time must also be sufficiently long in order to pump all the unreacted species and by-products formed in the reaction chamber. If the purge time is too short, then the two gaseous precursors are simultaneously present in the chamber and the GPC increases leading to a CVD type growth with uncontrolled final thickness. The purge time used in between the precursors for Al_2O_3 layers grown using ALD in this thesis is 8 seconds. A pressure profile of the chamber

during a reaction cycle in Figure 2.16 (b) shows that during the purge time the chamber pressure comes back to the base pressure. This indicates that all the reactive molecules in the gas phase have been pumped out of the chamber leading to a true ALD process.

2.8.2.4 Impact of TMA & H_2O dose rates

One of the principle requirements of the ALD based process is the self-termination of the half reactions where precursors saturate the growth surface by adsorbing to the reactive sites. Chemisorption of the precursors binding to the reactive sites must be quick (compared to the pulse time) and complete (saturating the surface) [127]. There is no exact dose rate that is needed if these requirements are met for thin film growth. The S200 system used here is designed for depositing ALD layers on substrate as large as 200 mm for which uniform growth is specified and guaranteed. In contrast, the biggest sample used in this thesis for depositing Al_2O_3 using ALD is a 8 mm square chip which implies that the pulse times mentioned in Table 2.1 are more than enough to ensure the surface is saturated with gaseous precursors.

2.9 Characterization of Aluminum Oxide grown using ALD

After successfully growing thin films of Al_2O_3 using ALD, characterization of the grown oxide is necessary to reproduce thin films of similar thickness and material properties. For a thickness measurement of grown films, the ellipsometer is used.

2.9.1 Ellipsometry to measure thickness of ALD deposited Al_2O_3 layers

Ellipsometry is an optical technique that measures the change in the polarization of an incident light beam as it reflects from the surface of a material with the basic measurement principle depicted in Figure 2.20. The observed change in the polarization can be measured as an amplitude ratio Ψ and the phase difference $\triangle$ [128]. The change in the polarization depends on the thickness and optical properties of the material being measured.

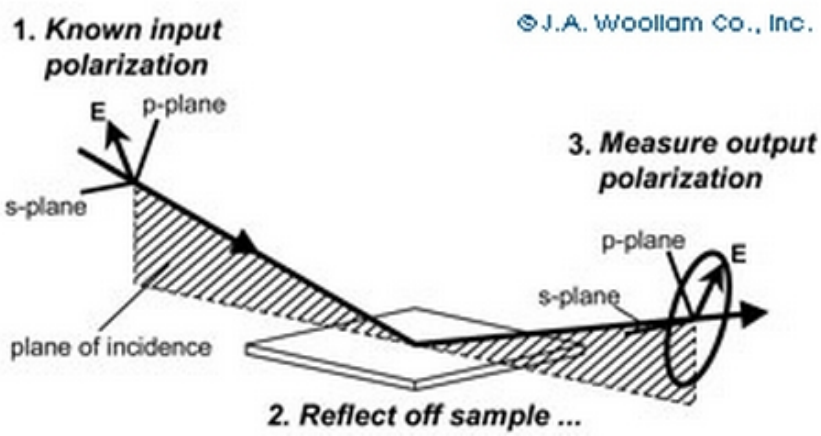

Figure 2.20: Schematic of Ellipsometry process [128]

The ellipsometer consists of a HeNe Laser (632.8 nm), a polarization generator, polarization analyzer and a detector. The polarization generator and analyzer are constructed from polarizers, compensators and phase modulators [128]. The incoming beam consisting of an unpolarized light is sent through the polarizer and light with a preferred electric field orientation is allowed to pass. This linearly polarized light reflects from the sample surface and becomes elliptically polarized before passing through the continually rotating analyzer [128]. The detector finally con-

verts the light into an electronic signal to quantify the reflected polarization which is compared with the input polarization to determine the change caused by the sample.

Ellipsometer used here can only determine the thickness of the deposited oxide by using a model and physical parameters such as dielectric constant and refractive index. However, it should be noted that using this technique to determine thickness of the ALD dielectric does not provide any meaningful information about the interface between silicon and Al_2O_3 or give a precise thickness of the native oxide formation. For all the Al_2O_3 ALD dielectric deposited on silicon in this thesis, a 0.15 nm of SiO_2 is assumed [125] in the model.

In summary, this chapter introduces the steps involved in fabricating the Si:P devices in the UHV using the STM along with their transport properties. Additionally, gate defined quantum dots that incorporate surface gates using a dielectric are also discussed. Lastly, the ALD process is explained for depositing Al_2O_3 dielectric on Si:P devices.

Chapter 3

Integration of a top gate on a Al_2O_3 dielectric

3.1 Reproducible ALD deposited Al_2O_3 layers

All the Al_2O_3 dielectric films used in this thesis were grown using the recipe as discussed in Table 2.1 using TMA and H_2O as precursors with 250 reaction cycles and a substrate temperature of 200 ℃. The thickness of these films is given by the number of cycles as outlined in Section 2.8 and verified using ellipsometry. An example of the device structure used for the ellipsometer calculation is shown in Figure 3.1 (a) together with the model parameters. Although the native oxide on the silicon surface is etched before the ALD deposition, a small interface layer of SiO_2, roughly 0.15 nm remains [125] which is incorporated in the model. The ellipsometer measures the changes in polarization and amplitude of an incident laser beam of known polarization (as outlined in Section 2.9) and therefore relies on model parameters to

convert these observables into dielectric properties and film thicknesses. An example of experimentally obtained results for a 28 nm of Al_2O_3 grown on top of a silicon surface at 200 ℃ for three different angles of the incident laser beam (55°, 65° and 75°) are displayed in Figure 3.1 (b). The amplitude ψ and phase $\triangle$, of the polarized light are the output parameters extracted after performing a ellipsometry measurement and describe the change in the polarization of the incident beam (containing electric field in both p and s polarization) when it interacts with the substrate containing thin film [128]. The substrate can distinctively separate p and s polarized light, thereby causing a change in the polarization. This is expressed using the relation that has both amplitude (ψ) and phase ($\triangle$), $tan(\psi)e^{i\triangle} = \frac{r_p}{r_s}$ [128]. Figure 3.1 (a) also shows the fitted model curves (black lines) with the refractive index and the thickness of the deposited ALD layer as the only free parameters. Very good agreement is found between the model fit and the experimentally obtained data which is quantified by MSE (mean square error).

Exemplary results for 5 different layers of Al_2O_3 are shown in Table 3.1. Determining the precise thickness of the grown ALD layer via ellipsometry is crucial to the fabrication strategy because it primarily signifies reproducible ALD growth (for example, with leaky valves, one would obtain CVD type growth with a strong discrepancy to the expected layer thickness given by the number of reaction cycles). It is also vital in optimizing the dose rate needed for EBL and for etching the deposited Al_2O_3 with high accuracy, i.e. with minimal undercut. Generally the grown dielectric films are very reproducible, with the strongest deviation from the mean also with the largest uncertainty (quantified by MSE) e.g. Mean: (28.570 ± 0.17)

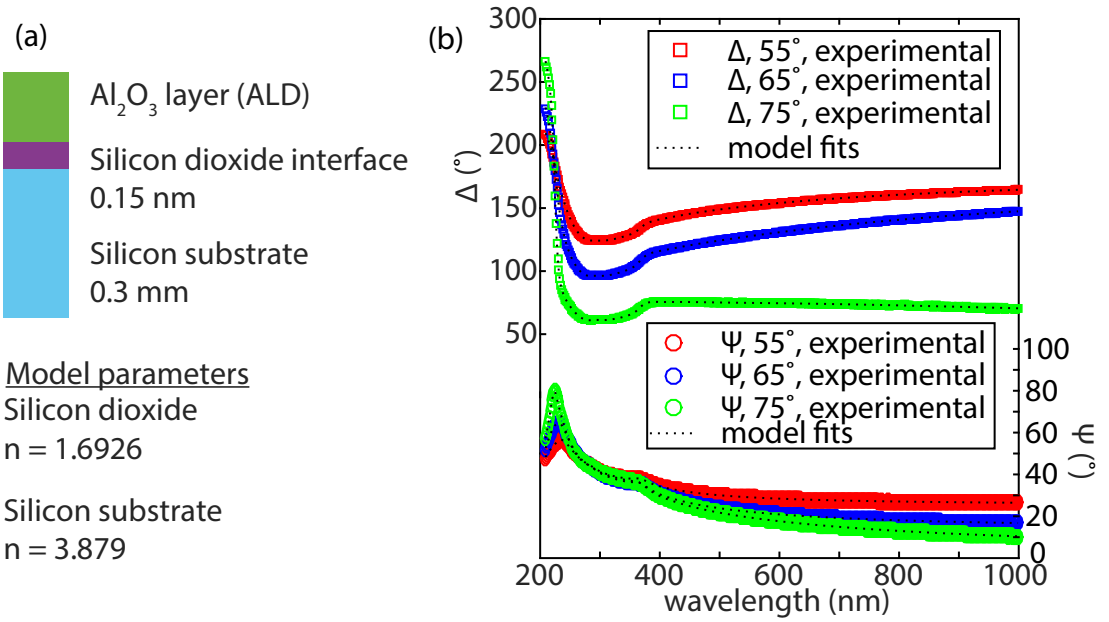

Figure 3.1: Ellipsometry measurements of Al_2O_3 layers. (a) Layered model of deposited thin film on bare silicon substrate. b) Data obtained from the ellipsometer after spectroscopy performed at 55 °, 65° and 75 °. Plot shows ψ and $\triangle$ plotted for different detection wavelengths.

nm (1 σ standard uncertainty of the mean). The GPC obtained here is 28.57 nm / 250 cycles = 0.1143 nm/cycle and this compares very well with both the manufacturer's specification of 0.111 nm/cycle for the growth conditions used [120] and literature values for 200 ℃ growth [7].

Thickness of ALD films on a silicon substrate with HF dip before deposition			
Number	ALD thickness (in nm)	Refractive Index	MSE
1	28.920	1.6566	5.368
2	28.274	1.6593	5.844
3	28.081	1.6583	7.116
4	28.866	1.6515	4.299
5	28.710	1.6594	4.797

Table 3.1: Thickness measurements of an ALD grown Al_2O_3 on a silicon substrate using ellipsometry considering 0.15 nm of SiO_2 formation during the initial ALD deposition phase. The refractive index value is calculated for the detection wavelength of 632 nm.

3.2 Integrating ALD deposited Al_2O_3 into STM fabricated devices

The precision donor fabrication scheme involves STM lithography on a hydrogen terminated silicon surface to pattern quantum nanostructures followed by phosphine dosing and an incorporation anneal at 350 ℃. A low temperature (250 ℃) epitaxial silicon is grown over the incorporated donor atoms and then *ex-situ* processing is performed to establish ohmic contacts to the buried STM-patterned nanostructures as discussed in Section 2.4. A schematic of a three-terminal device patterned in STM is shown in Figure 3.2 (a). Fabricating nanostructures in STM consists of patterning an inner device structure (tens-few hundred nanometers long) and patterning extension leads (few microns long) which terminate with a contact patch for integration with the ohmic contacts. The aim of introducing the dielectric layer is to mask the inner device structures with the dielectric as shown by the green box in Figure 3.2 (a). An etch mask is then defined to expose the contact patches of the STM fabricated device and make them accessible for depositing metal to form electrical contact leads. A cross-section schematic of a STM patterned device is shown in Figure 3.2 (b) with encapsulated silicon and native oxide present over the patterned planar nanostructures. Successful application of a dielectric layer of Al_2O_3 on a STM fabricated donor devices involves modifying the existing recipe for *ex-situ* processing.

Figure 3.2 (c) shows the step by step procedure for integrating ALD deposited Al_2O_3. First, a 30 s dip is performed in HF 1:10 solution for removing any native

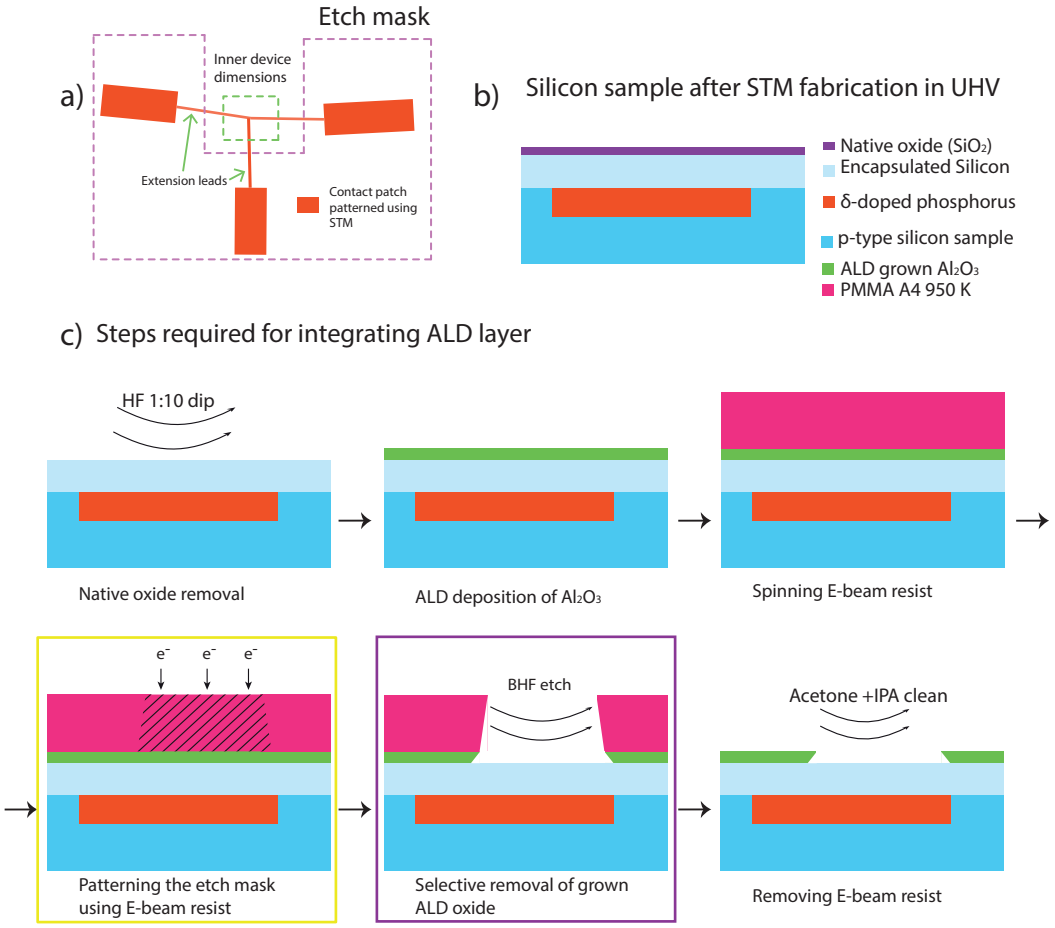

Figure 3.2: Strategy for integrating an ALD deposited dielectric onto STM fabricated devices. a) Schematic of a 3 terminal device patterned using STM. Box marked in dashed green line shows the inner device dimensions that span tens-hundred of nm. Extension leads patterned in STM devices are a few microns long. The device terminates with a contact patch used for *ex-situ* processing. Larger box marked with dashed pink line shows the etch mask used for masking critical device structures. b) Cross section schematic showing a silicon sample containing STM patterned planar-doped nanostructure after complete device fabrication in the UHV. c) Steps required for etching the grown ALD dielectric. First a BHF dip is performed and then ALD dielectric is deposited. PMMA resist is spin coated on the silicon sample with the dielectric and an etch mask is defined using the optimum dose rate. The etch mask is then removed using an appropriate etch solution that prevents undercut within the tolerance required for STM fabricated devices. The resist mask is removed finally using Acetone to continue standard cleanroom processing to establish ohmic contact to δ-doped nanostructures patterned using STM. Yellow and purple boxes indicate the two critical steps in integrating an ALD deposited dielectric: determining the optimal dose rate and calculating the precise etching rate for the dielectric.

oxide that is present on the sample followed by a 30 s DI water rinse. The sample is then blow dried using N_2 and transferred in a petri dish to the ALD reactor,

thereby minimizing any native oxide formation. The recipe shown in Table 2.1 is then followed to deposit Al_2O_3 dielectric onto the silicon substrate. Due to the presence of this additional Al_2O_3 layer of dielectric on the STM fabricated device, standard *ex-situ* cleanroom processing in terms of etching holes in order to contact the buried phosphorus layer as mentioned in Section 2.4 cannot be implemented. Here the ALD layer is quite robust to the RIE etch used to create holes and is often actually used as a RIE etch mask in processing silicon based devices [129]. Therefore the Al_2O_3 needs to be etched over the contact patches allowing access to use RIE to contact the buried Si:P pattern whilst still masking the inner device structure. Etching Al_2O_3 is a subtractive process and involves patterning an etch mask using EBL that protects the critical device structures but exposes the contact patches as shown in Figure 3.2 (c). After removing the ALD layer over the contact patches by wet etching, the buried phosphorus contact patches are only encapsulated with silicon and standard cleanroom processing as discussed in Section 2.4 can now be performed. Two critical steps which are essential for reproducibly etching Al_2O_3 are: (i) determining the optimal dose rate involved during the EBL exposure (shown in yellow box in Figure 3.2 (c)) to define the masked pattern protecting the inner device structures with high precision, and (ii) to establish a robust etch recipe (shown in purple box in Figure 3.2 (c)) that can remove Al_2O_3 selectively with a very low undercut, preferably 0.5 μm or less. This requirement becomes apparent from Figure 3.2 (a): because the extension leads patterned in the STM hydrogen lithography are typically $\sim$ 2 microns long and therefore, if the undercut is greater than 0.5 μm, there is a risk that the Al_2O_3 layer protecting the inner device dimensions gets etched

as well. This requirement is only weak though, since longer extension leads (> 1 μm) can always be fabricated in the STM.

3.3 Patterning Al_2O_3 to access buried nanostructures

In conventional cleanroom processing of the STM fabricated devices robust recipes are used to establish ohmic contacts with patterned nanostructures embedded in the silicon crystal. During this process, EBL for example is used to pattern ohmic contacts with a dose rate of 350 $\mu C/cm^2$. However, with the introduction of the dielectric over the silicon substrate, a new dose rate for patterning the resist over the dielectric needs to be determined (as shown in the yellow box in Figure 3.2 (c)). This is because the type of substrate used now contains an insulating dielectric and its electrical properties will change the optimal dose rate used to define patterns with the same dimensions. To determine the optimal dose rate, a dose test was conducted on a standard silicon wafer with the ALD grown Al_2O_3 of the same thickness as mentioned in Table 3.1. During a dose test, the exposure dose is continuously varied over a suitable range from: underdosed to overdosed. An exposure is classified as underdosed if the electron beam is too weak to break all polymer chains of the resist in the exposure pattern, resulting in structures being smaller than defined after development. On the contrary if the beam is too strong, overdosed structures are produced as a result of excess exposure from the electron beam creating a pattern that has its boundaries stretched. In between, there is range of optimal parameter

settings resulting in a well defined exposure pattern, the optimal dose. The test pattern chosen for this dose test is shown in Figure 3.3 and consists of structures that can provide useful information in determining the optimal dose rate: these are Koch snowflake fractal and maze patterns. Figure 3.3 (a) shows Koch snowflake fractal patterns of different levels which are used in performing a coarse analysis for establishing the optimum dose rate. However, a finer statistical analysis is performed on the pattern shown in Figure 3.3 (b) that consists of a maze with linespacing and linewidth of 300 nm. For this dose test, PMMA A4, 950K is used as a resist which will also be used later as a etch mask.

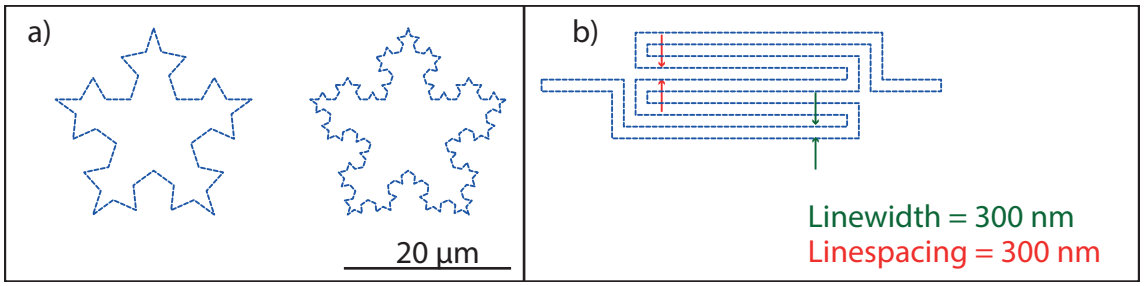

Figure 3.3: Dose test pattern used for Al_2O_3 deposited using ALD. a) Koch snowflake fractal pattern used for performing the dose test. b) Finer maze pattern used for dose test. Green arrows gives the linewidth and the red arrows indicate the linespacing used in the patter, with both equaling 300 nm.

First, a silicon wafer with ALD grown Al_2O_3 (using the recipe from Table 2.1) was cleaned with acetone and IPA before spin coating PMMA at 3000 rpm/second for 60 seconds. The sample is then baked at 180 ℃ for 10 minutes. This treatment gives a total PMMA thickness of ∼250 nm. The bake time is larger here because this will enhance the PMMA's resistance during the wet etch. Subsequently, the sample is loaded in the SEM to define the patterns shown in Figure 3.3 for a wide range of dose values (varying from 100-460 $\mu C/cm^2$). After EBL, the sample is taken out of the SEM and developed using MIBK and IPA for 40 seconds and 20 seconds,

respectively. In order to determine the effectiveness of the dose test, the developed pattern must be analyzed for the highest resolution that can be achieved using the SEM. However, the sample with developed resist mask cannot be imaged directly under the SEM, as imaging would further expose the resist mask. Therefore, in order to analyze the dose test under the SEM, 80 nm of aluminum was deposited to protect the developed resist mask. No lift-off of the aluminum was performed since this way the patterns in the SEM can be analyzed independently of (potential) issues with lift-off.

Figure 3.4 (a) (1-4) shows four extraordinary results of the Koch snowflake fractal patterns for varying dose values, all at the same magnification. The Figure 3.4 (a) (1) shows the situation when the defined pattern was under dosed (130 μC/cm^2) because the snowflake is not defined properly yet with its lateral dimensions significantly smaller than specified in the pattern and edges not sharply defined. In Figure 3.4 (a) (2) the snowflake pattern is well defined with sharp edges nicely resembling the test pattern shown in Figure 3.3 (a) for an optimal dose value of 235 μC/cm^2. This image also shows the advantage of using fractals for performing dose tests: while the edges provide the information about how close the chosen dose rate is to the optimum, the usage of strongly varying feature sizes allows to deduce the resolution of the lithography as well. In this case, the resolution probed with the finest fractal pattern is given by the length of the line segments which in this case is 700 nm for Figure 3.4 (a) (2). The image in Figure 3.4 (a) (3) shows the snowflake pattern for the dose value used for metallization of ohmic contacts in processing STM devices without a Al_2O_3 dielectric. The overexposure of this pattern (as can be seen in

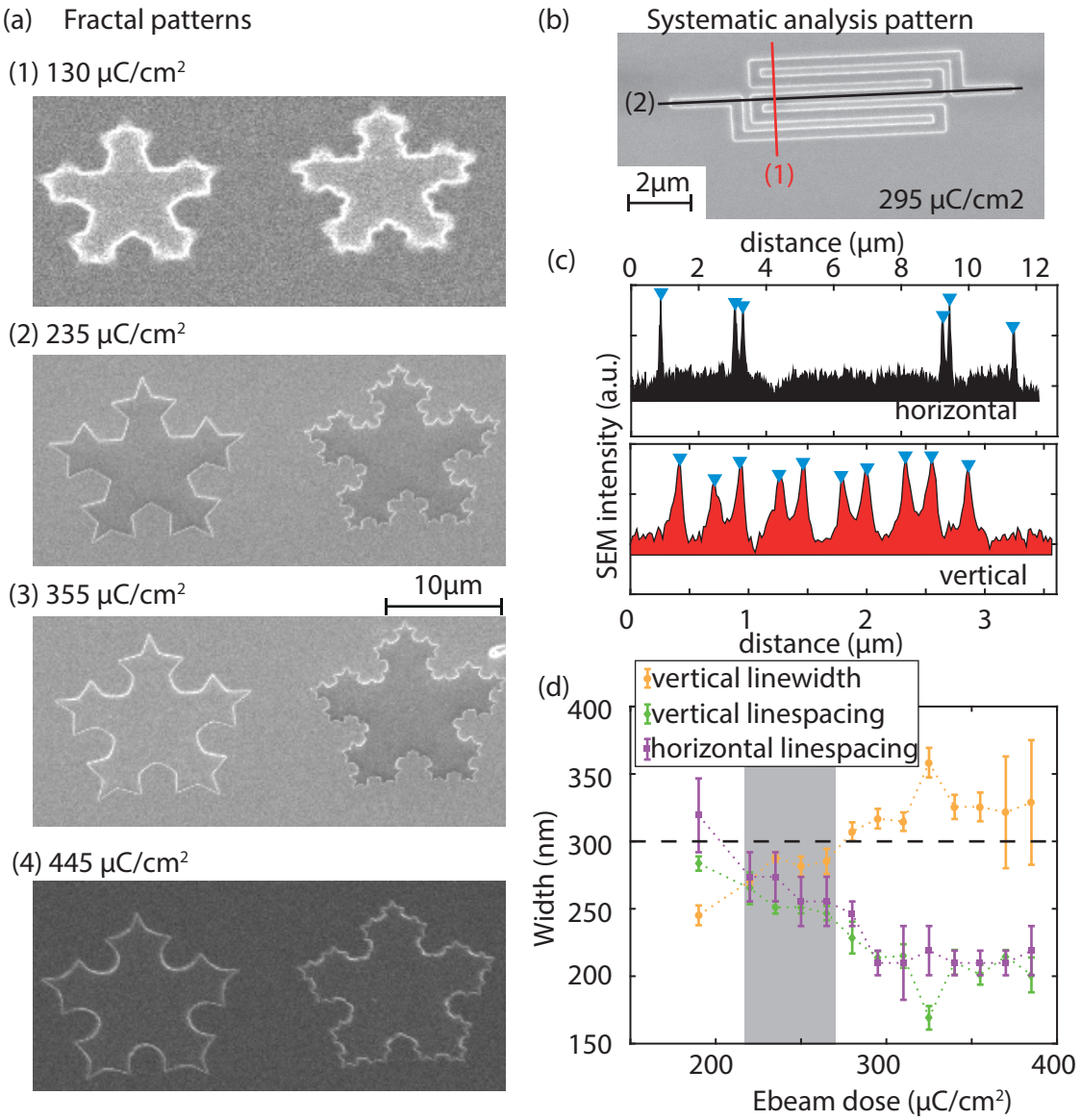

Figure 3.4: Dose pattern analysis. a) SEM image of fractal pattern for dose value of 1) 130 μC/cm^2, 2) 235 μC/cm^2, 3) 355 μC/cm^2 and 4) 445 μC/cm^2 that represent under dosed (as in 1)), optimal dosed (as in 2)) and over dosed cases (as in 3) & 4)), respectively. b) SEM image of the finer maze pattern with line spacing of 300 nm for dose value of 295 μC/cm^2. Two line cuts are taken for statistical analysis: horizontal and vertical, along which the boundaries between the dosed and undosed regions are determined and linespacing and linewidth are calculated. c) Exemplary line profiles for the horizontal and vertical cut in b) shown using black and red respectively. Blue triangles symbolize peaks identified using automated data evaluation in MATLAB. Separation of peaks together with the knowledge of the pattern allows to then determine the linespacing and linewidth. d) Line spacing of the finer maze pattern shown in b) is calculated using the horizontal and vertical profile analysis for different dose values. Grey shaded region shows the region of optimal dose. Error bars correspond to 1σ standard uncertainty of the mean values.

the slightly rounded edges of the left fractal) justifies the necessity for conducting a dose test, because the dose value that works on silicon gives slightly over-dosed images for ALD deposited Al_2O_3 due to the difference in the underlying surface. Lastly, in Figure 3.4 (a) (4) the pattern with a dose value of 445 $\mu C/cm^2$ is shown and as expected, the pattern looks heavily overdosed. To determine the quality of lithography the test pattern shown in Figure 3.3 (b) is used as a benchmark with a primary focus on the linespacing and linewidth of the maze pattern with a target spacing of 300 nm each. For statistical analysis, two line cuts are taken along the vertical and horizontal axis of the maze pattern to determine the type of dose by measuring the width of the exposed areas in the resist mask (linewidth) to the unexposed areas in the resist mask (linespacing). This analysis should yield a similar width for both exposed and the unexposed areas in the resist mask under the condition of an optimal dose. Figure 3.4 (c) shows an exemplary analysis performed for a dose value of 295 $\mu C/cm^2$ along the vertical and the horizontal cuts marked by the red and black lines in Figure 3.4 (b), respectively. In Figure 3.4 (c), the line profiles are analyzed by measuring the distance between the peaks representing the boundaries of the exposed and the unexposed areas in the resist mask. In the SEM image, these boundaries show up as bright lines, which correspond to peaks in the line profiles. Therefore, a MATLAB program to automatically determine these peaks was used (result is shown using blue triangles in Figure 3.4 (c)) and their spacing was calculated. In order to determine the optimum dose rate, this analysis was performed for different dose values and the plot showing the vertical linewidth, the vertical linespacing and the horizontal linespacing is given in Figure 3.4 (d). For

lowest dose values the linespacing is larger than the linewidth, clearly reproducing the situation observed for the Koch snowflake pattern in Figure 3.4 (a) (1), whereas for the higher dose values the linespacing is significantly decreased and the linewidth is strongly increased, similar to Figure 3.4 (a) (3) and (4). The optimal dose region in Figure 3.4 (d) is shown using grey where the linewidth and linespacing are similar as depicted in Figure 3.4 (a) (4). Following this depiction, the uncertainty in the analysis of the optimum dose value is reduced since the absolute values contain significant errors due to the limited resolution of the SEM images. This in turn explains the discrepancy between the region of equal linewith and linespacing to the targeted 300 nm (indicated using a dashed black line in Figure 3.4 (d)). After conducting the dose test, an optimal range of dose values between 220-250 $\mu C/cm^2$ was established for patterning ALD grown Al_2O_3 layers on silicon.

3.4 Etching ALD grown Al_2O_3 layers

After patterning the resist mask on the ALD deposited Al_2O_3 layers using an optimal dose value, the next step in the process before standard cleanroom processing of STM-patterned devices is etching the grown Al_2O_3 layer (as shown by purple box in Figure 3.2 (c)), thereby transferring the resist mask into the ALD layer. This can be achieved in two ways: dry etching or wet etching. Major parameters to be considered for choosing either of the two methods are the etch rate, the etch profile, the selectivity of the material to be etched (versus the mask) and the ability to self terminate once the material is fully etched and the substrate is exposed.

Dry etching is the process of removing material from a masked substrate by

bombarding high kinetic energy particles or ions that remove the material from the exposed surface. Dry etching can be either in the form of a physical etch, chemical etch or typically a combination of both. A major drawback of using a physical bombardment strategy is that the mask is similarly etched away in the process, that means the mask's thickness has to be chosen such that the desired material etches away before the mask is fully etched. Dry chemical etching has advantages in terms of being mostly anisotropic with very good selectivity for etched material, thereby having less undercut. Undercut is defined as the extra material that is etched away outside the pattern and the aim is always to reduce undercut during an etching process.

Dry Etching in the case of Al_2O_3 could only be done by physical bombardment of heavy ions as there are no suitable chemical etching agents available within ANFF facility at UNSW [130]. The main reagents used are halogen based molecules which are used in conjunction with inert gases. Since most dry etching recipes are not highly selective for aluminum oxide over silicon, they are not self-terminating in nature. Thus, dry etching will also start etching the silicon substrate, potentially harming the phosphorus nanostructures underneath.

Therefore, the etching method of choice within the ANFF facilities is a wet etch of the grown oxide layer. Wet etching is the process of removing material from a wafer using liquid chemicals or etchants. Wet etching can be highly selective, such as in case of tetramethylammonium hydroxide (TMAH) which is used for etching Si in (100) crystal plane alone, or in the case of Buffered Hydrogen Fluoride (BHF) which is used for removing native oxide on top of silicon leaving silicon unharmed,

thus providing a self-terminating etch.

Generally, wet etching in case of Al_2O_3 is carried out by introducing the sample surface containing the oxide in an acidic solution (mainly HF or H_3PO_4) [95, 85] which has strong selectivity for etching aluminum oxide over silicon, thus making the reaction self-terminating in nature. Wet etching is generally rather isotropic and leads to stray undercut in the defined pattern if the process is not controlled properly. Therefore, for etching Al_2O_3 a highly diluted BHF solution is used rather than a concentrated HF solution to reduce the etch rate of the solution and prevent fluorine based impurities to stick on the surface. In summary, wet etching is the preferred choice for etching grown ALD layers of Al_2O_3 using BHF solution. In the following section, the relevant details for etching Al_2O_3 using BHF are discussed.

3.4.1 BHF for etching ALD grown Al_2O_3

Parameters that influence the wet etch process using BHF are, among others, concentration, time duration and temperature of the BHF solution. Since, all these parameters affect the etch rate which in turn will determine the precision in the pattern transfer,a systematic study of precess parameters is necessary in order to establish a reproducible and robust recipe for etching Al_2O_3 using BHF. To this end, silicon samples are first patterned with Al_2O_3 using the ALD recipe as shown in Table 2.1 giving a total thickness of $\sim$ 28 nm (this thickness is held constant throughout the etch test process for different concentration of etching solutions used). PMMA resist is then spin coated on the silicon sample with ALD grown Al_2O_3 dielectric with a thickness of $\sim$ 250 nm. This is followed by a 10 minute bake at 180 ℃

to harden the PMMA resist which will act as an etch mask during the wet etch. The PMMA is patterned using EBL with the optimum dose rates as determined in Section 3.3 and developed subsequently using MIBK:IPA. Finally, the patterned samples are subject to a BHF solution where wet etching is performed to selectively remove Al_2O_3 from exposed areas in the pattern with minimum undercut. Post etching, a 30 seconds DI water rinse is performed immediately to stop the etching process. Etched silicon samples are then analyzed under SEM for determining the result of the etch in terms of undercut and pattern definition. SEM is used for analyzing the samples because the dielectric Al_2O_3 layer gives a sharp contrast on the conducting silicon wafer once the pattern has been etched completely. It is worth noting that optimum imaging parameters for the SEM are established by the user, by first coarse focusing the electron beam on gold colloidal particles spread on a carbon substrate and later fine focusing on the sample surface by adjusting the stage height. This technique is performed at different spot sizes to maximize the resolution obtained while imaging under SEM. These images are then further analyzed using image processing techniques to calculate relevant length-scales of the etched structures. Due to the limited resolution in the images obtained from the SEM, there is a finite accuracy in determining absolute length-scales which is why it is convenient to compare relative length-scales in order to minimize the systematic uncertainty associated with this effect as previously performed in Section 3.3.

The analysis employed on the SEM images in determining the robustness and reliability of the etching procedure is carried out in the following manner as depicted in the schematic of Figure 3.5 (a). The mask defined on top of the ALD layer dictates

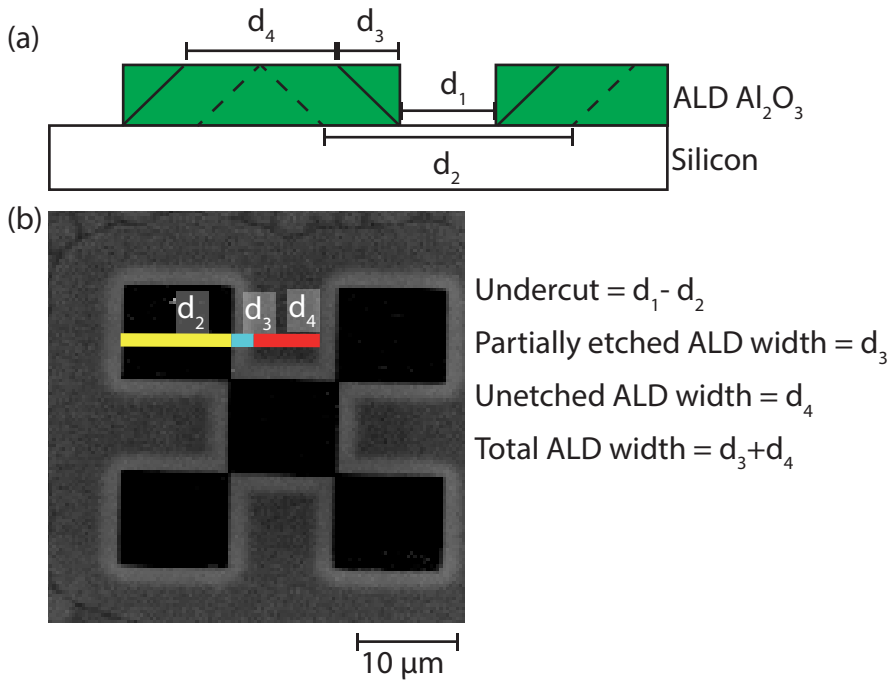

Figure 3.5: Analysis of etched pattern under SEM. (a) Schematic illustrating patterned ALD deposited Al_2O_3 on silicon substrate. Width d_1 is defined as 10 μm in the pattern, while d_2 is defined as the width of total etched structure, d_3 is defined as the width of partially etched Al_2O_3 and d_4 is the width of unetched Al_2O_3. Total ALD width remaining between fully etched structures is given by $d_3 + d_4$.

that the target width of the etched structure should come out to be 10 μm which is defined as d_1, as opposed to d_2 which is defined as the width of the etched structure obtained after the analysis of the etched pattern. Ideally, for precise etching of the patterned dielectric, d_1=d_2. However wet etching is a rather isotropic etching process, therefore typically $d_2 > d_1$ and with the difference between them $(d_2 - d_1)$ defined as the undercut. An example of a fully etched pattern analyzed under the SEM is shown in Figure 3.5 (b). As can be seen from Figure 3.5 (b), there is a lateral seam associated with the etched structures which is due to the fact that the etching solution attacks the deposited ALD dielectric from the side and causes partial etching of the deposited dielectric. This partially etched layer gives a different contrast in the SEM image and its width is labeled as d_3. However, the width of the

unetched ALD dielectric between the etched patterns is given by d_4. Finally, the total width of the pattern still protected by the ALD deposited dielectric is given by $d_3 + d_4$.

Performing the etch test involves dipping the sample in BHF solution, starting the timer, taking the sample out of BHF solution and rinsing the sample with DI water. There are two instances that can lead to uncertainty in the total etching which are: the uncertainty in starting the counter when the chip is dipped in BHF solution, and secondly, the time spent in transferring the sample from the BHF solution to the DI water beaker. In the second case BHF is still sticking to the surface and is etching the dielectric layer during the sample transfer, leading to unwanted undercut. Therefore, a robust recipe should allow for potential uncertainties in timing and yield acceptable results over a reasonably wide range of etch times.

3.4.2 BHF 1:10 solution as an etching agent for Al_2O_3 layers

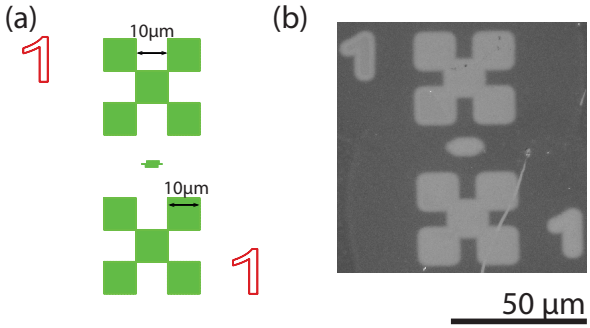

Figure 3.6: Etch Test performed on ALD grown Al_2O_3 layers using BHF 1:10 solution maintained at 30 ℃. a) Pattern used for etch test defined using EBL. b) SEM image of partially etched Al_2O_3 layer obtained after 18 seconds dip in BHF 1:10 solution.

The first series of etch tests was carried out using a 1:10 BHF solution maintained at 30 ℃ in a water bath. The etch pattern used in this etch test is shown in Figure

3.6 (a) and contains two checkerboard patterns with five squares measuring 100 μm^2 each, separated by one maze pattern in the middle with a line spacing of 300 nm. Note that the pattern was dropped out from subsequent etch tests as the line spacing was too small and it was hard to control the etching of the maze pattern using 1:10 BHF solution. Checkerboard boxes of 100 μm^2 are used in this etch test because they provide the ability to monitor and control the undercut at a scale of around 0.5 μm or less. This value of undercut is crucial for etching STM fabricated devices because the tolerance limit on the etched structures is also about 500 nm as discussed in Section 3.2. Figure 3.6 (b) shows the SEM image of the etched pattern after being etched for 18 seconds. As it can be seen from the image, the pattern has been transferred onto the dielectric layer, but the etch is not yet complete and the silicon surface is still fully covered with a dielectric layer (of varying height). This results in a low contrast and blurry features due to the insulation of the ALD layers. This image serves as a guide for determining whether Al_2O_3 deposited using ALD has etched fully or not.

Exemplary results of BHF 1:10 etch test are shown in Figure 3.7 (a-c) for etching times spanning 21 seconds, 24 seconds and 27 seconds, respectively. The dark areas correspond to the conducting silicon substrate where Al_2O_3 is etched completely and the bright areas to the dielectric layer of Al_2O_3. An etch rate of 1.33nm/s is obtained by using BHF 1:10 solution maintained at 30 ℃. However, using BHF 1:10 solution caused a lot of damage to the dielectric layer outside of the patterned area and this damage is quantified as undercut. The undercut obtained for 21 seconds etch in BHF 1:10 solution is 0.341 μm and is calculated as average of undercut at

four distinct positions on the pattern indicated by green lines in Figure 3.7 (a). 24 seconds dip in BHF 1:10 yielded a rather high undercut of 2.242 μm. Similarly, for 27 seconds of dip in BHF 1:10 solution, the undercut measured was 1.176 μm. It is worth noting that the edges of the pattern are damaged heavily as a result of prolonged etching in the BHF 1:10 solution as shown in Figure 3.7 (c) which introduces some uncertainty in the precise quantification of the undercut in the case of the 27 s etch. However, the effective width of the ALD layer, given by $d_3 + d_4$ is decreasing from 24 to 27 seconds which is as expected.

These results from the first etch test show that using BHF 1:10 solution is not ideal for etching ALD grown Al_2O_3 as it produces massive undercuts that are far greater than the tolerance needed for STM device processing. Also, it is worth noting that the undercut measured after 3 seconds with the uncertainty in handling the sample is almost four times the required tolerance limit of STM fabricated devices (in the case from 21 seconds to 24 seconds). Therefore, a more diluted BHF 1:15 solution was used in the next etch tests as it is a less aggressive etching solution.

Despite the aggressive etch reaction, one important point to note in the first etch test using BHF 1:10 solution is the presence of an incomplete etch of one of the structures in the pattern (the blurred label '1' in the bottom right) as shown in Figure 3.7 (b). This incomplete etch is attributed to residual PMMA left behind after the pattern was developed. It is worth noting that a longer bake time is used for hardening the resist prior to etching which might be a reason for this behavior. The presence of residual PMMA thereby inhibits the structure getting etched completely because the selectivity and etch rate for PMMA and Al_2O_3 are

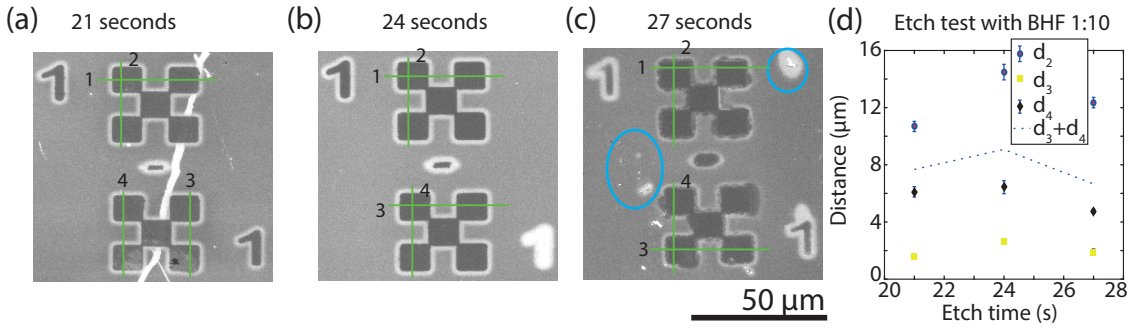

Figure 3.7: SEM images of the pattern obtained after etching in BHF 1:10 solution maintained at 30 ℃ giving an etch rate of 1.33 nm/s. Green lines show the location where analysis was performed. (a) SEM image obtained after 21 seconds dip in BHF 1:10 solution (dark contrast shows fully etched patterns) giving an average undercut of = 0.341 μm. (b) SEM image obtained after 24 seconds dip in BHF 1:10 solution giving an average undercut of 2.242 μm. (c) SEM image obtained after 27 seconds dip in BHF 1:10 solution giving an average undercut of 1.176 μm. (d) Plot comparing the differnt length-scales obtained after analyzing patterns etched in BHF 1:10 solution.

different. Alternatively, all the etched structures undergo complete etching for etch times lasting 21 s, 24 s (excluding the structure that was etched partially) and 27 s. In order to tackle this situation from happening again, an additional step was introduced for any future etch test to perform a short plasma treatment after development using O_2 plasma before the etching process. This process will uniformly remove a certain thickness of the PMMA mask controllable by the duration and power of the plasma and therefore remove any residual PMMA from the patterned mask and exposing the ALD layer underneath the patterned mask for the etchant.

Additionally, using BHF 1:10 for etching Al_2O_3 layer might affect the deposited dielectric outside of the defined pattern randomly as shown in Figure 3.7 (c) (indicated by blue circles). These patches encircled in blue establish the fact that the BHF 1:10 solution is attacking the resist layer at unintended areas and causing degradation to the definition of the deposited dielectric. This is not desirable in the

case of STM based devices as the removal of the dielectric over the masked nanostructures might expose inner device structures and lead to native oxide formation which would defeat the purpose of depositing dielectric and reduce the thickness (and thereby insulation) of the dielectric layer.

3.4.3 BHF 1:15 solution as an etching agent for Al_2O_3 layers

During the second series of etch test, BHF 1:15 solution maintained at 30 ℃ in a bath is used. The pattern used in this etch test is shown in Figure 3.8 (a) and it consists of checkerboard boxes along with rectangles that roughly resemble the area needed to open to access all ohmic contacts in a STM fabricated device ($20\mu m \times 5\mu m$). This etch test also involved an additional treatment of O_2 plasma before the patterns are etched to make sure that there is no residual PMMA left on the exposed area on the surface. The conditions used for O_2 plasma treatment are 30 seconds exposure to O_2 flow of 50 sccm at 50 mT pressure in the chamber with 20 Watts of applied power. These conditions are very mild and have no significant effect on the thickness of the PMMA resist which is $\sim$ 250 nm thick and requires much more power ($\sim$ 100 watts) and longer time ($\sim$ 180 seconds) to be removed completely. These parameters are typically used while processing STM fabricated devices to remove the PMMA resist mask after etching the holes to contact the buried phosphorus layer.

The results obtained after performing the etch test using BHF 1:15 solution maintained at 30 ℃ are shown in Figure 3.8 (b-d). The Al_2O_3 layer got completely etched away in 32 seconds using this solution as compared to 21 seconds for BHF 1:10 solution. The etch rate in case of BHF 1:15 solution is 0.875nm/s. All the length-

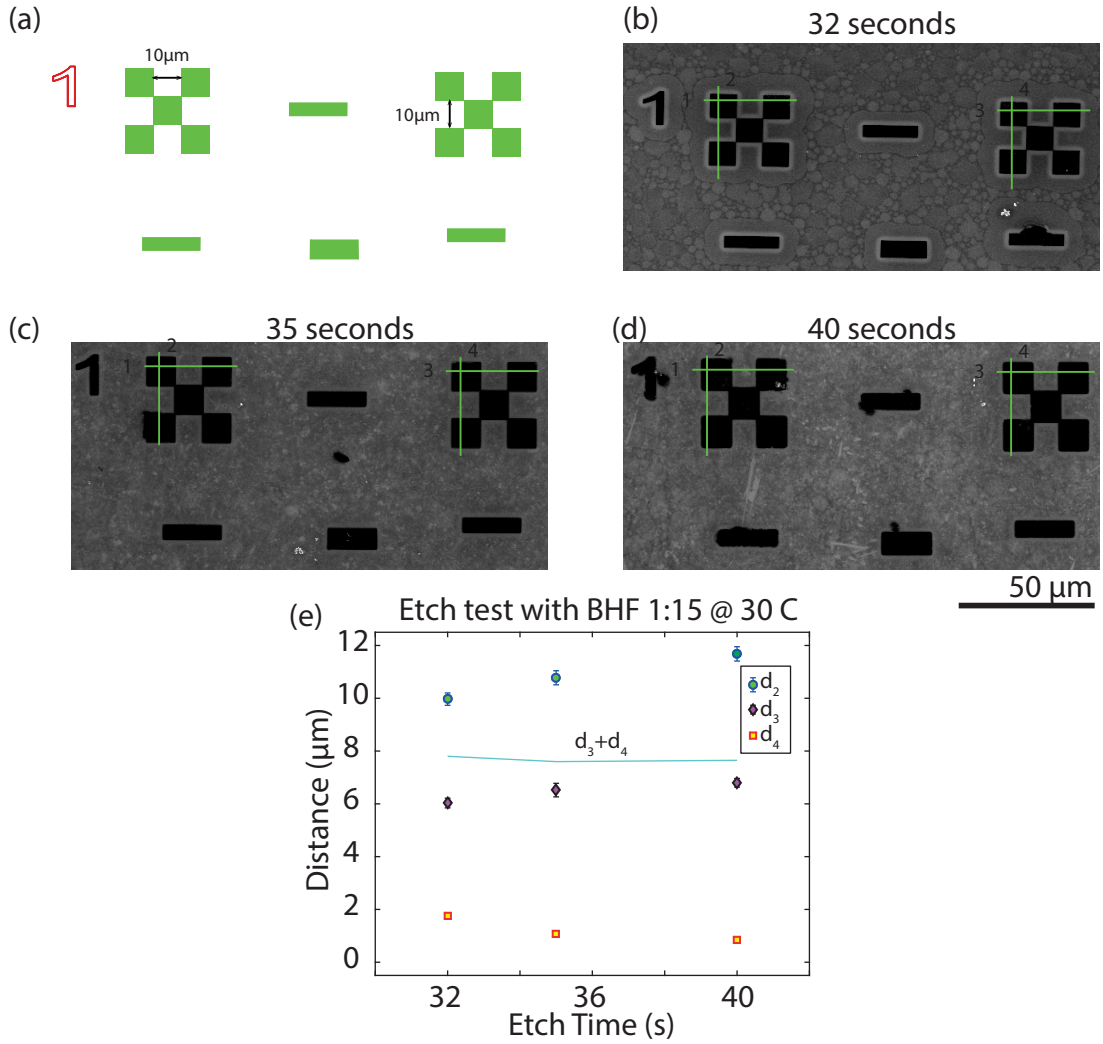

Figure 3.8: Etch test performed on ALD grown Al_2O_3 layers using BHF 1:15 solution maintained at 30 ℃. (a) New pattern used for etch tests defined using EBL. (b) SEM image obtained after 32 seconds dip in BHF 1:15 solution stored at 30 ℃ giving no undercut. (c) SEM image obtained after 35 seconds dip in BHF 1:15 solution giving an average undercut of 0.388 μm. (d) SEM image obtained after 40 seconds in BHF 1:15 solution giving an average undercut of 0.841 μm.

scales calculated in this case are reported for calculations across four checkerboard boxes (only two are shown in the Figure 3.8). For etches lasting 32 s no undercut was observed given by average of 4 lines shown in green in Figure 3.8 (b). For BHF 1:15 solution two etch test lasting 35 s and 40 s were also conducted to quantify the undercut. These longer etch times also provide information regarding the potential damage the surface might suffer due to the time uncertainty involved in handling

the sample. Surprisingly, the effective dielectric width remains the same in both cases, however it is reduced from when compared to the 32 s etch. A dashed blue line calculates the sum of d_3 and d_4 giving the total width of the ALD dielectric left and this is basically left unchanged for the 35 s and 40 s case as shown in Figure 3.8 (e). For the etch test lasting 35 s, 388 nm undercut was observed using profile measurements across four green lines as shown in Figure 3.8 (c) and similarly Figure 3.8 (d) shows the 40 s etch where 0.841 μm of undercut is observed. These results prove that using a BHF 1:15 solution leads to minimal undercut in the pattern and accounting for a time uncertainty of 3 seconds still limits the undercut to values that are within the tolerance ($<$ 500 nm) required for processing STM fabricated devices. Additionally, all the patterned structures for the three cases are fully etched, showing that using the O_2 plasma treatment before etching the dielectric is an effective step and leads to more reliable etching profile afterwards.

3.5 Effect of O_2 plasma treatment on the etch success

After having established a robust combination of etchant and etch time and in order to compare the effect of O_2 plasma treatment on the etched structures, Figure 3.9 shows the fraction of pattern etched completely without (purple) and with (yellow) initial O_2 plasma treatment in order to remove residual PMMA for varying etch times of 32 to 40 seconds. Throughout this investigation, a BHF 1:15 solution maintained at 30 ℃ in a water bath is used. Finally, it is observed that for the sample without

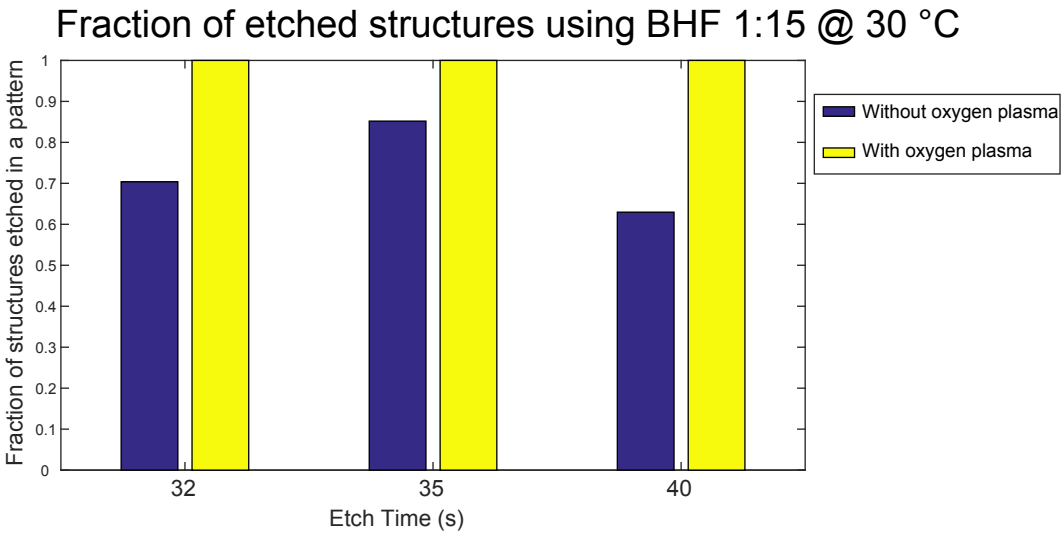

Figure 3.9: Bar graph showing showing the success rate in etched structures without (purple) and with (yellow) oxygen plasma for 32 seconds, 35 seconds and 40 seconds, respectively using a BHF 1:15 solution.

any O_2 plasma treatment, the success rate is drastically reduced. Even for etch times of 40 s, where etched patterns show a strong underetch of $> 1\mu$m, the success rate of etching is only 60%. This behavior is attributed to residual PMMA that is left on the patterned areas after developing the resist exposed during EBL. This behavior is further substantiated by the random, non-monotonic dependence of success rate on the etch time. To test this hypothesis, a mild oxygen plasma etch is introduced before the etch is performed. This oxygen plasma treatment will uniformly reduce the thickness of the PMMA mask, thereby exposing developed areas fully. As a result, the yellow bar graph shows that all the structures are etched completely removing any uncertainty in etch time caused by residual PMMA.

3.6 Effect of temperature on the etch process

Another process parameter studied is the influence of the temperature of the etch bath on the reactivity, parameterized by the etch time. Similar etch tests to the previous series were therefore conducted for a BHF 1:15 solution stored at 20 ℃.

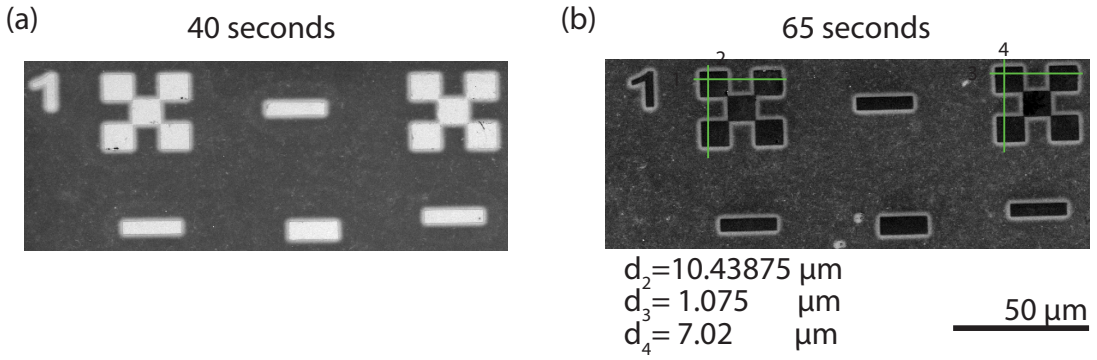

Figure 3.10: Etch test performed on ALD grown Al_2O_3 layers using BHF 1:15 solution stored at 20 ℃. a) SEM image obtained after 40 seconds dip in BHF 1:15 solution stored at 20 ℃ showing patterned structures that are not fully etched (as there is no dark contrast). b) SEM image obtained after 65 seconds dip in BHF 1:15 solution stored at 20 ℃ with fully etched structures giving an average undercut of 1.325 μm.

The pattern used in this etch test is similar to the pattern showed in Figure 3.8 (a). Results of this etch test are shown in Figure 3.10 (a) and (b). Etch rates for this test were expected to be less than the etch rate for the BHF 1:15 solution stored at 30 ℃ as the reactivity of the solution goes down with decreasing temperature. Indeed, the etch rate reduced by $\sim$ 50 ٪, falling from 0.875 nm/s to 0.431 nm/s. Figure 3.10 (a) shows the pattern after it was dipped in the BHF 1:15 solution stored at 20 ℃ for 40 seconds and the pattern has not etched completely while similar etch time for the temperature of the etchant at 30 ℃ already has a significant undercut of 840 nm. A dip for 65 seconds in the same solution shows the pattern etched uniformly across all structures. The undercut obtained for 65 seconds calculated across six

positions indicated using green arrows in Figure 3.10 (b) is 0.219 μm. While the undercut is well within the specified target range, using BHF 1:15 solution stored at 20 ℃ is not suitable for etching the patterned mask for STM fabricated devices as the time required to etch is impractical since the user needs to hold the wafer piece for a long time using a tweezer in a beaker filled with BHF.

3.7 Summary of all etch tests

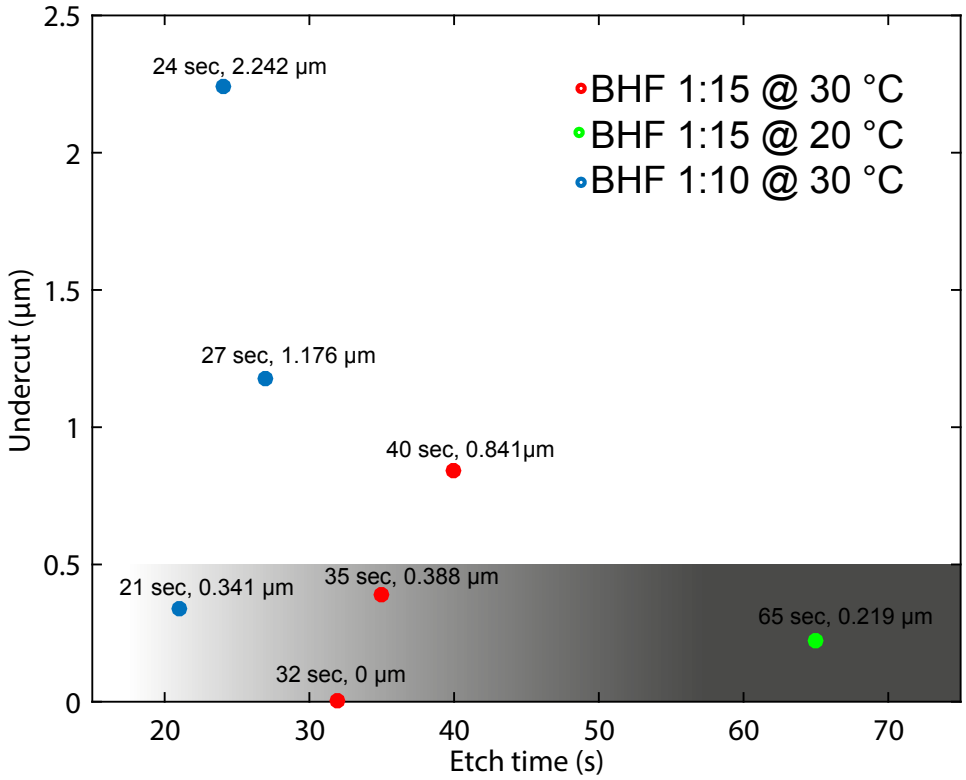

Figure 3.11: Analysis of etching times versus undercut for BHF 1:15 at 30 ℃, BHF 1:15 at 20 ℃ and BHF 1:10 at 30 ℃. Shaded region shows the desired area of operation for STM fabricated devices keeping the undercut less than 500 nm.

A summary of all the etch tests carried out on Al_2O_3 layer grown on silicon using ALD is shown in Figure 3.11. As discussed in Section 3.2, processing STM fabricated devices containing Al_2O_3 as a dielectric requires that the undercut is

limited to 500 nm or less. In Figure 3.11, a shaded region is constructed spanning 0 and 500 nm in undercut, representing the area where etching can be performed reliably without affecting the dielectric protecting the inner device dimensions. The etch rate obtained in the case of a BHF 1:10 solution maintained at a temperature of 30 ℃ is 1.33 nm/s for an Al_2O_3 dielectric 28 nm in thickness which was etched completely in 21 seconds. Although the etch rate is the fastest within this study, it does affect the sanctity of the film severely and shows a very large undercut of 1.607 μm during the short etch time of 21 s. Moreover, with a time uncertainty in handling the sample of 3 s, the undercut is increased by four times the tolerance limit required for processing STM fabricated devices. Using BHF 1:15 solution stored at 20 ℃, a moderate etch rate of 0.43 nm/s is observed. A major concern in using BHF 1:15 solution stored at 20 ℃ is the handling time for the entire process is rather long. Lastly, using 1:15 BHF solution maintained at 30 ℃ an etch rate of 0.875 nm/s is obtained providing excellent control over the undercut observed in the masked area in the pattern. Using 1:15 BHF solution gives no significant undercut after fully etching the grown Al_2O_3 layer in 32 seconds. Furthermore, for a time uncertainty of 3 s in the case of BHF 1:15 solution, an overall undercut of 388 nm is observed (for 35 s) which makes the process robust against human handling errors. In conclusion, a reliable etch profile, moderate etch rate and significantly less undercut makes using BHF 1:15 solution maintained at 30 ℃ for 32 s the preferred etching agent for removing ALD grown Al_2O_3 films on STM fabricated devices for quantum information processing.

Chapter 4

Electrical Characterization of Al_2O_3 top gated atomic precision devices

In this chapter, the electrical characterization of STM-patterned donors with an ALD deposited Al_2O_3 dielectric and Al top gate incorporated into the devices will be presented. In Chapter 3, various process parameters involved in the integration of Al_2O_3 dielectric layers into the existing *ex-situ* processing of STM-patterned donor based devices were discussed. The focus was to determine the optimal dose rate for the EBL resist to contact the buried STM-patterned devices and allow wet etching of the Al_2O_3 dielectric, minimizing the undercut of the dielectric to below 500 nm. This therefore maintains the integrity of the Al_2O_3 dielectric for the stable integration of 80 nm of Al top gate. In this chapter, this developed recipe is applied to three UHV fabricated Si:P devices, namely (i) a Hall bar with a global top gate, (ii) a STM-

patterned SET with ALD deposited Al_2O_3 dielectric and an Al gate, and finally (iii) a four quantum dot device with an Al top gate insulated with Al_2O_3 dielectric deposited using ALD.

4.1 Integrating a top gate on a 2D Si:P δ-layer fabricated in UHV

Hall bar devices are patterned on a δ-doped silicon layer prepared by phosphine dosing of a silicon substrate followed by silicon encapsulation at low temperature (250 ℃) in the UHV environment of the STM. Using the recipe mentioned in Section 2.3, Hall bars are patterned on a δ-doped silicon surface. Hall bars using P doping have previously reported high values of the 2D sheet carrier density $\sim$ 2-3 $\times 10^{14}$ cm^{-2} using this monolayer phosphorus doping of silicon δ-layers [131, 132]. With such high carrier densities, delta doped layers already demonstrate quasi-metallic behavior with 100 ⁒ dopant activation [131].

For performing electrical characterization of the device, a silicon sample containing four Hall bars was fabricated. One of the Hall bars was used to perform the magnetotransport experiments as shown in Figure 4.1 (a) using the contacts shown to measure V_{xx} and V_{xy}. The aspect ratio of the Hall bar used in this thesis is 0.2 (L=100 μm and W=20 μm). All the measurements shown in this section were performed in a Helium dewar at 4.2 K on a magnetic probe specifically designed for the Hall measurements. The experimental setup for performing the magnetotransport measurements on the Hall bar is shown in Figure 4.2. Here a 4 V sine wave with at

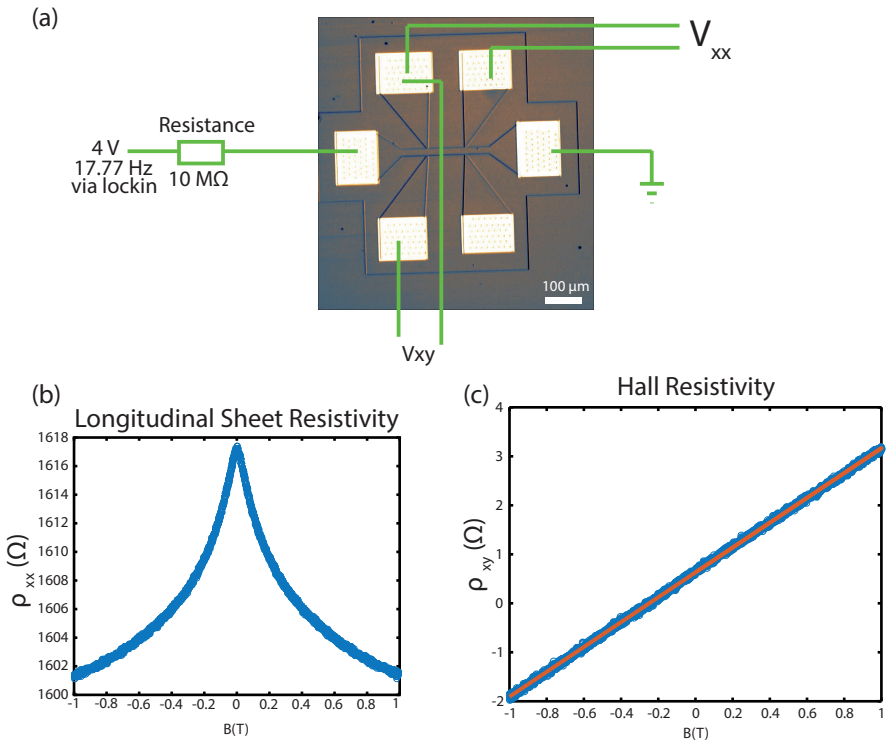

Figure 4.1: Characterization of Si:P δ-layer (without top gate). (a) Optical image of a Hall bar with ohmic contacts (bright white patches). Lines shown in green describe the measurement setup. V_{xx} is used for measuring μ and V_{xy} is used for calculating n_s. (b) Longitudinal sheet resistivity of the 2D electron system that is used for computing mobility by measuring voltage V_{xx}. (c) Hall resistivity for the patterned Hall bar used for determining the active carrier density, n_s of the 2D electron system.

a frequency of 17.77 Hz is used as an input signal to the conducting channel of the Hall bar with the other end of the Hall bar grounded. A 10 MΩ resistor is used in series with the source contact of the Hall bar to maintain a steady current of 400 nA through the conducting channel (this is very high current due to macroscopic size of the Hall bar as compared to the SET device where the current is around $\sim$ 0.5-1 nA). The voltage drop is then measured at two positions on the Hall bar using two lockin amplifiers as shown in Figure 4.2, across V_{xx} (longitudinal resistance) and across V_{xy} (transverse resistance). The longitudinal sheet resitivity and Hall resistivity obtained from the magnetotransport measurements on the Hall bar are shown

in Figure 4.1 (b) and (c). Weak localization behavior is visible for the longitudinal sheet resistivity data in Figure 4.1 (a) where increasing the magnetic field leads to decreased resistivity in the conducting channel as explained in Section 2.3. From these graphs, the active carrier density was calculated to be, $n_s = 2.46 \times 10^{14}$ cm^{-2} from the Hall slope and $\mu = 78.42$ cm^2/Vs calculated using the longitudinal sheet resistivity. These results obtained for ungated Hall bar are in good agreement with the previously reported values for 2D Si:P under similar growth conditions [131, 132].

4.1.1 Depositing Al_2O_3 using ALD on a Hall bar

After successfully measuring n_s, a dielectric layer of Al_2O_3 was deposited on the same silicon sample containing all four Hall bars. It is worth noting that for this 2D δ-doped layer no etching procedure is required after depositing the dielectric on the Hall bar devices to make contact to the buried ohmic patches because the bond can force through the deposited ALD layer and contact the Al patch directly. For depositing the Al_2O_3 dielectric the Hall bar was first dipped in BHF 1:15 for 8 s to remove any native oxide present on the surface. All the patterned ohmic contacts remain unaffected by this etch because BHF solution does not etch Al. The Hall bar sample was then rinsed with DI water for 7 seconds before being transported in a petri-dish to deposit Al_2O_3. The recipe for depositing Al_2O_3 using 200 cycles at 250 ℃ is shown in Table 2.1. After depositing $Al_2O_3 \approx 28$ nm thick, a top gate is patterned on the dielectric using EBL by utilizing the optimum dose rate calculated in Section 3.3 of 250 μC/cm^2 (similar to the dose rate for patterning the etch mask).

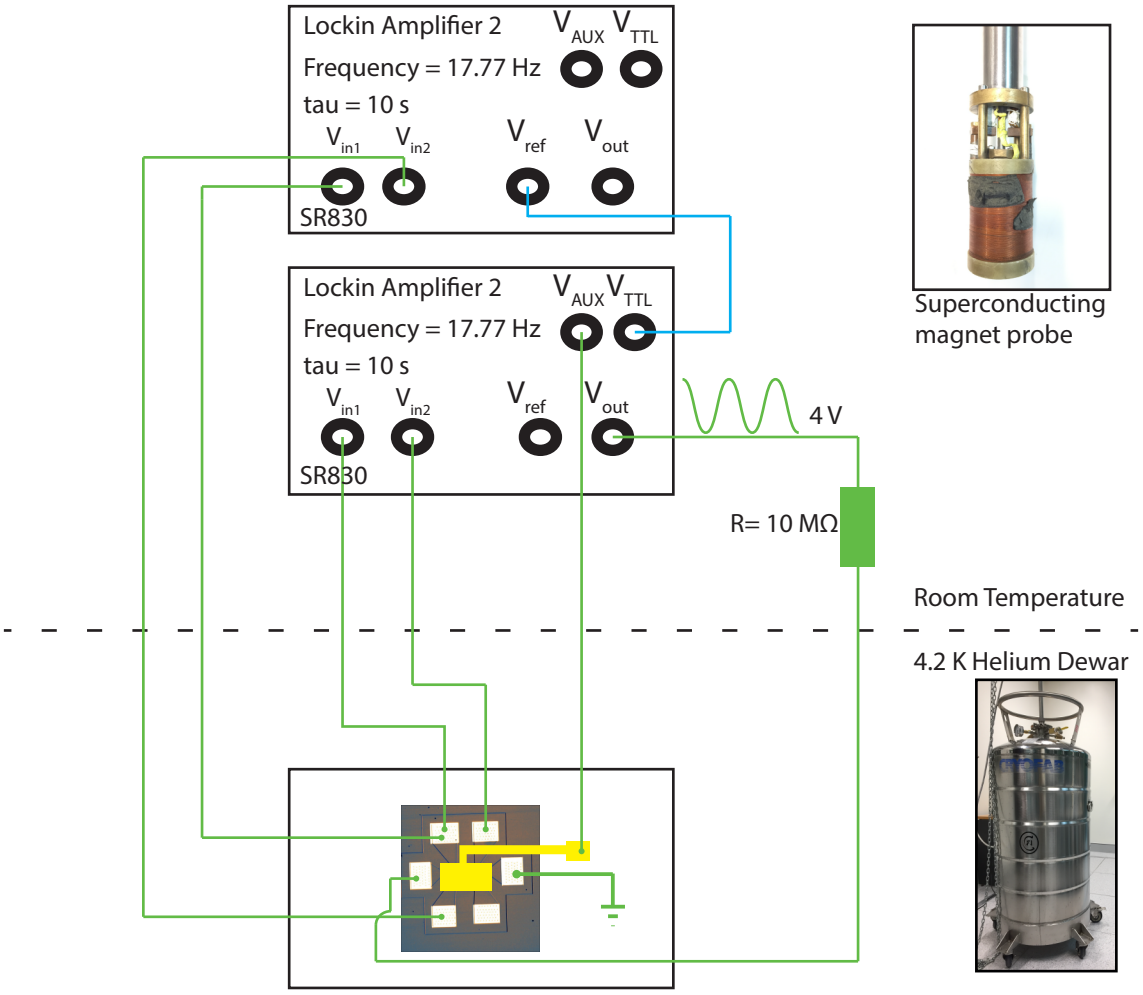

Figure 4.2: Electrical measurement configuration of the Hall bar consisting primarily of two lock-in amplifiers with their main settings depicted in the sketch using a frequency of 17.77 Hz and $\tau = 10$ s (time constant). All measurements have been performed in a Helium dewar at 4.2 K (depicted in the bottom right inset). A photography of the superconducting magnet probe is shown in the top right inset.

An 80 nm Aluminum layer is then evaporated on top of the Al_2O_3 dielectric to act as a metallic top gate. Finally lift-off is performed using NMP. The Hall bar was then glued to the charntex using PMMA A5 and the ohmic contacts bonded using an Al wedge bonder. The device was then remeasured at 4.2 K.

The silicon sample used for performing the magnetotransport measurements earlier in Section 3.1 had four Hall bars in total. The active carrier density n_s measured on the first Hall bar was 2.46×10^{14} cm^{-2}. However, a different Hall bar was used for

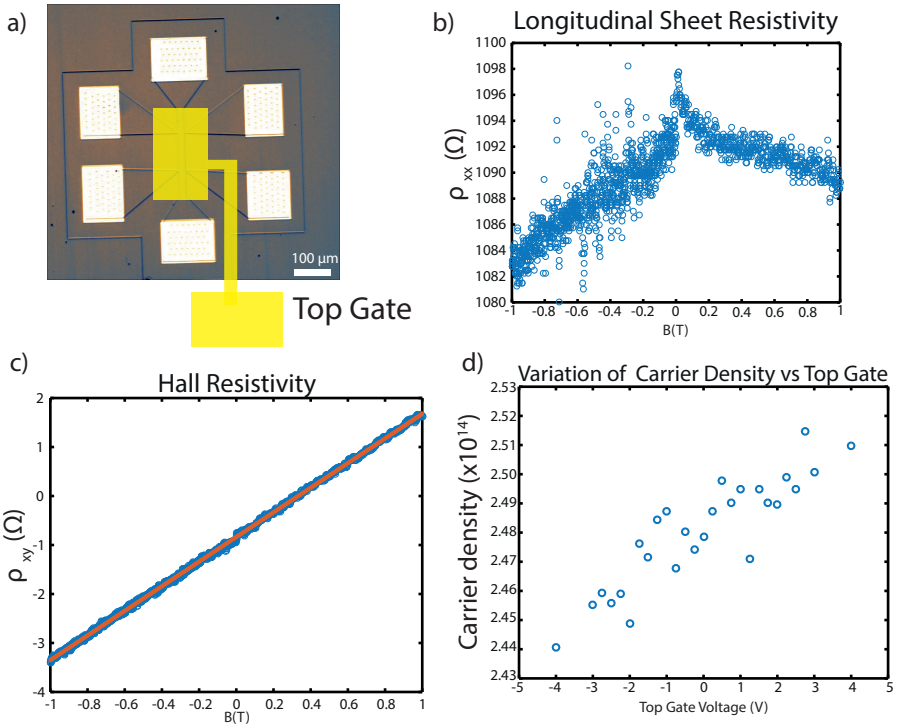

Figure 4.3: Characterization of Si:P δ-layer with a metallic top patterned gate on an Al_2O_3 dielectric. (a) Optical image of the Hall bar with the location of patterned top gate shown in yellow. (b) Longitudinal sheet resistivity of the Hall bar for a top gate voltage of 2 V. (c) Hall resistivity of the Hall bar for a top gate voltage of 2 V. (d) Variation of the carrier density with top gate voltage measured between -4 V to 4 V.

performing the electrical characterization after depositing Al_2O_3 layer due to some issues during lift-off for the patterned top gate. Figure 4.3 (a) shows an optical image of this second Hall bar with the location of the top gate shown using a schematic. The top gate is supplied with a bias voltage from -4 V to 4 V using the AUX port of one of the lockin amplifiers as indicated in Figure 4.2. Magnetotransport measurements were performed on the Hall bar under varying top gate voltages. Figure 4.3 (b) and (c) show the longitudinal sheet resistivity and Hall resistivity calculated between -1 Tesla to 1 Tesla for a top gate voltage of +2 V giving $n_s = 2.48 \times 10^{14}$ cm^{-2} and $\mu = 114.69$ cm^2/Vs. The carrier density and mobility for top gate voltage of 0 V are n_s 2.47×10^{14} cm^{-2} and $\mu = 113.71$ cm^2/Vs. Now, in order to determine

the influence of the top gate voltage on the active carrier density in the channel the device is measured at various top gate voltages as shown in Figure 4.3 (d). Very little tunability ($\leq 3\%$) is seen in the active carrier density from 2.44 to 2.51×10^{14} cm^{-2} for a top gate voltage range of -4 V to +4 V. This is expected for the Si:P δ-layers as they already highly metallic due to the large 2D sheet density [131]. In other material systems such as Si/SiGe based heterostructure, a high tunability ($\sim$ 80 %) of the carrier density has been achieved by employing a Al_2O_3 dielectric layer [93].

The top gate patterned for the Hall bar measurements was the largest surface area top gate (0.4 mm^2) in this thesis used to cover the Hall bar (20 μm $\times$ 100 μm). The overall robust operation of the top gate without leaking in the -4 V to 4 V range highlights the pinhole free growth of the ALD deposited dielectric. These results highlight the ability to introduce a dielectric layer of Al_2O_3 and Al top gate over an UHV δ-doped Si:P layer with minimal gate leakage.

4.2 Integrating a top gate on a planar STM-patterned SET

After having established the application of an Al_2O_3 ALD layer and Al top gate on a Hall bar and demonstrated the excellent insulation of the dielectric obtained for top gate voltages up to $\mid V_{TG} \mid = 4$ V (covering a large surface area), this strategy is now incorporated over a STM-patterned precision donor device. To achieve this, the full advantage of the careful study of patterning and etching the

ALD dielectric layer presented in Chapter 3 is employed. The SET quantum dot device is a three terminal device consisting of two leads, labelled source and drain, a central island in-between (SET quantum dot) and a SET gate to capacitively control the flow of current between the leads via the quantum dot island. Details of the theory of single-electron transport have been outlined in Section 2.4. The SET quantum dot is typically employed as a charge sensor for donor based quantum dot devices and has been used extensively before in a similar design [63, 64, 68]. The device fabrication procedure for making planar SET devices carried out in the UHV using STM hydrogen lithography on a silicon sample with etched registration markers is discussed in Chapter 2. A STM image of a hydrogen terminated Si (001) surface where lithography will be performed is shown in Figure 4.4 (a). Here, 2 step edges with the dimer rows running perpendicular to each other in each atomic layer are shown. Figure 4.4 (b) shows the SET quantum dot fabricated on the hydrogen terminated Si(001) surface by selectively desorbing H using the STM tip. The lithographically patterned surface in Figure 4.4 (b) looks bright because of the change in the electronic structure due to the presence of dangling bonds in the patterned regions compared to the nearby hydrogen-terminated Si(001) surface.

In this device, the quantum dot island is in the center connected via two tunnel junctions to the source and drain terminals as shown in Figure 4.4 (b). An additional gate, labelled the SET gate, was patterned in-plane to tune the electron number on the SET island by applying electrostatic gate voltages. The SET gate is capacitively coupled to the SET island and by applying a voltage to the SET gate the electrochemical potential of the SET island can be tuned. All the three

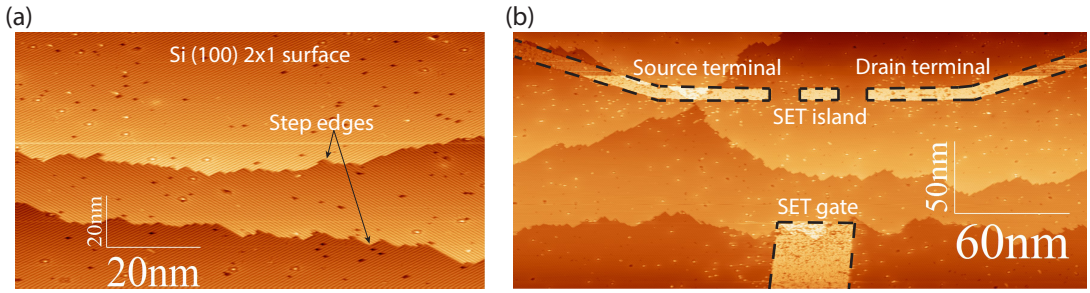

Figure 4.4: Fabrication of a STM based donor quantum dot device. (a) Hydrogen terminated Si (001) surface in the STM chamber before performing lithography. (b) A 3 terminal device consisting of source, drain and a gate patterned using the tip of the STM by selectively desorbing hydrogen from areas of interest. Source and drain terminals in this device are tunnel coupled to the SET island, while the gate is $\sim$ 85 nm away and is capacitively coupled to the SET island.

terminals in this quantum dot device were terminated by extension leads $\sim$ 2 μm long, which were patterned using the field emission mode in STM lithography and aligned to the etched registration markers in the substrate. After STM lithography, the silicon sample is dosed with PH_3 gas at a chamber pressure of 2×10^{-7} mbar for 2 mins. After dosing the surface with PH_3, an anneal for 1 minute is performed at 350℃ to incorporate the phosphorus donors into the silicon surface in the patterned regions. The final step in the STM fabrication process involves growing $\sim$ 45-50 nm of epitaxially silicon over the patterned device in which donor diffusion is minimized by maintaining a low substrate temperature of 250 ℃.

A full process flow for integrating ALD deposited thin films on to the STM fabricated devices is shown schematically in Figure 4.6 with all the steps from the moment when the device is taken out of the STM until depositing metal onto the EBL patterned ohmic contacts. This recipe should serve as a useful guide in integrating an ALD deposited Al_2O_3 dielectric for processing STM fabricated devices. To summarize the process, post-STM fabrication, the patterned quantum dot device (ALD-SET) is taken out of UHV and is treated with 1:10 HF solution for 30 s

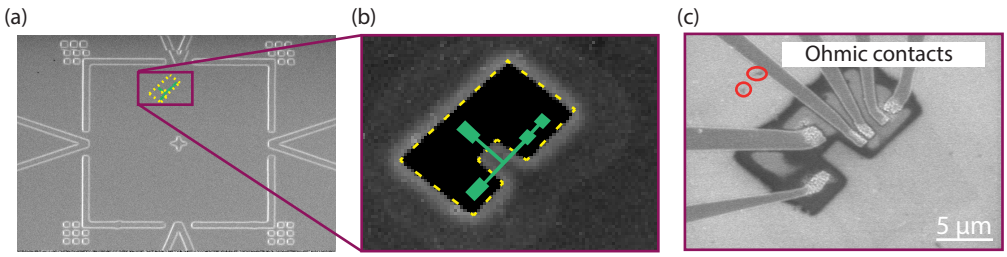

Figure 4.5: Cleanroom processing of the STM fabricated device deposited with an ALD grown dielectric. (a) Defining the etch mask for the ALD dielectric and patterning with the optimal dose rate of 220 μC /cm^2. (b) SEM image of the etched ALD over the STM patterned device (false colored green) after 35 seconds etch in BHF 1:15 solution. The STM pattern shown in green is aligned to the etched registration markers. (c) SEM image of the ohmic contacts, showing the ALD layer in light grey, the bare silicon substrate where etched in black and the metalization in dark grey aligning with the holes etched using RIE. Red encircled features are used later as reference markers to align the etched dielectric and top gate.

followed by DI water rinse for 30 s. The SET device is then loaded into the ALD chamber for depositing $\approx$ 28 nm of Al_2O_3 using the recipe mentioned in Table 2.1. After depositing Al_2O_3, pre-etched registration markers are used to locate the STM patterned terminals. A schematic of ALD-SET device is shown with green solid boxes in Figure 4.5 (a) where the accurate location of the STM fabricated donor device is shown. Dashed yellow pattern surrounding the ALD-SET represent the mask pattern which will be transferred on the grown dielectric patterned by EBL as discussed in Section 3.4. w Figure 4.5 (b) shows the masked pattern etched using BHF 1:15 solution whilst still covering the inner device dimensions. After this step, standard cleanroom processing used for STM based quantum dot devices is carried out and ohmic contacts are patterned as shown in Figure 4.5 (c). Aluminum metal is evaporated over the ohmics and lift off is performed using NMP. The device is then glued on a PCB board and bonded using the Aluminum wedge bonder.

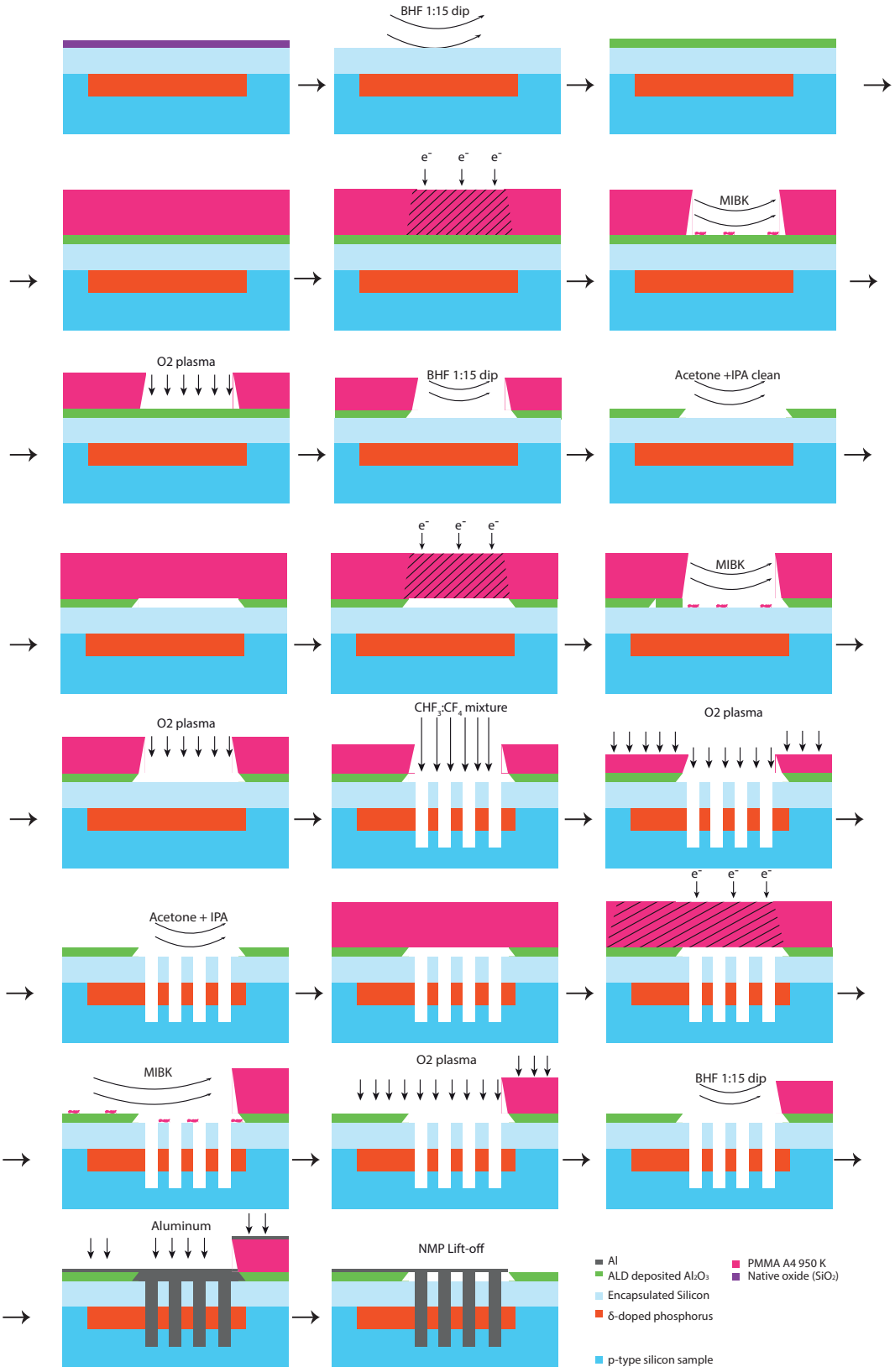

Figure 4.6: Process flow for adding a layer of Al_2O_3 dielectric and then establishing ohmic contact to the buried Si:P device.

4.2.1 Capacitance modeling for the ALD SET device before and after top gate

The electrical transport properties of the SET quantum dot device is presented in Section 4.2.2. Using the gate voltages i.e. the SET gate and the top gate, the electrochemical potential of the dot can be tuned over a wide range. The ability to tune the quantum dot depends on two factors: the gate lever arm and the effective gate range. The gate lever arm is given by $\frac{C_G}{C_\Sigma}$ and the effective gate range is determined by the gate geometry. It would be beneficial to be able to predict the gate lever arms and gate range before device fabrication as the STM fabrication process is lengthy. To model the devices patterned using the STM, capacitance modeling is done using COMSOL. COMSOL uses a finite element solver to perform classical electrostatic capacitive modeling for generating a capacitance matrix for a given device geometry.

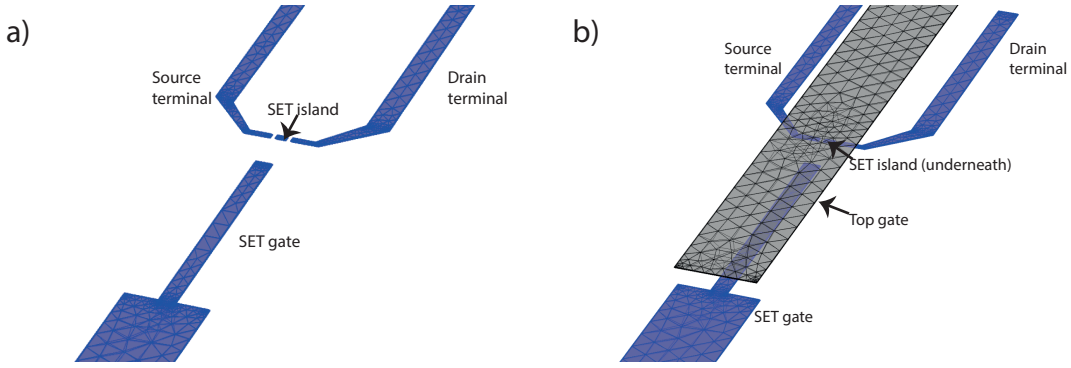

Figure 4.7: Schematic of ALD SET device in COMSOL. a) ALD SET device in a meshed configuration. b) ALD SET device patterned with a top gate in a meshed configuration.

Two types of device designs were modeled using COMSOL for the ALD SET

device. The first involved modeling the SET quantum dot device with a ALD grown dielectric on top. The second type included modeling the SET quantum dot device with an ALD grown dielectric and a top gate. Figure 4.7 shows both the geometries used for modeling the ALD SET quantum dot device.

Theoretical prediction from COMSOL			
	Charging Energy	SET Gate Lever arm	Top Gate Lever arm
ALD SET without top gate	9.1 meV	0.1417	n/a
ALD SET with top gate	9 meV	0.0674	0.4382

Table 4.1: Theoretical values obtained after solving the capacitance matrix generated from COMOSL modeling.

The major observations from the COMSOL modelling that show impact of the metallic top gate and the dielectric are:

1. The charging energy of the quantum dot is $E_c \sim 9$ meV. No significant impact of the top gate is observed as expected.

2. The SET gate lever arm is considerably affected by the presence of a metallic top gate as expected.

3. The lever arm of the top gate is larger than the SET gate due to the larger capacitive coupling of this larger gate with the STM-patterned nanostructures.

4.2.2 Characterization of the ALD-SET device

The electrical characterization presented in this section was carried out in a Helium dewar at 4.2 K. The measurement set-up is shown in Figure 4.8 and primarily consists of a NIDAQ USB 6363 data acquisiton module, providing up to 4 analog voltage outputs which are used for biasing gate electrodes. Alternatively, in case of

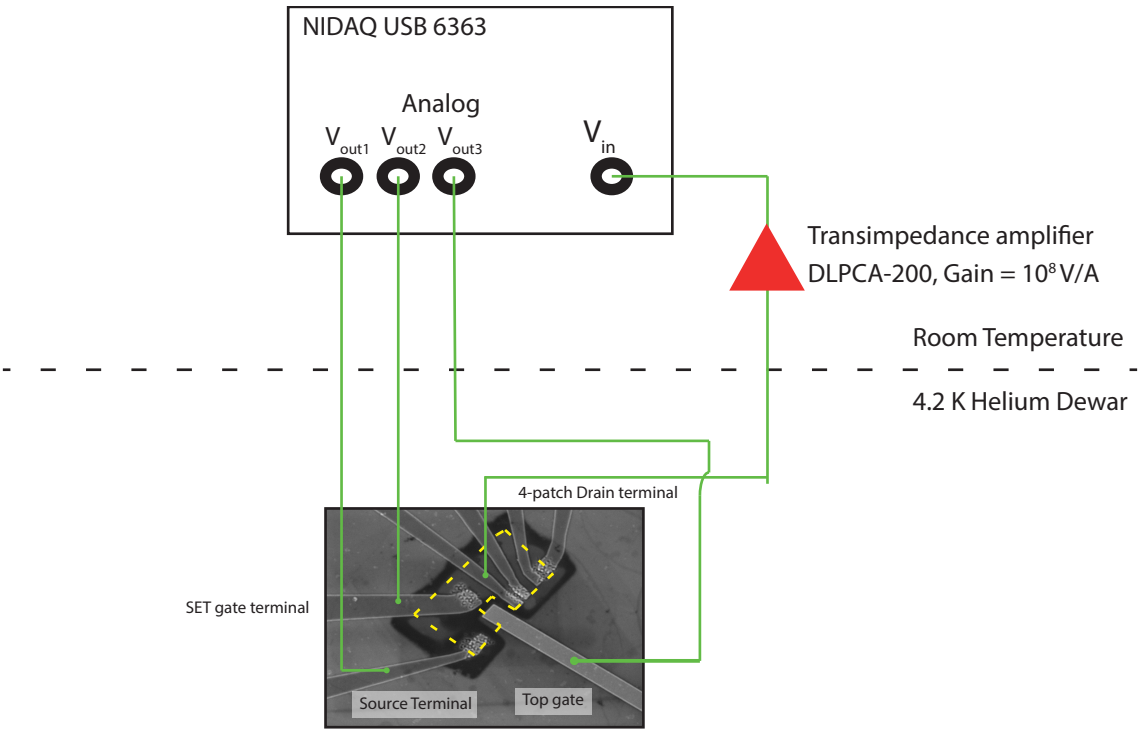

Figure 4.8: Measurement setup used in electrical characterization of the ALD-SET device. Analog voltage is applied through NIDAQ 6363 and output drain current is digitized using the same device after room temperature amplification using a Femto DLPCA-200 transimpedance amplifier with a gain of 10^8 V/A.

leakage measurements on the gate, a source measure unit Keithley 237 was used. Coulomb diamonds were observed when plotting the conductance through the SET as a function of the in-plane gate voltage, V_{SET} at various source-drain biases V_{sd} showing quantum dot behavior. The SET quantum dot used in this thesis is sensitive to single electron transitions within its vicinity and has been employed as a single electorn charge sensor for various single-shot read out applications [68, 63]. Therefore, determining the stability of the SET charge sensor for multi-qubit measurements is crucial. The stability can be quantitatively analyzed by following a charge transition over a period of time and measuring the drift accumulated over the entire duration. The SET gate stability for this device was recorded by scanning two conduction peaks for 12 hours. After this, a top gate was patterned on top of

the inner device dimensions masked with the grown dielectric layer. Coulomb diamond measurements were performed again but now using the top gate on top of the Al_2O_3 dielectric. There were some particular aspects of adding the top gate. Firstly, the presence of the top gate was observed to weaken the influence of the SET gate. However, the top gate provides a much larger tunability than the in-plane SET gate. The stability traces for the SET gate with and without the top gate were taken and are analyzed. Finally, the top gate was tested for a dynamic frequency response to determine if it can be used for pulsing experiments.

4.2.2.1 Electrical characterization of the SET without a top gate

The first set of electrical measurements performed on this device included studying standard transport properties for a many-electron single quantum dot device, also commonly referred as single electron transistor (SET). The quantum dot device discussed here consists of a source and a drain terminal tunnel coupled via a quantum dot island (SET island), which is also capacitively coupled to the SET gate electrode. The flow of current between the source and the drain terminal occurs via the SET island where energy levels of the SET island participate in transport.

At zero source drain bias and zero gate voltage, there are no energy levels participating in transport and no current flows. This condition is known as Coulomb blockade. However, at a finite source drain bias, when an energy level of the SET island comes in alignment in the source-drain bias window, current starts flowing and the repeated behavior of current switching on and off due to presence (absence) of energy levels for transport is depicted via Coulomb peaks (as shown in Figure 2.11 and 4.9 (b)). The finite source drain bias necessary for current flow from the con-

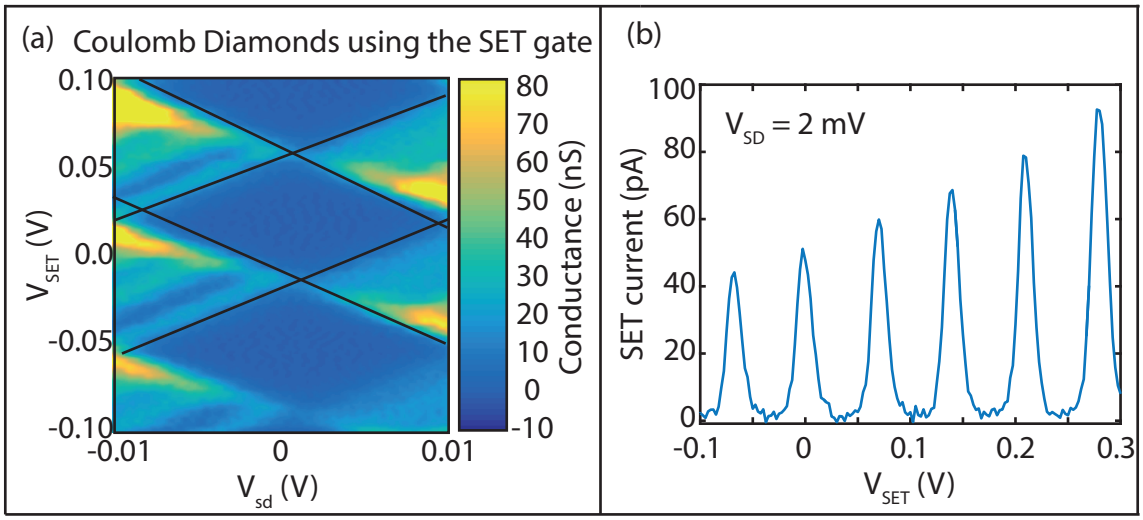

Figure 4.9: Electrical characterization of the ALD-SET device using the in-plane gate voltage V_{SET}. (a) The quantum dot conductance plotted as a function of source-drain bias voltage V_{sd} and the SET gate voltage. Coulomb blockade is observed with a constant charging energy of $\approx 7.748 \pm 0.0683$ mV. (b) Coulomb peaks are measured in this experiment by varying the gate voltage for a fixed source drain bias of 2 mV.

dition of Coulomb blockade is referred to as the charging energy E_c of the quantum dot. Another possible mechanism for tuning the energy levels of the SET island is to capacitively influence the electrochemical potential energy of the SET quantum dot by applying voltages on the SET gate. The influence of the in-plane SET gate on the quantum dot island is calculated using a coupling term, known as the lever arm (α), which calculates the effectiveness of the gate electrode in tuning the energy of the quantum dot. Figure 4.9 (a) shows a 2D surface plot obtained by sweeping the source drain bias for varying gate voltages. The diamond pattern drawn using black lines depicts an area of suppressed conductance and zero current flow. Figure 4.9 (a) is also commonly referred as the Coulomb diamond plot. The charging energy E_c, of the SET island was calculated from Figure 4.9 (a) by measuring the voltage that corresponds to the onset of current on the source-drain bias and is $\approx 7.748 \pm 0.0683$ mV. Source-drain current measurements show regular oscillations known as

coulomb oscillations (or coulomb peaks) shown in Figure 4.9 (b) for a fixed source-drain bias of 2 mV. The gate lever arm is calculated by dividing the charging energy by the width of the coulomb diamond (measured along the SET gate voltage axis) $\alpha_{SET} = E_c/E_{add}$. Using Figure 4.9 (a) and (b), the gate lever arm for the in-plane SET gate α_{SET} is calculated to be ≈ 0.107.

Due to the small size of the SET island, it is very sensitive to the electrostatic environment around it. Therefore, the presence of any charge traps or a small cluster of donors (containing a few phosphorus atoms) influences the behavior of the quantum dot and this is usually visible in the coulomb peaks. This sensitive behavior forms the backbone of the underlying charge sensing operation used widely for sensing and reading out the spin state of an electron [68, 63]. One way to determine the stability of the SET quantum dot device is to take a measurement where the same gate voltage range (covering one or more coulomb peaks) is scanned multiple times producing a map where noise and drift inherent in the system can be observed. A device stability map of the quantum dot device with a Al_2O_3 layer is shown in Figure 4.10 (a) where for a fixed source drain bias of 5mV, the in-plane gate voltage V_{SET} is swept between 0.1 V to 0.2 V locking onto two Coulomb peaks and then scanning repeatedly for 12 hours in the same gate voltage direction. Figure 4.10 (a) shows a waterfall pattern where the drain current through the SET is plotted against the gate voltage for all the traces taken within the 12 hours. To determine the stability of the device during this measurement, the position of both the peaks in gate voltage over the entire duration of the experiment is calculated. Figure 4.10 (b) shows the location of the first peak on the gate voltage axis during the entire

measurement and similarly, Figure 4.10 (c) shows the location of the second peak on the gate voltage axis. Figure 4.10 (d) plots the difference between the two peaks on the gate voltage axis.

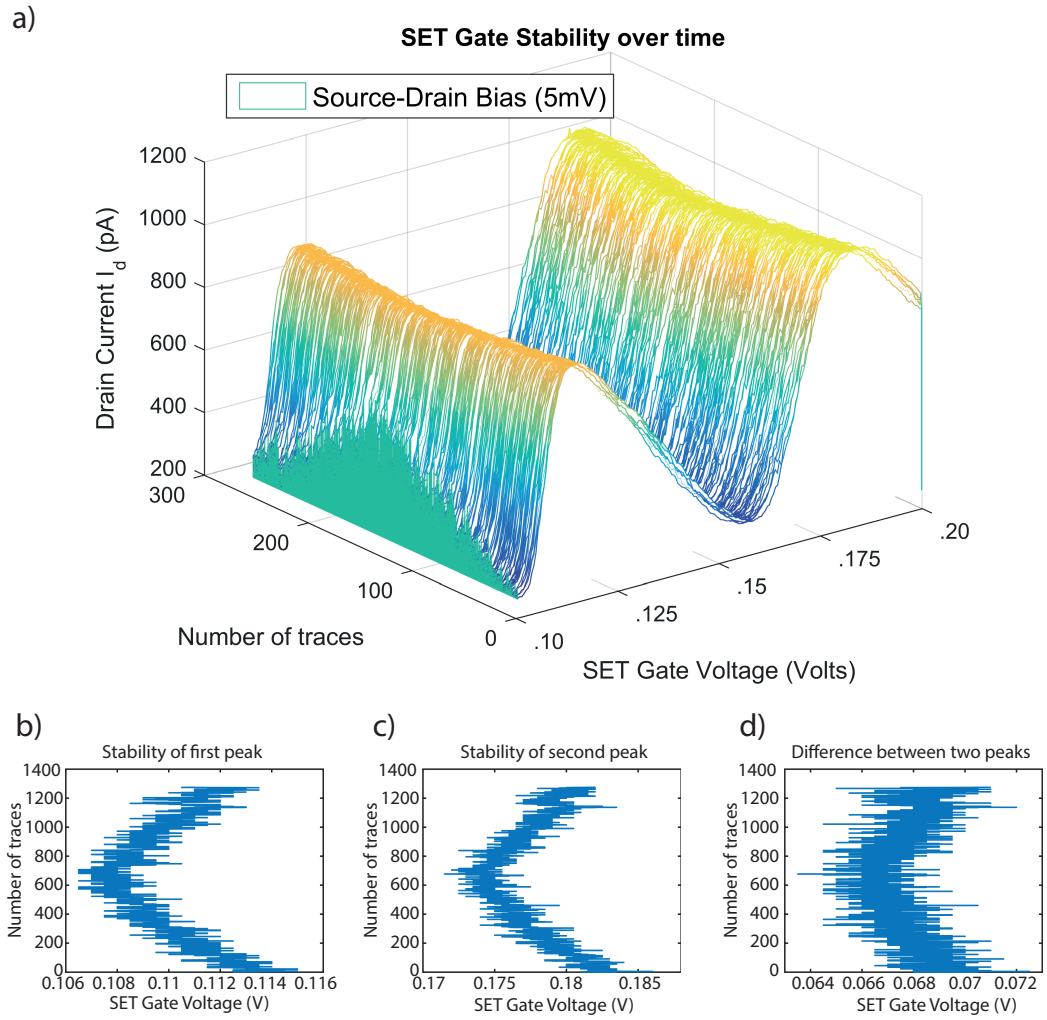

Figure 4.10: Stability of SET with the in-plane gate. (a) Waterfall pattern showing the quantum dot stability of the SET gate. This is plotted by sweeping the in-plane gate voltage for a source-drain bias of 5mV and repeating the measurement for 12 hours. (b) Location of the first coulomb peak for a given SET gate voltage over the entire map. (c) Location of the second coulomb peak for a given SET gate voltage over the entire map. (d) Difference between the location of the first and the second peak over the entire map.

To analyse the stability plot shown in Figure 4.10 (a), the mean position of the peak on the gate voltage axis is calculated and then the spread in the peak position

is provided by 2 σ (standard deviation) across the mean position. Calculating 2σ gives an indication of the noise associated in the system and it is also useful in providing information about the shift in the Coulomb peak position from the mean value throughout the measurement. Additionally, it is also essential to compute the total spread in the Coulomb peak shift i.e. minimum vs the maximum position on the gate voltage. This term will be referred to as $\triangle$. After analyzing the data shown in Figure 4.10 , $2\sigma_1$ for the first peak is 3.2mV. Similarly, for the second peak $2\sigma_2$ is 4.8mV. Whereas, $\triangle_1$ for the first peak is 8.5mV and 12.5mV for the second peak. Finally, $2\sigma_{1-2}$ the difference between the two peaks is 2.6mV and $\triangle_{1-2}$ is 8.5mV. This analysis presented here is the first of its kind and determines the stability of the system observed by looking at absolute values for σ and $\triangle$. If after the top gate incorporation the values obtained are lower, this means that the system is more stable and if the values obtained are higher, then the system is less stable.

4.2.2.2 Electrical Characterization of the SET with a top gate patterned on an Al_2O_3 dielectric

After studying the transport properties of the in-plane gated SET quantum dot device with $\approx$ 28 nm thick layer of Al_2O_3, the device was pulled out from the Helium dewar. In order to test the effectiveness of the ALD layer as a dielectric, a top gate was patterned over the planar SET as the next logical step. Before, patterning the top gate, all the bonds were ripped off from the PCB board and the device was unglued with acetone. The device was then cleaned using acetone and IPA. In order to accomplish patterning of the top gate, the sample was first spin coated with PMMA as a resist mask and then the top gate pattern was lithographically

transferred using EBL. After development of the resist mask, Ti(5 nm) and Au(80 nm) were deposited on the patterned top gate area. Lift off was then performed using NMP and the device was glued on the PCB board and bonded again using an Al wedge bonder. An SEM image shown on the right in Figure 4.11 contains ohmic contacts similar to the ones shown in Figure 4.5 (c) along with the top gate. Using the markers encircles in red, a yellow bounded dashed box is drawn to serve as an aid for accurately determining the position of top gate. It is evident from the image that the positioning of the top gate (1.5 μm wide) is directly on top of the patterned planar nanostructures as indicated using the SEM image.

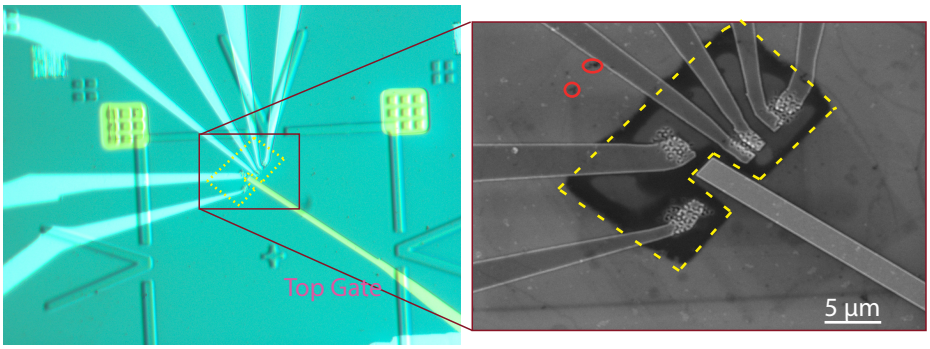

Figure 4.11: Optical (left) and SEM (right) image of the patterned top gate along with the ohmics for the SET quantum dot device. The dashed yellow box in the SEM image on the right is drawn to simply aid in determining the precise placement of the top gate over the the dielectric using the red encircled features as markers.

Previously, the SET quantum dot island was probed using the STM patterned in-plane SET gate. Now, with the integration of the Al_2O_3 layer deposited using ALD, a top gate patterned using electron beam lithography can also be utilized. With the introduction of this top gate, the transport properties of the SET quantum dot are studied once again with an additional tuning knob. Conductance measurement showing Coulomb diamonds were performed in this case for both varying, (i) the SET in-plane gate and, (ii) the top gate voltage as shown in Figure 4.12. Figure 4.12

(a) shows the quantum dot conductance and Figure 4.12 (b) shows coulomb peak oscillations obtained using the planar SET gate. The charging energy of ≈7.335 ± 0.0346 meV was calculated in agreement with the previous measurements. The SET gate lever arm computed using 4.12 (a) and (b) came out to be $\alpha_{SET} \approx 0.046$, reduced from the previous case ($\alpha_{SET} = .107$) where no top gate was patterned. It is noted that patterning a top gate over the planar quantum dot structures reduces the overall tunability of the SET gate which leads to a lower SET gate lever arm. This is the case because the top gate has a larger overlap with the STM patterned nanostructures as compared to the in-plane SET gate and therefore behaves as a parallel plate capacitor. This behaviour is expected as the tunability of the quantum dot island is now more strongly influenced by the top gate due to its larger size and proximity (encapsulation 45-50 nm + 28 nm ALD = ∼ 73-78 nm) to the planar nanostructures as compared to the in-plane SET gate (∼ 85 nm away).

Coulomb diamond measurements for varying top gate voltages are shown in Figure 4.12 (c) and (d). Figure 4.12 (c) shows the 2D conductance plot of the quantum dot as a function of source drain bias voltage and varying top gate voltage (with SET gate voltage set to 0 V). It is clearly visible from the conductance measurements that the ability of the top gate to tune the SET quantum dot island is much more pronounced than the planar STM patterned gate. The charging energy obtained from the height of the diamonds from Figure 4.12 (c) is ≈7.275 ± 0.0504 meV, as expected. Coulomb oscillations as a function of the top gate voltage are shown in Figure 4.12 (d) and the lever arm obtained for top gate using 4.12 (c) and (d) is ≈ 0.278. The computed top gate lever arm is roughly a factor of six greater as com-

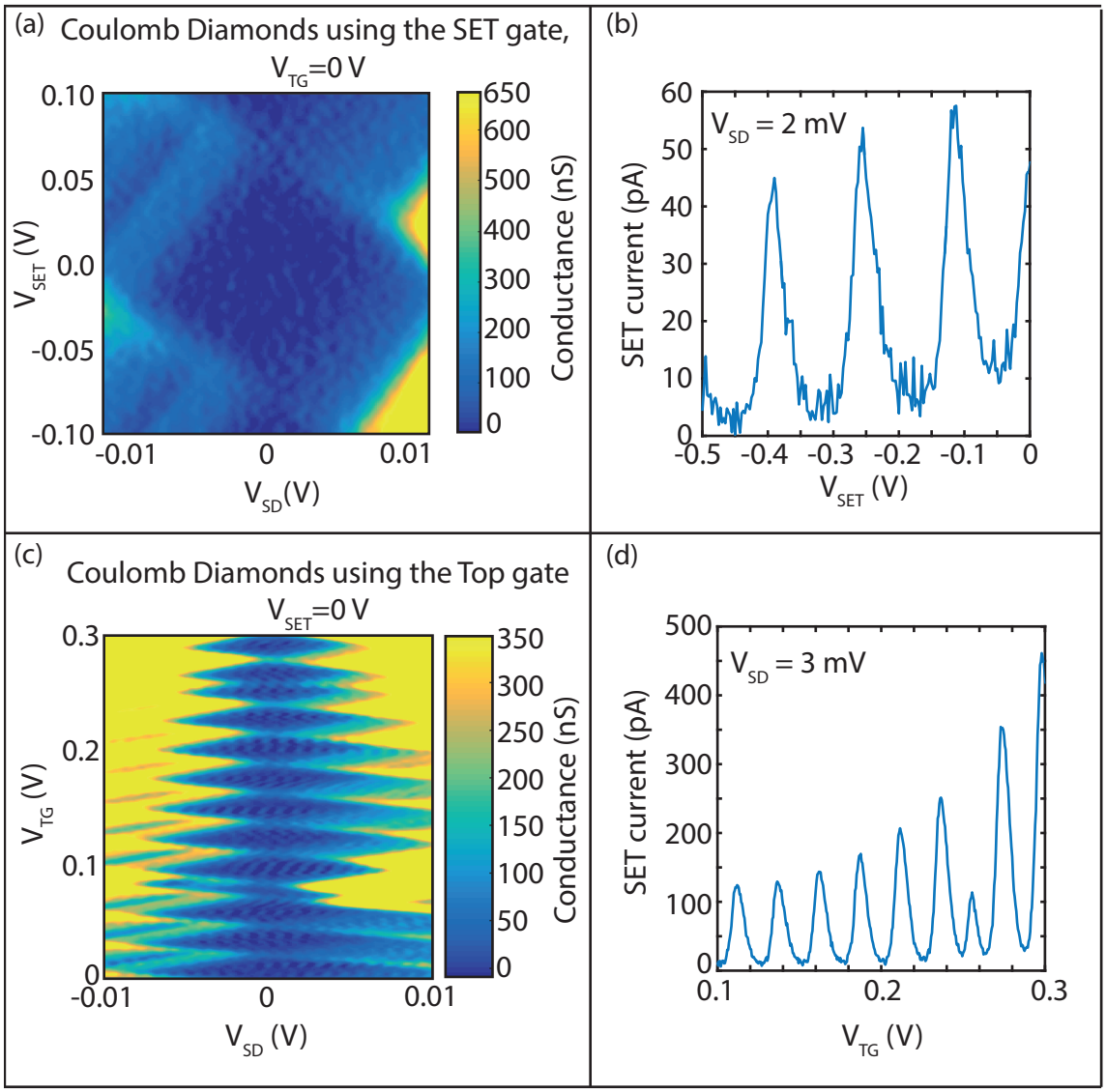

Figure 4.12: (a) Conductance of the quantum dot plotted as a function of source-drain bias and SET gate voltage. A charging energy of $\approx 7.335 \pm 0.0346$ meV is observed. (b) Coulomb peaks are measured for a source drain bias of 2 mV (with top gate voltage of 0 V). (c) Quantum dot conductance plotted as a function of source-drain bias and Top gate voltage with in-plane gate voltage at 0 V. A charging energy of $\approx 7.272 \pm 0.0504$ meV is observed. (d) Coulomb peaks are measured for a source drain bias of 3 mV.

pared to the in plane SET gate because of its large size (~ 1.5 μm wide) and higher capacitive coupling as compared to the planar nanostructures, where the capacitive coupling is much smaller in the only monolayer thick in-plane gates.

Before pronouncing the top gate patterned on a dielectric layer deposited using

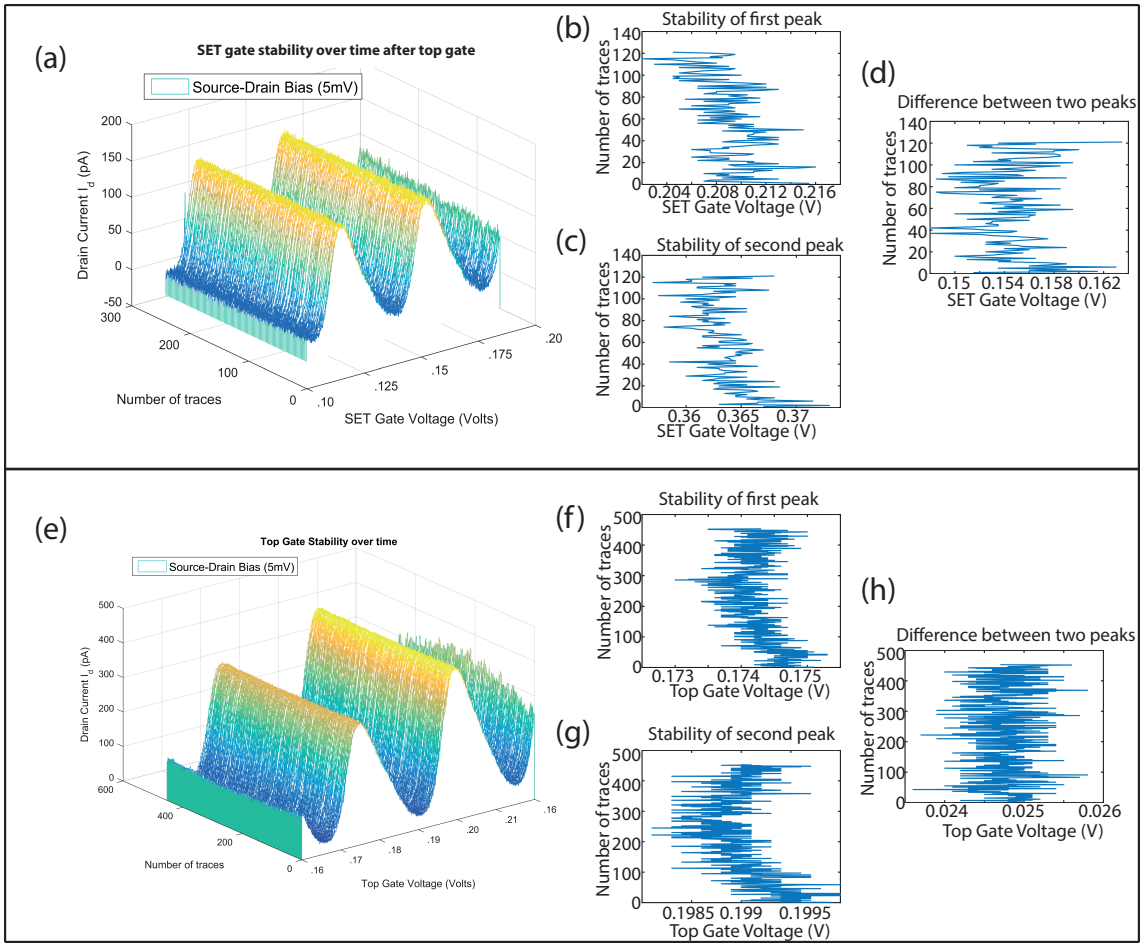

Figure 4.13: Stability of SET and Top gate. (a) Waterfall pattern showing the quantum dot stability of the SET gate. This is plotted by sweeping top gate voltage for a source-drain bias of 5mV and repeating the measurement for 4 hours. (b) Location of the first coulomb peak for a given SET gate voltage over the entire map. (c) Location of the second coulomb peak for a given SET gate voltage over the entire map. (d) Difference between the location of the first and the second peak over the entire map. e) Waterfall pattern showing the quantum dot stability of the top gate. This is plotted by sweeping the top gate voltage for a source-drain bias of 5mV and repeating the measurement for 12 hours. f) Location of the first coulomb peak for a given top gate voltage over the entire map. g) Location of the second coulomb peak for a given top gate voltage over the entire map. h) Difference between the location of the first and the second peak over the entire map.

ALD a success, stability measurements must be performed. Stability plots were repeated once again for the SET gate to determine any negative influence that might have occurred after patterning the top gate (with the top gate voltage set to 0 V). Figure 4.13 (a-d) shows the SET gate stability recorded over a period of 4

hours. Similar analysis as performed earlier is repeated for two peaks scanned over a constant gate voltage range visible in Figure 4.13 (a). Analysis of the first peak revealed a $2\sigma_1 = 5.2$ mV and $\triangle_1 = 14$ mV, for the second peak $2\sigma_1 = 5.2$ mV and $\triangle_2 = 16$ mV, and for the difference between the two peaks, $2\sigma_{1-2} = 6.2$ mV and $\triangle_1 = 15.5$ mV. This trend shows that all the values show similar stability as obtained earlier when no top gate was patterned.

Stability measurements using the top gate were also measured as shown in Figure 4.13 (e-h) (for an SET gate voltage of 0 V). Two peaks were locked on for a given range of top gate voltages as depicted in Figure 4.13 (e) and the measurement was repeated for 12 hours. Stability analysis for the top gate measurements revealed the most stable gating operation shown for the top gated ALD deposited quantum dot device. For the first peak as shown in Figure 4.13 (f), $2\sigma_1 = 0.75$ mV and $\triangle_1 = 2.3$ mV. For the second peak, $2\sigma_2 = 0.66$ mV and $\triangle_2 = 1.9$ mV as shown in Figure 4.13 (g). For the difference between the two peak positions, $2\sigma_{1-2} = 0.74$ mV and $\triangle_{1-2} = 2.2$ mV as shown in Figure 4.13 (h).

A table summarizing all the relevant stability parameters computed before and after the top gate are shown in Table 4.2.

Noise parameters	SET gate (no top gate)	SET gate (top gate voltage 0 V)	Top gate ($V_{SET} = 0$ V)
$2\sigma_1$	3.2 mV	5.2 mV	0.75 mV
$2\triangle_1$	8.5 mV	14 mV	2.3 mV
$2\sigma_2$	4.8 mV	5.2 mV	0.66 mV
$2\triangle_2$	12.5 mV	16 mV	1.9 mV
$2\sigma_{1-2}$	2.6 mV	6.2 mV	0.74 mV
$2\triangle_{1-2}$	8.5 mV	15.5 mV	2.2 mV

Table 4.2: Summary of noise parameters computed for the ALD-SET device.

4.2.3 Comparison of capacitance modelling with results

After performing the electrical characterization of the ALD patterned SET quantum dot device in two different cases: with and without top gate, the results are compared with the modelling performed earlier in Section 4.2.1.

Theoretical prediction from COMSOL			
	Charging Energy	SET Gate Lever arm	Top Gate Lever arm
ALD SET without top gate	9.1 meV	0.1417	n/a
ALD SET with top gate	9 meV	0.0674	0.4382
Experimental values obtained from measurement			
	Charging Energy	SET Gate Lever arm	Top Gate Lever arm
ALD SET without top gate	7.748 meV	0.107	n/a
ALD SET with top gate	7.305 meV	0.046	0.278

Table 4.3: Theoretical values obtained after solving the capacitance matrix generated from COMOSL modeling. And, experimental values obtained after measuring the quantum dot device for both the cases, without top gate and with top gate.

The major observations from the comparison are as follows:

1. $E_c \sim$ is slightly less than modelled using COMSOL, but within reasonable limits (±30%) as shown earlier as well (using FASTCAP model which is similar to COMSOL) [26]. Additionally, similar to the COMSOL modelling no significant impact due to the presence of the top gate on the charging energy is seen.

2. The absolute values of the SET gate lever arm do not match, but are within reasonable limits (±30%), as expected from COMSOL modelling [26].

3. The ratio of the top gate lever arm to the SET gate lever arm is comparable to both modelling and experiments. It has been shown previously that whilst absolute values are not identical between the model and the experiments, the ratios obtained are same [64].

4.2.4 Dynamic frequency response of the top gate

One of the principal requirements of a universal quantum computer is the implementation of one and two qubit logic gates. A one qubit logic gate in electron spin based systems can be performed by electron spin resonance. Similarly, for performing two qubit logic gates, exchange coupling of two electron spins is necessary. Inherent in both these operations is the ability to control the electron spins with high frequency signals ($\sim$ few GHz range) for realizing a universal quantum computer. Recently, GHz control of the planar gates patterned using STM fabrication was shown, demonstrating the nanosecond control needed for performing key quantum gate operations in a silicon based quantum computer [133]. However, the results presented in this thesis represent the first instance of patterning a top gate on Al_2O_3 dielectric over a STM-patterned device and as a consequence the frequency response of the top gate voltage is investigated. It is worth noting that all the measurements are performed at 4.2 K by applying square wave pulses to the top gate. Two things to keep in mind with this kind of measurement are: the potential interference with the SET quantum dot current, and severe attenuation of the applied frequency above 1 MHz due to limitations in the loom wire.

A square wave pulse of varying frequency was applied to the top gate along in addition to the top gate voltage to probe the frequency response. A Tektronic AFG3022 C waveform generator is used for applying square pulses of varying frequency. First a square wave pulse at 1 kHz with varying amplitude from 10-30 mV_{pp} was applied with the top gate voltage to observe the doubling of the coulomb peaks as shown in Figure 4.14 (a). For a square wave amplitude of 10 mV_{pp}, no

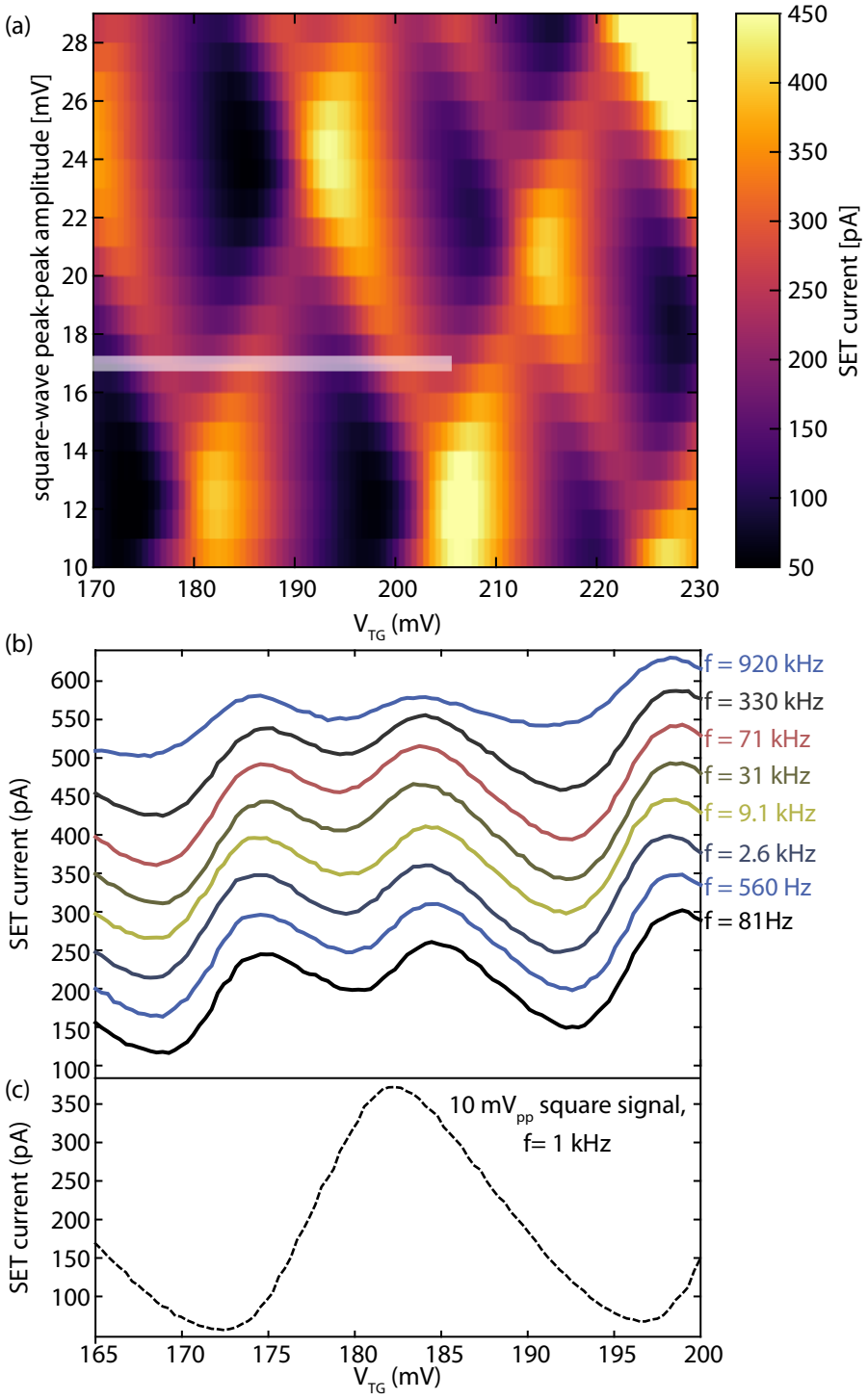

Figure 4.14: Dynamic frequency response of the top gate. (a) Doubling of the coulomb peak is observed after applying a 1 kHz square wave pulse with varying amplitude on the top gate. (b) Frequency response of the square wave pulses up to 920 kHz shown for square wave amplitude of 17mV_{pp}. (c) A single coulomb peak is shown at $V_{TG} \sim 180$ mV with a square wave amplitude of 10mV_{pp} and frequency 1 kHz.

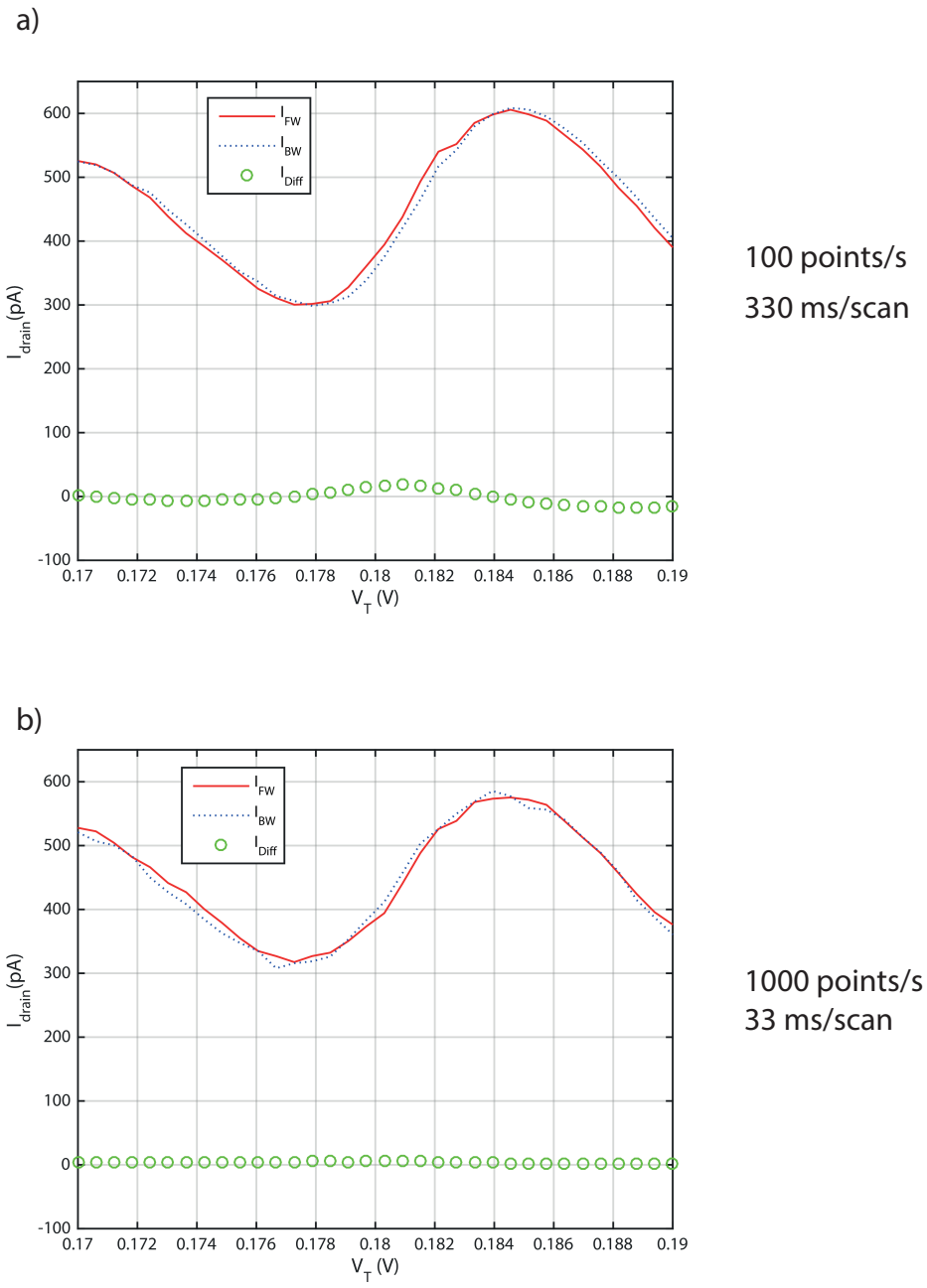

Figure 4.15: Forward and backward drain current shown using red and dashed blue lines is recorded for sweeping the top gate voltage back and forth once. Difference between the mean values of the forward and backward current (obtained after continuously scanning the gate voltage forward and backward) is shown using green bubbles. (a) Scan obtained for a data rate of 100 points/s (measured for 1 hour). (b) Scan obtained for a data rate of 1000 points/s (measured for 1 hour).

doubling is observed as shown in Figure 4.14 (c) because the voltage amplitude is not enough to separate the peaks. However, for a square wave pulse amplitude of 17 mV_{pp} and above shown above the white line in Figure 4.14 (a), doubling is clearly visible. Therefore, 17 mV_{pp} is chosen as the square wave pulse amplitude and the frequency is now varied from 81 Hz to 1 MHz. A robust top gate should show behaviour independent of all the frequencies probed in this measurement. As seen in Figure 4.14 (b), no change in the probed frequency response was observed for the top gate voltage. However, a change in the SET current is visible for 920 kHz frequency square wave pulse. This is attributed to the presence of the loom wires used in the 4 K measurement setup as they limit the ability to apply higher frequencies and result in attenuation for the higher frequency signals.

Another powerful method for testing the stability of the electrostatic environment after patterning the top gate is to measure the SET current (drain current) by sweeping the top gate voltage forwards and backwards. Then, calculating the difference between the forward and the backward drain current provides information about any hysteresis present in the system. A top gate voltage range is selected for locking onto one Coulomb peak and sweeping the top gate voltage forwards and backwards continuously for 2 output data rates: acquiring 100 points/s (measured for 1 hour) and acquiring 1000 points per/s (measured for 1 hour) as shown in Figure 4.15 (a) -(b). In these two plots, forward and backward drain current is marked using red and dashed blue lines respectively. The difference between the mean value of all the forward and backward drain currents is calculated and plotted using green bubbles. After carefully analysing all the data presented for the data rates of 100

points/s and 1000 points/s no hysteresis was found because and green bubble line is sitting at zero.

4.2.5 Effective gate range of the in-plane and surface gates

The effective gate range is determined by performing gate leakage measurement for the SET quantum dot device. These measurements show the robustness of the device geometry in field emission regime. Leakage current starts flowing when the barrier defined by the device geometry is overcome by the applied voltage. Gate leakage measurements were carried out for SET gate as shown in Figure 4.16 before patterning the top gate. Gate leakage occurs on the positive side at $\sim$ 1.7 V and on the negative side at $\sim$ -1.1 V. Thus, the effective gate range for the SET gate is -1.1 V to +1.7 V. Gate leakage measurements for the in-plane SET gate after patterning the top gate revealed a slightly reduced gate range of -0.9 V to 1.7 V. The top gate did not show any leakage from -4 V to 4 V and is plotted in Figure 4.16 (b). The gate range obtained for the top gate with Al_2O_3 dielectric here is similar to Si/SiGe heterostructures [134].

	V_{SET} SET (no top gate)	V_{SET} SET (with top gate)	V_{TG}
α	0.107	0.046	0.278
E_C	7.748 $\pm$ 0.0683 meV	7.335 $\pm$ 0.0346 meV	7.2722 $\pm$ 0.0504 meV
Gate range	-1.1 V to 1.7 V	-0.9 V to 1.7 V	-4 V to 4 V
Stability ($2\sigma_1$&$\triangle_1$)	3.2 mV&8.5 mV	5.2 mV&14 mV	0.75 mV&2.3 mV
Stability ($2\sigma_2$&$\triangle_2$)	4.8 mV&12.5 mV	5.2 mV&16 mV	0.66 mV&1.9 mV

Table 4.4: Summary of all the experimental parameters obtained from the electrical characterization of the SET quantum dot device before and after patterning the top gate.

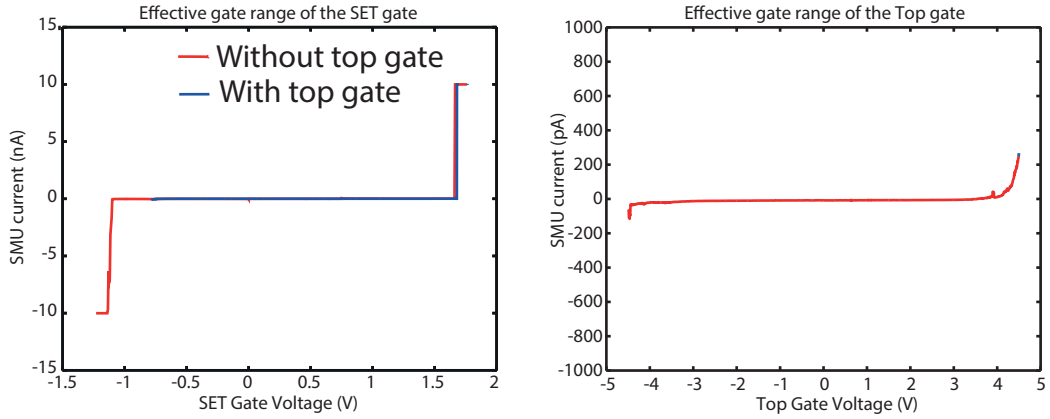

Figure 4.16: Gate leakage curves for the SET gate and the top gate. a) SET gate range before patterning the top gate. b) Effective gate range of top gate.

Table 4.4 summarizes all the relevant parameters obtained after measuring the SET quantum dot with the Al_2O_3 dielectric in two cases: without a top gate and with a top gate. The major observations are:

1. Successful integration of an 80 nm Al top gate on a 28 nm of Al_2O_3 dielectric was demonstrated.

2. The charging energy E_C of the SET quantum dot reduces slightly from no top gate to a device with a top gate. This follows the prediction made in the COMSOL model.

3. The patterned top gate has a significant impact on the in-plane gate lever arm α_{SET}, reducing it by $\sim$ 6.1 %. Moreover, a large lever arm of top gate compensates for the loss suffered by the in-plane gate.

4. The effective gate range of the SET gate is slightly reduced from -1.1 V to 1.7 V to -0.9 V to 1.7 V by the presence of the top gate. However, the top gate has a exceptionally large gate range of -4 V to 4 V.

5. The stability of the in-plane SET gate has slightly deteriorated from the ungated to the top gated case.

6. The stability of the top gate is robust with the lowest noise and drift observed for STM-patterned donor devices.

4.3 Integrating a top gate on a 4 quantum dot device

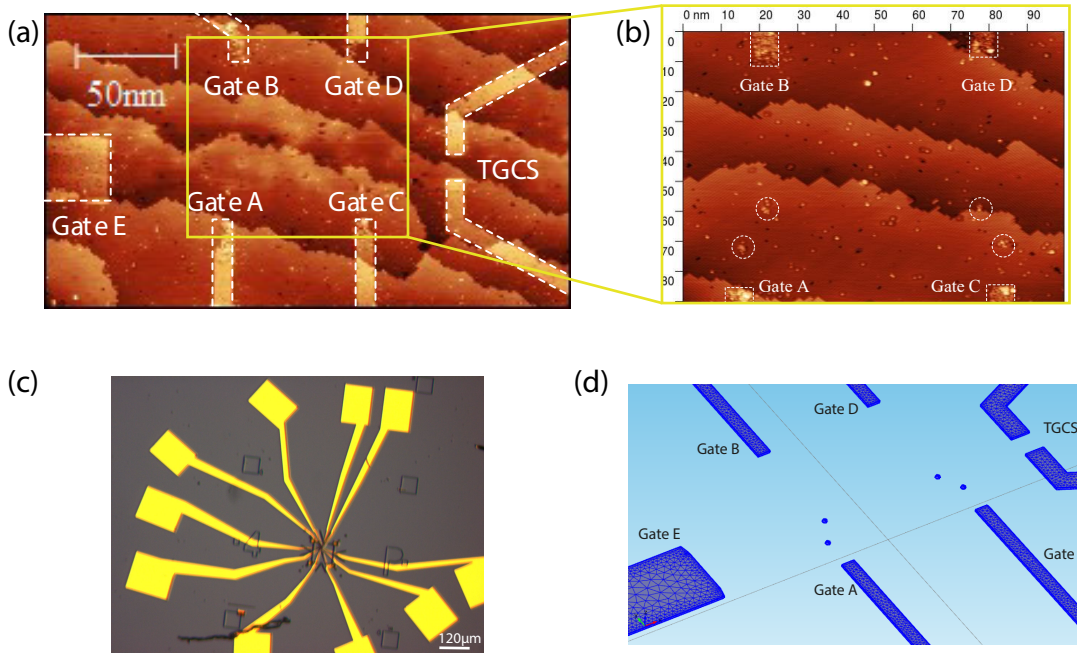

Figure 4.17: 4 STM-patterned donor dots in a coupled singlet-triplet architecture. (a) Overview of the 4-dot device. (b) Close-up of the 4-dot device showing the inner device dimensions containing all the four dots. (c) Optical image showing all the ohmic contacts patterned to establish contact with the buried phosphorus doped nnaostructures. (d) COMSOL model showing the patterned 4-dot device.

Successful operation of the top gate on the SET quantum dot insulated with a dielectric layer of Al_2O_3 paved the way for implementing this technique on a 4 quantum dot device. A 4 quantum dot device consists of 2 capacitively coupled

singlet-triplet qubits as shown in Figure 4.17 (a). The 4-quantum dot device presented here was patterned using STM based lithography as shown in Figure 4.17 (a) and (b). Figure 4.17 (a) shows the overview of device containing five gates and a tunnel gap charge sensor (TGCS). Gate A and Gate C are reservoirs which are used to load the dots, whilst Gate B and Gate D are used to capacitively influence the dots. Gate E is used as a global gate and the TGCS is used for dc-charge sensing. Figure 4.17 (b) shows the inner device structures where four dots are patterned. *Ex-situ* processing of this device was performed according to the standard cleanroom processing recipe for STM-patterned devices as discussed in Section 2.4. Figure 4.17 (c) shows the final step in processing where ohmic contacts are established to connect to the buried phosphorus doped nanostructures. Figure 4.17 (d) shows the COMSOL model of the 4-dot device used to calculate the capacitance matrix.

Given two electron spins across the two quantum dots for one pair of the singlet-triplet qubit, the effective spin states can be described by the singlet-triplet basis:

$$\begin{cases} S_0 = \frac{1}{\sqrt{2}}\left(|\downarrow\uparrow\rangle - |\uparrow\downarrow\rangle\right) \\ T_0 = \frac{1}{\sqrt{2}}\left(|\downarrow\uparrow\rangle + |\uparrow\downarrow\rangle\right) \\ T_- = |\downarrow\downarrow\rangle \\ T_+ = |\uparrow\uparrow\rangle \end{cases} . \tag{4.1}$$

A singlet-triplet qubit uses S_0 and T_0 as the basis states. It forms a promising platform for solid-state quantum computation due to its simple operation (all electrical control) and immunity to common mode magnetic field noise [74, 78]. Singlet triplet device architectures are one of the architectures being pursued actively by the STM fabrication group at UNSW. Entanglement between two singlet-triplet qubits

has already been demonstrated in GaAs/AlGaAs based heterostructures [78].

In a double quantum dot system there are two types of inter-dot electron transitions: even parity and odd parity. In an even parity transition, the two outermost unpaired electrons can be separated individually onto the two dots and brought together into a single dot (such as (1,1)→(2,0)). However, on the odd-parity, one electron simply shuttles across the dots (such as (1,0)→(0,1). One of the major requirements for a singlet triplet type qubit is the presence of an even parity inter-dot transition between an electron exchange coupled double quantum dot. One such device aimed at coupling two singlet-triplet qubits is the 4-quantum dot patterned by the STM and is discussed in this section. This device employs a TGCS [135] to detect charge transitions rather than a SET.

TGCS as a charge sensor

A TGCS requires two leads in a tunnel junction configuration where an applied bias voltage allows current to flow. On application of an electric field, the tunnel barrier is shifted and the current through the tunnel junction is altered. Charge transitions are visible when taking the derivative of the TGCS current [135].

Figure 4.18 shows the measurement set-up used for the 4 quantum dot device. It consists of NIDAQ USB 6363 module which is used for applying voltages on the gate and also for acquiring the TGCS current. SIM 928 voltage sources are also used for applying voltages on the gates.

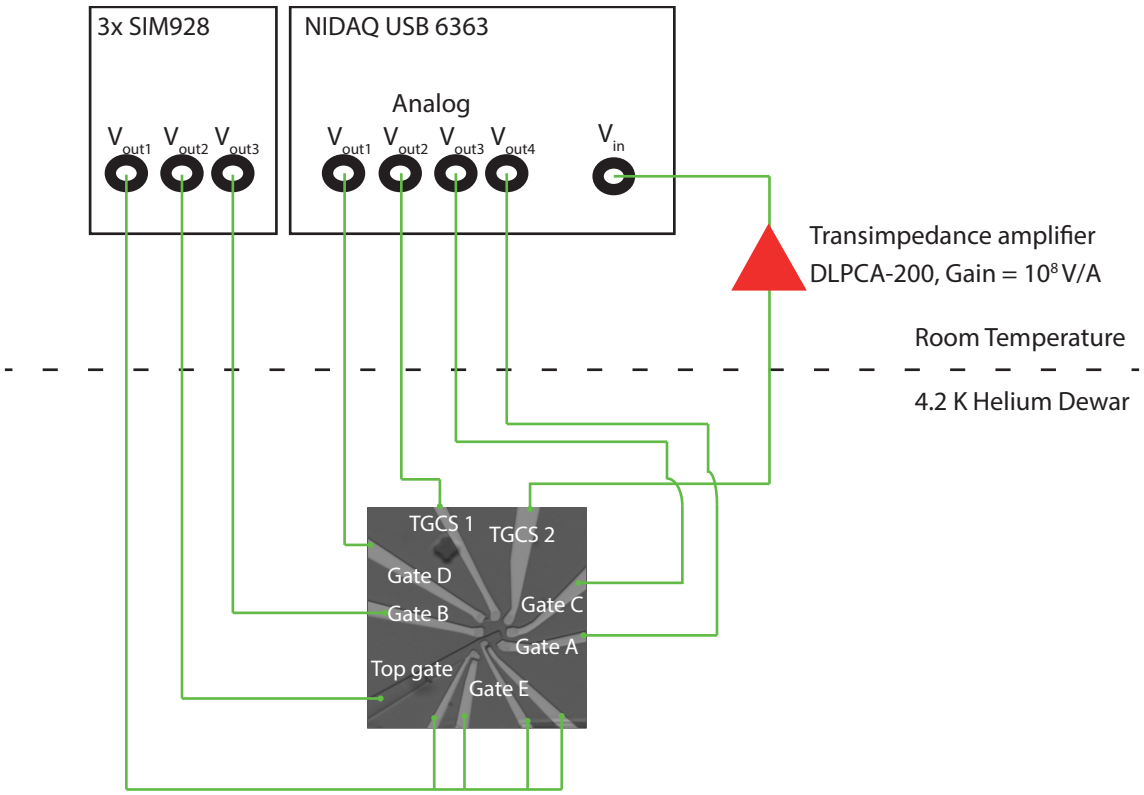

Figure 4.18: Measurement set-up for the 4-dot device primarily consisting of NIDAQ 6363 data acquisition module and SIM928 voltage sources. A Femto DLPCA-200 transimpedance amplifier is used for converting current to voltage and amplifying the TGCS current with a gain of 10^8 V/A.

4.3.1 Device characterization before the top gate

Figure 4.19 shows a gate-gate map with charge transitions from the left pair of quantum dots between Gate and Gate B. These transitions are obtained by varying the voltages on gates A and B. For a singlet-triplet inter-dot transition, when the system is in the ground state, the (0,2) state corresponds to the S_0. However in the equivalent (1,1) state all four basis states are degenerate. To break this degeneracy, one applies a global magnetic field where the new ground state is T_-. A simple demonstration of breaking the degeneracy of the singlet-triplet inter-dot transition is to take a gate-gate map before and after applying the magnetic field. On applying

the magnetic field, the interdot transition should disappear for large magnetic fields because the system remains in the (1,1) T_- state. Two inter-dot transitions (shown in black) are visible in Figure 4.19 at zero magnetic field. Both of these inter-dot transitions are of odd parity, because they did not show any magnetic field variation when measured in a dilution refrigerator and therefore singlet-triplet states could not be accessed on the left hand pair of quantum dots. The device had a limited gate range for gate C due to its proximity to the TGCS and hence no inter-dot transitions were measured on the right hand dot pair.

Left hand dot pair		
	COMSOL Simulation	Experimental results
Bottom dot B slope	5.72	4.92
Top dot A slope	4.74	3.87

Table 4.5: Comparison of slopes (as shown in Figure 4.19) obtained from COMSOL simulation and from experimental results.

To confirm that the transitions are from the patterned quantum dots, the device was modeled using COMSOL to theoretically obtain the slope of the charge transitions. Table 4.5 shows slopes of the quantum dot obtained from experimental and from COMSOL simulation. It is worth mentioning that the experimental results were obtained when gate C was floating. This places some unknown uncertainty on the measured values from the experimental results, because the voltage on Gate C was unknown and this has a influence on calculating slopes for the left quantum dot pair.

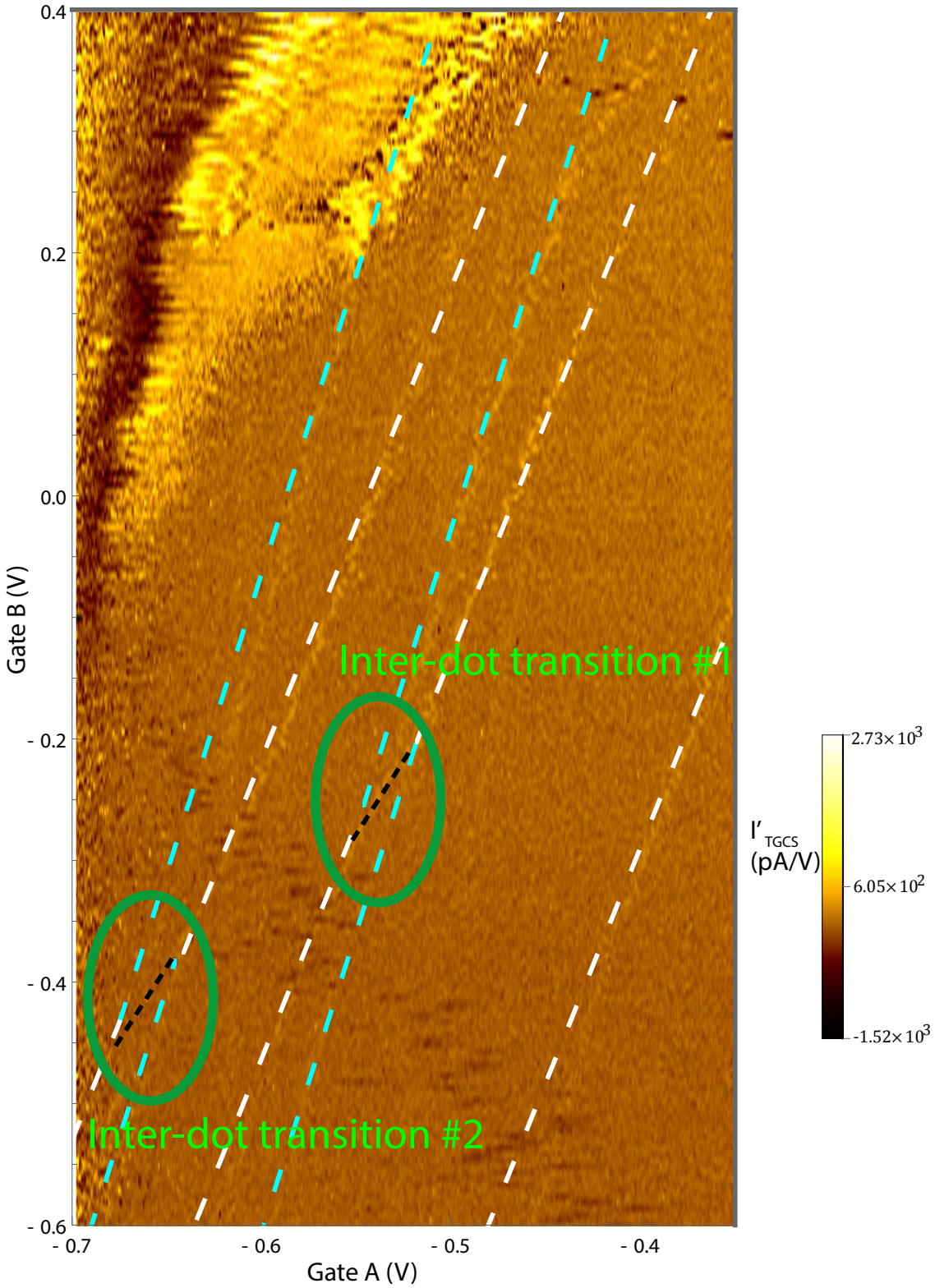

Figure 4.19: Gate-Gate map of the charge transitions from the left hand pair of dots taken by varying gate voltages A and B. Green circles highlight the position of the two inter-dot transitions. Cyan and white color lines have different slopes because they represent the transitions from the bottom and top dots, respectively. The black lines indicate the interdot transitions that were visible when this device was measured in dilution refrigerator.

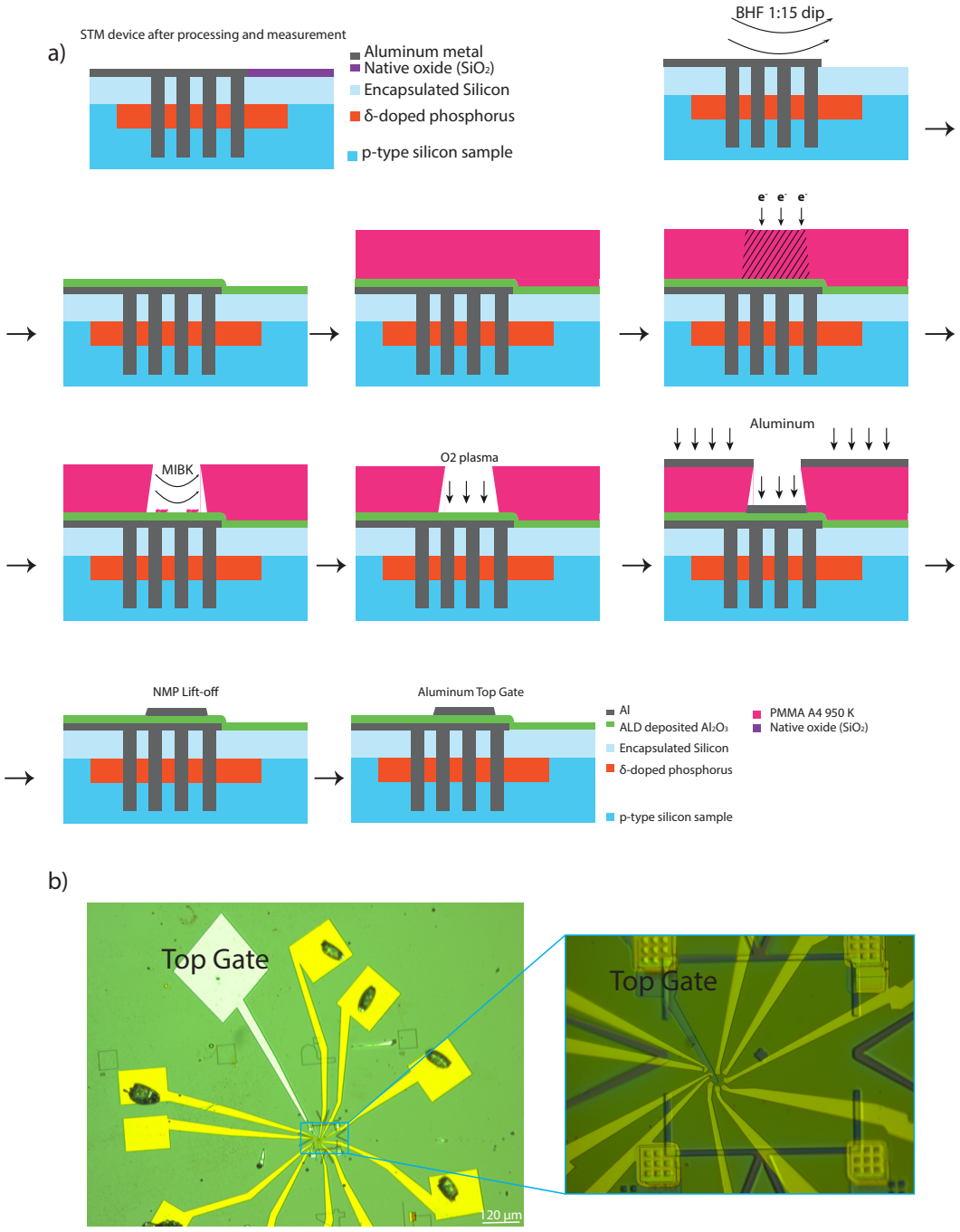

Figure 4.20: Integration of top gate on a 4 quantum dot STM patterned device . (a) Full processing recipe for patterning a top gate over STM fabricated devices. Note: These devices have native oxide present over the inner device structures, which is later removed when a BHF dip is performed. (b) Optical image showing the top gate along with the ohmics with the close-up image confirming that the position of the top gate is directly on top of the inner device structures which is crucial.

4.3.2 Device characterization after patterning the top gate

Since the 4-dot device presented above did not have any singlet-triplet type transitions in the available gate range, it was decided to investigate patterning a top gate to control the inter-dot transitions and determine whether additional inter-dot transitions could be accessed with a large gate range. The design of planar STM-patterned nanostructures often compromise the maximisation of the lever arms (by moving the gates closer to the dots) with a larger gate range (which requires the gates to move further away). The ALD SET device has already shown that a top gate can be used to apply up to ±4 V to the STM patterned device without leakage while retaining a large lever arm. Thus, the successful operation of the surface gated SET device motivated a top gate to be patterned on the 4-dot device.

Patterning a top gate on an already processed STM-fabricated device was achieved by depositing Al_2O_3 using ALD and then patterning a top gate over the inner device structures as shown using the flow chart recipe in Figure 4.20 (a). For depositing Al_2O_3, the device is subject to a BHF 1:15 treatment for 8 seconds to remove any native oxide present on the surface. The sample is then rinsed with DI water for 7 seconds before being transported in a petri-dish for depositing the ALD dielectric. The recipe shown in Table 2.1 is used to grow Al_2O_3 on the 4-dot device. After depositing ≈ 28 nm of Al_2O_3 at 200 °C, the top gate is patterned using EBL by utilizing the optimum dose rate of 220 $\mu C/cm^2$ as shown in Section 3.3. An 80 nm Aluminum layer is evaporated. Lift-off is performed using NMP. The full process is shown in Figure 4.20 (a) and the optical image of the device after patterning the top gate is shown in Figure 4.20 (b). The 4-dot device was then glued to the PCB

and bonded using Al wedge bonder. The device was then remeasured at 4.2 K.

Left hand dot pair		
	COMSOL Simulation	Experimental results
Bottom dot B slope	11.20	11.07
Top dot A slope	8.62	6.42

Table 4.6: Comparison of slopes (as shown in Figure 4.21) obtained from COMSOL simulation and from experimental results after patterning the top gate.

Figure 4.21 now shows the gate-gate map of the left hand dot pair after patterning the top gate. This plot was generated by stitching three gate maps taken over varying top gate voltages of 0 V, 3.0 V and 3.5 V. It can now be seen that there are two new inter-dot transitions visible in the gate-gate map due to increased gate range offered by the top gate. Inter-dot transitions #1 and #2 that were visible before the top gate was patterned were of odd parity as they did not show any singlet-triplet behavior. The top-right plot corresponds to the top gate voltage of 0 V (similar to gate-gate map shown in Figure 4.19). However, after patterning the top gate two new inter-dot transitions, #3 & #4 (shown with purple circles) became accessible as shown in Figure 4.21. The addition of the top gate makes the charge transition slopes higher thus moving the anti-crossings further apart vertically in gate space (as confirmed from COMSOL simulations as shown in Table 4.6). However, the large gate range offered by the top gate allows accessing additional charge transitions which were previously inaccessible due to limited in-plane gate range. Moreover, inter-dot transition #4 is of even parity because there are two concurrent inter-dot transition (#1 & #2) next to it that are of odd parity. Similarly, it is evident that the inter-dot transition #3 is of odd-parity. Therefore, using the top gate for the the 4-dot device has made the coveted singlet-triplet transition accessible due to its

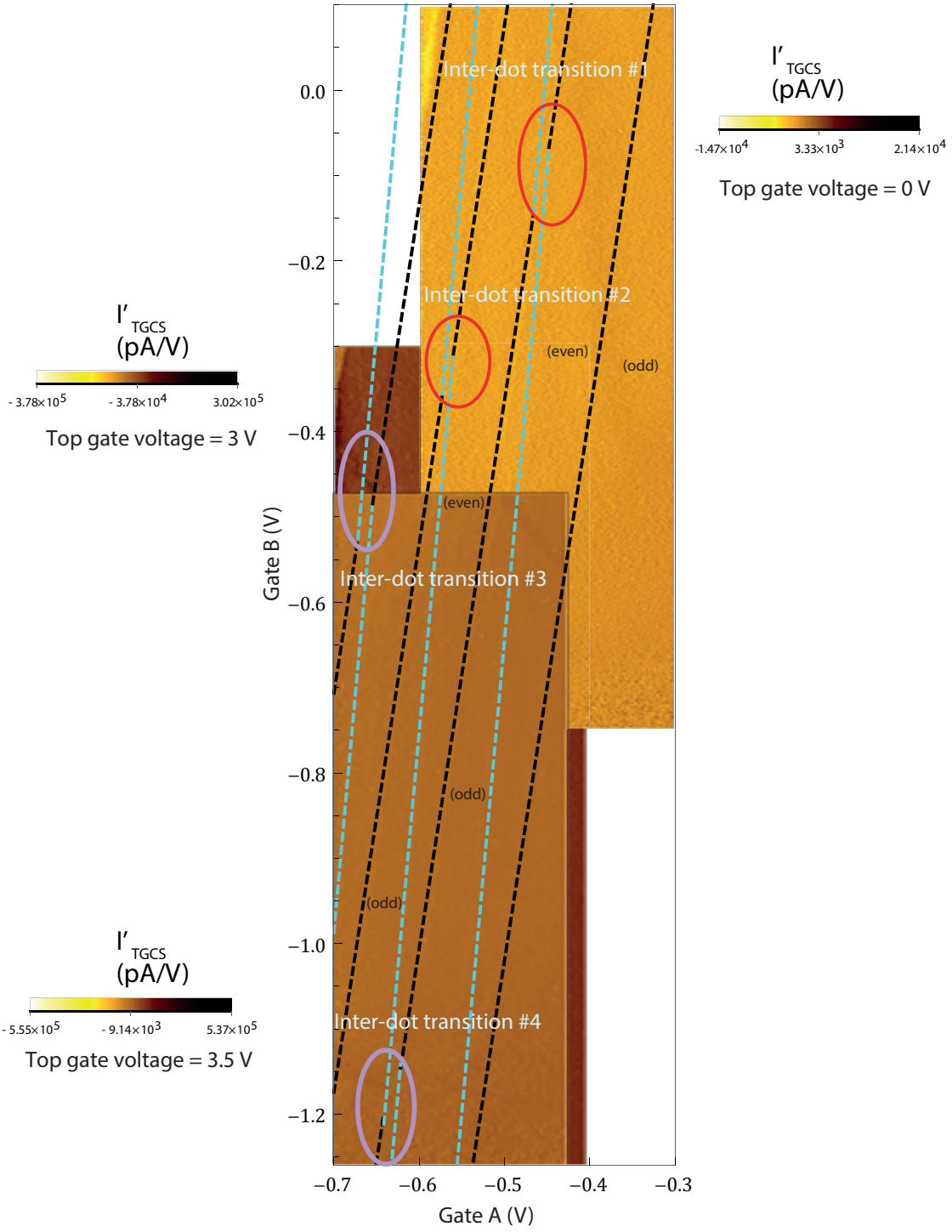

Figure 4.21: Gate-Gate map of the left hand dot pair taken by stitching three separate gate maps sweeping gate voltages A and B. The top gate voltages for the maps from top to bottom were 0.0 V, 3.0 V and 3.5 V, respectively. Red circles highlight the position of the inter-dot transitions #1 and #2 that were visible before the top gate was patterned. Purple circles highlight the position of two new inter-dot transitions, namely #3 and #4 which were not visible before. Cyan and black lines indicate bottom and top dots, respectively.

enhanced gate range.

Finally, the effective gate range was calculated for all the gates present in the 4-dot device after patterning the top gate. A comparison was made between the effective gate range observed before and after the top gate as shown in Figure 4.22 (a). The effective gate range for all the gates for the 4-dot device before patterning the top gate are shown using blue in Figure 4.22 (a). It should be noted that the TGCS and Gate C leaked to each other due to close proximity and therefore had a lower effective gate range even before patterning the top gate. No significant change in the effective gate range was observed for all the gates in the 4-dot device after patterning the top gate shown using red in Figure 4.22 (a), apart from TGCS and Gate C where the effective gate range reduced by $\sim$ 400 mV. However, this lower leakage range did not prove detrimental in measuring the inter-dot transitions through the TGCS due to its robust operation within the limited gate range. Additionally, the top gate operation was observed between -4 V to +4 V and no leakage occurred even for such extreme voltages. Although, it should be noted that the trend visible for the effective top gate range is due to the finite resistance of $\sim$ 50 GΩ. This is not a sign of leakage, but is rather a consequence of finite insulation of loom wires to ground or the internal resistance of the source measure unit used to determine the effective gate range.

In summary, successful implementation of a Al metal top gate (80 nm) on top of a $\approx$ 28 nm thick Al_2O_3 layer is demonstrated for a 4 quantum dot device. The effective gate range of the in-plane gates remained the same apart from Gate C and TGCS where the range reduced by $\sim$ 50 ⁒. The effective gate range of the top gate

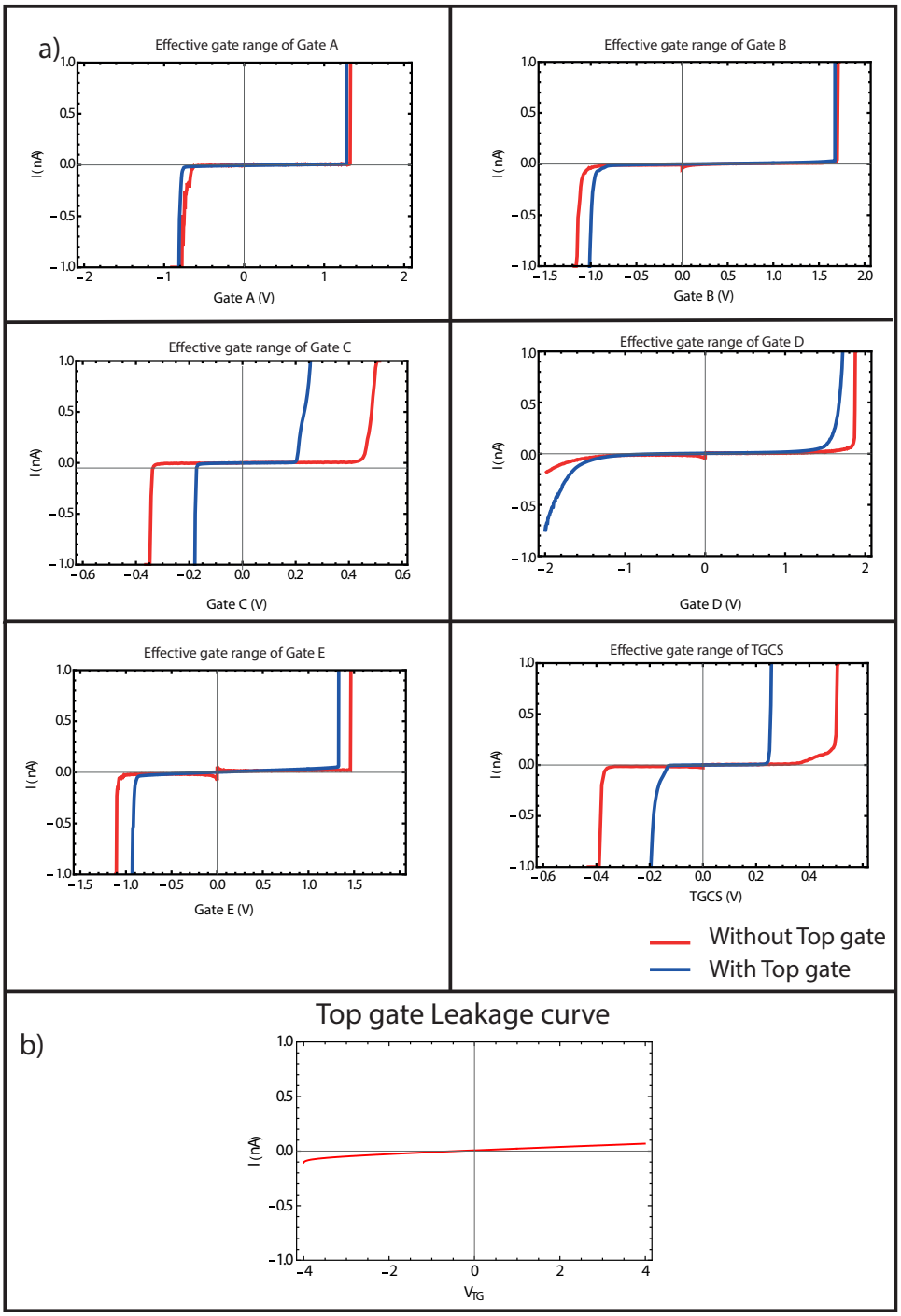

Figure 4.22: Gate leakage of all the gates. a) Gate leakage curves of all the in-plane gates. Red curve shows the leakage curves for all the in-plane gates without the top gate. Blue curve shows the leakage curves for all the in-plane gates with top gate. b) Leakage current curve for the top gate. It is worth noting that top gate did not leak from ±4V. The trend shown in the curve (similar to a transient response) is due to a finite resistance of $\sim$ 50 GΩ in the measurement setup arising from the finite insulation of loom wires to ground or the internal resistance of the source measure unit used for measuring leakage.

was observed to be -4 V to 4 V. Moreover, the introduction of the top gate allowed 2 more inter-dot transitions to be visible within the effective gate range of the 4 quantum dot device with one of them being the singlet-triplet type. The presence of singlet-triplet type transition is crucial for performing gate operations required for a universal quantum computer.

Chapter 5

Conclusions and Future Work

This thesis has demonstrated the development and implementation of a recipe for integrating an ALD deposited dielectric layer and surface "top gate"onto STM-patterned atomic precision devices.

Initially, reproducible growth of the Al_2O_3 layers $\approx$ 28 nm thick is demonstrated with a consistent thickness for different films deposited after 250 cycles of ALD growth at 200 ℃ using TMA and H_2O as precursors. Ellipsometry was used to confirm the thickness of Al_2O_3 layers deposited. Following this the optimum dose rate for the EBL and the reliable etching times were studied in great detail to pattern the ALD dielectric. An optimum dose range of 220-250 $\mu C/cm^2$ was found necessary to pattern the EBL resist mask on top of the ALD grown dielectric. After development of the pattern followed by a short O_2 plasma step, an etching time of 32 seconds in BHF 1:15 solution maintained at 30 ℃ was shown to completely etch the Al_2O_3 layer allowing to establish contact with the buried STM-patterned device. After determining robust process parameters, ALD deposition was performed over

STM-patterned devices.

Three sets of devices are characterized for testing the effectiveness of the Al_2O_3 layer. A high carrier density ($\sim 10^{14}$ cm^{-2}) δ-doped Hall bar device was first characterized using magnetotransport measurements performed before and after the Al_2O_3 dielectric layer ALD deposition. The carrier density n_s of the Si:P δ-doped Hall bar did not show any significant change ($\sim$3%) with varying the top gate voltage as expected due to its high carrier density. The top gate patterned over the Hall bar device yielded a very large gate range (-4 V to 4 V) highlighting the quality and uniformity of growth of the dielectric layer across a very large area ($>$ 400,000 μm^2).

Secondly, the Al_2O_3 dielectric was deposited and a top gate patterned over a 3-terminal SET quantum dot device and the results compared before and after depositing the top gate. The gate lever arm (α) for the in-plane STM-patterned gate was observed to reduce by 6.1 % by the presence of the top gate but no significant change in the charging energy was observed. The gate range of the in-plane gate was also observed to reduce slightly after patterning the top gate, but only in negative bias. The EBL-patterned top gate, positioned exactly over the STM patterned inner device structure, was however observed to have a large lever arm of 0.278 and a large gate range of -4 V to 4 V. Stability analysis of the device before and after patterning the top gate revealed the most stable gating operation observed with the top gate giving the lowest noise (0.75 mV and 0.66 mV) and lowest drift (2.3 mV and 1.9 mV). Additionally, a dynamic frequency response of the top gate highlighted successful gate pulsing using a square wave pulse for a frequency up to 1 MHz.

Finally, a 4 quantum dot device with potential applications in realizing a singlet-

triplet qubit for demonstrating quantum gate operations was characterized before and after patterning a top gate on top of the Al_2O_3 dielectric. Here the presence of singlet-triplet inter-dot transitions is absolutely essential for the operation of singlet-triplet qubits. However, the 4 quantum dot device discussed did not show any singlet-triplet inter-dot transitions when it was first patterned in the STM. The integration of a top gate patterned on top of the inner device structure insulated with a dielectric layer of Al_2O_3 did allow a much higher tunability of this device. The introduction of a top gate with its large gate range (-4 V to 4 V) made two new inter-dot transitions accessible within the gate range of the planar STM-patterned gates with one of them being a singlet-triplet inter-dot transition.

The results present in this Thesis demonstrate the successful integration of top gates on atomic scale silicon devices. This paves the way for more complex atomic scale devices to be realized using the precision of STM patterning, getting one step closer to the physical implementation of a universal quantum computer. The presence of a top gate definitely increases the tunability of devices and been shown to have minimal impact on the stability of the device. Future work involves, patterning a top gate on STM-patterned donors for realising single and two qubit gate operations.

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