Modular Multilevel Converters in Hybrid Multi-Terminal HVDC Systems

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Modular Multilevel Converters in Hybrid Multi-Terminal HVDC Systems

by

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High-voltage direct current (HVDC) systems are becoming commonplace in modern power systems. Line commutated converters (LCCs) are suitable for bulk power and ultra-HVDC (UHVDC) transmission, while with inflexible power reversal capability and possible commutation failures. However, voltage source converters (VSCs) possess flexible power reversal capability and provide immunity to commutation failures. Modular VSC topologies offer improved performance compared to conventional 2 level/3 level VSC-based HVDC. The family of modular VSCs includes the well-established modular multilevel converter (MMC) and other emerging modular VSC topologies such as the DC-fault tolerant alternate arm converter (AAC) that share topological and operational similarities with the MMC. It is noteworthy that the integration of LCC and modular VSCs leads to unique benefits despite the challenges of different HVDC configurations. Hence, it is necessary to explore the system performance of different HVDC converter topologies, especially more complex hybrid multiterminal HVDC (MTDC) systems and DC-grids combining different converters. This thesis focuses on the combination of the LCC, MMC and AAC to constitute different hybrid HVDC transmission systems.

It is of significance to provide a common platform where the proper comparison and evaluation of different HVDC systems and control methods can be completed and independently validated. Therefore, this thesis also provides an overview of current HVDC benchmark models available in the existing literature. In addition, the detailed modeling methods of HVDC systems are discussed in this thesis. For ensuring the static security of HVDC systems especially the future DC-grids, this thesis proposes a generalized expression of DC power flow under mixed power/voltage (P/V) and current/voltage (I/V) droop control, considering the DC power flow for normal operation and after converter outage.

Detailed simulation models are established in PLECS-Blockset and Simulink to study the hybrid HVDC/MTDC systems and DC grid combining the LCC with the MMC and (or) AAC. The detailed sets of results demonstrate the functionalities of developed hybrid HVDC systems and validate the performance of systems complying with widely accepted HVDC operating standards. The developed LCC/AAC-based HVDC/MTDC systems and LCC/MMC/AAC-based DC grid in this thesis are prime steps towards the study of more complex MTDC systems and a key element in the development of future DC super grids.

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Abstract

High-voltage direct current (HVDC) systems are becoming commonplace in modern power systems. On the one hand, thyristor-based line commutated converter (LCC) is a mature technology and suitable for bulk power and ultra-HVDC (UHVDC) transmission, while with inflexible power reversal capability and possible commutation failures. On the other hand, voltage source converters (VSCs) offer flexible power reversal capability and provide immunity to commutation failures. Hence, VSCs are more suitable for multiterminal HVDC (MTDC) systems and future DC grids. Moreover, hybrid MTDC systems and DC-grids combining LCCs and VSCs are options for delivering power from remote energy zones to main load centers or dealing with commutation failures by replacing LCCs in the inverter side with VSCs.

Modular VSC topologies offer improved performance compared to conventional two level or three level VSC-based HVDC. The family of modular VSCs includes the well-established modular multilevel converter (MMC) and other emerging modular VSC topologies that share topological and operational similarities with the MMC such as the DC-fault tolerant alternate arm converter (AAC). Although modular VSCs offer unique benefits over LCCs and conventional VSCs, there are still challenges that need to be further addressed, specifically in modular VSCs other than the MMC. It is noteworthy that the integration of LCC and modular VSCs leads to unique benefits despite the challenges of different HVDC configurations. Thus, it is necessary to explore the system performance of different HVDC converter topologies, especially more complex hybrid MTDC systems and DC-grids combining different converters. This thesis focuses on the combination of the LCC, MMC and AAC to constitute different hybrid HVDC transmission systems and hybrid DC grids.

The advantages of HVDC transmission in the current electricity grid environment have sparked an increased interest on HVDC system studies. A common challenge is the proper comparison and evaluation of different systems and control methods. Benchmark models facilitate this approach as they provide a common platform where such comparisons can be completed and independently validated. This thesis also provides an overview of current HVDC benchmark models available in the existing literature. The analysis and discussion based on the review identifies the current research gaps and opportunities for development of HVDC benchmark models, the importance of openly available data across all benchmark models covering a wide range of simulations and applications as well as the potential for development of extended models to facilitate large-scale network analysis and DC grids.

Different modeling approaches can be used in HVDC systems for specific studies. The detailed modeling approaches of HVDC systems are discussed in this thesis, including the electromagnetic transient (EMT), electromechanical transient, dynamic frequency capturing and co-simulation modeling methods. For ensuring the static security of HVDC systems especially that of future hybrid DC grids, this thesis proposes a generalized expression of DC power flow under mixed power/voltage (P/V) and current/voltage (I/V) droop control. The initial DC power flow for normal operation and the DC power flow after converter outage are discussed considering the maximum power limitation of converters. Also, the accuracy of proposed generalized expression of DC power flow is verified in an MMC-based DC grid and developed hybrid multi-converter DC grid.

Detailed simulation models are established in PLECS-Blockset and Simulink to study the hybrid point-to-point (PTP), multi-terminal HVDC systems and DC grid combining the LCC with the MMC and (or) AAC. A control hierarchy is developed and detailed control schemes under AC and DC faults are proposed for hybrid HVDC systems.

The detailed sets of results, including the steady-state operation, reference tracking and system performance under AC and DC faults, demonstrate the functionalities of developed hybrid HVDC systems and validate the performance of systems complying with widely accepted HVDC operating standards. The developed LCC and AAC-based PTP HVDC system, MTDC system and LCC, MMC and AAC-based DC grid in this thesis are prime steps towards the study of more complex MTDC systems and a key element in the development of future DC super grids.

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List of Abbreviations

Abbreviation	Definition
AAC	Alternate Arm Converter
AC	Alternating Current
AVM	Average Value Model
BTB	Back to Back
CB-PWM	Carrier-based Pulse Width Modulation
CCC	Capacitor Commutated Converter
CCSC	Circulating Current Suppression Control
CD-MMC	Clamped-Double Modular Multilevel Converter
CDSM	Clamped-Double Submodule
CSC	Current Source Converter
DAE	Differential-Algebraic Equation
DC	Direct Current
DE	Detailed Equivalent
DFSRF	Double-Frequency Synchronous Reference Frame
DP	Dynamic Phasor
DS	Direct Switch
EHV	Extra High Voltage
EMT	Electromagnetic Transient
EO-AAC	Extended Overlap AAC
FBSM	Full-Bridge Submodule
FB-MMC	Full-Bridge Modular Multilevel Converter
FCCC	Forced Circulating Current Control

FH-MMC	Full-Bridge and Half-Bridge Modular Multilevel Converter
FRT	Fault-Ride-Through
GTO	Gate Turn-Off
HB-MMC	Half-Bridge Modular Multilevel Converter
HBSM	Half-Bridge Submodule
HiL	Hardware-in-the-Loop
HVDC	High Voltage Direct Current
IGBT	Insulated gate bipolar transistor
LCC	Line Commutated Converter
LCC-D-MMC	Line Commutated Converter-Diode-Modular Multilevel Converter
LS-PWM	Level-Shift Pulse Width Modulation
MMC	Modular Multilevel Converter
MMCB	Bank of Modular Multilevel Converter
MTDC	Multiterminal High Voltage Direct Current
MV	Medium Voltage
NLM	Nearest Level Modulation
ODE	Ordinary Differential Equation
OHL	Overhead Line
OLTC	On-load Tap Changer
OOC	Overlap Onset Control
PDE	Partial Differential Equation
PI	Proportional Integral
PLL	Phase Locked Loop
PM	Phasor Model
PR	Proportional Resonant
PS-PWM	Phase-Shift Pulse Width Modulation
PTP	Point-to-Point
PWM	Pulse Width Modulation
RK	Runge-Kutta
RMS	Root Mean Square

RT	Real-Time
SCR	Short-Circuit-Ratio
SFP	Shifted Frequency Phasor
SM	Submodule
SO-AAC	Short Overlap Alternate Arm Converter
SSN	State-Space Nodal
SV-PWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
UGC	Underground Cable
UHVDC	Ultra High Voltage Direct Current
USC	Undersea Cable
VDCOL	Voltage Dependent Current Order Limiter
VSC	Voltage Source Converter
ZCS	Zero Current Switching

Abbreviation (Institution)	**Definition**
CIGRE	Conseil International Des Grands Reseaux Elecctriques
SGRI	State Grid Research Institution of China

Chapter 1

Introduction

1.1 Line-Commutated Converter (LCC) and Voltage Source Converter (VSC)-based Hybrid High-Voltage Direct Current (HVDC) Systems

High voltage direct current (HVDC) transmission has become an irreplacable part in the current electricity grid due to its unique advantages [1–3]. For long distance power transmission with the same voltage, HVDC is more efficient and economical than HV alternating current (AC), since the distance of DC transmission is not limited by the reactive power consumption and the cost of DC lines is lower than AC lines, while investments in DC stations are higher than AC stations [4]. Owing to the charging currents of the line capacitance, it is necessary to provide periodic reactive power compensation for AC transmission systems with the increase of transmission distance. Also, another limiting factor is the skin and proximity effect in AC lines, which will limit the current capacity of AC transmission. Hence, HVDC is more efficient and can play significant role in future long distance power transmission [5, 6].

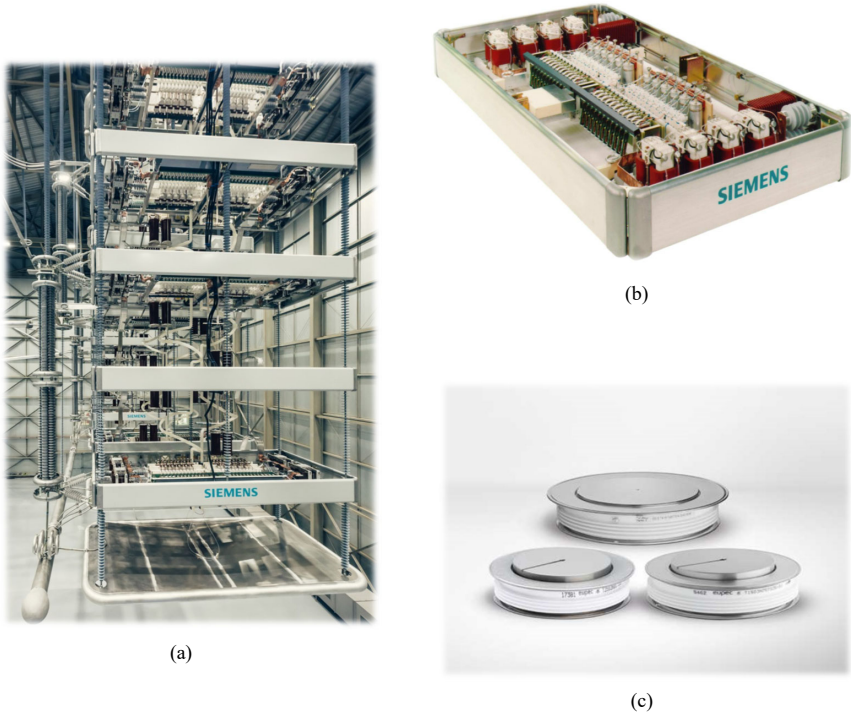
From line-commutated converter (LCC) or current source converter (CSC)-based high-voltage direct current (HVDC) transmission system (Fig. 1.1) to conventional voltage source converter (VSC)- and modular VSC-based HVDC transmission systems (Fig. 1.2 and Fig. 1.3), hundreds of HVDC projects have been commissioned and are now under construction in the world [7]. LCC-based HVDC system is the most mature technology and it is still the best choice for bulk power transmission due to the high voltage and current rating of thyristors such as the Changji-Guquan $\pm$1100 kV UHVDC transmission project (Fig. 1.4). However, there are some issues with LCC topologies:

i) Limited power reversal capability as the restriction of DC current direction,

ii) possible commutation failures mainly caused by severe AC voltage drop, and

iii) requirement of reactive power compensation due to the reactive power absorption from the AC system.

iv) Investments in additional filter devices because of the characteristic and uncharacteristic harmonics in AC-side and DC-link generated by the natural commutation process.



(a) (b) (c)

FIGURE 1.1: LCC-based HVDC station made by Siemens: (a) main station, (b) thyristor module and (c) high power thyristors (4 inch, 5 inch and 6 inch) [8].

By comparison, VSC-based HVDC systems with fully-controlled devices have many benifits over LCC-based HVDC systems:

i) independent control of active and reactive power,

ii) reduced or no filter requirement,

iii) no issue of commutation failures,

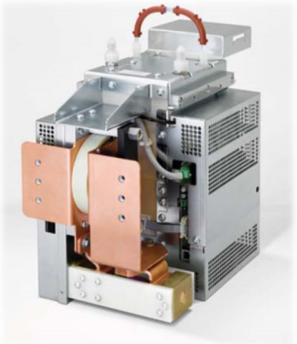
iv) potential capability of connecting passive networks, and

v) more feasible for the formation of multiterminal systems [1–3].

FIGURE 1.2: Conventional VSC-based HVDC station made by ABB [9].

(a)

(b)



(c)

FIGURE 1.3: Modular VSC-based HVDC station made by Siemens: (a) main station, (b) converter arm segment and (c) submodule [10].

(a)

(b)

(c)

FIGURE 1.4: Changji-Guquan ±1100 kV LCC-based UHVDC transmission system: (a) project map view, (b) aerial view of Guquan station and (c) 1100 kV transformer [11].

It is noted that modular VSC topologies provide improved performance compared to conventional VSC-based HVDC. The main features are:

i) modularity and scalability,

ii) capability to handle high power ratings,

iii) no filter requirement as they generate nearly sinusoidal output voltage,

iv) low switching losses, and

v) improved fault-ride-through (FRT) ability [4–6].

In addition, there is a range of modular VSC topologies that can be considered for hybrid HVDC system applications which include:

i) MMC with half-bridge sub-modules (HBSMs) [4, 12, 13],

ii) MMC with full-bridge SMs (FBSMs) or other bipolar SMs [14–19],

iii) MMC with hybrid configurations of SMs [20, 21],

iv) the alternate arm converter (AAC) [22–54], and

v) other hybrid converter configurations [55, 56].

Fig. 1.5 shows the recently commissioned Zhangbei meshed four-terminal DC grid project based on the MMC with HBSMs.

FIGURE 1.5: Zhangbei meshed four-terminal DC grid [57].

There are still many challenges for these modular VSC topologies, although the state-of-the-art modular VSC-based HVDC possesses incomparable benefits compared with LCC-based HVDC transmission system. The DC fault tolerance level and DC FRT capability are the key concerns. The main approaches of dealing with DC fault in actual project is to i) open AC-breakers, ii) install DC-breakers and iii) use bipolar SMs. Opening AC breakers

can isolate the AC-side and DC-link while the response of AC breakers is slow. DC breakers can interrupt the fault current at a short time but it requires high investment. In addition, bipolar SMs adopted in modular VSC topologies can limit the increase of fault current via the discharging of SM capacitors in blocking state, at the cost of losses and increased investment. Besides, the other main challenges of modular VSCs include:

i) high cost and low power density of converters,

ii) unbalanced energy and losses distribution amongst SMs,

iii) circulating current suppression,

iv) internal SM faults during long-term operation, and

v) increased number of sensors and measurements.

Despite the issues of LCC, conventional VSC and modular VSC topologies, the commissioned and constructed HVDC projects have confirmed the feasiblity of these basic topologies [7]. In addition, some projects combine different topologies together taking the respective advantages. The two-level VSC (2L-VSC) is selected to combine with LCC for the initial study on hybrid HVDC systems [58–76]. With the appearance of MMC, current study of hybrid HVDC systems focuses on the combination of LCC and MMC or other modular VSCs [6, 21, 77–94]. In general, the benefits of LCC and VSC-based hybrid HVDC transmission system are summarized below:

i) cost reduction and low losses,

ii) no commutation failures,

iii) potential connnection with passive networks and weak grids,

iv) reduced requirement of filter devices , and

v) improved DC fault clearing capability by force-retard of firing angle.

It is a paramount requirement for future development and extension of DC grids to integrate converters from multiple vendors [49]. Hence, the thesis studies the combination of LCC and modular VSC topologies, including the state-of-the-art MMC and the emerging DC-fault tolerant AAC, based on the current available benchmark models. The detailed parameter selection, steady-state and transient performance are considered demonstrating the feasibility of developed different hybrid HVDC systems in this thesis.

1.2 Literature Review

1.2.1 Background

The combination of LCC and VSC has long been attractive from the end of 20th century. However, the self-commutated converter of early hybrid HVDC system was gate turn-off (GTO) devices and mainly arranged at inverter side [58, 59]. Based on the hybrid PTP HVDC systems, the initial idea of constructing hybrid MTDC systems, was to replace the AC substation with rectifier and inverter station. The extra-HV (EHV) /HV AC substation is replaced by an LCC-based rectifier station, and the HV/medium voltage (MV) substation is replaced by VSC-based inverter station since most AC systems connected with HV/MV substations are passive networks [60, 61].

Due to the rapid development of power electronic devices, IGBT has become the main device for voltage source converters. In general, a hybrid HVDC system can be constituted by an LCC and two-level (2L), three-level (3L) or multilevel VSC. However, considering the requirements of modern projects, the combination scheme of LCC and modular VSC is more practical than the hybrid LCC-2L-VSC or LCC-3L-VSC scheme due to the increased handling ability of high power and voltage ratings [73].

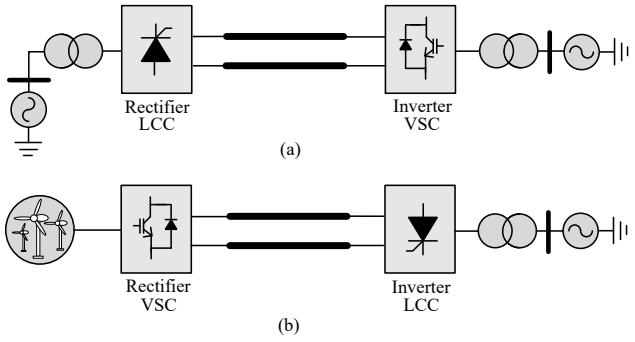


FIGURE 1.6: Hybrid HVDC PTP system: (a) configuration 1 and (b) configuration 2.

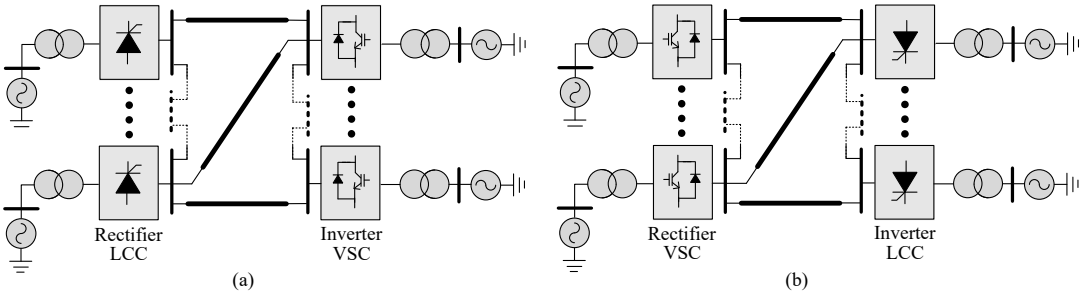


FIGURE 1.7: Hybrid MTDC system: (a) configuration 1 and (b) configuration 2.

For a hybrid PTP HVDC system, LCC and VSC in most cases function as the rectifier and the inverter, respectively (Fig. 1.6(a)). The goal of this configuration is to avoid commutation failures on the inverter side. An alternative option is that of a VSC set up at the rectifier side for the scenario of connecting passive networks such as wind farms (Fig. 1.6(b)), while consequent commutation failures of LCC in the inverter side need to be further considered and tolerated. For hybrid MTDC transmission system, LCCs can transmit bulk power from energy zones which can be absorbed by VSCs separately (Fig. 1.7) [63–66]. The study of hybrid MTDC system is similar as hybrid PTP HVDC system, while the control scheme is more complicated considering the coordination of multi-converters. The following sections will explore the current study on hybrid HVDC systems based on LCC and VSC.

1.2.2 LCC and Conventional VSC-based Hybrid HVDC Systems

LCC-2L-VSC and LCC-3L-VSC are the two main candidates of LCC and conventional VSC-based hybrid HVDC systems. Based on the description of previous section, the commutation failures should be considered when 2L (3L)-VSC is located at rectifier side and LCC is in the inverter side. An alternative approach is that capacitor commutated converter (CCC) can be applied to replace LCC for avoiding commutation failures [71–73]. In addition, a line-commutated converter based on pulse width modulation (PWM)-CSC can also be applied for connecting with wind farms, which also possesses the capability of inherent short-circuit protection [66]. From the control logic, LCC in the inverter side can adopt conventional voltage dependent current order limiter (VDCOL), which is also appropriate to the hybrid HVDC systems with LCC and other modular VSCs.

The study of LCC and 2L (3L)-VSC-based three-terminal hybrid HVDC system is the first exploration to hybrid MTDC systems. Such a configuration is applied to study different conditions, such as system start-up, steady state operation and AC voltage sag in the inverter side [75]. The basic configuration of three-terminal hybrid HVDC system is that LCC and VSC are arranged in the rectifier side and inverter side, respectively, the third terminal can be either LCC or VSC operating on rectifier mode or inverter mode depending on the actual requirement. Likewise, the rectifier side should be VSCs when connecting with passive networks or weak grids [68, 76]. In general, the study of hybrid HVDC systems based on conventional VSCs paves the way for the combination of LCC and modular VSCs due to the similar external characteristics of conventional and modular VSCs.

1.2.3 LCC and Modular Multilevel Converter (MMC)-based Hybrid Point-to-Point (PTP) HVDC Systems

The MMC, as the state-of-the-art VSC topology is the favorable choice for hybrid HVDC systems, and the current hybrid HVDC projects all adopt the LCC-MMC hybrid topology [6, 95–97]. Given the different SMs in hybrid LCC-MMC HVDC system, MMC side can adopt different arrangements of SMs to satisfy specific demand. The HB-MMC is the most economic choice for a hybrid system but it lacks the capability of clearing DC fault. FB-MMC and other MMCs with bipolar SMs have DC fault ride-through capabilities and the voltage polarity can be changed without stopping operation, as is the case with HB-MMC, at the cost of higher losses and investment [77, 78, 80].

A possible method, based on installing two sets of high power diodes between two converters creating an LCC-Diode-MMC (LCC-D-MMC) system, can handle DC line faults when adopting HB-SMs, but the power flow of such a system cannot be reversed due to the unidirectional continuity of the diode [88–91]. Besides, the combination scheme of full-bridge and half-bridge MMC (FH-MMC) is favorable for hybrid systems considering the investment costs, which can use either symmetric FH-MMC or asymmetric FH-MMC, while the detailed ratio of different SMs needs to be further explored. It is noted that asymmetric FH-MMC can effectively balance SM capacitor voltages under DC-bus voltage deviations [21, 79].

The available configurations of hybrid PTP HVDC systems are shown in Fig. 1.8. The configuration of hybrid monopole system with 12-pulse LCC and MMC follows with the Fig. 1.8(a). In addition, there are four possible configurations for bipole hybrid HVDC system. Two sets of 12-pulse LCCs and an MMC can be employed (Fig. 1.8(b)), but the system can be in monopole operation if with two MMCs (Fig. 1.8(d)). Also, each station can employ hybrid topology which is a 12-pulse LCC and an MMC are respectively distributed at positive or negative pole (Fig. 1.8(c), (e)). The topology of Skagerrak 3 and Skagerrak 4 between Denmark and Norway follows the configuration of Fig. 1.8(e), where Skagerrak 3 comprises two 12-pulse LCCs in negative pole while Skagerrak 4 comprises two MMCs in positive pole (Fig. 1.9) [95].

For hybrid UHVDC transmission systems, more converters in one station should be arranged (Fig. 1.10). Fig. 1.10 (a) is the conventional configuration that two sets of 12-pulse LCCs and MMCs are respectively series-connected arranging at their individual station of each pole. Based on the conventional configuration, one MMC or 12-pulse LCC in each pole can be replaced by each other constituting different topologies (Fig. 1.10 (b), (c), (d)). In addition, the capacity issue of MMC can be resolved by parallel connection of converters which is also called bank of MMCs (MMCB) [98, 99]. Fig. 1.10 (b) is an improved configuration of MMC-MMC PTP system which offers better DC FRT capability

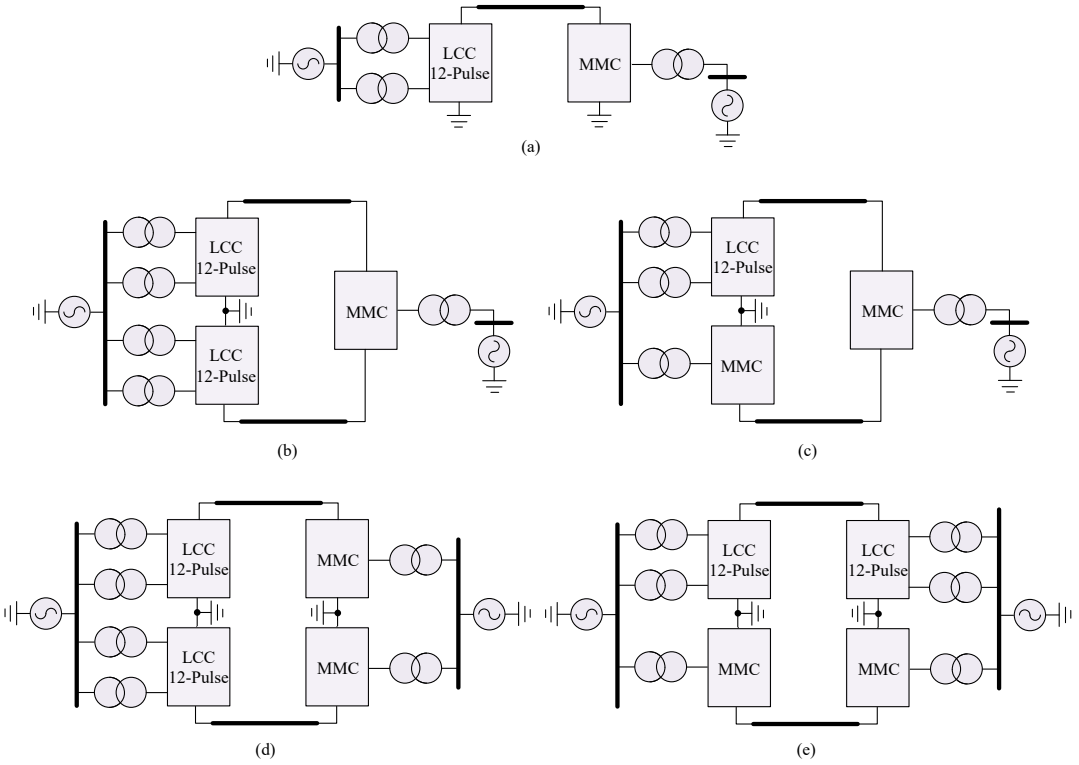


FIGURE 1.8: Available configurations of hybrid HVDC systems: (a) monopole configuration, (b) bipole configuration 1, (c) bipole configuration 2, (d) bipole configuration 3, and (e) bipole configuration 4.

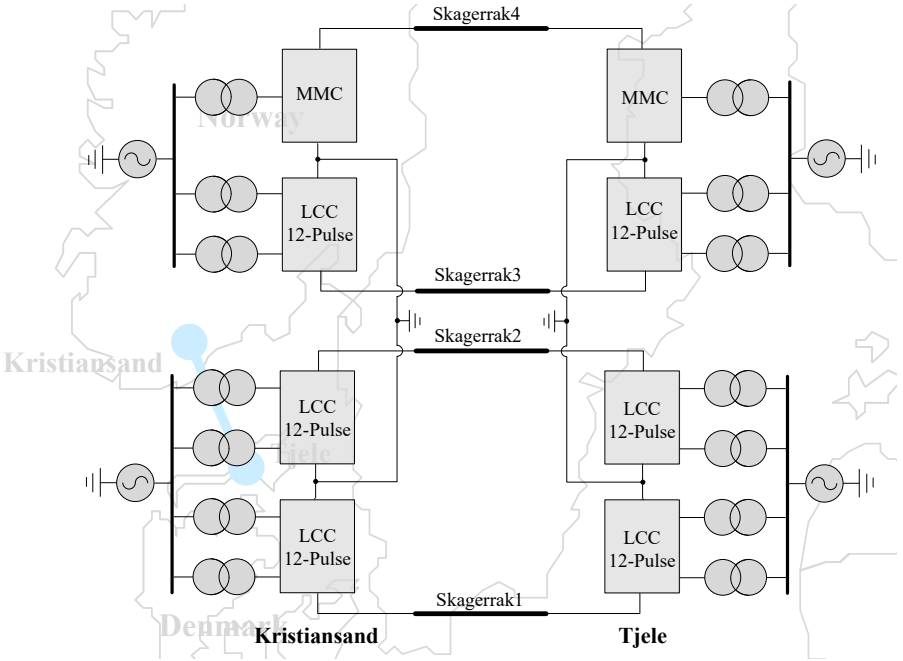


FIGURE 1.9: One-line diagram of the Skagerrak hybrid HVDC system.

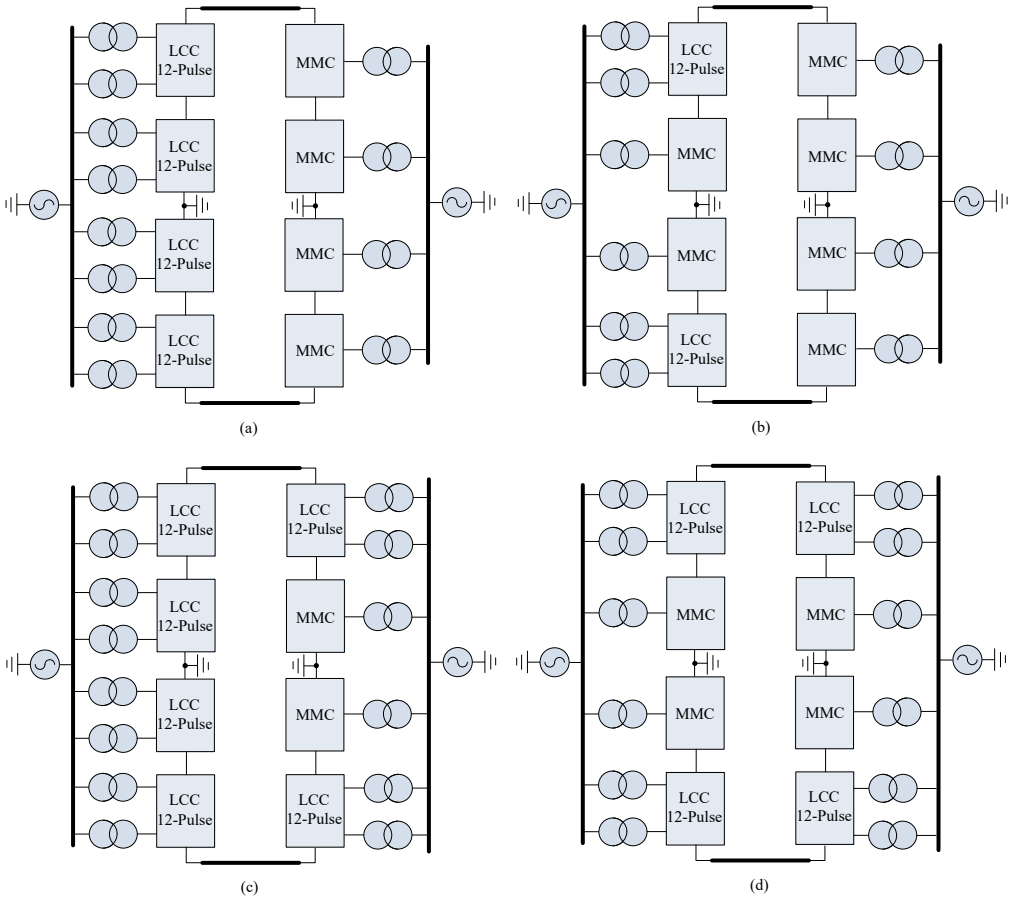


FIGURE 1.10: configurations of hybrid UHVDC systems: (a) configuration 1, (b) configuration 2, (c) configuration 3 and (d) configuration 4.

since the 12-pulse LCC can block the fault current of MMC during DC fault. In addition, the MMCB in the topology of Fig. 1.10 (c), as an extension of Fig. 1.10 (a), can provide reactive power support for 12-pulse LCC avoiding commutation failures to some extent. It is worth mentioning that the Baihetan-Jiangsu ±800 kV UHVDC project plans to adopt the configuration of Fig. 1.10 (c) and three MMCs in parallel connection forms an MMCB (Fig. 1.11) [97]. Although the configuration of Fig. 1.10 (d) has worse efficiency than the configuration of Fig. 1.10 (c), it can be considered a combination of Fig. 1.10 (b), (c) and also has many benefits compared to the conventional configuration of Fig. 1.10 (a):

i) potential capability of connecting with weak grid or passive network,

ii) independent control of active and reactive power,

iii) risk reduction of commutation failures, and

iv) improved DC fault handling capability via force-retard of firing angle and converter blocking.

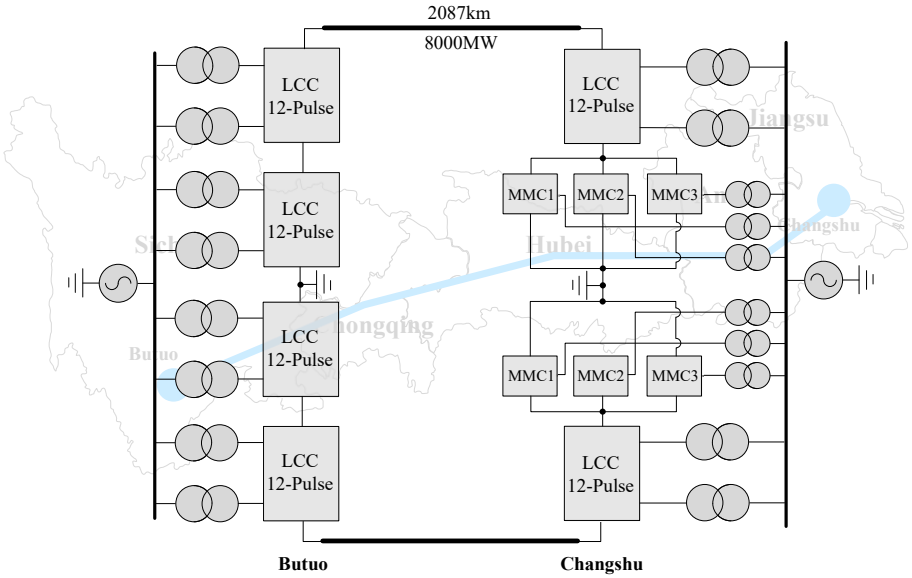


FIGURE 1.11: One-line diagram of the Baihetan hybrid HVDC systems.

1.2.4 LCC and MMC-based Hybrid Multiterminal HVDC (MTDC) Systems

The SM arrangements of LCC and MMC-based hybrid MTDC systems are similar as LCC and MMC-based hybrid PTP HVDC systems which have been described in Chapter 1.2.3.1. By setting up additional MMCs in the inverter side, the hybrid PTP HVDC system can be extended to the most commonly employed hybrid three-terminal HVDC system (Fig. 1.12(a)). Besides, multiple LCCs and MMCs in rectifier or inverter side can constitute more complex hybrid MTDC systems or simple DC grids (Fig. 1.12(b),(c)). Also, LCC can be as a sending end from long distance transmitting bulk power to a DC grid consisted by MMCs, as shown in Fig. 1.12 (d). Some current LCC PTP or LCC-MMC PTP sytems have the potential to further develop to a hybrid MTDC system with adding more converters. The Manitoba project is a two terminal LCC HVDC system, which now has been developed into a four-terminal HVDC system with two FB-MMCs [86].

For ultra long distance transmision, the hybrid UHVDC transmission systems will play significant role in the future [93]. The Kunliulong three-terminal hybrid UHVDC project ($\pm$800kV, 8000MW) with hybrid MMC SMs was put into operation on December, 2020 (Fig. 1.13) [6]. Taking the three-terminal hybrid HVDC system as an example (Fig. 1.14), there are six basic operation modes for conventional hybrid multiterminal UHVDC system:

i) bipole operation mode (Fig. 1.14 (a)),

ii) monopole operation mode (ground return) (Fig. 1.14 (b)),

iii) monopole operation mode (metallic return) (Fig. 1.14 (c)),

iv) two-terminal operation mode (Fig. 1.14 (d)),

v) bipole-monopole hybrid operation mode (Fig. 1.14 (e)) and

vi) single valve group operation mode (Fig. 1.14 (f)).

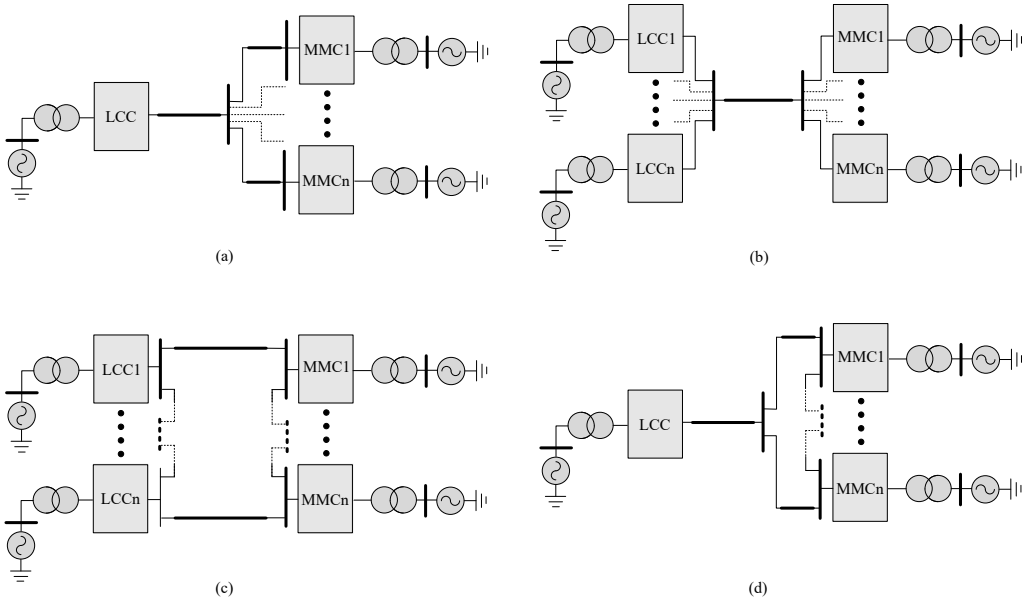


FIGURE 1.12: Available configurations of hybrid MTDC systems: (a) configuration 1, (b) configuration 2, (c) configuration 3 and (d) configuration 4.

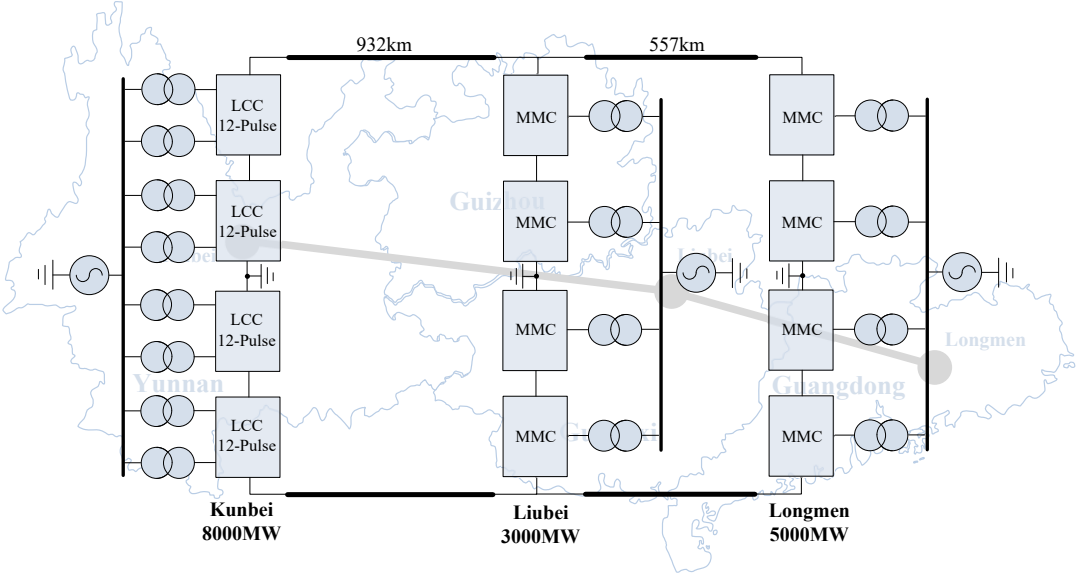


FIGURE 1.13: One-line diagram of the Kunliulong hybrid MTDC project.

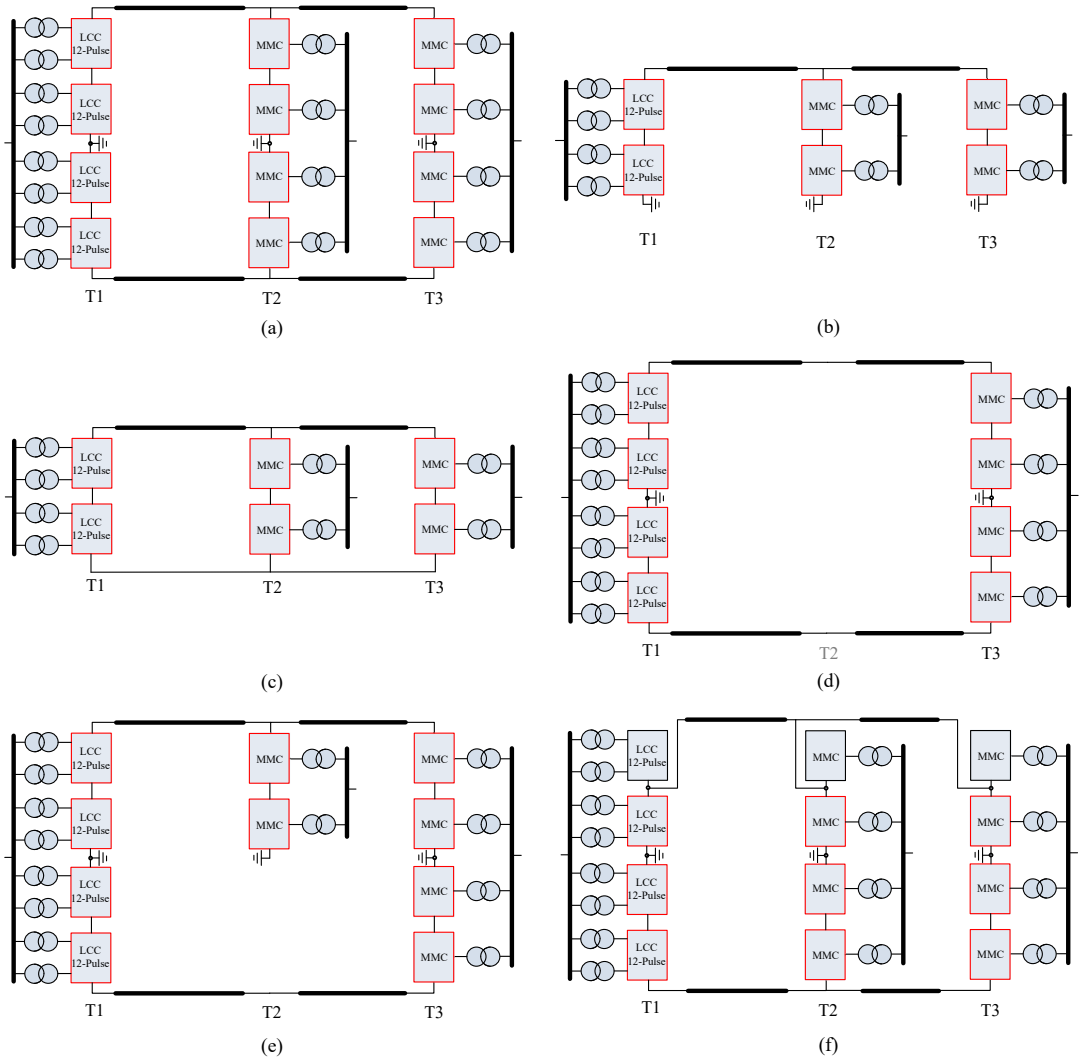


FIGURE 1.14: Operation modes of the three-termianl hybrid UHVDC system: (a) bipole operation mode, (b) monopole operation mode (ground return), (c) monopole operation mode (metallic return), (d) two-terminal operation mode, (e) bipole-monopole hybrid operation mode, and (f) single valve group operation mode.

The three-terminal HVDC hybrid system can transfer into monople operation taking advantage of the bipole operation flexibility. The system can automatically run into two-terminal operation mode if one receiving terminal is out of operation due to faults. In addition, the bipole-monopole hybrid operation mode or single valve group operation mode is possible in hybrid MTDC system when one pole of receiving terminal or one valve group is isolated. In general, hybrid MTDC systems possess potential capability handling different conditions, whether from faults or actual requirements, due to the various operating modes [100].

Based on the above description, there have been important advances in hybrid HVDC

systems based on the LCC and the VSC. However, there are still many challenges of hybrid HVDC systems, especially the MTDC systems and future DC-grids, mainly reflecting in:

i) improved DC fault tolerant topologies and efficient DC-breakers ensuring the reliability and resiliency of the hybrid HVDC systems,

ii) fast FRT capability and effective protection schemes under different faults,

iii) flexible power flow control and complete power flow analysis of hybrid MTDC systems and DC-grids,

iv) coordinated control of LCC with different modular VSCs from multiple vendors, and detailed system performance of hybrid multi-converter DC power systems.

1.3 Thesis Objectives

The main objectives of the thesis are:

- To review the available benchmark models for HVDC converters, HVDC systems and DC grid stuides.
- To summarize modeling approaches of HVDC systems from the aspect of computational complexity and simulation accuracy.
- To propose generalized expressions of DC power flow considering mixed droop control.
- To develop LCC, state-of-the-art and emerging modular VSC topologies-based hybrid HVDC and MTDC systems filling the research gaps on more complex HVDC systems combining different converters from multiple vendors.
- To study hybrid DC grids based on LCC, state-of-the-art and emerging modular VSC topologies and verify the system static security based on the proposed generalized expression of DC power flow.

1.4 Simulation Models and Tools

For facilitating specific studies on HVDC systems, various computational models (from RMS load-flow model to full physics based model) are defined in current literature with

different computational complexity [101]. Also, the computational models cover EMT and electromechanical transient (phasor) models. The types of computational models and the detailed modeling approaches are summarized in Chapter 2.3 and Chapter 4.2, respectively.

In this thesis, PLECS-Blockset [102] and Simulink [103] are the used simulation tools for different HVDC simulation models. Detailed equivalent models are used for simulations in Chapter 4, 5, 6 and 7 to study MMC-based DC grid, LCC and AAC-based PTP HVDC system, LCC and AAC-based MTDC system, and LCC, MMC and AAC-based multi-converter DC grid, respectively.

1.5 Thesis Contributions

The main contributions of the thesis are:

- The available benchmark models for HVDC converters, systems and DC grid stuides are reviewed (Chapter 2). The research gaps, data availability and expansion capability of benchmark models are discussed for the development of future complex HVDC benchmark models.
- Based on the DC power flow calculation methods of single P/V and I/V droop control, a generalized expression of DC power flow is proposed to ensure the static security of MTDC systems and DC grids under mixed P/V and I/V droop control (Chapter 4). The detailed theoretical analysis is conducted for deriving the initial DC power flow for normal operation and the DC power flow after converter outage. The theory results are verified by the simulation results in an MMC-based DC grid.
- The AAC in a hybrid HVDC system is demonstrated in Chapter 5 constituting a hybrid LCC-AAC PTP HVDC system with detailed description of control hierarchy and parameter design scheme. The steady-state operation and reference tracking of the hybrid HVDC system are demonstrated. The corresponding control schemes for handling AC and DC faults are proposed in developed hybrid HVDC system, which are verified by the related simulation results showing the better DC fault handling capability of AAC in the hybrid HVDC system than HB-MMC.
- An LCC and AAC-based hybrid MTDC system is further developed in Chapter 6. The simulation results of the LCC-AAC hybrid MTDC system are presented under multiple operating scenarios, AC and DC faults with P/V droop control demonstrating the feasibility of AAC in hybrid MTDC systems and laying the fundation for understanding the AAC in more complex hybrid MTDC systems and future DC super grids combining multiple converters.

- A hybrid DC grid combining multiple converters is presented, including the LCC, MMC and AACs, with different combinations of DC OHLs and cables (Chapter 7). The combined AC and DC fault handling schemes in LCC, MMC and AAC for a hybrid DC grid are investigated validating the transient performance and fault recovery capability under AC and DC faults for the developed hybrid DC grid. The DC power flow for initial operation and contingencies under mixed P/V and I/V droop control in the hybrid DC grid is also demonstrated by the proposed generalized expression of DC power flow.

1.6 List of Publications

The work presented in this thesis has resulted in a number of peer-reviewed journal publications and refereed papers presented in international conferences.

1.6.1 Journal Papers

The following list of papers have been published in international journals.

[1] **P. Sun**, H. R. Wickramasinghe, and G. Konstantinou, "Hybrid LCC-AAC HVDC transmission system," *Electric Power Systems Research*, vol. 192, 106910, Mar. 2021.

[2] **P. Sun**, H. R. Wickramasinghe, and G. Konstantinou, "Hybrid Multiterminal HVDC System based on Line-Commutated and Alternate Arm Converters," *IEEE Transactions on Power Delivery*, pp. 1-1, 2021.

1.6.2 International Conference Papers

The following papers have been presented in international conferences:

[3] **P. Sun**, F. Arrano-Vargas, H. R. Wickramasinghe, and G. Konstantinou, "Benchmark models for HVDC systems and DC-grid studies," in *Proc. ICPES 2019*, Dec. 2019, pp. 1-6.

[4] **P. Sun**, H. R. Wickramasinghe, and G. Konstantinou, "An LCC-AAC hybrid high-voltage DC transmission system," in *Proc. 2020 IEEE ECCE-Asia*, Nov. 2020, pp. 1516-1521.

1.6.3 Papers Under Revision or Review

[5] **P. Sun**, H. R. Wickramasinghe, and G. Konstantinou, "Fault and Power Flow Analysis in Hybrid Multi-Converter DC Grids," *International Journal of Electrical Power & Energy Systems*, 2021. (Under Review)

1.6.4 Other Publications

Additionally, sections of the work completed in this thesis has contributed to the following publications:

[6] H. R. Wickramasinghe, **P. Sun**, and G. Konstantinou, "Interoperability of Modular Multilevel and Alternate Arm Converters in Hybrid HVDC Systems," *Energies*, vol. 14 (5), 1363, 2021.

[7] H. R. Wickramasinghe, **P. Sun**, and G. Konstantinou, "A hybrid VSC-HVDC system based on modular multilevel converter and alternate arm converter," in *Proc. IEEE IECON 2020*, Oct. 2020, pp. 4141–4146.

The association between the chapters of the thesis and the journal and conference publications is listed in the following table.

Chapters	**Publications**
Chapter 2. Benchmark Models for HVDC Converters, HVDC Systems and DC Grid Studies	[3]
Chapter 3. Topologies for Hybrid HVDC Systems	
Chapter 4. Modeling Approaches and Power Flow Analysis of HVDC Systems	[5]
Chapter 5. LCC and AAC-based Hybrid PTP HVDC Transmission System	[1], [4]
Chapter 6. LCC and AAC-based Hybrid MTDC Transmission System	[2]
Chapter 7. LCC and AAC-based Hybrid Multi-Converter DC Grid	[5]

1.7 Thesis Outline

The thesis is organized as follows:

Chapter 2 reviews all the available benchmark models for HVDC converters, systems and DC grid studies. Eleven available benchmark models are described in detail. Also, the research gaps, data availability and expansion capability of current HVDC benchmark models are further discussed, which would facilitate the establishment of future more complex HVDC models.

Chapter 3 analyzes the conventional LCC, state-of-the-art MMC and emerging DC-fault tolerant AAC for hybrid HVDC systems in the following chapters. The basic topologies, operation principles and control schemes of the LCC, MMC and AAC are discussed in detail.

Chapter 4 summarizes the modeling approaches of HVDC systems, including the EMT, electromechanical transient and two dynamic frequency capturing modeling methods. A generalized expression of DC power flow under mixed P/V and I/V droop control is proposed in this chapter to assess the system static security based on the detailed description of droop control in HVDC systems. The accuracy of the proposed generalized expression of DC power flow is verified in an MMC-based DC grid by the analysis of initial power flow for normal operation and the power flow after converter outage.

Chapter 5 develops an LCC and AAC-based hybrid PTP HVDC system with detailed description of control hierarchy and system parameter selection. The simulation results of steady-state operation, reference tracking are demonstrated first, then the fault handling capability are validated with proposed corresponding control schemes for handling AC and DC faults. The DC fault simulation results also verify the AAC in hybrid HVDC system shows better DC fault handling capability than HB-MMC.

Chapter 6 extends the LCC and AAC-based hybrid PTP HVDC system to a hybrid MTDC system combining LCC and two AACs. The performance of the hybrid MTDC model is verified for multiple operating scenarios including AC and DC faults via simulation. The results demonstrate the feasibility of the developed LCC and AAC-based hybrid MTDC system under P/V droop control and proposed DC FRT scheme.

Chapter 7 combines an LCC, an MMC and two AACs to constitute a hybrid multi-converter DC grid with different combinations of DC OHLs and cables. The simulation results validate the AC and DC FRT capability of the hybrid DC grid by the combined AC

and DC fault handling schemes. The DC power flow analysis is also conducted in the hybrid DC grid by the generalized expression of DC power flow proposed in Chapter 4.

Finally, Chapter 8 concludes the main goals of the thesis and introduces future work.

Chapter 2

Benchmark Models for HVDC Converters, HVDC Systems and DC Grid Studies

2.1 Introduction

New research on topologies, control design, protection strategy and other aspects for HVDC systems can be greatly augmented by the availability of HVDC benchmark models. Benchmark models serve two key purposes. Firstly, they allow comparison of performance of control methods, control hardware and high-level coordination and protection strategies for different HVDC systems. Their secondary purpose is to provide a common reference basis for replication and cross-validation of results. Benchmark models developed with input from the industry can also address issues with parameter selection, typical design decisions and common configurations without intellectual property restrictions or project specific information. The objective of this chapter is to provide an overview of existing and most commonly used HVDC benchmark models covering all possible topology, station and system configurations. The goal of such review is to identify current gaps in availability of benchmark models and facilitate the development of more accurate and relevant HVDC benchmark models enabling future research pathways, especially towards the establishment of hybrid and complex converter and network models.

2.2 HVDC Transmission - From Converters to Systems

The nature of studies related to HVDC transmission ranges from detailed investigation of converter operation to integration of HVDC links to AC systems and DC-grids. This following sections briefly summarize different aspects of HVDC from power electronics topologies to systems.

2.2.1 HVDC Converter Topologies

LCC (Fig. 2.1(a)) represents the earliest and most mature converter technology for HVDC transmission. The power and voltage ratings of thyristors make them suitable for high-power transmission and UHVDC. Multiple projects with capacity over 6000 MW at 800 kV or 1100 kV have been commissioned in the last five years [6, 11, 104]. Nevertheless, grid strength requirements, AC filters and commutation failures are key challenges in the implementation of LCC-HVDC systems. The CCC of Fig. 2.1(b) addresses some of the issues, offering improved immunity to commutation failures, system stability and connection to weaker grids.

VSC-HVDC provides the grid with the controllability and flexibility of voltage source converters but is mainly limited by IGBT ratings. The series connection of IGBTs and switching frequency requirements in the original 2L-VSC of Fig. 2.1(c) were major limitations in expansion to higher power. Modular solutions such as the MMC (Fig. 2.1(d)) or the AAC (Fig. 2.1(e)) are the current state-of-the-art for VSC-HVDC and the topologies of choice for projects in the next decade. A power level of approximately 2 GW defines the maximum power rating with a variety of developments across multiple areas required to compete with LCC-HVDC in terms of maximum transfer capacity. The detailed operation and control of LCC and VSC topologies are outside the scope of this chapter, as they are analyzed in Chapter 3.

2.2.2 HVDC Converter Stations

In terms of converter station configurations, HVDC stations can be divided into monopolar station or bipolar station depending on the number of DC connectors that are at high voltage (Fig. 2.2(a) and (b), respectively). Monopole HVDC systems are simpler structures with a single (either the positive or the negative polarity) conductor at high voltage. This design option leads to overall lower cost systems. VSC-HVDC is usually configured as a symmetrical monopole (Fig. 2.2(a)). However, the additional flexibility and reliability that is provided by the bipolar configuration, despite the added cost, makes bipolar systems

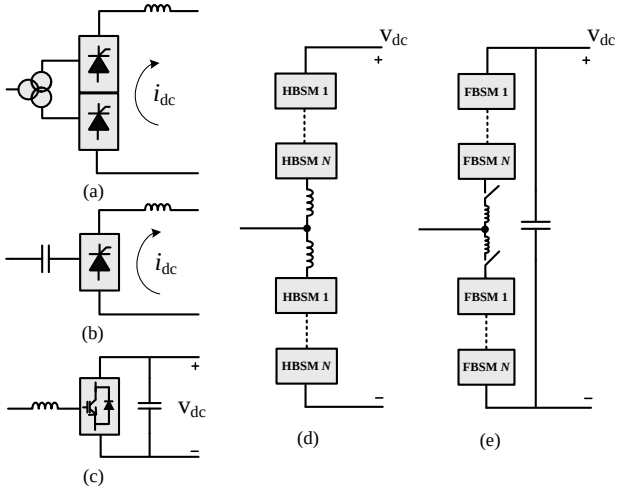


FIGURE 2.1: HVDC converter topologies: (a) 12-pulse LCC, (b) 6-pulse CCC, (c) 2L-VSC, (d) MMC (one phase) and (e) AAC (one phase).

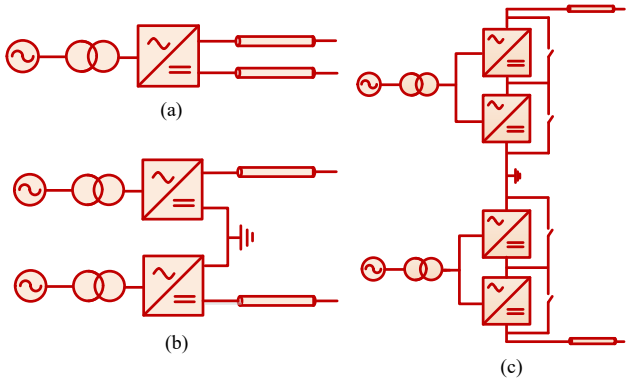


FIGURE 2.2: HVDC station configurations: (a) monopole station, (b) bipole station and (c) series-connected station.

the preferable option for LCC-HVDC. Connections between the two stations can be done either through the earth (or sea in case of undersea cables), through a metallic conductor (metallic return) in case of monopoles or with two terminals in the case of bipoles.

2.2.3 HVDC Systems

A classification of HVDC systems looks at their length and geographical extent. Back-to-back (BTB) systems are two-terminal systems with no transmission line inbetween, located in the same converter station (Fig. 2.3(a)). They are mainly applied for power transmission between two asynchronous systems or systems at different frequency (i.e. Japan) [105].

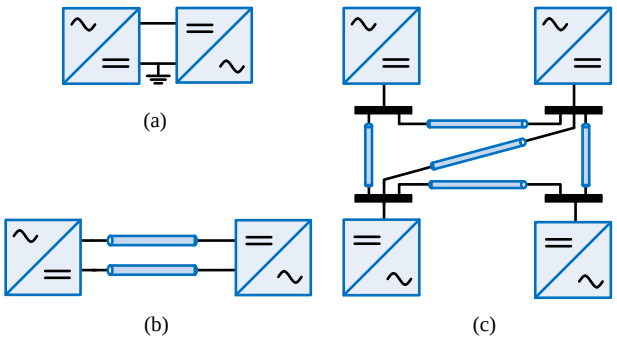


FIGURE 2.3: HVDC system configurations: (a) back-to-back (BTB) system, (b) point-to-point (PTP) system and (c) multiterminal (MTDC) system.

Systems with two separate terminals and a transmission line (either an overhead line, underground or undersea cable) are the most common applications of HVDC systems (Fig. 2.3(b)). Extended connections of HVDC converters create multiterminal systems or DC-grids (Fig. 2.3(c)).

2.3 Types of HVDC Computational Models

Modeling of HVDC systems and all related simulations are typically aimed at a specific application which defines the level of detail included in each model. Another benefit of this approach is that simulation tools, solving algorithms and computation times can be identified and selected accordingly. In order to facilitate such analysis, seven types of computational models have been defined to describe the level of detail included in a model [101]. These are:

Type 1 Full Physics Based Model

Type 2 Full Detailed Model

Type 3 Simplified Switchable Resistances Model

Type 4 Detailed Equivalent Circuit Model

Type 5 Average Value Model

Type 6 Phasor Model

Type 7 Root mean square (RMS) Load-Flow Model

Based on the above classification, the computational complexity of a model decreases as more simplifications are made. The detailed physics parameters required in Type 1

make the model extremely complex and difficult to simulate. Simplifications can be achieved by providing a generic but non-linear representation of switches (Type 2) and equivalent two-resistance switch models (Type 3).

Further simplifications through Thevenin/Norton equivalent circuits (Type 4) can lead to the development of average models where the switching functions are substituted by their averaged values (Type 5). Longer simulation times and system level evaluation such as simpler harmonic level analysis and load flows is then achieved with Type 6 and Type 7 models.

The level of detail in a model does not only define the computation time required for a specific system study but also the hardware requirements for developing real-time simulations and interfacing with external equipment in hardware-in-the-loop (HiL) configurations, a critical element of HVDC modeling and validation that will be discussed in following contents.

2.4 Review of HVDC Benchmark Models

Unsurprisingly, the first HVDC benchmark models were developed for LCC-HVDC systems. The CIGRE *"First Benchmark Model"* [106, 107] with the detailed parameters of a $\pm$500 kV, 1000 MW PTP transmission system has been the basis of a number of studies on LCC-HVDC systems and implemented as an HVDC transmission example in many simulation software (Table 2.1). The models has since seen multiple revisions to its converter, filter and control parameters [108, 109] as well as a redesign for 60 Hz networks [110]. An additional LCC-HVDC model was developed for comparison between the NETOMAC and EMTP EMT simulation software in [111] while a benchmark model for a CCC BTB HVDC system was proposed in [112]. The CCC benchmark model, developed by the CIGRE B4-34 working group, was based on the Garabi (Brazil - Argentina) HVDC link.

The first 2L-VSC topologies were installed and commissioned in 1999 - 2000. However, despite their relative popularity in HVDC projects and the immense research interest they have attracted over the last 20 years, a benchmark model for the 2L-VSC HVDC is not commonly available. The same also applies to the 3L-VSC topology that has seen limited development in the mid-2000s. Since 2L/3L converters are no longer considered for the use in HVDC systems, it is expected that such a model will be made unavailable. Just in 2010, a benchmark model based on VSC topologies were proposed for phasor level simulations and DC-grid studies [113].

Interest in VSC-HVDC benchmark models was sparked by the development and subsequent commercial success of the MMC topology. A detailed MMC model was established

for the planning of the Spain/France MMC-HVDC interconnector in 2012 [114]. In 2013, an extended benchmark model of MMC-based VSC-HVDC was developed by CIGRE B4-57 and B4-58 working groups [101, 115]. The model includes a total of 11 MMC terminals in multiple grid configurations and two different voltage levels (±200 kV and ±400 kV). The benchmark model also included two DC-DC converters for HVDC applications, an application that has not seen any practical demonstration and is considered as a critical element for the future development of DC-grids with multiple voltage levels. The original CIGRE model has then been developed for both commercial real-time power system simulation platforms, RSCAD by RTDS Inc. and HYPERSIM by Manitoba Hydro and OPAL-RT [116].

In order to address the gap of the CIGRE model, which focused predominanty in the integration of offshore wind farms with VSC-HVDC, a model that combined LCC-HVDC with VSC-HVDC systems in an extended AC/DC grid was proposed by the State Grid Research Institution of China (SGRI). In addition to this model, a simplified benchmark model for interconnection of two AC systems was also built [117]. Following the development of hybrid and modular multilevel topologies, a benchmark model of an AAC-based PTP VSC-HVDC was also developed for real-time studies [25, 118].

In total, there are eleven HVDC benchmark models currently available in the literature, predominantly developed for phasor, EMT and power flow studies. In addition, CIGRE WG B4-72 working group in 2020 develops a comprehensive DC grid benchmark model, which combines the summarized seventh, ninth and tenth benchmark models (Fig. 2.4). A comprehensive summary of these benchmark models is provided in Table 2.1.

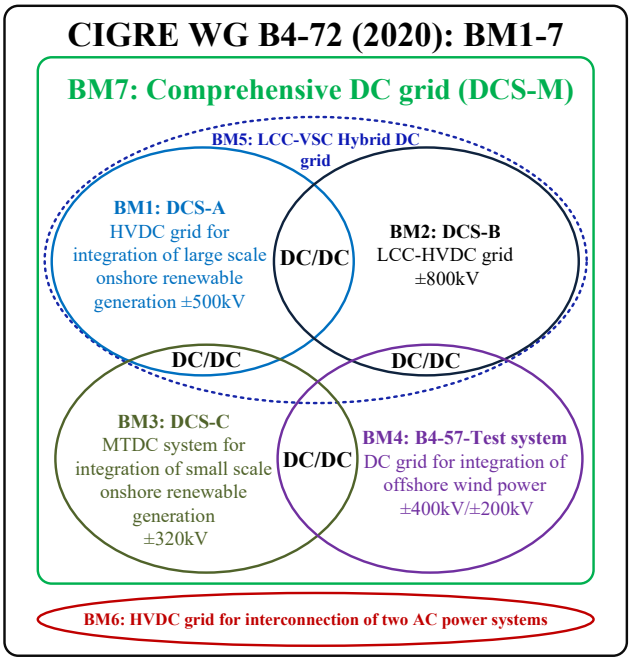


FIGURE 2.4: CIGRE B4-72 comprehensive DC grid benchmark model.

TABLE 2.1: Summary of HVDC benchmark models.

Year	Technology	Voltage (kV)	Power (MW)	Terminals	Line (km)	Software/ Hardware	Study	Model type	Ref.
1991	LCC	500	1000	2	UGC (100)	FGH Parity Simulator EMTDC EMTP NETOMAC	EMT	DE (4)	[107] [106]
1994	LCC	500	1000	2	UGC (100)	No data	EMT	DE (4)	[108]
1995	LCC	400	600	2	USC (66) OHL1 (43) OHL2 (42)	EMTP NETOMAC	EMT	DE (4)	[111]
2008	CCC	±500	2000	2	UGC (1000)	PSCAD/EMTDC	EMT	DE (4)	[112]
2010	VSC	±500 ±320	1400	1	UGC	No data	Phasor	PM (6)	[113]
			1000 700	2					
			1000 700	2					
			1400 600 400	3 (DC Hub)					
2012	MMC	±320	1000	2	UGC (70)	EMTP	EMT	AVM (5)	[114]

Year	Technology	Voltage (kV)	Power (MW)	Terminals	Line (km)	Software/ Hardware	Study	Model type	Ref.
2013	MMC	DCS1: ±200	8000	2	UGC (200)	MATLAB RSCAD HYPERSIM	Power Flow EMT RT	AVM (5) RMS (7)	[101]
		DCS2: ±200	200 800 1200	4	UGC (500) OHL (100)				
		DCS3: ±400	2×400 2×800 2×1200	5	UGC (900) OHL (1400)				
2014	LCC	500	1000	2	UGC (100)	PSCAD/EMTDC	EMT	DE (4)	[110]
2015	LCC/VSC	DCS-A: ±500	No data	4	OHL (2500)	PSS/E	Power Flow	RMS (7)	[117]
		DCS-B: ±800		7	OHL (6250)				
		DCS-C: ±320		2	OHL (500)				
		DCS-D: ±400		6	UGC (1050) OHL (1300)				
2015	VSC	±800 ±500 ±400	1×1000 1×1500 2×3200 5×7000 3×14000	13	OHL (9100)	PSS/E	Power Flow	RMS (7)	[117]
2019	AAC	±200	800	2	UGC (200)	RSCAD	RT	DE (4)	[118]

DE: Detailed equivalent circuit models PM: Phasor models AVM: Average value models RMS: RMS load flow models RT: Real-time
OHL: Overhead line UGC: Underground cable USC: Undersea cable

2.5 Discussion and Conclusion

2.5.1 Research Gaps in Benchmark Models

With the rapid development of HVDC technology, continuous increase in voltage level and capacity expansion of multiterminal networks, HVDC systems are again a very important research topic. However, HVDC transmission now is not limited to a small range of PTP transmission systems. For long-distance, high-power transmission, UHVDC is the first choice, but currently there is no established benchmark models for UHVDC transmission. Such a model, that removes some of the assumptions in the development of studies and control methods will set the basis for further research in the field potentially contributing to improve economic efficiency and pave the way for future large-scale UHVDC project construction.

There is also plenty of room for further development of the existing multiterminal benchmark models. Although the CIGRE DCS benchmark model and the SGRI DCS-M large-scale model can be used to conduct related multiterminal model research at this stage, the two models still have some limitations, as they were both created to meet specific project requirements. The CIGRE DCS benchmark model was developed for the integration of offshore wind farms and only considers a single topology, the MMC, as the basis of its converters. SGRI's DCS-M is a versatile benchmark model that covers onshore renewable energy grid, energy storage and long-distance power transmission studies but also offers room for improvement. For instance, it uses simple AC network models at both ends of the interconnections which removes some of the complexities in integrating large DC systems into AC networks. Some other gaps in existing benchmark models are:

i) models suited for large-scale AC and DC-grid studies,

ii) models for validation of grid support functions (for example virtual inertia) by HVDC systems,

iii) coordination of multiple converters to address issues such as controller interoperability and multi-vendor system compatibility - as analyzed in [119].

2.5.2 Data Availability

A critical element of all benchmark models is their openness, typically through availability of appropriate data so that the models can be used for different studies and across various software. The nature of the first HVDC benchmark model [108] is relatively simple, especially compared to modern implementations so a full of set of data (e.g. voltages,

converter and line impedances, transformer ratios, firing and extinction angles, short-circuit-ratios (SCR)). Therefore, a large number of model simulation studies have been performed based on this HVDC benchmark model, such as control improvement, small signal analysis, modeling method, etc. [120–127]. A similar approach in data availability can be seen in the development of the CCC model, with the proposed benchmark model verified through PSCAD/EMTDC and ATP simulations [112].

With regards to VSC-HVDC benchmark models, the 401-level MMC benchmark model [114] has detailed converter parameters for EMT type simulations together with associated results for validation while the AAC benchmark model has been fully developed for the RTDS real-time digital simulator with detailed parameters of the HVDC stations, transmission lines, and control parameters openly provided.

For larger benchmark models, data availability becomes a more complex issue. For example, the North Sea VSC-HVDC benchmark test system [113] only provides basic data, i.e. DC voltage levels and converter power ratings. Additional details are provided in the SGRI DCS-M benchmark model [117] although the full details of power rating cannot be easily found on the Internet. The CIGRE DCS models [115] are currently the most open DC-grid models in terms of data availability which has facilitated further developments for example through model conversion to real-time simulators.

The above discussion signifies the importance of developing fully open benchmark models for HVDC converters, HVDC systems and DC grid studies. Broader industry participation and direct involvement in what benchmark models and studies and what high-level assumptions can be made for HVDC systems can help in focusing research efforts around the world without the need for multiple validations of proposed approaches, for example how a particular design choice might exaggerate or obfuscate certain HVDC converter or system behaviors.

2.5.3 Expansion of Types and Complex Models

As the nature of studies involving HVDC systems is continuously expanding, it is necessary that benchmark models provide the same versatility and be available - to the extent that it is possible - for multiple simulation types. The CIGRE DCS model [101] and its current availability for multiple simulation types provides a practical example of the benefits of such an approach.

An additional benefit from co-ordinated benchmark development with open data that can be easily interchanged would be the expansion into extended and more complicated models. These extended HVDC models can be derived by combination or integration of

two or more smaller benchmark models, e.g. for multiterminal system studies, embedded HVDC systems, extended DC-grids, etc.

It is envisioned that open and fully developed benchmark models across multiple softwares/harwares from academia and industry will provide reliable reference basis, available parameter selection, and allow performance comparison of different HVDC systems.

Chapter 3

Topologies for Hybrid HVDC Systems

3.1 Introduction

The LCC and VSC are the two main technologies in current HVDC projects. The modular VSC technology has the most potential for future MTDC systems due to its modularity, scalability and improved harmonic properties of output voltage waveforms. Compared to the LCC, the VSC can regulate power flow flexibly and absorb/generate reactive power independently. Although the LCC lacks flexible power reversal capability and has to be equipped with additional AC filters, the thyristor-based LCC is still the best choice for bulk power or long-distance UHVDC transmission because of the high current and voltage ratings of thyristors. LCC and VSC topologies can be used in different power transmission scenarios, and the combination of various LCC and VSC topologies is a promising solution in future more complex HVDC systems. The state-of-the-art MMC and DC-fault tolerant AAC are the two representative modular VSC topologies, which are also used for the study of hybrid HVDC systems combining with the LCC in the following chapters of this thesis.

This chapter aims to provide an overview of the LCC, MMC and AAC for the development of hybrid HVDC systems. The system topologies, operation characteristics and control schemes of the LCC, MMC and AAC are analyzed comprehensively.

3.2 Line-Commutated Converter (LCC)

The technology of LCC was developed rapidly from 1970s to 1980s [128]. The LCC is a conventional and mature HVDC technology, which is suitable for UHVDC transmission due to the large voltage and current rating of thyristors [129]. The LCC uses thyristor-type

valves to commutate and works at foundamental frequency, hence the switching losses are less than the VSC [1, 3]. Considering better harmonic performance, double 6-pulse (12-pulse) bridge is usually used in LCC-based HVDC projects. The past few decades have seen the maturity of the LCC. The analysis and operation of the LCC have been reported extensively in the literature [1, 3, 49, 50, 53, 129–137]. This following section describes the basic topology, operation and control of the LCC.

3.2.1 Basic Topology and Operating Principles of the LCC

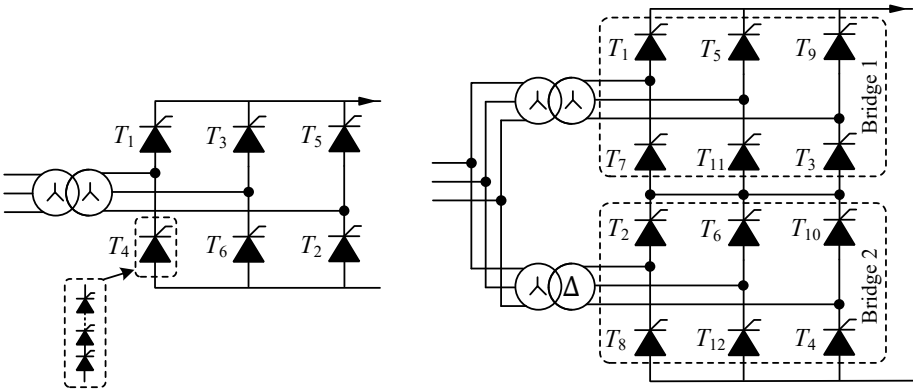


FIGURE 3.1: Converter topology of the LCC: (a) 6-pulse converter and (b) 12-pulse converter.

Fig. 3.1(a) and (b) depict the LCC in the rectifier side with 6-pulse and 12-pulse converter, respectively. Each phase-leg of the LCC has a thyristor valve with several series-connected thyristors. The thyristors of the LCC perform switch-on operation, while have to be forced to switch off. Each thyristor valve switches on with pulse signals generated by the firing angle, and the switching orders follow with the number sequence of thyristor valves in the figure. If the commutation process is ignored, there are only 2 valves (4 valves for 12-pulse converter) to be switched on at the same time, and the ideal no-load average DC voltage can be expressed as:

$$V_{dcr1} = kNV_{2tr}\cos\alpha, \tag{3.1}$$

where k is $3\sqrt{2}/\pi$ for a 6-pulse thyristor bridge, N represents the number of 6-pulse converters ($N = 2$ in 12-pulse converter), V_{2tr} refers to the rms value of line-to-line voltage in the secondary side of transformer, and α is the firing angle. However, the commutation process has to be considered due to the non-negligible system inductance. During the commutation process, three valves are switched on together leading to the overlap of

valve currents, hence the average DC voltage is decreased following with:

$$V_{dcr2} = kNV_{2tr}\cos\alpha - \frac{3N\omega L_{cr}}{\pi}I_{dc}, \tag{3.2}$$

where L_{cr} is the commutation inductance (leakage inductance of transformer) in rectifier side. Similarly, the average DC voltage for the LCC in inverter side can be calculated as:

$$V_{dci} = kNV_{2ti}\cos\beta + \frac{3N\omega L_{ci}}{\pi}I_{dc}, \quad \text{and} \tag{3.3}$$

$$V_{dci} = kNV_{2ti}\cos\gamma - \frac{3N\omega L_{ci}}{\pi}I_{dc}, \tag{3.4}$$

where β is the advance angle, γ is the extinction angle and $\pi = \alpha + \beta = \alpha + \gamma + \mu$ (μ is the commutation or overlap angle).

The DC voltage of 6-pulse and 12-pulse LCC contains $6k$ and $12k$ order characteristic harmonics, respectively. Moreover, the AC current for Yy or Yd connected transformer contains $6k \pm 1$ characteristic harmonics without considering commutation process as:

$$\begin{aligned} i_{Yy} = \frac{2\sqrt{3}}{\pi}I_d(&\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t \\ &+ \frac{1}{13}\cos 13\omega t - \frac{1}{17}\cos 17\omega t + \frac{1}{19}\cos 19\omega t...), \qquad \text{and} \end{aligned} \tag{3.5}$$

$$\begin{aligned} i_{Yd} = \frac{2\sqrt{3}}{\pi}I_d(&\cos\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t \\ &+ \frac{1}{13}\cos 13\omega t + \frac{1}{17}\cos 17\omega t - \frac{1}{19}\cos 19\omega t...). \end{aligned} \tag{3.6}$$

The 12-pulse LCC uses a set of Yy and Yd connected transformer cancelling out the $(12k - 6 \pm 1)$ order harmonics, thus the AC current for the 12-pulse LCC is:

$$i_{Yy,Yd} = \frac{4\sqrt{3}}{\pi}I_d(\cos\omega t - \frac{1}{11}\cos 11\omega t + \frac{1}{13}\cos 13\omega t - \frac{1}{23}\cos 23\omega t + \frac{1}{25}\cos 25\omega t...). \tag{3.7}$$

Eq. (3.7) shows there are only $12k \pm 1$ order characteristic harmonics in the AC current for Yy and Yd connected transformer, hence the tuning points of AC filters should be set at $12k \pm 1$ order, especially the 11^{st} and 13^{rd} characteristic harmonics.

Since the existence of harmonics in DC link and AC side, the LCC is necessary to be equipped with AC and DC filters. Additionally, AC filters play the role of reactive power compensation. The configuration of AC and DC filters are discussed in Chapter 3.2.3. The next section analyzes the conventional and improved control schemes of LCC.

3.2.2 Control Schemes of the LCC

3.2.2.1 Conventional Control Schemes

The LCC in the rectifier and inverter side generates firing signal to thyristor valves via different control modes [128, 130]. For the LCC in the rectifier side, there are four conventional control modes:

i) direct firing angle (α) control that a constant firing angle is set for the LCC in the rectifier side.

ii) DC current (I_{dc}) control that the DC current is controlled to be constant via the dynamic adjustment of the firing angle.

iii) DC power control (P_{dc}), but it is generally achieved by controlling the DC current derived from the expected DC power.

iv) DC voltage (V_{dc}) control that the firing angle is adjusted dynamically via the DC voltage controller to maintain constant DC voltage.

Moreover, the LCC in the inverter side can adopt:

i) direct advance angle (β) control and the advance angle is below 90° due to the firing angle is above 90° for the LCC in the inverter side.

ii) direct extinction angle (γ) control that the extinction angle is maintained to be constant via the adjustment of advance angle.

iii) DC current (I_{dc}) control that the output DC current tracks the specified reference by adjusting the advance angle in the inverter side.

iv) DC voltage (V_{dc}) control that the DC voltage is maintained to be constant by the DC voltage controller in the inverter side.

Table 3.1 summarizes the 13 possible combination schemes. Scheme 6 and 7 are the two commonly used control strategies in commissioned LCC-based HVDC projects considering control flexibility and automatic control capability [128]. In the control scheme 6, the LCC in the rectifier side adopts constant DC current control and the extinction angle is controlled by the inverter side, while the inverter side in the control scheme 7 controls the system DC voltage. The steady-state operating points for two schemes are shown in Fig. 3.2(a) and (b), respectively.

TABLE 3.1: Basic control schemes of the LCC.

Terminal \ Scheme	1	2	3	4	5	6	7	8	9	10	11	12	13
Rectifier	α	α	α	α	I_{dc}	I_{dc}	I_{dc}	P_{dc}	P_{dc}	P_{dc}	V_{dc}	V_{dc}	V_{dc}
Inverter	β	γ	I_{dc}	V_{dc}	β	γ	V_{dc}	β	γ	V_{dc}	β	γ	I_{dc}

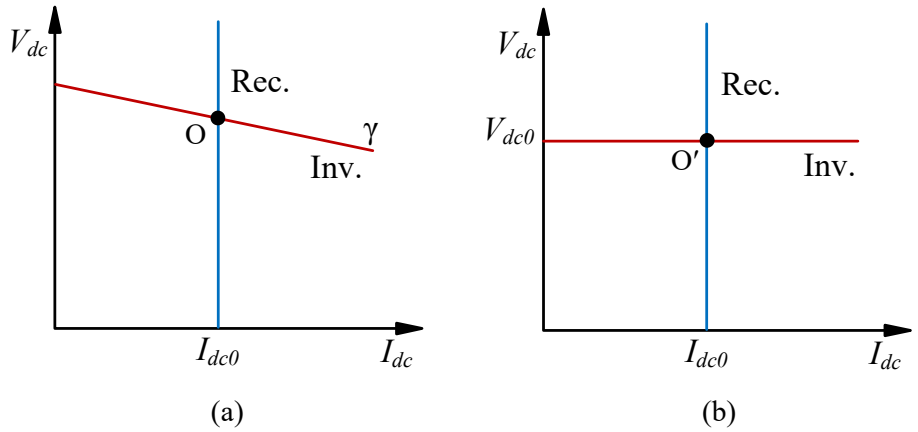


FIGURE 3.2: Conventional control schemes of the LCC: (a) control scheme 6 and (b) control scheme 7.

However, the above described conventional control schemes for the LCC do not include backup control. The next section discusses improved control schemes of the LCC including the limitation of minimum firing angle, maximum advance angle and minimum extinction angle, and VDCOL control for avoiding commutation failures and assisting fault recovery.

3.2.2.2 Improved Control Schemes

Fig. 3.3 depicts the corresponding improved control schemes of scheme 6 and 7. The V-I characteristic curves for the LCC in the rectifier side and inverter side consist of 4 sections and 6 sections, respectively. The 4 sections of the LCC in the rectifier side describe the following control characteristics:

- AB (A′B′): minimum firing angle control characteristic,
- BC (B′C′): constant DC current control characteristic,
- CD (C′D′): VDCOL control characteristic in the rectifier side, and
- DE (D′E′): constant DC current control characteristic after VDCOL.

The 6 sections of the LCC in the inverter side describe:

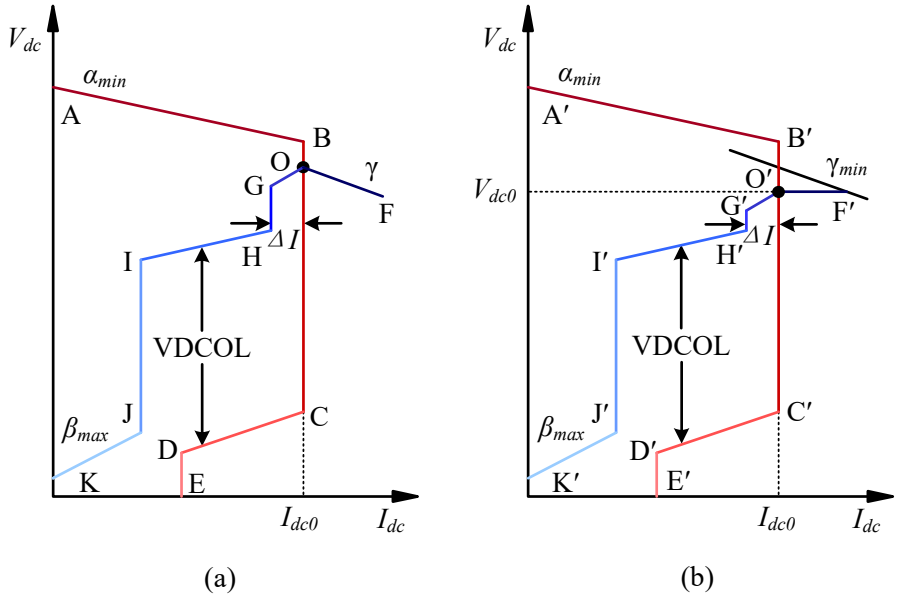


FIGURE 3.3: Improved control schemes of the LCC: (a) improved control scheme 6 and (b) improved control scheme 7.

- FO (F′O′): constant extinction angle control characteristic (constant DC voltage control characteristic with minimum extinction angle limitation),
- OG (O′G′): DC current deviation (ΔI) control characteristic,
- GH (G′H′): constant DC current control characteristic,
- HI (H′I′): VDCOL control characteristic in the inverter side,
- IJ (I′J′): constant DC current control characteristic after VDCOL, and
- JK (J′K′): maximum advance angle control characteristic.

It is noted that the VDCOL control sets in rectifier side guarantees smooth recovery of DC current from AC faults, while the risk of commutation failures can be reduced if it is set in inverter side [50, 138]. In addition to the described improved control schemes, the LCC can also adjust AC system frequency and reactive power to satisfy some other specific requirements such as offshore wind farm connection [135].

3.2.3 AC and DC Filters of the LCC

AC and DC filters in the LCC include both passive and active filters, and passive filters are commonly used in commissioned HVDC projects. The passive filters can be divided into:

i) tuned filters (e.g. single-tuned filter, double-tuned filter and triple-tuned filter) and

ii) damped filters (e.g. single-tuned damped filter, double-tuned damped filter, triple-tuned damped filter and C-type damped filter).

In damped filters, additional resistors are connected with inductors in parallel to provide damping characteristics for filters. The damped filters show better frequency deviation tolerance than the tuned filters and the resonance can be prevented, while the high impedance of damped filters at tuning points leads to relatively poor tuning performance [128, 130].

Fig. 3.4 shows the AC filter of CIGRE LCC benchmark model in rectifier side [106, 107] and a designed DC filter of the LCC, respectively. The AC filter in Fig. 3.4(a) is composed of a shunt capacitor, C-type damped filter (tuning point is set at 3^{rd}) and single-tuned damped filter (filtering 11^{st} harmonics). The designed DC filter in Fig. 3.4(b) is a double-tuned damped filter for filtering 12^{nd} and 24^{th} harmonics. Table 3.2 lists the parameters of AC and DC filters.

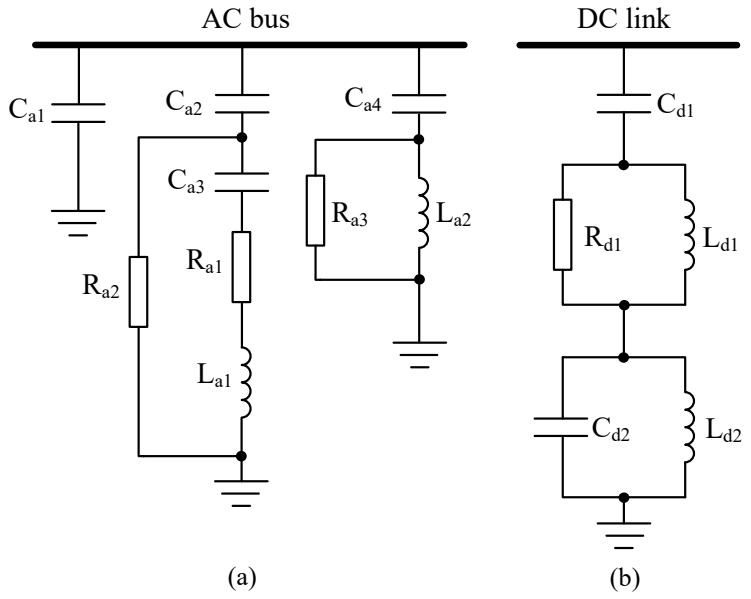


FIGURE 3.4: AC and DC filters of the LCC: (a) AC filter of CIGRE LCC benchmark model in rectifier side, and (b) a designed DC filter of the LCC.

In addition, the design of AC filters in the LCC has to consider the reactive capacity for compensating the reactive power consumption of the converter. Typically, the reactive power absorbed regardless converters in rectifier side or inverter side is about 40% to 60% of rated active power [128, 130]. The rated active power of CIGRE LCC benchmark model is 1000 MW, and the reactive power consumption is 542.4 MVar (54.24% of rated active power) [106, 107]. The total reactive capacity for the AC filter of CIGRE LCC

TABLE 3.2: Detailed paramerters of the AC and DC filters.

Parameters	**AC filter**			**DC filter**
	Shunt capacitor	3^{rd}	11^{st}	$12^{nd}/24^{th}$
Capacity (MVar)	125	250	250	-
C_{a1} (μF)	3.342	-	-	-
C_{a2} (μF)	-	6.685	-	-
C_{a3} (μF)	-	74.28	-	-
C_{a4} (μF)	-	-	6.685	-
L_{a1} (mH)	-	0.1364	-	-
L_{a2} (mH)	-	-	0.0136	-
R_{a1} (Ω)	-	29.76	-	-
R_{a2} (Ω)	-	261.87	-	-
R_{a3} (Ω)	-	-	83.32	-
C_{d1} (μF)	-	-	-	0.35
C_{d2} (μF)	-	-	-	0.81
L_{d1} (mH)	-	-	-	89.35
L_{d2} (mH)	-	-	-	48.86
R_{d1} (Ω)	-	-	-	10000

benchmark model in rectifier side is 625 MVar, hence it can compensate the reactive power consumption of the converter.

3.3 Modular Multilevel Converter (MMC)

Since the first MMC-HVDC project (Trans Bay Cable) was commissioned in 2010 [13], many MMC-based HVDC projects including the MTDC projects have been commisioned in succession or are now under construction. The MMC uses series-connected SMs rather than direct series-connected switches in each arm, which offers several salient features as modularity, scalability and excellent harmonic performance [2, 4, 4, 12, 14–19, 101, 114, 139–147]. Hence, the MMC is a potential candidate in HVDC transmission systems. The following sections first describe the topology of the MMC, then the operation and control of the MMC are discussed in detail.

3.3.1 Basic Topology and Operating Principles of the MMC

The schematic of a three-phase MMC is shown in Fig. 3.5. Each phase-leg of the MMC includes N SMs per arm in series and one arm inductor (L), and the arm inductor are used to limit the circulating current and the fault currents. There are various of SMs can

be used for the MMC including unipolar and bipolar SMs, as HBSM, FBSM, flying-capacitor SM, clamped-double SM, etc. [148]. The HBSM is the widely used simplest SM for the MMC, and the following description studies the HBSM-based MMC. The HBSMs in each arm of the MMC are controlled to generate the AC phase voltages, and the actual switching states decide the output voltage of each SM which is either equal to the capacitor voltage (v_c) or zero.

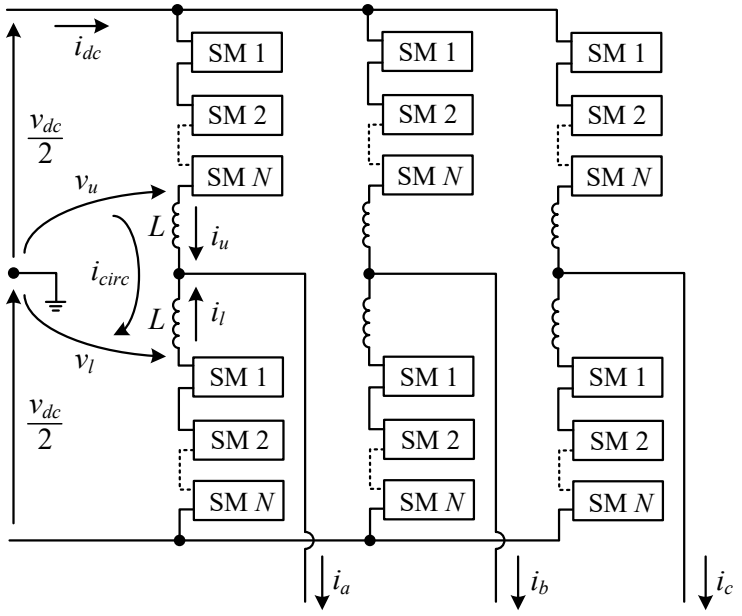


FIGURE 3.5: Three-phase topology of the MMC.

Employing the superposition theory, each phase-leg of the MMC can be separated into common mode circuit and differential mode circuit. The common and differential mode voltages (v_{commk} and v_{diffk}) can be expressed as:

$$v_{commk} = \frac{v_{uk} + v_{lk}}{2}, \qquad \text{and} \tag{3.8}$$

$$v_{diffk} = \frac{v_{uk} - v_{lk}}{2}, \tag{3.9}$$

respectively, where v_{uk} and v_{lk} are the voltages across to the upper and lower arm inductors, and k is the corresponding phase ($k \in (a, b, c)$). Similarly, the common and differential mode currents (i_{commk} and i_{diffk}) are:

$$i_{commk} = \frac{i_{uk} + i_{lk}}{2}, \qquad \text{and} \tag{3.10}$$

$$i_{diffk} = \frac{i_{uk} - i_{lk}}{2}, \tag{3.11}$$

respectively. The differential mode current in each arm also refers to the circulating current (i_{circk}) in this thesis, and the direction of circulating current is depicted in Fig. 3.5. Correspondingly, the arm currents (i_{uk} and i_{lk}) in three phases under balanced operating conditions can be obtained as:

$$i_{uk} = \frac{i_k}{2} + i_{diffk}, \qquad \text{and} \tag{3.12}$$

$$i_{lk} = \frac{i_k}{2} - i_{diffk}, \tag{3.13}$$

The differential voltage is employed to regulate circulating current in the MMC, which can also be expressed as:

$$v_{diffk} = L\frac{d}{dt}i_{diffk} = L\frac{d}{dt}i_{circk}. \tag{3.14}$$

Fig. 3.6 depicts the modulation waveform (v_{am}) and duty cycles (d_{ua} and d_{la}) in phase a, which are expressed as:

$$v_{am} = m_a \cos \omega t, \tag{3.15}$$

$$d_{ua} = \frac{1 - v_{am}}{2}, \qquad \text{and} \tag{3.16}$$

$$d_{la} = \frac{1 + v_{am}}{2}, \tag{3.17}$$

respectively, where m_a is the modulation index of the MMC and $m_a \in (0, 1)$. The number of SMs to be inserted/bypassed in each arm are determined by the modulation stage based on the above obtained duty cycles. The switching states (0 and 1) for upper and lower arms are defined as s_{uk} and s_{lk}, hence the voltages applied to the upper and lower arm

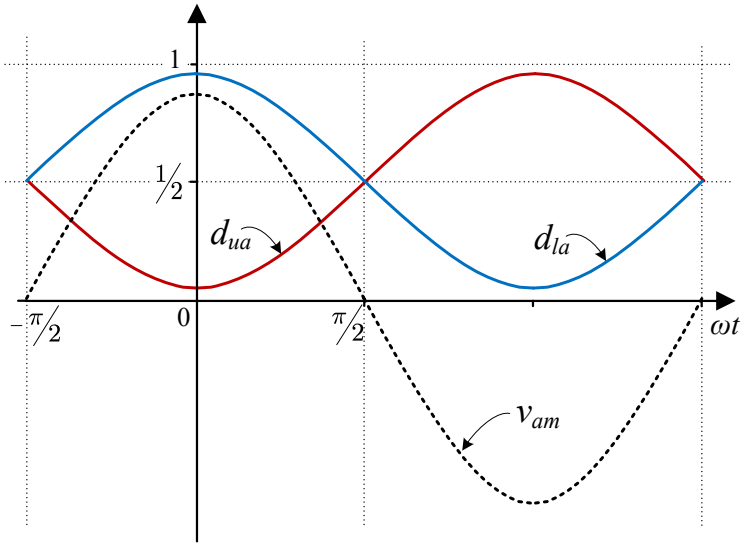


FIGURE 3.6: Operation of the MMC arms.

inductors (v_{uk} and v_{lk}) are:

$$v_{uk} = \frac{v_{dc}}{2} - \sum_{i=1}^{N}(s_{uki} \cdot v_{cuki} + i_{uk}R_{on} + \text{sgn}(i_{uk}) \cdot V_f), \qquad \text{and} \tag{3.18}$$

$$v_{lk} = -(\frac{v_{dc}}{2} - \sum_{i=1}^{N}(s_{lki} \cdot v_{clki} - i_{lk}R_{on} - \text{sgn}(i_{lk}) \cdot V_f)), \tag{3.19}$$

where v_{cuki} and v_{clki} are the capacitor voltages in upper and lower arms, R_{on} and V_f are the on-resistance and forward voltage drop across the MMC semiconductors, respectively.

3.3.2 Control Schemes of the MMC

3.3.2.1 Control Hierarchy

The control hierarchy of the MMC in HVDC consists of four main layers (Fig. 3.7). The function of the top layer (AC/DC grid control) is for necessary scheduling and dispatching. The second layer (coordinated system control) handles unscheduled events and defines the reference set-points for converters. The third layer (converter station control) performs the high level control of the MMC. The active/reactive power, node voltages/currents and frequency in the third layer are regulated based on the references. The bottom layer is the internal converter control, which is also the low-level control of the MMC that regulates the i) SM sorting, ii) SM energy, iii) circulating current and iv) arm energy [50, 51].

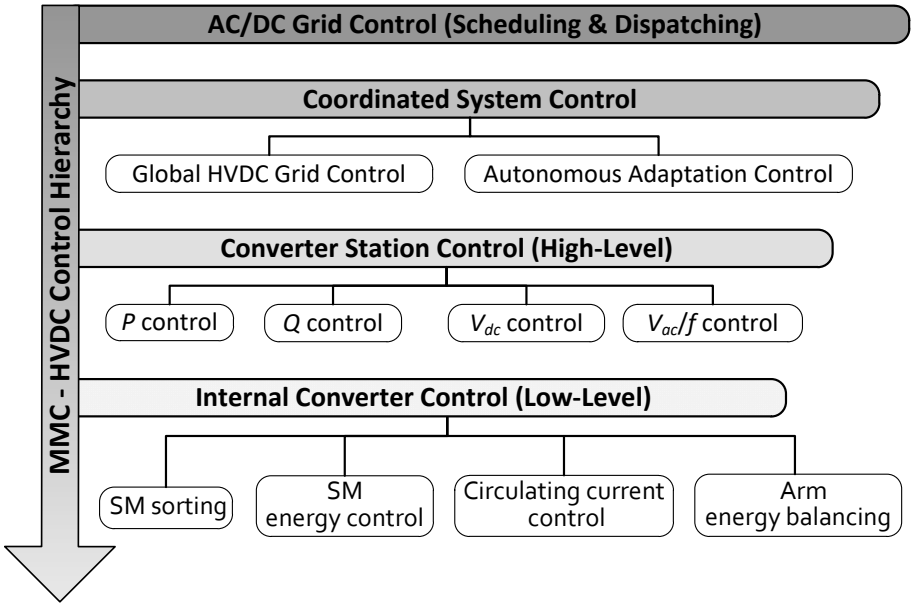


FIGURE 3.7: Control hierarchy of the MMC.

The high and low level control for the MMC can be divided into three main stages: i) outer controller, ii) inner current controller and iii) modulation & sorting. The outer controller for the MMC corresponds to the high level control generating the decoupled output current references (i_d^*, i_q^*) for inner current controller to calculate the final output voltage reference. The required number of SMs for each arm is determined in modulation stage and different modulation techniques can be applied while the nearest level modulation (NLM) is preferable to other pulse width modulation (PWM)-based methods with the increase of SMs [118]. The following section introduces the modulation techniques of the MMC.

3.3.2.2 Modulation Techniques

Different modulation techniques are used in the modulation stage to determine the switching states of SMs in the upper and lower arms based on expected modulation waveform. The typical modulation techniques are PWM- and staircase modulation-based methods. PWM-based methods deliver good tracking performance of modulation waveform with relatively simple implementation, and carrier-based PWM (CB-PWM), selective harmonic elimination PWM (SHE-PWM), space vector PWM (SV-PWM), etc. can be applied to the MMC. CB-PWM is the commonly used modulation scheme in multi-level converters, which can be classified into phase-shift PWM (PS-PWM) and level-shift PWM (LS-PWM) [139, 140, 142, 149].

The implementation of staircase modulation methods is simpler than PWM-based modulation methods with the increase of voltage levels [141]. The commonly applied staircase modulation method is NLM and two solutions can be used which are angle- and amplitude-based approaches. Based on (3.20) and (3.21), the pre-calculation of angles and reference voltage amplitude can be obtained. By comparison, the angle-based approach is more efficient than the amplitude-based approach due to less high frequency oscillations [101].

$$\theta_{(h,h+1)} = \sin^{-1}\left(\frac{2h}{N-1}\right), \tag{3.20}$$

$$N_{arm} = \frac{V_{dc}}{\bar{V}_c}, \tag{3.21}$$

where $\bar{V}_c$ is the average value of capacitor voltage.

3.3.2.3 SM Capacitor Voltage Balancing

The energy storage in DC-link of the MMC is maintained by series connected capacitors in arms, hence it is not only crucial to maintain constant DC voltage, but also to balance

all SM capacitor voltages. The widely used algorithm of SM capacitor voltage balancing is called "sort and select" [144]. Fig. 3.8 illustates the basic process of conventional SM capacitor voltage balancing algorithm, which are separated into three steps:

1) sorting SM capacitor voltages,

2) measuring arm current directions, and

3) selecting SMs to be inserted/bypassed based on arm current directions and instantaneous values of SM capacitors.

The sorting stage in the SM capacitor voltage balancing algorithm is intended to sort the SMs based on the detailed arm current directions, determined number of SMs to be inserted and current capacitor voltages [144]. However, PS-PWM can use simple proportional-integral (PI) controllers to regulate the SM capacitor voltages avoiding sorting stage, while the harmonic performance is reduced [41].

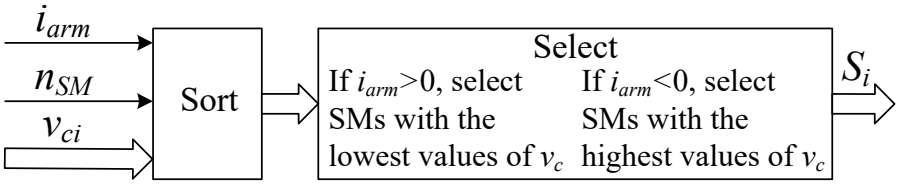


FIGURE 3.8: Conventional SM capacitor voltage balancing algorithm.

The conventional voltage balancing algorithm, while simple and efficient, will lead to high switching frequency. Various improved methods are reported in current literature for reducing switching frequency [146, 150, 151]. A modified algorithm, shown in Fig. 3.9, can reduce the switching frequency of SMs and ensure low complexity. This algorithm consists of descending sorting stage, ascending sorting stage and comparator to determine the selection of SMs. In addition, the restricted algorithm (Fig. 3.9(b)) can avoid additional switching transitions by adding a constant voltage offset K compared to the algorithm in Fig. 3.9(a), hence it further decreases switching frequency and losses [143].

3.3.2.4 Circulating Current Control

The circulating current control in the MMC also refers to arm current control, which can i) suppress second harmonic current, ii) maintain SM capacitor voltage, iii) regulate average SM energy and iv) balance upper/lower arm energy. The most commmly used methods for

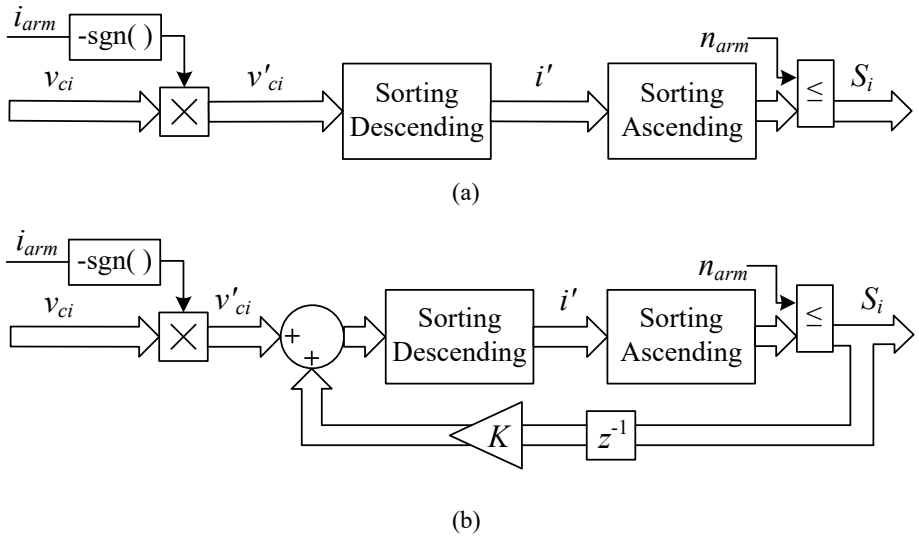


FIGURE 3.9: Modified SM capacitor voltage balancing algorithm: (a) conventional algorithm and (b) restricted algorithm.

arm current control are proportional-resonant (PR) controllers and double-frequency synchronous reference frame (DFSRF)-based techniques [145]. Circulating current suppression control (CCSC) and forced circulating current control (FCCC) are the two prevalent techniques representing the two commmly used methods [146, 147].

Eq. (3.22) shows that the differential currents in three phases consist of AC part (second harmonic current component) and DC part (one-third of the total DC current), and the steady-state second harmonic currents are of negative sequence. The purpose of CCSC is to eliminate the second harmonic AC component in differential currents. Two DC components ($i_{diff,d}$ and $i_{diff,q}$) can be obtained by transforming three-phase differential currents in the DFSRF as (3.23).

$$\begin{cases} i_{diffa} = \dfrac{I_{dc}}{3} + \hat{I}_{2a}\cos(2\omega t + \phi), \\ i_{diffb} = \dfrac{I_{dc}}{3} + \hat{I}_{2b}\cos\left[2(\omega t - \dfrac{2\pi}{3}) + \phi\right] = \dfrac{I_{dc}}{3} + \hat{I}_{2b}\cos(2\omega t + \dfrac{2\pi}{3} + \phi), \\ i_{diffc} = \dfrac{I_{dc}}{3} + \hat{I}_{2c}\cos\left[2(\omega t + \dfrac{2\pi}{3}) + \phi\right] = \dfrac{I_{dc}}{3} + \hat{I}_{2c}\cos(2\omega t - \dfrac{2\pi}{3} + \phi). \end{cases} \tag{3.22}$$

$$\begin{bmatrix} v_{diff,d} \\ v_{diff,q} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{diff,d} \\ i_{diff,q} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega L \\ 2\omega L & 0 \end{bmatrix}\begin{bmatrix} i_{diff,d} \\ i_{diff,q} \end{bmatrix}. \tag{3.23}$$

Fig. 3.10(a) shows the CCSC configuration based on (3.23). The differential current (i_{diff}) is first derived from arm currents following with (3.11), and PI controllers are used to minimize the second harmonic current via driving the two transformed DC components

to zero. The differential voltage references ($v_{diff,d}$ and $v_{diff,q}$) are finally obtained from PI controllers with feedforward coupling compensation. In general, CCSC suppresses the second harmonic current in differential current (circulating current), but it does not perform the average SM energy regulation, and upper/lower arm energy balancing [146].

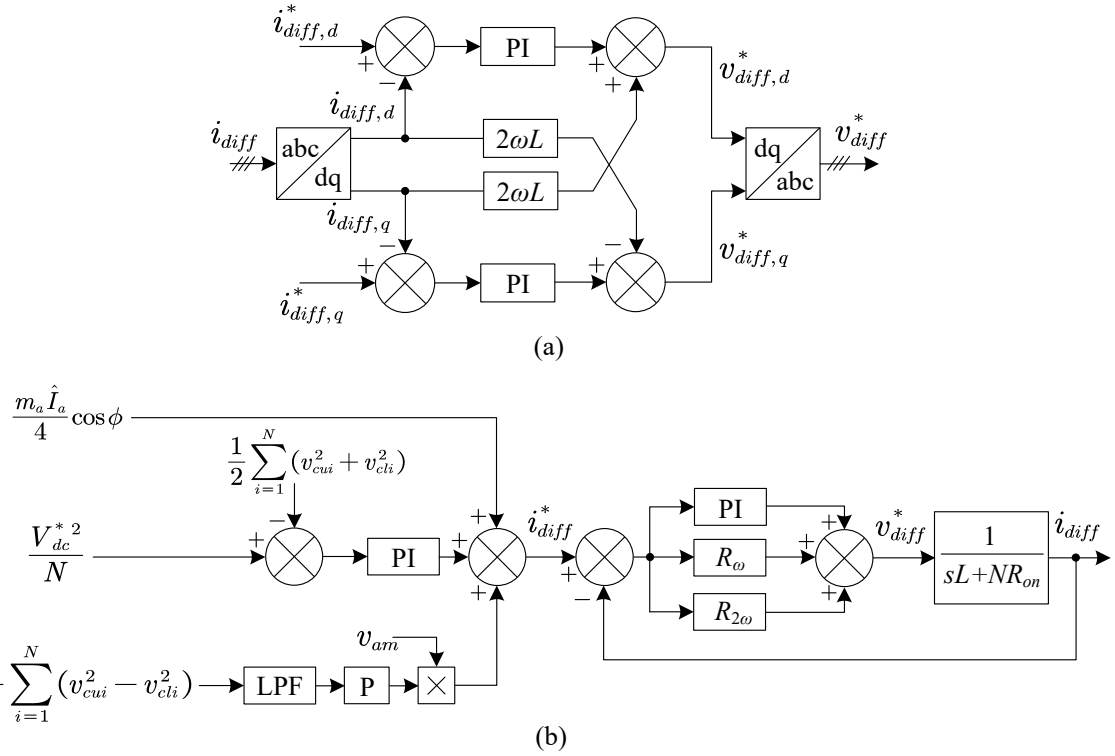


FIGURE 3.10: Circulating current controller: (a) CCSC and (b) FCCC.

Different from CCSC, FCCC is based on direct differerntial current control considering the average SM energy and energy exchange between the upper and lower arms in each phase. The first input in Fig. 3.10(b) defines the DC component ensuring the phase-leg energized, the second input maintains the average SM energy via a PI controller, and the third input balances the upper and lower arm energy in each phase by adding a fundamental frequency component. The differential current reference (i^*_{diff}) obtaining from the sum of three inputs is fed into the current controller composed of PI controller and resonant (R) controllers tuned at fundamental frequency and other even order harmonic frequencies. In addition to the DC component, the first input can also contain AC components with different even order harmonics for reducing the SM capacitor voltage ripples, while zero-sequence voltage injection can perform the same function by attenuating low frequency ripples in the capacitor voltages [147].

3.4 Alternate Arm Converter (AAC)

AAC belongs to the family of modular multilevel converters which combines the characteristics of the two-level converter and MMC in a modular topology [22–36]. Unlike the typical HBSM-based MMC, the AAC requires bipolar SMs, preferably FBSMs and provides DC-fault tolerant capability [37–41]. The alternate arm operation of the AAC leads to the decreased number of SMs in each arm and reduced total volume and losses [42–54]. Therefore, the AAC is a promising topology in the HVDC systems and future DC grids. The following sections describe the basic topology, operating principle, control schemes, and the extended overlap for the AAC.

3.4.1 Basic Topology and Operating Principles of the AAC

Fig. 3.11 shows the schematic of a three-phase AAC. Each arm of the AAC contains N series connected SMs (waveshaping circuit), one arm inductor (L), and one direct switch (DS) composed of IGBTs in series. Moreover, the AAC has reduced energy requirements compared to an MMC with similar voltage and power ratings but requires partial DC filtering due to the six-pulse harmonic in the DC-side. The extended overlap AAC (EO-AAC) offers reduced filtering requirements in the DC side, compared with short overlap AAC (SO-AAC), at the cost of increased number of devices, hence higher losses [49].

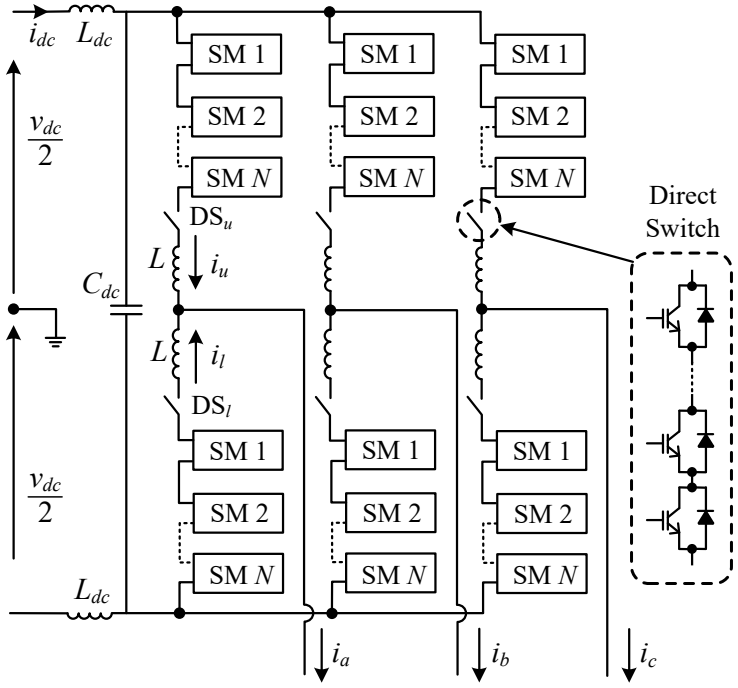


FIGURE 3.11: Three-phase topology of the AAC.

AAC can achieve over-modulation operation (m_a>1), and the two arms in each phase alternatively generate the AC output voltage and conduct the total AC current:

$$v_a = \frac{m_a V_{dc}}{2}\cos(\omega t), \tag{3.24}$$

$$i_a = \hat{I}_a \cos(\omega t + \phi). \tag{3.25}$$

The waveforms of duty cycles in the two arms of phase a are shown in Fig. 3.12 and the duty cycles can be expressed as:

$$d_{ua} = \frac{1 - v_{am}}{\hat{m}_a}, \qquad \text{and} \tag{3.26}$$

$$d_{la} = \frac{1 + v_{am}}{\hat{m}_a}, \tag{3.27}$$

where $\hat{m}_a$ is the maximum modulation index for the AAC. The total voltage in each arm of the AAC is lower than the full DC voltage due to the alternate arm operation, hence the number of SMs each arm for the AAC is:

$$N_{SM} = \frac{\hat{V}_a}{V_c} = \frac{\hat{m}_a V_{dc}}{2V_c}. \tag{3.28}$$

In addition, the peak voltage stress of DSs is the half of DC voltage as:

$$\hat{V}_{DS} = \frac{V_{dc}}{2}, \tag{3.29}$$

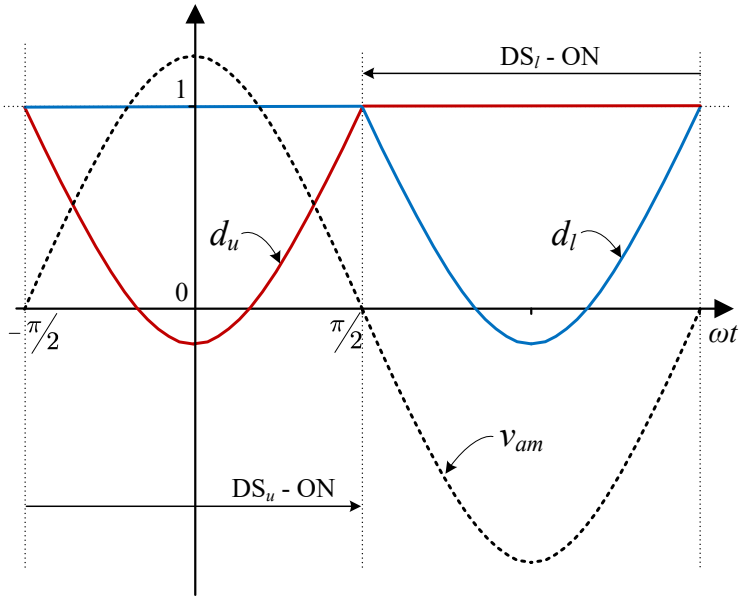


FIGURE 3.12: Operation of the AAC arms.

thus the number of devices in each DS per arm is:

$$N_{DS} = \frac{\hat{V}_{DS}}{V_c} = \frac{N_{SM}}{\hat{m}_a}. \tag{3.30}$$

3.4.2 Control Scheme of the AAC

3.4.2.1 Control Hierarchy

The control hierarchy of the AAC also consists of four main layers as shown in Fig. 3.13. The function of first three layers (AC/DC grid control, coordinated system control and converter station control) of the AAC is similar as the MMC which has been described in Section 3.3.2.1. The internal converter control (low-level control) of the AAC regulates the i) SM sorting, ii) SM energy, iii) zero-current switching, iv) circulating current and v) overlap period.

The switching signals of DSs and the required number of redunduant SMs are determined by the overlap period and circulating current controller, respectively. In addition to the aforementioned control, it is significant to achieve the zero current switching (ZCS) in the AAC for reducing the voltage stress of DSs, and on-load tap changer (OLTC) coordination can realize the region extension of ZCS [33].

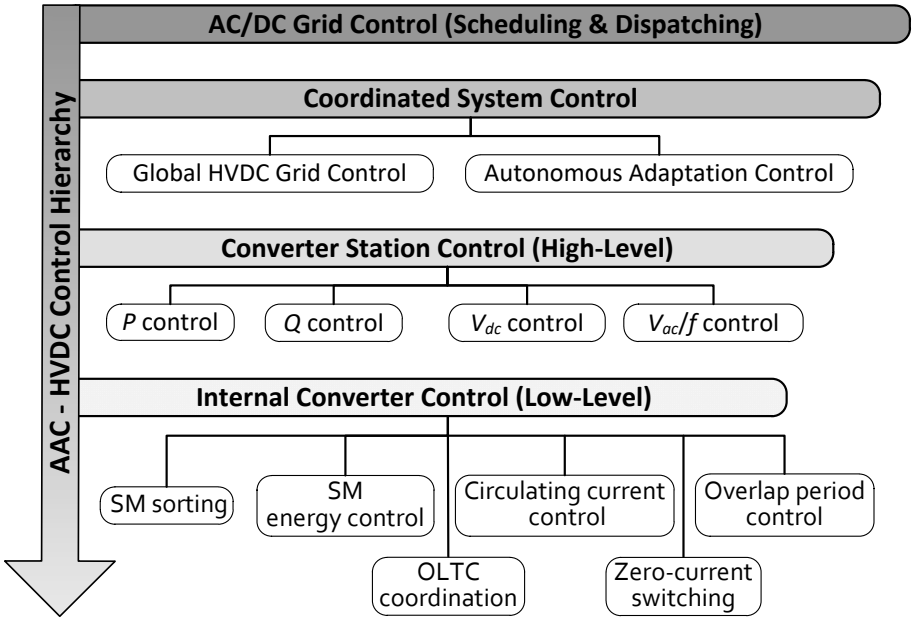


FIGURE 3.13: Control hierarchy of the AAC.

3.4.2.2 Energy Balancing Strategy

The inherent energy balancing point (standard operating point) for the AAC is called the "sweet-spot" ($m_a = M_a = 4/\pi$) that is determined by the zero net energy (3.33) from the energy exchange between AC side (3.31) and DC side (3.32).

$$E_{ac} = \int_{-T/4}^{T/4} \frac{m_a V_{dc} \hat{I}_a}{2} \cos(\omega t) \cos(\omega t + \phi) dt, \tag{3.31}$$

$$E_{dc} = \int_{-T/4}^{T/4} \frac{V_{dc} \hat{I}_a}{2} \cos(\omega t + \phi) dt, \tag{3.32}$$

$$\Delta E_{arm} = E_{ac} - E_{dc} = \frac{V_{dc} \hat{I}_a T \cos\phi}{8} (m_a - \frac{4}{\pi}). \tag{3.33}$$

In practical applications, the AAC could operate away from the sweet-spot causing energy surplus or deficit ($\Delta E_{arm} \neq 0$) within arms. The reported energy balancing methods in the literature are based on zero sequence current injection [37], overlap onset control (OOC) [40], overlap period [24] and circulating current gradient [30].

As described in Section 3.3.2.4, the circulating current is always present in the MMC which can be used to balance the arm energy. The six DSs in the AAC operate at foundamental frequency and two DSs in each phase-leg switch on/off alternatively, hence no circulating current presents in the AAC. A typical solution is to introduce an overlap period that the upper and lower DSs switch on together for mimicking the MMC operation enabling circulating current to balance arm energy. The overlap period and circulating current control is discussed in later sections.

3.4.2.3 Modulation and Direct Switch (DS) Control

Fig. 3.14(a) shows the schematic diagram of the modulation stage in the AAC. The AAC and MMC have similar topology structure, hence the commonly used modulation techniques in the MMC (Chapter 3.3.2.2) can also be applied in the AAC without modification. The modulation stage only defines the total number of SMs to be inserted in each arm if with the modulation techniques of CB-PWM and staircase. Hence, the detailed switching signals of SMs in the AAC are generated by the subsequent sorting and selecting algorithm.

Due to the introduction of DSs in the AAC, it is also necessary to determine the switching signals of all DSs. Upper and lower DSs in two arms of a phase-leg conduct half of cycle, respectively. Since the DSs only decide the alternate operation of six arms, comparators are used to generate the switching signals of DSs as Fig. 3.14(b) [41].

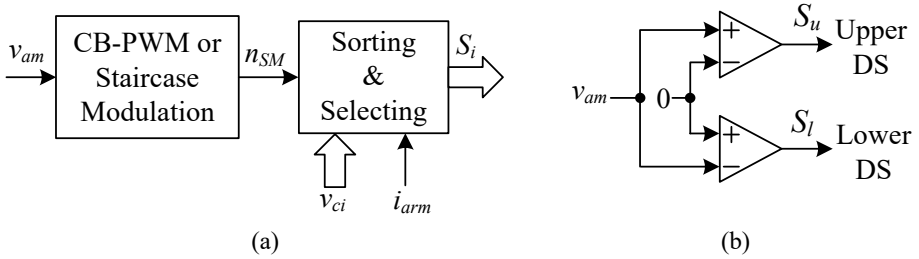


FIGURE 3.14: Modulation stage and direct switch control of the AAC: (a) modulation stage of the AAC and (b) direct switch control of the AAC.

3.4.2.4 Overlap Period Control

For achieving the arm energy balance in the AAC, an overlap period (t_{ov}) is introduced around the zero-crossing points of the modulation waveform for mimicking the MMC operation as shown in Fig. 3.15. The circulating current presents in the AAC during the overlap period, and the duration of overlap period defines the amount of energy exchanged by the circulating current. Moreover, the magnitude and direction of circulating current also influences such energy exchange [30].

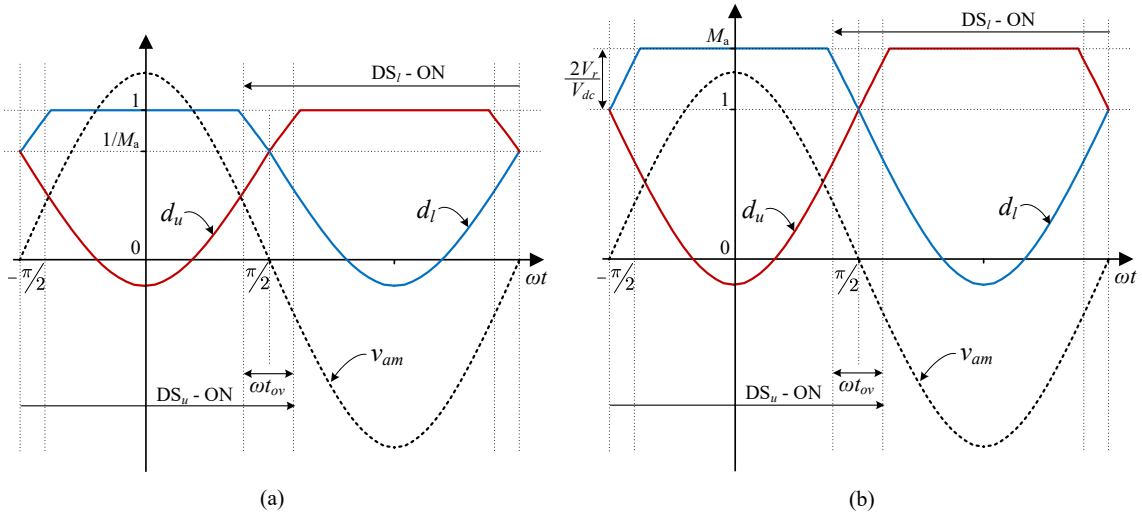


FIGURE 3.15: Overlap period configuration of the AAC: (a) conventional configuration and (b) configuration considering arm redundant voltage.

Fig. 3.15(a) and (b) show the conventional overlap period configuration of the AAC and configuration considering arm redundant voltage (V_r), respectively. For avoiding the output voltage distortion, the maximum achievable overlap period is defined as (3.34) considering the redundant arm voltage (3.35).

$$\hat{t}_{ov} = \frac{\pi - 2\cos^{-1}(\frac{M_a - 1}{m_a})}{\omega}, \tag{3.34}$$

$$V_r = NV_c - \frac{V_{dc}}{2}. \tag{3.35}$$

The overlap period for the AAC can be divided into "short-overlap" period and "extended overlap" period. The short overlap angle is typically in the range of 15° to 18°, which can be achieved by symmetrical- and asymmetrical-based fixed and variable overlap period [23, 43]. The extended overlap angle of the AAC is 60°, and the basic operation principle is discussed in Section 3.4.3.

3.4.2.5 Circulating Current Control

Section 3.3.2.4 has introduced the basic circulating current control of the MMC. The AAC mimics the MMC operation during the overlap period, hence the upper and lower arm currents in three phase legs are expressed as:

$$i_{uk} = \frac{i_k}{2} + i_{circk}, \qquad \text{and} \tag{3.36}$$

$$i_{lk} = \frac{i_k}{2} - i_{circk}, \tag{3.37}$$

In addition, the arm inductance determines the circulating current control dynamics of the AAC:

$$\frac{d}{dt} i_{circk} = \frac{1}{L} v_{diffk}. \tag{3.38}$$

The AAC has smaller arm inductance compared with the MMC that leads to fast rates of changes in circulating currents and arm currents.

The typical circulating current control methods for the AAC in current literature are classical PI control [38, 39], hysteresis control [23, 35] and gradient-based control [30].

3.4.2.6 Zero-Current Switch (ZCS) of the DSs

The alternate arm operation in the AAC leads to current interruption of arm inductors which will increase the voltage stress on the DSs. Moreover, the hard-switching of DSs also increases the switching losses of series-connected IGBTs in DSs. Therefore, ZCS should be ensured that forces the arm currents to zero before the DS is opened.

The LC resonant circuit composed of arm inductor and inserted SM capacitors during a fixed overlap period can achieve ZCS by generating a negative voltage across arm inductor [36]. Moreover, the double-band hysteresis current control based on asymmetric overlap period provides soft-switching for DSs without distorting current in the DC-link [23].

Also, the use of snubber circuits can reduce the voltage stress on DSs [34] and OLTC coordination can extend the ZCS region via changing tap positions of transformer [33].

3.4.3 Extended Overlap AAC (EO-AAC)

The principle of the EO-AAC aims to extend the overlap angle to $60°$ providing a full-time conduction path for DC current in one phase [44–46, 48]. Fig. 3.16 shows the conductions states of six arms in the AAC. There are six conduction states in one period describes as below:

- Conduction state 1: DS_{ua}, DS_{la}, DS_{uc} and DS_{lb} switch on $(-\frac{2\pi}{3} \leq \omega t \leq -\frac{\pi}{3})$
- Conduction state 2: DS_{uc}, DS_{lc}, DS_{ua} and DS_{lb} switch on $(-\frac{\pi}{3} \leq \omega t \leq 0)$
- Conduction state 3: DS_{ub}, DS_{lb}, DS_{ua} and DS_{lc} switch on $(0 \leq \omega t \leq \frac{\pi}{3})$
- Conduction state 4: DS_{ua}, DS_{la}, DS_{ub} and DS_{lc} switch on $(\frac{\pi}{3} \leq \omega t \leq \frac{2\pi}{3})$
- Conduction state 5: DS_{uc}, DS_{lc}, DS_{ub} and DS_{la} switch on $(\frac{2\pi}{3} \leq \omega t \leq \pi)$
- Conduction state 6: DS_{ub}, DS_{lb}, DS_{uc} and DS_{la} switch on $(\pi \leq \omega t \leq \frac{4\pi}{3})$

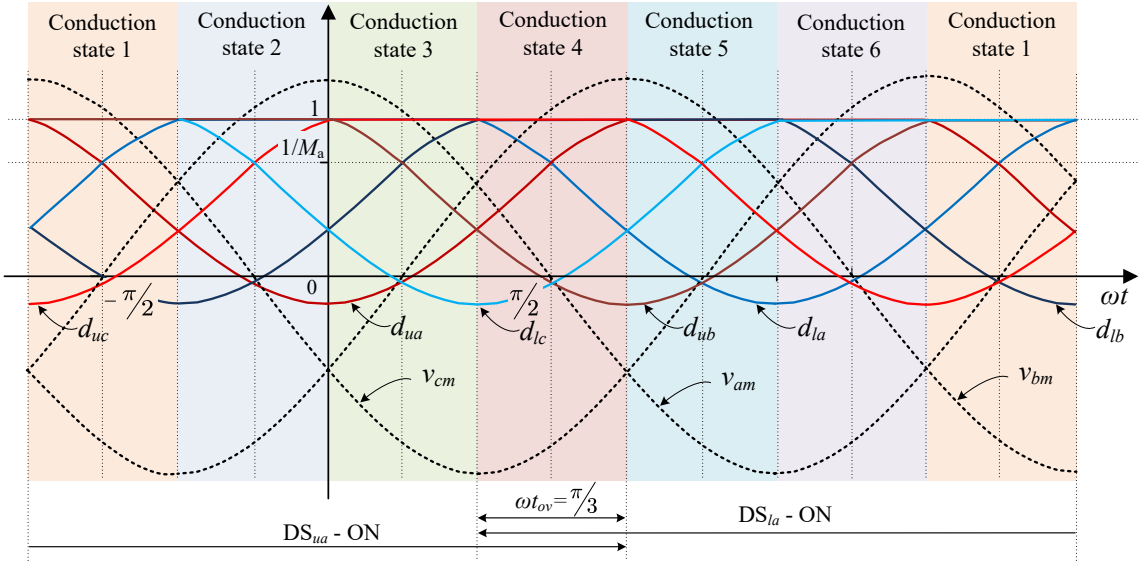


FIGURE 3.16: Extended overlap period configuration of the AAC.

Therefore, the AC currents can always circulate through upper and lower arms in one phase resulting in decoupling of DC and AC currents, and they are cancelled within converter. This also implies that no six-pulse ripples appear in the DC-link, hence EO-AAC

does not need to install DC filters. Another significant feature for EO-AAC is the elimination of energy balancing point (removal of sweet spot) because there is always a energy exchange path for DC and AC energy from DC-link to two arms in one phase, hence a wider AC voltage magnitude [45].

However, each arm for EO-AAC has to match the AC voltage during a longer time (more than half-cycle), hence more SMs are required. Although the zero sequence voltage injection can reduce the number of SMs by lowering the maximal voltage in each arm that SMs have to generate, the voltage rating of DSs (required number of IGBTs) will be increased. Another issue needs to be overcome for EO-AAC is the ZCS and active filtering cannot be achieved simultaneously as the circulating current can only control either of them. Detailed description of EO-AAC can be found in [44, 45].

3.5 Conclusion

The LCC is a conventional and mature HVDC technology which is suitable for bulk power transmission, while it has restricted power reversal capability and needs reactive power compensation. The VSC especially the modular VSC overcomes the drawbacks of LCC and has been commercially available. Although the state-of-the-art MMC and the emerging AAC all belong to the modular VSC topology, the typical MMC with HBSMs lacks the vital DC-fault tolerant capability. The emerging AAC presents DC-fault tolerant capability due to the use of bipolar SMs as FBSMs, hence the AAC is a potential candidate for MTDC systems and future DC grids.

The conventional LCC, state-of-the-art MMC and emerging AAC are the three basic topologies used in Chapter 4 to 7 for the verification of proposed generalized expression of DC power flow analysis and the development of different hybrid HVDC systems. The topologies, operating principles and control schemes of the three converters are described in detail with comprehensive theory analysis in this chapter. Besides, the design principle of AC/DC filters for the LCC and the extended overlap operation of the AAC are discussed as well.

Chapter 4

Modeling Approaches and Power Flow Analysis of HVDC systems

4.1 Introduction

This chapter first focuses on the available modeling approaches of HVDC systems including the EMT modeling, electromechanical transient modeling, dynamic frequency capturing modeling and the combination of different modeling methods. EMT modeling is the main focus in this chapter, which is analyzed from the aspects of different analysis methods in simulation tools, numerical integration theory, and possible parallel computation method. Detailed droop control theory for HVDC systems is also described which includes single P/V droop control, single I/V droop control and mixed P/V, I/V droop control. Based on the description of droop control, a generalized expression of DC power flow is proposed considering the initial power flow for normal operation and power flow after converter outage. A detailed equivalent model of a four terminal MMC-based DC grid in PLECS-Blockset and Simulink further verifies the accuracy of proposed generalized expression of DC power flow.

4.2 Modeling Approaches for HVDC Systems

The various digital simulation tools play significant role in the study of time-domain transient characteristics of HVDC systems [152]. The widely-adopted time-simulation methods can be classified into two major categories:

i) electromagnetic transient (EMT) simulation [153, 154] and

ii) electromechanical transient simulation [155, 156].

In addition to the two modeling methods, some other modeling approaches can also be used:

i) dynamic phasor (DP) modeling method based on time-varying Fourier transform [136, 157–160],

ii) shifted frequency phasor (SFP) modeling method based on frequency shift of complex signal [161–166], and

iii) co-simulation method combining different modeling approaches [167–171].

This section provides a detailed introduction of these modeling approaches for HVDC systems.

4.2.1 Electromagnetic Transient (EMT) Modeling

EMT simulation is a convenient method to study the dynamic behaviours of HVDC systems accurately, which can precisely capture the switching actions of different semiconductors due to the much smaller time step (usually 20-50 μs or even less). The modeling method of EMT simulation is based on the differential equations to describe the transient process of the whole AC and DC systems, while with complex computing procedure [153]. This section discusses the analysis methods in EMT programs, based on the numerical integration theory establishing discrete models. In addition, the general parallel computation method for HVDC systems is also summarized in this section.

4.2.1.1 Analysis Methods in EMT Programs

Three basic analysis methods can be employed for current in industry-grade EMT programs tailoring for both offline and real-time analyzes:

i) nodal analysis method represented by offline-simulation-based PSCAD/EMTDC [172], real-time simulation-based RSCAD [173] and HYPERSIM [174],

ii) state-space method represented by offline programs as MATLAB/Simulink [175] and Plecs [102], and

iii) state-space nodal (SSN) method typified by RT-LAB platform [176].

The process of nodal analysis can be divided into two steps [152]:

1) establishment of companion branch models by discretizing differential equations of dynamic system components via numerical integration.

$$\begin{cases} \dfrac{dx}{dt} = f(x,t), \\ x(0) = x_0, \end{cases} \tag{4.1}$$

where x is the system variables that can refer to inductor current and capacitor voltage, and x_0 is the known initial value.

2) combination of the discretized differential equations to create a system of nodal admittance matrix.

$$\boldsymbol{YV} = \boldsymbol{I} \tag{4.2}$$

The commonly used numerical integration method solving differential equations in nodal analysis is implicit trapezoidal integration based on Dommel simulation algorithm [177], which will be discussed in the following section in detail.

The state-space method uses diffential equations or differential-algebraic equations (DAEs) in state-space form describing the composite system:

$$\begin{cases} \dfrac{d\boldsymbol{x}}{dt} = \boldsymbol{Ax} + \boldsymbol{Bu}, \\ \boldsymbol{y} = \boldsymbol{Cx} + \boldsymbol{Du}, \end{cases} \tag{4.3}$$

where $\boldsymbol{x}$ is the system state vectors refering to inductor current and capacitor voltage, $\boldsymbol{u}$ is the input vectors, $\boldsymbol{y}$ is the output vectors, and the state-space matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$ and $\boldsymbol{D}$ correspond to the permutation of switches and piecewise linear device segments [178]. In addition, the automated state model generation method separates the composite system to different state-space groups, which can obviously reduce the system formulation time [179]. Variety of numerical integration methods can be used in solving the state-space equations depending on actual requirements. It is noteworthy that the system matrices in state-space method are independent of the simulation step size, hence both the fixed and variable step-size solvers can be adopted, and the variable step-size solvers can reduce simulation time, as different ODE solvers in Simulink [175].

However, massive switching events cannot be handled by the discrete state-space solvers efficiently. The SSN method combines the nodal and state-space methods together and adopts parallel computation with diakoptic analysis to accelerate simulation [178], which has been validated in RT-LAB by ARTEMiS (art 5) algorithm [176]. Additionally, the parallel computation is significant for HVDC systems as the switching states either for

LCC or VSC change many times per duty cycle. The basic solving process is described in Chapter 4.2.1.3.

4.2.1.2 Numerical Integration Theory

Based on the specific EMT process, the system components of HVDC systems can be described by lumped and distributed parameters, which are represented by ordinary differential equations (ODEs) and partial differential equations (PDEs), respectively. In addition, the nodal analysis method-based EMT simulation programs adopt discrete companion models to solve differential equations by numerical integration algorithms.

This section discusses the numerical integration theory in HVDC systems based on the nodal analysis method, while the state-space method is also based on the selection of numerical integration techniques after formulation. The key of discrete companion models aims to simplify the lumped energy storage components and distributed components into a combination of resistance and voltage source (Thevenin equivalent) or inductance and current source (Norton equivalent). In other words, the network equations described by differential equations are converted into the networks of algebraic equations via model discretization [152].

Numerical integration algorithms are typically divided into the explicit integration method and the implicit integration method. From the basic Euler method to improved Euler method (or trapezoidal integration method), Runge-Kutta (RK) method, Simpson method, Adams method, Gears method, etc [180], the selection of a proper integration algorithm for HVDC systems should be considered from the three aspects:

i) the numerical stability,

ii) the local truncation error and

iii) the self-startup characteristic.

In general, the implicit integration method shows better performance in the aspect of numerical stability and local truncation error than explicit integration method, while it requires estimation and iteration due to the lack of self-startup capability [152, 180].

According to the above analysis, the EMT simulation of HVDC systems usually adopts the implicit Euler method and trapezoidal method. Moreover, the implicit Euler method is also the Gear 1 method, and the trapezoidal method belongs to the RK 2 method. The following contents analyze the resistance-inductance (R-L) series branch, inductance branch (Fig 4.1) and capacitance branch based on the two integration methods (Fig 4.2).

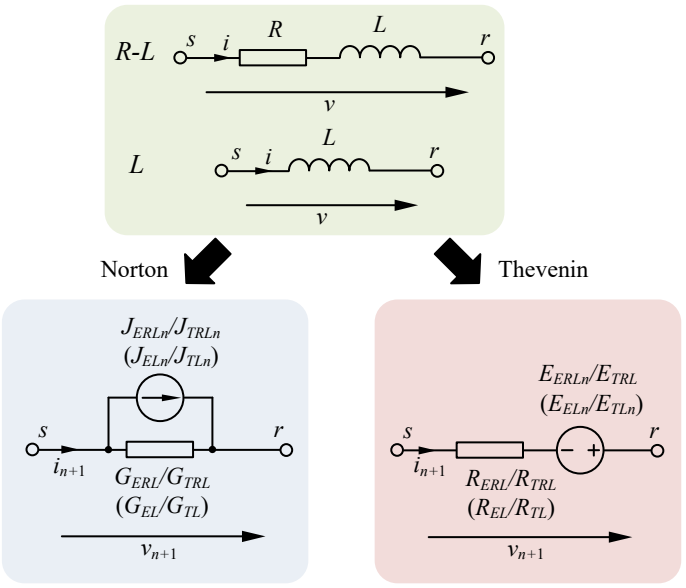


FIGURE 4.1: Discrete companion model of R-L series branch and inductance branch.

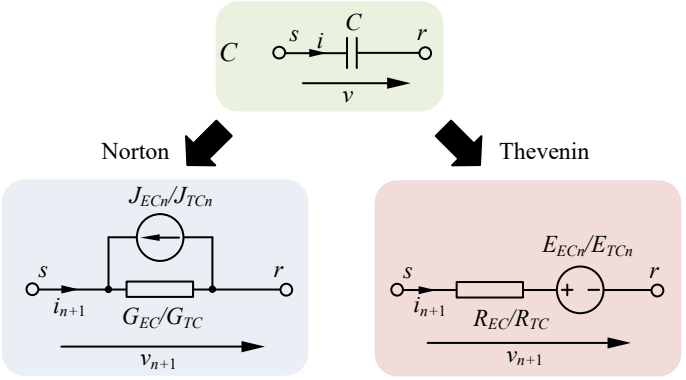


FIGURE 4.2: Discrete companion model of capacitance branch.

The differential equation of an R-L series branch is:

$$v(t) = Ri(t) + L\frac{di(t)}{dt}, \tag{4.4}$$

and

$$i'(t) = \frac{di(t)}{dt} = \frac{v(t) - Ri(t)}{L}. \tag{4.5}$$

Employing the implicit Euler method and assuming the step size is h, (4.5) is discretized into:

$$i_{n+1} = i_n + hi'_{n+1} = i_n + \frac{h}{L}(v_{n+1} - Ri_{n+1}), \tag{4.6}$$

then it can be simplified into:

$$i_{n+1} = \frac{h}{L+hR}v_{n+1} + \frac{L}{L+hR}i_n = G_{ERL}v_{n+1} + J_{ERLn}, \tag{4.7}$$

also,

$$v_{n+1} = \frac{L+hR}{h} i_{n+1} - \frac{L}{h} i_n = R_{ERL} i_{n+1} - E_{ERLn}, \tag{4.8}$$

where G_{ERL} and R_{ERL} is the equivalent conductance and resistance of R-L series branch under explicit Euler method, respectively, and J_{ERLn} and E_{ERLn} is the corresponding equivalent current source and voltage source, respectively. If only consider the inductance branch, eq. (4.7) and (4.8) can be rewitten by eliminating R:

$$i_{n+1} = \frac{h}{L} v_{n+1} + i_n = G_{EL} v_{n+1} + J_{ELn}, \quad \text{and} \tag{4.9}$$

$$v_{n+1} = \frac{L}{h} i_{n+1} - \frac{L}{h} i_n = R_{EL} i_{n+1} - E_{ELn}, \tag{4.10}$$

where G_{EL} and R_{EL} is the equivalent conductance and resistance of inductance branch under explicit Euler method, respectively, and J_{ELn} and E_{ELn} is the corresponding equivalent current source and voltage source, respectively. Employing the trapezoidal method with the same step size, (4.5) now can be discretized into:

$$i_{n+1} = i_n + \frac{h}{2}(i'_n + i'_{n+1}) = i_n + \frac{h}{2L}(v_n - R i_n + v_{n+1} - R i_{n+1}), \tag{4.11}$$

hence,

$$i_{n+1} = \frac{h}{2L+hR} v_{n+1} + (\frac{h}{2L+hR} v_n + \frac{2L-hR}{2L+hR} i_n) = G_{TRL} v_{n+1} + J_{TRLn}, \tag{4.12}$$

also,

$$v_{n+1} = \frac{2L+hR}{h} i_{n+1} - (v_n + \frac{2L-hR}{h} i_n) = R_{TRL} u_{n+1} - E_{TRLn}, \tag{4.13}$$

where G_{TRL} and R_{TRL} is the equivalent conductance and resistance of R-L series branch under trapezoidal method, respectively, and J_{TRLn} and E_{TRLn} is the corresponding equivalent current source and voltage source, respectively. Similarly, (4.12) and (4.13) can be simplified as (4.14) and (4.15) when only consider the inductance branch.

$$i_{n+1} = \frac{h}{2L} v_{n+1} + (\frac{h}{2L} v_n + i_n) = G_{TL} v_{n+1} + J_{TLn}, \quad \text{and} \tag{4.14}$$

$$v_{n+1} = \frac{2L}{h} i_{n+1} - (v_n + \frac{2L}{h} i_n) = R_{TL} v_{n+1} - E_{TLn}, \tag{4.15}$$

where G_{TL} and R_{TL} is the equivalent conductance and resistance of inductance branch under trapzoidal method, respectively, and J_{TLn} and E_{TLn} is the corresponding equivalent current source and voltage source, respectively.

The EMT simulation of HVDC systems is usually based on the piecewise linearization method handling nonlinear problem of components. Hence, it is paramount to study the

boundary point (breaking point) and the initial value at the boundary point. Eq. (4.9) and (4.10) of implicit Euler method show that the equivalent current source (J_{ELn}) and voltage source (E_{ELn}) are only determined by the current value (i_n), while the equivalent current source (J_{TLn}) (4.14) and voltage source (E_{TLn}) (4.15) in trapezoidal method include both the current value (i_n) and the voltage value (v_n). At the boundary point, only one value (i_n or v_n) can be guaranteed to be continuous, hence the trapezoidal method is not suitable for the first step calculation. Additionally, the equivalent conductance (G_{EL}) in implicit Euler method is twice the value of such conductance (G_{TL}) in trapezoidal method, since the explicit Euler method is based on first-order equation with the local truncation error of $O(h^2)$, while trapezoidal method is based on second-order equation with the local truncation error of $O(h^3)$. Therefore, a feasible scheme for EMT simulation at boundary point is to use implicit Euler method with reduced step size for the first step, then use trapezoidal method for the second step after boundary point.

This conclusion can also be confirmed in the discretized capacitance branch. The differential equation for the capacitance branch is:

$$v_c'(t) = \frac{dv_c(t)}{dt} = \frac{i_c(t)}{C}. \tag{4.16}$$

Similar as the derivation process for R-L series branch, (4.16) can be discretized into (4.17) and (4.18) by the implicit Euler method.

$$v_{n+1} = v_n + hv'_{n+1} = v_n + \frac{h}{C}i_{n+1} = R_{EC}i_{n+1} + E_{ECn}, \tag{4.17}$$

$$i_{n+1} = \frac{C}{h}v_{n+1} - \frac{C}{h}v_n = G_{EC}v_{n+1} - J_{ECn}, \tag{4.18}$$

where R_{EC} and G_{EC} is the equivalent resistance and conductance of capacitance branch under explicit Euler method, respectively, and E_{EC} and J_{EC} is the corresponding equivalent voltage source and current source, respectively. With trapezoidal method, (4.16) can be expressed as:

$$\begin{aligned} v_{n+1} = v_n + \frac{h}{2}(v'_n + v'_{n+1}) = v_n + \frac{h}{2C}(i_n + i_{n+1}) = \frac{h}{2C}i_{n+1} + (v_n + \frac{h}{2C}i_n) \\ = R_{TC}i_{n+1} + E_{TCn}, \end{aligned} \tag{4.19}$$

also,

$$i_{n+1} = \frac{2C}{h}v_{n+1} - (i_n + \frac{2C}{h}v_n) = G_{TC}v_{n+1} - J_{TCn}, \tag{4.20}$$

where R_{TC} and G_{TC} is the equivalent resistance and conductance of capacitance branch under trapezoidal method, respectively, and E_{TC} and J_{TC} is the corresponding equivalent voltage source and current source, respectively.

4.2.1.3 Parallel Computation Method

This section focuses on the parallel computation method of EMT fast simulation for avoiding cumbersome computations in HVDC systems. Since the network equations have to be re-established with every change of switching states, hence the parallel computation with switching analysis is of importance to improve computational efficiency. The parallel computation method aims to divide the whole system to different subdivisions which will be calculated independently and encapsulated in interfaces [154, 181].

Based on the analysis methods in EMT programs (Chapter 4.2.1.1), the parallel computation can use either nodal analysis method or state-space method for each subdivision. The basic process can be divided into three steps:

1) discretize the equations of subdivisions by nodal analysis method or state-space method obtaining equivalent branches,

2) replace the original subdivisions by the equivalent branches acquiring the whole equivalent network, and

3) compute the acquired equivalent network and obtain all parameters in the original network.

The aforementioned SSN method of Chapter 4.2.1.1 is based on the basic process, which uses the state-space method solving the equations of subdivisions and nodal analysis is adopted for interface computation.

Fig. 4.3 shows the parallel computation method in LCC and MMC-based HVDC systems. The whole system can be subdivided into different units mainly including AC networks, converters and DC lines. In addition, the MMC requires to establish discrete models for SM units. The HBSMs are the commonly used SMs for MMC, the next contents in this section introduces the discrete model of single HBSM and further derive the arm equivalent model based on the nodal analysis mentioned in Chapter 4.2.1.2 and the modeling method of full detailed equivalent model (Type 4) (Chapter 2.3).

Eq. (4.19) describes the discrete model of capacitance branch, which can be used in HBSM model discretization as:

$$\begin{aligned} v_c(t) &= v_c(t-h) + \frac{h}{2C}(i_c(t-h) + i_c(t)) \\ &= \frac{h}{2C} i_c(t) + (v_c(t-h) + \frac{h}{2C} i_c(t-h)) \\ &= R_c i_c(t) + E_{eq,c}(t-h), \end{aligned} \tag{4.21}$$

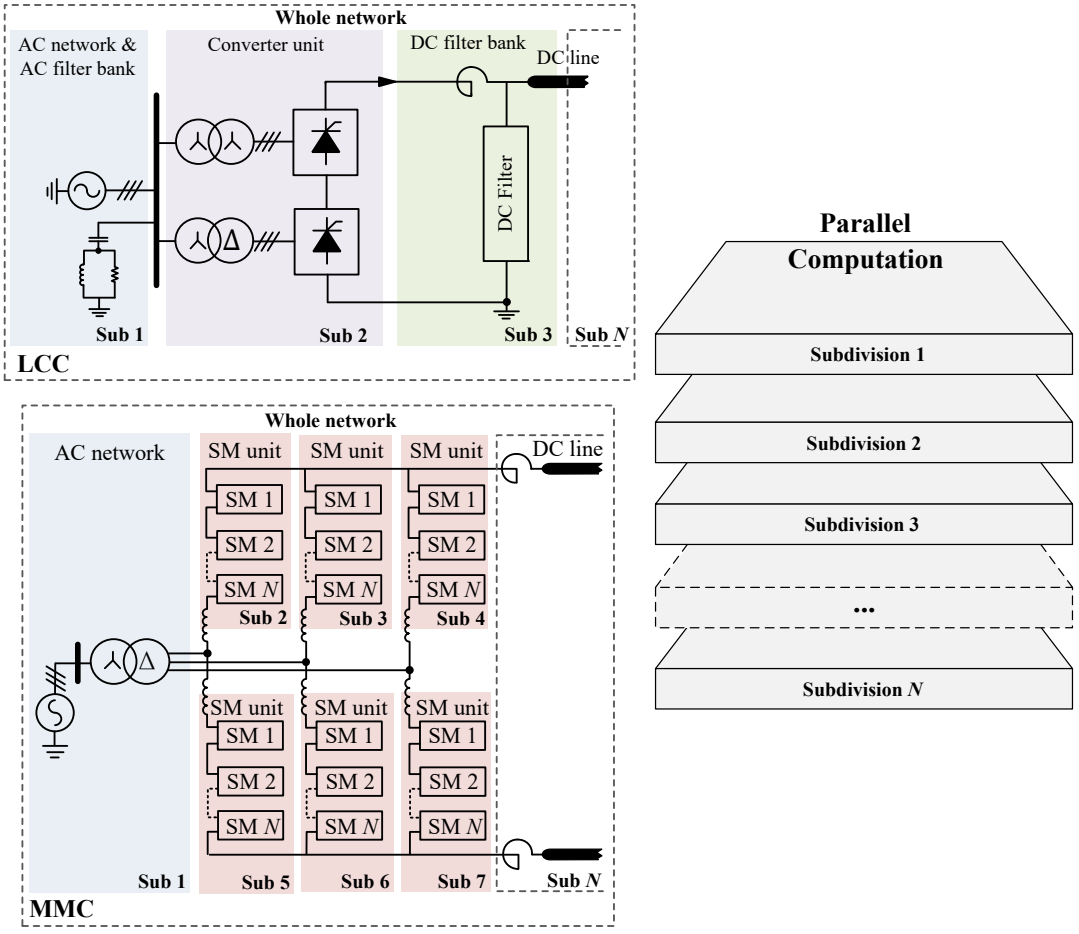


FIGURE 4.3: Parallel computation method of LCC and MMC.

where R_c is the equivalent resistance of HBSM capacitor, and $v_{ceq}(t-h)$ is the history equivalent voltage source of HBSM capacitor with the step size h. If use variable resistors (R_1, R_2) to replace the IGBTs with different switching states, the equivalent model of each HBSM can be established as Fig. 4.4, and the equation of such model follows:

$$\begin{aligned} v_{sm}(t) &= R_{eq,sm} i_{sm}(t) + E_{eq,sm}(t-h) \\ &= \frac{R_2(R_1+R_c)}{R_1+R_2+R_c} i_{sm}(t) + \frac{R_2}{R_1+R_2+R_c} E_{eq,c}(t-h). \end{aligned} \tag{4.22}$$

Hence, the arm instantaneous voltage can be expressed as:

$$\begin{aligned} v_{arm}(t) = \sum_{i=1}^{N} v_{sm}^{i}(t) &= (\sum_{i=1}^{N} R_{eq,sm}^{i}) i_{arm}(t) + \sum_{i=1}^{N} E_{eq,sm}^{i}(t-h) \\ &= R_{eq,arm} i_{arm}(t) + E_{eq,arm}(t-h). \end{aligned} \tag{4.23}$$

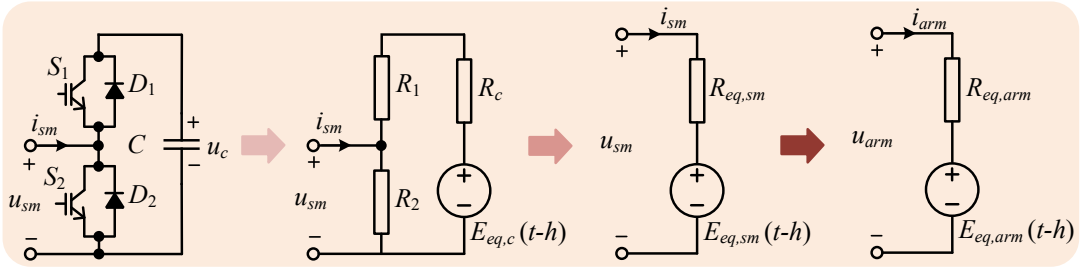


FIGURE 4.4: Discrete model of HBSMs and equivalent arm structure.

4.2.2 Electromechanical Transient Modeling

Since the extensive use of semiconductor devices with high switching frequency in HVDC systems, EMT simulation cannot be appplied to the study of large-scale HVDC systems, especially the interaction of AC and DC systems, although many equivalent models can be used to reduce the EMT simulation time [114, 154, 182–186]. However, electromechanical transient simulation ignores the harmonic influence and only considers the system operation and control characteristics under foundamental frequency. Hence, electromechanical transient simulation is more suitable for the study of large-scale HVDC systems. In addition, a balanced system is assumed at all times in the electromechanical transient simulation and the whole system can be described by the positive-sequence component under foundamental frequency, thus such modeling approach cannot reflect the system inner characteristics [155, 156, 187].

The electromechinal transient model is also called root mean square (RMS) model or phasor model as it ignores the system high frequency components. From the aspect of large-scale AC/DC grid, the purpose of electromechanical transient modeling for HVDC systems is intended to tackle two main issues:

i) the power flow calculation of DC and AC systems, and

ii) the mathematical description about steady-state and transient response characteristics of HVDC systems.

During the process of electromechanical transient modeling, the AC and DC systems are solved independently, where the AC systems are represented by phasor under foundamental frequency, the DC systems can be regarded as a variable source or load for AC systems and emulated by a branch with variable power (Fig. 4.5). Moreover, the DC systems can be solved if the AC bus voltages and converter control schemes are confirmed [156].

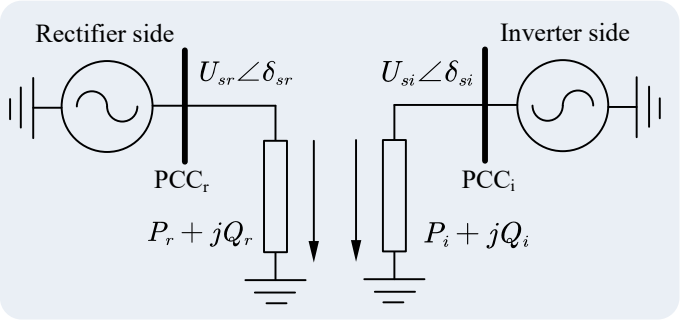


FIGURE 4.5: Equivalent function of DC systems in electromechanical modeling.

The general modeling approach for electromechanical transient characteristics of HVDC systems aims at formulating corresponding algebraic-differential equations. In addition, the unified modeling framework can be separated into three main steps:

1) converter modeling including the equivalent models in AC and DC sides,

2) controller modeling including the high- and low-level control, and

3) DC network modeling with different equivalent line models.

The initialization of electromechnical transient model is from the detailed system power flow calculation, which can be divided into sequential AC/DC power flow [188] and unified AC/DC power flow [189]; the unified method is easy to realize in simulators [156]. After detailed power flow calculations, the dynamic simulation can be proceeded with the assignment of initial values.

4.2.3 Other Modeling Approaches and Co-Simulation Studies

The EMT modeling approach can study the detailed switching characteristics due to its ultra-wide frequency-band capturing capability, while the foundamental frequency-based electromechanical transient modeling approach can be used in overall system stability analysis. In addition, some other modeling approaches that can capture dynamic frequency are developed for avoiding time-consuming calculation while retaining simulation accuracy. This section introduces two main techniques in the time-domain, DP model and SFP model, for capturing wide frequency-band interactions between different components in large-scale AC/DC grids. Besides, this section also discusses the potential of different modeling appraches for co-simulation study.

4.2.3.1 Dynamic Frequency Capturing Modeling

The DP modeling approach uses state-space equations to describe electrical variables (e.g. voltage or current) in one period T_s (sliding window), which are decomposed into harmonics of different frequencies based on Fourier transform, hence any high frequency components can be contained depending on the analysis requirements (Fig. 4.6). In addition, the corresponding Fourier series (also called DPs) are changed with the move of sliding window [157].

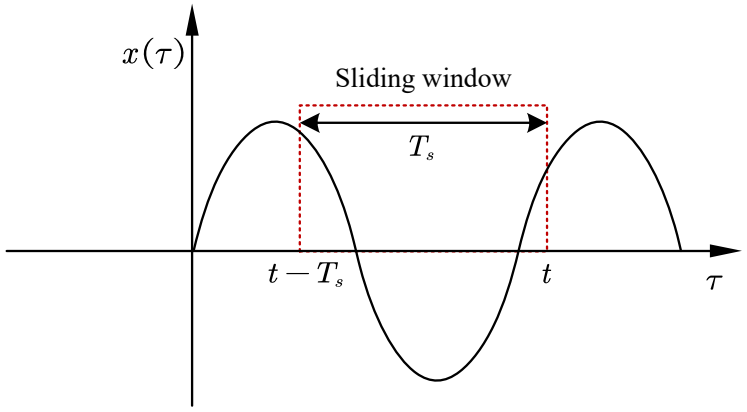


FIGURE 4.6: Time-varing Fourier transform in DP modeling approach.

A periodic variable $x(\tau), (\tau \in (t-T_s, T_s])$ with the period T_s can be expressed in the time-varying Fourier series by:

$$x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{j\omega_s \tau}, \tag{4.24}$$

where $\langle x \rangle_k(t)$ is the k^{th} Fourier series of $x(\tau)$, and $\omega_s = 2\pi/T_s$. The k^{th} Fourier series $\langle x \rangle_k(t)$ is determined by:

$$\langle x \rangle_k(t) = \frac{1}{T_s} \int_{t-\tau}^{t} x(\tau) e^{-j\omega_s \tau} d\tau. \tag{4.25}$$

The features of product and differential for $\langle x \rangle_k(t)$ are provided as:

$$\langle xy \rangle_k = \sum_i \langle x \rangle_{k-i} \langle y \rangle_i, \qquad \text{and} \tag{4.26}$$

$$\frac{d\langle x \rangle_k(t)}{dt} = \langle \frac{dx}{dt} \rangle_k(t) - j\omega_s \langle x \rangle_k(t). \tag{4.27}$$

Applying (4.27) to inductance and capacitance branch, the corresponding DP equations are:

$$L\frac{d\langle i_L \rangle_k(t)}{dt} = \langle v_L \rangle_k(t) - j\omega_s L \langle i_L \rangle_k(t), \qquad \text{and} \tag{4.28}$$

$$C\frac{d\langle v_c\rangle_k(t)}{dt} = \langle i_c\rangle_k(t) - j\omega_s C\langle u_c\rangle_k(t). \tag{4.29}$$

In general, the DP modeling approach can be used in the situation of analyzing specific frequency range. It is noted that the simulation accuracy will not be sacrificed within the selected frequencies.

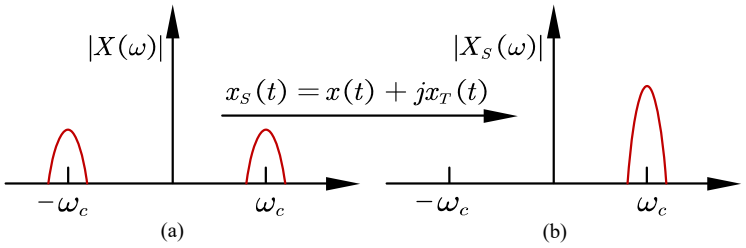


FIGURE 4.7: Spectra of original signal and complex signal: (a) original signal and (b) complex signal.

The nodal analysis-based SFP modeling approach uses the bandpass characteristics of electrical variables around the center frequency to construct a complex signal. A bandpass signal $x(t)$ with a bilateral spectrum is assumed to be with a center frequency ω_c (Fig. 4.7(a)). For obtaining the signal only with positive frequency (single-side spectrum), introduce a new complex signal $x_S(t)$ (Fig. 4.7(b)), and it can be expressed as:

$$x_S(t) = x(t) + jx_T(t), \tag{4.30}$$

where $x_T(t)$ is the transform of $x(t)$ by specific methods, as Hilbert transform $x_T(t) = x_H(t) = \int_{-\infty}^{\infty}\frac{x(\tau)}{\pi(t-\tau)}d\tau$ [161], differential transform $x_T(t) = x_D(t) = -\frac{x'(t)}{\omega_c}$ [163] and integral transform $x_T(t) = x_I(t) = \int_{-\infty}^{t} x(\tau)d\tau$ [190]. In addition, the spectra of complex signals ($x_{SH}(t) = x(t) + jx_H(t), x_{SD}(t) = x(t) + jx_D(t), x_{SI}(t) = x(t) + jx_I(t)$) under different transforms can be obtained via Fourier transform, which are $X_{SH}(\omega) = (1+\mathrm{sgn}(\omega))X(\omega)$, $X_{SD}(\omega) = (1+\frac{\omega}{\omega_c})X(\omega)$ and $X_{SI}(\omega) = (1+\frac{\omega_c}{\omega})X(\omega)$, respectively. It is noted that Hilter transform has no negative frequency components compared with other two methods (Fig. 4.8).

To reconstruct (4.30) by frequency shift of ω_s, (4.31) can be deduced. If the shift frequency is set to zero ($\omega_s = 0$), the SFP model will be equal to conventional EMT model, while the complex signal will convert to complex envelope signal if the shift frequency is set to the center frequency ($\omega_s = -\omega_c$ where the minus refers to left shift) as (4.32).

$$x_{SS}(t) = x_S(t)e^{j\omega_s t}, \tag{4.31}$$

$$x_E(t) = x_S(t)e^{-j\omega_c t}. \tag{4.32}$$

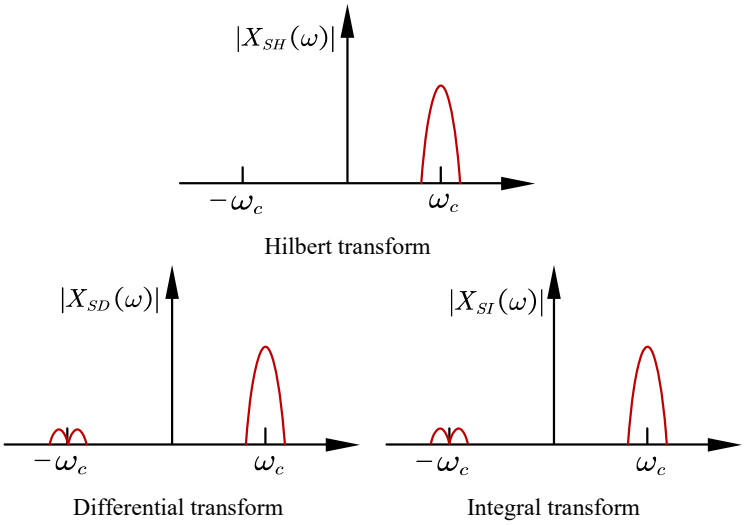


FIGURE 4.8: Spectra of complex signal under different transforms.

Fig. 4.9 shows the maximum frequency of complex envolope signal is far less than the original signal. Therefore, based on Shannon sampling theorem, SPF modeling approach can provide larger time step without sacrificing simulation accuracy [161].

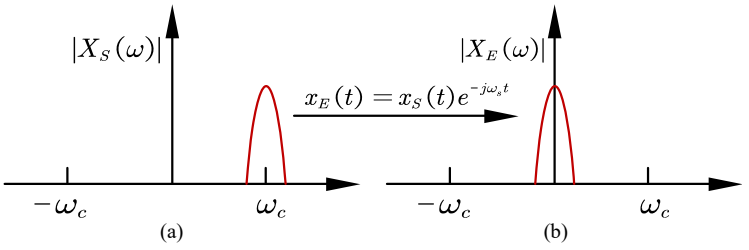


FIGURE 4.9: Spectra of complex signal and complex envolope signal: (a) complex signal and (b) complex envolope signal.

Based on the description of numerical integration in Chapter 4.2.1.2, the discrete companion model of system components can be established. Assuming $\frac{dx_S(t)}{dt} = f_S(t)$, hence the differential equation of complex envolope signal is:

$$\frac{dx_E(t)}{dt} = f_E(t) - j\omega_s x_E(t), \tag{4.33}$$

where $f_E(t) = f_S(t)e^{-j\omega_s t}$. Employing traprzoidal integration method to discretize (4.33):

$$x_E(t) = x_E(t-h) + \frac{h}{2}((f_E(t) - j\omega_s x_E(t)) + (f_E(t-h) - j\omega_s x_E(t-h))), \tag{4.34}$$

Moreover, combining (4.31) and (4.34), the discrete equation of complex signal can be further acquired as:

$$x_S(t) = x_S(t-h)e^{j\omega_s h} + \frac{h}{2}((f_S(t) - j\omega_s x_S(t)) + (f_S(t-h)e^{j\omega_s h} - j\omega_s x_S(t-h)e^{j\omega_s h})). \quad (4.35)$$

4.2.3.2 Co-simulation Studies

The purpose of co-simulation studies in HVDC systems is to achieve a balance between the modeling scale and accuracy. Based on the aforementioned different modeling approaches, a typical co-simulation study is that AC systems are modeled by EMT modeling approach and electromechanical transient method is used for converter modeling [167, 168]. By interfacing the two basic modeling approaches, the computation speed can be increased with acceptable simulation accuracy [168]. Additionally, the EMT modeling method has been used to combine DP or (and) SFP approaches for specific study requirements in current literature [169–171].

4.3 Detailed Description of Droop Control

In LCC-based MTDC systems, the DC voltage is usually controlled by one converter for improving the system operation stability, thus the balance of DC current and power has to be coordinated by the upper layer control [191]. Unlike LCC-based MTDC systems, there are three basic control schemes in system level for VSC-based MTDC systems and DC grids [192–194]:

i) master/slave control,

ii) DC voltage margin control, and

iii) droop control.

In the first two schemes, one converter has to act as a slack bus controlling the DC voltage of the whole system, and other converters adopt constant AC active power (DC power) or DC current control [195]. The DC voltage margin control requires no communication compared to the master-slave control in a fixed operation range, while it requires relatively complex controller design, especially the two stage DC voltage control method [193]. By comparison, the droop control is easy to implement since all converters in an MTDC system coordinate to balance the DC voltage by given droop constants, hence operate independent of communication [195]. Power/voltage (P/V) droop control is a conventional droop

control scheme, which can be extended to DC current/voltage (I/V) droop control and mixed droop control combining them for different converters. This section discusses the single P/V, I/V droop and mixed droop control for HVDC systems.

4.3.1 Basic Theory

The conventional P/V droop control for MTDC systems or DC grids is originated from the power/frequency (P/f) droop control in AC systems [194]. For P/V droop control, the control of DC voltage is shared by different converters with droop control, and the droop control can be considered as an extension of constant power or DC voltage control, which can improve the system reliability and reduce the telecommunication dependence among all converters as well. The function of I/V droop control is similar as P/V droop control that the DC current is controlled rather than power. In addtion, it is also possible to arrange P/V and I/V droop control in different converters constituting mixed droop control.

4.3.2 Static Characteristic

The static characteristic and controller structure of droop control are shown in Fig. 4.10 where a three terminal HVDC system is adopted as an example. Converter 1 in rectifier side delivers power to converter 2 and 3 in inverter side, and DC voltage is balanced by the three converters via corresponding droop characteristic. Matrix $\boldsymbol{K_{droop}}$ represents the droop constants of all converters in an HVDC system, and the ratio of characteristic curve is defined as $\boldsymbol{R} = -(\boldsymbol{K_{droop}})^{-1}$. It is noted that the power limitation is a concern for each converter, since the converter will lose DC voltage balance capability if it reaches the maximum power rating after system power disturbance. When an HVDC system with droop control is in steady-state operation, eq. (4.36) and (4.37) can be established for P/V droop control and I/V droop control, respectively.

$$\begin{cases} (\boldsymbol{P_{dc}^*} - \boldsymbol{P_{dc}}) + \mathrm{diag}(\boldsymbol{K_{droop_P}})(\boldsymbol{V_{dc}^*} - \boldsymbol{V_{dc}}) = \boldsymbol{0}, \\ (\boldsymbol{P_{dc0}^*} - \boldsymbol{P_{dc0}}) + \mathrm{diag}(\boldsymbol{K_{droop_P}})(\boldsymbol{V_{dc0}^*} - \boldsymbol{V_{dc0}}) = \boldsymbol{0}, \end{cases} \tag{4.36}$$

$$\begin{cases} (\boldsymbol{I_{dc}^*} - \boldsymbol{I_{dc}}) + \mathrm{diag}(\boldsymbol{K_{droop_I}})(\boldsymbol{V_{dc}^*} - \boldsymbol{V_{dc}}) = \boldsymbol{0}, \\ (\boldsymbol{I_{dc0}^*} - \boldsymbol{I_{dc0}}) + \mathrm{diag}(\boldsymbol{K_{droop_I}})(\boldsymbol{V_{dc0}^*} - \boldsymbol{V_{dc0}}) = \boldsymbol{0}, \end{cases} \tag{4.37}$$

where the superscript * and subscript $_0$ refer to corresponding reference values and initial values, respectively. In addition, the droop constants for P/V and I/V droop control in this thesis are defined as (4.38) and (4.39), respectively .

$$K_{droop_P} = \frac{P_{dc_{rated}}}{V_{dc_{rated}} \delta_{droop}} \ (\mathrm{MW/kV}), \tag{4.38}$$

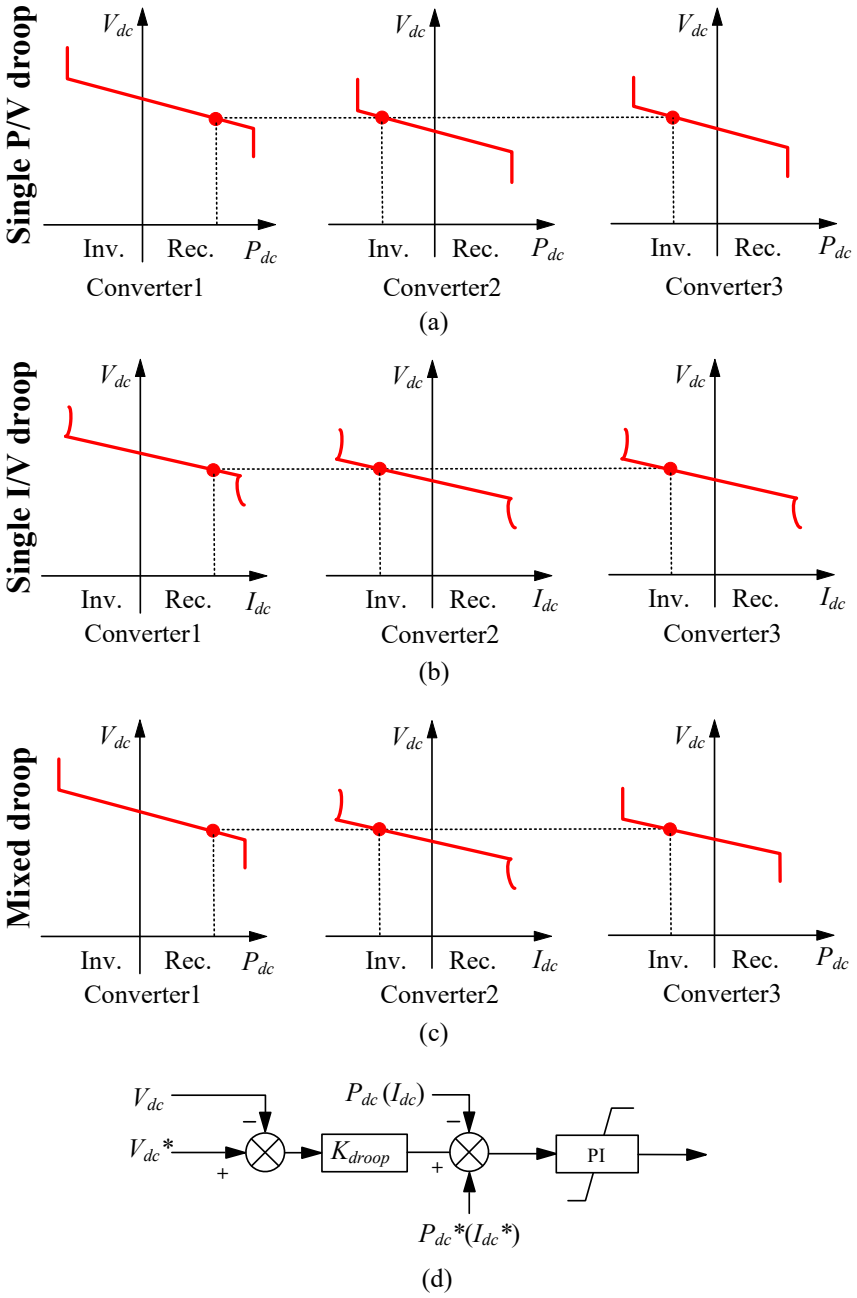


FIGURE 4.10: Static characteristic of droop control in HVDC systems: (a) single P/V droop control, (b) single I/V droop control, (c) mixed P/V and I/V droop control, and (d) structure of droop controller.

$$K_{droop_I} = \frac{P_{dc_{rated}}}{V_{dc_{rated}}^2 \delta_{droop}} \text{ (A/kV)}, \tag{4.39}$$

where $P_{dc_{rated}}$ and $V_{dc_{rated}}$ is the rated DC power and rated DC voltage of each converter, respectively, and δ_{droop} in this thesis refers to the DC voltage deviation ratio. It is noted that the converter will run in constant DC power (DC current) control or DC voltage control if

$K_{droop} = 0$ or $K_{droop} = \infty$, respectively.

4.4 Generalized Expression of DC Power Flow

Power flow analysis is important for HVDC systems as it is used for static security assessment. Different from HVAC systems, the DC power flow analysis has to be conducted in HVDC systems [188, 189], which should consider the effect of single P/V or I/V droop control. The initial DC power flow can be obtained by different power flow calculation methods as Newton Raphson [196]. Moreover, the DC power flow under reference change can be determined by the droop characteristic of different converters [192, 195]. However, the detailed DC power flow analysis under mixed P/V and I/V droop control is not reported in current literature.

Based on the description of droop control in Chapter 4.3, this section first introduces the basic single droop control-based DC power flow calculation. Furthermore, it is expanded to a generalized calculation method obtaining the initial DC power flow for normal operation and the DC power flow after converter outage under mixed P/V and I/V droop control. The power limitation of all remaining converters after a converter outage is also considered for avoiding long-term overload operation. The accuracy of proposed generalized expression of DC power flow is verified in an MMC-based four terminal DC grid.

4.4.1 Initial DC Power Flow for Normal Operation

4.4.1.1 Single P/V or I/V Droop Control

An MTDC system or a DC grid of n buses under P/V droop control is assumed to be with one known DC voltage reference, and $n-1$ known DC power references. The initial power flow can be solved by Newton-Raphson method as (4.40), obtaining one unknown DC power and $n-1$ DC voltages (n unknowns) [192]. In addition, the DC currents of all terminals and branches can also be derived.

$$\boldsymbol{P_{dc0_P}} = \boldsymbol{V_{dc0_P}} \odot (\boldsymbol{Y_{dc}} \boldsymbol{V_{dc0_P}}), \tag{4.40}$$

where $\boldsymbol{P_{dc0_P}}$ and $\boldsymbol{V_{dc0_P}}$ refer to the column vectors of terminal DC powers and DC voltages under P/V droop control, respectively, $\boldsymbol{Y_{dc}}$ is the nodal admittance matrix and $\odot$ refers to the Hadamard product.

Similarly, if an MTDC system or a DC grid of n buses under I/V droop control is assumed to be with one known DC voltage reference, and $n-1$ known DC current references, the initial power flow for single I/V droop control can be obtained by:

$$\begin{cases} \boldsymbol{I_{dc0_I}} = \boldsymbol{Y_{dc}} \boldsymbol{V_{dc0_I}}, \\ \boldsymbol{P_{dc0_I}} = \boldsymbol{V_{dc,ini_I}} \odot \boldsymbol{I_{dc0_I}}, \end{cases} \tag{4.41}$$

where $\boldsymbol{I_{dc0_I}}$, $\boldsymbol{P_{dc0_I}}$ and $\boldsymbol{V_{dc0_I}}$ refer to the column vectors of terminal DC currents, DC powers and DC voltages under I/V droop control, respectively.

The basic initial DC power flow calculation for single droop control aims to establish the relationship between powers or currents and voltages via nodal admittance matrix, creating a one-to-one correspondence.

4.4.1.2 Mixed P/V and I/V Droop Control

In the scenario of mixed P/V and I/V droop control, there are one known DC voltage reference, a known DC power references, and b known DC current references. Therefore, it is necessary to build the relationship amongst currents, voltages and powers, creating a one-to-many (two) correspondence and line currents can be as a bridge connecting the three.

First, b DC current references (a DC power references) are assumed to be b DC power references (a DC current references), then the current directions in each transmission line can be determined by the single P/V or I/V droop calculation method described in Chapter 4.4.1.1. Based on the known line current directions, the final initial power flow can be derived from (4.42), obtanining $n-a$ DC powers, $n-1$ DC voltages, $n-b$ DC terminal currents and k DC line currents ($2n+k$ unknowns).

$$\begin{cases} \boldsymbol{P_{dc0_M}} = \boldsymbol{V_{dc0_M}} \odot \boldsymbol{I_{dc0_M}} \\ \mathrm{diag}(\boldsymbol{G_l}) \boldsymbol{V_{l0_M}} = \boldsymbol{I_{l0_M}} \\ \boldsymbol{I_{dc0_M}} = \boldsymbol{\Lambda} \boldsymbol{I_{l0_M}} \end{cases}, \tag{4.42}$$

where $\boldsymbol{P_{dc0_M}}$ and $\boldsymbol{V_{dc0_M}}$ refer to the column vectors of terminal DC powers and DC voltages under mixed droop control, respectively, $\boldsymbol{G_l}$ is a single column matrix composed by k line conductances, $\boldsymbol{V_{l0_M}}$ and $\boldsymbol{I_{l0_M}}$ refer to the corresponding line voltage drop and line current expressed in single column matrix, respectively, and $\boldsymbol{\Lambda}$ is the coefficient ($n \times k$ matrix) connecting DC currents between terminals and branches and the value depends on the actual system.

Fig. 4.11 shows the flowchart of initial power flow calculation for single and mixed droop control. The results of initial DC power flow in Chapter 4.4.1.1 and 4.4.1.2 are used as references of each terminal for single and mixed droop control.

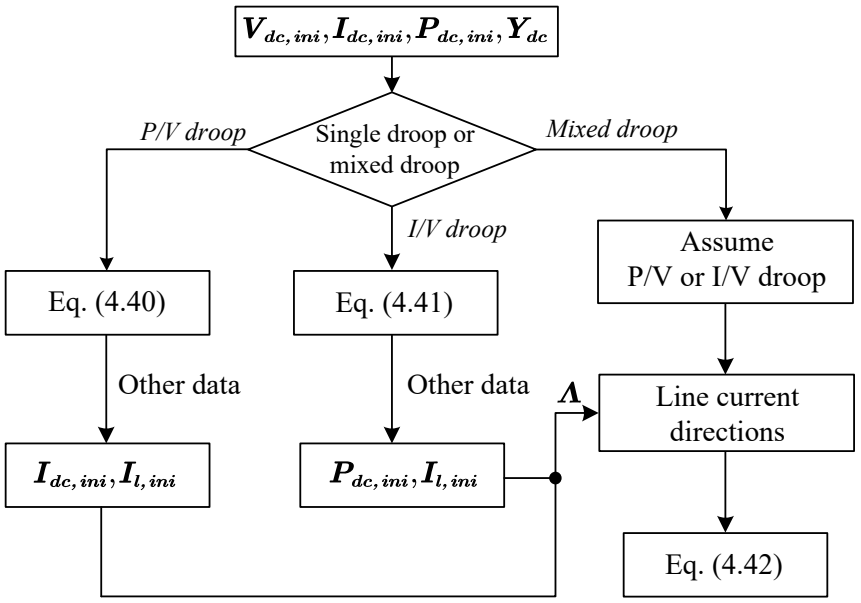


FIGURE 4.11: Flowchart of initial DC power flow calculation.

4.4.2 DC Power Flow after Converter Outage

The impact of converter outage to a MTDC system or DC grid can be considered as a system power disturbance, and it is necessary to re-construct the network equations for obtaining redistributed DC power flow. For single P/V droop control, the deviation of DC power and DC voltage after system disturbance in each terminal can be expressed as:

$$\begin{cases} \boldsymbol{\Delta P_{dc}^{*}} = \boldsymbol{P_{dc}^{*}} - \boldsymbol{P_{dc0}^{*}}, \\ \boldsymbol{\Delta P_{dc}} = \boldsymbol{P_{dc}} - \boldsymbol{P_{dc0}}, \\ \boldsymbol{\Delta V_{dc}^{*}} = \boldsymbol{V_{dc}^{*}} - \boldsymbol{V_{dc0}^{*}}, \\ \boldsymbol{\Delta V_{dc}} = \boldsymbol{V_{dc}} - \boldsymbol{V_{dc0}}. \end{cases} \tag{4.43}$$

Similarly, the deviation of DC current and DC voltage after system disturbance in each terminal for I/V droop control are:

$$\begin{cases} \boldsymbol{\Delta I_{dc}^{*}} = \boldsymbol{I_{dc}^{*}} - \boldsymbol{I_{dc0}^{*}}, \\ \boldsymbol{\Delta I_{dc}} = \boldsymbol{I_{dc}} - \boldsymbol{I_{dc0}}, \\ \boldsymbol{\Delta V_{dc}^{*}} = \boldsymbol{V_{dc}^{*}} - \boldsymbol{V_{dc0}^{*}}, \\ \boldsymbol{\Delta V_{dc}} = \boldsymbol{V_{dc}} - \boldsymbol{V_{dc0}}. \end{cases} \tag{4.44}$$

Combining (4.36) and (4.43), (4.45) can be obtained for single P/V droop control. For single I/V droop control, eq. (4.46) can also be yielded combining (4.37) and (4.44).

$$\boldsymbol{\Delta P_{dc}} - \boldsymbol{\Delta P_{dc}^{*}} = \mathrm{diag}(\boldsymbol{K_{droop_P}})(\boldsymbol{\Delta V_{dc}^{*}} - \boldsymbol{\Delta V_{dc}}), \tag{4.45}$$

$$\boldsymbol{\Delta I_{dc}} - \boldsymbol{\Delta I_{dc}^{*}} = \mathrm{diag}(\boldsymbol{K_{droop_I}})(\boldsymbol{\Delta V_{dc}^{*}} - \boldsymbol{\Delta V_{dc}}). \tag{4.46}$$

Additionally, the relationship between $\boldsymbol{\Delta P_{dc}}$ and $\boldsymbol{\Delta V_{dc}}$ for single P/V droop control can be approximately established as:

$$\boldsymbol{\Delta P_{dc}} \approx \boldsymbol{J_{dc}}\boldsymbol{\Delta V_{dc}}, \tag{4.47}$$

where $\boldsymbol{J_{dc}}$ is DC jacobian matrix of certain MTDC system or DC grid. The relationship between $\boldsymbol{\Delta I_{dc}}$ and $\boldsymbol{\Delta V_{dc}}$ for single I/V droop control is:

$$\boldsymbol{\Delta I_{dc}} = \boldsymbol{Y_{dc}}\boldsymbol{\Delta V_{dc}}. \tag{4.48}$$

The following contents analyze the detailed DC power flow variation after converter outage with single P/V or I/V droop control and mixed P/V and I/V droop control.

4.4.2.1 Single P/V or I/V Droop Control

For determining the re-distributed DC power flow after converter outage with single P/V or I/V droop control, eq. (4.49) and (4.50) are established to obtain the DC power and DC voltage deviation by combining (4.45), (4.47) and (4.46), (4.48), respectively.

$$\begin{cases} \boldsymbol{\Delta P_{dc}} = \dfrac{\boldsymbol{\Delta P_{dc}^{*}} + \mathrm{diag}(\boldsymbol{K_{droop_P}})\boldsymbol{\Delta V_{dc}^{*}}}{\boldsymbol{I} + \mathrm{diag}(\boldsymbol{K_{droop_P}})\boldsymbol{J_{dc}}^{-1}}, \\ \boldsymbol{\Delta V_{dc}} = \dfrac{\boldsymbol{\Delta P_{dc}^{*}} + \mathrm{diag}(\boldsymbol{K_{droop_P}})\boldsymbol{\Delta V_{dc}^{*}}}{\mathrm{diag}(\boldsymbol{K_{droop_P}}) + \boldsymbol{J_{dc}}}, \end{cases} \tag{4.49}$$

$$\begin{cases} \boldsymbol{\Delta I_{dc}} = \dfrac{\boldsymbol{\Delta I_{dc}^{*}} + \mathrm{diag}(\boldsymbol{K_{droop_I}})\boldsymbol{\Delta V_{dc}^{*}}}{\boldsymbol{I} + \mathrm{diag}(\boldsymbol{K_{droop_I}})\boldsymbol{Y_{dc}}^{-1}}, \\ \boldsymbol{\Delta V_{dc}} = \dfrac{\boldsymbol{\Delta I_{dc}^{*}} + \mathrm{diag}(\boldsymbol{K_{droop_I}})\boldsymbol{\Delta V_{dc}^{*}}}{\mathrm{diag}(\boldsymbol{K_{droop_I}}) + \boldsymbol{Y_{dc}}}, \end{cases} \tag{4.50}$$

where $\boldsymbol{I}$ is the $n \times n$ identity matrix. Supposing no deviation of DC voltage references ($\boldsymbol{\Delta V_{dc}^{*}} = \boldsymbol{0}$), eq. (4.49) and (4.50) can be simplified as:

$$\begin{cases} \boldsymbol{\Delta P_{dc}} = \dfrac{\boldsymbol{\Delta P_{dc}^{*}}}{\boldsymbol{I} + \mathrm{diag}(\boldsymbol{K_{droop_P}})\boldsymbol{J_{dc}}^{-1}} = \boldsymbol{A_P}\boldsymbol{\Delta P_{dc}^{*}}, \\ \boldsymbol{\Delta V_{dc}} = \dfrac{\boldsymbol{\Delta P_{dc}^{*}}}{\mathrm{diag}(\boldsymbol{K_{droop_P}}) + \boldsymbol{J_{dc}}} = \boldsymbol{B_P}\boldsymbol{\Delta P_{dc}^{*}}, \end{cases} \tag{4.51}$$

and

$$\begin{cases} \boldsymbol{\Delta I_{dc}} = \dfrac{\boldsymbol{\Delta I_{dc}^*}}{\boldsymbol{I} + \mathrm{diag}(\boldsymbol{K_{droop_I}})\boldsymbol{Y_{dc}}^{-1}} = \boldsymbol{A_I}\boldsymbol{\Delta I_{dc}^*}, \\ \boldsymbol{\Delta V_{dc}} = \dfrac{\boldsymbol{\Delta I_{dc}^*}}{\mathrm{diag}(\boldsymbol{K_{droop_I}}) + \boldsymbol{Y_{dc}}} = \boldsymbol{B_I}\boldsymbol{\Delta I_{dc}^*}, \end{cases} \tag{4.52}$$

respectively, where $\boldsymbol{A_P}$, $\boldsymbol{B_P}$, $\boldsymbol{A_I}$ and $\boldsymbol{B_I}$ refer to the corresponding coefficient matrix. The outage of certain converter in an MTDC system or DC grid, reflecting in (4.51) and (4.52), can be summarized as:

$$\begin{cases} \Delta P_{dc,out}^* = -P_{dc0,out}, \\ K_{droop,out_P} = 0, \end{cases} \tag{4.53}$$

and

$$\begin{cases} \Delta I_{dc,out}^* = -I_{dc0,out}, \\ K_{droop,out_I} = 0, \end{cases} \tag{4.54}$$

respectively, then the final DC power flow for single droop control can be obtained.

However, the above description does not consider the power limitation of converters after converter outage. If one converter with P/V droop control is overloaded after preliminary calculation (4.55), the converter should be in constant DC power control in actual operation, and the actual DC power variation of such converter can be calclulated as (4.56).

$$P_{dc0,over} + \Delta P_{dc,pre} > P_{dc,max}, \tag{4.55}$$

$$\Delta P_{dc,act_P} = P_{dc,max} - P_{dc0,over}. \tag{4.56}$$

Setting the droop constant of the oveloaded converter as zero (4.57), then the final DC power flow for single P/V droop control can be accurately derived by substituting (4.53), (4.56) and (4.57) into (4.51).

$$K_{droop,over} = 0 \tag{4.57}$$

For single I/V droop control, if a certain converter is overloaded after converter outage (4.58), such converter in the text is designed to switch into constant DC power control ($K_{droop,over} = 0$) for avoiding long-term overload operation.

$$(V_{dc0,over} + \Delta V_{dc,pre})(I_{dc0,over} + \Delta I_{dc,pre}) > P_{dc,max}, \tag{4.58}$$

Correspondingly, the single I/V droop control transforms into mixed P/V and I/V droop control, and the remaining maximum power capacity of an overloaded converter is:

$$\Delta P_{dc,act_I} = P_{dc,max} - V_{dc0,over} I_{dc0,over}. \tag{4.59}$$

It is worth mentioning that the further derived line current directions under single droop control can be used in mixed droop control for building the relationship amongst the

DC powers, currents and voltages in the remaining converters. The following section introduces the power flow calculation method for mixed P/V and I/V droop control.

4.4.2.2 Mixed P/V and I/V Droop Control

The current directions of branches in an MTDC system or a DC grid may change after converter outage. Thus, the line current directions should be first obtained based on single droop control assumption as described in the previous section. Then (4.60) can be established yielding $\boldsymbol{\Delta P_{dc}}, \boldsymbol{\Delta V_{dc}}, \boldsymbol{\Delta I_{dc}}$ in each station and $\boldsymbol{\Delta I_l}$ in transmission lines. There are in total $3(n-m)+k'$ unknowns if m converters are isolated, and k' is the remaining number of branches.

$$\begin{cases} \boldsymbol{P_{dc0_M}} + \boldsymbol{\Delta P_{dc}} = (\boldsymbol{V_{dc0_M}} + \boldsymbol{\Delta V_{dc}}) \odot (\boldsymbol{I_{dc0_M}} + \boldsymbol{\Delta I_{dc}}) \\ \mathrm{diag}(\boldsymbol{G_l})(\boldsymbol{V_{l0_M}} + \boldsymbol{\Delta V_l}) = \boldsymbol{I_{l0_M}} + \boldsymbol{\Delta I_l}, \\ (\boldsymbol{I_{dc0_M}} + \boldsymbol{\Delta I_{dc}}) = \boldsymbol{\Lambda'}(\boldsymbol{I_{l0_M}} + \boldsymbol{\Delta I_l}), \end{cases} \tag{4.60}$$

where $\boldsymbol{\Lambda'}$ is a $(n-m)\times k'$ coefficient matrix here, and $\boldsymbol{G_l}$ is a single column matrix of k' elements. In addition, the references are not changed for the remaining $n-m$ converters, hence eq. (4.45) and (4.46) can be reduced to (4.61) and (4.62), respectively.

$$\boldsymbol{\Delta P_{dc}} = -\mathrm{diag}(\boldsymbol{K_{droop_P}})\boldsymbol{\Delta V_{dc}} \tag{4.61}$$

$$\boldsymbol{\Delta I_{dc}} = -\mathrm{diag}(\boldsymbol{K_{droop_I}})\boldsymbol{\Delta V_{dc}} \tag{4.62}$$

If no converter is overloaded, the final DC power flow can be derived by combining (4.61), (4.62) and (4.60).

When one converter with P/V droop control exceeds the maximum power limitation (4.55), (4.56) has to be used to substitute corresponding ΔP_{dc} in (4.61), and droop constant of such converter should be set as zero ($K_{droop,over} = 0$) as well. In addition, if one converter with I/V droop control is overloaded, such converter should switch into constant DC power control, hence (4.61) and (4.62) will be updated. The final accurate DC power flow can be obtained by substituting updated (4.61) and (4.62) into (4.60).

The flowchart of power flow calculation after converter outage for single and mixed droop control is shown in Fig. 4.12. In general, the power flow calculation method for mixed droop control aims to construct the detailed network equations based on actual steady-state operation after converter outage. Since (4.60) in mixed droop control can also be expressed as (4.47) by ignoring the nonlinear terms in single P/V droop control, or (4.48) in single I/V droop control, the calculation methods are equivalent for single and mixed droop control.

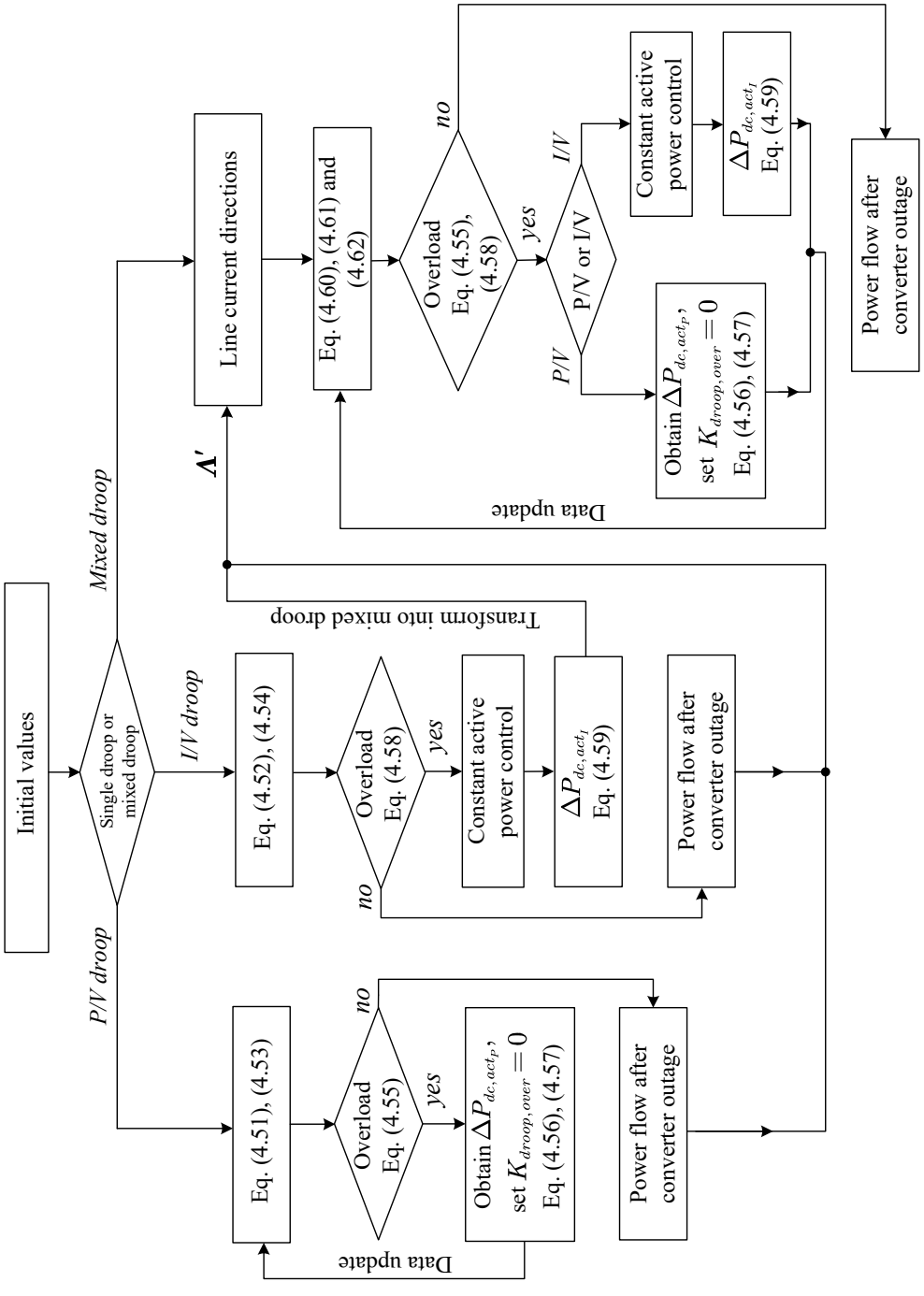


FIGURE 4.12: Flowchart of DC power flow under converter outage.

4.4.3 Case Study

A detailed equivalent model of MMC-based four-terminal DC grid (Fig. 4.13) is estalished in PLECS-Blockset and Simulink for verifying the accuracy of described generalized expression of DC power flow. The parameters of the four MMCs are listed in Table 4.1, and Table 4.2 provides the parameters of DC transmission lines. In addition, MMC1 is located at rectifier side delivering power to other MMCs (MMC2, MMC3 and MMC4).

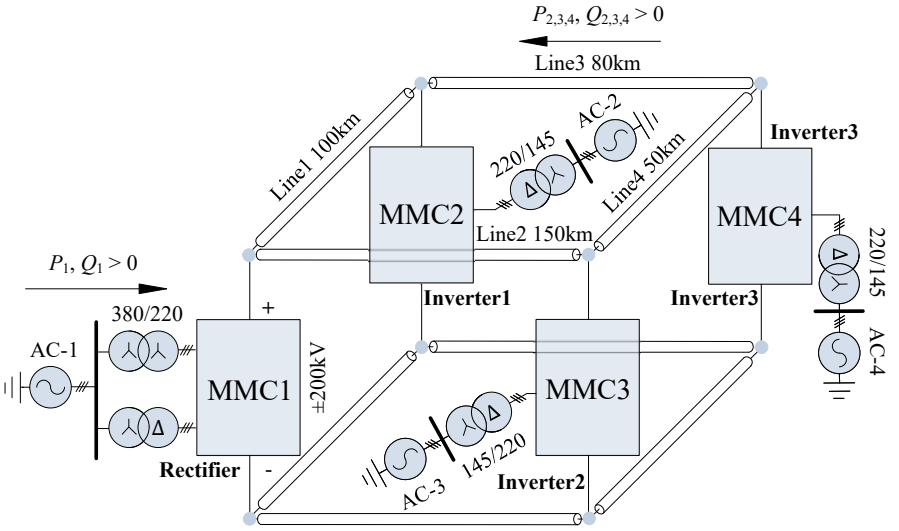


FIGURE 4.13: MMC-based four terminal DC grid.

TABLE 4.1: Parameters of four MMCs in the DC grid.

Parameter	MMC1	MMC2	MMC3	MMC4
Rated Power (MVA)	800	400	150	250
DC Voltage (kV)	±200	±200	±200	±200
AC Voltage (L-L rms) (kV)	380	145	145	145
Transformer Ratio	380/220	145/220	145/220	145/220
Number of SMs per Arm	400	400	400	400
Nominal Operating Point (m_a)	0.9	0.9	0.9	0.9

TABLE 4.2: Parameters of DC transmission lines in the MMC-based DC grid.

Parameters	Line 1	Line 2	Line 3	Line 4
Type	Cable	Cable	Cable	Cable
Distance (km)	100	150	80	50
Resistance (Ω/km)	0.011	0.011	0.011	0.011
Capacitance (μF/km)	0.2185	0.2185	0.2185	0.2185
Inductance (mH/km)	0.2615	0.2615	0.2615	0.2615

4.4.3.1 Verification in MMC-based DC Grid under Single P/V Droop Control

In this case, a single P/V droop control is adopted in the MMC-based DC grid (Fig. 4.14(a)). Table 4.3 lists the initial references and droop constants of four MMCs for deriving the initial power flow. Based on eq. (4.40), DC power of MMC1 and DC voltages of MMC2, MMC3 and MMC4 can be obtained. Besides, DC currents of all terminals and branches can be further derived (Table 4.4).

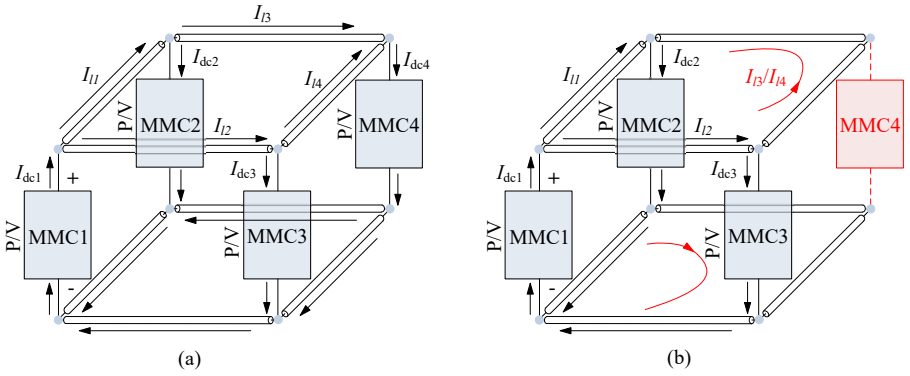


FIGURE 4.14: Detailed current directions of MMC-based DC grid under single P/V droop control in the MMC-based DC grid: (a) initial power flow, and (b) power flow after MMC4 outage.

TABLE 4.3: References of outer control loop for single P/V droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P^*_{dc} (MW)	-	-380	-100	-120
I^*_{dc} (kA)	-	-	-	-
V^*_{dc} (kV)	400	-	-	-
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40 MW/kV	20 MW/kV	7.5 MW/kV	12.5 MW/kV

TABLE 4.4: Calculation of initial DC power flow for single P/V droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P_{dc} (MW)	603.1145	-380.0000	-100.0000	-120.0000
I_{dc} (kA)	1.5078	-0.9551	-0.2511	-0.3016
V_{dc} (kV)	400.0000	397.8845	398.1976	397.8730
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40	20	7.5	12.5
Line currents	I_{l1}	I_{l2}	I_{l3}	I_{l4}
(kA)	0.9616	0.5462	0.0065	0.2951

The obtained voltages and powers are used as references for four MMCs with P/V droop control in simulation. The steady-state results in simulation are shown in Table 4.5, which verifies the accuracy of intial power flow calculation. Additionally, the corresponding DC jacobian matrix ($\boldsymbol{J_{dc}}$) of the MMC-based DC grid can also be obtained as:

$$\boldsymbol{J_{dc}} = \begin{bmatrix} 304.5381 & -181.8182 & -121.2121 & 0 \\ -180.8566 & 405.9723 & 0 & -226.0707 \\ -120.6659 & 0 & 482.4126 & -361.9978 \\ 0 & -226.0642 & -361.7027 & 587.4653 \end{bmatrix} \tag{4.63}$$

TABLE 4.5: Simulation results of initial DC power flow for single P/V droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P_{dc} (MW)	603.1145	−379.9999	−100.0000	−120.0005
I_{dc} (kA)	1.5078	−0.9551	−0.2511	−0.3016
V_{dc} (kV)	400.0000	397.8835	398.1976	397.8730
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40	20	7.5	12.5
Line currents	I_{l1}	I_{l2}	I_{l3}	I_{l4}
(kA)	0.9616	0.5462	0.0065	0.2951

When MMC4 is isolated due to outage ($\Delta P^{*}_{dc,MMC4} = 120\,\mathrm{MW}$, $K_{droop,MMC4} = 0$), the power flow is re-distributed in the remaining three MMCs. As described in Chapter 4.4.2.1, the first step is to conduct preliminary power flow calculation deriving $\boldsymbol{\Delta P_{dc}}$ and $\boldsymbol{\Delta V_{dc}}$ based on (4.51). The matrix of droop constants in four MMCs ($\boldsymbol{K_{droop_P}}$) is $[40, 20, 7.5, 0]^{\mathrm{T}}$ under MMC4 outage, hence the resulting coefficient matrices ($\boldsymbol{A_P^{(1)}}$, $\boldsymbol{B_P^{(1)}}$) are:

$$\boldsymbol{A_P^{(1)}} = \begin{bmatrix} 0.3895 & -0.5617 & -0.5699 & -0.5673 \\ -0.2794 & 0.6679 & -0.2999 & -0.3126 \\ -0.1064 & -0.1126 & 0.8650 & -0.1265 \\ 0.0000 & 0.0000 & 0.0000 & 1.0000 \end{bmatrix}, \quad \text{and} \tag{4.64}$$

$$\boldsymbol{B_P^{(1)}} = \begin{bmatrix} 0.0153 & 0.0140 & 0.0142 & 0.0142 \\ 0.0140 & 0.0166 & 0.0150 & 0.0156 \\ 0.0142 & 0.0150 & 0.0180 & 0.0169 \\ 0.0141 & 0.0156 & 0.0169 & 0.0181 \end{bmatrix}. \tag{4.65}$$

Then the deviations of DC powers ($\boldsymbol{\Delta P_{dc}}$) and DC voltages ($\boldsymbol{\Delta V_{dc}}$) are $[-68.0812, -37.5125, -15.1836, 120.0000]^{\mathrm{T}}$ and $[1.7020, 1.8756, 2.0245, 2.1725]^{\mathrm{T}}$, respectively. However, the results show MMC2 is overloaded (4.55), hence the droop constant of MMC2 should be set as zero ($K_{droop,MMC2} = 0$) and the maximum power deviation of MMC2

is -20 MW (4.56). Hence, the updated matrix of droop constants ($\boldsymbol{K_{droop_P}}$) and power reference deviations ($\boldsymbol{\Delta P^*_{dc}}$) are $[40, 0, 7.5, 0]^{\mathrm{T}}$ and $[0, -20, 0, 120]^{\mathrm{T}}$, respectively.

The next step is to update (4.51) obtaining a new set of coefficient matrices ($\boldsymbol{A_P^{(2)}}$, $\boldsymbol{B_P^{(2)}}$):

$$\boldsymbol{A_P^{(2)}} = \begin{bmatrix} 0.1545 & -0.8410 & -0.8221 & -0.8302 \\ 0.0000 & 1.0000 & 0.0000 & 0.0000 \\ -0.1535 & -0.1685 & 0.8144 & -0.1792 \\ 0.0000 & 0.0000 & 0.0000 & 1.0000 \end{bmatrix}, \quad \text{and} \tag{4.66}$$

$$\boldsymbol{B_P^{(2)}} = \begin{bmatrix} 0.0211 & 0.0210 & 0.0206 & 0.0208 \\ 0.0209 & 0.0249 & 0.0225 & 0.0234 \\ 0.0205 & 0.0225 & 0.0247 & 0.0239 \\ 0.0206 & 0.0234 & 0.0239 & 0.0254 \end{bmatrix}. \tag{4.67}$$

Therefore, the current $\boldsymbol{\Delta P_{dc}}$ and $\boldsymbol{\Delta V_{dc}}$ are $[-82.8086, -20.0000, -18.1348, 120.0000]^{\mathrm{T}}$ and $[2.0702, 2.3110, 2.4180, 2.5823]^{\mathrm{T}}$, respectively. Table 4.6 lists the calculation results of DC power flow in the remaining three MMCs, and Fig. 4.14(b) shows the new topology after MMC4 outage with detailed current directions.

TABLE 4.6: Calculation of DC power flow for single P/V droop control after MMC4 outage in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**
P_{dc} (MW)	520.3059	-400.0000	-118.1348
I_{dc} (kA)	1.2941	-0.9995	-0.2949
V_{dc} (kV)	402.0702	400.1955	400.6155
δ_{droop}	0.05	-	0.05
K_{droop}	40	0	7.5
Line currents (kA)	I_{l1}	I_{l2}	I_{l3}
	0.8521	0.4408	0.1469

TABLE 4.7: Simulation results of DC power flow for single P/V droop control after MMC4 outage in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**
P_{dc} (MW)	520.4074	-399.9999	-118.0999
I_{dc} (kA)	1.2943	-0.9995	-0.2948
V_{dc} (kV)	402.0677	400.1915	400.6109
δ_{droop}	0.05	-	0.05
K_{droop}	40	0	7.5
Line currents (kA)	I_{l1}	I_{l2}	I_{l3}
	0.8529	0.4415	0.1467

Table 4.7 presents the simulation results of DC power flow after MMC4 outage. Because jacobian matrix refers to linear mapping, the obtained calculation results inevitably have errors compared with the results in simulation, while the errors are in acceptable range.

4.4.3.2 Verification in MMC-based DC Grid under Mixed Droop Control

The second case is that MMC2 adopts I/V droop control and the remaining MMCs still use P/V droop control constituting mixed P/V and I/V droop control (Table 4.8). Based on the description in Chapter 4.4.1.2, the line current directions have to be determined first for building the relationship amongst DC powers, currents and voltages of four MMCs. Supposing the initial reference of MMC2 is still DC power (-380 MW), the branch current directions can be obtained as Fig. 4.15(a). Then the coefficient $\boldsymbol{\Lambda}$ in (4.42) can be further acquired as:

$$\boldsymbol{\Lambda} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \\ 0 & 0 & -1 & -1 \end{bmatrix}, \tag{4.68}$$

where 1 refers to current flows out from a converter while -1 indicates current flows into a converter. The line conductance matrix ($\boldsymbol{G_l}$) of the DC grid is $[0.4545, 0.3030, 0.5682, 0.9091]^{\mathrm{T}}$. Substituting the known values (2 DC powers, 1 DC current and 1 DC voltage) into (4.42), the initial DC power flow can be derived shown in Table 4.9. Similar as single droop control, the references of outer loop control for four MMCs with mixed droop control in simulation use the derived parameters. Also, the simulation results in Table 4.10 evidences the precise initial DC power flow calculation.

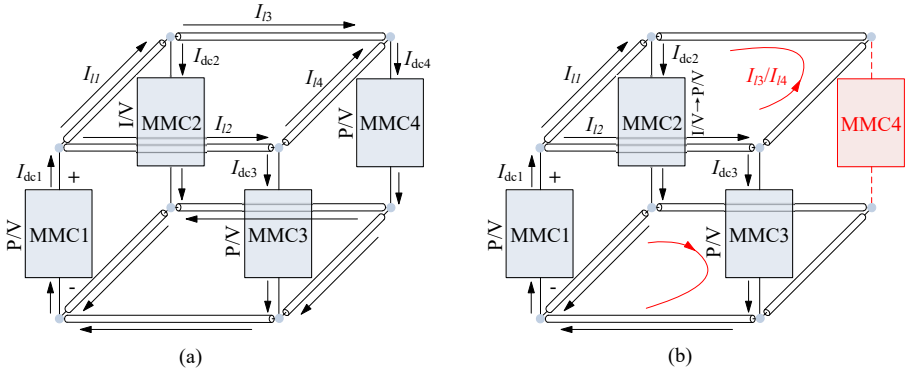


FIGURE 4.15: Detailed current directions of MMC-based DC grid under mixed droop control: (a) initial power flow, and (b) power flow after MMC4 outage.

TABLE 4.8: References of outer control loop for mixed droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P^*_{dc} (MW)	-	-	-100	-120
I^*_{dc} (kA)	-	-0.95	-	-
V^*_{dc} (kV)	400	-	-	-
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40 MW/kV	50 A/kV	7.5 MW/kV	12.5 MW/kV

TABLE 4.9: Calculation of initial DC power flow of mixed droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P_{dc} (MW)	601.0913	-377.9981	-100.0000	-120.0000
I_{dc} (kA)	1.5027	-0.9500	-0.2511	-0.3016
V_{dc} (kV)	400.0000	397.8927	398.2020	397.8788
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40	50	7.5	12.5
Line currents	I_{l1}	I_{l2}	I_{l3}	I_{l4}
(kA)	0.9579	0.5449	0.0079	0.2937

TABLE 4.10: Simulation results of initial DC power flow of mixed droop control in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**	**MMC4**
P_{dc} (MW)	601.0911	-377.9981	-99.9999	-120.0000
I_{dc} (kA)	1.5027	-0.9500	-0.2511	-0.3016
V_{dc} (kV)	400.0002	397.8927	398.2020	397.8788
δ_{droop}	0.05	0.05	0.05	0.05
K_{droop}	40	50	7.5	12.5
Line currents	I_{l1}	I_{l2}	I_{l3}	I_{l4}
(kA)	0.9578	0.5450	0.0079	0.2937

For obtaining the final DC power flow under mixed droop control after an outage of MMC4, the line current directions in current topology should also be determined first by assuming MMC2 operates with P/V droop control, which indicates the current directions in single P/V droop control (Chapter 4.4.3.1) can be used for such mixed droop control (Fig. 4.15 (b)). The next step is the establishment of power flow calculation equation (4.60) for the current topology after MMC4 isolation. The current coefficient $\boldsymbol{\Lambda'}$ is:

$$\boldsymbol{\Lambda'} = \begin{bmatrix} 1 & 1 & 0 \\ -1 & 0 & -1 \\ 0 & -1 & 1 \end{bmatrix}, \tag{4.69}$$

and the current line conductance matrix $\boldsymbol{G_l}$ is $[0.4545, 0.3030, 0.3497]^{\mathrm{T}}$. In addition, the references of remaining three MMCs are not changed, thus substituting known values into (4.60), (4.61) and (4.62), the DC power flow after MMC4 outage can be yielded.

Nevertheless, the power of MMC2 exceeds the maximum power limitation after the preliminary calculation (4.58), and the actual remaining power capacity of MMC2 is 22.0019 MW (4.58). Hence, the control mode of MMC2 switches into constant DC power control for protecting converter, and the updated $\boldsymbol{K_{droop_P}}$ and $\boldsymbol{\Delta P^*_{dc}}$ are $[40, 0, 7.5]^{\mathrm{T}}$ and $[0, -22.0019, 0]^{\mathrm{T}}$, respectively. Then the final DC power flow can be accurately derived by re-constructing (4.60), (4.61) and (4.62) considering the updated vectors of droop constants and actual DC power deviations (Table 4.11). The simulation results are shown in Table 4.12, which demonstrates the accuracy of proposed DC power flow calculation method under mixed droop control.

TABLE 4.11: Calculation of DC power flow for mixed droop control after MMC4 outage in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**
P_{dc} (MW)	520.0655	-400.0000	-117.7626
I_{dc} (kA)	1.2936	-0.9996	-0.2940
V_{dc} (kV)	402.0256	400.1499	400.5703
δ_{droop}	0.05	-	0.05
K_{droop}	40	0	7.5
Line currents	I_{l1}	I_{l2}	I_{l3}
(kA)	0.8526	0.4410	0.1470

TABLE 4.12: Simulation results of DC power flow for mixed droop control after MMC4 outage in the MMC-based DC grid.

Parameter	**MMC1**	**MMC2**	**MMC3**
P_{dc} (MW)	520.0654	-400.0000	-117.7627
I_{dc} (kA)	1.2935	-0.9996	-0.2939
V_{dc} (kV)	402.0256	400.1499	400.5704
δ_{droop}	0.05	-	0.05
K_{droop}	40	0	7.5
Line currents	I_{l1}	I_{l2}	I_{l3}
(kA)	0.8525	0.4410	0.1471

4.5 Conclusion

Various modeling approaches are described in the simulation of HVDC systems based on actual study requirements. Also, numerical integration plays significant role in solving network differential equations. EMT modeling captures the detailed switching behaviours and parallel computation avails the increase of EMT simulation speed. Electromechanical transient modeling approach is suitable for studying large-scale HVDC systems by simplifying controller design and ignoring high frequency dynamic behaviours. DP and SFP modeling methods increases simulation speed while retains accuracy by capturing dynamic frequency of HVDC systems. Co-simulation study combines different modeling approaches that serves specific requirements of accuracy in subsystems.

Droop control is a conventional control strategy for MTDC systems and DC grids. Detailed P/V, I/V and mixed droop control schemes are described considering maximum power limitation. The proposed generalized DC power flow expression studies the initial DC power flow for normal operation and the DC power flow after converter outage. A four-terminal MMC-based DC grid simulation model is built to obtain the initial power flow and the power flow after MMC outage. The maximum power limitation of MMC is also considered. The simulation results are consistent with the obtained results in simulation verifying the accuracy of proposed generalized expression of DC power flow, which can also be used to assess the static security of MTDC systems and DC grids.

Chapter 5

LCC and AAC-Based Hybrid PTP HVDC Transmission System

5.1 Introduction

This chapter introduces the development of a hybrid PTP HVDC transmission system based on an LCC and an AAC. The basic operation principles and control methods of the developed LCC-AAC hybrid PTP HVDC system are demonstrated following with appropriate system design and parameter selection. In addition, a set of control schemes is proposed for riding through AC faults and handling DC faults. The operation and performance of both converters in such a hybrid HVDC configuration are verified through a detailed set of results based on an LCC-AAC hybrid PTP HVDC system. These include steady state operation, AC-grid harmonics & DC-side ripple analysis, reference tracking (active power change at LCC station, reactive power change at AAC station) and system performance under AC-grid faults without blocking converter at both terminals of the HVDC system. Also, the response of the hybrid system under DC fault presents potential DC fault handling capability compared with the hybrid system based on LCC and MMC with HBSMs. The hybrid LCC-AAC PTP HVDC transmission system lays preliminary steps for research on complex mixed converter multiterminal DC configurations in future DC super grids.

5.2 Converter Description and Control Hierarchy

5.2.1 Converter Description

The topologies and operations of the LCC and AAC were extensively discussed in Chapter 3 and only the necessary information relevant to this chapter are described in this chapter. The operation of the LCC relies on firing angle enabling the LCC to work in rectifier or inverter mode. The typical firing angle for the LCC in rectifier mode is around $5°$ or $15°$ [138]. A smaller firing angle is more attractive due to the reduced reactive power consumption and lower overall losses, at the cost of limited system adjusting capability [138]. The normal operation of the AAC is different from the MMC due to the alternate operation of the two arms in a phase during each half-cycle of the output voltage, which also means the arms conduct the total output current (i_a). The definition of output voltage in the AAC, $v_{ac} = m_a \frac{V_{dc}}{2} \cos(\omega t + \phi)$ is similar to the MMC. The distinct operating point that has the inherent energy balancing of the AAC is called the "sweet-spot", which was explained in Chapter 3.4.2.2. The sweet-spot operation ($m_a = M_a = 4/\pi$) can be determined by the zero net energy from the energy exchange between AC side and DC side [118].

5.2.2 Control Hierarchy

The control hierarchy of the hybrid PTP HVDC systems is shown in Fig. 5.1. Following with the control hierarchy description of the MMC and AAC in Chapter 3.3.2.1 and 3.4.2.1, respectively. The first two layers (AC/DC grid control & coordinated system control) apply to both the LCC and AAC. The third layer (converter station control) performs the high level control of the LCC and AAC stations. The active/reactive power, node voltages/currents, frequency and firing/extinction angle in the third layer are regulated based on the references. The bottom layer is the internal converter control, which is also the low-level control of the LCC and AAC that regulates the i) pulse signal triggering, ii) SM sorting, iii) SM energy, iv) zero-current switching, v) circulating current, vi) overlap period and vii) OLTC coordination for extending ZCS region [118].

The LCC can adopt either constant DC current or voltage control generating proper firing angle to pulse controller, while constant firing angle/extinction angle control, if necessary, can be employed as well [128, 137]. In addition, LCC at the inverter side can equip with VDCOL avoiding coummutation failures, while the VDCOL at the rectifier side can ensure the fast and stable recovery of the LCC from faults to some extent [138]. The high and low level control for the AAC were introduced in Chapter 3.4.2.1.

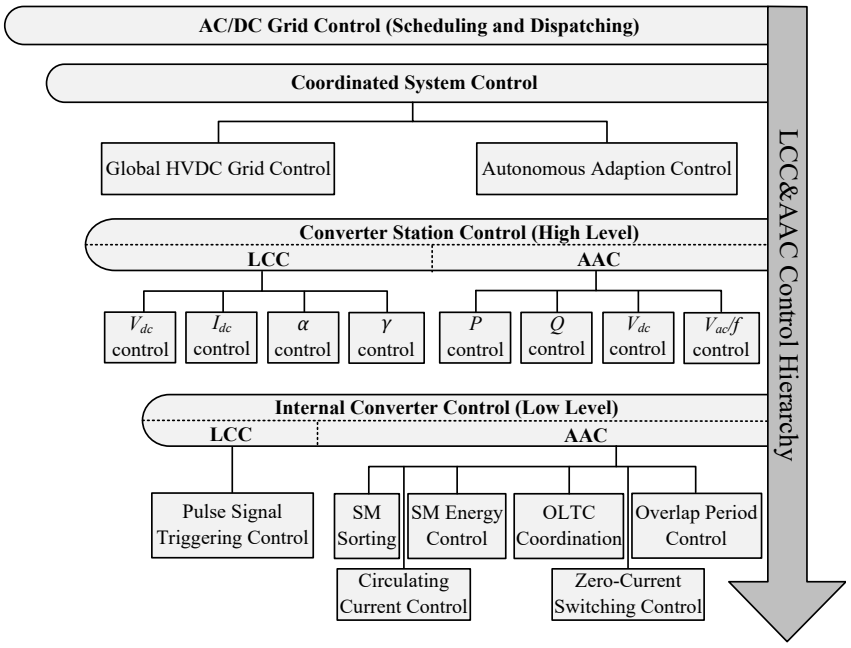


FIGURE 5.1: Control Hierarchy of the LCC and AAC-based hybrid PTP HVDC transmission system.

5.3 System Topology and Control Scheme

5.3.1 System Topology

The topology of the hybrid HVDC system, based on a ±500 kV, 3000 MVA bipole system with two 12-pulse LCCs in rectifier side and an AAC in the inverter side is shown in Fig. 5.2. Similarly to other LCC-VSC hybrid HVDC systems (Chapter 1.2), the LCC and AAC can be either in the rectifier or in the inverter terminal. Accordingly, the LCC side can adopt constant DC current or voltage control, while the AAC can adopt constant DC voltage control or power control, respectively. In this chapter, the hybrid LCC-AAC HVDC system embraces the natural immunity to commutation failures as the AAC is in the inverter side. Thus, it is not necessary for such configuration to set additional control units to handle commutation failures.

The system circuit under DC fault is shown in Fig. 5.3, which depicts the potential DC fault current path of pole-to-pole DC fault occuring at the midpoint of DC transmission line.

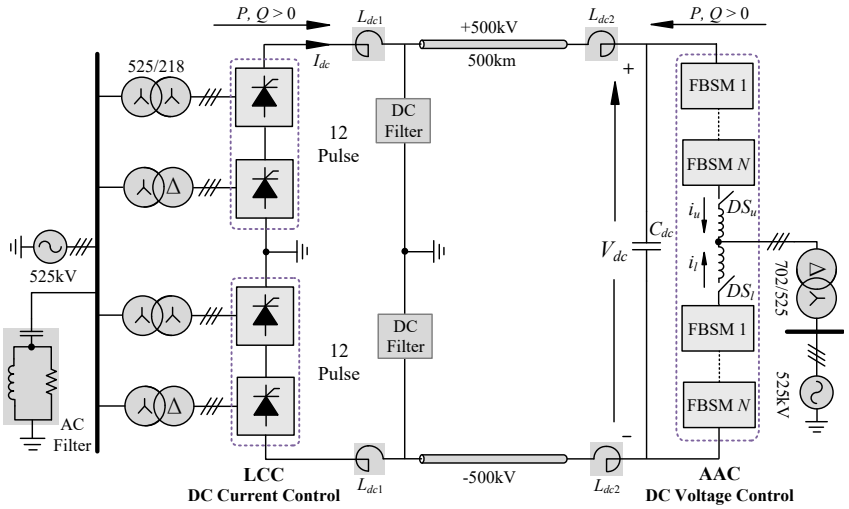


FIGURE 5.2: Topology of the LCC and AAC-based hybrid PTP HVDC transmission system.

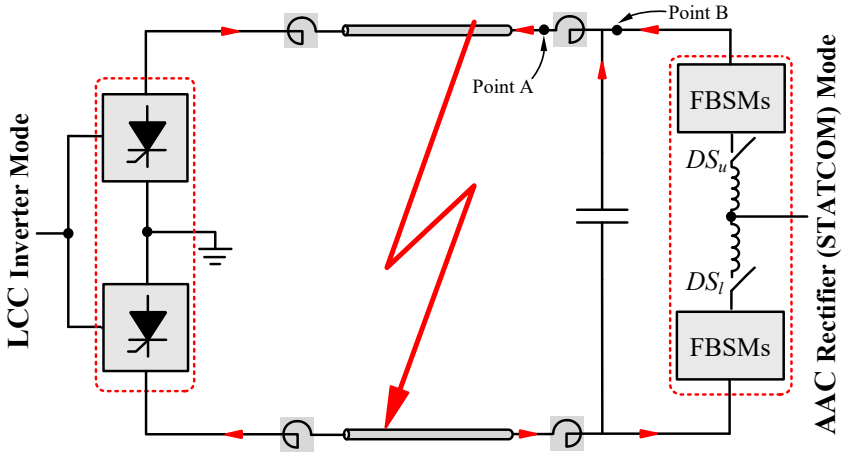


FIGURE 5.3: System circuit of the LCC and AAC-based hybrid PTP HVDC transmission system under DC fault.

5.3.2 Control Scheme

5.3.2.1 Control Scheme under Normal Operation

Fig. 5.4 provides a complete description of all levels of control considered in the hybrid PTP LCC-AAC HVDC system. As mentioned earlier, the LCC side controller does not consider additional functionalities for handling commutation failures and the AAC side control has been implemented without energy regulation of the AAC during direct or indirect control [30]. At the LCC station, the DC current is controlled by generating firing angles from 5° to 150°. As the system is based on a 12-pulse rectifier, the controller generates two sets of pulses with 30 degree shift. In order to coordinate with the controller of the LCC station, the AAC side controls the DC voltage to maintain constant power with additional

reactive power control as the outer control loops. In addition, the AC output voltage reference generated from the inner current controller is used the modulation stage, overlap period and circulating current.

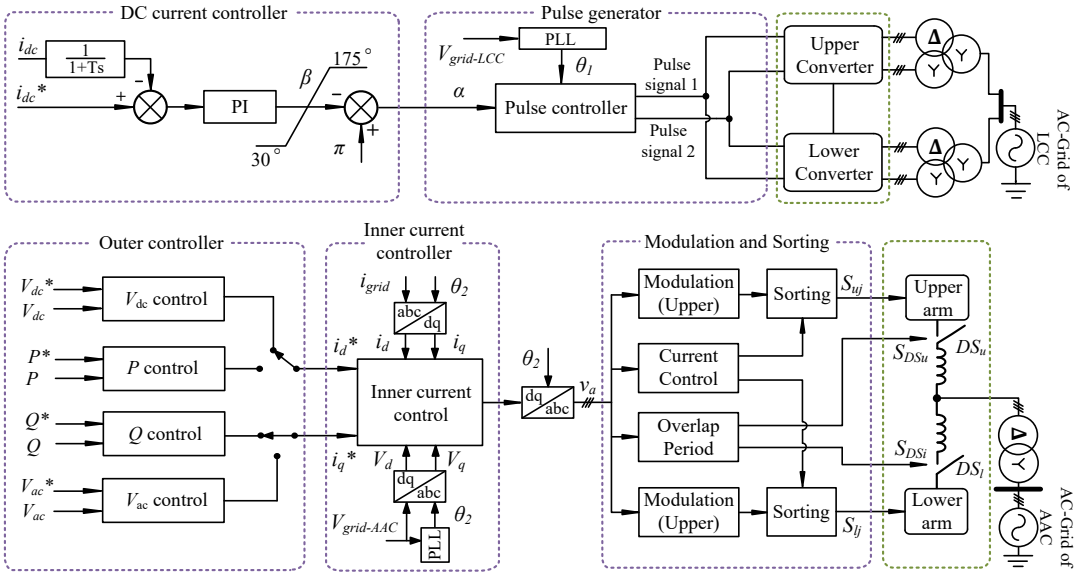


FIGURE 5.4: Control Structure of the LCC and AAC-based hybrid PTP HVDC transmission system.

The main purpose of the modulation stage is to determine the number of SMs utilized in each arm, and the nearest level modulation (NLM) is adopted for the AAC, which is also the most advantageous method for the large number of SMs [197]. The overlap period controller determines the alternate operation of director switches (DSs) and the energy balancing when the AAC operates with a short overlap period, while the circulating current controller decides the number of additional SMs for over-modulation operation [118].

5.3.2.2 Control Scheme under AC and DC Faults

Based on the aforementioned control structure of the LCC and AAC-based hybrid HVDC system, the LCC cannot maintain DC current constant when AC fault occuring at the LCC side, which means the DC current will decrease with the fault level. When the AC fault is cleared, the DC voltage of the LCC will experience instantaneous increase which would lead to a transient overcurrent in the DC-link of the LCC side. Fig. 5.5 (a) shows the recovery control strategy for riding through AC fault of the LCC side and avoiding overcurrent. First, the VDCOL can be employed for stable recovery of DC current [138]. In addition, the integrator of DC current controller will be reset to 0 for increasing the firing angle, then reducing the DC voltage of LCC side to a maximal degree.

Similarly, in the case of an AC fault on the AAC side, the outer control loop for the AAC is temporarily disabled in order to assist the response of the converter due to the fast response of the inner current controller compared to the outer loop. In addition, the controller of the AAC will be re-enabled when receiving the clearing signal of the AC fault, as shown in Fig. 5.5 (b).

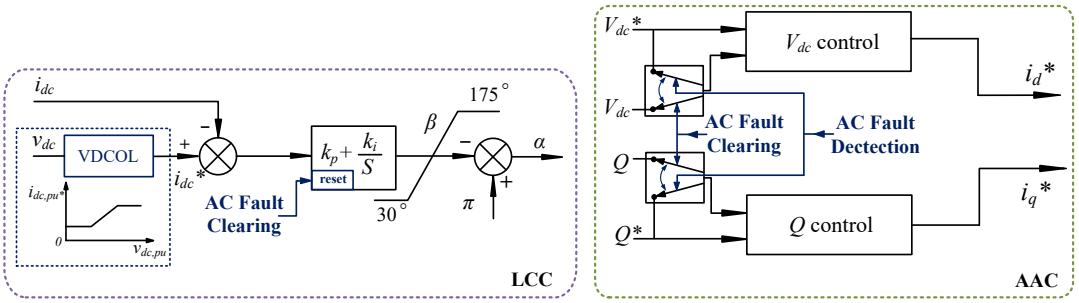


FIGURE 5.5: Control scheme for riding through AC fault in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) AC fault occurring at LCC side and (b) AC fault occuring at AAC side.

Fig. 5.6 (a) and (b) show the control schemes for a handling permanent DC fault in the hybrid HVDC system based on the LCC with AAC and HB-MMC, respectively. First, the LCC has to force the firing angle into the maximum value, then the LCC will operate as inverter [88]. Moreover, the AAC and HB-MMC are blocked when detecting the DC fault for protecting IGBTs of SMs, and the DC voltage and reactive power references of the AAC are set to 0 at the same time. For the combination of LCC and HB-MMC, the AC breaker for the HB-MMC has to open for utterly cutting off the fault current while the DC breaker is

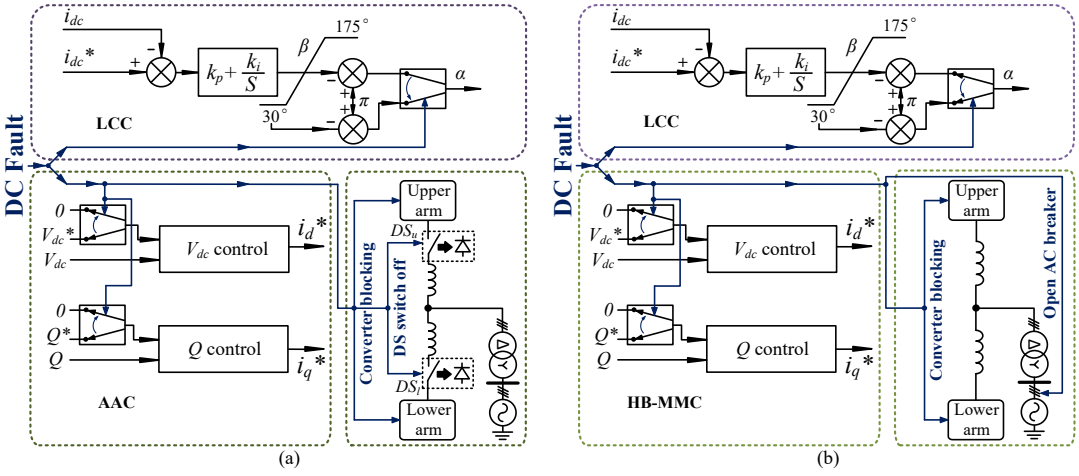


FIGURE 5.6: Control scheme for handling permanent DC fault in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) LCC-AAC hybrid HVDC system and (b) LCC-HBMMC hybrid HVDC system.

more efficient at the cost of high investment. It is worth mentioning that it is necessary to switch the DSs off during the DC fault for thoroughly cutting off the fault current, since the antiparallel diodes in DSs further ensures the fault current can only flow from fault point to upper arms via lower arms. The comparison of DC fault handling capability between the LCC with the HB-MMC and AAC will be shown in Chapter 5.5.4.

5.4 System Parameter Selection

5.4.1 Main Parameters of the LCC

The detailed model parameters of the LCC are given in Table 5.1, with the rated AC voltage level for the LCC side selected as 525 kV. The DC output voltage (V_{dcl}) of LCC terminal is:

$$V_{dcl} = R_{dc} I_{dcl} + V_{dca}, \tag{5.1}$$

where I_{dcl} and R_{dc} is the DC current of the LCC side and line resistance respectively, V_{dca} is the DC output voltage at the AAC DC terminals ($\pm$500 kV). The active power and reactive power can be calculated as (5.2) and (5.3) , where ϕ is power factor angle.

$$P_{dcl} = V_{dcl} I_{dcl}, \tag{5.2}$$

$$Q_{dcl} = P_{dcl} \tan \phi. \tag{5.3}$$

TABLE 5.1: Rectifier parameters (LCC) in the LCC and AAC-based hybrid PTP HVDC transmission system.

Parameters	**LCC Rectifier Side**
Rated Power	3000 MVA
Nominal Frequency	50 Hz
AC Voltage (L-L,rms)	525 kV
Transformer Ratio	525/218
Transformer Leakage Inductance (p.u.)	0.18
AC System Impedance	23.5$\angle$84.3°
Reactive Compensation Capacity	1400 MVar (140 MVar/group)

The secondary side voltage of transformer follows (5.4), where N is the number of 6-pulse converters ($N = 2$ in 12-pulse converter), k_s is $3\sqrt{2}/\pi$ for a 6-pulse thyristor bridge,

α is the firing angle and X_L is the leakage reactance of transformer.

$$V_{2l} = \frac{V_{dcl}}{k_s N \cos\alpha} + \frac{X_L I_{dcl}}{\sqrt{2}\cos\alpha} = \frac{V_{dcl}}{k_s N(\cos\alpha - \frac{X_{\text{p.u.}}}{2})}. \tag{5.4}$$

5.4.2 Main Parameters of the AAC

Each arm in the AAC consists of H-bridge SMs and an array of DSs. Adopting H-bridge SMs enables the AAC to operate in the over-modulation range and embrace DC line fault ride-through capabilities. In addition, the arm voltage in the AAC is only half of the DC voltage, since two DSs in each phase alternately conduct the AC current. The parameters of the AAC station are provided in Table 5.2, which can be divided into four main aspects: i) system standard operating point; ii) the number of SMs and IGBTs in each DS; iii) overlap period and iv) SM capacitance and arm inductance [118].

The energy exchange between the arms in each phase is limited by the alternate operation of DSs, and the final AC and DC energy balancing point is defined as the system operating point, which is also called sweet spot ($M_a = 4/\pi = 1.27$), but considering $\pm 10\%$ voltage variation under normal operation, the standard operating point (m_a) adopted in the hybrid system is expressed as (5.5).

$$m_a = \frac{M_a}{k_a}, \tag{5.5}$$

TABLE 5.2: Inverter parameters (AAC) in the LCC and AAC-based hybrid PTP HVDC transmission system.

Parameters	**AAC Inverter Side**
Rated Power	3000 MVA
Nominal Frequency	50 Hz
AC Voltage (L-L,rms)	525 kV
Transformer Ratio	525/702
Transformer Leakage Inductance (p.u.)	0.18
Transformer Resistance (p.u.)	0.006
Number of SMs per arm	640
Nominal SM Voltage	1 kV
Stored Energy	11 kJ/MVA
SM Capacitance	17.2 mF
Arm Inductance (p.u.)	0.02
Nominal Operating Point (m_a)	1.15
AC System Impedance	$7.9 \angle 84.3°$

where $k_a \in (1, 1.1)$. Accordingly, the peak voltage stress of DSs ($\hat{V}_{DS}$) and peak output voltage of the AAC ($\hat{V}_a$) at such standard operating point are:

$$\hat{V}_{DS} = \frac{V_{dc}}{2} \tag{5.6}$$

$$\hat{V}_a = m_a \hat{V}_{DS} = \frac{M_a V_{dc}}{2k_a} \tag{5.7}$$

FBSMs adopted in the AAC can block the AC voltage at the standard operating point and enable the AAC to operate at over-modulation range. In addition, the maximum withstand voltage for nonconducting DSs per arm is half of the DC voltage. Hence, the number of SMs (N_{SM}) and IGBTs in each DS (N_{DS}) per arm at standard operating point is determined as:

$$N_{SM} = \frac{\hat{V}_a}{V_c} = \frac{M_a V_{dc}}{2k_a V_c} \tag{5.8}$$

$$N_{DS} = \frac{\hat{V}_{DS}}{V_c} = \frac{k_a N_{SM}}{M_a}, \tag{5.9}$$

where V_c is the nominal capacitor voltage of each SM in the AAC and is set as 1 kV in this chapter.

The overlap period in the AAC allows exchange of energy between upper arm and lower arm, and the output current flowing two arms is equally distributed. The period of overlap should be within a reasonable range avoiding output voltage distortions, and the maximum value of it is limited by the redundant voltage (V_r). Additionally, the redundant voltage varies within a $\pm 10\%$ range considering the SM capacitor voltage ripple. Thus, assuming the output reference voltage $v_o = m_a \cos(\omega t)$, the range of redundant voltage and overlap period ($\hat{t}_{ov}$) in the AAC can be respectively expressed as:

$$\frac{V_{dc}(0.9M_a - k_a)}{2k_a} \leq V_r \leq \frac{V_{dc}(1.1M_a - k_a)}{2k_a}, \qquad \text{and} \tag{5.10}$$

$$\hat{t}_{ov} = \frac{\pi - 2\cos^{-1}(1 - \frac{k_a}{M_a})}{\omega} \tag{5.11}$$

The energy stored in AAC is set to 11 kJ/MVA. The value of capacitance in each SM of the converter is calculated based on (5.12). The value of the arm inductance follows with the calculation in [118] and can be determined as (5.13), which considers the redundant voltage utilization efficiency to achieve circulating current control, and a minimum circulating current gradient.

$$C_{SM} = \frac{2SE_{AAC}}{6N_{SM}V_c^2} \tag{5.12}$$

$$L \leq \frac{3V_{dc}V_r(\pi - 2\cos^{-1}(1 - \frac{k_a}{M_a}))}{8\omega\pi S} \tag{5.13}$$

where, S is the converter rating and E_{AAC} is the energy requirement in each SM of the AAC.

5.4.3 DC Transmission Line and Control Parameters

The system includes a 500 km DC transmission line (cable) at voltage level of $\pm$500 kV. The parameters of the transmission line (lumped parameter pi-section) are listed in Table 5.3. In addition, Table 5.3 also provides the control parameters used in the low-level and high-level controllers for both stations.

TABLE 5.3: DC transmission line and control parameters in the LCC and AAC-based hybrid PTP HVDC transmission system.

Transmission Line Parameters	
DC Line Voltage (kV)	$\pm$500
Length (km)	500
Resistance (Ω/km)	0.011
Inductance (mH/km)	0.2615
Capacitance (μF/km)	0.2185
Conductance (μS/km)	0.055
Control Parameters	
DC Current Control - LCC	$K_P = 0.25, K_I = 92.85$
DC Voltage Control - AAC	$K_P = 8, K_I = 272.5$
Reactive Power Control - AAC	$K_P = 1.3, K_I = 30$
Energy Balancing - AAC [30]	$K_P = 2.9, K_I = 75$
PLL - LCC	$K_P = 5, K_I = 10$
PLL - AAC	$K_P = 0.084, K_I = 4.69$

5.4.4 AC and DC Link Filters

Harmonics in AC and DC sides need to be considered in HVDC transmission systems, as the harmonic currents lead to voltage and current distortion at the point of common coupling (PCC) and DC-link. Therefore, AC and DC filtering requirements are major design considerations for LCC-VSC hybrid HVDC systems.

The LCC-based HVDC station has both characteristic and uncharacteristic harmonics in the AC and DC sides [198]. Thus, AC and DC filters are required to reduce harmonic levels. The tuning points for AC filters of LCC are set at 3^{rd}, 11^{st}, 13^{rd}, 24^{th} and 36^{th},

respectively. There are in total 10 groups of AC filters (140 MVar/group) installed for flexible switching, which are further classified into i) 3 groups of shunt capacitor (SC), ii) 4 groups of double-tuning (DT) filters tuned at $11^{st}/13^{rd}$ and iii) 4 groups of triple-tuning (TT) filters tuned at $3^{rd}/24^{th}/36^{th}$. The configurations and detailed parameters are shown in Fig. 5.7 and Table. 5.4. In addition, the 12^{nd} & 24^{th} harmonics are the main characteristic harmonics in the DC side of LCC, hence a DT DC filter is designed as Fig. 5.8 with detailed parameters in Table 5.6. Moreover, the smoothing reactor in DC-link of LCC station is necessary to be installed for decreasing DC current ripple and avoiding current discontinuity in minimum power [128, 199].

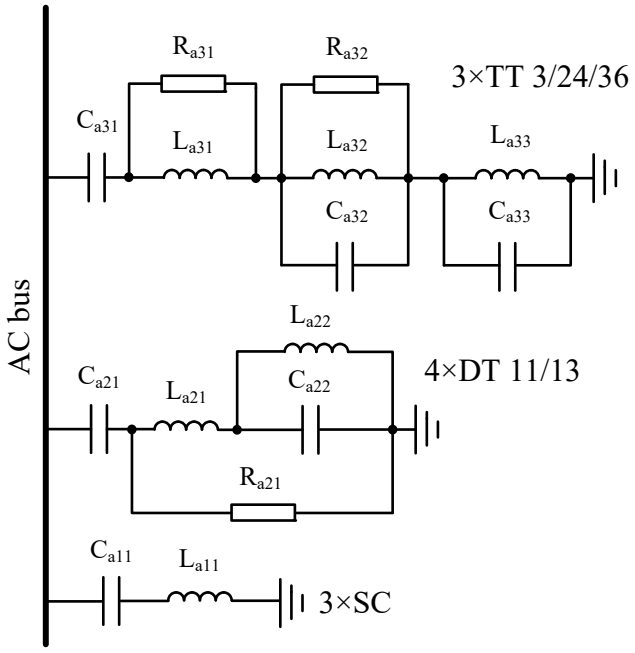


FIGURE 5.7: AC filters in the LCC station.

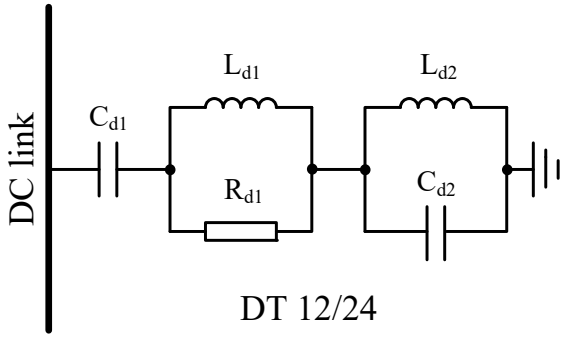


FIGURE 5.8: DC filters in the LCC station.

The DC-link current at the AAC side contains a six-pulse ripple, hence the AAC also requires the use of a DC filter [22, 118]. However, AC filters are not necessary for

TABLE 5.4: Detailed paramerters of AC filters in the LCC station.

Parameters	**SC**	**DT (11/13)**	**TT (3/24/36)**
Number of Groups	3	4	3
Capacity (MVar)	140	140	140
C_{a11} (μF)	1.616	-	-
C_{a21} (μF)	-	1.605	-
C_{a22} (μF)	-	56.824	-
C_{a31} (μF)	-	-	1.578
C_{a32} (μF)	-	-	7.218
C_{a33} (μF)	-	-	7.704
L_{a11} (mH)	2.721	-	-
L_{a21} (mH)	-	44.731	-
L_{a22} (mH)	-	1.239	-
L_{a31} (mH)	-	-	8.116
L_{a32} (mH)	-	-	129.39
L_{a33} (mH)	-	-	1.634
R_{a21} (Ω)	-	2500	-
R_{a31} (Ω)	-	-	400
R_{a32} (Ω)	-	-	1500

the AAC, owing to the near sinusoidal multilevel output voltages. The AAC with short overlap period requires a DC capacitor to realise sufficient energy exchange between DC side and SMs, and the energy stored in DC-link capacitor for the AAC is equal to about one third of the total capacitive energy in SMs. Considering the energy deviation ($\Delta E_{AAC} \in (0.9, 1.1)$) of SMs, the energy storage of DC capacitor can be calculated as $C_{dc}V_{dc}^2/2 = S\Delta E_{AAC}E_{AAC}/3$ [200], then the required capacitance value at DC-link can follow with (5.14).

$$C_{dc} > \frac{2S\Delta E_{AAC}E_{AAC}}{3V_{dc}^2} \tag{5.14}$$

The DC-link capacitor and smoothing reactor are essential in AAC terminal due to the six-pulse current ripple caused by the alternate operation of the AAC arms [118]. For filtering the 6^{th} harmonic and other higher harmonics, the reactance value is calculated as (5.15), following the characteristics of an LC filter with a cut-off frequency below $6f$.

$$L_{dc} > \frac{1}{144\pi^2 f^2 C_{dc}} \tag{5.15}$$

The smoothing reactance value in DC-link of the LCC is far larger than the AAC [118, 128] which is usually from 200 mH to 700 mH [201]. Additionally, the DC voltage in developed system is controlled by the AAC side, thus the DC voltage deviation at the AAC station will make an impact on DC voltage of the LCC, although the main characteristic

harmonics are filterd by two sets of double-tuned damping DC filters. In general, the DC filter and smoothing reactor design of the LCC can follow with conventional scheme [128], and the values of DC capacitance and smoothing reactance of the AAC can be decided by (5.14) and (5.15) (Table 5.5).

TABLE 5.5: The limitation of DC-link filters in the LCC and AAC stations.

Parameters	**LCC (rectifier)**	**AAC (inverter)**
L_{dc1}/L_{dc2}	200 mH$\sim$700 mH	$>$11.6 mH
DC filter/C_{dc}	double (triple)-tuned damping filter	$>$24.2 μF

For determining the appropriate DC-link filters in the LCC-AAC hybrid system, it is necessary to analyze DC-side ripples for both the LCC and AAC stations, since the low ripples mean high quality of output waveforms. Moreover, the low ripples also reflect less AC components (harmonics) in DC voltage and current.

Based on the above analysis, the related values of DC-link filters for developed system are shown in Table 5.6 restricting DC current ripples below 3% and voltage ripples below 2% of both stations. The values of smoothing reactance of the LCC and AAC should be in the range of limitation in Table 5.5 and can be changed by the expected DC-link ripples. In addition, the DC capacitor of AAC with proper value can not only coordinate with smoothing reactor to obtain smoother DC current and decrease voltage ripples, but also ensure system stable operation by balancing power between DC and AC. The DC-link ripples can be further reduced, if necessary, with larger smoothing reactor, capacitor as well as multi-tuned DC filter at the cost of higher investment.

TABLE 5.6: Detailed paramerters of DC-link filters in the LCC and AAC stations.

DC-link filters at LCC and AAC stations	
DC Filter of LCC	C_{d1} = 0.35 μF, L_{d1} = 89.35 mH C_{d2} = 0.81 μF, L_{d2} = 48.86 mH R_{d1} = 10000 Ω
Smoothing Reactance of LCC	250 mH
DC Capacitance of AAC	65 μF
Smoothing Reactance of AAC	25 mH

5.4.5 Comparison between the MMC and the AAC

In order to demonstrate benefits of the AAC in hybrid HVDC systems, the main differences between the MMC and the AAC are described with the same power rating and voltage level. The related parameters of the MMC are in Table 5.7. Compared with HB-MMC,

AAC has over-modulation capability as the employment of bipolar SMs, hence potential DC fault handling capability. In addition, the AAC requires a lower number of SMs per arm compared with FB-MMC due to the alternate operation of two arms in each phase. Although the introduction of DSs for the AAC lead to additional IGBTs per arm, the total number of semiconductor devices for the AAC are still less than the FB-MMC. Considering the $\pm$10% capacitor voltage deviation, the energy requirement of SMs in the AAC is only 11 kJ/MVA, which is about one third of such in the MMC. The capacitors of SMs occupy the main volume in modular VSCs, thus the total converter size of the AAC is less than the MMC while the AAC has to install additional DC-link filter [118].

Based on the above discussion, the AAC is suitable for future HVDC market. Hence, the AAC can replace the MMC combining with the mature LCC to constitute hybrid LCC and AAC-based HVDC system by employing individual benefits.

TABLE 5.7: Inverter Parameters (MMC) in the LCC and MMC-based hybrid PTP HVDC transmission system.

Parameters	**MMC Inverter Side**
Rated Power	3000 MVA
Nominal Frequency	50 Hz
AC Voltage (L-L,rms)	525 kV
Transformer Ratio	525/551
Transformer Leakage Inductance (p.u.)	0.18
Transformer Resistance (p.u.)	0.006
Number of SMs per Arm	1000
Nominal SM Voltage	1 kV
Stored Energy	30 kJ/MVA
SM Capacitance	30 mF
Arm Inductance (p.u.)	0.15
Nominal Operating Point (m_a)	0.9
R/X Ratio of AC System	0.1

5.5 Simulation Results

In order to verify the performance of the LCC-AAC hybrid HVDC system, a detailed simulation model (Fig. 5.2) is implemented using PLECS-Blockset and Simulink. The results based on the implemented 3000 MVA hybrid HVDC system demonstrate four different operating scenarios: i) steady state operation with harmonic and ripple analysis for AC side and DC link, respectively, ii) reference tracking including the active power change of LCC side and reactive power change of AAC side, iii) AC faults at both stations, and iv) DC

fault at the midpoint of the DC tranmission line, validating the operation of hybrid HVDC system within widely accepted HVDC operating standards [101, 202].

5.5.1 Steady-State Operation

In steady-state operation, the LCC station (rectifier) operates in DC current ($I^*_{dc1} = 3$ kA) control mode obtaining firing angle about 15°. The AAC station (inverter) operates in the DC voltage ($V^*_{dc} = 1000$ kV) and reactive power ($Q^* = 0$ MVAr). Fig. 5.9 and Fig. 5.10 show the AC and DC side voltages and currents of the hybrid HVDC system, respectively.

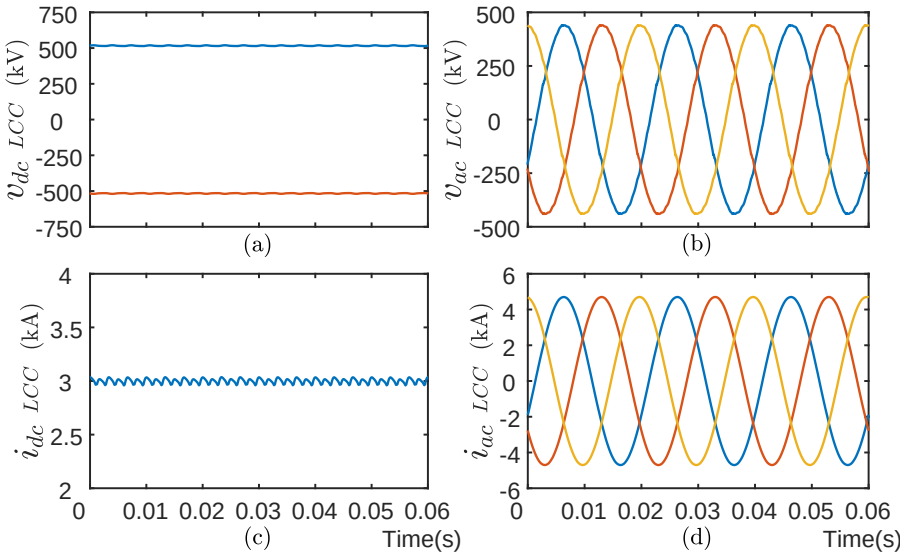


FIGURE 5.9: Steady state waveforms of the LCC side in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) DC voltage, (b) AC grid voltage, (c) DC current and (d) AC grid current.

The DC current at the rectifier side is regulated to the reference, I^*_{dc} with a ripple of 2.5%. The rectifier DC voltages is at $1.033V^*_{dc}$ and the direct converter output voltage before DC filters consists of the twelve-pulse ripple of 18.3%, while such ripple is reduced to 1.2% after DC filters. The inverter side DC voltage is regulated to the reference, V^*_{dc} with ripple of 0.8% and the DC current comprises of a sixth harmonic ripple of 2% which is imposed by the alternate operation of the AAC arm [22]. The DC voltages and currents demonstrate that all ripples are contained within the network standard limits at full rated power and also the appropriate design and selection of the DC filter parameters from Chapter 5.4.4.

Fig. 5.11(a) and Fig. 5.12(a) respectively show the harmonics of DC side after filters in the LCC and AAC station. The DC current in the LCC station mainly contains $6k$ order harmonics (Fig. 5.11(a)), and the low order harmonics of DC current in the AAC station

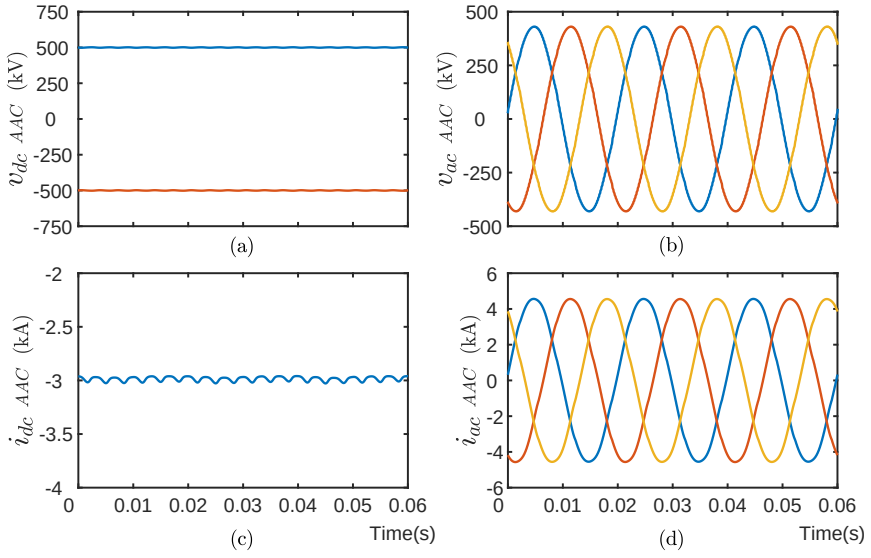


FIGURE 5.10: Steady state waveforms of the AAC side in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) DC voltage, (b) AC grid voltage, (c) DC current and (d) AC grid current.

(Fig. 5.12(a)) is larger than the LCC station, with each individual harmonic for the DC side of the hybrid HVDC system below 1%.

The AC voltages and currents are also maintained to comply with network operating standards, limiting the %THDs below 2% as shown in Fig. 5.11(b) and Fig. 5.12(b),

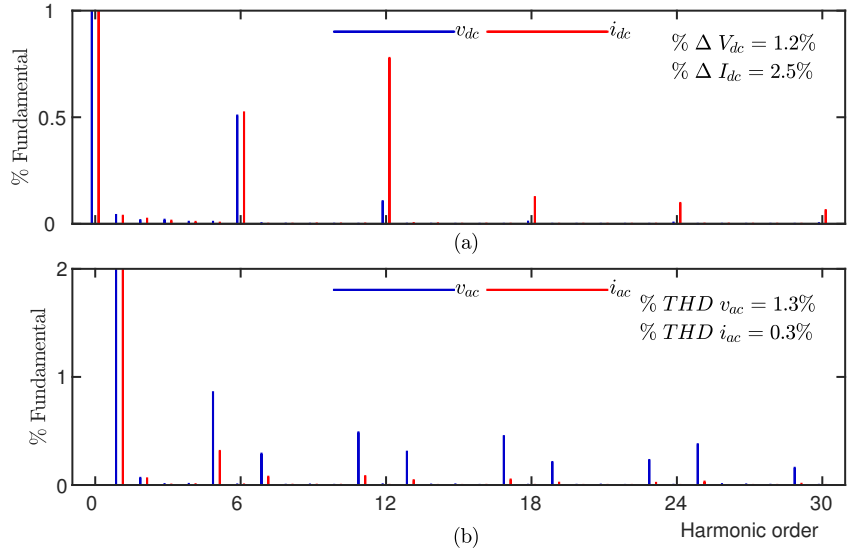


FIGURE 5.11: Harmonics of the LCC station in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) harmonics of DC voltage and DC current and (b) harmonics of AC voltage and AC current.

which also satisfy the IEEE standard for THD at PCC (2% for AC voltage, 1.5% for AC current) [202]. In addition, the power from both AC systems agree with the desired operation of the HVDC system according to the references.

The AAC requires active energy balancing for the normal operation which is performed using the low-level control functions [22, 30, 118]. Fig. 5.13(a) and (b) show the SM capacitor voltages and arm currents of the AAC HVDC station, and the arm current direction follows with the Fig. 5.2. The active energy balancing and overlap circulating current control method of [30] is employed in the AAC HVDC station. The SM capacitor voltages are regulated to their nominal references and the arm currents remain balanced demonstrating the performance of low-level energy balancing and circulating current control functions. Hence, these results demonstrate the performance of high-level control functions of the LCC and AAC HVDC stations and the feasible operation of the LCC-AAC hybrid system.

5.5.2 Reference Tracking / Steady-State

5.5.2.1 DC Current Reference Change

The LCC side adopts a constant DC current control mode to control active power, and the initial active power is set at 3000 MW (1 p.u.). The system performance when the active

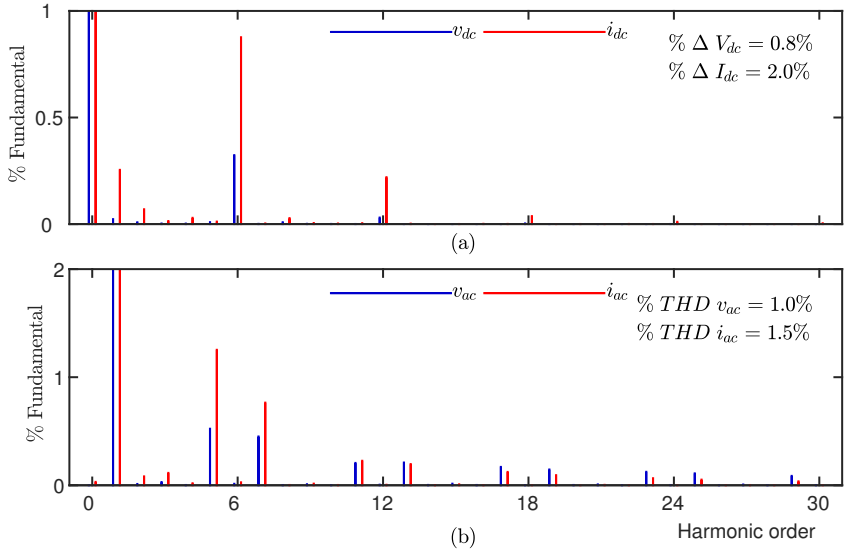


FIGURE 5.12: Harmonics of the AAC station in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) harmonics of DC voltage and DC current and (b) harmonics of AC voltage and AC current.

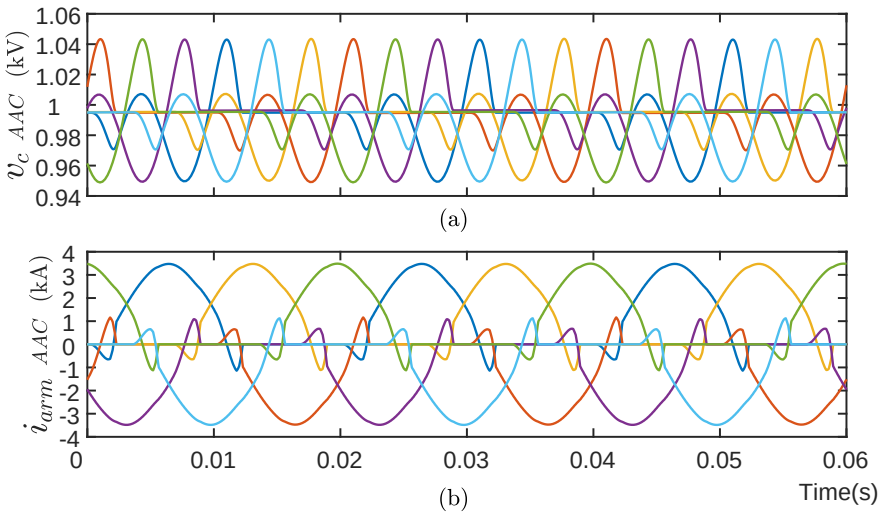
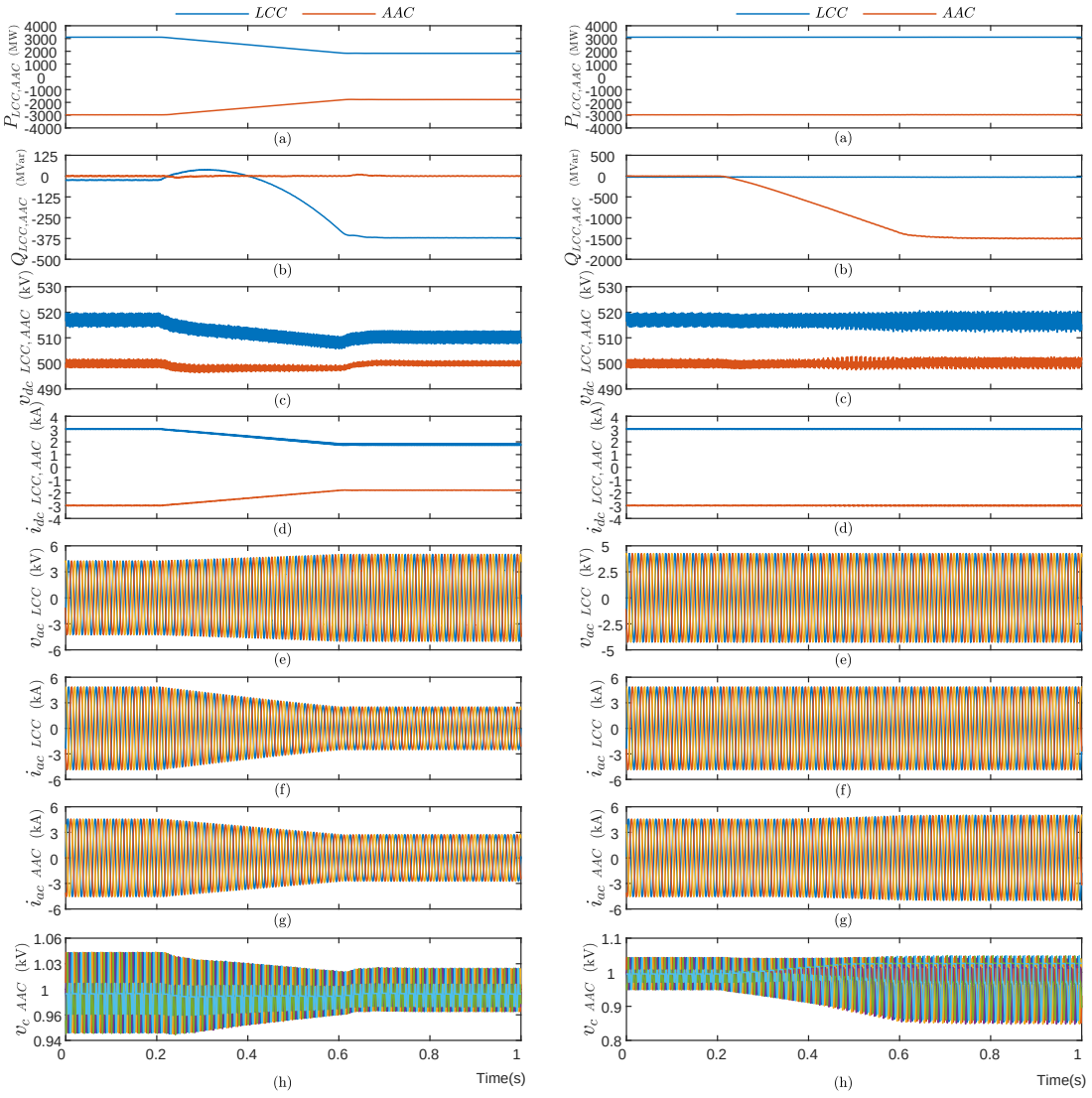


FIGURE 5.13: Capacitor voltages and arm currents of the AAC in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) SM capacitor voltages and (b) arm currents.

power reference decreases to 0.6 p.u at 0.2 s. is shown in Fig. 5.14(1). Fig. 5.14(1) (a)-(b) show the power variation of both terminals, where the decrease of active power at the LCC side coincides with the increase of reactive power due to the decreased reactive power consumption of LCC, while the reactive power of the AAC side is maintained constant as the AAC can independently control the reactive power at its AC terminal. Moreover, the AC voltage and current change of the LCC side is shown in Fig. 5.14(1) (e)-(f). However, the AC voltage of the AAC keeps constant and the AC current drops with change of power (Fig. 5.14(1) (g)). In addition, the ripple of capacitor voltage in Fig. 5.14(1) (h) reduces significantly during the process.

5.5.2.2 Reactive Power Reference Change

Fig 5.14(2) shows the hybrid system response when reactive power of the AAC terminal increases to 0.5 p.u. from 0 at 0.2 s. Fig 5.14(2) (a) and (b) show the power regulation of both stations. Fig 5.14(2) (c) and (d) demonstrate the DC voltage and current can maintain constant during reactive power change. Moreover, there are only small deviations of both AC voltage and current (Fig 5.14(2) (e) and (g)) in the AAC station. The result demonstrates that the developed hybrid system can work under reactive power reference change while with larger ripple of capacitor voltage and arm current. In addition, the change of reactive power reference has no impact to the LCC side (Fig 5.14(2) (f)), which guarantees the system reliability when providing reactive power support at the AAC side.



(1) DC current reference change. (2) Reactive power reference change.

FIGURE 5.14: Performance under DC current and reactive power reference changes in the LCC and AAC-based hybrid PTP HVDC transmission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC grid voltage of LCC, (f) AC grid current of LCC, (g) AC grid current of AAC and (h) SM capacitor voltage of AAC.

5.5.3 Performance under AC Faults

The AC FRT capability of hybrid HVDC system ensures robustness of the hybrid HVDC system. Thus, this part will discuss both the single-line to ground fault (SLG) and three-phase short circuit fault at both the LCC and AAC sides. Both AC-grid faults are applied at the terminals of each station and with AC voltage drop about 60%, defining the envelope of performance for the hybrid system.

5.5.3.1 AC Faults at the AC-Grid of the LCC

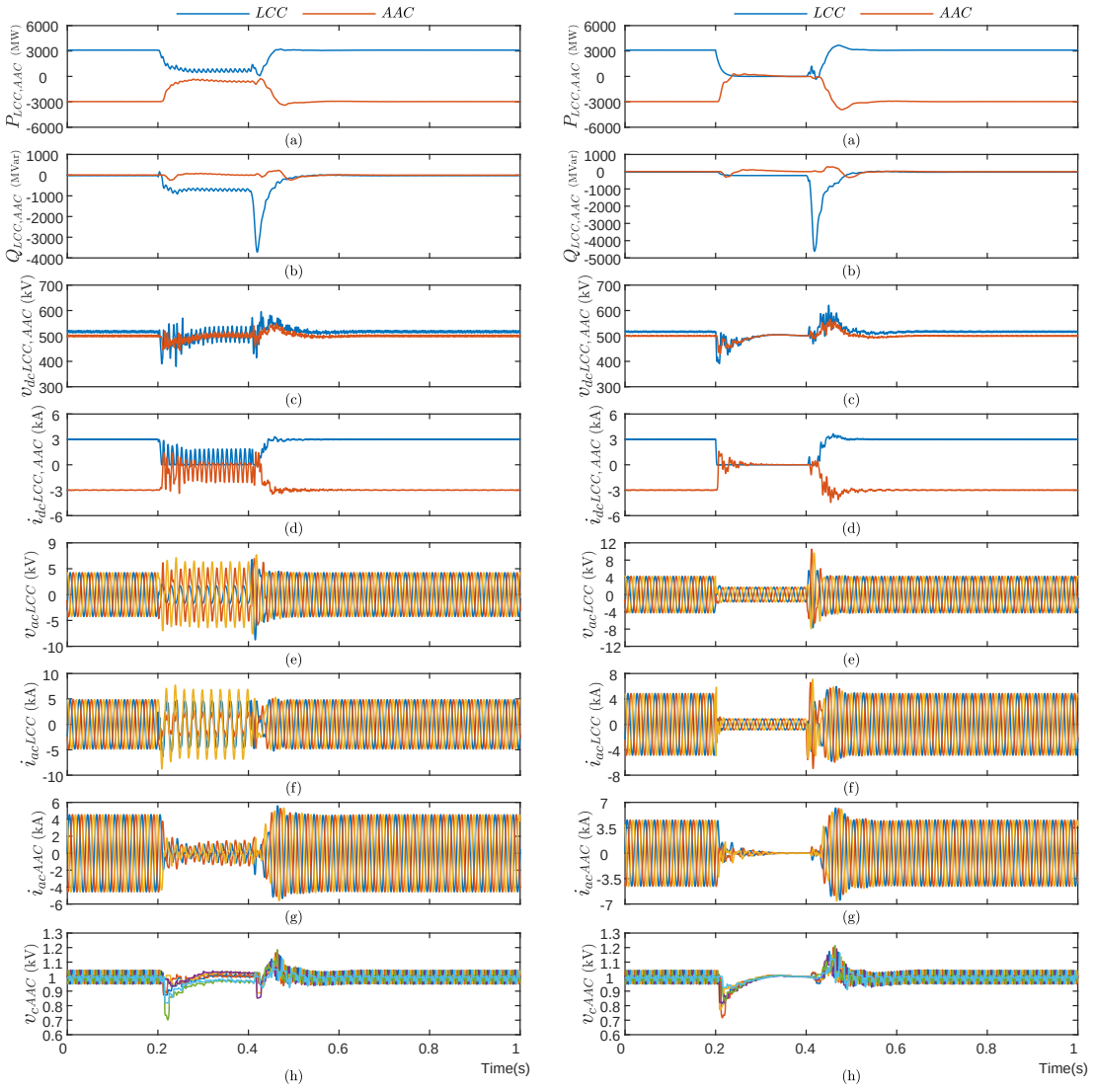
Fig. 5.15(1) shows the behavior of the overall system during a 200 ms SLG fault at the AC-grid of the LCC side. The power oscillation during the fault is shown in Fig. 5.15(1) (a)-(b) with a DC side voltage and current deviation in Fig. 5.15(1) (c)-(d) due to the oscillations of AC side at the LCC terminal (Fig. 5.15(1) (e)-(f)). The AC current reduction at the AAC side (Fig. 5.15(1) (g)) is due to the instantaneous power drop in the DC side. In addition, the system performance under 200 ms three-phase short circuit fault of the LCC side (Fig. 5.15(2)) is similar as SLG fault, but power (Fig. 5.15(2) (a)-(b)) and AC current (Fig. 5.15(2) (e) and (g)) of both sides temporarily reduce to zero. The capacitor voltage (Fig. 5.15(1) (h) and Fig. 5.15(2) (h)) increases approximately by 15% and 20%, respectively at the moment of fault recovery with the increase of DC voltage.

It is noteworthy that the firing angle increases, reducing the higher instantaneous DC voltage of the LCC terminal via integrator reset of DC current controller, hence there is no obvious DC current increase for both the LCC and AAC stations. In addition, VDCOL is adopted for fast recovery of DC current. In general, the developed system under AC faults at the LCC station presents the same performance of other LCC-VSC topologies demonstrating the accuracy of developed LCC-AAC hybrid system [65, 77, 80].

5.5.3.2 AC Faults at the AC-Grid of the AAC

Fig. 5.16(1) and Fig. 5.16(2) show the system performance during a SLG and three-phase short circuit fault at the AAC side, respectively. Similarly to the previous analysis, the power oscillation, DC side voltage and current are shown in Figs. 5.16(1) (a)-(d) and Figs. 5.16(2) (a)-(d). The AC voltage and current oscillations are respectively shown in Fig. 5.16(1) (e)-(h) and Fig. 5.16(2) (e)-(h). In addition, the capacitor voltage deviation is within 0.5 p.u during a SLG fault (Fig. 5.16(1) (i)) and 0.7 p.u. during a three-phase short circuit fault (Fig. 5.16(2) (i)).

The results show that the developed hybrid system can ride through AC faults of the AAC station and maintain power transmission under low voltage level without blocking converter. When the AC faults are cleared, the whole system can recover to normal operation in less than 150 ms, demonstrating the recovery capability of developed hybrid HVDC system.



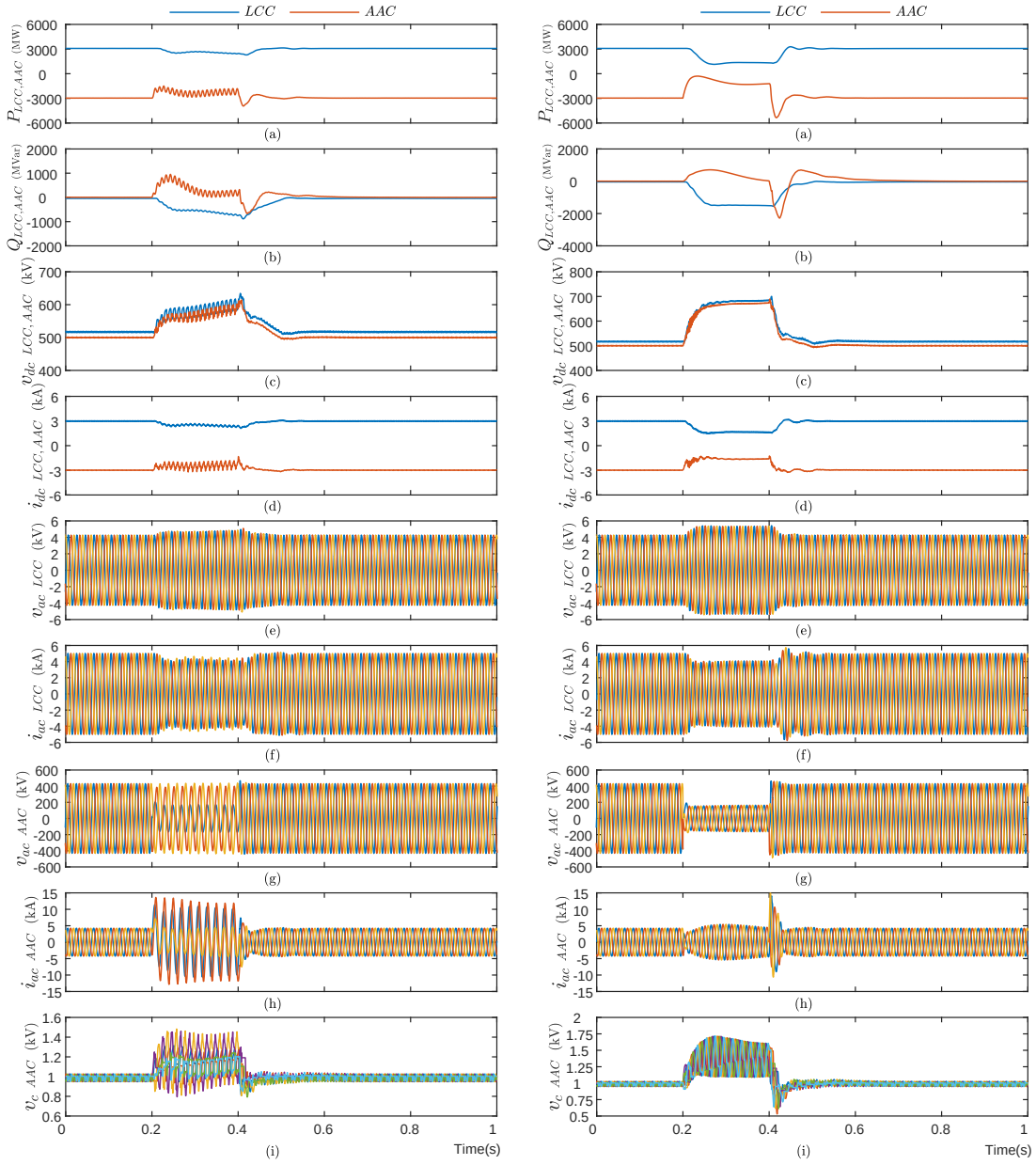
(1) Single-line to ground fault at the AC-grid of the LCC.

(2) Three-phase short circuit fault at the AC-grid of the LCC.

FIGURE 5.15: Single-line to ground and short-circuit faults at the AC-grid of the LCC in the LCC and AAC-based hybrid PTP HVDC transimission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC grid voltage of LCC, (f) AC grid current of LCC, (g) AC grid current of AAC and (h) SM capacitor voltage of AAC.

5.5.4 Permanent Pole-to-Pole DC Fault

The LCC can block DC fault current by increasing its firing angle to above 90°, switching to inverter operation mode. The AAC is capable of clearing DC faults without AC and DC-breakers via converter blocking. Thus, the developed LCC-AAC hybrid system can achieve



(1) Single-line to ground fault at the AC-grid of the AAC.

(2) Three-phase short circuit fault at the AC-grid of the AAC.

FIGURE 5.16: Single-line to ground and short-circuit faults at the AC-grid of the AAC in the LCC and AAC-based hybrid PTP HVDC transimission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC grid voltage of LCC, (f) AC grid current of LCC, (g) AC grid voltage of AAC, (h) AC grid current of AAC and (i) SM capacitor voltage of AAC.

DC fault self-clearance capability. For comparison, this part also shows the result of DC fault handling capability in the hybrid HVDC system based on the LCC and the HB-MMC.

A pole-to-pole permanent DC fault at the midpoint of the line occurs at 0.2s with

resistor of 10 Ω as shown in Fig. 5.17. When the DC fault is detected, the firing angle in the LCC side increases to maximum value (150°) forcing the LCC to inverter operation (Fig. 5.17(f)). The AAC converter is blocked after 4 ms. The active and reactive power changes are shown in Fig. 5.17(a)-(b). The active power of both the LCC and AAC stations drops to 0 after blocking converter. The reactive power is constant during the fault in the AAC station, while the increase of reactive power in the LCC station increases is due to the presence of AC filters. Oscillations in the DC voltages during DC fault caused by the discharge of the DC capacitances and inductances, as shown in Fig. 5.17(c). In addition, the DC current in the LCC station increases to 7 kA at the moment of DC fault, while the DC fault current at point A of Fig. 5.3 in the AAC station increases to 5 times the nominal value and presents obvious oscillation due to the discharging of DC capacitor (Fig. 5.17(d)). Although the fault current to the converter of the AAC (point B in Fig. 5.3) increases to about 8 kA when DC fault occuring, it rapidly decreases to zero after converter blocking (Fig. 5.17(e)). The capacitor voltages of the AAC first discharge to the DC-link when DC fault occuring, then increase after converter blocking to partially absorb energy from the DC-link and AC system (Fig. 5.17(h)).

Fig. 5.18 shows the results of the HB-MMC replacing the AAC in hybrid HVDC system. The MMC with HB-SMs does not posssess the DC fault self-clearing capability, hence it is necessary to open AC-grid breakers after converter blocking. In the hybrid HVDC system based on the LCC and the HB-MMC, the tripping signals of AC-breaker are triggered together with the converter blocking (after a delay of 4 ms) and within 10 ms all the AC breakers open, then the fault current of the MMC side will gradually decrease from 14 kA to 0, and the decay time is about 50 ms (Fig. 5.18(b)). The oscillation of DC voltage in the DC-link of the MMC is less than the AAC due to the absence of DC filter (Fig. 5.18(a)). The SM capacitors of the HB-MMC discharge first when DC fault occurring, but the SM capacitor voltages of the HB-MMC keep constant after converter blocking (Fig. 5.18(e)). In general, the results demonstrate the DC fault handling capability of the developed hybrid LCC-AAC HVDC transmission system, and the AAC in hybrid HVDC system offers improved performance than the HB-MMC.

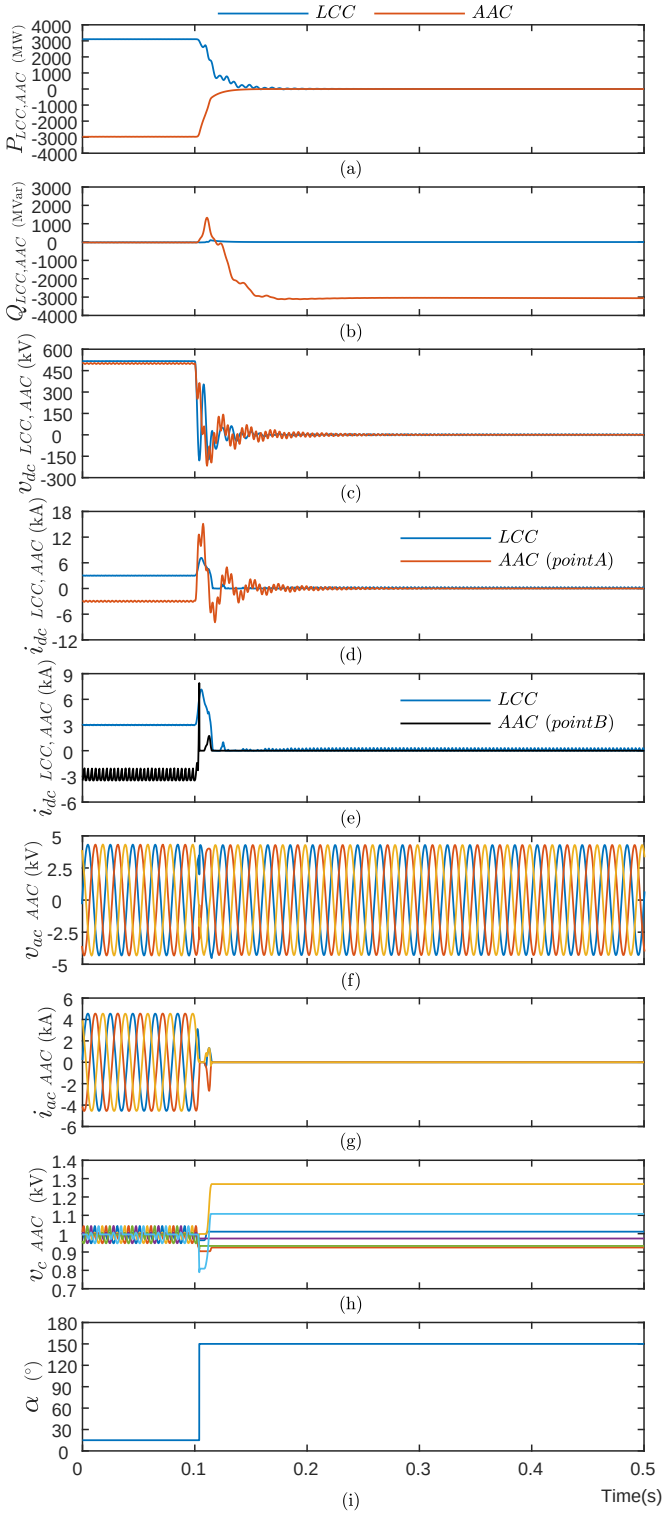


FIGURE 5.17: DC fault at the midpoint of the line in the hybrid PTP HVDC transmission system based on the LCC and the AAC: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current of LCC and AAC at point A, (e) DC current of LCC and AAC at point B, (f) AC grid voltage of AAC, (g) AC grid current of AAC, (h) SM capacitor voltage of AAC and (i) Firing angle of LCC.

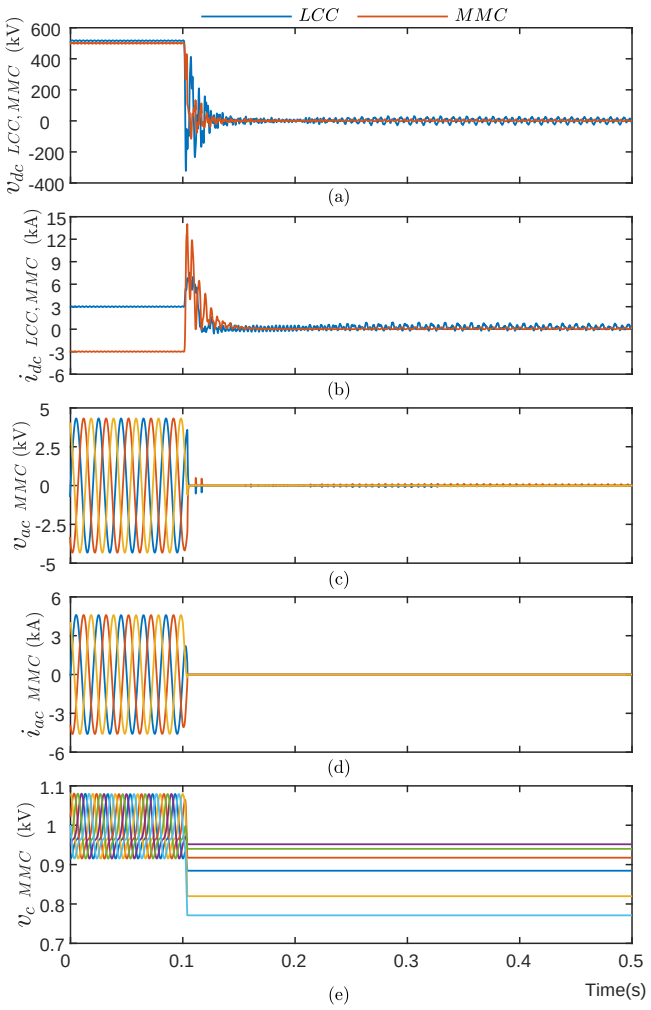


FIGURE 5.18: DC fault at the midpoint of the line in the hybrid PTP HVDC transmission system based on the LCC and the HB-MMC: (a) DC voltage, (b) DC current, (c) AC grid voltage of HB-MMC, (d) AC grid current of HB-MMC and (e) SM capacitor voltage of HB-MMC.

5.6 Conclusion

This chapter develops a hybrid PTP HVDC transmission system based on the combination of an LCC and an AAC converter as the system rectifier and inverter stations, respectively. Firstly, the employed converters and control hierarchy are described for the hybrid PTP HVDC transmission system. Also, the topology of the developed system is introduced with proposed control schemes under normal/fault operations. Finally, through analytical selection of the system parameters and considering various system operating conditions, verification and validation of the performance of the hybrid LCC-AAC system considering widely accepted HVDC operating standards is performed.

The detailed set of results demonstrate that the hybrid HVDC system operate under acceptable harmonic levels and within DC voltage & current ripple limits. Moreover, the system performance under various transient conditions demonstrate the robust operation including power reference tracking, AC and DC fault ride through capabilites, while ensuring prompt energy regulation and SM capacitor voltage balancing of the AAC. The results of DC fault also verify the AAC in hybrid HVDC system shows preferable DC fault handling capability compared with the HB-MMC. Development of the LCC and AAC-based hybrid PTP HVDC transmission system complements to the research and development of more complex hybrid HVDC systems combining the LCC and different modular VSCs.

Chapter 6

LCC and AAC-Based Hybrid MTDC Transmission System

6.1 Introduction

Challenges in long distance power transmission and large-scale integration of renewable energy systems drive the development of HVDC systems. Various hybrid HVDC systems can be configured as integrations of LCCs, VSCs by combining their benefits. Although each hybrid configuration poses its own challenges and requires specific control, the integration leads to unique benefits. Thus, it is necessary to explore the performance of different configurations, especially the more complex hybrid MTDC systems and future DC grids. This chapter develops the steps for integration of AACs in hybrid MTDCs and demonstrates the operation of AACs in a hybrid MTDC system. The detailed system structure and control hierarchy are developed. The performance of the hybrid MTDC system under multiple operating scenarios including AC and DC faults are demonstrated, verifying the feasibility of an LCC and AAC-based hybrid MTDC system.

6.2 Detailed System Description

6.2.1 System Topology

For further exploring the performance of the AAC in hybrid MTDC systems, the chapter develops a three-terminal hybrid HVDC system with one LCC station and two AAC stations. The detailed system topology of the hybrid MTDC system is shown in Fig. 6.1, and Fig. 6.2 describes the system control structure. The voltage level is selected as $\pm$500 kV, the power

ratings for the three stations are 2000 MVA, 800 MVA and 1200 MVA, respectively, and the detailed system parameters are shown in Table 6.1. Both AACs in the inverter side adopt P/V droop control and reactive power control while the LCC controls the DC current. The basic comparison of the required number of devices in hybrid MTDC system under the same voltage level with the LCC and different modular VSCs (HB-MMCs, FB-MMCs, clamped-double (CD)-MMCs and AACs) is provided in Table 6.2. In addition, the required number of devices for the configuration of LCC with MMC (hybrid SMs) is between the configuration of the LCC with HB-MMCs and with FB-MMCs. The following sections will

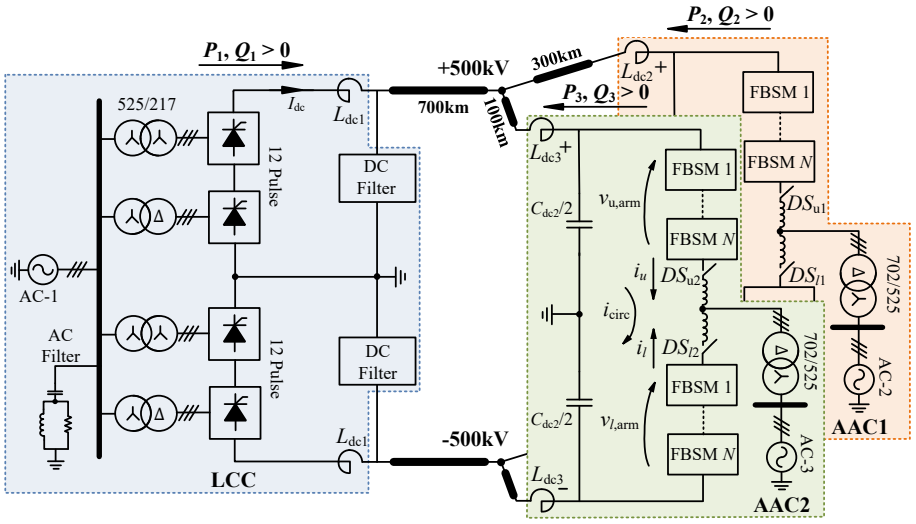


FIGURE 6.1: Configuration of the LCC and AAC-based hybrid MTDC transmission system.

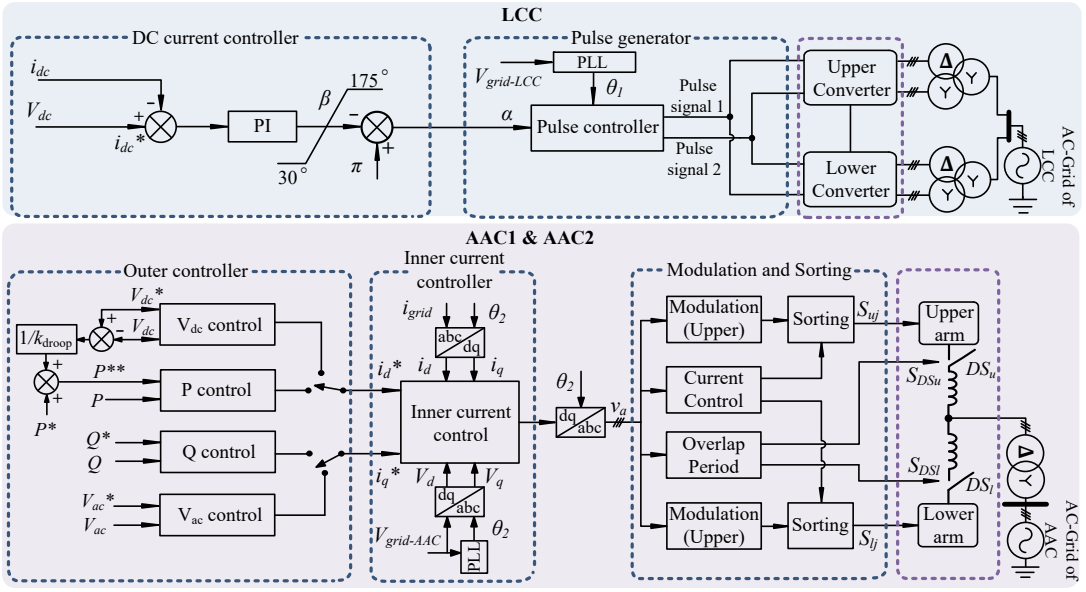


FIGURE 6.2: Control structure of the LCC and AAC-based hybrid MTDC transmission system.

discuss the detailed parameter selection for the LCC and AACs-based hybrid MTDC system.

TABLE 6.1: Parameters of the LCC and AAC-based hybrid MTDC transmission system.

Parameter	**LCC**	**AAC1 (AAC2)**
Rated Power (MVA)	2000	800 (1200)
Nominal Frequency (Hz)	50	50
DC Voltage (kV)	$\pm$500	$\pm$500
AC Voltage (L-L rms) (kV)	525	525
R/X Ratio	0.1	0.1
Transf. Ratio	525/217	525/702
Transf. Leakage Inductance (p.u.)	0.18	0.18
Transf. Resistance (p.u.)	0	0.006
Number of SMs per arm	-	640
Nominal SM Voltage (kV)	-	1
Stored Energy (kJ/MVA)	-	11
SM Capacitance (mF)	-	4.6 (6.9)
Arm Inductance (p.u.)	-	0.02
Nominal Operating Point (m_a)	-	1.15
DC Inductance (mH)	250	30 (25)
DC Capacitance (μF)	-	90 (60)

TABLE 6.2: Comparison of main modular VSCs in hybrid MTDC systems.

Parameters	**LCC-MMCs (HBSM)**	**LCC-MMCs (FBSM)**	**LCC-MMCs (CDSM)**	**LCC-AACs (FBSM)**
DC Voltage Level (kV)	$\pm$500	$\pm$500	$\pm$500	$\pm$500
Operaing Point (m_a)	0.9	0.9	0.9	1.27 (4/π)
Number of SMs (per arm)	900	900	450	640
Number of IGBTs (per arm)	1800	3600	2250	2560 (SMs) + 500 (DSs)
Number of Diodes (per arm)	1800	3600	3150	2560 (SMs) + 500 (DSs)
Number of Capacitors (per arm)	900	900	900	640
Energy Requirement of SMs (kJ/MVA)	30$\sim$40	30$\sim$40	30$\sim$40	11
Requirement of DC-Link Filters	LCC	LCC	LCC	LCC + AACs*

* EO-AAC can provide active filtering for DC-link.

6.2.2 System Parameter Selection

6.2.2.1 DC Output Voltage of the LCC

The value of DC output voltage in the LCC can be calculated as (6.1). This is mainly determined by the firing angle (α) and the secondary side voltage of transformer (V_{2t}), while the influence of leakage inductance (L_l) in transformer has to be considered as well.

$$V_{dcr} = kNV_{2t}\cos(\alpha) - \frac{3N\omega L_l}{\pi} I_{dcr}, \tag{6.1}$$

where k is $3\sqrt{2}/\pi$ for a 6-pulse thyristor bridge, N represents the number of 6-pulse converters ($N = 2$ in 12-pulse converter) and I_{dcr} the DC-link current of the LCC.

6.2.2.2 Power Calculation of the LCC

The power (P_{dcr}, Q_{dcr}) of DC-link and related power factor (ϕ) can be expressed as:

$$\begin{cases} P_{dcr} = V_{dcr} I_{dcr}, \\ Q_{dcr} = P_{dcr}\tan(\phi), \end{cases} \tag{6.2}$$

$$\phi = \cos^{-1}\Big(\frac{\cos(\alpha) + \cos(\alpha + \mu)}{2}\Big), \tag{6.3}$$

where μ represents the commutation overlap angle.

6.2.2.3 Operating Point and Overlap Period of the AAC

Considering the $\pm 10\%$ voltage variation under normal operation, the operating point of both AACs adopted in the hybrid system is expressed as:

$$m_{a,AACx} = \frac{M_a}{k_a} = 1.157, \tag{6.4}$$

where $x = 1, 2$ and $k_a = 1.1$. Additionally, the short-overlap period is adopted in both AACs and can be calculated as:

$$\hat{t}_{ov,AACx} = \frac{\pi - 2\cos^{-1}(1 - m_{a,AACx})}{\omega}. \tag{6.5}$$

6.2.2.4 Number of SMs and Switching Devices of the AAC

The required number of SMs per arm and the switching devices per DS can be derived from:

$$\begin{cases} N_{SM,AACx} = \dfrac{\hat{V}_{ac,AACx}}{V_{c,AACx}}, \\ N_{DS,AACx} = \dfrac{\hat{V}_{DS,AACx}}{V_{c,AACx}} = \dfrac{N_{SM}}{M_a}, \end{cases} \tag{6.6}$$

where $\hat{V}_{ac,AACx}$ and and $V_{c,AACx}$ represent the peak ac output voltage and the nominal SM capacitor voltage of both AACs, respectively.

6.2.2.5 SM Capacitance of the AAC

The SM capacitance of borh AACs follows the calculation in CIGRE benchmark model of MMC-HVDC [101], as:

$$C_{AACx} = \frac{S_{AACx} E_{AACx}}{3 N_{SM,AACx} V_{c,AACx}^2}, \tag{6.7}$$

where S_{AACx} is the rated power of both AACs and E_{AACx} is the required energy storage for AAC1 and AAC2.

6.2.2.6 Filters and DC Transmission Line

Based on the previous discussion of filters in Chapter 3.2.3 and Chapter 5.4.4. The AC filters of the LCC in the hybrid MTDC system adopt the combination of double-tuned damped filter and shunt capacitor for filtering $12k\pm1$ and low order harmonics, while the tuning points are set at 12/24 and 6/30 for DC filters [128]. The smoothing reactance in the LCC side can play the role of smoothing ripples of DC current. In addition, the smoothing reactance is also significant for both AACs which can be coordinated with DC capacitance for smoothing the 6-pulse ripple. The DC-link inductance and capacitance for the AAC can follow the top equation of (6.8). Moreover, considering the energy exchange between AC and DC, the energy storage of DC capacitor can be calculated as $C_{dc}V_{dc}^2/2 = S\Delta E_{AAC} E_{AAC}/3$ [200], then the required capacitance value at the DC-link can follow (6.8) .

$$\begin{cases} \dfrac{L_{dcx} C_{dcx}}{2} > \dfrac{1}{\omega_c^2}, \\ C_{dcx} > \dfrac{2 S k_e E_{AACx}}{3 V_{dc}^2}, \end{cases} \tag{6.8}$$

where ω_c is the cut-off frequency of DC-link filters in both AACs, $k_e \in (0.9, 1.1)$ that is the energy deviation of SMs. The parameters of DC inductance and capacitance for the LCC and AACs are shown in Table 6.1.

An overhead line (OHL) is employed in the hybrid MTDC system and the equivalent lumped parameters of the OHL are shown in Table 6.3. Besides, Table 6.4 lists the related control parameters of the LCC and AACs.

TABLE 6.3: Parameters of DC transmission line in the LCC and AAC-based hybrid MTDC transmission system.

Parameters of Transmission Line (Overhead Line) [101, 203]	
DC Line Voltage (kV)	$\pm$500
Length (LCC/AAC1/AAC2) (km)	700/300/100
Resistance (Ω/km)	0.0127
Inductance (mH/km)	0.88
Capacitance (μF/km)	0.013

TABLE 6.4: Control parameters in the LCC and AAC-based hybrid MTDC transmission system.

Control Parameters	
DC Current Control - LCC	$K_P = 0.3, K_I = 80$
Active/Reactive power control - AACs	$K_P = 1.3, K_I = 33$
Droop Constant - AACs	$k_{droop} = 0.2$
Energy Balancing - AACs [30]	$K_P = 2.9, K_I = 75$
PLL - LCC	$K_P = 5, K_I = 10$
PLL - AACs	$K_P = 0.084, K_I = 4.69$

6.3 P/V Droop Control and DC Fault-Ride-Through (FRT) Scheme

6.3.1 P/V Droop Control

The conventional P/V droop control is adopted in the hybrid MTDC system. The control of DC voltage is shared by AAC1 and AAC2 with P/V droop control because the DC voltage is determined by the power variation in both AACs via actual droop charateristic. The droop control can be considered as an extension of constant power or DC voltage control, which can improve the system reliability and reduce the telecommunication dependence among the three converters as well. The expresssion of droop control follows (6.9), and the droop constant is defined as (6.10) where R is the slope of droop characteristic curve.

The station will run in constant power control or DC voltage control if $k_p = 1, k_u = 0$ or $k_p = 0, k_u = 1$, respectively. The droop constant in both AAC terminals is set as 0.2 [101].

$$\text{error} = k_p(P^* - P) + k_u(V_{dc}^* - V_{dc}) \tag{6.9}$$

$$k_{droop} = |R| = \frac{k_p}{k_u} \tag{6.10}$$

6.3.2 DC FRT Scheme

The LCC and AACs-based hybrid MTDC system has capability for riding through DC fault, and Fig. 6.3 shows the potential pole to pole fault current path and the proposed DC fault ride through scheme for the hybrid MTDC system.

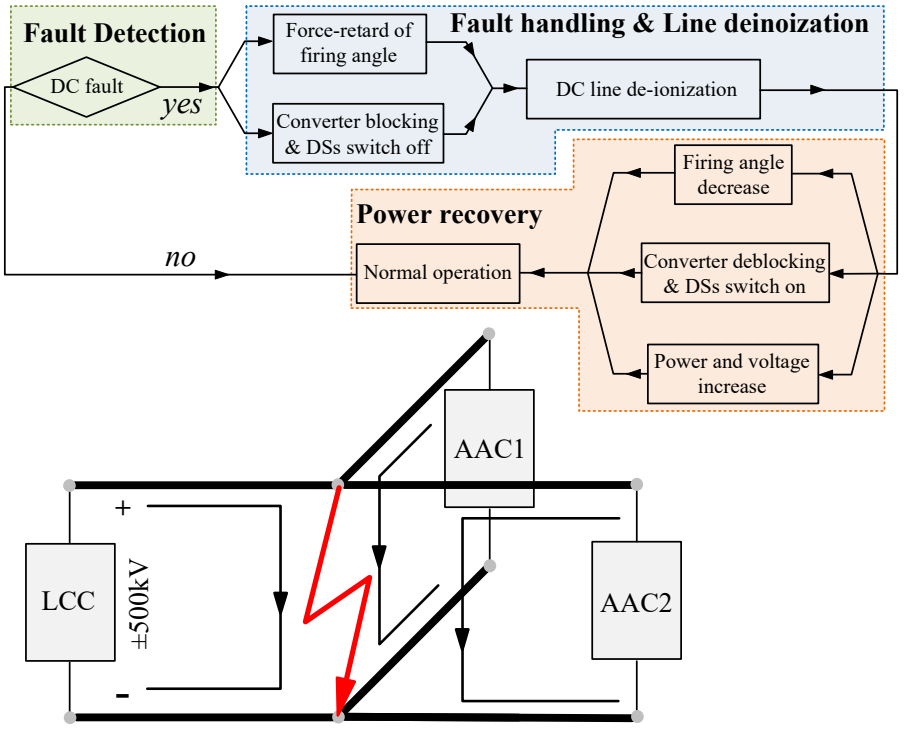


FIGURE 6.3: DC fault ride through scheme in the LCC and AAC-based hybrid MTDC transmission system.

When the DC fault signal reaches the three converters, the LCC in the rectifier side reverts to the inverter operating mode via firing angle force retard, all SMs in both AACs are blocked and DSs are switched off at the same time. The fault is detected via monitoring the line current difference in three converters [204, 205], and the detection time is set as 0.5 ms in this hybrid HVDC system. After the line deionization, the both AACs are first de-blocked, then power and voltage references are ramped to pre-fault values. In addition, the LCC will switch into constant DC current control when the firing angle decreases to

around the steady-state value, at which point the system will recover from DC fault. It is noteworthy that it is not necessary to open the AC breakers for LCC and both AACs, since the fault current path can be blocked by the thyristors of the LCC, and both AACs can block the fault current from AC side to DC-link. The related results are shown in Chapter 6.4.4.

6.4 Simulation Results

The results of four operating scenarios are presented including i) the steady-state operation, ii) power adjustment of the LCC, iii) active power reference change of the AAC, and iv) reactive power reference change of the AAC. Besides, this section will also discuss the system performance under AC faults at both rectifier side (LCC) and inverter side (AAC1) as well as DC fault ride through capability. The detailed set of results verify the functionalities of the hybrid MTDC system and validate the system performance complying with widely accepted HVDC operating standards.

6.4.1 Steady-State Operation

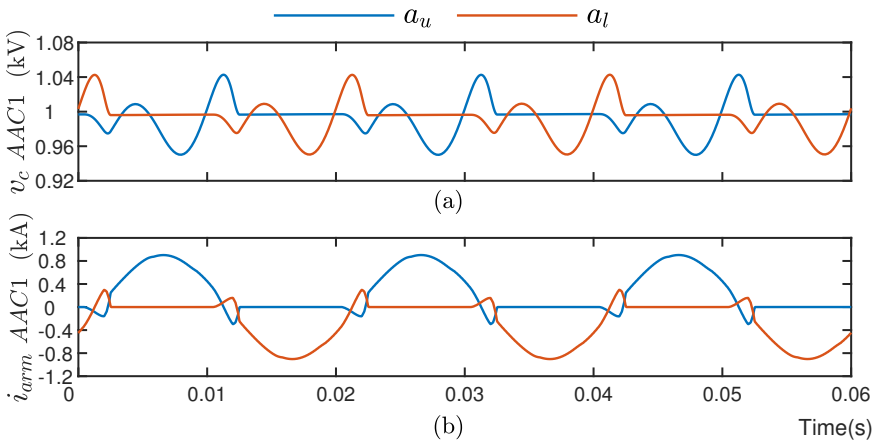


FIGURE 6.4: Capacitor voltage and arm current of AAC1 in the LCC and AAC-based hybrid MTDC transmission system: (a) capacitor voltage and arm current of AAC1 and (b) capacitor voltage and arm current of AAC1.

In steady state, the LCC in rectifier side regulates the DC current (2 kA) and both AACs that operate at the predefined operating point (M_a = 1.157) sharing the control of DC voltage via P/V droop control. The ripples of DC voltages and currents are limited within 5% with the appropriate selection of DC-link filters. In addition, the AC voltages and currents of three terminals also comply with network operating standards, limiting the THDs below 2% [202]. The results of DC voltages and active power flow under initial

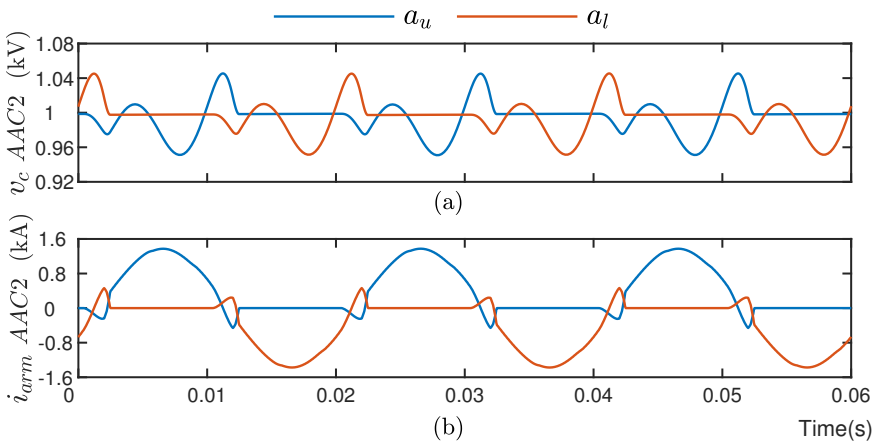


FIGURE 6.5: Capacitor voltage and arm current of AAC2 in the LCC and AAC-based hybrid MTDC transmission system: (a) capacitor voltage and arm current of AAC2 and (b) capacitor voltage and arm current of AAC2.

steady-state operation in the hybrid MTDC system are given in the operating scenario 1 of Table 6.5. The capacitor voltage and arm current of both AACs in phase a are respectively shown in Fig. 6.4 and Fig. 6.5. In addition, the capacitor voltages are contained within the designed $\pm$10% range where applicable.

It is noteworthy that the waveforms of arm currents and capacitor voltages are different from an MMC due to the arm current interruption in one phase-leg.

TABLE 6.5: DC Voltages and active power flow for the LCC and AAC-based hybrid MTDC transmission system.

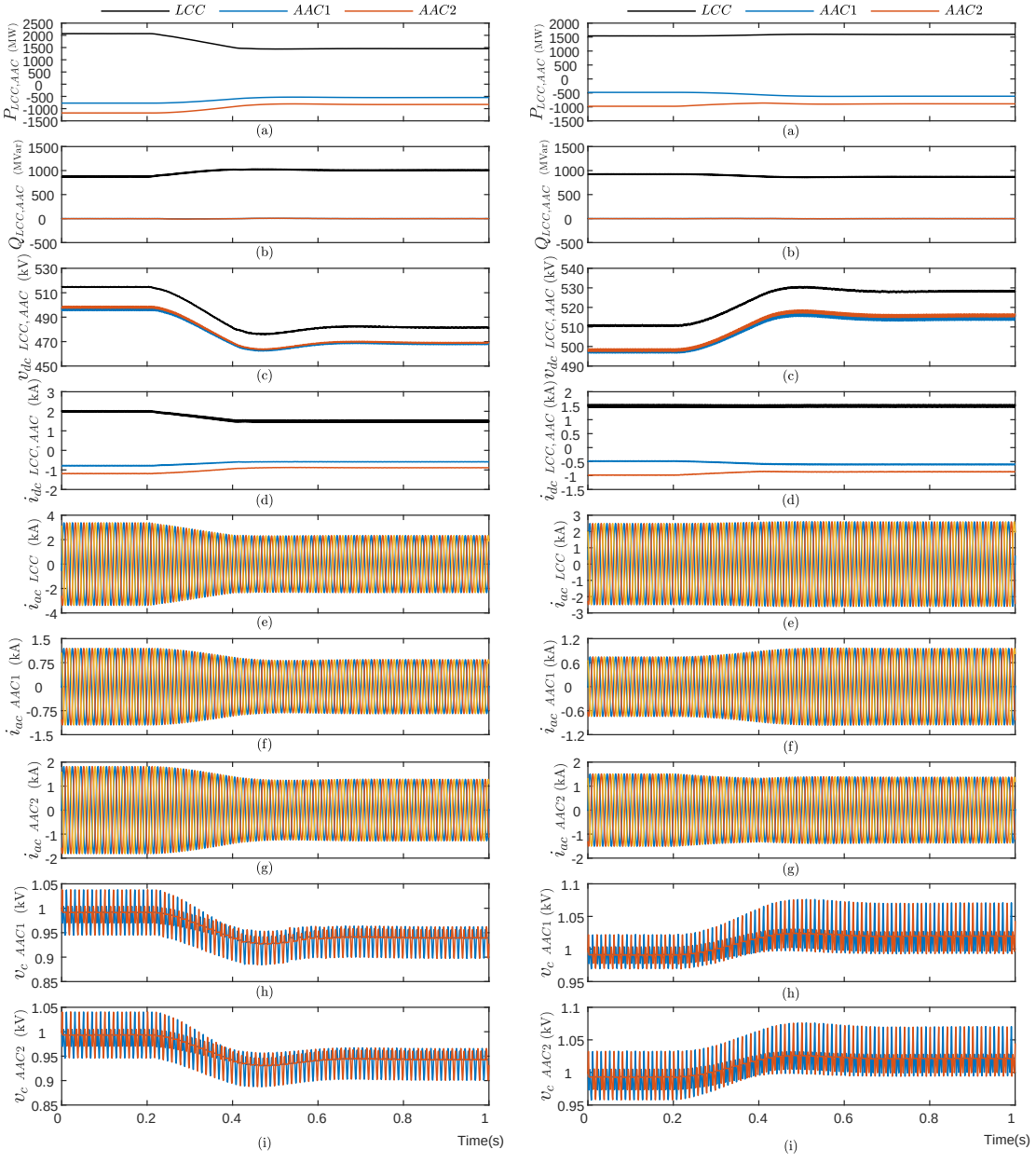
Parameter	**Scenario 1**	**Scenario 2**	**Scenario 3**
$V_{dc,LCC}$ (p.u.)	1.029	0.963	1.061
$V_{dc,AAC1}$ (p.u.)	0.994	0.936	1.033
$V_{dc,AAC2}$ (p.u.)	0.996	0.938	1.036
$P_{ac,LCC}$ (MW)	2069.13	1455.06	1599.62
$P_{ac,AAC1}$ (MW)	$-$773.87	$-$544.79	$-$633.07
$P_{ac,AAC2}$ (MW)	$-$1177.09	$-$829.19	$-$913.36

6.4.2 Reference Tracking

6.4.2.1 Power Adjustment of the LCC

Fig. 6.6(1) shows the results of scenario 2 (power adjustment of the LCC). The DC current reference of the LCC is changed from 1.0 p.u. to 0.75 p.u. at 0.2s (Fig. 6.6(1) (d)). The results of power and DC voltage are shown in Fig. 6.6(1) (a)-(c), respectively. In

addition, the corresponding voltages and active power flow are listed in Table 6.5. The DC voltages of all three terminals drop by approximately 6% relative to the steady-state values, and the active powers amongst the three terminals are adjusted based on the droop characteristic and DC current reference change. Moreover, the reactive powers of



(1) Power adjustment of the LCC. (2) Active power reference change of AAC2.

FIGURE 6.6: Power adjustment of the LCC and active power reference change of AAC2 in the LCC and AAC-based hybrid MTDC transmission system: (a) active power, (b) DC voltage, (c) reactive power (d) DC current, (e) AC-grid current of LCC, (f) AC-grid current of AAC1, (g) AC-grid current of AAC2, (h) capacitor voltage of AAC1 and (i) capacitor voltage of AAC2.

both AACs keep constant due to the independent reactive power control of the AAC. The reactive power consumption of the LCC deviates with the change of active power and firing angle following with (6.2) and (6.3), which can also explain the reactive power change of the LCC in the following two scenarios.

The AC grid current change of three terminals is shown in Fig. 6.6(1) (e)-(g), which coincides with the decrease of active power. In addition, the average values of capacitor voltage in Fig. 6.6(1) (h)-(i) slightly deviate with the change of DC voltage, while the ripple of SM capacitor voltage declines with the power adjustment of the LCC.

6.4.2.2 Active Power Reference Change of AAC2

The initial DC current is 1.5 kA, regulated by the LCC, and the active power references in the both AACs are 500 MW and 1000 MW, respectively in scenario 3. At 0.2s, the active power reference of AAC2 is changed from 1.0 p.u. to 0.7 p.u (Fig. 6.6(2) (a)). The final steady state operating piont is determined by the droop controller in the both AAC terminals. Table 6.5 and Fig. 6.6(2) (a) show that the final active power of AAC2 is 0.91 p.u, which is caused by the compensation of DC voltage variation (Fig. 6.6(2) (c)). In addition, the DC current in AAC1 and AAC2 follow the change of active power (Fig. 6.6(2) (d)). The change of AC grid currents in the three terminals is shown in Fig. 6.6(2) (e)-(g), respectively. Besides, Fig. 6.6(2) (h)-(i) show that the ripple of SM capacitor voltages in both AACs slightly increases during the change of active power reference.

6.4.2.3 Reactive Power Reference Change of both AACs

Both AACs can independently control reactive power at individual station. In scenario 4, the reactive power reference of AAC1 and AAC2 is changed from 0 p.u. to -0.5 p.u. at 0.2s and 0 p.u. to 0.5 p.u. at 0.5s, respectively. The related results in Fig. 6.7 show the reactive power control capability of both AACs without interfering the LCC station. The AC grid currents of both AACs deviate slightly in the process (Fig. 6.7(f)-(g)), while with larger ripple in SM capacitor voltages (Fig. 6.7(h)-(i)).

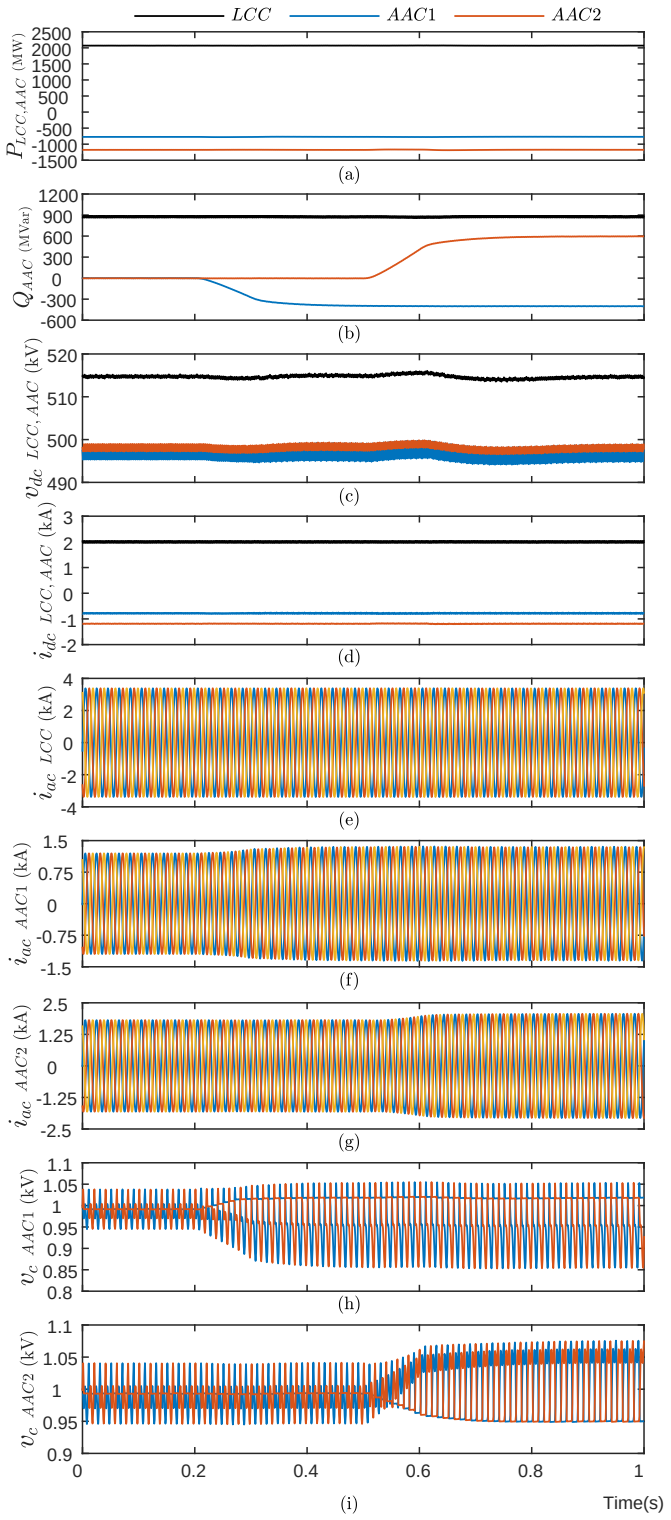


FIGURE 6.7: Reactive power reference change of both AACs in the LCC and AAC-based hybrid MTDC transmission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC-grid current of LCC, (f) AC-grid current of AAC1, (g) AC-grid current of AAC2, (h) capacitor voltage of AAC1 and (i) capacitor voltage of AAC2.

6.4.3 System Performance under AC Faults

This part discusses the AC FRT capability of the LCC and AAC-based hybrid MTDC system verifying the robustness of such system. A 200ms single-line to ground (SLG) fault and three-phase short circuit fault are set at both rectifier and inverter side, and the controller of AAC2 is identical with AAC1, thus the AC faults at inverter side are only set at AAC1. In addition, the fault resistance is 0.01 Ω which can represent the worst AC faults case.

6.4.3.1 AC Faults at Rectifier Side (LCC)

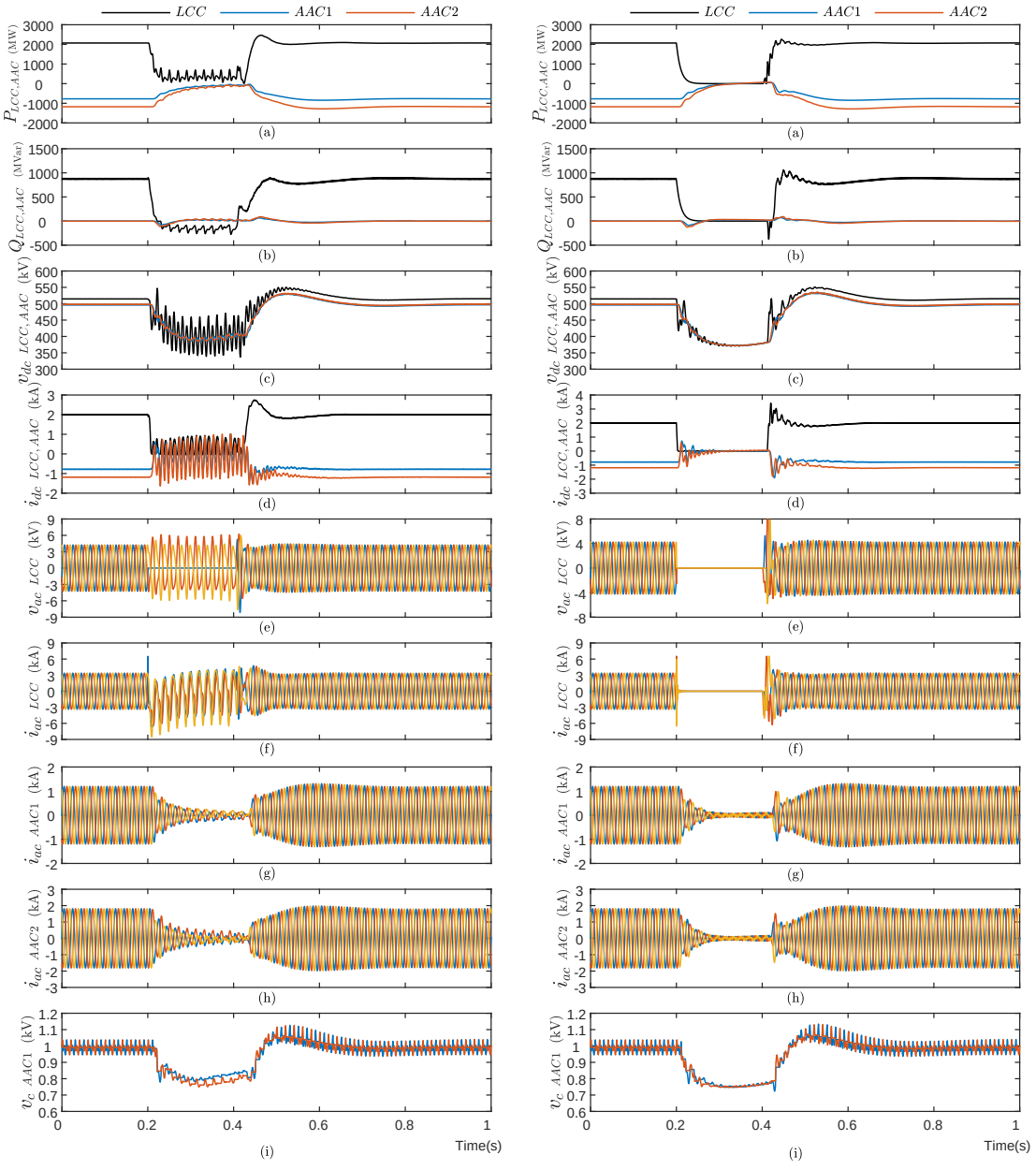
Both the SLG and three-phase short circuit faults of the LCC are set at 0.2s shown in Fig. 6.8(1) and Fig. 6.8(2), respectively. During a SLG fault of the LCC, there is still redundant power for the whole system (Fig. 6.8(1) (a)), while the power transmissin is interrupted during a three-phase short circuit fault at the LCC side (Fig. 6.8(2) (a)), which are caused by DC current decrease at the LCC side (Fig. 6.8(1) (d) and Fig. 6.8(2) (d)). The reactive power oscillations of three terminals during SLG and three-phase short circuit fault are respectively shown in Fig. 6.8(1) (b) and Fig. 6.8(2) (b).

In addition, the DC voltages drop by about 0.2 p.u. (Fig. 6.8(1) (c)) and 0.25 p.u. (Fig. 6.8(2) (c)), for SLG fault and three-phase short circuit fault, respectively. Accordingly, the capacitor voltages of both AACs experience the same drop with DC voltages (Fig. 6.8(1) (i) and Fig. 6.8(2) (i)). In general, the performance of AAC1 and AAC2 is similar under AC faults of the LCC, and the AC grid currents of two stations are respectively shown in Fig. 6.8(1) (g), (h) and Fig. 6.8(2) (g), (h). The system can recover from AC faults of the LCC side within 300ms that presents the reliable AC FRT capability of sending terminal in the hybrid MTDC system.

6.4.3.2 AC Faults at Inverter Side (AAC1)

As shown in Fig. 6.9(1) and Fig. 6.9(2), the AC faults occuring at AAC1 at 0.2s lead to the DC voltage increase by approximately 0.08 p.u. (Fig. 6.9(1) (c)) and 0.15 p.u. (Fig. 6.9(2) (c)) for SLG fault and three-phase short circuit fault, respectively. Accordingly, the SM capacitor voltage of AAC1 under such two types of faults respectively increase about by 0.3 p.u. (Fig. 6.9(1) (i)) and 0.5 p.u. (Fig. 6.9(2) (i)). It is noteworthy that the deviation of SM capacitor voltage in AAC2, whether under SLG fault or three-phase short circuit fault, is less than such in AAC1 which is within 0.13 p.u. (Fig. 6.9(1) (j)) and 0.26 p.u. (Fig. 6.9(2) (j)), respectively.

The power oscillations of three terminals for two types of ac faults at AAC1 are respectively shown in Fig. 6.9(1) (a), (b) and Fig. 6.9(2) (a), (b). It can be found that the LCC side can maintain the power transmission capability since the DC current is controlled



(1) Single line to ground fault at the AC-grid of the LCC.

(2) Three-phase short-circuit fault at the AC-grid of the LCC.

FIGURE 6.8: Single line to ground and three-phase short-circuit faults of the LCC in the LCC and AAC-based hybrid MTDC transmission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC-grid voltage of LCC, (f) AC-grid current of LCC, (g) AC-grid current of AAC1, (h) AC-grid current of AAC2 and (i) capacitor voltage of AAC1.

by the LCC while slightly drops with the increase of DC voltage. Moreover, there is no serious overcurrent occuring at AAC2 although the decline of DC current at AAC1 leads to the increase of DC current at AAC2 (Fig. 6.9(1) (d) and Fig. 6.9(2) (d)). Besides, the AC grid voltage of AAC1 and ac grid currents of three terminals are respectively shown in Fig. 6.9(1) (e)-(h) and Fig. 6.9(2) (e)-(h). The recovery time is also within 300 ms as AC faults at rectifier side, and the whole process verifies that the AAC as inverter in hybrid MTDC system can ride-through AC faults and the oscillation of current and voltage is within acceptable level.

6.4.4 Temporary Pole-to-Pole DC Fault

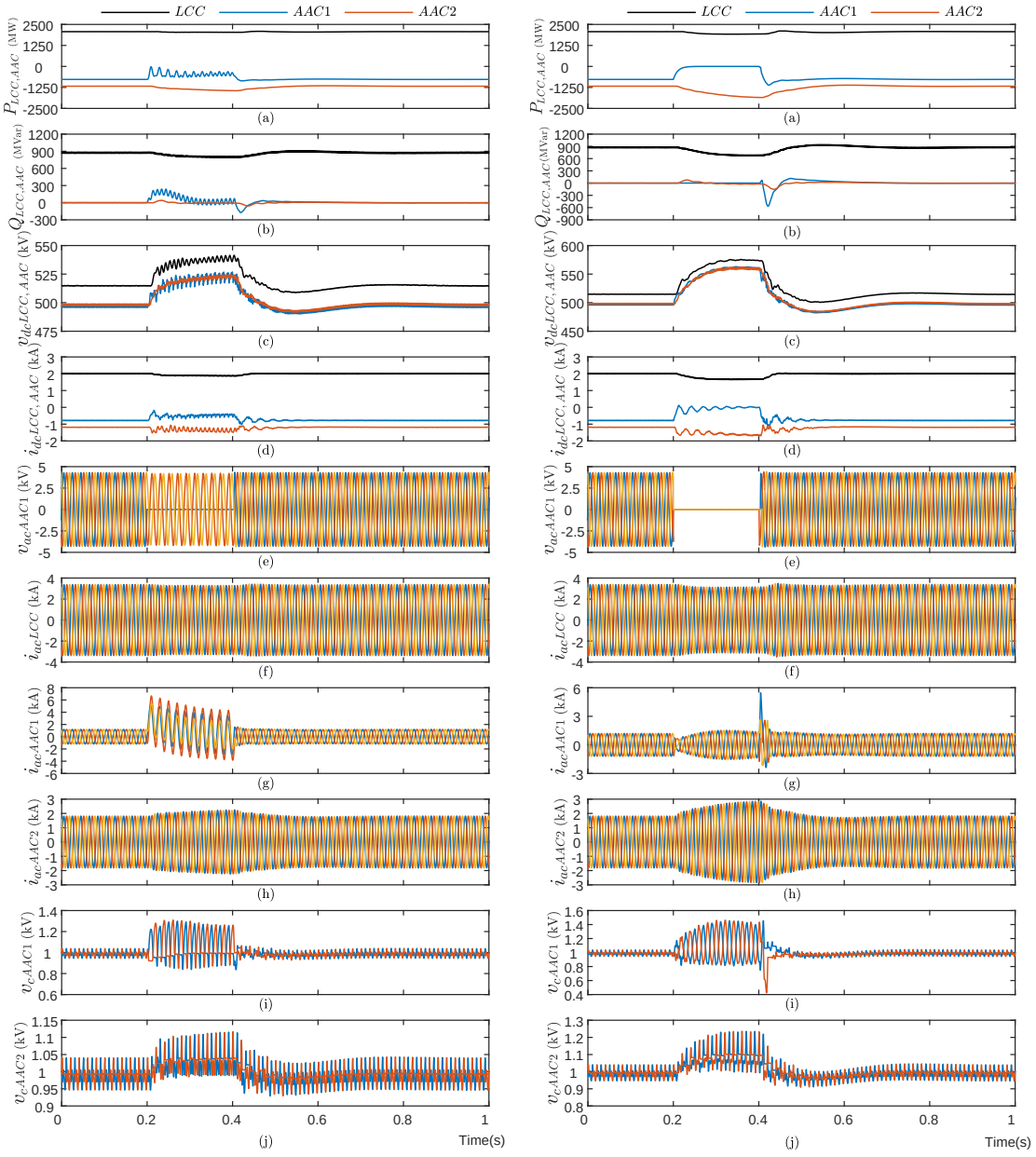
A temporary pole to pole DC fault via a 10 Ω resistor is set at 0.2 s, at the end of the first transmission line (700 km) and lasts for 0.1 s. After the DC fault clearing, the whole system recovers at 0.7 s with a 0.4 s line de-ionization [88].

In the hybrid MTDC system, the LCC in the rectifier side can ride through DC fault via firing angle force retard. When the DC fault occurs, the DC current in the LCC side first increases to a value of 4 kA in such hybrid system (Fig. 6.10(d)). After detecting the DC fault, the firing angle of the LCC is increased to 150° enabling the LCC to run in inverter operation, then the fault current path will be blocked by thyristors. The AC filters can provide reactive current to the AC grid of the LCC during DC fault (Fig. 6.10(g)).

The DC fault ride through scheme for the AAC is to force the fault current to zero by utilizing the series connnected capacitors in its bipolar SMs. The fault currents in the both AAC terminals will first increase following the fault current path (from positive pole to negative pole) as the SM capacitors and DC-link capacitors discharge and the fault current flows from AC side. The maximum fault currents for AAC1 and AAC2 are about 4 kA and 8 kA, respectively (Fig. 6.10(e) and (f)). For protecting the IGBTs in SMs, both converters of both AACs are blocked after 4 ms, then the fault currents in both AAC terminals will gradually decrease to zero. The oscillation of DC voltages in all three converters are due to the discharge of the DC-link capacitors and smoothing reactors (Fig. 6.10(c)). In addition, AAC is capable of blocking the fault current (Fig. 6.10(h), (i)), thus the AC breakers are not opened. Besides, the DSs in both AACs should be switched off during the DC fault for employing the antiparallel diodes in IGBTs of DSs to thoroughly cut off the fault current.

In recovery mode, both AACs first deblock and all DSs switch on. In addition, the power and voltage references for both AACs are gradually increased with a rate of 8 MW/ms for AAC1 (12 MW/ms for AAC2) and 40 kV/ms, respectively. At 0.7 s, the firing angle of the LCC is decreased to 20°, then the LCC switches to normal DC current control mode (Fig. 6.10(l)). After about 0.3 s, the whole system totally recovers from DC fault

(Fig. 6.10(a), (b)) with acceptable SM capacitor voltage deviation (0.3 p.u.) in both AACs (Fig. 6.10(j), (k)).



(1) Single line to ground fault at the AC-grid of AAC1. (2) Three-phase short-circuit fault at the AC-grid of AAC1.

FIGURE 6.9: Single line to ground and three-phase short-circuit faults of AAC1 in the LCC and AAC-based hybrid MTDC transmission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current, (e) AC-grid voltage of AAC1, (f) AC-grid current of LCC, (g) AC-grid current of AAC1, (h) AC-grid current of AAC2, (i) capacitor voltage of AAC1 and (j) capacitor voltage of AAC2.

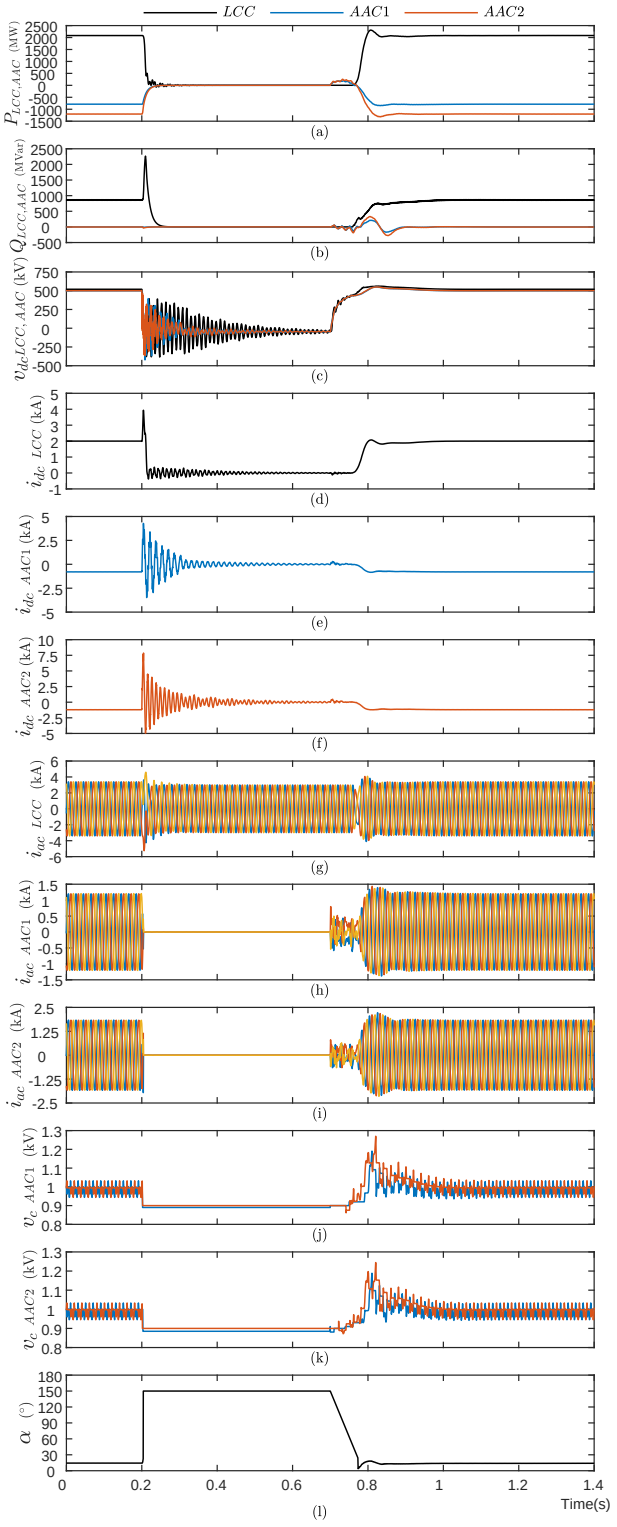


FIGURE 6.10: Pole to pole temporary DC fault in the LCC and AAC-based hybrid MTDC transmission system: (a) active power, (b) reactive power, (c) DC voltage, (d) DC current of the LCC, (e) DC current of AAC1, (f) DC current of AAC2, (g) AC-grid current of LCC, (h) AC-grid current of AAC1, (i) AC-grid current of AAC2, (j) capacitor voltage of AAC1, (k) capacitor voltage of AAC2 and (l) firing angle of LCC.

6.5 Conclusion

This chapter investigates a novel hybrid MTDC system topology combining one LCC station (two 12-pulse converters) and two AAC stations. The detailed system description is introduced first considering the system topology and parameter selection. P/V droop control is considered for both AACs and a DC FRT scheme is proposed for riding through temporary DC fault in the hybrid MTDC system. For verifying the operation of the hybrid MTDC system, simulation results are demonstrated including the steady-state operation, power adjustment of the LCC, active/reactive power reference change of the AAC, and AC/DC fault performance.

The results of four operating scenarios validate the feasibility of LCC-AAC hybrid MTDC system under P/V droop control. Moreover, the LCC-AAC hybrid MTDC system shows AC FRT capability whether SLG fault or three-phase short circuit fault at both LCC and AAC termimals, and satisfactory temporary DC fault handling performance. In general, the work of this chapter contributes to the further understanding of more complex mixed-converter DC networks in future research on DC-grids.

Chapter 7

Development of Hybrid Multi-Converter DC Grids

7.1 Introduction

Hybrid multi-converter DC grids are extended DC grids formed by combinations of different converter topologies such as the LCC, MMC, AAC and other various topologies. The stable and secure operation of such systems in steady-stage and transient conditions is critical for ensuring the robustness of hybrid multi-converter DC grids. This chapter investigates the AC and DC FRT capability and the generalized expression of DC power flow in a hybrid multi-converter DC grid consisting of LCCs, MMCs and AACs. Fault handling schemes of the LCC, MMC and AAC are combined, extended and coordinated to provide satisfactory transient response of the hybrid DC grid under both AC and DC faults. In order to ensure the static security of developed DC grid, this chapter uses the generalized expression of DC power flow described in Chapter 4 to derive the power flow after converter outage under mixed P/V and I/V droop control considering power limitation, based on the determined initial power flow for normal operation. Simulation results for steady-state and transient operation based on a detailed equivalent model verify the fault handling capability of the hybrid DC grid, and further validate the accuracy of the proposed DC power flow expression in Chapter 4.

7.2 Configuration of Hybrid Multi-Converter DC Grid

For exploring more complex DC grids combining multiple converters, a hybrid multi-converter DC grid is developed as Fig. 7.1 with DC voltage of $\pm$500 kV, which functions

as power delivery from remote generation zones (e.g. large-scale renewables) to load centers. In the hybrid DC grid, one 12-pulse LCC with power rating of 3000 MVA in the rectifier side, via a combination of OHL and cables, delivers power to both AACs and one MMC with power rating of 900 MVA, 1200 MVA and 1000 MVA, respectively. The detailed parameters of the DC transmission lines are given in Table 7.1.

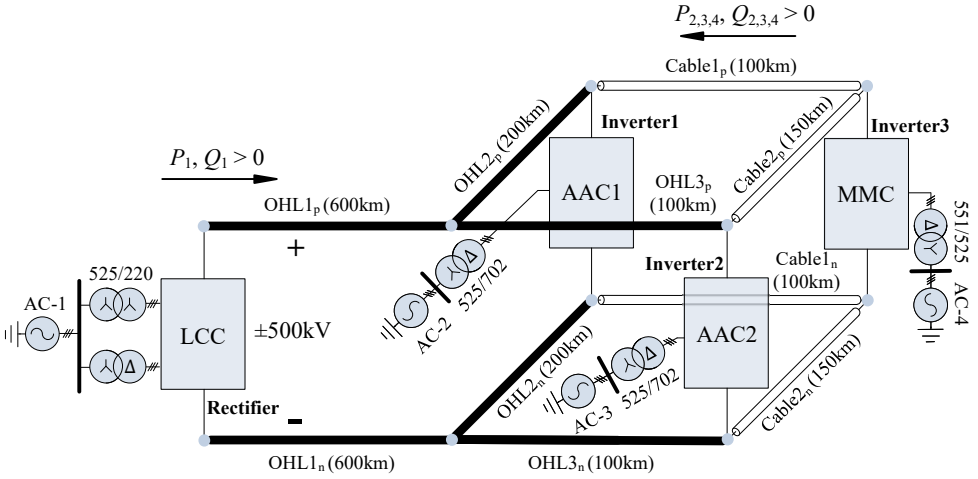


FIGURE 7.1: Topology of the hybrid multi-converter DC grid.

TABLE 7.1: Parameters of DC transmission lines in the hybrid multi-converter DC grid.

Parameters	**Line 1**	**Line 2**	**Line 3**	**Line 4**	**Line 5**
Type	OHL	OHL	OHL	Cable	Cable
Distance (km)	600	200	100	100	150
Resistance (Ω/km)	0.0127	0.0127	0.0127	0.011	0.011
Capacitance (μF/km)	0.013	0.013	0.013	0.2185	0.2185
Inductance (mH/km)	0.88	0.88	0.88	0.2615	0.2615

7.2.1 Description of the LCC

The basic high level control modes of an LCC are i) constant DC current or voltage control and ii) constant firing angle or extinction angle control. Other control modes for LCCs can be developed based on the basic control modes as described in Chapter 3.2.2, e.g. constant power, frequency and damping control. For LCCs in the inverter side, VDCOL is usually adopted for reducing the risk of commutation failures [128].

The LCC in the hybrid DC grid is located at rectifier side and operates with constant DC current control. The active and reactive power for LCC is $P_{dc_{LCC}} = V_{dc_{LCC}} I_{dc_{LCC}}$ and $Q_{LCC} = P_{dc_{LCC}} \tan\phi$ (ϕ is the power factor angle), respectively. The detailed parameters of LCC are shown in Table 7.2.

TABLE 7.2: Parameters of LCC in the hybrid multi-converter DC grid.

Parameter	**LCC**
Rated Power (MVA)	3000
DC Voltage (kV)	$\pm$500
AC Voltage (L-L rms) (kV)	525
Transformer Ratio	525/220

7.2.2 Description of the MMC and the AAC

MMCs and AACs all belong to the modular VSC family, thus high level control is similar while with different low level control. The system parameters of MMC and both AACs in the hybrid DC grid are shown in Table 7.3. For the high-level control, P/V or I/V droop control is adopted for three inverters, thus the DC voltage of the hybrid dc grid is balanced by MMC and both AACs. Moreover, the reactive power of MMC and both AACs is set as zero.

TABLE 7.3: Parameters of MMC and AACs in the hybrid multi-converter DC grid.

Parameter	**MMC**	**AAC1 (AAC2)**
Rated Power (MVA)	1000	900 (1200)
DC Voltage (kV)	$\pm$500	$\pm$500
AC Voltage (L-L rms) (kV)	525	525
Transformer Ratio	525/551	525/702
Number of SMs per arm	1000	640
Nominal SM Voltage (kV)	1	1
Arm Inductance (p.u.)	0.15	0.02
Nominal Operating Point (m_a)	0.9	1.15
DC Inductance (mH)	30	80 (75)
DC Capacitance (μF)	-	100 (110)

7.3 AC and DC Fault Handling Scheme

This section discusses the combined temporary AC and DC fault handling schemes in the hybrid multi-converter DC grid. Special emphasis is given on AC faults at inverter side,

since AC faults at the LCC (rectifier) side will lead to power interruption of the whole proposed system, similarly to [49, 50, 88].

7.3.1 AC Fault Handling Scheme

When temporary AC faults occur at either the MMC or AAC stations, the hybrid DC grid should be capable of riding through these AC faults. In the FRT scheme, the outer control loop is temporarily disabled in order to assist the response of the converter, due to the fast response of the inner current controller compared to the outer loop. The controller will be re-enabled when receiving the clearing signal of the AC faults. Fig. 7.2 shows the AC FRT control scheme when a temporary AC fault occurs at the MMC side of the hybrid DC grid.

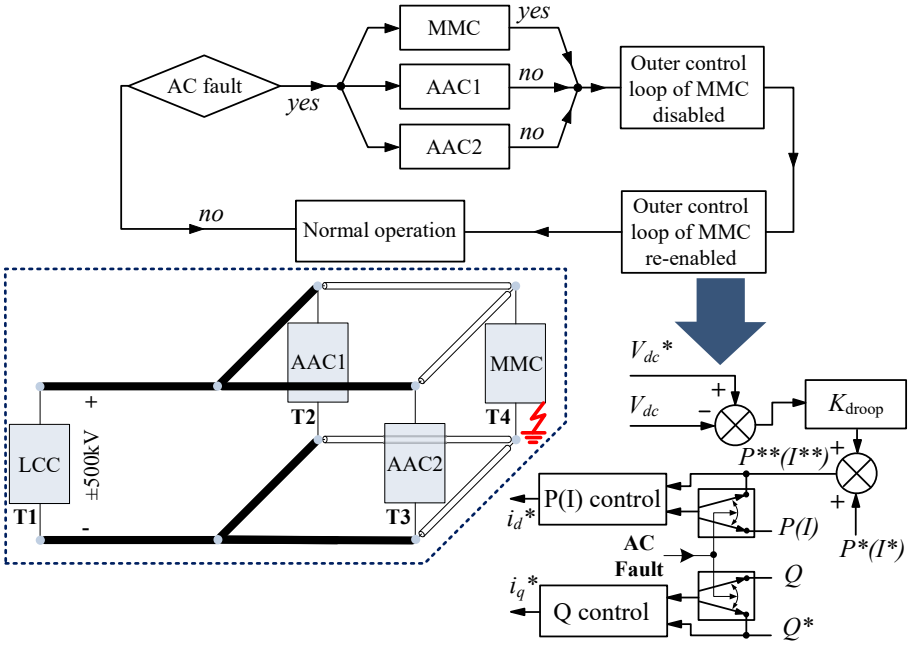


FIGURE 7.2: AC fault ride through scheme in the hybrid multi-converter DC grid.

7.3.2 DC Fault Handling Scheme

The hybrid multi-converter DC grid should also be capable of riding-through DC faults. When a DC fault is detected (Fig. 7.3), the firing angle of LCC is increased to above 90° reverting to inverter operating mode, the MMC and AACs are blocked and DSs in AACs are switched off at the same time. Also, the power (or current) and voltage references of MMC and AACs are decreased to zero. Besides, it is necessary to open the AC breakers of the MMC after converter blocking since the MMC with HBSMs cannot self-extinguish the fault current. After the necessary line deionization, the firing angle of LCC will be

gradually decreased, the MMC and both AACs are de-blocked and all DSs are switched on. Meanwhile, the AC breakers of MMC will be re-closed, then power (or current) and voltage references are ramped to the pre-fault values. In addition, LCC will switch into constant DC current control when the firing angle decreases to around the steady-state value, at which point the hybrid multi-converter DC grid will recover from the DC fault.

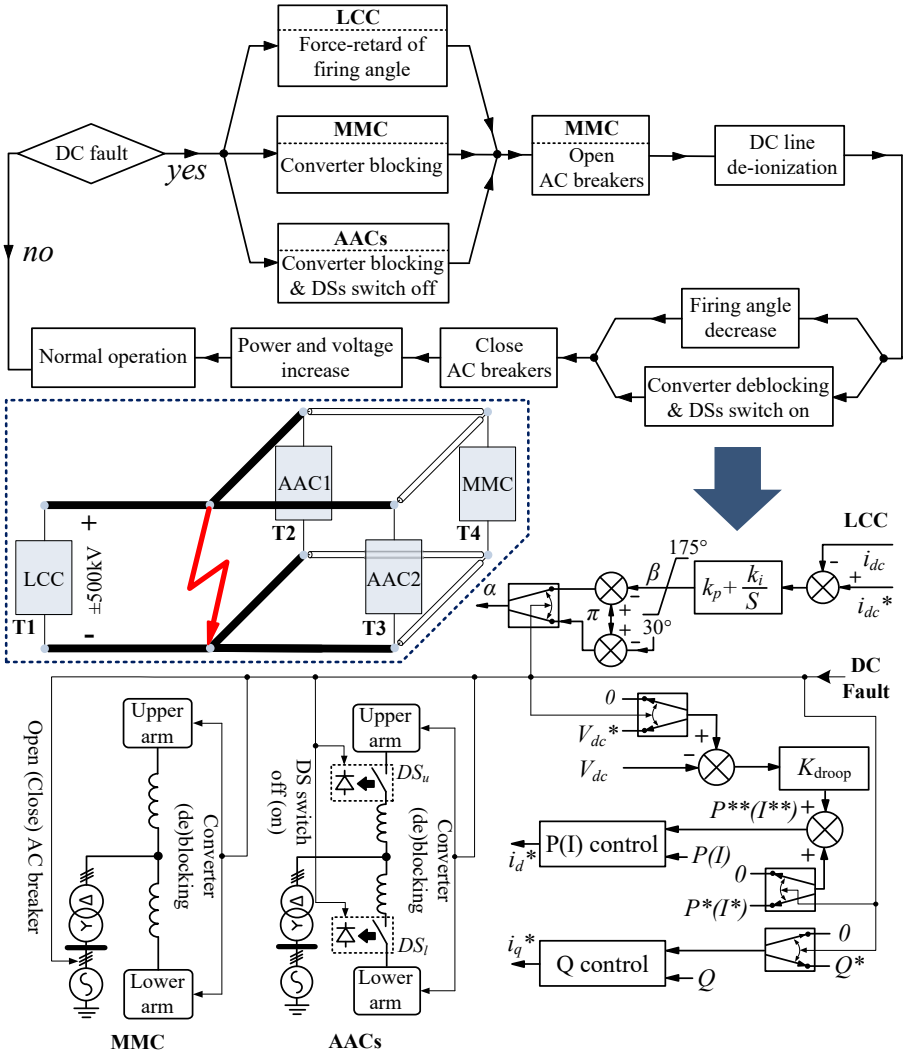


FIGURE 7.3: DC fault ride through scheme in the hybrid multi-converter DC grid.

7.4 DC Power Flow in the Hybrid Multi-Converter DC Grid

Two control configurations of the four-terminal hybrid DC grid are analyzed in this section. In the first configuration (C1), the LCC in the sending end controls the DC current as constant (2 kA) while are three inverters in the receiving end adopt P/V droop control. In

the second configuration (C2), the control mode of AAC2 changes to I/V droop control. The control modes of C1 and C2 all belong to mixed droop control.

7.4.1 DC Power Flow under Normal Operation

The initial power references for AAC1, AAC2 and MMC are -500 MW, -900 MW (or -0.9 kA) and 1000 kV, respectively (Table 7.4). Moreover, the AC reactive powers for both AACs and MMC are all set as zero.

TABLE 7.4: References for high-level control in the hybrid multi-converter DC grid.

Parameter		**LCC (T1)**	**AAC1 (T2)**	**AAC2 (T3)**	**MMC (T4)**
I_{dc}^{*} (kA)	C1	2	-	-	-
	C2	2	-	-0.9	-
V_{dc}^{*} (kV)	C1	-	-	-	1000
	C2	-	-	-	1000
P_{dc}^{*} (MW)	C1	-	-500	-900	-
	C2	-	-500	-	-
δ_{droop}		-	0.05	0.05	0.05
K_{droop}		0	18	24*	20

*24 MW/kV for P/V droop control and 24 A/kV for I/V droop control.

Following with the initial power flow calculation method in Chapter 4.4.1, the DC current directions in each branch (Fig. 7.4) can be obtained by assuming the initial current references as power references (2000 MW for LCC and 900 MW for AAC2 with I/V droop control), and the coefficient $\boldsymbol{\Lambda}$ is:

$$\boldsymbol{\Lambda} = \begin{bmatrix} 0 & 1 & 1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 \end{bmatrix}. \tag{7.1}$$

Moreover, the line conductance matrix ($\boldsymbol{G_l}$) of the DC grid is $[0.1312, 0.3937, 0.7874, 0.9091, 0.6061]^{\mathrm{T}}$.

Substituting the known values into (4.42), the initial DC power flow can be derived (Table 7.5) which also includes all DC current values. In addition, the LCC in the rectifier adopts constant DC current control, thus the droop constant is zero. The DC voltage deviation ratio is 0.05, and the droop constants for the three terminals are set as 18, 24 and 20, respectively.

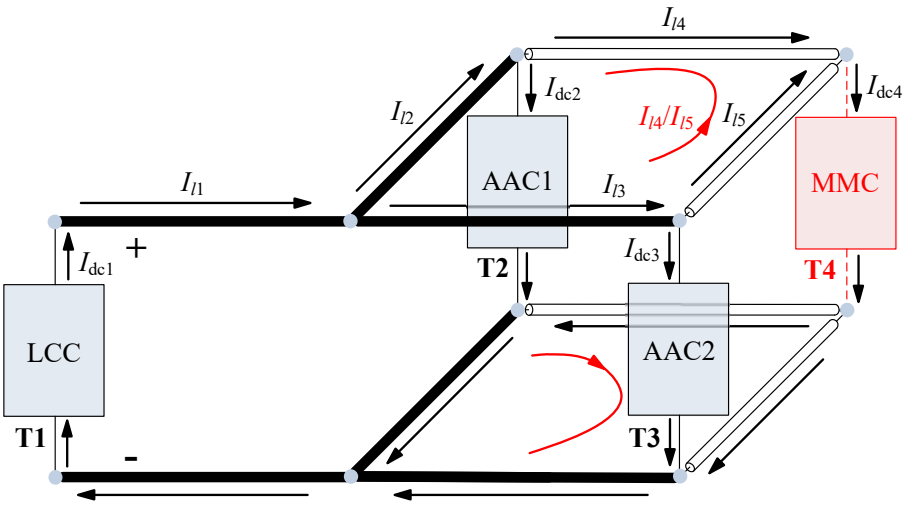


FIGURE 7.4: Detailed current directions of initial state (black) and after MMC outage (red) in the hybrid multi-converter DC grid.

TABLE 7.5: Calculation of initial DC power flow for normal operation in the hybrid multi-converter DC grid.

Parameter		**LCC (T1)**	**AAC1 (T2)**	**AAC2 (T3)**	**MMC (T4)**
I_{dc} (kA)	C1	2.0000	−0.4997	−0.8991	−0.6012
	C2	2.0000	−0.4997	−0.9000	−0.6003
V_{dc} (kV)	C1	1034.5333	1000.6561	1000.9999	1000.0000
	C2	1034.5319	1000.6555	1000.9979	1000.0000
P_{dc} (MW)	C1	2069.0666	−500.0000	−900.0000	−601.2269
	C2	2069.0638	−500.0000	−900.8981	−600.3275
I_{line} (kA)	I_{l1}	I_{l2}	I_{l3}	I_{l4}	I_{l5}
C1	2.0000	0.7979	1.2021	0.2982	0.3030
C2	2.0000	0.7976	1.2024	0.2979	0.3024

7.4.2 DC Power Flow after MMC Outage

When the MMC in the 4-terminal hybrid DC grid is isolated due to a permanent AC fault, the DC power is re-distributed in the remaining three converters (LCC and both AACs). The current topology configuration is shown in Fig. 7.4, following with the current directions in each branch (red lines) obtained by single P/V droop control assumption. The current coefficient $\boldsymbol{\Lambda}'$ is:

$$\boldsymbol{\Lambda}' = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 0 & -1 & 0 & -1 \\ 0 & 0 & -1 & 1 \end{bmatrix}, \tag{7.2}$$

and the line conductance matrix ($\boldsymbol{G}_l'$) is $[0.1312, 0.3937, 0.7874, 0.3636]^{\mathrm{T}}$.

It is necessary to determine the power limitation of other converters after MMC outage. Combining (4.38), (4.60) and (4.39)-(4.62), the DC power deviations for C1 in LCC, AAC1 and AAC2 are 30.5150 MW, -271.2725 MW and -360.5483 MW, respectively, which shows AAC2 is overloaded. For calculating the power flow accurately, AAC2 should be in constant DC power control ($K_{droop,AAC2} = 0$) and the final DC power flow can be obtained by further substituting $\Delta P_{dc_{AAC2}}$ ($\Delta P_{dc_{AAC2}} = -300$ MW) into (4.61). For C2, the DC power of AAC2 is -1268.0533 MW (eq. (4.58)) which also exceeds the maximum power limitation, thus AAC2 switches into constant DC power control. The obtained power flows for the two control configurations after the MMC outage are given in Table 7.6.

TABLE 7.6: Calculation of DC power flow after MMC outage in the hybrid multi-converter DC grid.

Parameter		**LCC (T1)**	**AAC1 (T2)**	**AAC2 (T3)**
I_{dc} (kA)	C1	2.0000	-0.8236	-1.1764
	C2	2.0000	-0.8236	-1.1764
V_{dc} (kV)	C1	1053.7257	1019.5249	1020.0261
	C2	1053.7250	1019.5243	1020.0254
P_{dc} (MW)	C1	2107.4514	-839.6395	-1200.0000
	C2	2107.4501	-839.6381	-1200.0000
K_{droop}		0	18	0
I_{line} (kA)	I_{l1}	I_{l2}	I_{l3}	I_{l4}/I_{l5}
C1	2.0000	0.7324	1.2676	0.0911
C2	2.0000	0.7324	1.2676	0.0911

7.5 Simulation Results

This section provides verification of the power flow generalized calculation results for the hybrid DC grid via simulation in PLECS-Blockset and Simulink. The temporary AC and DC FRT capabilities of the hybrid DC grid are also demonstrated with control configuration 1 based on the combined fault handling schemes.

7.5.1 Power Flow Verification

Table 7.7 shows the simulation results of the initial DC power flow for two control configurations (C1 and C2) under mixed droop control. The results validate the precise initial

DC power flow calculation.

The DC power and current of MMC drops to zero due to the converter outage, thus the DC power flow is re-distributed within LCC, AAC1 and AAC2. The power flow simulation results of the remaining three converter are summarizied in Table 7.8. The simulation results are in accordance with the calculation results of Table 7.6 validating the accuracy of the power flow expression after the MMC outage.

TABLE 7.7: Simulation results of initial DC power flow for normal operation in the hybrid multi-converter DC grid.

Parameter		**LCC (T1)**	**AAC1 (T2)**	**AAC2 (T3)**	**MMC (T4)**
I_{dc} (kA)	C1	2.0002	−0.4997	−0.8992	−0.6013
	C2	2.0000	−0.4996	−0.8999	−0.6003
V_{dc} (kV)	C1	1034.5333	1000.6561	1001.0000	999.9999
	C2	1034.5319	1000.6557	1000.9979	1000.0000
P_{dc} (MW)	C1	2069.0667	−500.0000	−900.0000	−601.2270
	C2	2069.0640	−500.0002	−900.8980	−600.3275
I_{line} (kA)	I_{l1}	I_{l2}	I_{l3}	I_{l4}	I_{l5}
C1	2.0002	0.7980	1.2022	0.2983	0.3030
C2	2.0000	0.7975	1.2025	0.2979	0.3024

TABLE 7.8: Simulation results of DC power flow after MMC outage in the hybrid multi-converter DC grid.

Parameter		**LCC (T1)**	**AAC1 (T2)**	**AAC2 (T3)**
I_{dc} (kA)	C1	2.0000	−0.8236	−1.1764
	C2	1.9998	−0.8236	−1.1765
V_{dc} (kV)	C1	1053.7257	1019.5250	1020.0260
	C2	1053.7250	1019.5243	1020.0254
P_{dc} (MW)	C1	2107.4514	−839.6395	−1200.0001
	C2	2107.4501	−839.6380	−1199.9999
K_{droop}		0	18	0
I_{line} (kA)	I_{l1}	I_{l2}	I_{l3}	I_{l4}/I_{l5}
C1	2.0000	0.7324	1.2676	0.0911
C2	1.9998	0.7324	1.2674	0.0910

Fig. 7.5 shows the waveforms of DC powers, voltages, currents and five line currents for normal operation (0 $\sim$ 1 s) and after the MMC outage (1 s $\sim$ 5 s) with C1 in the hybrid DC grid. The waveforms of C2 are not shown as the control modes are identical for both

control configurations after an MMC outage. It is noted that the sudden increase of DC voltages in the remaining converters is due to the instantaneous power shortage at the inverter side.

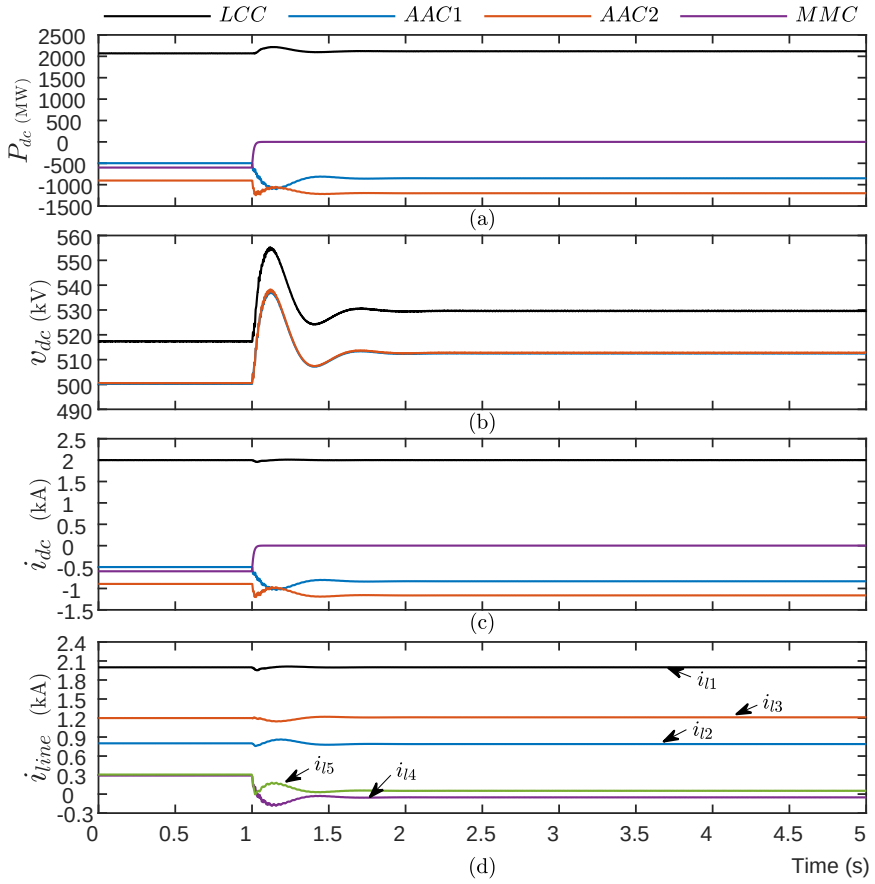


FIGURE 7.5: Steady-state and transient waveforms before and after MMC outage with C1 in the hybrid multi-converter DC grid: (a) DC power, (b) DC voltage, (c) DC current and (d) line currents.

7.5.2 AC FRT Capability

Based on the temporary AC fault handling scheme in Chapter 7.3.1, Fig. 7.6 shows the results of a 0.2 s three-phase short-circuit fault of MMC occurring at 0.2 s. Active and reactive power variations in the four terminals of the AC-grid are shown in Fig. 7.6(a) and (b), respectively. The active power and DC current of MMC decreases to zero during AC fault, thus leading to the oscillation of the active powers and DC currents (Fig. 7.6(f)) in LCC, AAC1 and AAC2. Accordingly, the line currents in the five branches (Fig. 7.6(g)) also oscillate with the DC current oscillation that i_{l1} (or DC current in LCC) keeps almost

constant, i_{l2} decreases to below 0.5 kA, i_{l3} increases to above 1.5 kA, i_{l4} decreases and i_{l5} increases but the current direction is changed.

In addition, the DC voltages of the four terminals and SM capacitors of both AACs and MMC all increase on different levels during the AC fault of MMC. The increase of DC voltages in four terminals is within 0.07 p.u. (Fig. 7.6(e)), while the deviation of AAC1, AAC2 and MMC is within 0.13 p.u., 0.2 p.u. and 0.15 p.u., respectively (Fig. 7.6(h)-(j)). In general, the hybrid DC grid shows satisfactory AC FRT capability with the proposed AC fault control scheme.

7.5.3 DC FRT Capability

At 0.2 s, a 0.1 s pole to pole DC fault with resistance of 10 Ω occurring at the end of OHL 1 as Fig. 7.3. The system recovers from DC fault after fault clearance and 0.4 s line de-ionization. Following the DC fault handling scheme of Chapter 7.3.2 (Fig. 7.7(a), (b)), the firing angle of the LCC is increased to 150° after 4 ms, extinguishing the fault current in the rectifier side (Fig. 7.7(l)). The SMs at the inverters, meanwhile, are blocked, DSs of AACs are switched off and DC voltage and power references decrease to zero (Fig. 7.7(c), (d)). In addition, the AC breakers of MMC open after 60 ms for protecting the SMs of MMC (Fig. 7.7(e)). It is noteworthy that thyristors are required in HBSMs for protecting antiparallel diodes during the 60 ms. At 0.7 s, the firing angle of LCC is gradually decreased to the pre-fault value, all SMs and DSs of AACs and MMC are debloked and switched on, respectively. Then, the AC breakers of MMC are closed, while the references of powers and DC voltages of AACs and MMC are ramped from zero to pre-fault vaules.

During the DC fault, the DC voltages in four terminals are gradually decreased to zero due to the energy reduction in the DC-link (Fig. 7.7(f)), and the oscillation of DC currents is caused by the discharging of DC-link capacitors (Fig. 7.7(g), (h)). The SM capacitor voltages of both AACs are slightly higher after converter blocking due to the energy absorption from AC-side to DC-link, while the SM capacitor voltages of MMC are not affected. In the whole DC fault handling process, the deviation of SM capacitor voltages is regulated within the range of 0.3 p.u. (Fig. 7.7(i)-(k)), and the DC grid returns to normal operation within 0.5 s. The results of DC fault also demonstrate the difference between AAC and MMC that the AAC shows the potential of DC fault self-clearing capability while MMC with HBSMs has to rely on breakers handling DC fault.

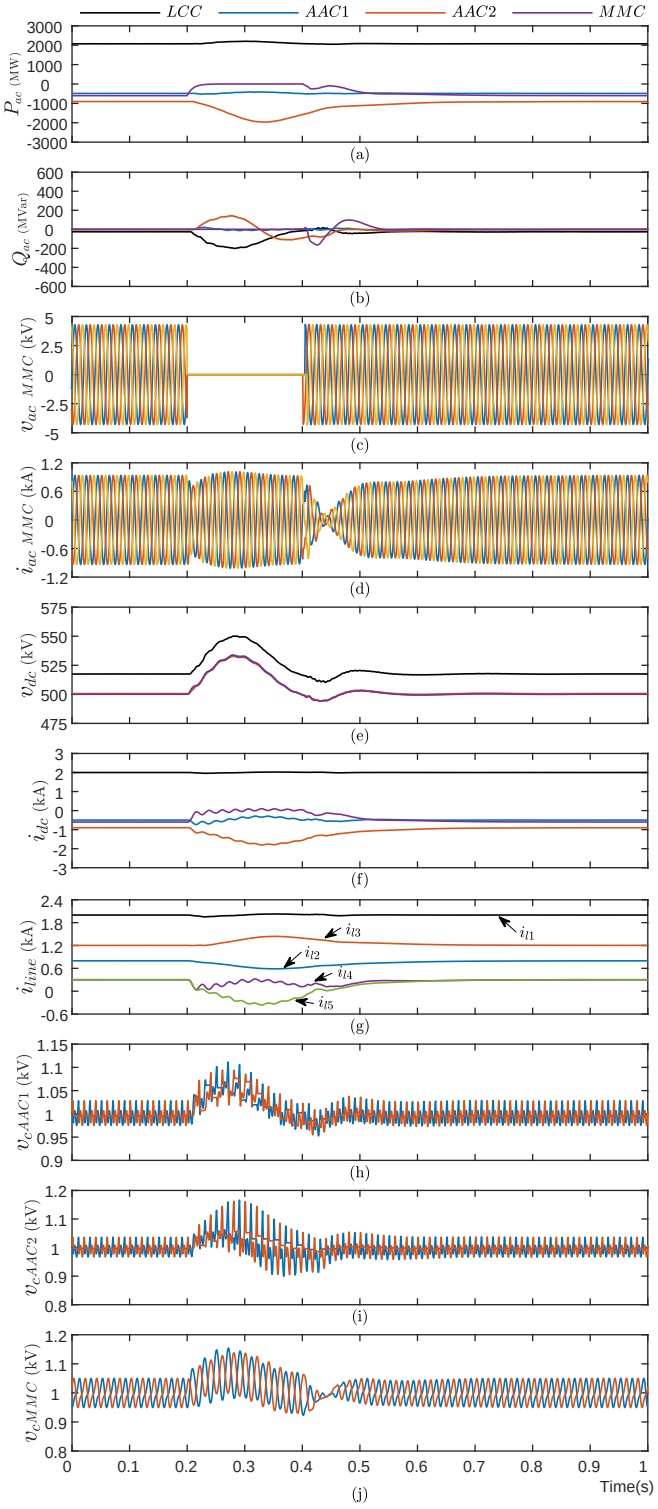


FIGURE 7.6: Temporary three-phase short-circuit fault at MMC in the hybrid multi-converter DC grid: (a) AC active power, (b) AC reactive power, (c) AC voltages of MMC, (d) AC currents of MMC, (e) DC voltages, (f) DC currents, (g) Line currents, (h) SM capacitor voltages of AAC1, (i) SM capacitor voltages of AAC2 and (j) SM capacitor voltages of MMC.

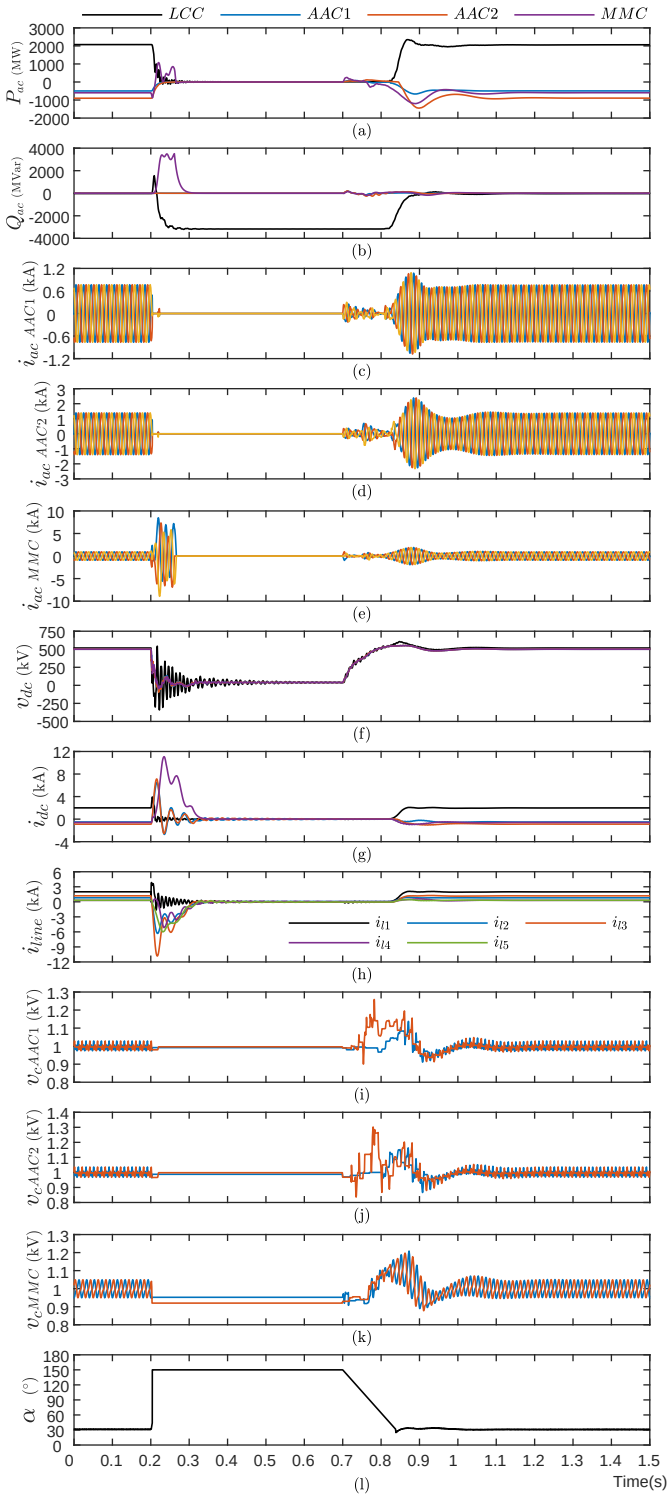


FIGURE 7.7: Temporary pole to pole DC fault in the hybrid multi-converter DC grid: (a) AC active power, (b) AC reactive power, (c) AC currents of AAC1, (d) AC currents of AAC2, (e) AC currents of MMC, (f) DC voltages, (g) DC currents, (h) line currents, (i) SM capacitor voltages of AAC1, (j) SM capacitor voltages of AAC2, (k) SM capacitor voltages of MMC and (l) firing angle of LCC.

7.5.4 Discussion

Excellent AC and DC FRT capability is of paramount importance for future complex multi-converter DC grids. The simulation results of AC and DC faults in the developed hybrid multi-converter DC grid show the combined AC and DC fault handling schemes can ensure the safe operation of the hybrid DC grid. The oscillations of corresponding powers, voltages, currents during faults are all within acceptable range, and the fault recovery stage is stable and rapid.

Additionally, the power flow analysis can be used to assess the static security of multi-converter DC grids. The proposed generalized expression of DC power flow in Chapter 4.4 first determines the initial power flow for normal operation at steady-state operating point under mixed P/V and I/V droop control (Fig. 4.11). Then, the power flow of post contingency (converter outage) operation is derived considering the power limitation (Fig. 4.12), which assesses the power flow in the remaining converters precisely. Since the power flow of post fault (temporary AC and DC fault) operation should restore to the initial power flow, the fault recovery level can be estimated by the determined initial DC power flow.

7.6 Conclusion

The AC and DC FRT capability combined with proposed DC power flow generalized expression under mixed P/V and I/V droop control are investigated in the LCC, MMC and AACs-based hybrid DC grid. The correlation between simulation-based DC power flow results and the theoretical power flow calculations for initial and post contingency scenarios verify and validate the performance of the hybrid DC grid. The results of temporary AC and DC fault demonstrate the robustness of the hybrid system under the combined fault handling schemes. Moreover, the power transmission can rapidly recover from faults, and the power flow is restored to the initial state. In general, hybrid multi-converter DC grid and its operation are valid steps towards investigation of more complex DC-grids, and the DC power flow analysis can be utilized for effective reconfiguration of complex DC grids under post fault and contingency operation.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The future trend for HVDC market would be the combination of multiple converters to constitute complex MTDC systems and DC grids. This thesis focuses on the development of hybrid HVDC system, MTDC system, DC grid combining multiple technologies (LCC, VSC) and topologies (MMC, AAC and other various topologies). The work of this thesis is summarized as below:

- LCC is the most mature technology and many HVDC projects have been commissioned in the world, while the majority are PTP systems. VSC overcomes commutation failures and is more suitable for the formation of MTDC systems. The modular VSC topologies, including the MMC with various SMs, AAC and other hybrid converter configurations, provide improved performances than conventional VSC-based HVDC. The emerging AAC possesses DC fault self-clearing capability and reduces the energy storage in SM capacitors. Also, the integration of LCCs at the sending ends and different modular VSCs at the receiving ends benefits the remote power delivery and flexible power flow regulation. Three different hybrid HVDC systems are developed in Chapters 5, 6 and 7 for demonstrating the feasibility of combination of multiple technologies and topologies.
- HVDC benchmark models can provide reference basis and allow comparison of system performances for future study of different HVDC systems. From the summarization of the available benchmark models for HVDC converters, systems and DC grid studies, the research gaps, data availability and expansion capability of these benchmark models are addressed in Chapter 2 facilitating the future development of more accurate and relevant HVDC benchmark models.

- The basic topologies, operations and control schemes of the LCC, MMC and AAC are reviewed in Chapter 3 with comprehensive theory analysis for the development of hybrid HVDC systems. Besides, the EMT, electromechanical transient, dynamic frequency capturing modeling approaches and co-simulation studies for HVDC systems are discussed in detail. The detailed equivalent models based on the EMT modeling method are adopted for simulations in Chapters 4 - 7 of this thesis.

- A generalized expression of DC power flow is proposed in Chapter 4 to ensure the static security of MTDC systems and DC grids under mixed P/V and I/V droop control. The generalized expression is the extension of the DC power flow calculation methods of single P/V and I/V droop control. Results derived from the theoretical analysis of the initial DC power flow for normal operation and the DC power flow after converter outage are consistent with the simulation results in an MMC- and further developed LCC, MMC and AAC-based DC grids.

- For exploring integrations of different HVDC technologies and topologies, an LCC and AAC-based hybrid PTP system is first developed in Chapter 5 with detailed control hierarchy description and parameter selection. The simulation results of steady-state operation, reference tracking and fault handling performance of AC and DC faults show the robustness of the hybrid HVDC system. Also, the AAC shows better DC fault handling capability in the hybrid HVDC system than typical HB-MMC. Although the MMC with FBSMs can also tolerate DC fault, the required number of SMs in the AAC is less than the MMC with HBSMs and FBSMs.

- By extending the hybrid LCC-AAC PTP HVDC system, a hybrid MTDC system with one LCC and two AACs under P/V droop control is further demonstrated in Chapter 6 to verify the feasibility of the AAC in hybrid MTDC systems. Presented simulation results of multiple operating scenarios and fault performance of AC and DC faults validate AACs can be in receiving ends to flexibly absorb the power delivered from the LCC.

- Combining the conventional LCC, state-of-the-art MMC and emerging AAC, a hybrid DC grid with the three converters is finally presented in Chapter 7 investigating hybrid multiple DC grids constituted by different converter topologies. The impact of transient AC and DC faults is examined in the hybrid multi-converter DC grid following with the FRT combination schemes. In general, the different hybrid HVDC systems developed in the thesis lay the preliminary fundation for future more complex MTDC systems and DC super grids combining different converters from multiple vendors.

8.2 Future Work

This section introduces the suggested future work based on the work in this thesis.

- Development of other hybrid HVDC systems considering the connection of the AAC to passive networks and the commutation support of the AAC to the LCC operating in inverter mode.
- Exploration of detailed fault location and protection for MTDC systems and more complex multi-converter DC grids.
- Research on fault analysis and calculations for different modular VSCs and hybrid multi-converter DC grids.
- Implementation of developed HVDC systems in real-time digital simulators focusing on the system of systems integration, protection validation, hardware testing and the path to a virtual digital twin.
- Further study on the application of LCC, MMC and AAC for DC systems at medium voltage level for large-scale renewable energy integration both as distribution networks and as collection grids.

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