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Post Correlation CWI and Cross Correlation Mitigation Using Delayed PIC

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BIOGRAPHY

Éamonn Glennon is a Principal Engineer at SigNav Pty Ltd and has over 16 years experience in GPS receiver firmware development. For the last 12 years he has been employed at SigNav where he has had an integral role in the development of much of the company's software. This work encompasses a wide range of GPS chipsets, including a custom ASIC and RF front end developed by Auspace Limited, the well known Zarlink chipsets (GP2021/GP2010, GP4020/GP2015), latest generation uNAV Microelectronics GPS chipsets and the UNSW Namuru FPGA GPS platform. He holds a B.Sc, B.E (Hons) and a M.Eng.Sc and is currently pursuing a PhD at the University of New South Wales part time.

Dr Rod Bryant has been leading GPS receiver developments for 18 years. During the past 7 years the primary focus of this work has been on weak signal and indoor GPS and Assisted GPS, with particular emphasis on indoor timing. Prior to that the focus was on GPS Dead Reckoning and near real-time post-processing solutions for vehicle tracking. Dr Bryant is the founder and CTO of SigNav Pty Ltd. He was awarded a William Culross Prize For Scientific research for his PhD in Optimal Systems for Echo-Location in 1986 after 5 years at the University and a twelve year career with PMG/Telecom Australia.

A/Prof Andrew Dempster was appointed Director of Research in the School of Surveying and Spatial Information Systems at the University of New South Wales in mid-2004. His research interests are signal processing in GPS receivers, software-based approaches, and new positioning technologies. His previous appointment was with the Department of Electronic Systems at the University of Westminster, London, where he was appointed in 1995 after completing his PhD at University of Cambridge.

Peter Mumford is a researcher at the School of Surveying and Spatial Information Systems, University of New South Wales. Currently he is working on GNSS receiver design and INS/GNSS integration. Peter holds a BE in Surveying and a B.Sc in Mathematics. He specializes in FPGA, embedded software and electronic design in the GNSS realm.

ABSTRACT

A number of different techniques are available to mitigate the problem of cross correlations caused by the limited dynamic range of the 10-bit Gold codes used for the GPS C/A codes. These techniques include Successive Interference Cancellation (SIC) and parallel-interference cancellation (PIC), where the strong signals are subtracted at IF prior to attempting to detect the weak signals. In this paper, a variation of these techniques is proposed whereby the subtraction process is delayed until after the correlation process, although still employing a pure reconstructed C/A code signal to permit prediction of the cross correlation process. This paper provides details on the method as well as showing the results obtained when the method was implemented in a hardware receiver on a large scale FPGA. The benefits of this approach are also described, as is the application of the method to the cancellation of CW interference.

INTRODUCTION

The Global Positioning System has found widespread usage in a large number of different applications, including many that were not in the original requirements. Examples of such applications include the use of GPS in indoor applications, remote sensing and the addition of pseudolites to improve accuracy in locations where satellite visibility is impaired. These applications all share a common difficulty, namely a requirement to operate in scenarios where weak signals need to be processed in the presence of other strong signals. This is a problem because the 10-bit Gold codes used for the C/A spreading code only offer 21 dB of isolation between strong and weak signals as the C/A codes are not completely orthogonal [1]. This means that components of the strong signal can leak into the weak signal space causing spurious detections of the weak signal.

A number of different techniques are available for cross correlation mitigation (CCM) in GPS C/A code receivers, although most are not suitable for use in low-cost real time GPS receivers. Successive Interference Cancellation (SIC) is a well known Multiple Access Interference (MAI) mitigation technique that has been applied to GPS operating in the presence of pseudolites [2], with the method having been verified using both Matlab generated and pre-recorded GPS IF data. Subspace projection

techniques [3] can also be applied to GPS signals [4], although such techniques have a very high computational load thereby making the methods impractical for typical commercial receivers. Approximations to subspace projection techniques can be employed to overcome the computation difficulties, with the projection-subtraction method of [5] requiring subtraction from the raw GPS intermediate frequency (IF) samples only those components of the strong signals that lie in the weak signal subspace prior to weak signal despreading and down-conversion. The technique can therefore be considered a refinement of SIC in which the entire strong signal is subtracted, with both methods requiring IF data representation that has sufficient dynamic range to permit such subtraction to take place. The projection-subtraction technique has only been applied to Matlab simulated data. Another suboptimal subspace projection technique is Adaptive Orthogonalization Using Constraints (AOUC) [6, 7]. AOUC has been proven using both Matlab simulated and real GPS receiver data via post-processing in a software correlator, but has the disadvantage that the number of strong signals that can be handled is limited to less than four. MAI can also be removed post-correlation, with the method of [8]. This method shares some similarities with the technique of this paper, which we call Delayed Parallel Interference Cancellation (DPIC), although there are also important differences. DPIC can also be shown to be related to Decorrelating Detector [9], but offers a simpler implementation.

DPIC CONCEPT

The basic idea for DPIC can be traced to the design of SIC and the question of how best to implement the subtractive elements. The reason this is a problem is that GPS input signals as output by GPS front end (FE) chips are typically one, two or three bit values with the GPS signals buried well below the noise. One method is to convert the signal to more bits, perform the subtraction at full resolution and then to re-quantize back to one, two or three bits after a dither operation to ensure that the re-quantized signal differs from the original input signal.

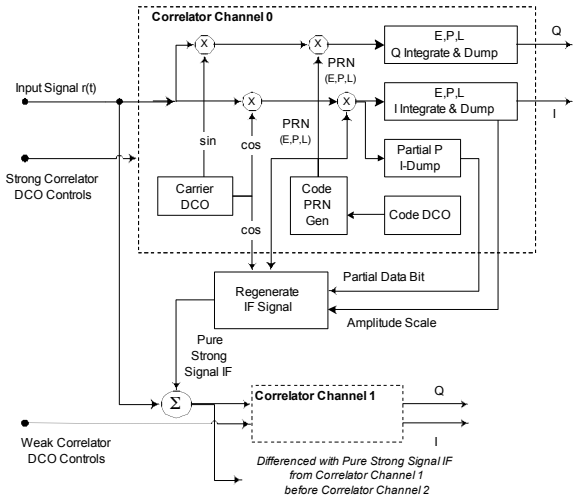

Figure 1: Detailed SIC

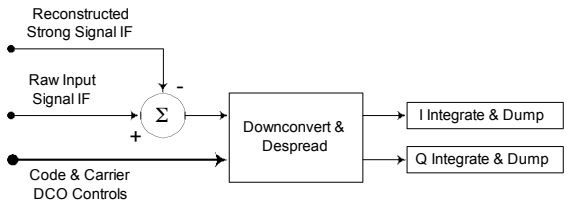

Figure 2: Standard Processing of Differenced IF

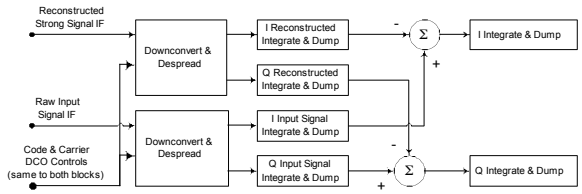

Figure 3: Alternate Processing of Differenced IF

An alternative solution to this problem is to avoid performing the subtraction at the low bit quantization level, which is possible using the following argument. Consider Figure 1 and 2 which show respectively a detailed block diagram of a single stage of SIC and a simplified portion of the SIC segment of direct interest, namely the subtraction between the pure reconstructed strong signal IF and the raw input IF prior to down-conversion and despreading at each stage. Taking into account the linearity of the downconvert and despread (DCD) block, the operations can be rearranged to give the block diagram of Figure 3. This shows the single DCD block moved from after the subtraction process to a new case where each input signal is processed with its own DCD block and with each DCD block subject to the same code & carrier DCO control signals. The DCD block processing the reconstructed pure IF signal is slaved to the DCD block being used to search for the real GPS signal present in the raw IF bit-stream and performs the function of calculating in real-time the I & Q cross correlations between the strong signal & weak signal being searched for by the correlator. Since each DCD block comes with its own set of accumulation registers, the subtraction process applies to those values and occurs at a lower rate due to the decreased rate of the I & Q integrate and dump samples.

DETAILED DPIC DESIGN

Figure 4 shows a detailed block diagram showing SigNav's patent-pending DPIC scheme with a single strong signal cancellation, but with some additional refinements. The first refinement is to simplify the process of reconstructing the pure strong signal IF to the noise free product of the strong signal PRN code, the strong signal data-bit value and strong signal in-phase carrier signal. Compensation for the strong-signal amplitude is then performed by scaling the reconstructed strong signal IF integrate and dump samples by the magnitude of the strong signal (or magnitude of the strong signal in-phase component) prior to subtraction from the raw IF integrate and dump samples. Implicit in this process is that the strong signal is being tracked and the carrier DCO for the

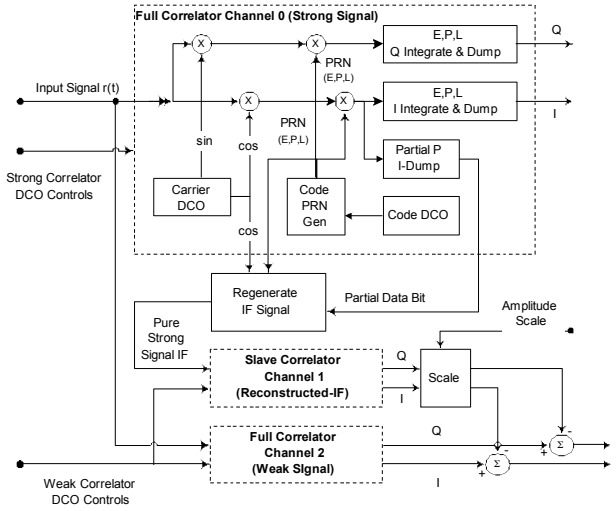

Figure 4: Detailed DPIC with 1 strong signal cancellation

strong signal is phase-locked. A truth table showing the reconstruction of the strong signal IF is given in Table 1 assuming 1 and 0 indicate positive and negative signs in the sign/magnitude representation respectively. This representation is employed by the Zarlink GP2015 front end chip [10], although some other chipsets use the reverse convention. It should be noted that in the software correlator implementation described in reference [11], the reverse sign convention was employed with no ill effects even using the GP2015.

The second refinement is inclusion of a partial I accumulation register in the full channel that outputs the best estimate of the strong signal data-bit given the signal received thus far. Proper compensation for strong signal data bits is essential because as this is a fully coherent subtractive process, failure to account for the strong data bit sign will result in addition instead of subtraction thereby exacerbating the cross correlation (CC) noise. The partial I accumulation is reset at the end of each strong signal C/A code epoch if strong signal bit-synchronization has not been achieved or on the bit boundary if bit synchronization has been achieved and a hardware maintained bit counter is available and set appropriately. Both of these bit-estimation methods were used in the FPGA implementation, although the software correlator implementation of [11] used a different method whereby the most recent latched I sample dump value was used for the first 250 chips in the C/A code epoch (while the SNR value is still accumulating) and the partial I accumulation for the last 773 chips. This ensures that for most epochs, the bit estimation will be correct unless there is a bit-change. Using a bit estimation process is required because the strong signal C/A code epoch rollover is not aligned to the weak signal C/A code epochs and hence strong signal bit transitions will usually occur partway through a weak signal C/A code epoch. It is for the same reason that the data sign bit cannot be applied during the software scaling process prior to subtraction. An unfortunate consequence of this process is that the value of the sign bit will almost always be incorrect for a short period following reset of

Data Bit Modulated Strong PRN Chip Sample		Strong In-Phase Carrier DCO Sample			Reconstructed Strong Signal Sample		
DP	DPs	C	Cs	Cm	RS	RSs	RSm
1	1	-2	0	1	-2	0	1
1	1	-1	0	0	-1	0	0
1	1	1	1	0	1	1	0
1	1	2	1	1	2	1	1
-1	0	-2	0	1	2	1	1
-1	0	-1	0	0	1	1	0
-1	0	1	1	1	-1	0	0
-1	0	2	1	1	-2	0	1

Table 2: Strong Signal Reconstruction Truth Table

the accumulation, although the stronger the signal the faster the correct value will be reached. As such, the use of bit-synchronized reset of the partial I accumulation is recommended for best results.

Although block diagrams thus far refer to a single strong signal only, extension of the process to multiple strong signals is straightforward. The GPS receiver software or hardware correlator is required to have a number of slave channels in addition to the complement of full channels that are typically employed. Slave channels differ from full channels in that they do not require code & carrier Numerically Controlled Oscillators (NCOs) or code generators, using instead the signals from the master full channels, although they do require pure IF regeneration blocks as well as mixers, de-spreaders and accumulators for the pure IF signals. The number of fingers present in each slave channel is the same as the full correlator channel and they are required to have identical code phase separations. A slave channel must be allocated to each strong/weak signal pair that is likely to suffer from CC effects. The master of each slave channel is the full correlator channel index *WI* being used to search for the weak signal and the signals fed into the 'Regenerate IF' block are sourced from the full channel index *SI* that is phase locked to the strong signal.

In a hardware (FPGA) implementation, the slave channel block differs from the full channel block since the latter typically consumes more silicon resource and the functions performed by the blocks differ. Linkage between the full correlators and the slave correlators takes place via a bus, where each full channel outputs a number of signals that form part of the bus. The bus made up of signals from all of the full channels is then input to each slave channel which is then able to select those signals that are pertinent to it, depending on the weak/strong channel indices applicable. The selection process is performed using multiplexers that select based on the values of *SI* and *WI*. This arrangement differs from a software correlator architecture where all the channels are identical and logic switches determine channel behaviour and input

selections, while shared memory accesses permit communication between master and slave channels.

It should be apparent the number of required slave channels depends on both the number of strong signals and the number of weak signals that need to be acquired. If there are N_s strong signals and N_w weak signals, then the total number of full correlators N_{Full} and slave correlators N_{Slave} required to detect & mitigate all of the signals is:

$$N_{Slave} = N_s \times N_w$$
$$N_{Full} = N_s + N_w$$

N_{Full} is typically greater than the total number of visible signals, which in the case of GPS is usually constrained to 12. The maximum value for N_{Slaves} given a value for N_{Full} of 12 is 36. This number of correlators is not excessive given modern silicon capacity. Furthermore, inclusion of additional multiplexing and delay elements can also permit the slave channels to process raw-IF inputs using delayed C/A code sequences thereby permitting the channels to be reconfigured to allow for correlator search acceleration, albeit without the benefit of CCM. This makes the disadvantage of requiring a large number of correlator channels far less of a problem. It should also be pointed out that a decision to leave some strong signals unmitigated could also be made, since not all strong signals will cause problems. In fact, only those strong signals have a relative Doppler carrier (RDC) frequency separation of multiples of one kHz from the weak signals are likely to cause difficulty [5] and hence only those CCs need to be cancelled.

DPIC SOFTWARE PROCESSING

When the software is processing the weak signals, it is required to subtract from the weak full correlator I&Q integrate and dump samples a scaled multiple of each slave I&Q integrate and dump sample associated with the weak channel. Mathematically this can be written as:

$$iq = iq_w - \sum_{k=0}^{N-1} iqs_k \cdot \frac{|i_k|}{20000}$$

where iq is the complex noise cancelled correlator output, iq_w is the full complex weak signal correlator output, iqs_k are the complex correlator outputs for slave channels k, i_k is the in-phase output for strong signal k, N is the number of slave channels and *20000* is the scale factor for a Zarlink GP2015/GP2021 chipset and the Namuru correlator design which shares some features of the GP2021 correlator.

Since the subtraction process is performed in parallel in each case, the process is similar to parallel interference cancellation (PIC), whilst the "delayed" prefix refers to the fact that the subtraction process is delayed until after the correlation has been performed. This is an advantage of the method since the strong signal amplitude $|i_k|$ needs to be examined during the subtraction process which means that should the amplitude reduce, the subtraction can be skipped since the CC noise from that satellite will be lower and may not cause a problem. The subtraction can therefore be conditional on $|i_k|$ exceeding a specified threshold.

The source of the nominal 20000 scale factor can be easily derived by consideration of the processing by a slave channel of the reconstructed IF for a strong signal channel using the carrier and code NCO settings from the same strong signal channel. This is different to the normal CCM procedure whereby the correlators in the slave channel are driven by the carrier and code NCO settings from a weak channel correlator. In this scenario, the PRN codes in the slave correlator and the reconstructor IF block are identical and hence the product is always one. Similarly, the carrier NCO outputs NCO_{out} and regenerated IF outputs IF_{out} are also identical, although the meanings assigned the signals bit values differ. For the reconstructed IF output, the magnitude bit value of 0 and 1 indicates a weightings of 1 and 3 respectively, whereby for the carrier DCO signals the weightings are 1 and 2 instead [12]. An example of element by element matching sequences excluding effects of code spreading is given below.

$$NCO_{out} = \{-1,+1,+2,+2,+1,-1,-2,-2,-1,+1,+2,+2,\cdots\}$$
$$IF_{out} = \{-1,+1,+3,+3,+1,-1,-3,-3,-1,+1,+3,+3,\cdots\}$$

In both cases the probability of the magnitude bit having a particular value is equal, which means that the expected value of the product between the pure IF NCO carrier output and the slave channel NCO carrier output can be written as:

$$SF = 40000/7 \times E(1\times1\times½+2\times3\times½) = 20000$$

where E indicates expected value and 40000/7 is the number of IF samples per millisecond. Note that the AGC constraint of having the magnitude bit set 30% of the time does not apply to regenerated IF output which inherits the magnitude statistics from the carrier NCO instead.

DECORRELATING DETECTOR SIMILARITIES

The Decorrelating Detector (DD) is a well known multi-user detector that is able to completely eliminate MAI [9]. Like DPIC, the process is applied post-correlation and involves application of a linear transformation to the vector of standard correlator (matched filter) outputs, where the output of the linear transformation is MAI free.

To understand the operation of the DD, consider the output from each correlator tracking satellite i:

$$y_i(n) = \sum_{k=1}^{N} \int_{nT}^{(n+M)T} A_k d_k(t-\tau_k^d)\, c_k(t-\tau_k)\, d_k(t-\tau_i)\, c_i(t-\tau_i)\, e^{j(2\pi f t+\phi)}\, dt + n_i$$

A_k, d_k, and c_k are the amplitude, data-bit, spreading code for satellite k, f_{dki} and φ_{ki} are relative Doppler carrier

(RDC) frequency and phases between satellite k and i respectively and n_i is the noise. This can be written in a matrix/vector format whereby the data-bits d_i are considered to be elements of input vector $\boldsymbol{d}$ and the amplitudes A_k are the diagonal elements in a diagonal matrix A. The integral term comprised of the product of the spreading codes and relative Doppler are elements ρ_{ki} in the matrix R, where:

$$\rho_{ki} = \int_{nT}^{(n+M)T} d_k(t-\tau_k^d)\, c_k(t-\tau_k)\, c_i(t-\tau_i)\, e^{j(2\pi f t+\phi)}\, dt$$

R is therefore a matrix is a matrix of 'normalized' cross correlations, where the diagonal elements will be autocorrelations with values of 1 and the off-diagonal elements are generally small in magnitude, assuming the codes are scaled appropriately. The entire system can be written as:

$$\mathbf{y} = R\,A\,\mathbf{d} + \mathbf{n}$$

Multiplying both sides by R^{-1} then permits the original input A $\mathbf{d}$ to be recovered, with this process completely eliminating the MAI.

$$R^{-1}\mathbf{y} = A\,\mathbf{d} + R^{-1}\mathbf{n}$$

Expressing R as the sum of the identity matrix and a matrix of small zero-diagonal cross correlation terms C, it is possible to approximate R^{-1} as:

$$R^{-1} = (I + C)^{-1} \approx I - C$$
$$A\,\mathbf{d} \approx (I - C)\,\mathbf{y} = \mathbf{y} - C\,\mathbf{y}$$

Hence it is clear that DPIC calculates the elements R via the slaved correlator channels and then performs a very simple approximation when applying R^{-1}.

SIMILARITIES TO OTHER METHODS

As previously mentioned, DPIC shares some features with the method described in [8], hereafter referred to as the Zero Doppler Approximation Method (ZDAM). Nonetheless, the differences in the detail between the two techniques are important. Both methods involve post correlation subtraction of the CC noise, although unlike DPIC, ZDAM estimates the cross correlations by means of an approximation that is only accurate when the RDC frequency difference Δf between the strong and weak signals is small. The approximation separates the CC estimate as the product of the strong signal amplitude, the CC calculated assuming Δf of zero and a frequency correcting scaling factor given by sinc(Δf), where first quantity is easily measured and the last two are easily calculated quantities. The CC values with zero Δf needs to be recomputed every 0.1 seconds (10 Hz update rate) since the code phase between strong and weak signals changes at a rate of no more than 6 chips per second.

Unfortunately the frequency correcting scaling factor given in [8] represents a very poor approximation when the Doppler difference between the weak and strong signals is large. For example, consider the results presented in Tables 4.8 and 4.9 of Ward, et-al [13]. Table 4.8 shows that at zero Doppler the worst case cross correlation between any two codes is -23.9 dB. However when measured across all Doppler frequency differences, Table 4.9 shows that Doppler offsets of 1 and 2 kHz the worst case cross correlation between two codes increases to -21.1 dB, albeit with low probability. This is clearly inconsistent with the quoted frequency correction factor.

As a result, when Δf is large ZDAM will fail. It will fail catastrophically if Δf is a non-zero multiple of 1 kHz. This is because when Δf is a multiple of 1 kHz, several cycles of RDC may occur in each C/A code epoch which when mixed with the standard strong signal code completely changes the effective strong signal spreading code as seen by the weak code.

Another inadequacy of the ZDAM CC estimate concerns the handling the effect of data-bit transitions. Since the relative code-phase between the strong and weak signals is randomly distributed across the code-space, the effect of any strong signal data-bit transition is to randomly invert that segment of the strong signal code after the transition for the remainder of the weak signal C/A code epoch. During such events the zero Δf CC estimate will also be incorrect, although since bit transitions only occur in 1 out of every 20 epochs the effect is not excessive. It is also unclear whether the CC estimates are corrected for data-bit sign since the only mention of the effect of data-bits is in regard to their effect on the strong signal carrier phase which needs to be corrected for the corresponding 180 degree phase shifts. This suggests that the technique is limited to being applied to magnitudes only and is therefore not a fully coherent technique.

These differences mean that DPIC is much more effective than ZDAM. This is because the cross correlation predictions used in DPIC are much closer to the exact results as given by van Dierendonck [14]. An additional consequence of these differences is that DPIC is able to mitigate against additional classes of interference that cannot be handled by ZDAM, with Continuous Wave Interference (CWI) being a notable example.

FPGA IMPLEMENTATION & TEST

Although DPIC had been previously tested and proven using a software correlator, a hardware based solution was considered to be significantly more useful. This stems from the significant speed benefits to be gained from hardware, as well as the fact that the vast majority of GPS receivers on the market are hardware based. To achieve this, the Verilog FPGA correlator of the UNSW Namuru GPS receiver [15] was modified to support the DPIC design. This required minor modifications to the existing twelve full-correlators to allow interfacing to the slave signal bus, inclusion of instantaneous bit estimation with

	Standard (Logic Elements)	DPIC (Logic Elements)
1 Full Channel	585	605
1 Slave Channel	0	348
12 Channels	9048	14625
Full Design	14313	19873

Table 2: FPGA Utilization for Standard & DPIC Designs

both bit-synchronized and non bit-synchronized modes, inclusion of twelve slave correlator channels and inclusion of a register file to permit control of the configuration of the slave channels. A comparison of the FPGA utilization between the original Namuru Verilog implementation and the DPIC enhanced Namuru implementation is given in Table 2.

For the software component, a new suite of software was created for the Namuru FPGA hardware platform that also included specific serial port commands to allow direct control over satellite channel allocation. The command included selection of parameters such as satellite number, full correlator hardware channel, coherent integration periods, number of non-coherent rounds, the satellite Doppler frequency and Doppler search window, the detection threshold, activation of DPIC and the hardware channels strong signals requiring mitigation. This command was useful during the testing process and was used to configure the correlators when obtaining the experimental results. Automatic activation of CCM functionality within a navigating GPS receiver operating in an environment of high signal level dynamic range is currently not supported.

Once the design has been debugged to the point where can be tested on the target platform, there are number of useful tests that can be performed. A useful initial test is to configure the slave channel with both WI and SI indices equal. If the slave channel is then configured to use the IF samples from the external FE chip, verification that the slave and master channels have equal I&Q integrate and dump samples can occur. Changing the slave channel to process the regenerated signal should result in outputs that are proportional to the master channel. This can permit inadvertent sign inversions to be identified which can be corrected in software if necessary, something that turned out to be necessary in this implementation.

A more practical test that permits the efficacy of the cancellation to be quantified is a single strong signal cancellation test. This requires the use of a hardware GPS simulator that is configured to output a single strong satellite signal. The receiver is then configured such that one channel tracks the strong signal (SI), a second channel searches for the strong signal with acquisition inhibited (by setting the acquisition threshold high) and a third channel (WI) searches for the strong signal but with mitigation enabled and the acquisition inhibited. The outputs from the second and third channels are then examined, with the desired response being that strong satellite should be easily

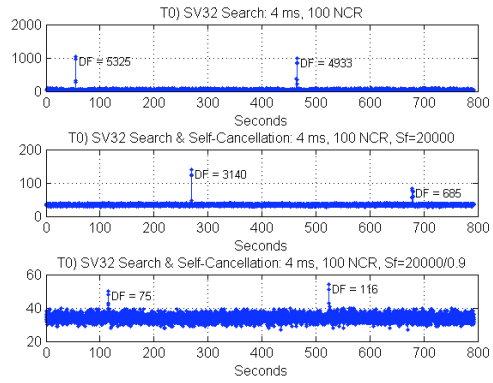

Figure 5: Self-cancellation test with only one signal present. Top row has no cancellation and middle & bottom have cancellation with scale-factors of 20000 and 20000/0.9 respectively

visible in the second and not visible in the third. During these tests, care must be taken to ensure that the searching channels are set to Doppler frequencies that match the tracking channel as closely as possible.

The initial test of this type employed a six channel Welnavigate GS700 GPS simulator running in "low level receiver test" mode. This permits direct control of each of the six simulator hardware channels, one of which was configured to generate SV32 with a Doppler frequency of 0 Hertz, a data navigation message of alternating ones and zeros, parity generation enabled and a power attenuation of 110 dB (GS700) units. This is believed to be approximately -111 dBm, although there are a large number of losses that can be accounted for before processing by the receiver software. These losses include 1.5 dB of noise due to the higher effective antenna temperature caused by use of a GPS simulator [16], 2 dB of cable losses, an estimated 3 dB of ceramic filter insertion loss, an estimated 2 dB of LNA noise figure and 1 dB of bandwidth loss due to use of narrow bandwidth. The amplitude of the tracked signal was slightly less than the maximum of 1050 that is observed when using a roof antenna and live satellites, so this scenario is reasonable.

The output from a test of this type is shown in Figure 5, where both search operations use a 4 ms coherent integration period with 100 non-coherent rounds (NCR). The top plot shows the outputs during a sequential search where it can be seen that without cancellation the strong signal is easily visible with an amplitude of about 1000 and with autocorrelation-sidelobes with an amplitude of 50. In comparison, the middle plot shows the outputs, which are not aligned in code phase to the top plot, having a mean noise floor of about 35 and a signal peak amplitude of 130, with all autocorrelation side-lobes having been removed. It should be remarked that this capability to remove autocorrelation sidelobes may have a practical application, namely improved observation of sea-surface reflected GPS signals as employed for remote sensing

Test	SV	SNR dB-Hz	Pwr dB	Doppler Hz	NavData Hex
1	32	~50	113	0	55555…
	1	~27	136	1000	0
2	32	~50	113	0	55555…
	31	~50	113	0	44444…
	1	~27	136	1000	0
3	32	~50	113	0	55555…
	31	~50	113	0	44444…
	30	~50	113	-1000	22222…
	1	~27	136	1000	0
4	32	~50	113	0	55555…
	31	~50	113	0	44444…
	30	~50	113	-1000	22222…
	29	~50	113	2000	12341…
	1	~27	136	1000	0
5	32	~50	113	0	55555…
	30	~50	113	0	44444…
	30	~50	113	-1000	22222…
	29	~50	113	2000	12341…
	28	~50	113	3000	ABCDA
	1	~27	136	1000	0
6	32	~50	113	0	55555…
	CW	~59	105	-2000	0
	1	~27	136	1000	0
7	32	~50	113	0	55555…
	CW	~59	105	-16000 to 16000 @ +25 Hz/s	0
	1	~27	136	1000	0

Table 3: Test Case Scenarios

applications. The final plot shows the same process, but using scale factor of 20000/0.9 instead, where it can be seen that the leakage has been reduced. The division factor of 0.9 was determined by trial and error and is believed to compensate for the fact the raw IF is band-limited but the regenerated pure IF is not. This hypothesis has not been proven though.

Each peak in the search process has been labeled with a detectabilty factor metric *DF*, which is defined as follows.

$$DF = \frac{(P - Mean(Noise))^2}{Var(Noise)}$$

P is the amplitude of the 'true' signal, *Mean(Noise)* is the mean noise floor and *Var(Noise)* is the noise floor variance. This makes the DF similar to a power signal-to-noise ratio.

FPGA CROSS CORRELATION MITIGATION

Experimental testing of DPIC running on the Namuru Field Programmable Gate Array (FPGA) GPS platform was performed using the GS700 simulator. Table 3 indicates the simulator configuration for each test, where it can be seen that the number of strong signals present has

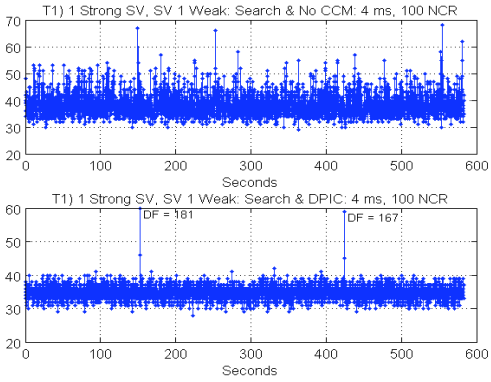

Figure 6: One Strong Signal without & with DPIC

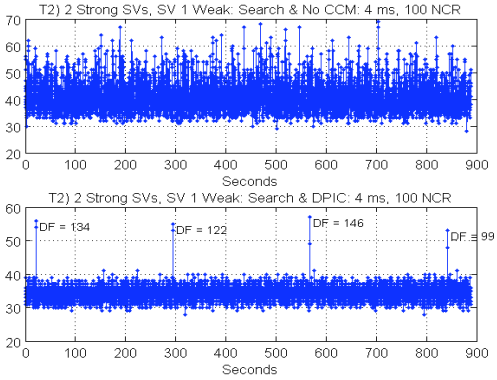

Figure 7: Two Strong Signals without & with DPIC

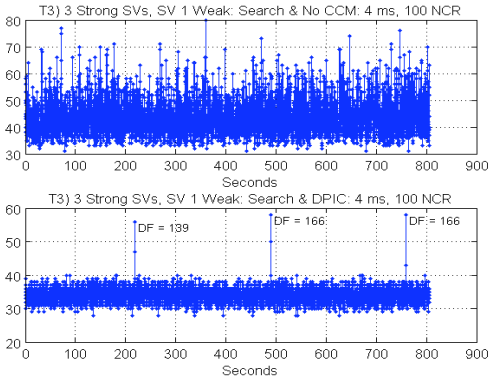

Figure 8: Three Strong Signals without & with DPIC

Figure 9: Four Strong Signals without & with DPIC

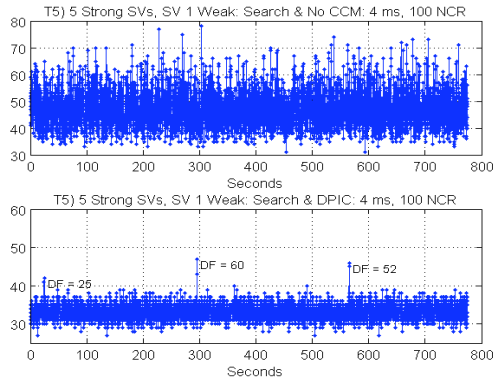

Figure 10: Five Strong Signals without & with DPIC

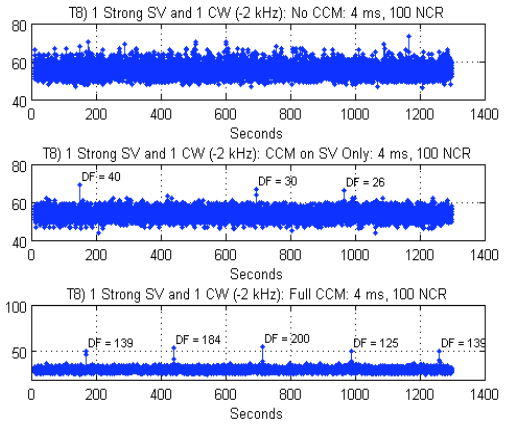

Figure 11: 1 Strong SV & 1 CW (-106 dBm) with no cancellation (top), with cancellation of strong SV only (middle) and with full DPIC (bottom).

been varied in each case. The tests were limited to a maximum of five strong signals and a single weak signal. All cases have the RDC frequency set to a multiple of 1000 Hz, this representing the worst case scenario and all strong signals include data-modulation, although the data-bit patterns vary for each strong signal satellite. The simulator power attenuation in dB corresponds to the value entered into the GPS simulator, where an estimate of the simulated satellite signal strength in dBm is given by:

SignalStrength (dBm) = - Simulator Attenuation (dB) - 1

Unfortunately not much weight can be given to the absolute power level because of the simulator losses already described and due to the fact that the GPS simulator was exhibiting a problem when run at higher signal levels. The problem caused steps in the output power of 3 dB at random times thereby making a comparison of signal detectability difficult. It is for this reason that the simulator was set to produce output amplitudes of about 700 compared to the maximum typically observed values of about 1050 and a manual check on the signal levels was conducted to ensure the problem did not occur.

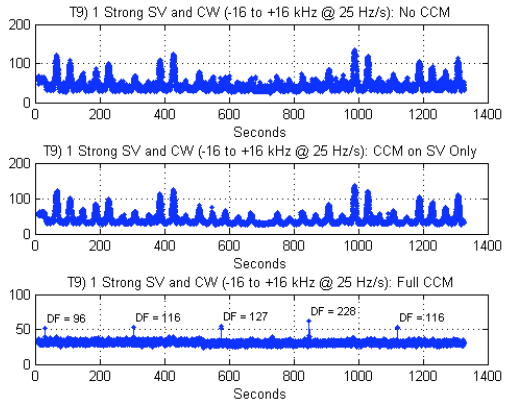

Figure 12: 1 Strong SV & 1 CW (-106 dBm being swept from -16 kHz to +16 kHz at 25 Hz/s) with no cancellation (top), with cancellation of strong SV only (middle) and with full DPIC (bottom). This dataset was affected by an increase in simulator output power of 1.5 dB at t=515 seconds. Zero Hertz from the simulator occurs at t=668 seconds. Notice the line spectra structure of the spread CW in the top two plots.

For each test, a series of RS232 serial port commands was issued to the receiver that were used to configure each of the channels. Each strong signal satellite was allocated a single channel which was permitted to acquire and track, except for one which was duplicated in another channel with acquisition inhibited. This allowed the search process to be observed with a strong signal. The weak signal satellite was allocated to two channels both of which were inhibited from acquiring. One of the channels had DPIC enabled and the other did not thereby allowing the benefits of the DPIC to be illustrated. Debugging output was written to a logic analyzer that was used to capture the results for each hardware channel. This information included NCO Doppler frequency controls and the measured amplitudes on each of the three fingers every 400 ms (4 ms by 100 non-coherent rounds). With 3 half chip separated fingers per channel, it takes 272.8 seconds to scan through the entire 1023 chips so approximately 10 minutes of search data was captured in each case. This allowed sufficient time for at least two detections to be observed. Care was taken to ensure that the TCXO on the Namuru had stabilized therefore allowing the search process to properly tune out frequency offset due to the TCXO. This logic analyzer data was subsequently read into Matlab for plotting and calculation of the detectability factor in each case.

The results of these tests are shown in Figures 6 to 10 corresponding to Tests 1 to 5 respectively. In all cases it can be seen the DPIC has permitted the MAI affected signal to be detected. Although the detectability factor is reduced as more strong signals are added, detection clearly took place even with 5 pathologically bad signals.

FPGA CWI MITIGATION

One of the advantages of DPIC is cancellation of CWI signals can be performed with minor additions to the correlator and software design. The correlator design requires addition of a feature permitting the despreading code to be disabled thereby permitting a full correlator channel to track a CW signal. The software also needs to be modified to disable the code delay locked loop (DLL); running a carrier phase locked loop (PLL) only. The presence of a CW signal was specified by selection of SV 255 which had the effect of setting up the PRN generator for CW signals, disabling code-phase related functions, disabling data extraction and preventing the DLL from running.

To demonstrate this capability, a feature of the GS700 GPS simulator whereby simulator code spreading is not performed when SV 0 is selected was exploited. When the data-message is set to all zeros, this approximates a CW signal except possibly during navigation message segments when the simulator corrects for parity and incrementing Z count. Test configurations that clearly demonstrate problems caused by CW are given by Test 6 and 7 in Table 3. Test 6 contains a single (pseudo) CW signal at a Doppler frequency -2000 Hz and a single strong signal at a Doppler frequency of 0 Hz. Both of these test signals use worst case RDC frequency offsets that are multiples of one kHz, although in the case of the CW a frequency that has a reasonable effect at the weak signal Doppler frequency has been chosen. The results of applying DPIC on this scenario are shown in Figure 11. The plots show the effect of applying no cancellation (top), only cancelling the strong PRN from SV 32 (middle) and cancelling both the strong SV 32 and the CW (bottom). It can be seen that when no cancellation is applied, there are no detections. When only the strong PRN is cancelled, the detection rate is marginal because the presence of the CW signal has substantially raised the noise floor. When all the signals are cancelled the noise floor is reduced and reliable detections are achieved.

Test 7 shows a similar scenario to Test 6, although in this case the CW signal is swept from -16 kHz to +16 kHz at a rate of 25 Hz/s. Since the weak signal search occurs at 1000 Hz, the line structure of the spread CW signal becomes readily apparent. In the time series from the channel applying DPIC to both SV32 and the CW signal, the line structure is not visible thereby proving beyond doubt that CW cancellation has occurred.

DPIC SEARCH ENGINE FEASIBILITY

Many high sensitivity GPS receivers feature massively parallel correlator banks that are capable of searching a significant portion of the code space at several frequency bins. Given that the purpose of such hardware is rapid detection of weak signals that may be subject to cross correlation noise, it is reasonable to consider the feasibility of including DPIC within such a design. This in turn depends on how the search engine itself has been implemented.

In a synthesized search engine (SE) created from a software correlator employing DPIC, it makes sense to build the SE functionality on top of the basic software correlator design. For a software correlator channel providing 32 fingers of code phase, as was the case in [11], the correlator allocated to the SE function is used repeatedly on the same IF input data, but cycles through different code phases and Doppler frequencies. A DPIC enabled SE is therefore implemented by simply replacing the standard correlator with a DPIC correlator plus a number of slave correlators. Linkages between the channels tracking strong signals and the SE are included, as is logic to perform the scaling and subtraction at the end of each weak signal C/A code epoch so as to produce the clean weak signal I & Q samples. The non-coherent accumulation is then performed in the usual way using the clean I & Q samples.

Given a hardware implementation that mirrors the above software implementation, it is clear that construction of a DPIC enabled SE is feasible despite the fact that each strong signal requires its own slave correlator channel (with matching number of fingers) to reconstruct the cross correlation at each code phase. Most likely the design would be limited to a fixed number of slave channels per SE, with one or two being recommended depending on the number of strong signals requiring mitigation. The main factor to bear in mind is that much of the cost involved in the construction of a SE is actually due to the large amount of memory required for the coherent and non-coherent rounds. The computation portion can be reduced through hardware reuse and therefore should not cause difficulties.

CONCLUSIONS AND FUTURE WORK

In this paper, a technique for post correlation cancellation of C/A code multiple access interference (MAI) has been presented. This approach, which we call Delayed Parallel Interference Cancellation (DPIC) requires the use of additional slave correlator channels that are used to calculate in real-time the scaled cross correlation between a pair of weak and strong signals. Use of slave channels permits the effect of signal characteristics such as data-bit transitions and carrier frequency and phase effects to be properly accounted for. The results from the slave correlators are then subtracted from the weak signal correlations after appropriate scaling.

The method is applicable to both hardware and software receivers, with the results presented in this paper being for an FPGA hardware implementation. A hardware implementation such as this greatly increases potential applications for this technology by significantly reducing the any processor loading considerations. The FPGA implementation was tested using signals generated by a WelNav GS700 GPS simulator and clearly demonstrates the ability of DPIC to allow detection of weak signals that are affected by MAI. The technique is also able to remove

CWI interference. These new results are consistent with the software correlation results previously reported.

It should be clear that the reason DPIC works well is that the constructed hardware or software avoids the need for complicated processes when predicting the cross correlations between strong and weak signals. This clearly differentiates DPIC from some other techniques and is inherent in the design of the solution.

Although the principals and operation of DPIC have been properly established, there still remain a number of facets of the process that could benefit from additional study. These include further investigation into the scaling factors required for the cancellation process, with a proper explanation for the 1/0.9 correction being a particular example. A more rigorous examination of the methods of bit-prediction should be performed. The limits of the algorithm are also yet to be determined, with the results presented here focusing on demonstrating the technology.

ACKNOWLEDGEMENT

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