Resistive switching properties of p-type cobalt oxide thin films and devices

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Resistive Switching Properties of p-type Cobalt Oxide Thin Films and Devices

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One of the emerging semiconductor memories, the resistive random-access memory (RRAM), has attracted extensive attention for its application as the next-generation non-volatile memories, due to the excellent characteristics of high-density, high-speed, low-power-consumption and good reliability. Cobalt oxide (CoO), a p-type binary transition metal oxide, has shown good potential as a resistive switching material but has not been extensively studied yet. In this dissertation, we investigated the RS behaviours of the oxide molecular beam epitaxy (OMBE) fabricated CoO thin films and CoO-TiO_2 p-n heterostructures, trying to reveal the RS mechanism in the CoO material system and to find new material structures as good RRAM candidates.

RS performance and mechanism in the OMBE fabricated CoO thin film were studied. It shows bipolar RS characteristic with good endurance and retention performance, showing good potential for RRAM application. A conductive atomic force microscopy (CAFM) writing/reading study reveals the conductive filamentary switching nature in the CoO/Pt memory device.

Growth conditions play a key role in determining the properties of thin films. The impact of oxygen partial pressure during the deposition on the RS behaviour of CoO thin film was studied. A combination of CAFM and Kelvin probe force microscopy study shows that higher oxygen pressure leads to higher conducting filament density in the CoO film, which is attributed to higher defects concentration in this p-type oxide. The RS mechanism in this tip/CoO/Pt memory device can be explained by a novel charge-injection/conductive-filamentary model.

RRAMs with multilayered structure may exhibit different RS behaviour from those with single-layered structure. A CoO/TiO_2 p-n heterostructure memory cell was fabricated and unique nonpolar RS behaviour has been found. Effect of growth temperatures as well as film thickness on the stability of switching parameters, such as cycle-to-cycle ret and reset voltages and resistance at HRS and LRS, have been explored. Growth conditions that result in better RS performance have been suggested.

In summary, the results in this dissertation reveal cobalt oxide's great potential in RRAMs application and provide more evince in understanding the RS mechanisms in this material. In addition, a p-n junction structured RRAM device with unique RS properties is developed.

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ABSTRACT

Conventional semiconductor memories have encountered their limitations for sustained advance in data processing and storage technologies. One emerging memory, the resistive random access memory (RRAM), has attracted extensive attention for its application in the next-generation non-volatile memories, due to the excellent characteristics of high-density, high-speed, low-power-consumption and good reliability. Cobalt oxide (CoO), a p-type binary transition metal oxide, has shown good potential as a resistive switching (RS) material but has not been extensively studied yet. In this dissertation, the RS behaviours in the oxide molecular beam epitaxy (OMBE) fabricated CoO thin films and CoO-TiO_2 p-n heterostructures were investigated by cyclic voltammetry measurement, conductive atomic force microscopy (CAFM) and Kelvin probe force microscopy (KPFM) methods, trying to reveal the RS mechanism in the CoO material system and to find new material structures as good RRAM candidates.

RS performance and mechanism in the OMBE fabricated CoO thin film were studied. It shows bipolar RS characteristic with good endurance and retention performance, showing good potential for RRAM application. A CAFM writing/reading study reveals the conductive filamentary switching nature in the CoO/Pt memory device.

Growth conditions play a key role in determining the properties of thin films. The impact of oxygen partial pressure during the deposition on the RS behaviour of CoO thin film was studied. A combination of CAFM and KPFM study shows that higher growth oxygen pressure leads to higher conducting filament density in the CoO film, which is attributed to higher intrinsic defects concentration in this p-type oxide. The RS mechanism in this tip/CoO/Pt memory device can be explained by a novel charge-injection/conductive-filamentary model.

RRAMs with multilayered structure may exhibit different RS behaviour from those with single-layered structure. A CoO/TiO_2 p-n heterostructure memory cell was fabricated and unique nonpolar RS behaviour has been found. Effect of growth temperatures as well as film thickness on the stability of switching parameters, such as cycle-to-cycle ret and reset voltages and resistance at HRS and LRS, have been explored. Growth conditions that result in better RS performance have been suggested.

In summary, the results in this dissertation reveal cobalt oxide's great potential in RRAMs application and provide more evince in understanding the RS mechanisms in this material. In addition, a p-n junction structured RRAM device with unique RS properties is developed.

LIST OF PUBLICATIONS

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ABBREVIATIONS AND SYMBOLS

RS	Resistive Switching
RRAM	Resistive random access memory
CAFM	Conductive atomic force microscopy
KPFM	Kelvin probe force microscopy
HRS	High resistive state
LRS	Low resistive state

Chapter 1 Introduction

In modern society, computers have become an indispensable part of people's life and work due to their powerful data processing capabilities. Portable mobile electronic devices, such as mobile phones, digital cameras and tablet computers, etc., have brought people with much convenience and enjoyment. Sustained advances in computers and portable mobile electronic devices heavily rely on high-speed, high-density and low-power-consumption semiconductor memories. Dynamic random access memories (DRAMs) and flash memories are most widely used among conventional semiconductor memories. DRAMs are mainly used as the main memory due to its lowest cost and highest density. Flash memories are traditionally used as secondary-memories in personal computers, digital audio players and mobile phones due to the high-density and high-durability characteristics. However, both DRAMs and flash memories have obvious disadvantages. For DRAMs, high power consumption is a critical issue[1]. The memory cells in DRAMs need to be refreshed (recharged) periodically as they always discharge slowly and lose the stored data. The requirement of periodic recharging process makes it consume a relatively large amount of power. For flash memories, low write/read speed and finite write/read cycles are the main challenges. The write/erase time of flash memories is of milliseconds (DRAM <10ns) and the endurance is about 10^5 cycles (DRAM $>10^{16}$)[1]. Therefore, developing new memories, which are high-density, high-speed, low-power-consumption and reliable, are crucial for sustained advancement in the information storage/processing technologies.

In the recent decades, extensive studies have been done to find out alternatives to DRAMs and flash memories. People have been focusing on exploring new memories with more powerful data storage capacities. Among these new memories, magneto-resistive RAM (MRAM), phase-change RAM (PRAM), ferroelectric RAM (FRAM) and resistive RAM (RRAM) are considered as superior candidates to overcome the limitations of conventional semiconductor memories. A comparison of conventional and new memories have been done by Jeong[2]. Each of these emerging memories has its advantages as well as drawbacks. For example, MRAM has fast writ/read operation speed(~10ns) and very good endurance ($>3x10^{16}$cycles), but the minimum cell size is relatively large ($20F^2$, F is the minimum feature size). FRAM also encounters the problem in reducing the minimum cell size ($22\ F^2$), but its operation speed and

endurance performance is good. For PRAM, though minimum cell size($4F^2$) and operation speed (20ns) meet the requirement for new memories, its endurance performance is not very good (10^8 cycles). Among these emerging memories, RRAM has exhibited the greatest potential as candidate for next-generation memories. The write/read speed is very fast (5ns) and its minimum cell size can be reduced to $4F^2$. The endurance cyclability of RRAM has proved larger than 10^{10} cycles[3]. Thus, RRAM has been considered very good candidate for next-generation non-volatile memories (NVMs) and has attracted extensive research attention [4-6].

RRAM is characterized by resistance switching between high resistance state (HRS) and low resistance state (LRS) in a metal-insulator-metal (MIM) structure under applied electrical field. Resistive switching (RS) behaviour has been studied in many materials, such as perovskite oxides [7-9], binary transition metal oxides (TMOs) [10-13], higher chalcogenides [14, 15] and carbon-based materials [16, 17], etc. Though numbers of literatures on RRAMs have been published in the last few decades, the mechanism of RS behaviour has not been fully understood yet. Existence of different RS behaviours in the same material system makes the understanding even more challenging [10, 18-20]. Exploring RS behaviour in different material systems may help gain wider and deeper insight in the understanding of RS mechanisms and thus get better control in fabrication of RRAM devices with better memory storage performance.

Binary TMOs, because of their good compatibility with complementary metal oxide semiconductor (CMOS) process and simple composition and structure control, have gained considerable attention in RRAMs research. Cobalt oxide (CoO) is a binary oxide and has shown promising good potential in RRAM application [21-23]. In addition, cobalt is relatively abundant on the earth and is also an environment-friendly element. All these characteristics make it a good candidate for fabricating next-generation NVMs. However, to date extensive study on the RS properties of this material system is still quite limited. More investigation is needed to fully explore the potential in this material system.

Furthermore, compared to the generally used MIM structure, RRAM devices constructed from p-n heterojunction or multilayered structures sandwiched by two metal electrodes may exhibit excellent resistive switching properties, such as fast switching speed [24], improved switching uniformity[25, 26], good scalability[27] and low power

consumption[28]. Constructing RRAM device with different structures may offer more possibilities for improving the RS properties and may also provide new ways of fabricating RRAM device.

1.1. Objectives

In this dissertation, the RS properties of cobalt oxide thin films prepared by oxygen plasma assisted molecular beam epitaxy (OMA-MBE) technique were investigated. Conductive atomic force microscopy (CAFM) and Kelvin probe force microscopy (KPFM) were used to study the RS behaviour from a nanoscale viewpoint, trying to reveal the RS mechanism in cobalt oxide thin films. CoO-based p-n heterojunction structures were fabricated to explore new RRAM device configurations with unique RS properties. The objective of this project is to explore new material systems with good potential for RRAM application, to provide more insight in understanding the RS mechanism and to develop new RRAM device configurations with unique RS properties.

1.2. Overview

Chapter 1 gives a brief introduction to the current research background RRAMs and objectives of this thesis.

This is followed by Chapter 2, which is a literature review that compares the conventional memories with emerging memories and reviews the fundamental knowledge of resistive switching behaviour, including RS types, RS mechanisms and conduction mechanisms, as well as RS materials.

Chapter 3 is a description of the experimental procedures for fabricating cobalt oxide thin films as well as top and bottom electrodes. The material microstructural and electrical characterization methods are included.

In Chapter 4, bipolar resistive switching behaviour found in cobalt oxide thin films by I-V curves and CAFM current mapping is being discussed. The I-V curves are used to characterize the RS performance of cobalt oxide thin film, such as endurance and retention. CAFM current mapping is used to find out the nature of RS in cobalt oxide thin films.

Chapter 5 is a report of RS properties of CoO thin films under different oxygen partial pressures. The RS mechanisms in the Pt-tip/CoO/LSMO memory device are studied using CAFM and KPFM methods. The effect of oxygen partial pressure on the RS behaviour is explored. A model integrated of conductive filaments and charge injection is proposed to explain the results.

In Chapter 6, the unique nonpolar RS properties of a p-n heterojunction structure fabricated with p-type CoO and n-type TiO_2 are investigated. RS mechanism is discussed based on a conductive filamentary model.

Chapter 7 presents a discussion of the impact of growth temperatures on the RS properties of CoO/TiO_2 p-n junction structure. An optimized growth temperature region is suggested for obtaining CoO/TiO_2 p-n junction memory cells with better RS properties.

In Chapter 8, the effect of CoO layer thickness on the resistive switching stability of Au/CoO/TiO_2/Pt p-n heterojunction structure is investigated. The thickness impact on variation in resistance at HRS and LRS and set and reset voltages is evaluated.

Chapter 9 summarizes the experimental results in this thesis and put up with the future work of this project.

Chapter 2 Literature review

2.1. Limitations of current semiconductor memories

2.1.1. Semiconductor memories

Semiconductor memories play a crucial role in modern computers and portable mobile electronic devices. High-density, high-speed and low-power-consumption semiconductor memories are needed to get people access to computers and portable electronic devices with more powerful processing capability.

Figure 2.1 exhibits the classification of semiconductor memories. Based on the information rewriting times, semiconductor memories can be categorised into two large groups: random access memory (RAM) and read-only memory (ROM). The data write/read cycles are unlimited in RAM; in ROM, however, the write/read cycles are finite. Based on the data retention, semiconductor memories can be grouped into volatile memories and non-volatile memories. The stored information will get lost when volatile memories are powered off. In the non-volatile memories, the information can be stored for a very long time even if the power is off. The most widely used RAMs are Static RAM (SRAM) and dynamic RAM (DRAM), both of which are volatile memories. SRAM's operation speed is very fast but its capacity is low, thus it is suitable for cache memories; DRAM's operation speed is relatively slow but its capacity is very high and is suitable to work as primary storage in computers. The ROMs can be classified into erasable programmable ROM (EPROM) and one-time programmable ROM (OTPROM), based on its re-programmability. EPROMs include electrically erasable programmable ROM (EEPROM) and ultraviolet erasable programmable ROM (UVEPROM), which erases the information by exposing memory to the electrical field and ultraviolet, respectively. Flash memory is developed from EEPROM, and is characteristic for its ability of write/read in blocks or even single machine word. Some novel non-volatile memories, such as ferroelectric memory (FRAM), magnetic memory (MRAM), phase-change memory (PRAM) and resistance memory (RRAM), will be discussed in the later section.

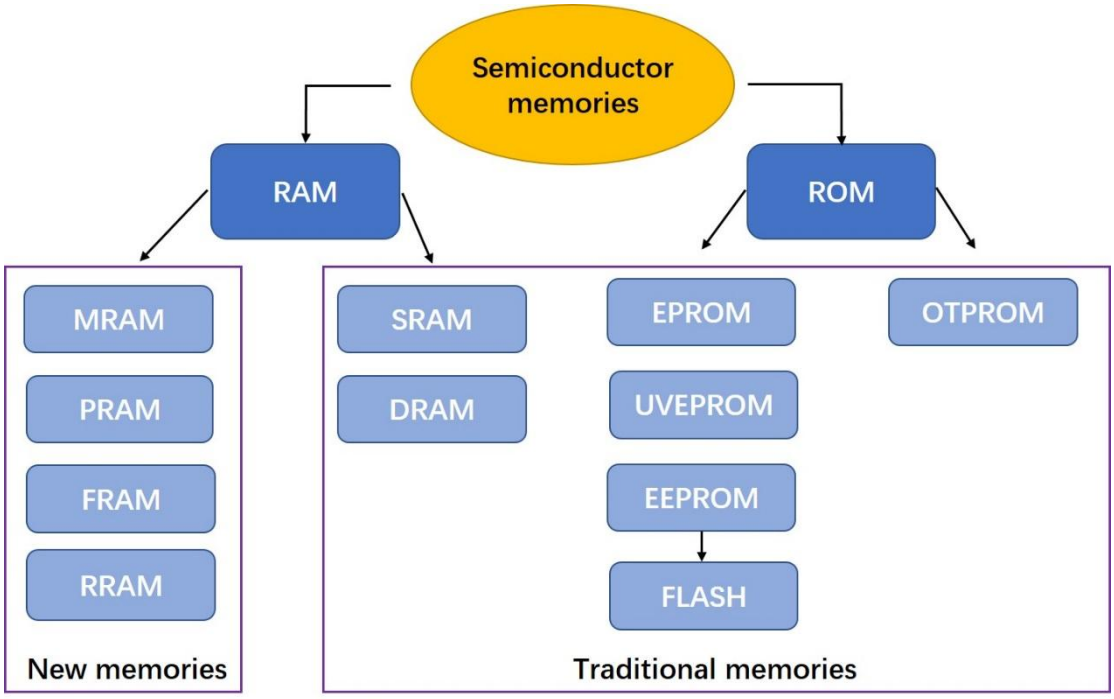


Figure 2-1 Classification of semiconductor memories

2.1.2. Limitations of current memory technologies

Currently, the most widely used semiconductor memories are DRAM and Flash memories. Both memories, however, have encountered their limitations that prevent people from accessing to computers and electronic devices with more powerful processing or storage capability.

DRAM is made of separate capacitors in which each capacitor stores a data bit. The charged and discharged states of each capacitor represent the data bit '0' and '1', respectively. DRAM can be integrated in a very high-density due to its simple structure, so DRAM is a low-cost and high storage capacity memory. DRAM is mostly used as the primary storage in computers. DRAM is a volatile memory as the data fades away fast after the power is cut off. In the practical applications, reducing the power consumption is a critical issue for DRAM[1]. The capacitors in DRAM need to be charged periodically as they always discharge slowly and lose the stored data. The requirement for periodic charging process makes it a large-power-consumption memory.

The flash memory is one type of electrically reprogrammable non-volatile memory. It is usually used as secondary storage in home computers, mobile phones and digital cameras, etc., due to their characteristic of high data-storage density. The high

mechanical resistance and high temperature and pressure withstanding ability make it popular in mobile portable device applications. One of the main disadvantages of flash memory is its finite write/read cycles[29]. Though the design of flash memory is very suitable for 5V operation, they may not work reliably at 0.5V to meet future electronic industry standard. In addition, the reading method in a flash memory can cause nearby cells to be programmed over accumulated reading cycles[30].

Table 2.1 lists the comparison of different semiconductor memories in respect to minimum cell size, write/read time and endurance, etc. The characteristics of emerging non-volatile memories will be discussed in the later section.

Table 2.1 Comparison of different memories. Data are taken from [2]. F stands for the minimum feature size**.**

Type	Volatile		Non-volatile	New non-volatile memories			
	SRAM	DRAM	Flash	MRAM	PRAM	FRAM	RRAM
Cell	Latch	Stack capacitor	Floating gate/charge trap	Magnetor esistance	Phase-change	Polarization change	Resistance change
Minimum cell size	$140F^2$	$6F^2$	$5F^2$	$20F^2$	$4F^2$	$22F^2$	$4F^2$
Write/read time	0.3ns/0.3ns	10ns/10ns	1ms/0.1ms	10ns/10ns	20ns/50ns	10ns/10ns	5ns/5ns
Endurance	$>10^{16}$ cycles	$>10^{16}$ cycles	$>10^5$cycles	$>10^{16}$ cycles	$>10^8$ cycles	$>10^{14}$ cycles	$>10^{10}$ cycles
Application	Cache	Main memory	Storage	Storage	Storage	Storage	Storage /Main memory

2.1.3. Novel non-volatile memories

To break through the limitations of conventional memories (DRAM and flash memories), people have put a lot of efforts in exploring new types of memories based on different principles.

(1) Magnetoresistive RAM (MRAM)

MRAM is a non-volatile RAM in which information is stored in magnetic storage elements[31]. The storage element consists of an insulating thin film sandwiched by two ferromagnetic plates. One plate is a permanent magnet with one particular magnetic polarity and the other plate's magnetization can be changed by the external magnetic field. The resistance of the storage element is different if the magnetization alignments of two plates are different.

As seen in Table 2.1, compared to other memories, MRAM has fast write/read operation (~10ns) and very good endurance ($>3x10^{16}$). In addition, unlike DRAM, MRAM requires less power during operation as no refresh process is needed[32]. The minimum cell size of MRAM, however, is larger than other memories, due to the 'half-selection' problem, which is caused by the overlap of induced field with adjacent cells.

(2) Phase-change memory (PRAM)

PRAM is also a non-volatile RAM. The PRAM materials are usually higher chalcogenide glasses, which can undergo phase transformation between amorphous and crystalline phases under the external electric field[33]. The resistances of chalcogenide glasses at amorphous and crystalline states are different, which can be used as binary '0' and '1', respectively.

According to Table 2.1, PRAM's write/read operation is very fast (tens of ns) compared to flash memories (around millisecond). The minimum cell size of PRAM can be as small as $4F^2$ (F is the minimum feature size), which makes it very superb as high-density memories. The endurance is longer than that of the flash memories, but worse than other memories. PRAM usually requires high programming current density which makes the high power consumption issue a big challenge[34].

(3) Ferroelectric RAM (FRAM)

FRAM is a non-volatile memory based on the ferroelectric polarization reversal effect. The change of ferroelectric polarization direction under external electric field may lead to the change in a ferroelectric's conduction band configuration and thus result in the switch between different resistance states[35].

It can be seen in Table 2.1, the write/read of FRAM is fast (10ns) and the endurance is good (10^{14} cycles). The main problem for FRAM is the limit of scaling down of the cell size. Compared to other memories, the minimum cell size is big. In addition, another problem in size limit is that the material may lose ferroelectric effect when it is too small[36].

(4) Resistance RAM (RRAM)

RRAM is a non-volatile memory that relies on the change of resistance under external electric field. The resistance of material sandwiched between two conductive electrodes can be switched between different states by applied bias.

From Table 2.1, it can be found that RRAM has very fast write/read operation (5ns) and the minimum cell size is the smallest among different types of memories. The endurance is also proved to be good for practical application.

Based on the above comparison among the conventional and novel memories in Table 2.1, it can be found that RRAM seems to possess greater potential for future memories applications which require fast-operation, good-reliability and high-density. The good memory qualities of RRAMs have attracted extensive research interest for next-generation non-volatile memory applications. This dissertation will focus on exploring the properties and potential of RRAM.

2.2. Principles of resistive switching

2.2.1. Types of resistive switching

The resistive switching (RS) phenomenon is a reversible resistance-changing process occurring in a dielectric material sandwiched between two electrodes with the application of an external electric field. The resistance of the insulating layer can be electrically switched between a low resistance state (LRS) and a high resistance state

(HRS). The typical structure of a RS-based memory cell (usually known as resistive switching random access memory (RRAM)) is shown in Figure 2.2.

The most general configuration of a RRAM device is of a vertical structure, as shown in Figure 2.2(a). This capacitor-like structure has a few advantages: it is easy to fabricate and it is also very convenient to apply a large electric field on the dielectric material. With this structure, however, it is difficult to observe the internal structure changes in the dielectric layer during the RS process, unless a sophisticated but destructive method is used. For instance, after the forming/set process, a diamond tip can be used to remove the material and the exposed surface is scanned by CAFM. The 3D shape and size of the conductive elements can be measured in the depth profile [37]. To overcome this issue, an in-plane configuration is developed for direct observation of the microstructural changes in the RS process [38-41], as displayed in Figure 2.2(b).

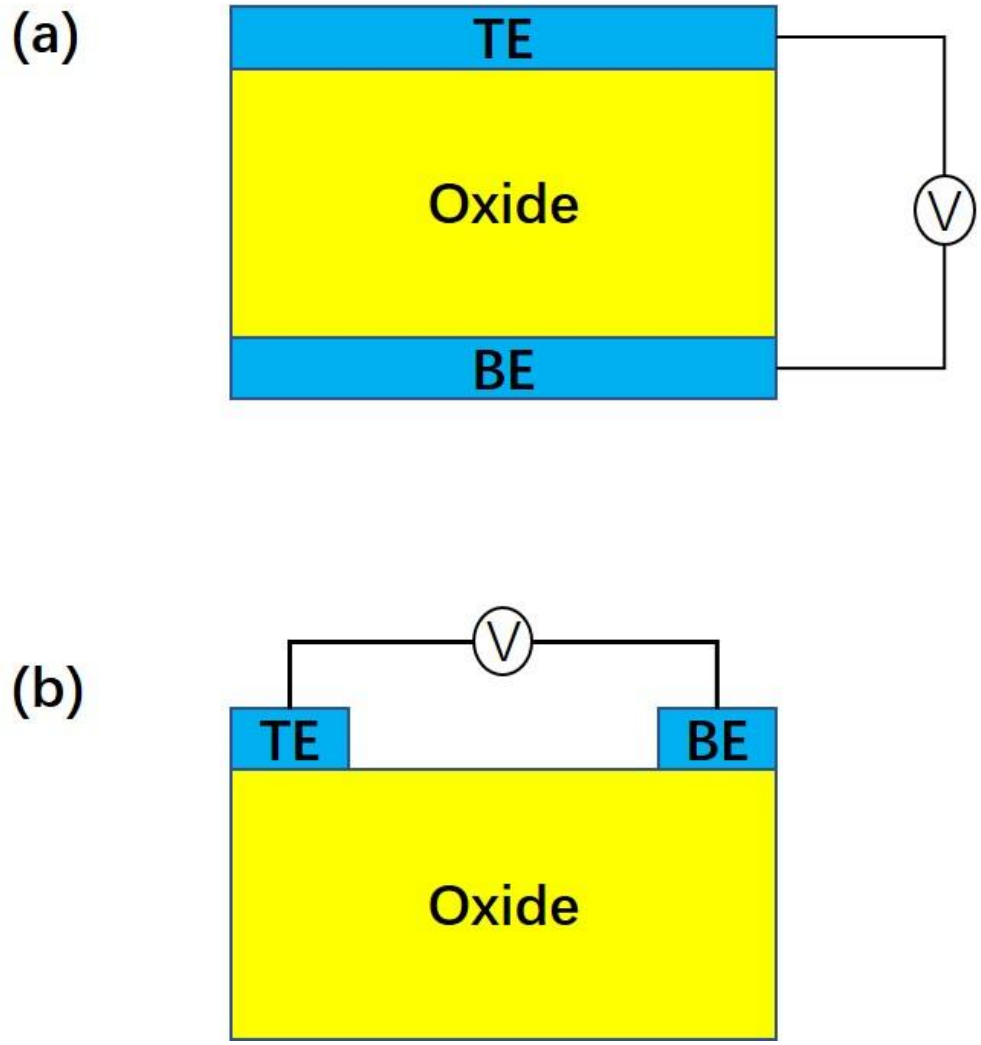


Figure 2-2 Schematics of the typical configurations of RS memory cells: (a) vertical and (b) planar structures. TE and BE stand for the top and bottom electrode, respectively.

Figure 2-3(a) Schematic I-V curves of unipolar RS, (b) Schematic I-V curves of bipolar RS with a figure-of-eight (F8) shape,(c) Schematic I-V curves of bipolar RS with a counter-figure-of-eight (cF8) shape,(d) Schematic I-V curves of threshold RS. Figure has been removed due to copyright restrictions. Figure reproduced from [42].

Resistive switching can generally be classified into three groups: unipolar, bipolar and threshold RS. Unipolar and bipolar RS have two stable resistive states even without exerting the external electric filed. Threshold RS can exhibit multi-resistive states with an applied bias, but if the electric field becomes zero, it shows only one stable resistive state. Figure 2.3 displays the schematics of I-V curves for different types of RS.

(1) Unipolar resistive switching

Unipolar RS refers to the resistive switching process in which only one voltage polarity is needed for RS operation. Figure 2.3(a) shows the I-V curves for unipolar RS. After the forming operation with a large applied voltage, the RS device is switched to LRS. If, for example, a positive voltage is applied to the device, it can be switched to HRS with a sudden decrease in current. This is called reset process. The set process, which will switch the device to LRS again, occurs when applying another positive electric field to the device. It should be noted that similar forming, set and reset process can also occur with negative voltage polarity. It has been found that many materials exhibit unipolar resistive switching behaviour, such as Cu_xO[43], FeO_x[44, 45], NiO[46-50] and TiO_x[51-56], etc. The unipolar RS has the advantages of high memory density, large memory window (high R_{off}/R_{on} ratio) and easy operation.

(2) Bipolar resistive switching

Bipolar RS refers to the switching process in which both positive and negative voltage polarities are required to switch the RS device between LRS and HRS. As shown in Figure 2.3(b) and 2.3(c), the bipolar RS I-V curves have two kinds of shape: “figure-of-eight” (F8) and “counter-figure-of-eight” (cF8). For F8 bipolar RS, positive voltage is required for set process and negative voltage for reset switch. This type of bipolar switching behaviour has been found in many material systems, such as TiO_2[57-59], WO_x[60], ZnO[61-63] and CuO_x[64, 65], etc. For cF8 bipolar RS, negative voltage is needed for set switch and positive voltage for reset process. Many materials exhibit cF8 feather of bipolar RS, such as Cr_2O_3[66], SiO_2[67], Al_2O_3[68] and TiO_x[69, 70], etc. The existence of both F8 and cF8 bipolar RS may be closely related to the film microstructures[42]. The bipolar RS has the advantages in low operation power, fast switching rate and good switching uniformity.

(3) Threshold resistive switching

Threshold RS refers to the switching process in which only one stable resistive state exists if no electric filed is applied. As shown in Figure 2.3(d), a positive (or negative) bias can set the device to LRS, but the device will return to HRS if the applied voltage is lower than a certain value. The threshold RS is not suitable for non-volatile memory application as it cannot maintain two stable resistive states without application of

electric field. But it has potential in applications for electrical switches[71], memory metamaterials[72], and also can be used as selector in RRAM crossbar array[73].

2.2.2. Resistive switching mechanisms

Resistive switching phenomenon has been found in a variety of material systems, such as transition metal oxides[74], silicon oxides[75], polymer and organic materials[76, 77], chalcogenides[78] and graphene materials[79]. The mechanisms for resistive switching, though extensively investigated, are still not fully clarified. On one hand, there are so many RS material systems to find out the exact RS mechanism of each; on the other hand, RS behaviour may be different even in the same material or different RS behaviour may coexist in the same switching material system. For example, unipolar RS has been reported in some TiO_x system[80-82], while many results have also been reported on bipolar RS in TiO_x[83-87]. In some other TiO_x systems, however, coexistence of unipolar and bipolar RS has been found[10, 88, 89].

Despite of the complexity of RS behaviour, the RS mechanisms can be generally classified into two groups: conductive filamentary (CF) switching and non-filamentary switching.

(1) Conductive filamentary switching

Conductive filamentary switching has widely been proposed and accepted as the switching mechanism in many RS systems, especially for unipolar RS. The set and reset process correspond to the formation and rupture of conductive filaments in the film, respectively. Formation (or recovery) of conductive filaments that penetrating the film bulk sets the device from HRS to LRS; and rupture (or dissolution) of these conductive filaments leads to the transition from LRS to HRS. Figure 2.4 schematically exhibits these two processes.

Based on the composition of the conductive filaments, the CF switching can further be grouped into two categories: One is film bulk related. The conductive filaments consist of secondary phase formed during the forming or set process in the film bulk by redox-related chemical effects[81]. The other is related to the active electrode used for conduction contact. The conductive filaments are composed of metallic channels from

the active metal electrodes. Memories based on this CF switching are also called electrochemical metallization memories[90].

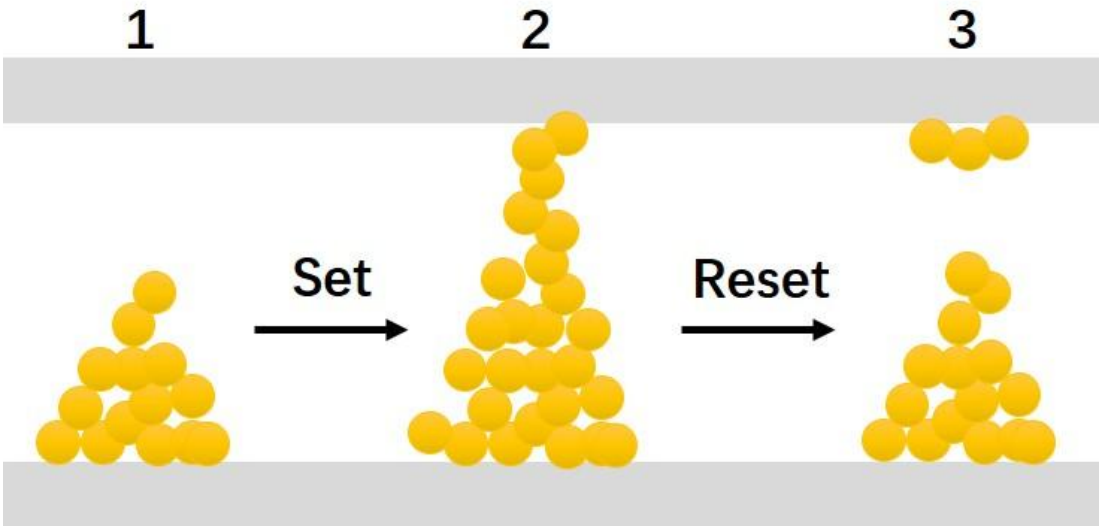


Figure 2-4 Schematics of the formation (stage 1 to stage 2) and rupture (stage 2 to stage 3) of conductive filaments, corresponding to set and reset process, respectively.

1) Film-bulk-related CF switching

The conductive filamentary model was first proposed by Dearnaley[91]. The inhomogeneity in microstructure and composition induced by external electric field may play an important role in the formation of CFs. Under the applied electric field, anodic reaction occurs and the created ionic defects migrate towards and pile up at the cathode. CFs consisting of an ionic-deficient phase grows from the cathode to the anode.

Many transition metal oxides (TMOs) have been found to be resistive switching materials. Based on the intrinsic defect type, TMOs can be grouped into p-type (cation vacancies or oxygen interstitials) and n-type (oxygen vacancies or cation interstitials). In this review, NiO and TiO_2 will be used as examples of p-type and n-type TMOs, respectively, to discuss the CF switching process. Figure 2.5 shows the growth of conductive filaments in the p-type NiO, and n-type TiO_2.

Figure 2-5 Schematics of the growth of conductive filaments in (a) p-type NiO, and (b) n-type TiO_2. Figure has been removed due to copyright restrictions. Figure reproduced from [92]

In NiO, oxygen and nickel vacancy is thought to coexist as inherent defects[93]. As shown in Figure 2.5 (a), under the applied electric field, nickel and oxygen vacancies move towards the anode and cathode, respectively. The concentration of nickel vacancies quickly decreases as lack of nickel vacancy source. The concentration of oxygen vacancies, at the same time, increases at the cathode. The locally oxygen-deficient NiO is thermodynamically unstable and a phase separation may occur with NiO reduced to NiO_x and Ni. The phase separation reaction can be expressed as:

$$Ni_{Ni}^{\times}(NiO) \rightarrow V_{Ni}^{''}(NiO) + 2h^{\cdot}(NiO) + Ni_{(s)}(Ni) \qquad \textbf{Equation 2.1}$$

and

$$V_{Ni}^{''}(NiO) \rightarrow V_{O}^{\cdot\cdot}(NiO) + 2e^{'}(NiO) + 2h^{\cdot}(NiO) \rightarrow null(Ni) \qquad \textbf{Equation 2.2}$$

As the reduction of NiO keeps going, a conductive filament consisting of metallic Ni phase grows from the cathode to the anode. When the CF connects to the anode, the forming or set process completes and the memory cell is switched to LRS. The reset process has been supposed to be the result of CF dissolution induced by Joule heat[4, 94]. The injection current in the set process may heat up the local region to very high temperature. Oxygen ions move from NiO region to the Ni filament by the thermal-assisted-electromigration effect and oxidize the Ni filament[95]. This process will switch the device to HRS again. The Ni filament channels have been observed by high-resolution TEM and electron energy-loss spectroscopy (EELS) in a Pt/NiO/Pt RS memory device[96].

In TiO_2, the major inherent defect is oxygen vacancy[97]. In addition to the inherently contained defects, oxygen vacancies can be produced through the electrochemical reduction occurring at the anode with applied bias:

$$o_{O}^{\times} \rightarrow V_{O}^{\cdot\cdot} + 2e^{'} + \frac{1}{2}O_{2(g)} \qquad \textbf{Equation 2.3}$$

Figure 2.5 (b) schematically shows the growth of CF in a TiO_2-based memory cell. The inherent and electric-field-induced oxygen vacancies move towards the cathode under the applied electric field. As the oxygen vacancies accumulate at the cathode, a secondary oxygen-deficient phase grows towards the anode. Kwon[98] studied the TiO_2 microstructure transformation during RS operation using high-resolution TEM (shown in Figure 2.6). It has been found that cone-shaped CFs consisting of Magnéli phase (Ti_4O_7) involved in the RS process. The formation and dissolution Magnéli phase of correspond to the set and reset process, respectively.

Figure 2-6 Microstructure change after an in-situ reset operation. (a) High-resolution TEM image, diffraction pattern and fast Fourier transformed pattern of the Magnéli phase before reset process. (b) The corresponding images after reset operation. The diffraction pattern shows that the Magnéli phase disappeared after the reset operation. Figure has been removed due to copyright restrictions. Figure reproduced from[98]

From the above discussion, it can be found that RS based on CFs formation and rupture involves the following phenomena: (1) redox reaction introducing or eliminating additional point defects; (2) defects migration under electrochemical and/or thermodynamic effect; (3) secondary phase separation and dissolution.

2) Active-electrode-related CF switching

There is another class of CF switching RRAMs: electrochemical metallization memories (ECMs). This type of memory involves an active metal electrode (Ag or Cu) which dissolves and forms conductive nanofilaments in the RS operation. In recent years, ECMs have gotten extensive research attraction [99-103].

An ECM cell generally has a metal/ion conductor/metal (MIM) structure. One layer of solid electrolyte thin film is sandwiched between an active metal electrode and an electrochemically inert counter electrode. Figure 2.7 schematically exhibits a bipolar RS process in an ECM cell. Without the external electric field, no active metal electrode dissolves in the solid electrolyte film (A). In the set process, when a positive voltage bias is applied to the active electrode, it will dissolve at the anode:

$$Ag \rightarrow Ag^+ + e^- \qquad \textbf{Equation 2.4}$$

Then the Ag ions will migrate through the solid electrolyte film to inert metal cathode under the action of electric field (B). When the Ag ions reach the inert metal electrode, it will deposit on the cathode:

$$Ag^+ + e^- \rightarrow Ag \qquad \textbf{Equation 2.5}$$

This electro-deposition process results in the formation of metal filaments which grow towards the anode (C). When the metal filaments touch the anode, the memory cell is switched to LRS (D). To switch the memory cell back to HRS, a negative bias is needed to electrochemically dissolve the metal filament (E).

Yang[104] has studied the RS operation in an $Ag/SiO_2/Pt$ ECM cell using high-resolution TEM. The formation and dissolution of Ag filaments in the RS process have been observed (Figure 2.8).

Figure 2-7 Schematics of the set ((A)–(D)) and reset (E) process of an electrochemical metallization memory (ECM) cell. Figure has been removed due to copyright restrictions. Figure reproduced from [105].

Figure 2-8 TEM image of $Ag/SiO_2/Pt$ memory cell structure (a)before forming(b)after a writing voltage applied on Ag electrode(c) after an erasing voltage applied on Ag electrode(d) schematic transport of Ag cations and formation of dendrite structure. Figure has been removed due to copyright restrictions. Figure reproduced from [104].

(2) Non-filamentary switching

Different from that in the CF switching materials, the RS in many resistive-switchable material systems may involve no formation and rupture of CFs [106-110]. This is called non-filamentary resistive switching.

Sawa[111] studied the resistive switching behaviour at a $Ti/Pr_{0.7}Ca_{0.3}MnO_3$(PCMO) heterojunction device. It shows hysteretic and rectifying characteristics in the I-V curve, which indicates a formation of Schottky barrier at the Ti/PCMO interface. A Schottky barrier model was proposed to discuss the possible RS mechanism in this device. The

electrochemical migration of oxygen vacancies is supposed to play a key role in the change of Schottky barrier height and width of a depletion layer. When the concentration of oxygen vacancies becomes larger at the interface under a large applied reverse bias, the width of depletion layer gets larger and Schottky barrier becomes higher, the device is switched to HRS. When a forward bias is applied, the concentration of oxygen vacancies becomes smaller at the interface, the width of depletion layer gets narrower and Schottky barrier height becomes lower, the device will be switched to LRS. Figure 2.9 schematically exhibits the electronic band diagrams of the HRS and LRS at the Ti/PCMO interface.

Figure 2-9 Schematics of electronic band diagrams of (a) high resistance state (HRS) and (b) low resistance state (LRS) at the Ti/PCMO heterointerface. Φ_B and W_D is effective Schottky barrier height and width, respectively. Figure has been removed due to copyright restrictions. Figure reproduced from [111].

Chen[112] has used a trapping-assisted tunnelling model to explore the RS mechanism in the Ag/CeO_2/$La_{0.7}(Sr_{0.1}Ca_{0.9})_{0.3}MnO_3$ (LSMO) heterostructure. It is assumed that the PLD-fabricated CeO_2 layer contains two parts: one oxygen vacancies sufficient part at the CeO_2/LSMO interface and the other insulating part close to the Ag top electrode. The CeO_2/LSMO interface forms a Schottky junction. The initial voltage sweeping leads to the trapping of electrons in the impurity bands at the Schottky depletion layer and the film is at HRS. A forward bias will modify the Schottky barrier height and built-in potential and pull the trapped electrons out of the impurity bands. The oxygen vacancies accumulate at the interface and the heterostructure is switched to LRS. A reversing bias can inject the electrons into the impurity band and switch the device to HRS again. Figure 2.10 schematically illustrates this trap-assisted tunnelling model for RS process.

The trap-assisted-tunnelling model has also been used for understanding the RS mechanism in other material systems.[113-115]

Figure 2-10 Schematic band diagram of electronic trapping-assisted tunnelling model for the CeO_2/LSCMO system**.** Figure has been removed due to copyright restrictions. Figure reproduced from [112].

Xia[116] has proposed a space-charge-limited-conduction (SCLC) model to explain the RS process in a Pt/$(Ba_{0.5}Sr_{0.5})(Zr_{0.2}Ti_{0.8})O_3$/Pt memory device. The SCLC conduction characterizes by Ohmic conduction at lower applied bias (I~V) and Child's law conduction at higher applied bias($I \sim V^2$)[117]. Figure 2.11 schematically shows the RS process by a SCLC model. As positive voltage sweeping starts from 0V, the device is in HRS and Ohmic conduction is dominated. As with the increase of voltage (larger than trap filling voltage V_T), the electrons begin to fill in the trap and concentration of free electrons increases, the resistance of the film gets to decrease. As the electron concentration in the film increases with increasing voltage, the sample finally arrives at the LRS. When the voltage begins to sweep inversely, the trap is still in filled state and electron concentration is still high. The sample keeps at LRS. When the voltage comes to the negative region, the detrapping process occurs when electrons can jump over the energy barrier, but the film is still at LRS because of the high electron concentration produced in the previous stage. When the voltage is higher than V_T, electron trapping process happens again. But the injected electrons can contribute to the current directly due to the large activation energy at this voltage region. When the negative voltage becomes to decrease and lower than V_T, electrons cannot fill into the trap and the film comes to a trap-free state. The decrease of electron concentration leads to the increase of film resistance. When it becomes lower than the equilibrium concentration, the film comes to HRS again.

Figure 2-11 Schematic diagram of the SCLC model for resistive switching. In shadowed areas, the electron concentration is higher than the equilibrium concentration. Figure has been removed due to copyright restrictions. Figure reproduced from [116].

The ferroelectric RS memory with a metal/ferroelectric/metal (MIM) structure is based on the ferroelectric polarization reversal effect. The change of polarization direction may lead to the change in a ferroelectric's conduction band configuration and thus result

in the switch between different resistance states. This RS phenomenon has been found in many ferroelectric materials.[118-121]

The major resistive switching mechanisms have been reviewed as above. But as has already been mentioned, the RS phenomenon is so material dependent that the exact RS mechanism must be checked in the specific material system. This may put somewhat difficulty on understanding the RS phenomena and finding RRAMs with great performance.

2.2.3. Conduction mechanisms in RS process

Identifying the conduction mechanisms in the RS set and reset process may play a key role in understanding the switching mechanism in RRAM operation. This may help find out the exact physical conduction mechanism and help find ways to improve the RS performance. Conduction mechanisms vary in different resistive-switchable material systems. The electrode materials, interface between the oxide and metal electrode and oxide microstructures all can affect the conduction mechanisms. The most commonly seen conduction mechanisms in RS process include: (1) Ohmic conduction; (2) Poole-Frenkel (P-F) emission; (3) space-charge-limited-current (SCLC); (4) hopping conduction; (5) Schottky emission; (6) Fowler-Nordheim (F-N) tunnelling conduction.

(1) Ohmic conduction

The Ohmic conduction current results from the movement of electrons in the conduction band or holes in the valence band. The current density is linearly proportional to the electric field. It can be expressed as[122]:

$$J = \sigma E = q\upsilon E N_C \exp\left[\frac{-(E_C - E_F)}{kT}\right] \qquad \textbf{Equation 2.6}$$

In Equation 2.6, σ is electrical conductivity, q is electronic charge, υ is electron mobility, N_C is the effective density of states of the conduction band, E_C is the conduction band, E_F is the Fermi energy level, k is Boltzmann's constant and T is the absolute temperature.

To identify the Ohmic conduction, plotting the I-V curves in a double-logarithmic scale, if the slope is 1, the conduction matches the Ohmic conduction[123, 124].

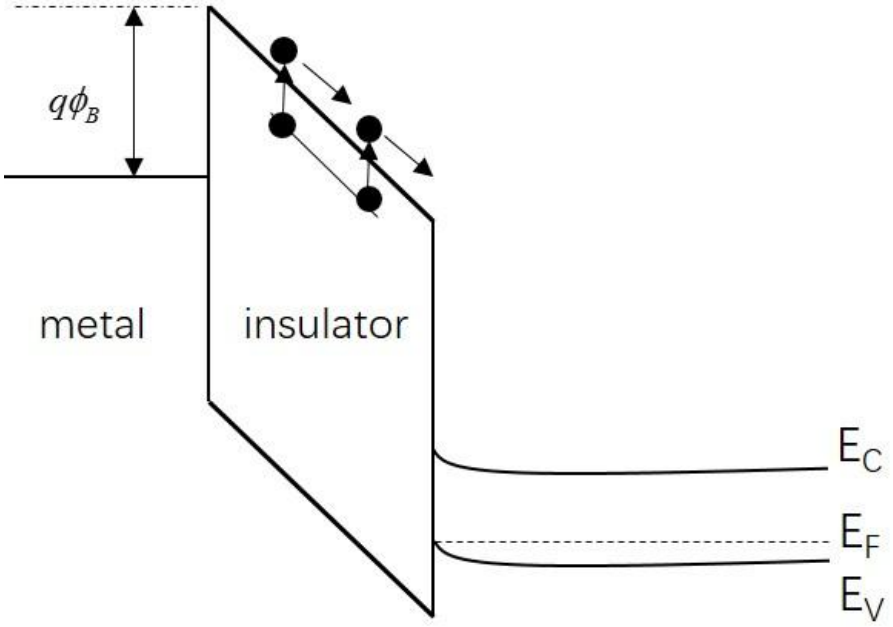


Figure 2-12 Schematic energy band diagram of Ohmic conduction.

(2) Pool-Frenkel (P-F) emission

The Poole-Frenkel (P-F) emission occurs under a certain electric field where electrons at the trapping centre are thermally excited to the conduction band. This conduction is often found at high temperature and high electric field. The current density of P-F emission can be expressed as:

$$J = q\mu N_C E \exp\left[\frac{-q(\phi_T - \sqrt{qE/\pi\varepsilon})}{kT}\right] \qquad \textbf{Equation 2.7}$$

In Equation 2.7, q is electronic charge, μ is the electronic drift mobility, N_C is the density of states in conduction band, E is the applied electric field, Φ_T is the depth of traps potential well, ε is the permittivity of the oxide, k is Boltzmann's constant and T is the absolute temperature[125].

By plotting the I-V curves in a In(I/V) versus $V^{1/2}$ scale, it will present a linear relationship for P-F emission.

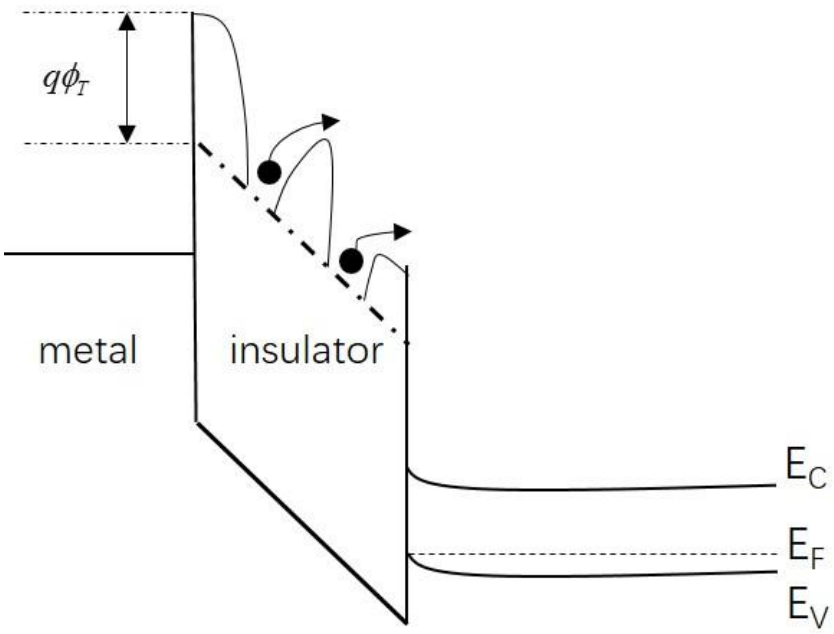


Figure 2-13 Schematic energy band diagram of Poole-Frenkel emission.

(3) SCLC conduction

Space-charge-limited conduction (SCLC) in a solid material is caused by injection of electrons at an Ohmic contact. At lower electric field, where free carrier density by thermal-excitation is larger than that of the injected carriers, conduction follows the Ohmic law. At higher applied bias, the density of injected free carriers increases. The traps are filled up and a space charge layer is formed. The conduction at this stage is space-charge limited and obeys the Child's law ($I \propto V^2$).

By plotting the I-V curves in a double-logarithmic scale, if the slope of the plot at the lower applied voltage is about 1 and slope of the plot at the higher bias is about 2, the conduction in the memory cell matches the SCLC mechanism (Figure 2.14).

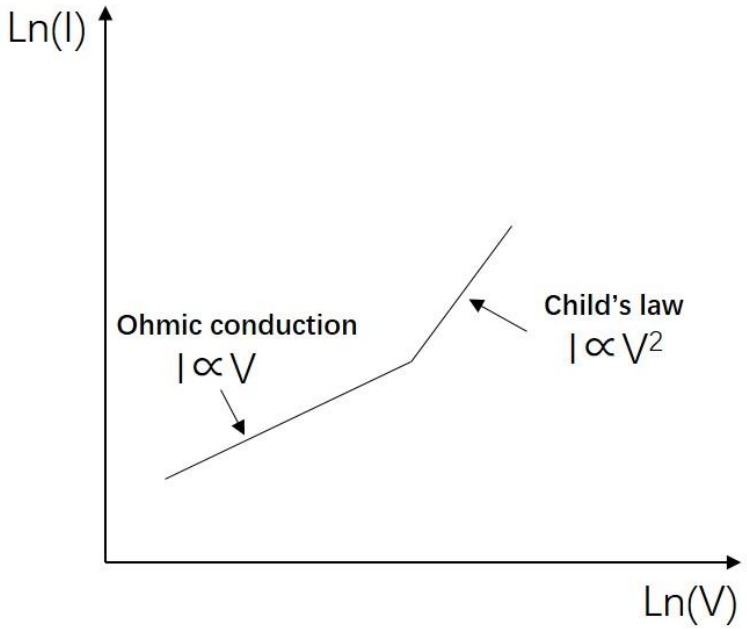


Figure 2-14 A typical current-voltage (*I-V*) characteristic of space-charge-limited conduction current.

(4) Hopping conduction

In hopping conduction, the trapped electrons in dielectric film "hop" from one trap site to another by tunnelling effect. It can be expressed as:

$$J = qan\nu \exp\left[\frac{aEq}{kT} - \frac{E_a}{kT}\right] \qquad \textbf{Equation 2.8}$$

In Equation 2.8, q is electronic charge, a is the mean hopping distance, n is the electron concentration in the conduction band of the dielectric, υ is the frequency of thermal vibration of electrons at trap sites, E_a is the activation energy, E is the electric field, k is Boltzmann's constant and T is the absolute temperature [126].

Different from P-F emission, carriers in hopping conduction cannot overcome the potential barrier height between two trapping sites. But carriers can transit by the tunnel mechanism for conduction (Figure 2.15).

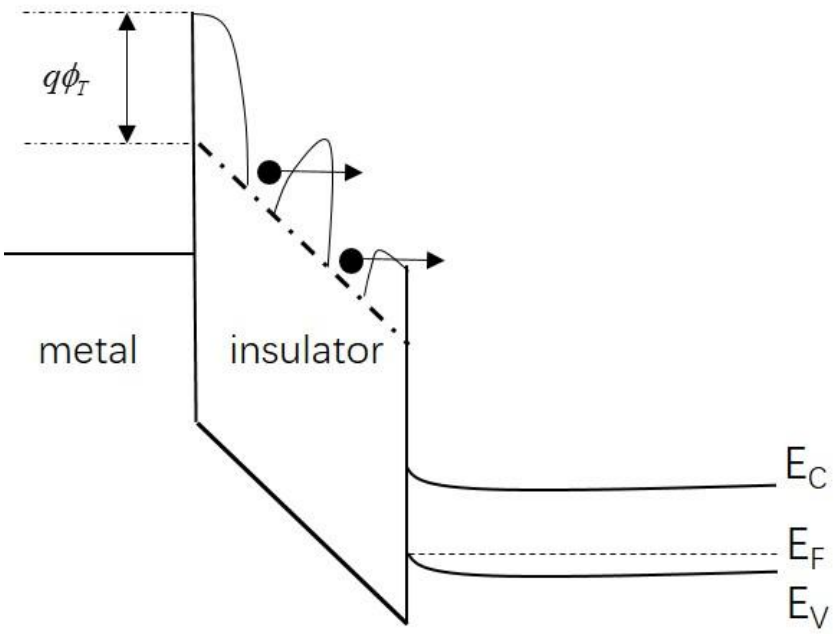


Figure 2-15 Schematic energy band diagram of hopping conduction.

(5) Schottky emission

In a metal/dielectric structure, electrons in the metal side will travel to the dielectric side when they obtain enough energy by thermal activation to overcome the barrier height at the metal-dielectric interface. This conduction is called Schottky emission. The current density can be expressed as:

$$J = \frac{4\pi q m^{*}(kT)^{2}}{h^{3}} \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon})}{kT}\right] \qquad \textbf{Equation 2.9}$$

In Equation 2.9, q is electronic charge, m* is the electron effective mass in the oxide, h is Planck's constant, E is the electric field across the oxide, Φ_B is the junction barrier height and ε is the permittivity of the oxide, k is Boltzmann's constant, T is the absolute temperature[127].

By plotting the I-V curves in the $\ln(I/V^2)$ versus $V^{1/2}$ scale, it will present a linear relationship for Schottky emission. This can be used to identify the Schottky emission conduction.

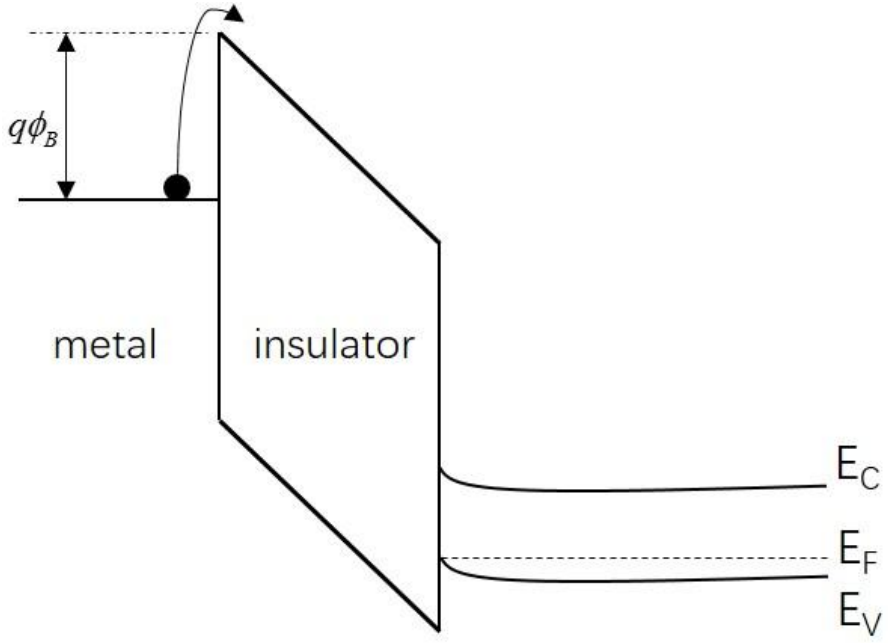


Figure 2-16 Schematic energy band diagram of Schottky emission.

(6) Direct tunnelling and Fowler-Nordheim (F-N) tunnelling

Depending on the thickness of the oxide thin films, the gate current can be categorized as either direct tunnelling or Fowler-Nordheim (F-N) tunnelling conduction. When the film is very thin, the electrons can travel across the film and the conduction is direct tunnelling. When the film is thick, the electrons can still travel across gate oxide by means of quantum mechanism effect and this conduction is F-N tunnelling. The current density of direct tunnelling can be expressed as:

$$J \approx \exp\left[\frac{-8\pi(2q)^{1/2}}{3h}(m^*\phi_B)^{1/2}\kappa t_{ox,eq}\right] \qquad \textbf{Equation 2.10}$$

In Equation 2.10, q is electronic charge, m^* is the tunnelling effective mass in dielectric, h is Planck's constant, E is the electric field across the oxide, Φ_B is the junction barrier height, κ is the relative dielectric constant of the oxide layer and $t_{ox,eq}$ is the equivalent oxide thickness. [128]

The current density of F-N tunnelling can be expressed as:

$$J = \frac{q^3E^2}{8\pi hq\phi_B}\exp\left[\frac{-8\pi(2qm^*)^{1/2}}{3hE}\phi_B^{3/2}\right] \qquad \textbf{Equation 2.11}$$

In Equation 2.11, q is electronic charge, m^* is the tunnelling effective mass in dielectric, h is Planck's constant, E is the electric field across the oxide, Φ_B is the junction barrier height. [127]

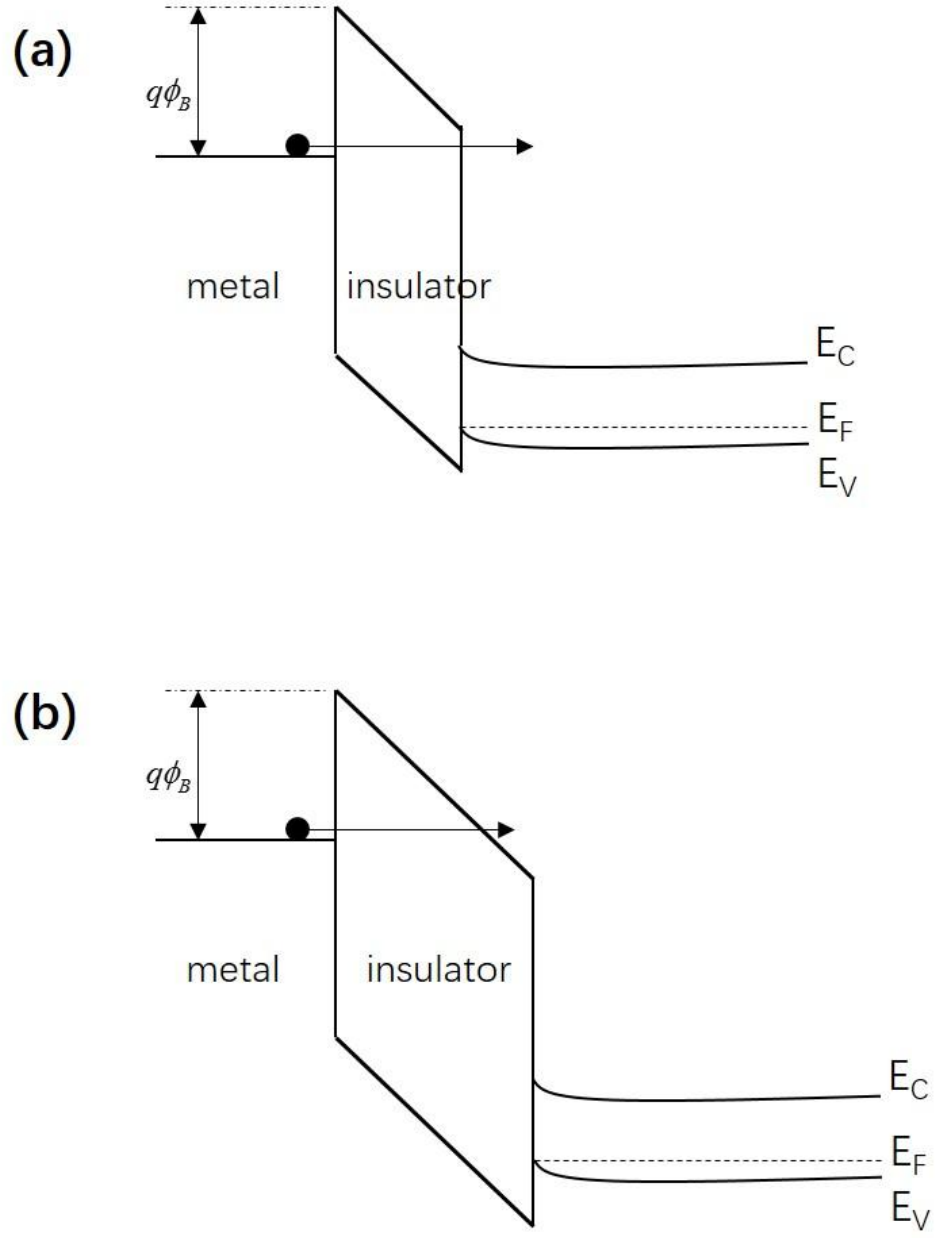


Figure 2-17 Schematic energy band diagram of (a) direct tunnelling and (b) Fowler-Nordheim tunnelling.

2.3. Materials for resistive switching application

Though resistive switching mechanisms in different materials are still not well understood, people have kept exploring new RS material systems that may lead to findings in new RS phenomena and better performance in RRAM devices. RS has been observed in a variety of materials, such as oxides, higher chalcogenides and graphene materials, etc.

2.3.1. RS in oxide materials

RS phenomenon has been found in various oxide materials, including binary metal oxides and perovskite oxides, etc.

(1) RS in binary metal oxides

The binary metal oxides have attracted much attention in application as RRAM materials. They have several excellent characteristics for RRAM application, for example, a simple composition and compatibility with complementary metal-oxide semiconductor (CMOS) process.

Al_2O_3, which is a high-κ dielectric oxide with large band gap (>7.0 eV)[129], has received extensive investigation on its resistive switching properties[130-135]. Different RS types are found in different Al_2O_3 based memory devices. Unipolar RS behaviour is found in Pt/ Al_2O_3/Ru memory device[135] and a bipolar RS characteristic is observed in a Ti/Al_2O_3/Pt structure[130]. In a Pt/Al_2O_3/TiN memory cell, coexistence of unipolar and bipolar RS is found[131]. The different RS behaviour may come from the different fabrication method, as well as different metal electrodes used. Hubbard [133] studied the formation and regeneration of Cu nanofilaments during switching in a Cu/Al_2O_3 electrochemical metallization memory cell using in-situ TEM method. This reveals Al_2O_3 as an effective solid electrolyte for ECM memories.

Cobalt oxides based RRAMs have been studied by several groups. Nagashima[136] demonstrated the multistate bipolar RS in a single Co_3O_4 nanowire, which shows great potential as next-generation non-volatile memories with the ultimate size limit. Younis[23] developed an electrochemical deposition method for fabricating high-quality Co_3O_4 nanosheets which exhibit excellent resistive switching performance. This experiment demonstrates two dimensional nanosheets as good-potential RRAM

materials. Shima[13] and Kwak[22] studied the post-annealing effect on the unipolar RS properties of CoO_x thin films. These experiments implied that intrinsic defects (Co vacancies in this case) play an important role in the RS process. Kawabata[137] presented the process integration and device technology for a CoO_x-based RRAM 128Kbits memory array. It was found that the film quality has a very strong impact on the resistance of CoO_x film and its quality. The basic writing and reading operation of the 128Kbit memory array was demonstrated.

RS behaviour in CuO_x has also been studied[138-140]. Fujiwara[40] observed the formation of a conductive bridge during the forming process in a planar metal/CuO/metal memory device, see Figure 2.18. The results demonstrate that the reduction and oxidation of the conducting bridge is responsible for the RS operation. Park[141] synthesized Ni/CuO/Ni nanowires on anodized aluminium oxide membrane template. The Ni/CuO/Ni nanowire devices exhibit a self-compliance bipolar RS behaviour and may have applications in highly scalable memory and neuromorphic devices.

Figure 2-18 SEM image of the formation of a single conductive bridge (a)before and (b) after the forming process in a Ni/CuO/Ni memory device. Figure has been removed due to copyright restrictions. Figure reproduced from [40].

Study on FeO_x based RS memory devices is relatively rare[142-145]. Yun[144] fabricated an Au/α-Fe_2O_3/Pt memory device in an oxygen-sufficient atmosphere. The device exhibits a bipolar resistive switching characteristic and an obvious difference in the transport and magnetic property between HRS and LRS is observed. An enhanced electron hopping between Fe^{3+}-Fe^{2+} pairs and Fe^{3+}-O- Fe^{2+} double exchange coupling effect is referred to be the reason for enhancement in conductivity and magnetization.

HfO_x based RS memory devices exhibit good RS performance[12, 113, 146-153]. Yu[146] and Chen[150] have fabricated HfO_x based vertical RRAM which shows fast switching speed, low reset current and good switching endurance. In their work, a cost-effective fabrication process that requires only one critical lithography step or mask was used to build a three-dimensional cross-point array, see Figure 2.19. Govoreanu[148] fabricated a 10x10nm^2 Hf/HfO_x crossbar RRAM device with fast switching speed, high

switching reliability and low operation energy. Their results suggest HfO_x based RRAM a good candidate for ultra-high-density, low operating energy and high stability non-volatile memory application.

Figure 2-19 Schematic of the proposed 3D cross-point architecture using the vertical TiN/HfOx/Pt RRAM cell. Figure has been removed due to copyright restrictions. Figure reproduced from [146].

MnO_x has also been investigated on its RS performance[11, 154-158]. Koza[156] fabricated Mn_3O_4 thin films by an electrodeposition method. The crystallinity of the as-deposited film varies with the applied voltage. The Au/Mn_3O_4/AuPd memory cell shows a unipolar RS behaviour with a large memory window (>10^6) and long retention time, indicating great potential for non-volatile memory application. Zhang[11] found unipolar RS behaviour in the Pt/MnO_x/Al memory device and explained the RS mechanism using a conductive filamentary model. Yang[158] demonstrated a bipolar RS behaviour in the TiN/MnO_2/Pt cell, which possesses characteristics of low power operation, good endurance and reliable data retention. The TiN top electrode is believed to work as an oxygen reservoir that can offer enough non-lattice oxygen ions to recover the oxygen vacancies produced during the reset process, which will maintain good switching endurance.

NiO is one of the most extensively studied materials for RRAMs[159-167]. Gibbons[168] found resistive switching behaviour in nickel oxide and he proposed that the formation and rupture of nickel metallic filaments in the NiO matrix lead to the RS process. NiO RRAMs usually exhibit unipolar RS behaviour. Chang[169], however, found the occurrence of both unipolar and threshold RS in the NiO thin film. The unipolar RS occurs at low temperatures and threshold RS at high temperatures. They proposed a dynamic percolation model to explain these RS phenomena and achieved to control the switching type by thermal cycling. Oka[166] reported non-volatile bipolar resistive switching in a single crystal NiO nanowire for the first time, which open up opportunities to explore next-generation high-density integrated non-volatile memories.

TiO_2 is also among the most widely studied materials for RS memories[55, 58, 69, 98, 117, 170-173]. As has been mentioned in previous section, both unipolar and bipolar

have been found in TiO_2 based RRAM. For instance, unipolar RS has been reported in some TiO_x systems[80-82], and bipolar RS are reported in other TiO_x[83-87]. And in some other TiO_x systems, coexistence of unipolar and bipolar RS has been found[10, 88, 89]. TiO_2 can be used not only as a RS material, but also as a selection diode material for suppressing the sneak current in RRAM devices. Park[170] used $Pt/TiO_2/Ti$ as a selection device in the RRAM cross-bar. It is found that this Schottky-type diode can effectively alleviate the sneak current without adverse interference in the RRAM cross-bar array.

WO_x thin films have been used to fabricate RRAM cross-bar array[174-176]. Ho[177] succeed to fabricate 9nm half-pitch RRAM cells with a very low programming current of 1μA. Their results show good potential for high-density and low-power-operation RRAM application. Lee[178] reported bipolar resistive switching in a WO_x/Au core-shell nanowire device array. The device not only shows good RS performance but also present a super-hydrophobic property, which can protect the device from failure caused by water contact (see Figure 2.20).

Figure 2-20 Digital images of patterned device states before, during and after submergence in water. The inset I-V curve shows that the memory device can still work even after submerged in water. Figure has been removed due to copyright restrictions. Figure reproduced from [178].

(2) RS in perovskite oxides

Resistive switching behaviour has been found in various perovskite-type TMOs, such as $SrTiO_3$[8, 110, 179], PCMO[180], $SmNiO_3$[181], and $BaTiO_3$[182], etc[183, 184]. RS in perovskite-type TMOs is usually of bipolar characteristic. The RS mechanisms in perovskite TMOs with different functionalities may be different.

Choi[185] studied the bipolar resistive switching behaviour in the paraelectric $SrTiO_3$ thin film. The RS mechanism was explained with a ‘trapping-detrapping’ model. The conductivity at the top layer of the $SrTiO_3$ thin film is lower than the bulk after a post-annealing process. Traps (intrinsic defects) at the top layer interface are filled with electrons and the film is in HRS. When the applied bias reaches the set voltage, the electrons will be removed from the traps, the film is set to LRS.

Pantel[120] explored the resistive switching in ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ thin film using conducting force microscopy and piezoelectric force microscopy. The result shows that the resistance state and ferroelectric polarization direction are unambiguously correlated. Recently, Lu[186] has fabricated well-ordered and high-density nano memory cell arrays based on continuous $BiFeO_3$ thin film and isolated Pt nanoelectrodes. These nano memory cells achieve a large memory window ($>10^3$) and reliable retention performance, showing great potential for high-density data storage application.

Resistive switching can also occur in manganese oxides with a perovskite structure (manganites). Asamitsu[187] has shown that switching of resistance state in PCMO can be solely achieved by an electric filed without application of magnetic field.

2.3.2. RS in higher chalcogenides and other materials

Many higher chalcogenides, including sulphides[188-192], tellurides[193-196] and selenides[197, 198], have been found to be resistive switchable materials. Sulphides usually work as a solid electrolyte in an active metal/sulphides/inert metal RS memory cell. Xu[188] studied the RS process in a $Ag/Ag_2S/W$ memory cell with in-situ high-resolution TEM technique. The formation and rupture of a nanoscale conductive path consisting of a conducting argentite phase and a Ag nanocrystal was observed in real-time. Electrical switching effect has been found in some telluride glasses. Rajesh[199] studied the memory switching behaviour in In-Te glasses and their heat-transport experiment supports the thermal model that explains the memory switching behaviour. The steady state of the material will get thermal breakdown by the generated Joule heat, which will switch the device to LRS. The selenides can also serve as a solid electrolyte in an ECM cell. Schindler[198] studied the resistive switching in Ag-Ge-Se material. The Ag/Ag-Ge-Se/Pt memory cell exhibits a very large resistance ratio of five orders of magnitude and extremely low writing current of 1nA. The RS mechanism can be explained by the formation and dissolution of Ag metal filament in the film bulk.

Resistive switching has been found in graphene oxides (GOs) materials[16, 200-205]. The application of metal oxides based RRAMs to large-area flexible substrates has been limited due to the general high-temperature fabrication process. A graphene oxide based RS memory cell, however, can be easily produced at room temperature and on large-area flexible substrates with a spin-coating method. Jeong[17] revealed the microscopic

nature of the bipolar RS behaviour in a Al/GO/Al memory device. The high-resolution TEM and in-situ XPS measurement shows that the formation and rupture of CFs at the top interface layer between GO and Al electrode is responsible for the bipolar RS process. Zhuge[201] used the conducting atomic force microscopy (CAFM) technology to study the RS property of a GO/Pt structure. The RS behaviour was explained by the redox reactions of GO induced by the adsorbed water. A positive voltage can oxidize the adsorbed water into hydrogen ions which may play a role in reducing the GO. The reduced GO will be switched to LRS. A negative voltage will oxidize the GO to HRS again.

2.3.3. RS in multilayered structures

The most commonly seen structure of a RS memory cell is a metal/insulator/metal (MIM) configuration. Over the past few decades, extensive research has been done on the RS behaviour of MIM-structured memory cells and good RS performance has been achieved in some RS memory devices. Meanwhile, a lot of efforts have been put into exploration for RRAMs with multilayered structures, such as bilayers[25, 26, 206-213], superlattices[214-216] and metal embedded active layer[217-223], in order to find RRAMs with better switching properties.

People have fabricated many RRAM devices with bilayer-structures, trying to solve the problems in single-layered memory cells, such as non-uniformity of set and rest voltages and wide HRS or LRS resistance distribution. Improvement of uniformity of resistive switching parameters has been achieved in many bilayer-structured RS memory devices. Ye[25] has fabricated a Pt/HfO_2/TiO_2/ITO memory cell with lower and more uniform switching voltages than those in Pt/HfO_2/ITO device. The inserted TiO_2 layer is thought to act as an oxygen reservoir for reducing the switching voltages and the enhanced uniformity is attributed to the connection and rupture of conductive filament at the interface of the HfO_2 and TiO_2. Sadaf[206] found highly uniform and reliable RS in a WO_x/NbO_x bilayer memory device. The CFs connect and break at the interface between WO_x and NbO_x. Strong conductive filaments are formed in the thicker NbO_x layer, served as lighting rods, from which small and weak CFs grow. This will help reduce the randomness of filament formation and rupture.

Bilayer-structured RRAM cells composed of a p-type oxide and a n-type oxide have also been fabricated[24, 27, 224-228]. Resistive switching in these p-n heterojunction

memory cell characterizes by transition between rectifying and Ohmic conduction. Zheng[27] studied the resistive switching in a GaO_x-NiO_x p-n heterojunction structure. The p-n junction barrier controls the connection and rupture of CFs at the GaO_x-NiO_x interface which result in the RS process. Kim[24] fabricated a NiO/TiO_2 p-n heterostructure and found that the reset time can be dramatically reduced.

Resistive switching study on superlattice structure is rare. Jammalamadaka[214] fabricated ultra-thin $La_{0.7}Sr_{0.3}MnO_3$/$SrRuO_3$ superlattices and studied RS property of this hybrid structure. The bipolar resistive switching behaviour was found in the $La_{0.7}Sr_{0.3}MnO_3$/$SrRuO_3$ superlattices memory device with a planar configuration. This work shows the potential of superlattices in the next generation electronic devices.

Metal embedded method has attracted extensive research interest for improving the reliability of RRAMs. A variety of metal nanocrystals (Pt, Au, Mo, Cr, Al, etc.) have been used in RS materials. Guan[217] fabricated RS memory devices with gold nanocrystals embedded ZrO_2. Three multilayers of ZrO_2/Au/ZrO_2 were sequentially deposited on the substrate, after which the sample was annealed in nitrogen atmosphere at high temperature to introduce gold nanocrystals in the ZrO_2 matrix. Good RS performance was achieved in this metal-embedded memory device. The embedded gold nanocrystal is thought to provide more uniformly distributed trap centres in the ZrO_2 film, which can help improve the uniformity of switching parameters. Active metal nanocrystals, such as Mo[221] and Cr[223], are considered as oxygen getters, which provide more oxygen vacancies in the film bulk and thus enhance the oxygen-vacancy-assisted filament formation. One drawback of this metal embedded method is the necessity of high-temperature annealing process to induce the formation of metal nanocrystals.

2.3.4. Summary

Based on the above survey of materials for RRAMs, cobalt oxide (CoO) is chosen as the RS material in this dissertation.

Firstly, CoO is a binary transition metal oxide with simple crystal structure and composition, which is easy for fabrication. Besides, cobalt is also an environment-friendly and relatively abundant element on the earth.

Secondly, Reports on the RS mechanisms of p-type semiconducting materials are relatively limited. In n-type oxide semiconductor RRAMs, such as TiO_2, the formation and dissolution of a metallic second phase is thought to be the mechanism for resistive switching process. And recently, an in-situ high resolution TEM imaging has clearly shows that formation and disappearing of Magneli phase during the set and reset operation in the resistive switching process of TiO_2. The RS mechanism in p-type oxide semiconducting material system is still unclear. NiO is the most extensively studied p-type binary transition metal oxide for RRAMs. Though many people explained the RS process with the formation and dissolution of conductive Ni metal filaments, the difficulty in imaging the nano-sized metal filaments with high resolution imaging may impede the understanding its the resistive switching mechanism. Studying RS in p-type CoO may provide more evidence to reveal the resistive switching mechanism of p-type semiconducting materials.

Finally, many efforts have been put into the exploration for RRAMs with multilayered structures, such as bilayers, supperlattices and metal embedded active layers. Uniform set and rest voltages variation and narrow HRS or LRS resistance distribution has been achieved in many bilayer-structured RS memory devices. The devices with superlattice structure demonstrate a promising potential for applications of next generation solid-state memories. Active metal nanocrystals, are considered as oxygen getters, which provide more oxygen vacancies in the film bulk, thus enhancing the oxygen-vacancy-assisted filament formation. Exploring the RS behaviour of CoO-based multilayer-structured RRAMs may provide more ways to develop the unique RS properties and also offer new approaches to fabricate RRAM devices.

Chapter 3 Experimental Procedures

3.1. Fabrication of memory cells

The CoO-based RRAM devices in this dissertation have a capacitor-like structure, as shown in Figure 3.1. The bottom electrode, cobalt oxide thin films and top electrode are deposited on the substrate successively.

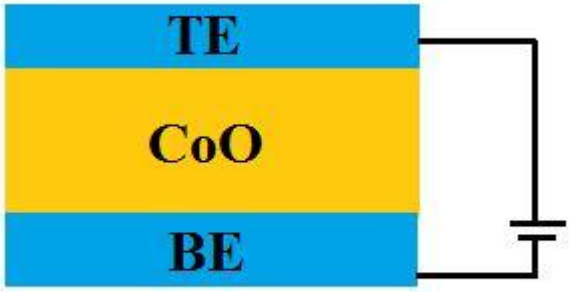


Figure 3-1 Schematic of our CoO-based RRAM structure

3.1.1. Bottom electrode fabrication

Two kinds of bottom electrodes have been used in our experiments: Pt and $La_{0.7}Sr_{0.3}MnO_3$(LSMO). To make Pt electrodes, SiO_2 (50nm), Ti (20nm) and Pt (100nm) layers are successively deposited on the Si (001) substrate with a Kurt J. Lesker PVD-75 system at room temperature. SiO_2 and Ti layers serve as a Pt adhesive to the silicon substrate. LSMO bottom electrode layer is deposited by pulsed laser deposition (PLD) on the $SrTiO_3$ (001) at a substrate temperature of 800 ℃ under an oxygen partial pressure of 10 mTorr[229].

3.1.2. Oxide thin films fabrication

Oxide thin films in this dissertation are deposited on the bottom electrodes with an oxygen-plasma-assisted molecular beam epitaxy (OPA-MBE) system (DCA M600). First, the substrate is transferred and fixed on the manipulator in the main growth chamber. Then, the substrate is heated to the required growth temperature and held until the chamber pressure is pumped to a high vacuum level (chamber pressure $<10^{-7}$ Torr). Next, ignite oxygen plasma and tune plasma power to 300W. Oxygen gas is introduced

into the chamber through a leak valve. Next, set effusion cell temperatures to the required values. When all the temperatures and chamber pressure are stable, open the plasma and effusion cell shutters simultaneously and the deposition process begins. After the film growth finishes, close plasma and effusion cell shutters. The specific deposition parameters will be listed in the experimental section of each chapter.

The DCA M600 system is versatile MBE system for oxide epitaxy. Figure 3.2 shows the schematic configuration of the main growth chamber. The chamber has a vertical configuration with 10 upward-facing source ports (2 electron-beam evaporators and 8 Knudsen effusion cells). The downward-facing substrate manipulator is located along the central axis of the chamber and allows substrate temperature up to 1000 ℃. Atomic oxygen can be generated by a plasma power source with a radio frequency of 13.56MHz at 300W. Molecular ultra-pure oxygen gas is delivered to the plasma power source through a leak valve. The flux of metals out of the effusion cells and atomic oxygen flux out of plasma source can be controlled by the linearly activated shutters. The MBE system is also equipped with a cryopump and liquid-nitrogen cooled cryo-panels, which allows the system base pressure down to 10^{-11} Torr.

Figure 3-2 Schematic of OPA-MBE system configuration. Figure has been removed due to copyright restrictions. Figure reproduced from[230].

This MBE system is equipped with reflection high-energy electron diffraction (RHEED), which is located at a very small glazing angle (~1 °) towards the substrate surface. Due to the very small glancing incidence, RHEED is very sensitive to the structure changes in the top few atomic layers of thin films. Thus, it can be used in monitoring the surface structure as well as surface roughness of deposited thin films, as shown in Figure 3.3 (a) and (b). In addition, the RHEED intensity oscillations can be used to monitor the development of thin film thickness. As seen in Figure 3.3 (c), in the layer-by-layer growth mode, one RHEED intensity oscillation refers to the completion of one monolayer deposition (where the coverage rate on the growing surface is 1).

Figure 3-3 RHEED diffraction patterns of (a) rough surface and (b) smooth surface; (c) schematic of the relation between RHEED intensity oscillation and film coverage rate. Figure has been removed due to copyright restrictions. Figure reproduced from [230]

Quartz crystal microbalance (QCM) (INFICON SQM-160) is installed in the main growth chamber to measure and monitor the metal flux of each source (Figure 3.4). Knowing the metal flux is crucial for the growth of complex oxide thin films, in which the exact ratio of each element must be known. Monitoring the metal flux can also help know when to refill the metal source before it runs out. As the QCM sensor cannot be placed at the same position as the substrate, an initial calibration of the tooling factor is required for each metal source. Tooling Factor is a correction for the difference in material deposited on the quartz sensor versus the substrate.

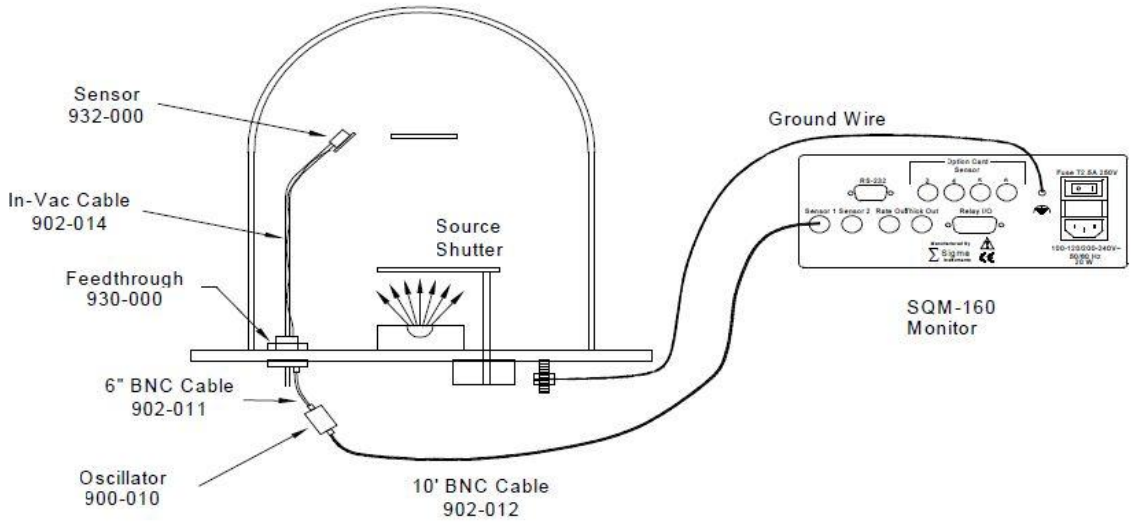


Figure 3-4 Schematic configuration of SQM-160 system

OPA-MBE system is a powerful tool for fabrication of high-quality epitaxial oxide thin films. The ultra-high background vacuum achieved by cryopump and liquid-nitrogen cryo-panels can ensure very low impurity level in the fabricated films. Application of RHEED and QCM makes it possible for in-situ and real-time monitoring of the surface morphology and thin film thickness. With so many source ports and the exact control on metal flux, the element doping in thin film can be managed. However, different from other thin film deposition methods (such as sputtering and spin coating), the growth rate of MBE is very low. In addition, the control on metal flux is very complicated and

professional personnel are required. High cost on purchase and maintenance is another issue.

3.1.3. Top electrode fabrication

Metal top electrodes (gold and silver) with a diameter of 200μm are fabricated by dc sputtering (Leica EM SCD050) with a metal shadow mask at room temperature.

3.2. Materials characterization

3.2.1. X-ray diffraction

X-ray diffraction (XRD) is one of the most widely used techniques to determine the atomic structure of crystal materials. When incident radiation of X-rays reaches a crystalline material, constructive interference of X-rays will occur in directions where the Brag's law is satisfied:

$$2d\sin\theta = n\lambda \qquad \textbf{Equation 3.1}$$

(d is the lattice plane spacing, θ is the angle between incident X-ray and lattice plane, λ is X-ray wavelength and n is an integer.)

Figure 3-5 Schematic of diffraction of X-rays in a crystal material. Figure has been removed due to copyright restrictions. Figure reproduced from[231].

Figure 3.5 shows the diffraction of X-rays in an ordered structure (crystal). By measuring the angles and intensities of those reflected radiation, a picture of the density of electrons within the crystal can be obtained. The mean positions of the atoms in the crystal can be determined from this density image. In this dissertation, the phase and crystal structure of the prepared thin films are detected by an X-ray diffractometer (PANalytical X'pert MRD x-ray Diffraction System) with copper K_α radiation (1.54056 Å).

3.2.2. Scanning electron microscopy and Transmission electron microscopy

Scanning electron microscopy (SEM) is widely used to produce images of surface morphology on the sample. In SEM scanning, an electron beam is focused on the

sample surface and secondary electrons is emitted from the sample. By collecting the emitted secondary electrons signal, the surface morphology can be mapped. In the present study, SEM (Navo NanoSEM 230) is used to measure the surface morphology of the thin film samples.

Figure 3-6 Schematic of structure of a SEM device. Figure has been removed due to copyright restrictions. Figure reproduced from [232].

Transmission electron microscopy (TEM) is a technique used for high-resolution imaging and crystalline structure identification. A focused electron beam transmits through a very thin specimen (<100nm) to form an image from the interaction between the sample and electrons. In this study, TEM (Philips CM200) is used to reveal the stacked structure in the memory devices. Focused ion beam (FIB) technique is applied to prepare specimens for cross-sectional TEM imaging.

Figure 3-7 Schematic configuration of a TEM device. Figure has been removed due to copyright restrictions. Figure reproduced from [233].

3.2.3. X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) can be used to determine the elemental composition in the material. The electrons get activated and escape from the material surface when it is irradiated by a beam of X-rays. By measuring the kinetic energy and number of the escaped electrons, X-ray photoelectron spectroscopy of this material can be obtained. As each element has its characteristic kinetic energy, the elemental composition in this material can be identified. In the present study, both surface and depth-profile XPS measurements are carried out to quantitatively determine the chemical composition in the cobalt oxide thin film.

Figure 3-8 (a) electron energy levels showing the production of XPS signal, (b)typical XPS results, and (c)schematic of a XPS device with its three types of results. Figure has been removed due to copyright restrictions. Figure reproduced from [234].

3.2.4. Conductive atomic force microscopy

Atomic force microscopy (AFM) is a tool used to measure the surface morphology of materials. A silicon cantilever with a sharp tip is landed close to the sample surface moves in the x and y directions by line-scanning. The inter-atomic force causes a deflection of the cantilever when the tip gets very close to sample surface. AFM records the movement of cantilever in the x, y and z directions. Thus, the surface height variation on the sample surface can be mapped. (see Figure 3.9). Conductive AFM (CAFM) is a contact-mode AFM scanning mode which receives both electrical and morphological information simultaneously. It provides high-resolution observation for both lateral topographical and conductive features, so it is a very effective method to study the formation and rupture of conductive filaments during RS process.

Figure 3-9 Schematic of an AFM configuration. Figure has been removed due to copyright restrictions. Figure reproduced from[235].

In this study, a Joel 5400 conductive AFM is used to measure the current mappings as well as current versus voltage (I-V) curves on the CoO film surface in contact mode. For current mapping, a ‘write-erase-rewrite’ process is performed. A positive voltage is applied to scan a larger area to ‘write’ information into the sample; then a negative voltage is applied to scan a smaller area to ‘erase’ information from the sample; then again, a positive voltage is applied to scan an even smaller area in the centre to ‘rewrite’ information in the sample. After each of above step, a reading voltage is applied to the whole area to get the mapping image. For I-V curves measurement, Pt probe is landed on the arbitrary points on sample surface, and cyclic voltage sweeping is applied to obtain I-V curves.

3.2.5. Cyclic voltammetry measurement

The RS performance of CoO-based RRAM devices are checked by measuring I-V curves. I-V curves are measured at the room temperature in a voltage-sweeping mode using a Keithley 2400C source meter. In the forming and set process, a compliance current of 10 mA is used to avoid permanent dielectric breakdown.

During the I-V measurement, the voltage is swept from 0 to a certain value and the corresponding current is recorded. Cyclic voltage-sweeping measurement (endurance and retention) is also performed to check the stability and reproducibility of the as-prepared memory devices.

In the endurance measurement, 50 consecutive voltage-sweeping cycles are conducted. The current of both HRS and LRS at a small reading voltage (for instance, -0.2V) is extracted. Resistance of HRS and LRS at the reading voltage can be calculated and a figure of resistance versus sweeping cycle number can be plotted. The set and reset voltages can also be extracted from the 50 consecutive sweeping cycles I-V curves. A figure of set/reset voltages versus sweeping cycle number can be plotted.

In the retention measurement, the memory cell is firstly switched to LRS and then current is read at a small voltage (for example, -0.2V) with an interval of 10s for a period of 10^4s. Then, the memory cell is switched to HRS and current is read at the same small voltage with an interval of 10s for 10^4s. Resistance of HRS and LRS at the reading voltage can be calculated and a figure of resistance versus time can be plotted.

Chapter 4 Bipolar resistive switching in cobalt oxide thin film studied by I-V characterization and CAFM

4.1. Introduction

Developing new memories, which are high-density, high-speed and low-power-consumption, are important for sustained advances in information storage/processing technologies. RRAMs have attracted extensive research interest in recent few decades and had been proven to be a good candidate for next-generation non-volatile memories [4-6]. Binary transition metal oxides (TMOs), that have very simple composition and structure and are compatible with complementary metal oxide semiconductor (CMOS) process, have gained considerable attention in RRAMs research [10-13]. But compared to n-type oxides, studies on the resistive switching properties of p-type oxides, especially on understanding the switching mechanisms, are relatively limited. This thesis will focus on studying the RS property of p-type CoO thin films.

The exact RS mechanism is still in debate. Various models have been proposed to explain the switching mechanism in different material systems, such as formation and rupture of conductive filaments[81], change of Schottky barriers at the metal-oxide interface[110], trap charging/discharging[159], etc.. Conductive filaments are widely accepted to be the microscopic mechanism for most RS phenomena. However, because of the nanoscale size of conductive filaments, it is usually difficult to observe the filaments directly. Conductive atomic force microscopy (CAFM) provides high-resolution observation for both lateral topographical and conductive features, so it could act as an effective method to study the formation and rupture of conductive filaments in the resistive switching process [8, 236-238].

In this chapter, a combination study of conventional I-V characterization and CAFM current mapping is used to investigate the resistance switching process in a CoO/Pt structure and try to find out the RS mechanism in p-type CoO thin films.

4.2. Experimental details

The cobalt oxide thin film is deposited on Pt/Ti/Si (111) substrate with an oxygen-plasma-assisted molecular beam epitaxy (OPA-MBE) system (DCA M600). During the film deposition, the substrate temperature is kept at 300 ℃. Atomic oxygen is used as

oxidizing agent and generated by an oxygen plasma power source. Oxygen gas is delivered to the plasma power source through a leak valve. Chamber pressure during deposition is $5x10^{-6}$ Torr with oxygen plasma power of 300W. The temperature of cobalt effusion cell during deposition is 1440℃. Deposition time is 2-hour. The bottom electrodes (BE) Pt/Ti are fabricated on silicon substrate with Kurt J. Lesker PVD-75 system. Ti serves as an adhesive layer to silicon substrate. Ag is used as top electrode, which is fabricated by sputtering (Leica EM SCD050) with a metal shadow mask.

The crystalline structure and cross-sectional microstructure of the cobalt oxide thin film are characterized using PANalytical Empyrean thin-film X-ray diffraction (XRD) and Philips CM200 transmission electron microscopy (TEM), respectively.

The dc current-voltage (I-V) characteristic of the Ag/CoO/Pt structure is measured using Autolab 302N electrochemical workstation at room temperature (RT). A Joel 5400 CAFM is used to measure the current images and I-V curves on the CoO film surface in contact mode. A Pt coated silicon tip with a spring constant of ~2.8 N/m and a resonant frequency of ~75 kHz is used for CAFM scan. The CAFM images are processed by Gwyddion software.

4.3. Results and discussion

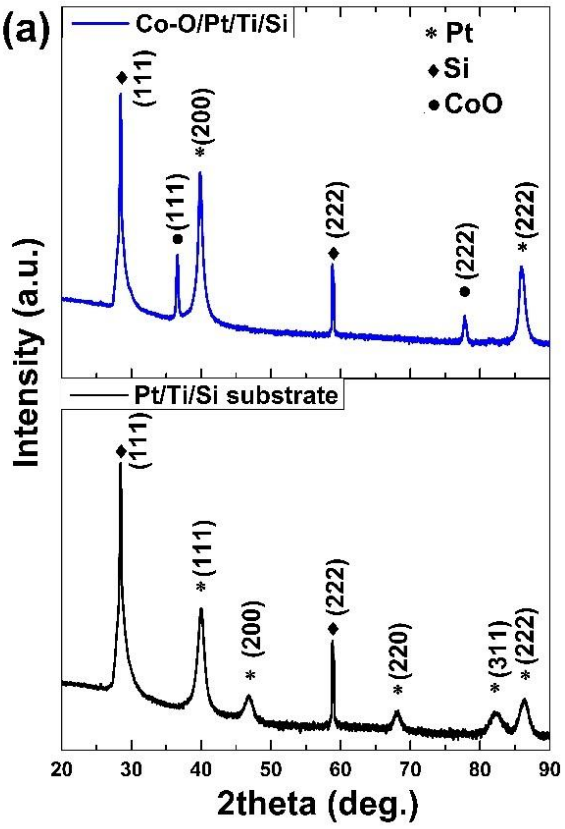
The crystalline phase and microstructure of the prepared cobalt oxide thin film was investigated by X-ray diffraction (XRD) and transmission electron microscopy (TEM), respectively (Figure 4.1). From the XRD pattern, CoO phase can be identified for the as-prepared cobalt oxide thin film. The CoO/Pt/Ti/Si stack structure can be seen clearly in TEM cross-sectional image, showing the thickness of CoO layer to be about 90nm.

The semiconducting type of the CoO film has been tested by Hall Effect measurement. With the known direction of current and magnetic field, the semiconducting type can be determined by the polarity of the induced Hall electric field. In our experiment, the CoO film was found to be p-type.

To investigate the resistive switching properties of the prepared Ag/CoO/Pt structure, the dc current versus voltage (I-V) curve was measured with a voltage-sweeping mode, with a sweeping rate of 0.05V/s. The schematic view of the Ag/CoO/Pt memory device is displayed in Figure 4.2(a). In Figure 4.2(b), the I-V curve of this Ag/CoO/Pt structure is plotted in a semi-logarithmic scale, which shows a typical bipolar resistance

switching characteristic. The numbers along with the arrows represent the voltage sweeping direction (0V→-2V→0V→2V→0V). In its pristine state, the film presents a high resistance state (HRS), where the current flowing through the film is relatively small (for instance, it is less than -10^{-3}A at -0.5V, as indicated by arrow 1). When the voltage is increased to about -1.5V, the current suddenly increases to a much higher value (for instance, it is larger than -10^{-2}A at -0.5V). At this moment, the film enters the low resistance state (LRS). This transition is often called a "Set" process. The device is now turned into an "ON" state. To turn off the device, a bias with opposite polarity must be applied. When the voltage is reaching about 1.0V, the current decreases suddenly and the device enters the HRS again. This so-called "Reset" process turns the device into "OFF" state. It should be noted that the voltage used to reset the device back into HRS should not be too large, because large bias may turn the device back to LRS, and even lead to permanent dielectric breakdown. Therefore, to protect the device from breaking down, the sweeping voltage range is limited in [-1.8V, +1.8V].

It was found in our experiment that the start of resistance switching in this Ag/CoO/Pt structure does not require an "electroforming" process. In most resistance switching memory devices, a high voltage is usually needed to set the device from the primary high resistance state into a low resistance state by soft dielectric breakdown. In this process, the high electric field may introduce many microstructural defects, such as oxygen vacancies (or metal vacancies), which penetrate the film bulk and form conductive channels that connect the top and bottom electrodes. However, this electroforming process is not only time consuming, but also brings additional design problem in memory circuit for the high voltage source[223]. An electroforming-free memory device can avoid these problems. The electroforming-free characteristic of this Ag/CoO/Pt device may be due to the high defects density in the CoO film fabricated under the current deposition condition. The high defect density makes it easier to form conductive channels penetrating the film buck without the requirement of high applied voltage. In this Ag/CoO/Pt memory device, the set and reset voltages (~ -1.5V and 1V, respectively) are quite small, which is favourable for low voltage operation as required in next-generation non-volatile memories.



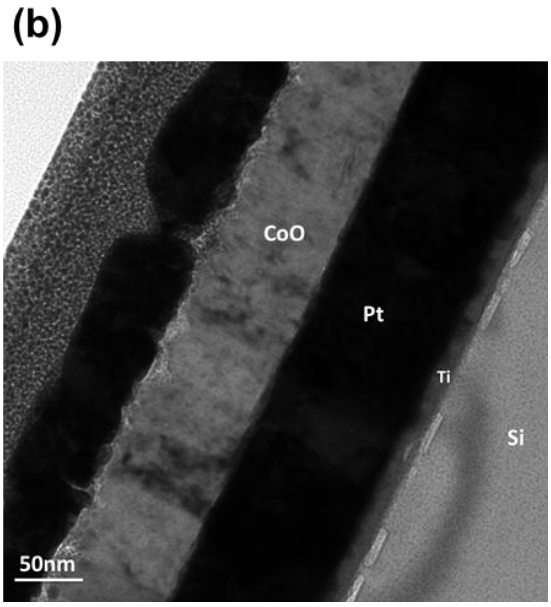


Figure 4-1 (a) XRD patterns of the Co-O/Pt/Ti/Si device, (b) TEM image of the CoO/Pt/Ti/Si structure

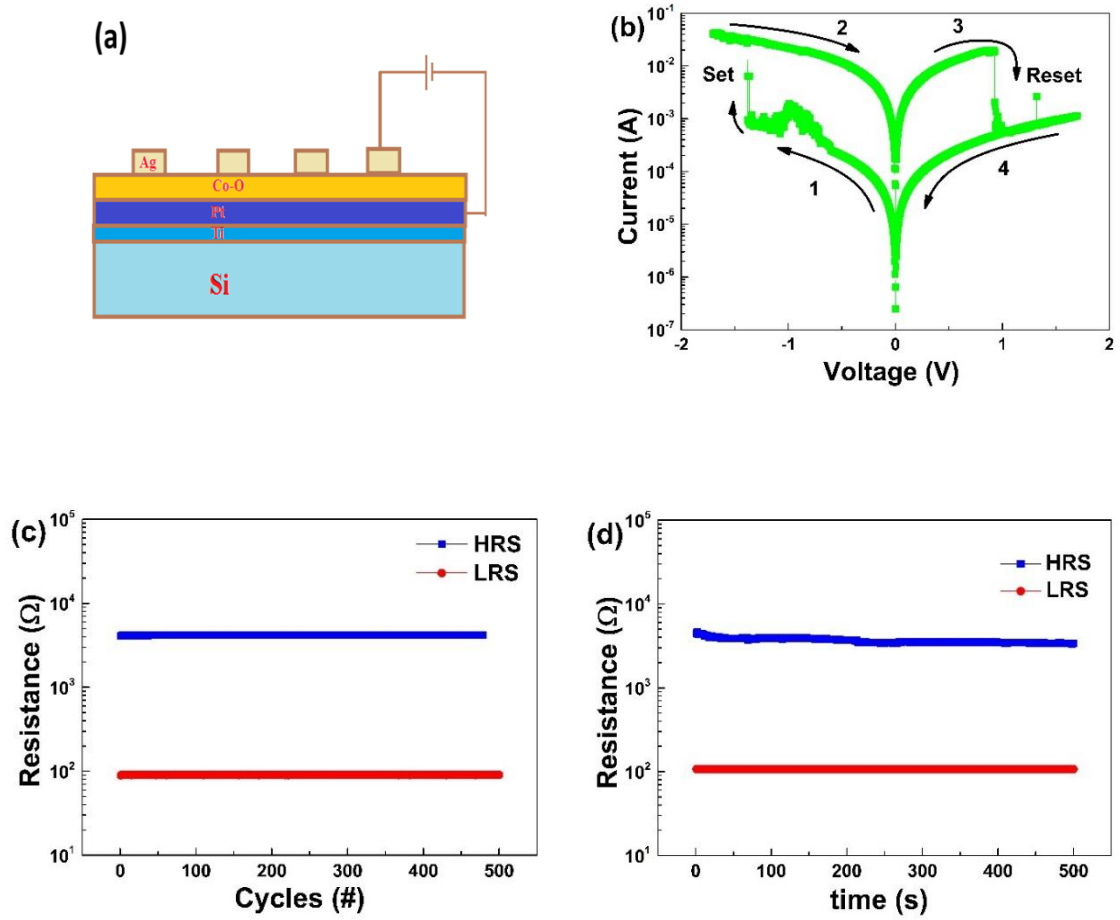


Figure 4-2 (a) Schematic view of the Ag/CoO//Pt/Ti/Si memory device, (b) I-V curve, (c) Endurance and (d) Retention performance of the Ag/CoO//Pt/Ti/Si device

Two key criteria for memory device materials is reproducibility and stability. To evaluate the potential of the Ag/CoO/Pt memory device as next-generation non-volatile RAMs, the reproducibility and stability of resistive switching performance in this device was studied by performing the endurance and retention tests (presented in Fig4.2(c) and (d), respectively). The reading voltage is -0.8V. The memory window (defined as the ratio of resistance between high and low resistance state, R_{HRS}/R_{LRS}) is found to be larger than 40. large memory window is crucial to the success of RS material as memories because the larger ratio ensure clear distinction of low and high resistance state essential for data storage. Endurance test (Figure 4.2(c)) shows that resistances in both HRS and LRS exhibit very small fluctuation for 500 consecutive sweeping cycles, implying highly reproducible and reversible switching performance. Retention test (Figure 4.2(d)) indicates that the ON/OFF ratio remains constant for more than 500 seconds, confirming the non-volatile and reliable nature of this device. With the low set and reset voltage, good endurance and retention performance, and large memory window, this device exhibits very good potential for application in non-volatile RAMs.

To probe the conduction and switching mechanisms in this Ag/CoO/Pt memory device, the I-V characteristics are replotted in log-log scale (Figure 4.3). I-V curves in both positive and negative voltage ranges are linearly fitted. It is to find that the slopes of LRS curves at both bias polarity ranges are approximately 1, showing linearly Ohmic conduction behaviour. This Ohmic conducting behaviour indicates the formation of conductive filaments with metallic nature in the set process [239]. It should be noted that the bipolar resistive switching behaviour in this Ag/CoO/Pt memory device is different from that in an electrochemical metallization (ECM) memory cell with Ag or other active metal as electrodes[87, 99]. The set process in this Ag/CoO/Pt memory device is induced with a negative bias applied on Ag electrode, which will prevent the dissolution of Ag. Thus, it can be inferred that the conductive filaments consist of the internal defects in the film bulk.

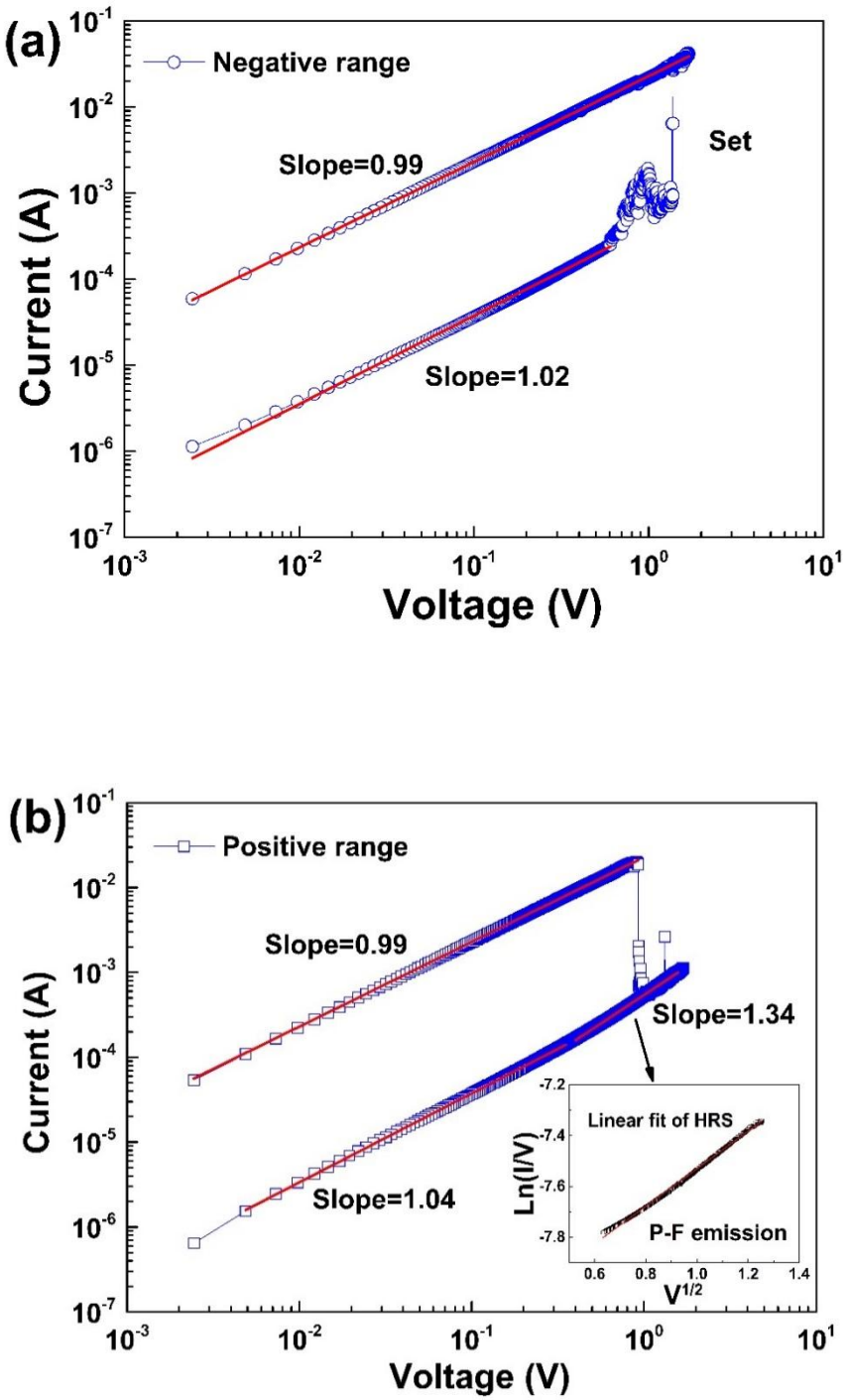


Figure 4-3 Linear fittings of the I-V curve of the Ag/CoO//Pt/Ti/Si memory cell plotted in log-log scale, (a) in the negative and (b) positive voltage range, inset is the $Ln(I/V)\sim V^{1/2}$ linear fit, which corresponds to Poole-Frenkel emission conduction[113].

CAFM is used to reveal the filamentary nature of the resistive switching mechanism in the CoO/Pt structure and to demonstrate the formation and rupture of the conductive filaments during switching process.

The CAFM measurements were conducted on the CoO/Pt film surface in ambient atmosphere at room temperature. The Pt-coated silicon tip operated in contact mode serves as top electrode, and the bottom electrode (Pt) is grounded during the scan. Topographic and dc current image are obtained simultaneously in one scan. A schematic illustration of the CAFM measurement setup is shown in the inset of Figure 4.4(a). Figure 4.4(b) is a topographic image of an area on the CoO film surface, which shows quite uniform surface morphology. I-V curves were obtained by applying an electric field on arbitrary points on CoO film surface. The voltage sweeping sequence was 0V→-3V→0V→3V→0V. It can be seen that: by applying -3V on the tip, the resistance is set to low resistive 'ON' state, while sweeping to +3V can reset the film back to high resistive 'OFF' state. This exhibits a typical bipolar resistance switching behaviour in the Pt-tip/CoO/Pt structure.

It can be found that the set/reset voltages, as well as the on/off ratio, are different between the CAFM measurements (Figure 4.4) and normal I-V characterization results (Figure 4.2). This may be an instrumental issue. In the CAFM measurement, the AFM tip is very small (~100nm in diameter) and it touches the sample surface directly during the scanning. The contact resistance may be large and thus it needs higher voltage to set the film to low resistance. In the normal I-V measurement, however, the tip is much larger and touches the top electrode (gold) during measurement, so the contact resistance is much smaller and only a small voltage is required to set the film into low resistive state. The difficulty in drive the movement of defects in the film by an AFM tip may be the reason for the smaller on/off ratio in CAFM measurement.

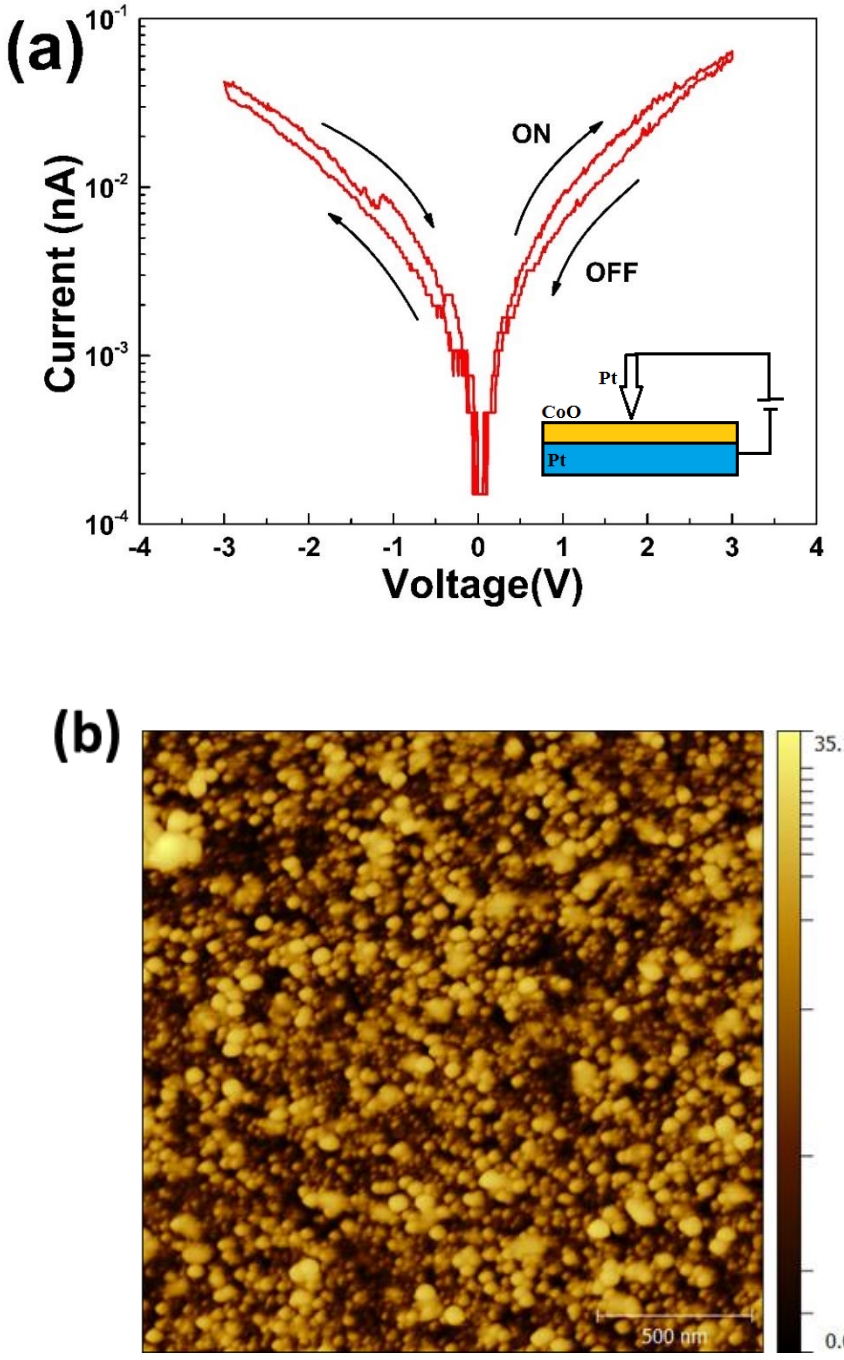


Figure 4-4 (a) I-V curve of Pt-tip/CoO/Pt structure (inset is the schematic diagram of CAFM measurement setup), (b) Topographic image of the CoO thin film

Figure 4.5 illustrates the current mapping images on CoO/Pt film in a 'writing-erasing-rewriting' process. First, a large area (2μm × 2μm) was scanned at a reading-voltage of -1V, seen in Figure 4.5(a). It can be found that the current is very small and dispersive in the entire area. This presents the pristine high resistance state of the film. Then, a writing voltage of -3V was applied to scan the centre area (1μm × 1μm), and the large area was read-out by scanning at -1V again (Figure 4.5(b)). It displays that the current in the centre area is higher than that in the surrounding area, which means that -3V scanning has switched the centre area into low resistance state. In the next step, in order to reset the film from LRS back to HRS, the centre area was scanned with an erasing voltage of +3V, and then the large area was read out at -1V again, see Figure 4.5(c). It can be seen that the centre area now presents very low current, even lower than that in the surrounding un-switched area. This means the centre area has been turned to "OFF" state. If -3V is applied to the centre area again, the film can be switched to LRS again, as seen in Figure 4.5(d). This indicates that resistance switching behaviour is reproducible in this Pt-tip/CoO/Pt structure. It is also found that, although the topography image has drifted a bit, morphology change of the film after the 'writing-erasing-rewriting' process is negligible (Figure 4.6).

Though in a few literatures high-resolution TEM has been used for imaging the microstructure changes during the set and reset operation in the resistive switching process, this technique has its own drawbacks. It costs a lot of time and effort to prepare the TEM sample. Sometimes, it is very difficult to locate the conductive channels that possess nano-sized features. CAFM, however, provides a much easier way to study the electrical properties of the conductive filaments. CAFM can provide high-resolution characterization for both lateral topographical and conductive features. As shown in the current mapping images (Figure 4.5), the bright dots refer to the conductive filaments in the film, and the formation and dissolution of conductive filaments corresponding to the set and reset process can be clearly seen. So it is an effective technique to study the behaviour of nanoscale conductive filaments during the resistive switching process.

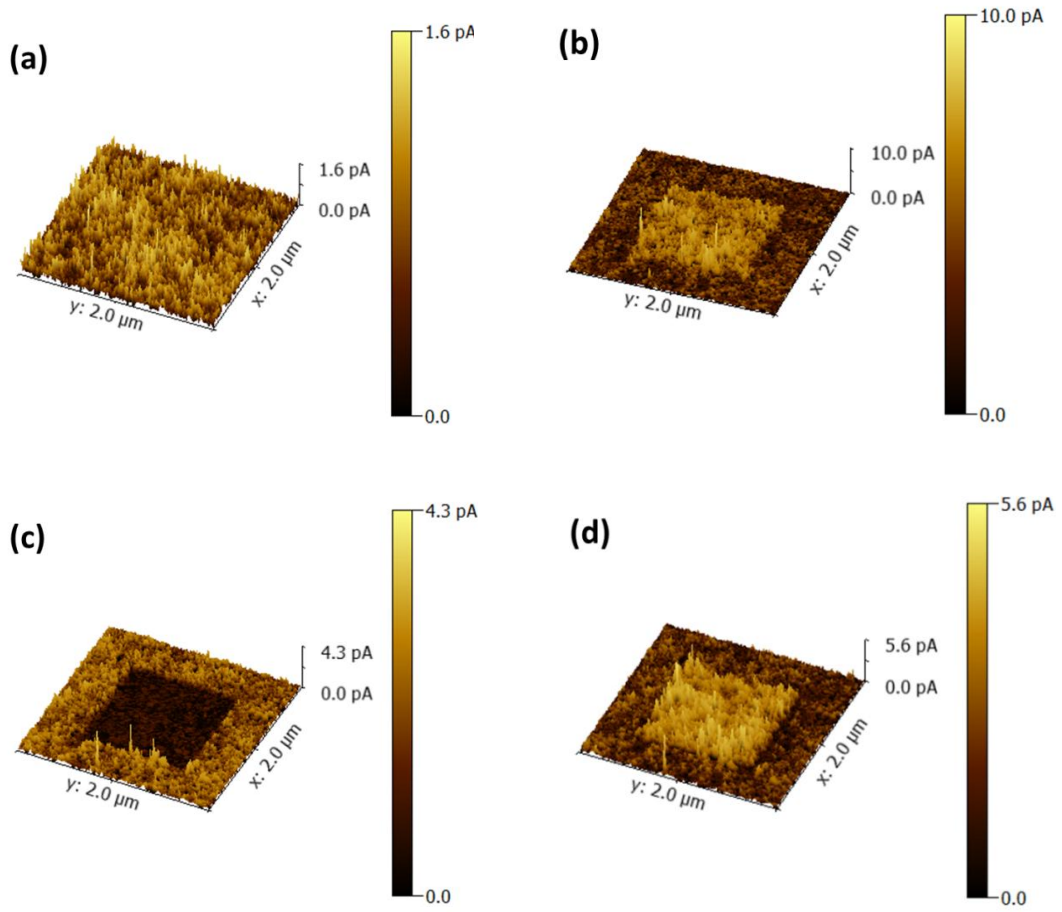


Figure 4-5 Current images of CoO/Pt film (a) at pristine state, (b) after 'writing' scan at the centre area, (c) after 'erasing' scan in the centre, and (d) after 'rewriting' at the centre area. Reading-voltage is -1V

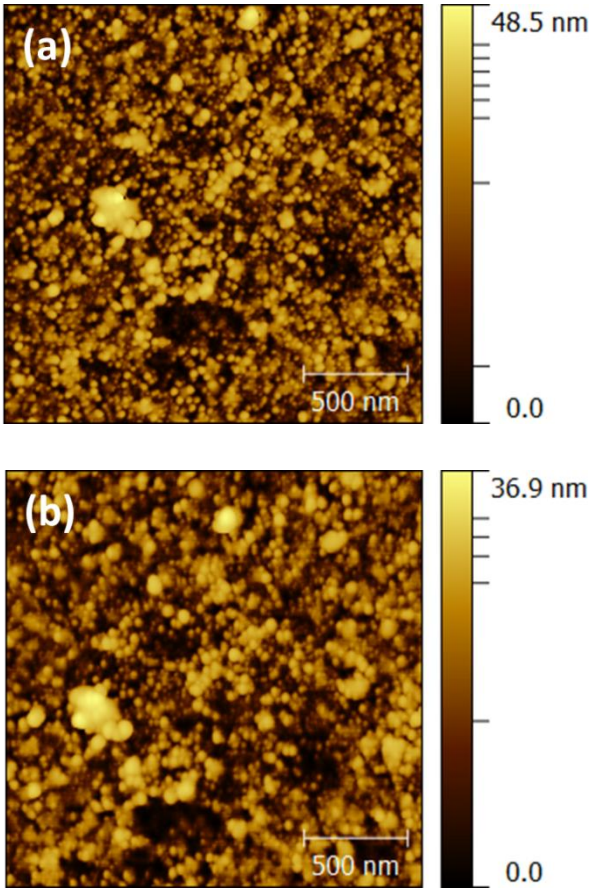


Figure 4-6 Surface morphology of the CoO/Pt thin film (a) before and (b) after the 'writing-erasing-rewriting' process

Based on the above I-V and CAFM characterization of the resistive switching process in the CoO/Pt structure, the bipolar resistive switching mechanism can be interpreted with a conductive filamentary model. Figure 4.7 schematically illustrates the formation and rupture of conductive filaments in the CoO film bulk during the resistive switching process. CoO is generally a nonstoichiometric compound and a p-type semiconductor with cobalt deficiency or oxygen excess [240-242]. At the pristine state, the as-prepared CoO film contains many internal defects, i.e. cobalt deficiency or oxygen excess. When a high electric field is applied between the top and bottom electrodes (Figure 4.7(a)), the oxygen ions in the CoO film, which are negatively charged, would migrate towards the anode. This would induce the reduction of CoO in the local region (even formation of Co clusters in heavily reduced region), resulting in the formation of conductive paths along the electric field. When the top and bottom electrodes are connected by the penetrating conductive filaments, the device is set to less resistive 'ON' state. When a high electric field with opposite polarity is applied on the top electrode Figure 4.7(b)), the oxygen ions will move towards the opposite direction. As a result, the conductive

filaments which consist of highly reduced CoO or even Co metal clusters will locally be oxidized to more stoichiometric phase with high resistance and the conductive filaments get ruptured. The CoO/Pt structure is then switched back to more resistive 'OFF' state.

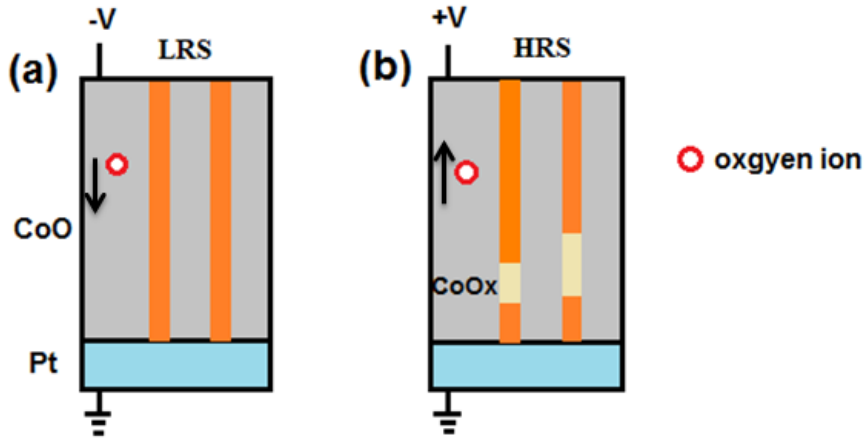


Figure 4-7 Schematic model of the formation and rupture of conductive filaments in the CoO/Pt device, (a) LRS, (b) HRS

4.4. Summary

This work studied the RS behaviour in the OPA-MBE prepared cobalt oxide thin films with a combination of I-V characterization and CAFM current mapping for the first time. Bipolar resistive switching behaviour is exhibited in the CoO thin films. Good resistive switching properties, such as excellent endurance and retention performance, are demonstrated. The Ohmic conduction at LRS indicates the formation of metallic conductive filaments in the set process, which is well consistent to the results in CAFM experiment, in which the formation and dissolution of conductive filaments are observed in a writing-erasing process. This reveals the conductive filamentary RS nature in the cobalt oxide thin film. This study not only demonstrates the good potential of cobalt oxide thin films for non-volatile memory application, but also provides more evidence in understanding the bipolar resistive switching mechanism in the CoO-base RS memory.

Chapter 5 CAFM and KPFM study on the resistive switching property of CoO thin films prepared under different oxygen partial pressures

5.1. Introduction

Formation and rupture of conductive filaments are widely accepted as the microscopic mechanism for most RS phenomena[98, 104, 243]. These conductive filaments have been proved composed of secondary phase or metal chains generated from the redox reaction resulting from the electromigration of defects in the materials[96, 98] under external electric field. Therefore, it can be inferred that defect concentration in the oxide thin films may play an important role in affecting the formation and rupture of conductive filaments during the set and reset RS process. The defect concentration in the oxide thin film is affected by many factors during deposition process, among of which oxygen partial pressure plays a crucial role. This thesis is making an effort to study the effect of oxygen partial pressures on the RS process in CoO-based RRAM cell.

CAFM working in a contact-mode can provide high-resolution observation for both lateral topographical and conductive features, so it is an effective technique to study the behaviour of nanoscale conductive filaments during switching process. Kelvin probe force microscopy (KPFM) is usually used for measuring the sample work function or surface potential of with high spatial resolution[244]. It can also be applied to explain charge-related resistive switching process[245].

In this chapter, CAFM and KPFM are used to study the resistive switching behaviour of cobalt oxide thin films prepared under varied oxygen partial pressures. The effect of oxygen partial pressure on the formation and rupture of conductive filaments during the RS process is investigated. A novel charge-injection/conductive-filamentary model is used to explain the switching mechanism.

5.2. Experimental details

CoO thin films are grown on the $La_{0.7}Sr_{0.3}MnO_3$(LSMO)/$SrTiO_3$ (001) substrate with an oxygen-plasma-assisted molecular beam epitaxy (OPA-MBE) system (DCA M600). LSMO film is deposited by pulsed laser deposition (PLD) technique and serves as a

bottom electrode[229]. During the deposition of CoO thin films, the substrate temperature is 500 ℃. Two CoO thin films are deposited on LSMO under the chamber pressure of 1×10^{-6} Torr and 1×10^{-5} Torr, respectively. Oxygen plasma is used as the oxidizing source and plasma power is set to 300W. The cobalt effusion cell temperature during film deposition is 1440 ℃. Deposition time is 2160s.

X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) are used to identify the phase and composition in the cobalt oxide thin films. To study the resistive switching behaviour, a Joel 5400 CAFM is used to measure the current images and I-V curves on the CoO film surface in contact mode. To study the surface charging properties, a Bruker Icon atomic force microscopy is used first to inject charges into film surface in contact mode, and then to measure the contact potential in KPFM (tapping) mode. A Pt coated silicon tip with a spring constant of ~0.18 N/m and a resonant frequency of ~64 kHz is used for contact mode charging scan. A Pt coated silicon tip with a spring constant of ~2.8 N/m and a resonant frequency of ~75 kHz is used for CAFM and KPFM scan. KPFM measurement is done with 0.5V AC voltage and a lift height of 30nm. Both CAFM and KPFM scan are performed in ambient air.

5.3. Results and discussion

As illustrated in Figure 5.1, XRD patterns of the cobalt oxide thin films grown in both 1×10^{-6} Torr and 1×10^{-5} Torr show only CoO phase. Film deposited in 1×10^{-6} Torr shows preferential (200) orientation growth, while film grown under 1×10^{-5} Torr presents a polycrystalline feature (as found with (200) and (220) peaks). The topographic images of both films are characterized with AFM and shown in Figure 5.1(b) and (c). It can be found that CoO film grown in 1×10^{-5} Torr contains smaller grains than the 1×10^{-6}Torr one. This means that CoO film grown in 1×10^{-5} Torr contains more grains boundaries. Under the high growth pressure, more nuclei on the substrate surface will start to grow up simultaneously, which may result in more grains in the film. These grain boundaries may become the source of formation of conductive channels. The difference in the density of grain boundaries may induce different resistive switching behaviour in two films.

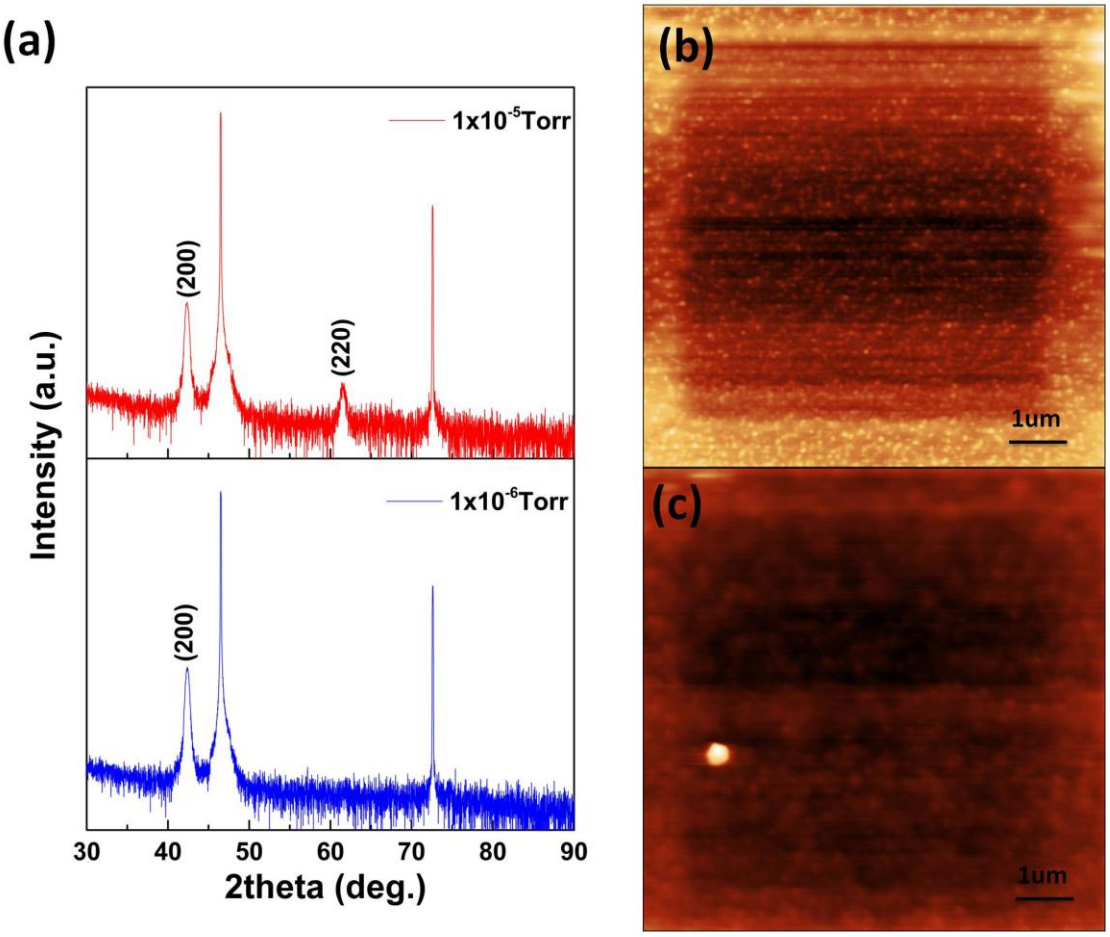


Figure 5-1 (a) XRD patterns of CoO thin films grown in 1×10^{-5} Torr and 1×10^{-6} Torr oxygen partial pressures; (b) AFM topographic image of CoO thin films grown in 1×10^{-5} Torr; (c) AFM topographic image of CoO thin films grown in 1×10^{-6} Torr.

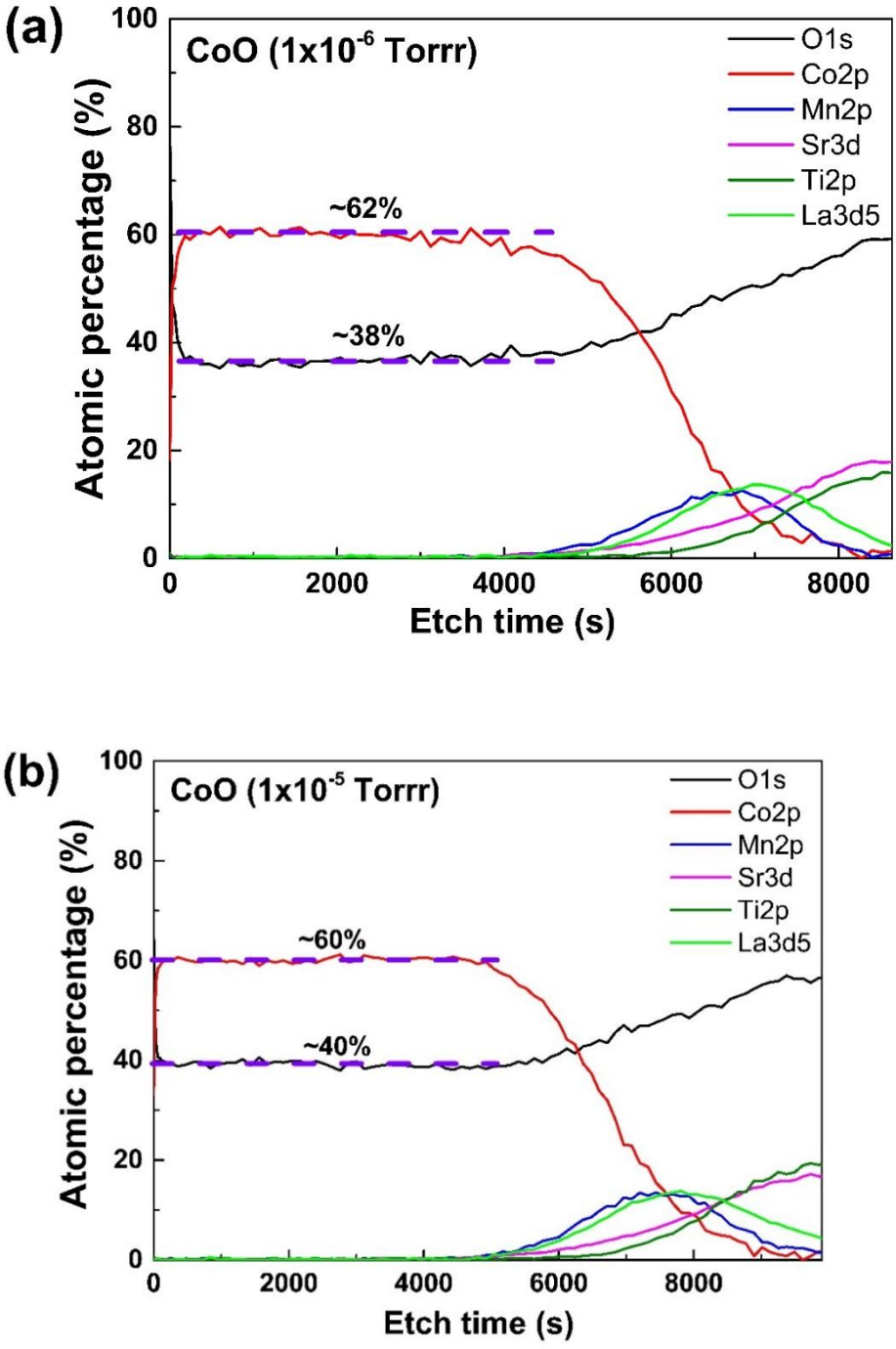


Figure 5-2 XPS depth profile of CoO/LSMO/STO stacks. CoO thin film is prepared in (a) 1×10^{-6} Torr, (b) 1×10^{-5} Torr.

To check the chemical composition of the prepared CoO films, an XPS depth profile study is performed and results are presented in Figure 5.2. It should be noted that during the Ar ion etching process in the XPS measurement some oxygen atoms are inevitably removed from the films by the ions bombardment. Therefore, the obtained oxygen atomic percentage in the film is much lower than that of cobalt. However, because the XPS depth profiles of two samples are performed under the same condition, we can still use the Co/O atomic ratio to qualitatively compare the composition in both CoO films. As demonstrated in Figure 5.2, the Co/O ratio is larger in the 1×10^{-6} Torr sample than in the 1×10^{-5} Torr one. This means that the cobalt content is lower in 1×10^{-5} Torr sample. CoO is normally a nonstoichiometric compound and a p-type semiconductor with cobalt deficiency or oxygen excess [240-242]. Therefore, the 1×10^{-5} Torr sample with lower cobalt content is more off-stoichiometric, containing more chemical defects (cobalt vacancy or excessive oxygen ions) than the 1×10^{-6} Torr sample.

From the above microstructural and chemical analysis, it can be found that the CoO sample prepared under 1×10^{-5} Torr contains more internal defects (either grain boundaries or cobalt vacancies or excessive oxygen ions). It can thus be inferred that the different defects level in these two samples may lead to difference in their electrical conduction and resistive switching properties.

CAFM is used to measure the I-V curves and current images on the CoO thin film surface under applied electric field. Figure 5.3 shows the I-V curves of the Pt-tip/CoO/LSMO stacks at arbitrary points on CoO surface. The voltage is swept in a sequence of 0V → 2V → 0V → -2V → 0V. As can be seen, both Pt-tip/CoO/LSMO memory cells display a current hysteresis loop, showing a bipolar resistive switching characteristic. Sweeping voltage to 2V can switch the cell to ‘ON’ state with higher current. This is called a ‘Set’ process. When the voltage is reversed and swept to -2V, the cell is reset to ‘OFF’ state with lower current flow. By comparing Fig 5.3(a) and (b), it can be found that current in the 1×10^{-5} Torr sample is higher than that in sample grown in 1×10^{-6} Torr, which means that the resistance of the CoO thin film deposited in 1×10^{-5} Torr oxygen pressure is lower. This can be expected, because as discussed above the 1×10^{-5} Torr prepared sample contains more internal defects in the film. This is also consistent with the results in [242], in which it is found that the resistance of CoO single crystal decreases with increasing oxygen partial pressure.

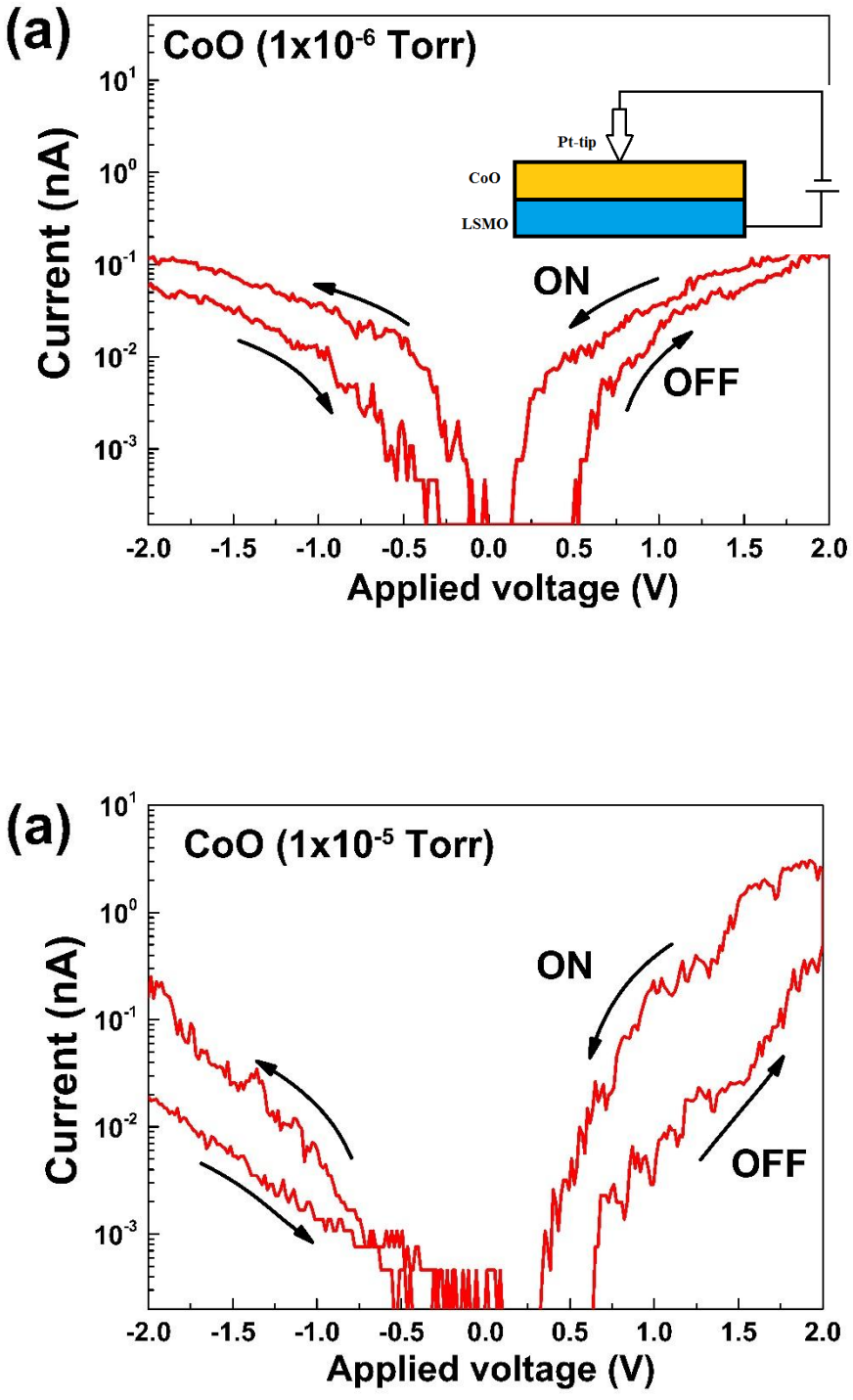


Figure 5-3 I-V curves of Pt-tip/CoO/LSMO structure, with CoO film prepared in (a)1×10^{-6} Torr, (b)1×10^{-5} Torr. Arrows indicate the voltage sweeping direction. Inset is the schematic setup of CAFM measurement.

Current mapping images can give a direct view of the conduction and resistive switching behaviour in the film. A consecutive writing/erasing process by CAFM is performed to study the bipolar switching behaviour in the CoO thin films. The measurement is done as follows. First, a 0.5V reading scan is performed on the CoO films at the pristine state with a scan size of 2μm × 2μm. Then, a 2V writing scan is conducted on a 1μm ×1μm square in the centre. This process is to set the centre area to 'ON' state. After the writing process, a 0.5V reading scan is carried out in the 2μm × 2μm area. Finally, a -2V erasing scan is performed in the centre 0.5μm × 0.5μm area to switch the film back to 'OFF' state. A 0.5V reading scan on 2μm × 2μm area is also done after this erasing process. Figure 5.4 presents the current mapping images after each 0.5V reading scan for CoO samples prepared in 1×10^{-6} Torr (Figure 5.4(a), (b) and (c)) and 1×10^{-5} Torr (Figure 5.4(d), (e) and (f)). It can be seen that both CoO films show typical bipolar resistive switching behaviour. After the 2V writing process, many conducting filaments (white points) are formed in the film. A -2V erasing process, however, can break these filaments and reset the film to high resistance state. An obvious difference between these two CoO samples is that the conducting filament density is much larger in the film prepared under 1×10^{-5} Torr oxygen partial pressure than in the 1×10^{-6} Torr one. This can be attributed to the higher defect concentration (i.e. grain boundaries and cobalt vacancies) in the 1×10^{-5} Torr prepared sample. The conducting filaments are essentially electrically conducting channels consisting of defects [96, 98, 246]. The internal defects (either grain boundaries or point defects) in the CoO film may facilitate the filament formation by providing electrical conducting paths or defect source. It can be noted in Figure 5.4(d) that there are a few conducting filaments formed even under 0.5V reading scan. This can be understood if one considers the so higher defect concentration in CoO (1×10^{-5} Torr) that defect paths can be easily connected to form conducting filaments even under small electric field.

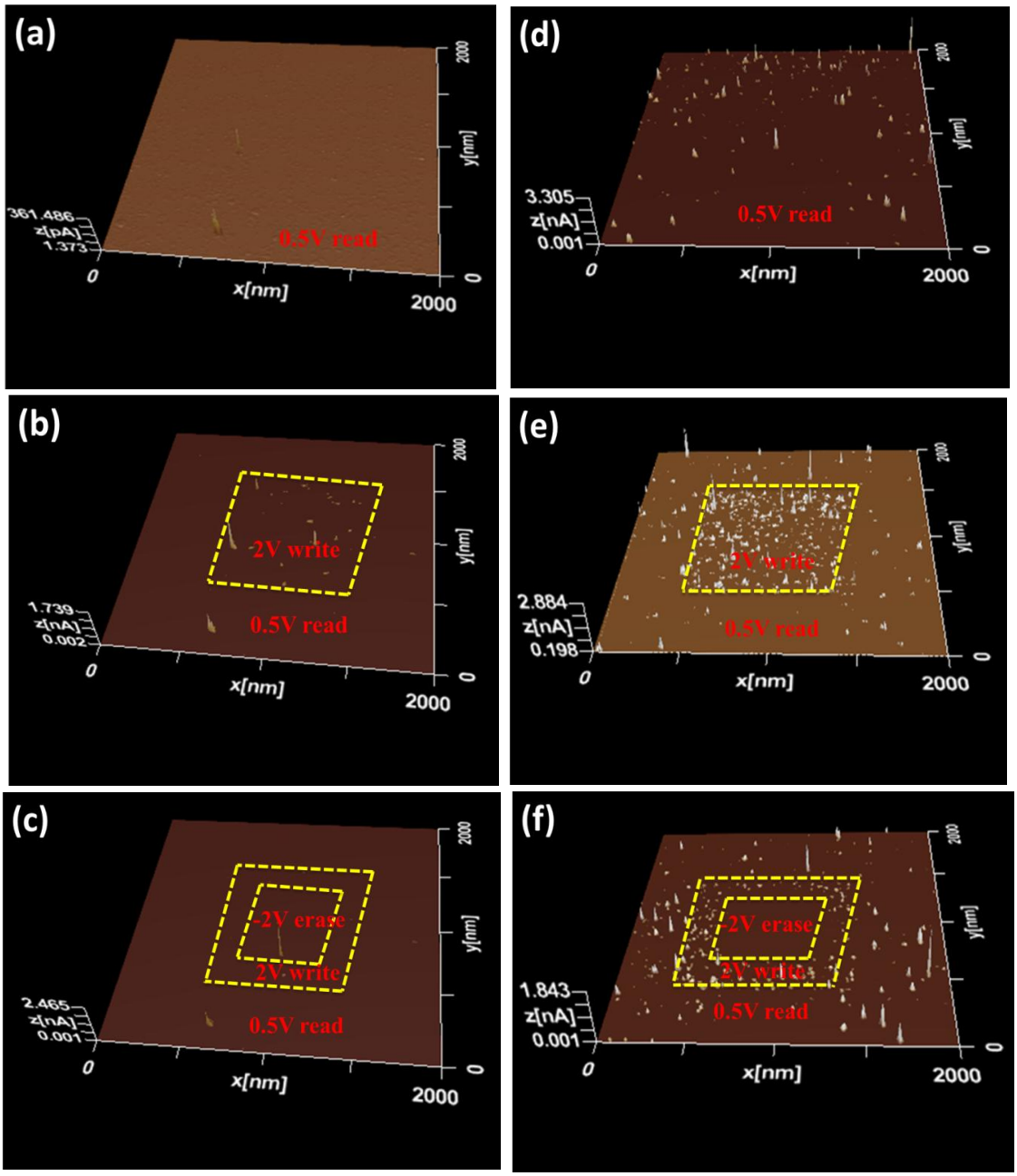


Figure 5-4 CAFM current mapping of CoO samples under consecutive writing/erasing process. (a)(b)(c) and (d)(e)(f) for sample prepared in 10^{-6} and10^{-5} Torr, respectively. (a)(d) pristine state, (b)(e)2V writing in the centre, (c)(f)-2V erasing in the most centre

The filamentary resistive switching behaviour in the NiO thin film has been explained by carrier-injection-induced redox reaction under applied electric field [95]. CoO, like NiO, is also a p-type oxide semiconductor. It could show similar carrier injection characteristic as NiO. KPFM is used to study the charge injection property of CoO under an applied electric field. First, a charge pattern is written on CoO film surface by applying different positive and negative DC bias to the Pt coated tip (bottom electrode grounded) and scanning a 500nm×500nm area in contact mode using 1Hz line scan frequency. Then, these areas are scanned with KPFM in tapping mode with 0.5V AC voltage at a 30nm lift height. Because the contact potential can be affected by the tip-surface interaction, as well as absorbents on the surface, the contact potential of the unbiased area is set to zero so that different results can be compared quantitatively.

As can be seen in Figure 5.5(a) and (b), the CoO surface displays white and black contrast, after written by the positive and negative bias, respectively. The white contrast, which represents higher surface potential, is attributed to the injection of positive charges (i.e. holes) on the surface, while the black contrast, implying lower surface potential, is due to the accumulation of negative charges (i.e. electrons or oxygen ions) on surface. Figure 5.5(c) and (d) shows the surface potential distribution along the arrows in Figure 5.5(a) and (b), respectively. The surface potentials versus applied bias are plotted in Figure 5.5(e) for comparison between CoO samples prepared under different oxygen partial pressures. As can be found, the potential difference is larger on positive bias scanned area (for instance, >100mV at +5V) than on negative biased area (<50mV at -5V), which means the injection of positive charges is more efficient than negative charges. Also, the surface potentials on CoO (1×10^{-5} Torr) is higher than that on CoO (1×10^{-6} Torr). This may be attributed to the difference in defects concentration in the films. CoO (1×10^{-5} Torr), which contains more internal defects, could provide more trapping sites for the injected charges.

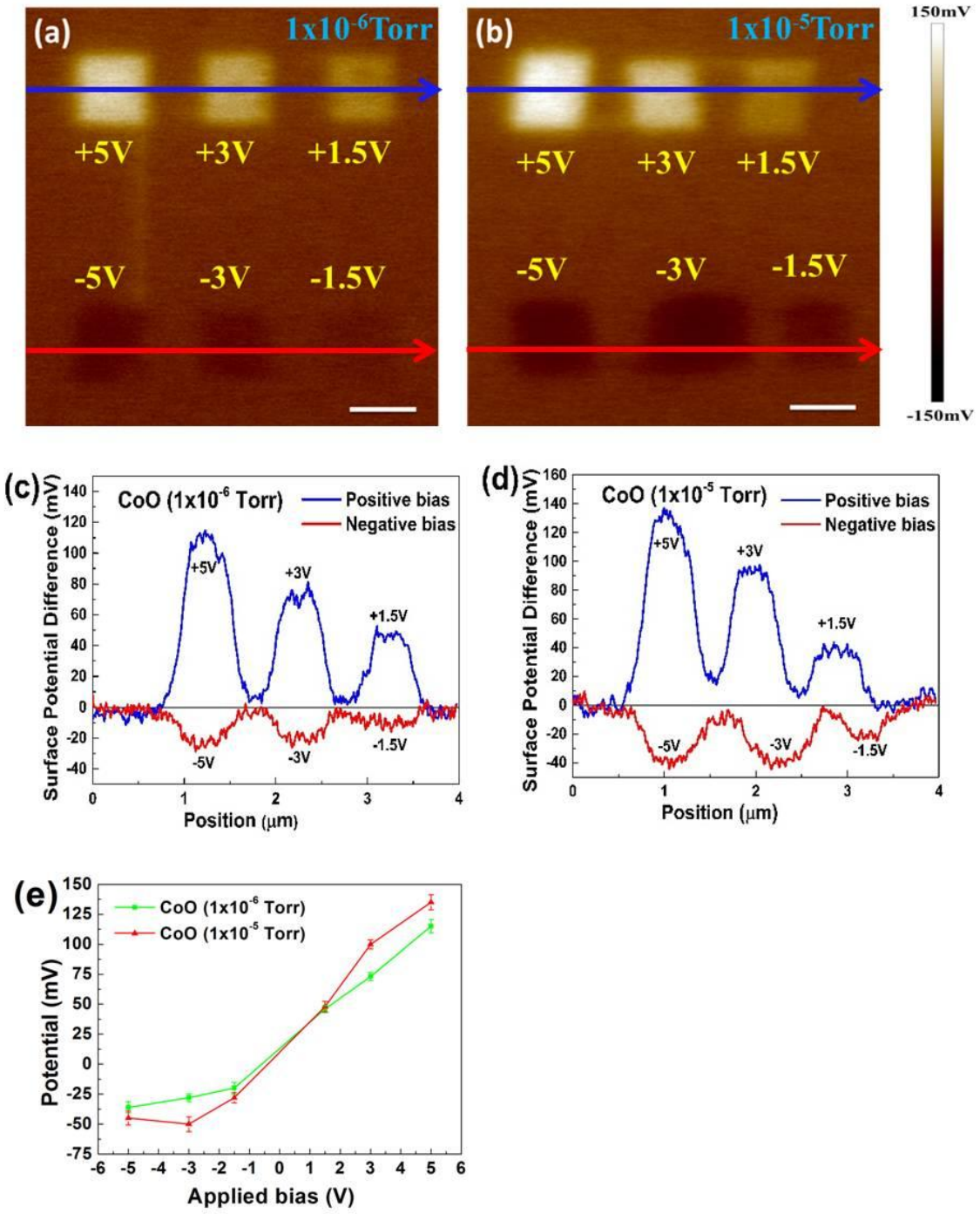


Figure 5-5 KPFM surface potential after charging the CoO surface. Potential pattern for (a)1×10^{-6} (b)1×10^{-5} Torr sample. (c) and (d) surface potential distribution along the blue and red arrows in (a) and (b), respectively. (e)surface potential versus applied bias.

To study the stability of the injected charges on the CoO surface, the surface potential time evolution is investigated. The KPFM image is measured about every 40 minutes after the charging scan. Figure 5.6 shows the surface potential mapping immediately (0h) and 8 hours after charge injection. As can be seen, the contrast becomes obviously weaker 8 hours after charging scan. Figure 5.7(a) demonstrates the time evolution of surface potential after +5V and -5V writing. The surface potential decreases as time elapses. The decrease may come from the lateral dissipation or tunnelling through the conducting substrate[247]. To compare the potential decay rates on two samples, Figure 5.7(a) is replotted to show the remaining surface potential versus time, as seen in Figure 5.7(b) and (c). It is evident that the surface potential decay on CoO (1×10^{-6} Torr) sample is faster than on CoO (1×10^{-5} Torr). This is believed to be related to the difference in defects concentration in two samples. More internal defects in CoO (1×10^{-5} Torr) may trap charges more effectively at defect sites.

During the charging process, the defects near the surface areas of the film can act as trapping sites for injected charges. These injected charges, such as oxygen ions, can play a role in the redox reaction during the formation of conductive filaments. The oxygen ions (both injected and film contained) travel to anode under the applied electric field and this will lead to the reduction of local film and the formation of conduction filaments with metallic nature. The defects at both the surface areas and bulk areas can contribute to the formation of conductive filaments during the resistive switching process.

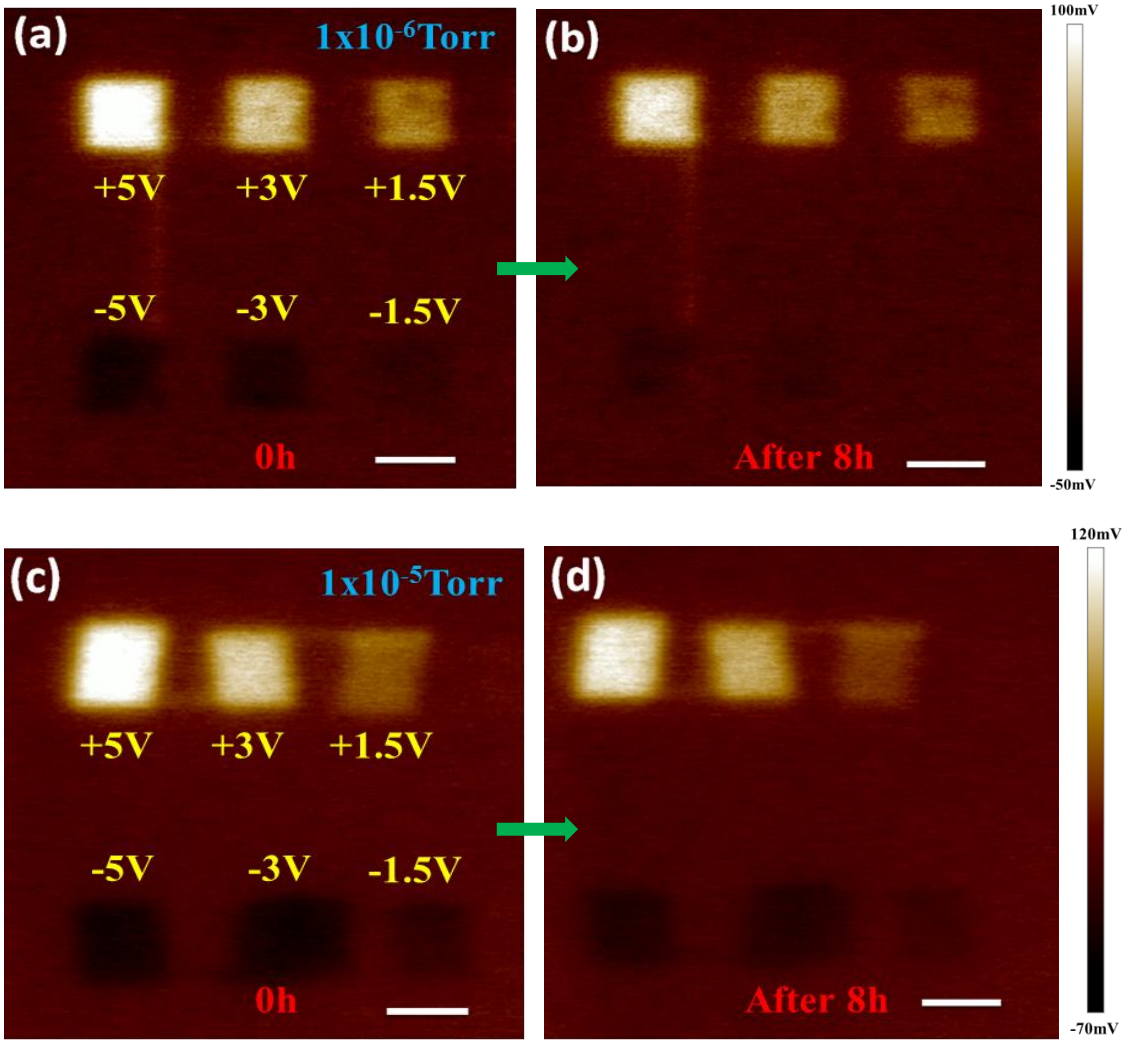
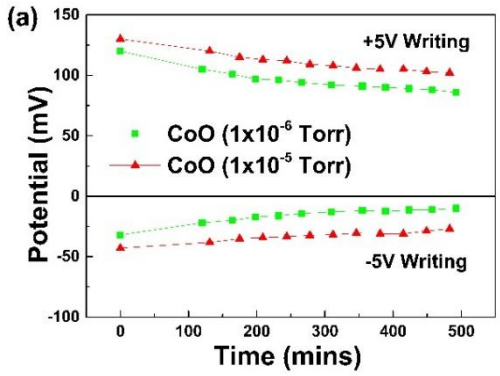
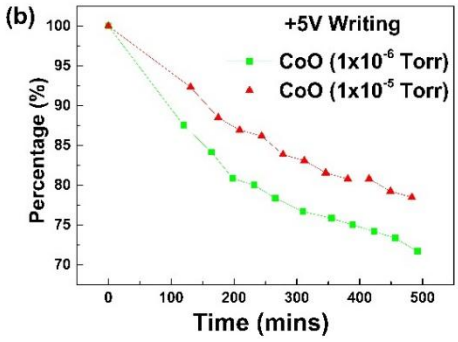


Figure 5-6 Time evolution of KPFM surface potential on CoO thin film: (a) (c) immediately after charge injection, (b) (d) after about 8 hours. The scale bar is 500nm.





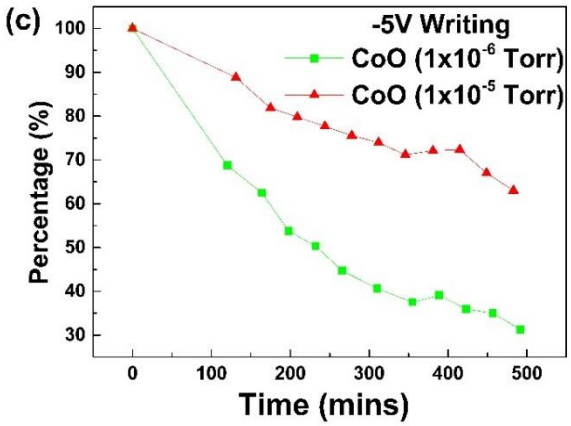


Figure 5-7 Time evolution of surface potential on CoO thin film after +5V and -5V charging scan: (a) potential versus time, (b) (c) remaining surface potential percentage versus time.

Similar to the CAFM writing/erasing scan, a consecutive writing/erasing process is also carried out using KPFM. First, a 2V writing scan is done on a 2μm × 2μm area in contact mode. A -2V erasing scan is subsequently performed in the centre 1μm × 1μm area. Finally, KPFM scan is done on a 3μm × 3μm area to include all the unbiased, written and erased area in one image, as seen in Figure 5.8. It can be found that the 2V writing scan results in a positive surface potential, while the -2V erasing scan could switch the centre area into negative surface potential. This writing/erasing scan shows that the surface potential of CoO thin film can be switched between positive and negative state by applying different polarized electrical bias through the injection of positive and negative charges, respectively.

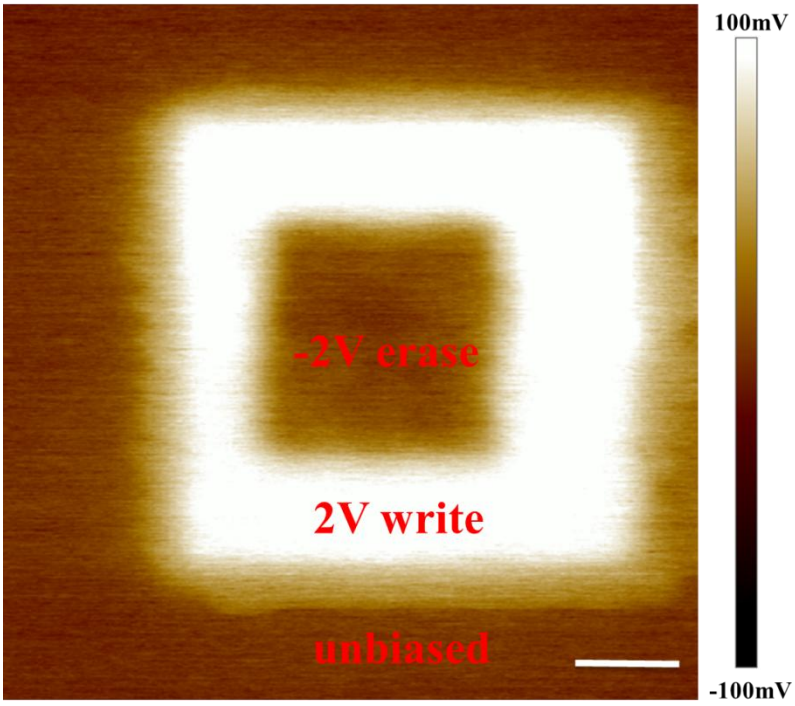


Figure 5-8 KPFM surface potential mapping on CoO thin film after a consecutive writing/erasing scan in the centre. The scale bar is 500nm.

Based on the above CAFM and KPFM study, a charge injection combined with conductive filamentary model is proposed to explain the resistive switching mechanism in the Pt-tip/CoO/LSMO memory cell. As seen in Figure 5.9(a), when a negative bias is applied to the Pt tip, negatively charged electrons and oxygen ions (O^{2-}) are injected into CoO film and trapped mainly at the trapping sites near an interfacial layer (IL). At the same time, oxygen ions in the film bulk migrate towards the anode (LSMO) under the applied electric field. The LSMO bottom electrode serves as an oxygen reservoir and accepts the migrated oxygen ions from CoO. The movement of O^{2-} ions results in the reduction at local CoO region, which becomes reduced to a phase with metallic nature or even metallic cobalt clusters. As the process of O^{2-} ions electromigration continues, the metallic cobalt grows from anode towards cathode. Once the metallic cobalt chain touches the cathode, a conducting filament is formed which connects the top and bottom electrodes. The CoO film is set to low resistance state. It should be noted that the injection of oxygen ions into CoO from Pt tip may lead to the oxidation of local CoO, which is adverse to the formation of conductive filaments. The final connection of top and bottom electrodes by conductive filaments is the result of competition between the injection and extraction O^{2-} ions from the IL. When a positive bias is applied (see Figure 5.9(b)), positively charged holes are injected into CoO film and trapped mainly near the interfacial layer (IL). The negatively charged O^{2-} ions near the top electrode may be extracted from the CoO film. At the same time, oxygen ions in LSMO may migrate into CoO film and move towards the anode and then react with the metallic cobalt chain to form less conductive CoO_x phase. This results in the rupture of conductive filaments. The film is then reset to high resistance state.

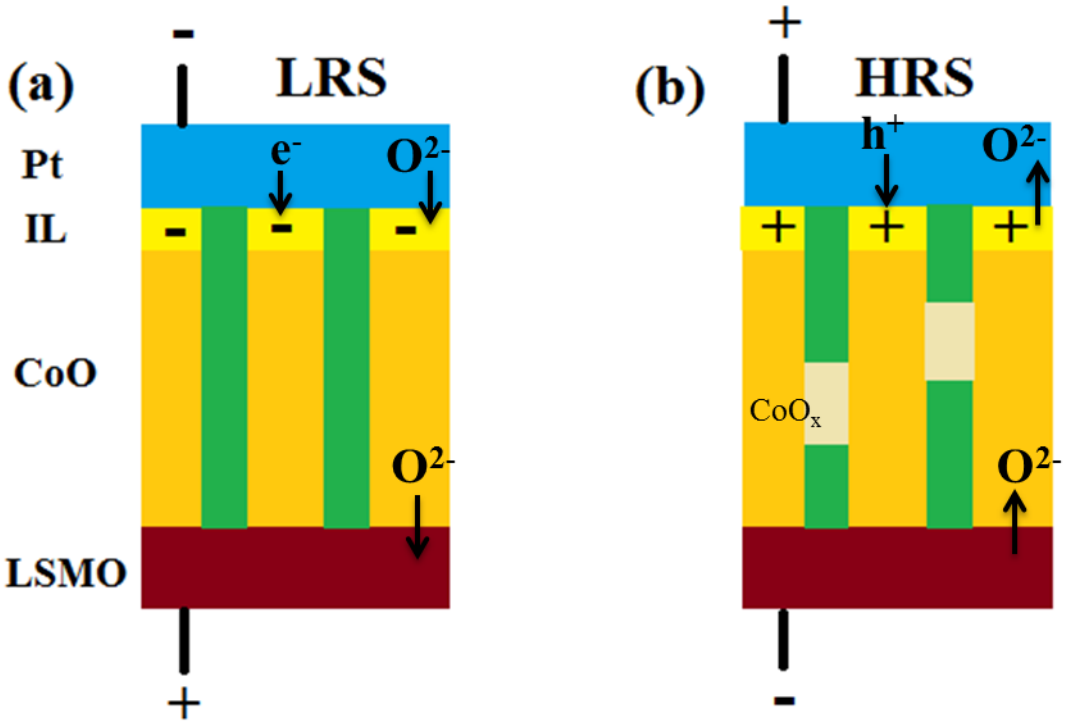


Figure 5-9 Schematic illustration of the resistive switching mechanism in Pt-tip/CoO/LSMO memory cell: (a) conducting filaments form under negative bias, (b) conductive filaments rupture under positive bias.

5.4. Summary

The resistance switching behaviour in the p-type CoO thin film was investigated by a combination of CAFM and KPFM methods for the first time. RS process in the CoO thin films prepared under different oxygen partial pressures (1×10^{-6} Torr and 1×10^{-5} Torr) was studied. CAFM study shows bipolar resistive switching characteristic in both CoO samples, with CoO (1×10^{-5} Torr) sample presenting higher conducting filament density, which can be attributed to higher defects concentration in this film. KPFM measurement shows that the surface potential state of CoO thin film could be switched by charge injections with different electrical bias. The stability of CoO surface potential is related to the internal defects concentration. A charge injection combined with conductive filamentary model is proposed to explain the bipolar resistive switching mechanism in the Pt-tip/CoO/LSMO system.

Chapter 6 Nonpolar resistive switching behaviour in an Au/p-type CoO/n-type TiO_2/Pt heterojunction structure

6.1. Introduction

Most RS memory cells have a metal/insulator/metal (MIM) configuration [10, 11, 21, 248]. Though extensive studies have been done on improving RS performance of MIM-structured RRAMs, there are still some problems remaining to be solved, such as non-uniformity of set and rest voltages and wide HRS or LRS resistance distribution. Compared with the common MIM-structured RRAM devices, memories constructed from multilayer structures sandwiched by two metal electrodes, may exhibit more excellent resistive switching properties, such as fast switching speed[24], improved switching uniformity[25, 26], good scalability [27] and low power consumption[28].

Among the multilayer-structured RRAMs, study on p-n junction based RRAM devices has recently attracted increasing research interest. Resistive switching in these p-n heterojunction memory cell characterizes by transition between rectifying and Ohmic conduction. Different RS behaviours have been found in different p-n heterojunction material systems. In some devices, the p-n heterojunction structures exhibit only bipolar resistive switching (RS) behaviour [27, 225, 227]; while some other devices present transition between bipolar and unipolar RS[224, 226]. In this chapter, we fabricate a CoO/TiO_2 p-n heterojunction structure and study its RS properties, anticipating finding a new material system with good RS application potential.

6.2. Experimental details

The p-type CoO/n-type TiO_2 thin film heterojunction structure is fabricated on the Pt/Ti/SiO_2/Si(001) substrate by an oxygen-plasma-assisted molecular beam epitaxy (OPA-MBE) method. SiO_2 (50nm), Ti (20nm) and Pt (100nm) layers are successively deposited on the Si (001) substrate by means of electron beam evaporation at room temperature. Pt works as the bottom electrode in the memory cell. The TiO_2 and CoO thin films are deposited on the Pt layer successively in the MBE chamber. During the deposition, the substrate temperature is 300 ℃ and chamber pressure is 5×10^{-6} Torr with an oxygen plasma power of 300W. The effusion cell temperatures for Ti and Co are 1580 ℃ and 1450 ℃, respectively. Deposition time for either Co or Ti is 1h. Gold

top electrodes with a diameter of 200μm are coated on top of the CoO layer by DC magnetron sputtering at room temperature through a metal shadow mask. X-ray diffraction (XRD) and transmission electron microscopy (TEM) are used to examine the crystalline and microstructural structure of the CoO/TiO_2 bilayer, respectively. To investigate the resistive switching behaviour of the $Au/CoO/TiO_2/Pt$ memory cell, the current versus voltage (I-V) curves are measured at room temperature in a voltage-sweeping mode using a Keithley 2400C source meter.

6.3. Results and discussion

6.3.1. Structural characterization

The crystalline structure of the as-deposited $CoO/TiO_2/Pt/Ti/SiO_2/Si$ stacked layer was investigated by XRD. As illustrated in Figure 6.1, the diffraction peaks at 36.6° and 77.5° correspond to the CoO (111) and (222) planes, respectively, indicating a preferred [111] growth orientation of the CoO thin film. The diffraction peaks for TiO_2, however, cannot be found in the XRD patterns, which indicates that the TiO_2 thin film prepared at 300℃ is amorphous, or only partially crystallized but beyond the detection limit of our XRD. No impurity phase peaks except for those from $Pt/Ti/SiO_2/Si$ substrate can be detected in the XRD patterns.

The microstructure of the $CoO/TiO_2/Pt$ stacked layer was checked with TEM. Figure 6.1(c) shows the cross-sectional TEM image of the thin films. As can be found, the thickness of the CoO and TiO_2 thin films are 50nm and 30nm, respectively.

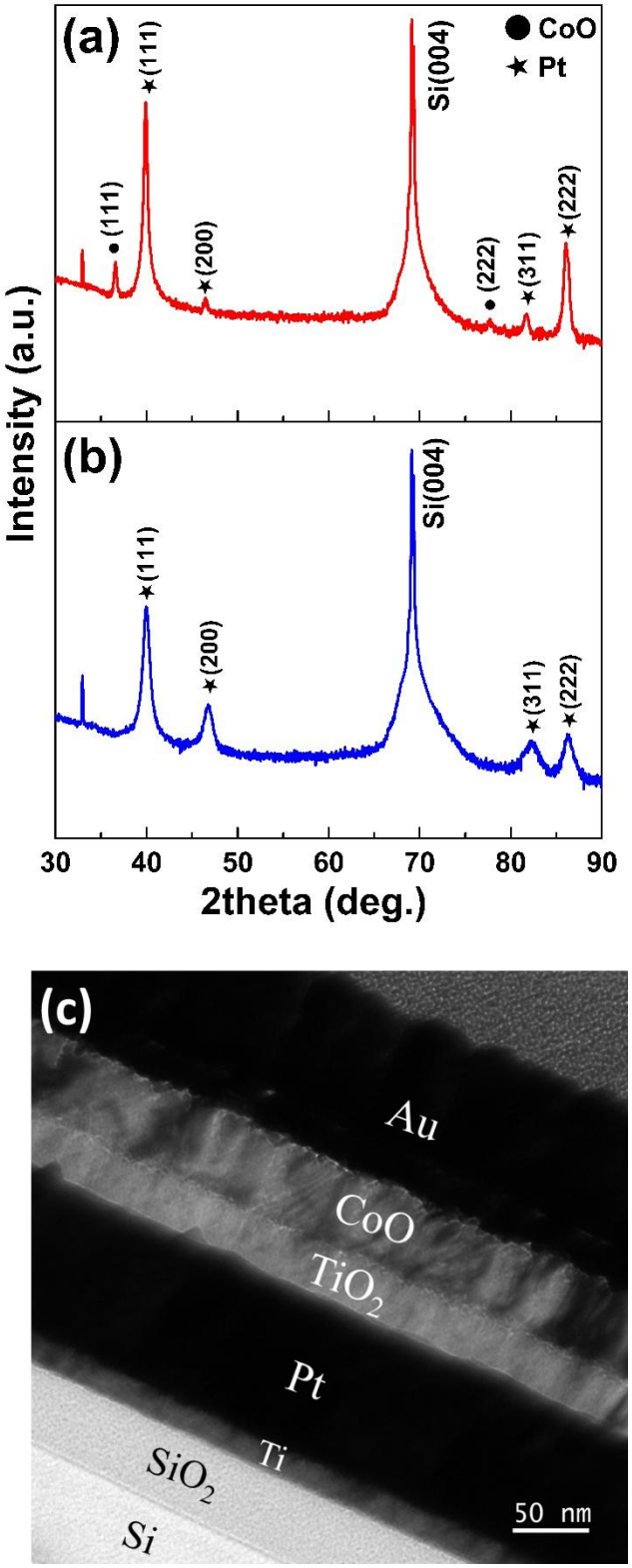


Figure 6-1 XRD patterns of (a) $CoO/TiO_2/Pt/Ti/SiO_2/Si$ structure, and (b) $Pt/Ti/SiO_2/Si$ substrate; (c) Cross-sectional TEM image of the $Au/CoO/TiO_2/Pt/Ti/SiO_2/Si$ stacked layers

6.3.2. Electrical properties characterization

Figure 6.2 shows the I-V curve of the Au/CoO/TiO_2/Pt stacked structure at the pristine state. The inset shows the schematic structure of the stacked layers. During the I-V test, the gold top electrode is biased, while the Pt bottom electrode is always grounded. It can be seen that the I-V curve of the stack at the pristine state displays a typical rectifying characteristic with a turn-on voltage of ~1V, which indicates that either a Schottky barrier junction is formed at the Au/CoO or TiO_2/Pt interface, or a p-n junction is formed at the p-type CoO/n-type TiO_2 interface. As in our Au/CoO/TiO_2/Pt stack structure, the positive bias applied to Au is the forward bias (where the current increases much faster compared to that under reverse bias), the possibility that the rectification behaviour coming from the Schottky barrier at Au/CoO or TiO_2/Pt interface can be excluded. Supposing a Schottky barrier is formed at either the Au/p-type CoO or n-type TiO_2/Pt interface, when a positive bias is applied to Au (i.e. negative bias is applied to Pt), the forward bias should be in the negative bias range and reverse bias should be in the positive bias range[127]. Therefore, it can be concluded that the rectifying characteristic comes from the p-n junction formed at the interface between the CoO and TiO_2 thin films.

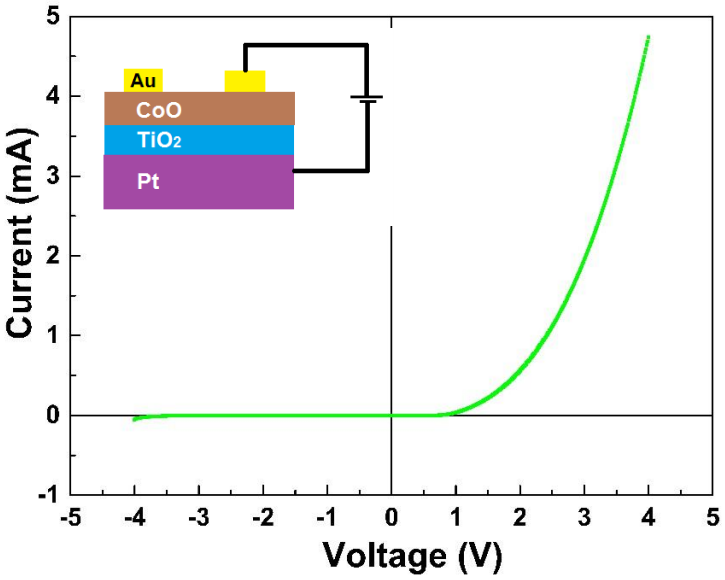


Figure 6-2 The I-V curve of the Au/CoO/TiO_2/Pt memory cell at the pristine state, showing a typical rectifying characteristic. Inset demonstrates the schematic stack structure of the Au/CoO/TiO_2/Pt memory device.

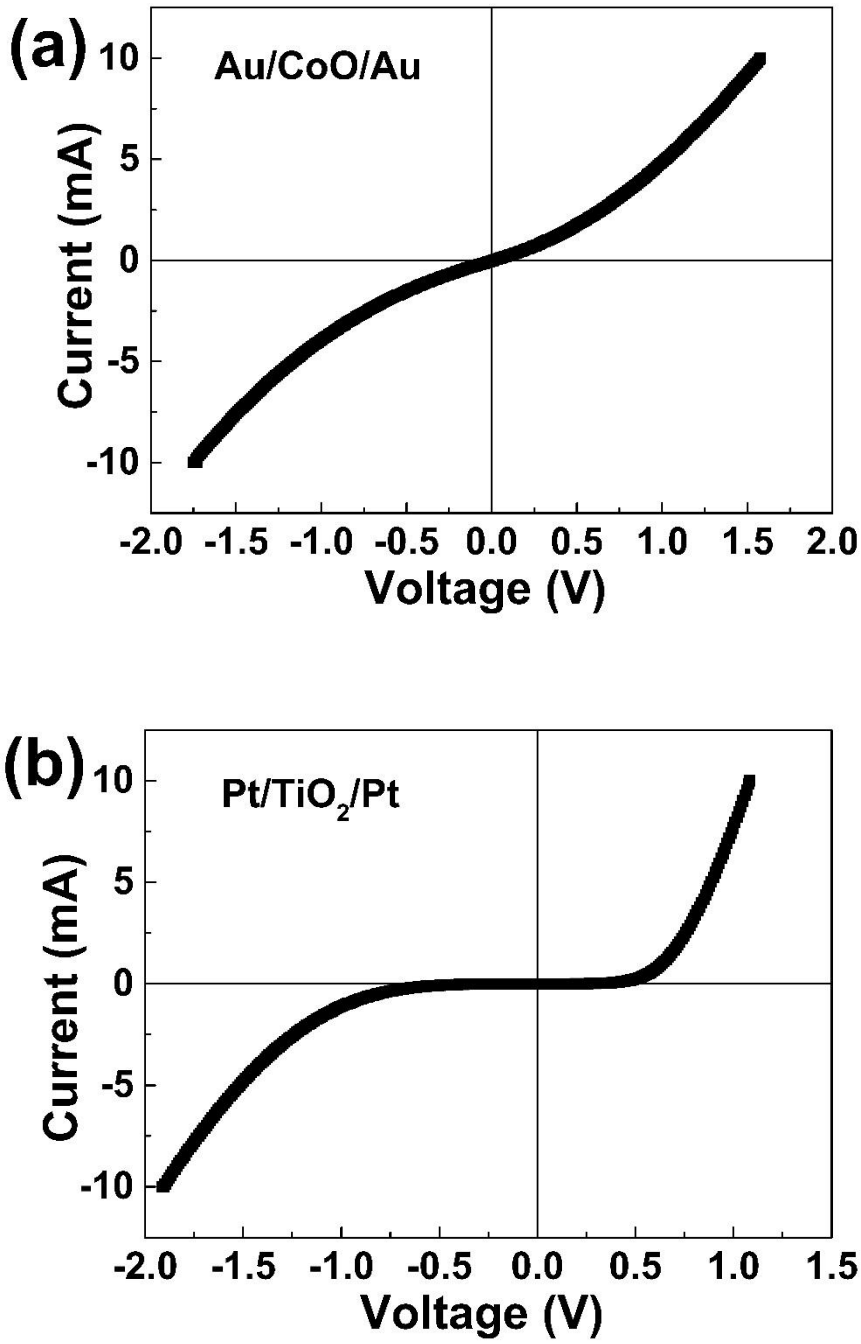


Figure 6-3 The I-V curve of (a) Au/CoO/Au and (b) Pt/TiO_2/Pt single layer structure

Figure 6.3 shows the I-V curves of Au/CoO/Au and Pt/TiO_2/Pt single layer structure. It can be seen that at the current film preparation conditions, both CoO layer and TiO_2 layer exhibit no resistive switching behaviour.

The Au/CoO/TiO_2/Pt stack structure can be turned into a memory cell by an electroforming process. As seen in the inset of Figure 6.4(a), sweeping the voltage from zero to about -9.5V leads the Au/CoO/TiO_2/Pt device to a 'soft breakdown', with current suddenly increasing to the compliance current (10mA). The memory cell enters a low resistance state (LRS). This is called an 'electroforming', or 'set' process. A subsequent negative bias sweeping can switch the cell back to high resistance state (HRS) through a 'reset' process. The memory cell can be switched between LRS and HRS by applying successive negative bias to the gold electrode. The device exhibits unipolar resistive switching behaviour. Figure 6.4(a) shows the unipolar RS I-V curves of the Au/CoO/TiO_2/Pt memory device for more than 50 successive sweeping cycles. It demonstrates a reproducible and stable resistive switching performance in our Au/CoO/TiO_2/Pt heterojunction device.

It should be noted that because of the rectifying characteristic of I-V curve of the Au/CoO/TiO_2/Pt heterojunction at the pristine state, if we try to start the electroforming process by applying a positive bias to the gold electrode, the current fast increases to the compliance current before soft breakdown could occur. (Note: the compliance current cannot exceed 15mA, or else permanent breakdown occurs and the device gets completely damaged.) At some points on the device, however, the electroforming may occur and it also exhibits unipolar resistive switching in the positive bias range. But this resistive switching at positive bias range is not very reproducible; it cannot be switched to LRS after several sweeping cycles. Figure 6.4(b) displays the unipolar resistive switching characteristics of the Au/CoO/TiO_2/Pt memory device under positive bias. The magenta line shows the electroforming process. As can be found, the current at the forming voltage is very close to the compliance current. The red and blue lines represent the 'reset' and 'set' process, respectively. The green line indicates that the device stays at HRS after 10 successive sweeping cycles and cannot be switched to LRS anymore.

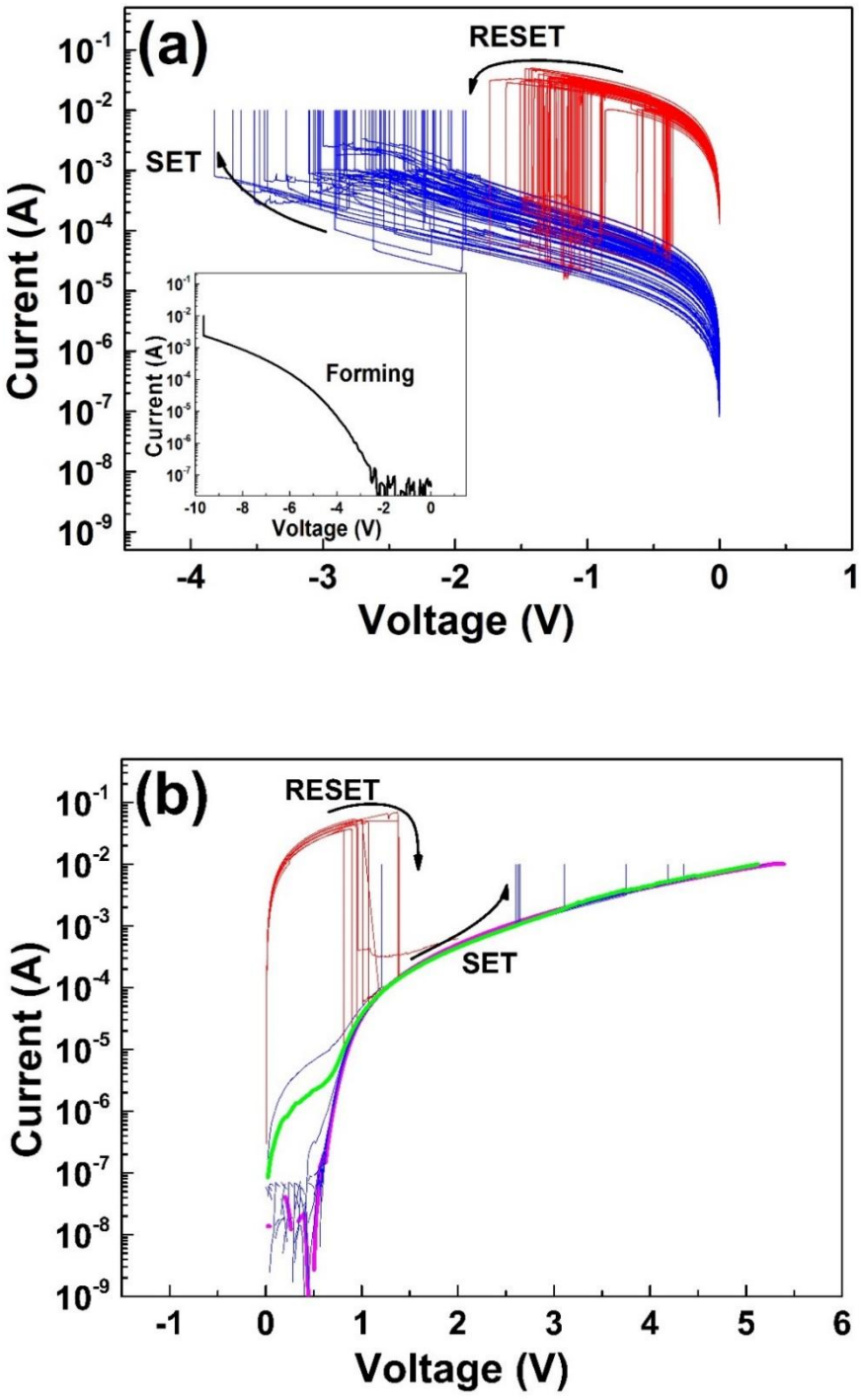


Figure 6-4 Unipolar I-V characteristics of the Au/CoO/TiO_2/Pt memory cell under (a) negative bias and (b) positive bias. Inset in (a) shows the electroforming I-V curve.

Interestingly, the Au/CoO/TiO_2/Pt device can also be reset to HRS with a positive bias after a negative bias set process. As seen in Figure 6.5, after an electroforming process (shown in the inset) in the negative bias range, the device is set to a low resistive ON state. Sweeping voltage from zero to a threshold value in the positive bias range can reset to device to a high resistive OFF state. The Au/CoO/TiO_2/Pt memory device can be switched successively between LRS and HRS by applying negative and positive bias to the Au electrode, respectively. It can be inferred that the device could also be set by positive bias and reset by negative bias, respectively, though the set process in the positive bias range is not reproducible. This indicates a polarity-independent RS characteristic in our Au/CoO/TiO_2/Pt memory cell, also called 'nonpolar' RS behaviour.

It is worth to note that the reset process in the positive bias range may be induced by the Joule heat [249]. When a relatively small compliance current (≤10mA) is used in the reset process, the device cannot be switched to HRS even if the voltage is swept to a large value. Only the compliance is set to a high current or no compliance is set, can the device be reset to OFF state. This means that the reset process may induced by the Joule heat created from high reset current.

From the above analysis on the I-V curves of the Au/CoO/TiO_2/Pt device, it is found that the device shows a nonpolar RS property, quite different from other reported p-n heterojunction memory devices [27, 28, 224-227]. In the reverse bias range, reproducible unipolar resistive switching can always occur. But due to the nature of unidirectional conduction in the p-n junction, in the forward bias range, where current can increase very fast to the compliance, the set process is not very reproducible. Setting and resetting can also be achieved by applying negative and positive bias to Au top electrode, respectively, and vice versa.

Non-polar resistive switching behaviour allows people to control the ON and OFF of the memory cell with either polarity of the electric field. While in bipolar RS process, an opposite electric polarity must be applied to change the resistive state of the cell and unipolar RS requires the same polarity of electric field, the non-polar RS may provide memory cells with more operational choices. Exploring the RS behaviour in this structure may lead to more understanding in the RS mechanism in p-n heterojunction structures.

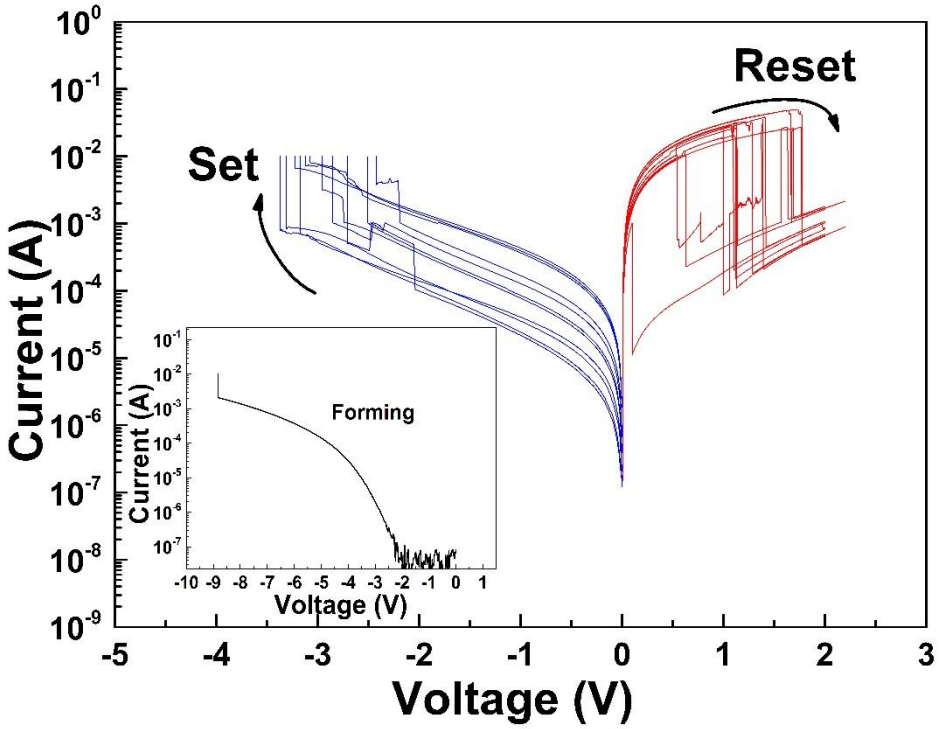


Figure 6-5 Bipolar resistive switching behaviour in the Au/CoO/TiO_2/Pt memory device; Inset shows the forming process.

In order to evaluate the reliability of the Au/CoO/TiO_2/Pt structure as a memory device, endurance and retention test have been conducted in the reverse bias range, where the RS is most reproducible. The resistance of the device was measured at room temperature at a reading voltage of -0.2V. Figure 6.6(a) shows the endurance performance of the Au/CoO/TiO_2/Pt memory cell. It can be seen that the resistance at LRS remains quite stable over 50 successive sweeping cycles, while resistance at HRS undergoes a slight fluctuation. The resistance ratio of HRS to LRS is larger than two orders of magnitude, which is suitable for practical applications as non-volatile memories. Figure 6.6(b) demonstrates the retention performance of the Au/CoO/TiO_2/Pt memory cell. As can be seen, the resistance at either HRS or LRS remains very stable over a long period (>10^4s), which indicates that the Au/CoO/TiO_2/Pt memory cell can store information for a long time without obvious degradation. Both endurance and retention tests proves that the Au/CoO/TiO_2/Pt memory device owns good potential for non-volatile memory application.

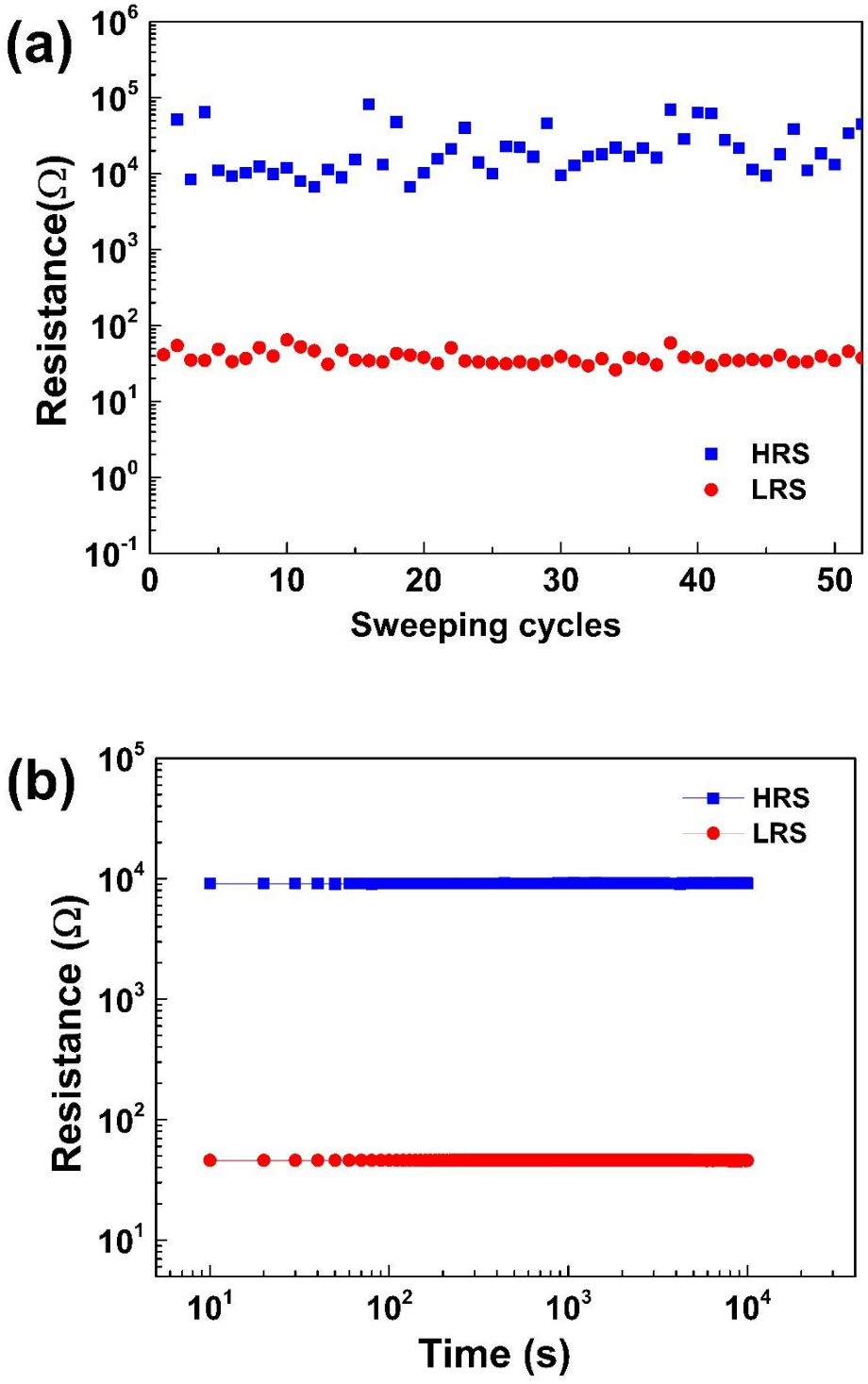


Figure 6-6 (a) Endurance and (b) retention performance of the Au/CoO/TiO_2/Pt memory device under unipolar resistive switching mode; All resistances were measured with a reading voltage of -0.2V at room temperature.

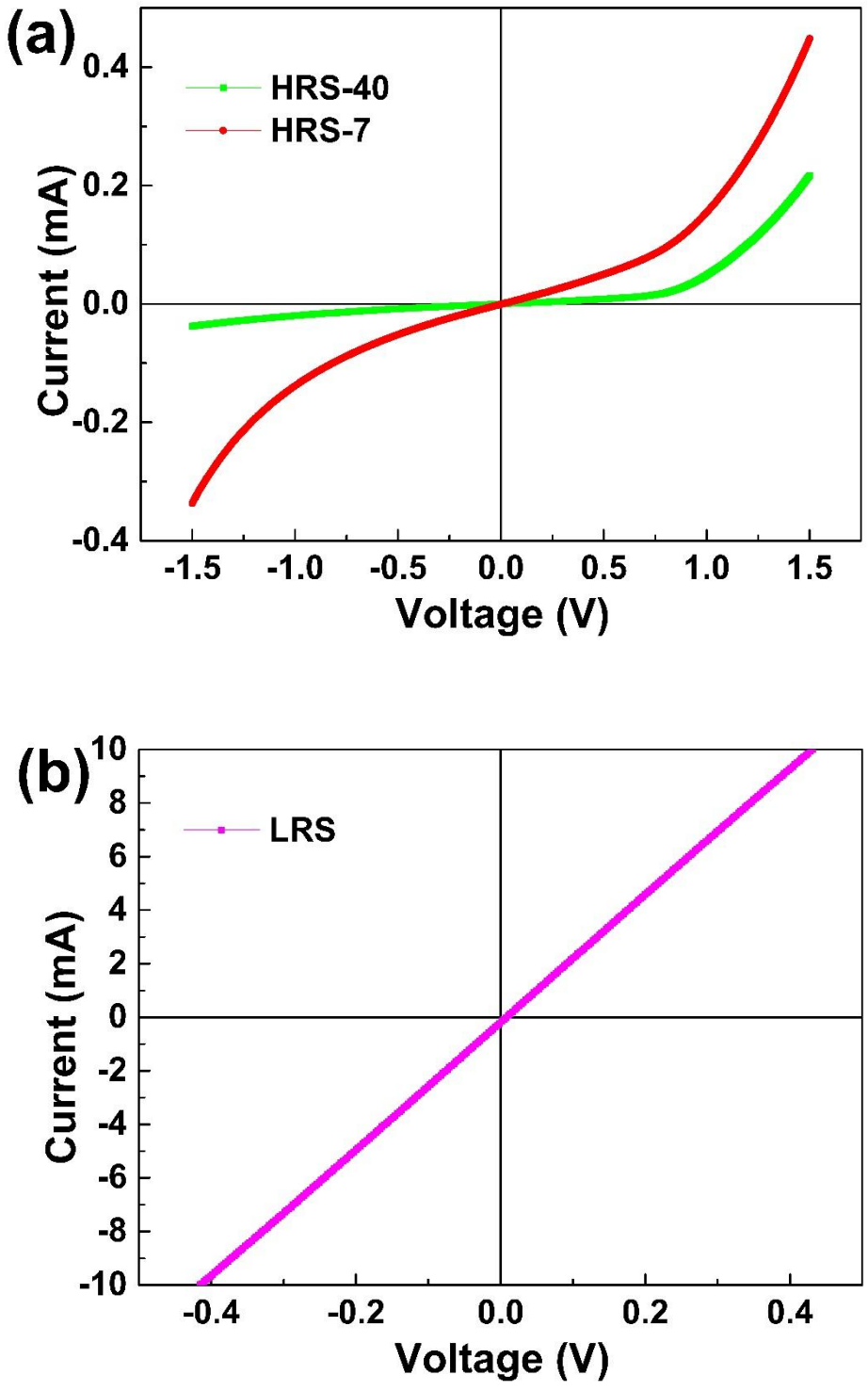


Figure 6-7 I-V characteristics of the Au/CoO/TiO_2/Pt memory device at (a) HRS and (b) LRS

To investigate the electrical conducting behaviour in the resistive switching of the Au/CoO/TiO_2/Pt memory cell, the I-V curves at both HRS and LRS are measured at lower electric field (smaller than the set voltages). Figure 6.7(a) shows the I-V characteristics of HRS in the 7th and 40th sweeping cycles in Figure 6.6(a). Both I-V curves at HRS show rectifying characteristics. It can be found that a higher resistance corresponds to a more obvious rectifying behaviour (in the 40th cycle, HRS=63523Ω; in the 7th cycle, HRS=10296Ω). The rectifying conduction behaviour comes from the p-n junction formed at the interface of the CoO/TiO_2 structure. This indicates that conduction at the CoO/TiO_2 interface may dominate at HRS. Figure 6.7(b) displays the I-V curve at LRS, which shows a linear relationship between current and applied voltage, suggesting that Ohmic conduction dominates at LRS. During the voltage sweeping cycles, the device switches between rectifying and Ohmic conduction behaviour.

In order to further study the conduction mechanism during the resistive switching, the I-V curves at both HRS and LRS under negative bias are fitted to different conduction models (space charge limited conduction (SCLC)[250, 251], Schottky emission (SE)[122, 164], Poole-Frenkel emission (P-F)[252, 253], Fowler-Nordheim tunnelling (F-N)[122, 254], etc.). Figure 6.8 shows the I-V curves replotted in a log-log scale. It is found that, at LRS, the current increases in a nearly linear trend (with a slope≈1) with voltage, exhibiting Ohmic conduction behaviour. This implies that metallic filaments may have formed after the ‘set’ process[90]. At HRS, however, the conduction behaviour is different. It exhibits Ohmic conduction at lower electric field (slope≈1). At higher electric field, the current increases nonlinearly with voltage with a slope of ~2. This characteristic fits well with the SCLC model, in which Ohmic conduction ($I \propto V$) dominates at lower electric filed, while conduction obeys Child’s law ($I \propto V^2$) at higher electric field[251]. The conduction behaviour under very lower electric field (<0.05V) at HRS cannot be fitted to any aforementioned models. The generation-recombination conduction in the p-n junction may dominate in this low electric field range[127].

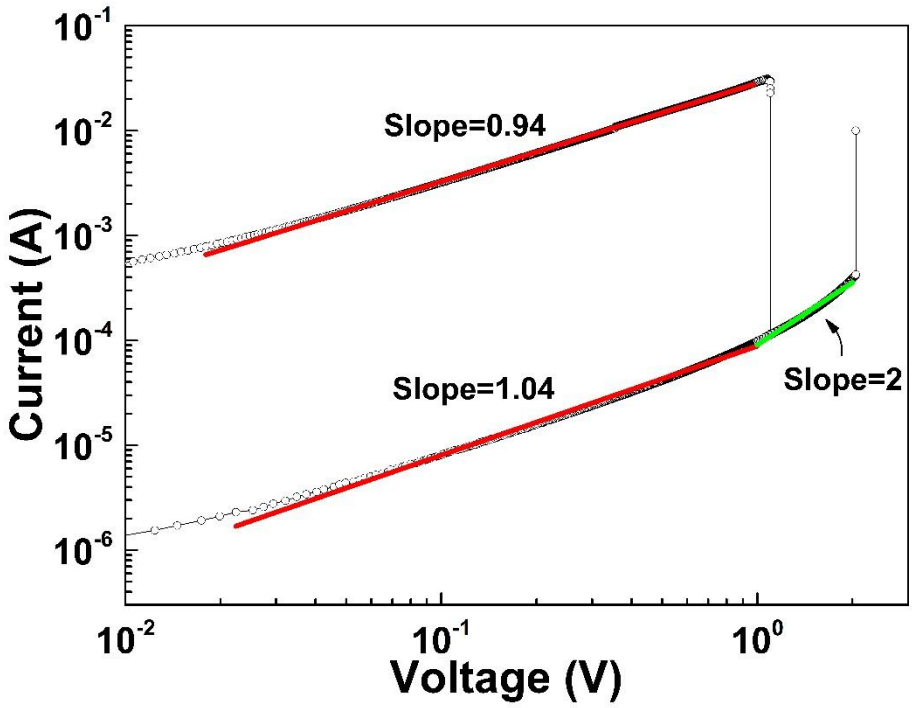


Figure 6-8 I-V curves of the unipolar resistive switching under negative bias, drawn in a log-log scale

The conduction mechanism of resistive switching under the positive bias is also investigated. From Figure 6.4(b), it can be seen that I-V curves at HRS shows two kinds of features: for one, the current at low electric field (<0.5V) is very low (<10^{-7}A), while for the other, the current is high. At higher voltage (>1V), the two I-V curves coincide. This may be attributed to the more complete rupture of conducting filaments in the lower current case. I-V curves of both HRS and LRS are replotted in a log-log scale (Figure 6.9). It can be found that I-V at LRS obeys the Ohmic conduction law with a slope of ~1, which implies the formation of conductive filaments in the 'ON' state. The conduction flow at HRS under the lower electric field also follows Ohmic conduction, but it is more complicated under higher electric field. Schottky emission, Poole-Frenkel emission and Schottky emission are well fitted to the curves with a slope of 6, 3.3 and 11.4, respectively. This implies that under intermediate electric field the conduction follows Schottky emission, while at higher voltage Poole-Frenkel emission dominates the conduction.

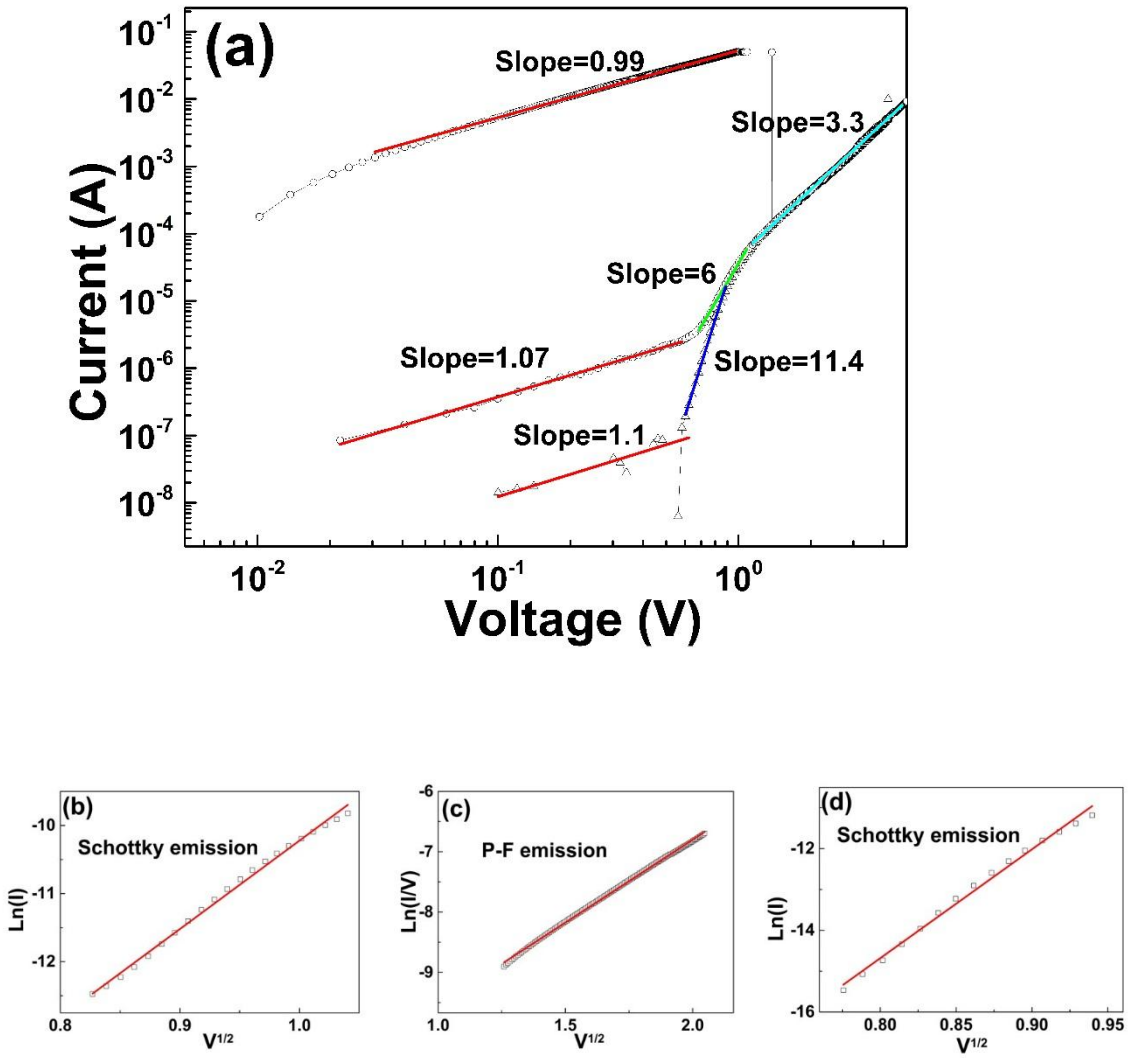


Figure 6-9 (a)I-V curves of the unipolar resistive switching under positive bias, drawn in a log-log scale; (b), (c) (d) are curve fittings to plots in (a) with a slope of 6, 3.3 and 11.4, respectively

Based on the above discussion on the I-V characterization and conduction mechanism, a conductive filamentary model is proposed to explain the resistive switching mechanism in the Au/CoO/TiO_2/Pt p-n junction memory device. Figure 6.10 schematically illustrates the resistive switching mechanism in this memory cell. At the pristine state, defects in both CoO and TiO_2 films are randomly distributed through the film, no conductive paths percolating through the films. The heterojunction structure exhibits rectifying conduction behaviour due to the existence of p-n junction at the CoO and TiO_2 interface. When a negative bias is applied to the Au electrode, negatively charged oxygen ions (excessive oxygen ions are intrinsic defects in p-type CoO) in the CoO film will migrate towards the anode, while positively charged oxygen vacancies (intrinsic

defects in the n-type TiO_2) in the TiO_2 film will travel towards the cathode. Conductive paths are formed in both CoO and TiO_2 films [13, 22, 81, 98]. When the electrical bias reaches a threshold value, the conductive path from the CoO side connects to that from the TiO_2 side; the top electrode and bottom electrode are then connected by the conductive path penetrating through both the CoO and TiO_2 films. The device is set to LRS (Figure 6.10(a)). The conductive filaments exhibit metallic conduction behaviour, so the conduction at LRS obeys Ohmic conduction (Figure 6.7(b)). When the bias is applied to the Au electrode without current compliance, the high current running through the conductive path will produce a large amount of Joule heat and lead the conductive filament to rupture. The device is reset to HRS (Figure 6.10(b)). In this scenario, conduction at the CoO/TiO_2 interface dominates and the heterostructure shows rectifying conduction behaviour. It can also be inferred that the conductive filament ruptures at the CoO/TiO_2 interface rather than inside the CoO or TiO_2 film, because if it ruptures within CoO or TiO_2 film, the conductive filament at the interface area would still exist and then the conduction at HRS would not show rectifying characteristic. This implies that conductive filaments at the interface are weaker than those inside the CoO and TiO_2 film. With respective to the 'bipolar' RS behaviour in Figure 6.5, the mechanism is similar. In the negative bias set process, conductive filaments form and penetrate both CoO and TiO_2 film to connect the top and bottom electrodes. The device is switched to LRS. In the positive bias reset process, as discussed in the previous section, the Joule heat induced filament rupture dominates, which results in the fuse of conductive filaments. The device is switched to HRS.

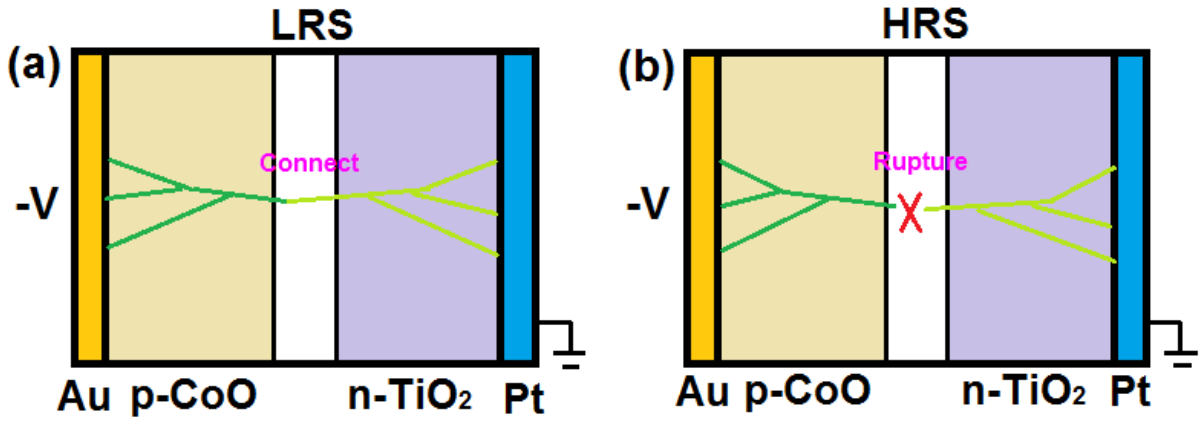


Figure 6-10 Schematic diagram of RS mechanism in the Au/CoO/TiO_2/Pt memory device at (a) LRS and (b) HRS

6.4. Summary

The RS properties in a p-type CoO/ n-type TiO_2 heterojunction were investigated. The prepared Au/CoO/TiO_2/Pt heterojunction structure exhibits unique nonpolar resistive switching behaviour, which is different from previously reported results in other p-n heterojunction memories. Under applied external bias, the memory device switches between rectifying behaviour (HRS) and Ohmic conduction (LRS). While the set process in the positive bias range is not very reproducible due to the unidirectional conduction nature of the CoO/TiO_2 p-n junction, set and reset process in the negative bias range can always occur. A conductive filamentary model is proposed to explain the resistive switching mechanism in the Au/CoO/TiO_2/Pt memory device. The formation and rupture of conductive filaments at the interface between CoO and TiO_2 is responsible for the set and reset process in the resistive switching, respectively. This study not only demonstrates good RS application potential in p-n junction memory cells, but also provides more evidence in understanding the RS mechanism in p-n heterojunction structures.

Chapter 7 Dependence of film growth temperatures on resistive switching properties in Au/CoO/TiO_2/Pt heterojunction structures

7.1. Introduction

Resistive random access memories (RRAMs) have been regarded as a very promising candidate for next generation non-volatile memories[90, 255]. One of the major challenges in the practical use of RRAMs remains in their reliable and stable operation. To be suitable for practical use, the resistive switching based memories should not only possess highly uniform switching parameters (such as set and reset voltages) in numbers of switching cycles, but also demonstrate stable resistances (or conductance) at both HRS and LRS in consecutive sweeping cycles. To date, the most widely accepted mechanism for resistive switching phenomenon is the formation and fuse of conductive filaments[90], which are consist of microstructural defects in the film bulk. Therefore, tuning the defect concentration in the film is a direct and effective way to change the conductive filament formation process for improved switching performance. Adjusting the film growth parameters (such as growth temperatures) would be an effective approach to tune the defect concentration and microstructural uniformity in the film bulk and thus obtain enhanced RS performance.

In this section, the impact of the growth temperatures of either CoO layer or TiO_2 layer on the resistance switching property of the Au/CoO/TiO_2/Pt memory cell is investigated. A growth temperature range that leads to good RS performance is suggested.

7.2. Experimental details

P-type CoO/n-type TiO_2 thin film heterojunction structures are fabricated on a Pt/Ti/SiO_2/Si (001) substrate by an oxygen-plasma-assisted molecular beam epitaxy (OPA-MBE) method. SiO_2(50nm), Ti(20nm) and Pt(100nm) layers are successively deposited on Si (001) substrate by means of electron beam evaporation at room temperature. Pt works as the bottom electrode for current-voltage (I-V) characteristic measurement. TiO_2 and CoO thin films are deposited on the Pt layer successively in the MBE chamber. To investigate the effect of CoO growth temperature on the RS property, during the TiO_2 thin films deposition, substrate temperature is kept at 300 ℃, while

growth temperature for CoO thin film varies from room temperature (RT), 150 ℃, 300 ℃, 375 ℃, 450 ℃ to 600 ℃. To explore the impact of TiO_2 growth temperature on RS property, during the TiO_2 thin films deposition, substrate temperature varies from 300 ℃, 500 ℃ to 650 ℃, while growth temperature for CoO thin film is kept at 300 ℃. Chamber pressure during deposition is kept at 5×10^{-6} Torr for all the films with an oxygen plasma power of 300W. The effusion cell temperatures for Ti and Co during the deposition are 1580 ℃ and 1450 ℃, respectively. Deposition time for both Ti and Co is 1h. Gold top electrodes with a diameter of 200μm are coated by DC magnetron sputtering at room temperature through a metal shadow mask. X-ray diffraction (XRD) is used to identify the phase structure in the CoO/TiO_2 bilayer; scanning electron microscopy (SEM) is used to check the microstructures of the bilayers; Secondary ion mass spectroscopy (SIMS) is used to investigate the film composition in a depth profile. To investigate the resistive switching properties of the $Au/CoO/TiO_2/Pt$ memory cells, I-V curves are measured at room temperature in a voltage-sweeping mode using a Keithley 2400C source meter and Everbeing-4 probe station.

7.3. Results

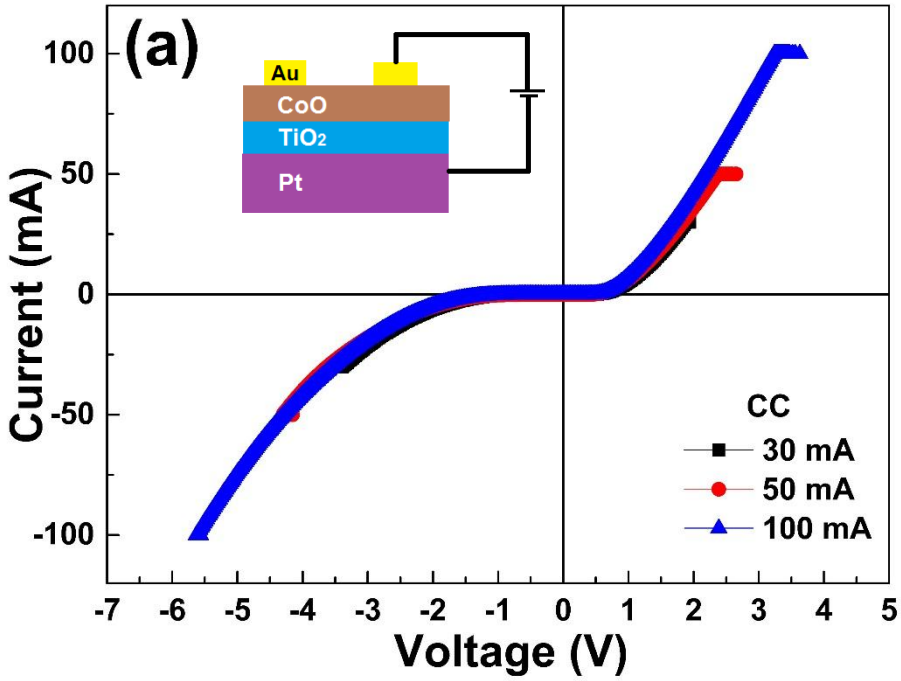
7.3.1. RS properties characterization

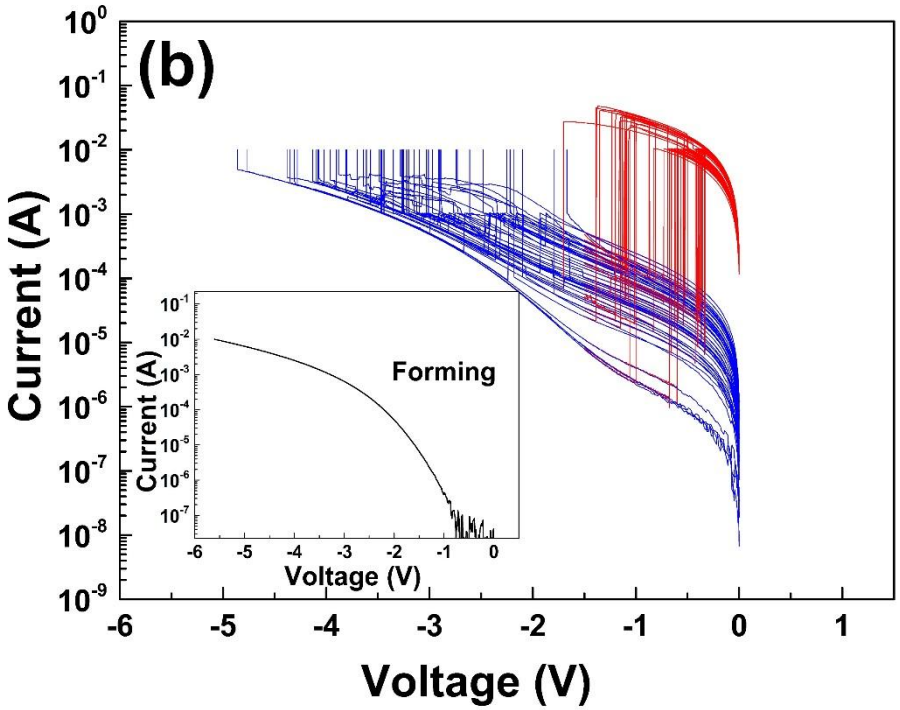
(1) CoO growth temperature effect

Firstly, the impact of CoO growth temperature on the RS property of the $Au/CoO/TiO_2/Pt$ heterojunction is investigated. During the TiO_2 thin films deposition, substrate temperature is kept at 300 ℃, while growth temperature for CoO thin film varies from room temperature (RT), 150 ℃, 300 ℃, 375 ℃, 450 ℃ to 600 ℃. For convenience, $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) samples, with CoO prepared at RT, 150 ℃, 300 ℃, 375 ℃, 450 ℃ and 600 ℃, are denoted as S-RT, S-150, S-300, S-375, S-450 and S-600, respectively.

The resistive switching properties of these $Au/CoO/TiO_2/Pt$ heterojunction structures are investigated. The electrical circuit connection is schematically illustrated in the inset of Figure 7.1(a). During the measurement, Pt bottom electrode is grounded and electrical bias is applied to Au top electrode. First, to turn the $Au/CoO/TiO_2/Pt$ structure into a memory device, an ‘electroforming’ process is required. A compliance current (CC) of 10mA is set to prevent the device from permanent breakdown. The voltage is

then swept from 0V to -10V while the current is measured. For sample S-RT, there is no electroforming occurring. Even if we increase the CC to as high as 100mA, as seen in Figure 7.1(a), no abrupt current increase can be observed. This means that for Au/CoO/TiO_2/Pt sample in which CoO is prepared in RT, there is no resistive switching process occurring in the device under external electrical field. For the S-150 sample, there is abrupt current increase happening just before the current reaches CC (10mA), and subsequent voltage sweeping reveals a unipolar resistive switching characteristic in the sample (Figure 7.1(b)). For samples with CoO prepared at 300 ℃ and 375 ℃, when the voltage is swept to a threshold value, the current increases abruptly and the samples are set from a high resistance state (HRS) into a low resistance state (LRS). In the following successive voltage sweepings, the Au/CoO/TiO_2/Pt devices can be switched between LRS and HRS, showing reproducible unipolar switching behaviour, seen in Fig. 1(c) and (d). Because of the unidirectional nature of current flow in the p-n junction, the positive voltage cannot induce resistive switching in these samples. The current quickly increases to CC before resistive switching could occur. For CoO thin films prepared at 450 ℃ and 600 ℃, the original samples are at low resistance state, which means the defects in these films have penetrate the film bulk and connect the top and bottom surface. Under this circumstance, the original current through the film is very high and larger than the compliance current, applying external electric field cannot switch it to high resistance state, so there is no RS behaviour can be observed in these samples.


(a)
Au
CoO
TiO2
Pt
Current (mA)
Voltage (V)
CC
30 mA
50 mA
100 mA


(b)
Current (A)
Voltage (V)
Forming
Current (A)
Voltage (V)

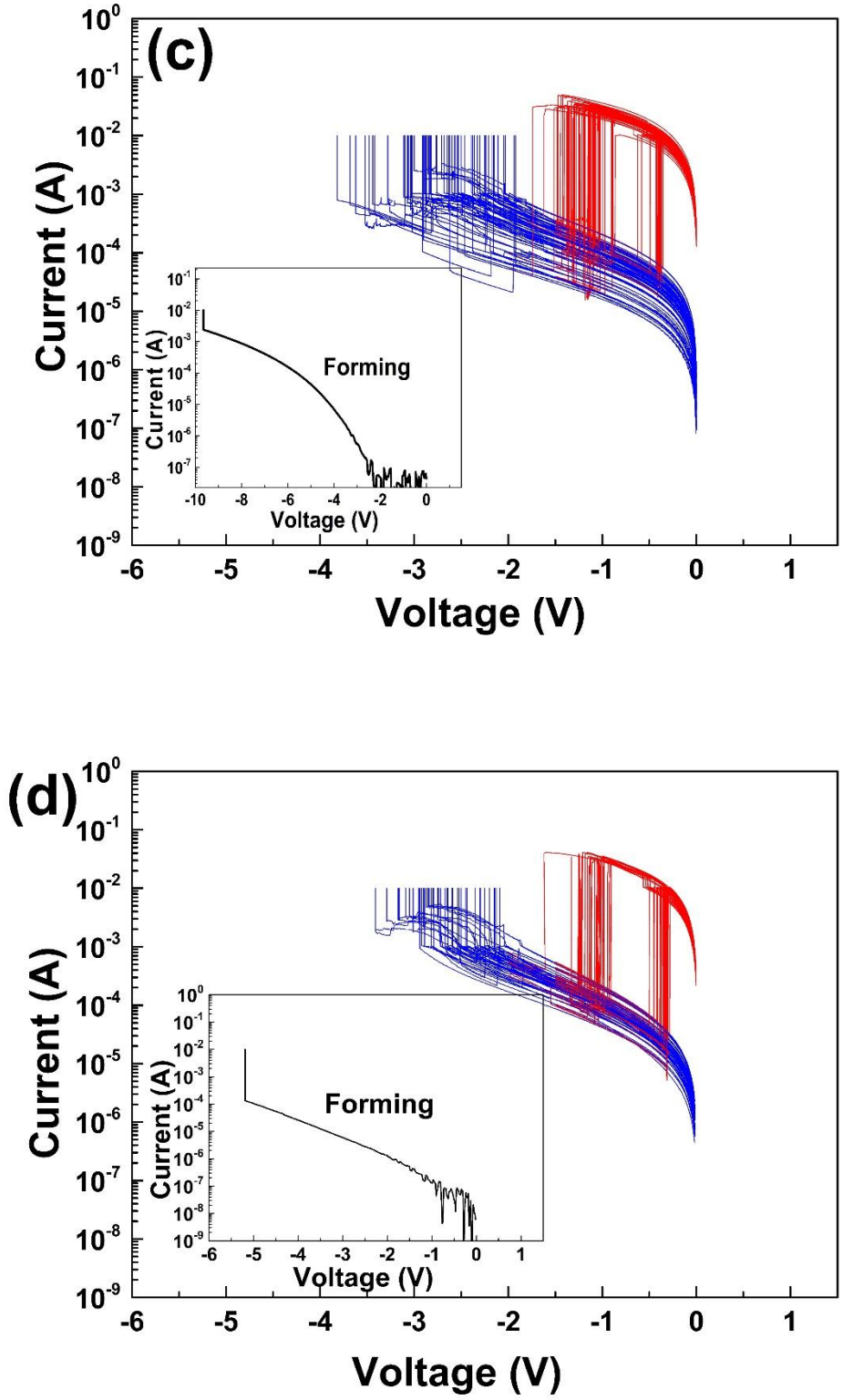


Figure 7-1 I-V curves of Au/CoO/TiO_2/Pt heterojunction structures: (a) S-RT, (b) S-150, (c) S-300, and (d) S-375

To evaluate the reproducibility and stability of the Au/CoO/TiO_2/Pt memory devices, endurance test was performed on resistance-switchable samples S-150, S-300 and S-375, respectively. The distribution of resistance at HRS and LRS with a reading voltage of -0.2V, as well as the distribution of set and reset voltages during 50 successive sweeping cycles, are shown in Figure 7.2. It can be found that all three samples exhibit a large resistance ratio of HRS to LRS, about two orders of magnitude, which is large enough for practical application. With respect to the distribution of resistance at HRS and LRS, it can be seen that resistance at LRS in all three samples is quite stable during 50 sweeping cycles, but the HRS resistance undergoes relatively large fluctuation in S150 and S-300 while there is only a slight fluctuation for S-375. In addition, it can be found that S-375 exhibits most densely distributed set and reset voltages in the 50 successive sweeping cycles. The dense distribution of set and reset voltage is favourable for avoiding failure in the reading and writing process of the memory cell.

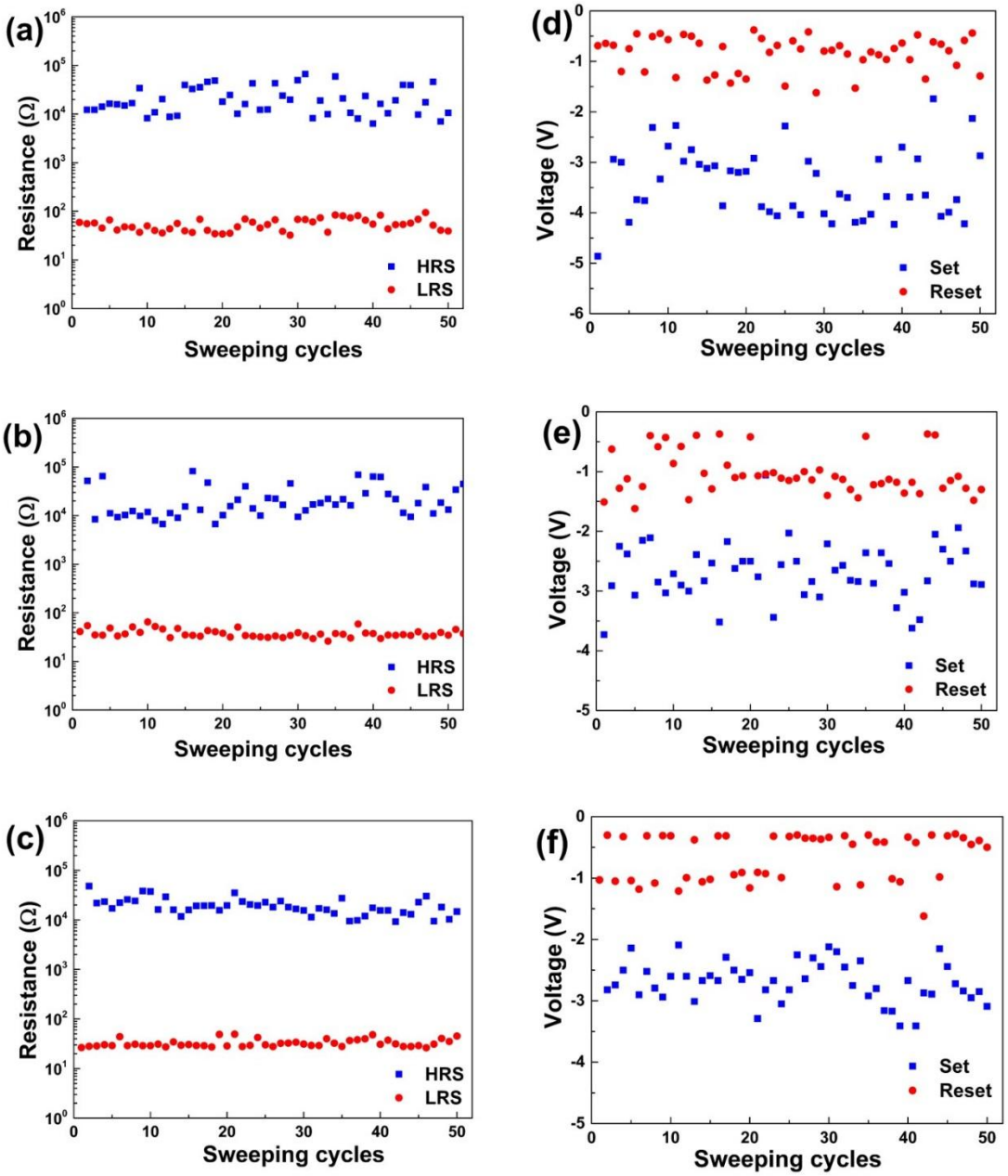


Figure 7-2 Left column: distribution of resistance at HRS and LRS; Right column: distribution of set and reset voltages in Au/CoO/TiO_2/Pt memory device for 50 sweeping, (a)(d): S-150, (b)(e): S-300, and (c)(f): S-375. Reading voltage is -0.2V.

Figure 7.3 presents the resistances at different resistive states in the Au/CoO/TiO_2/Pt memory devices prepared with different CoO growth temperatures. As can be seen, resistance at the pristine state increases with increasing CoO growth temperature. Resistance at HRS and LRS does not change much with increased growth temperature.

Based on the above I-V results, it can be inferred that higher CoO growth temperature (>300 ℃) is better to achieve good switching stability and sustainability. Too higher growth temperature (>450 ℃), however, may result in the deterioration/disappearance of the resistive switching property. The reason for this deterioration will be explored by examining the microstructures of the films in the following part.

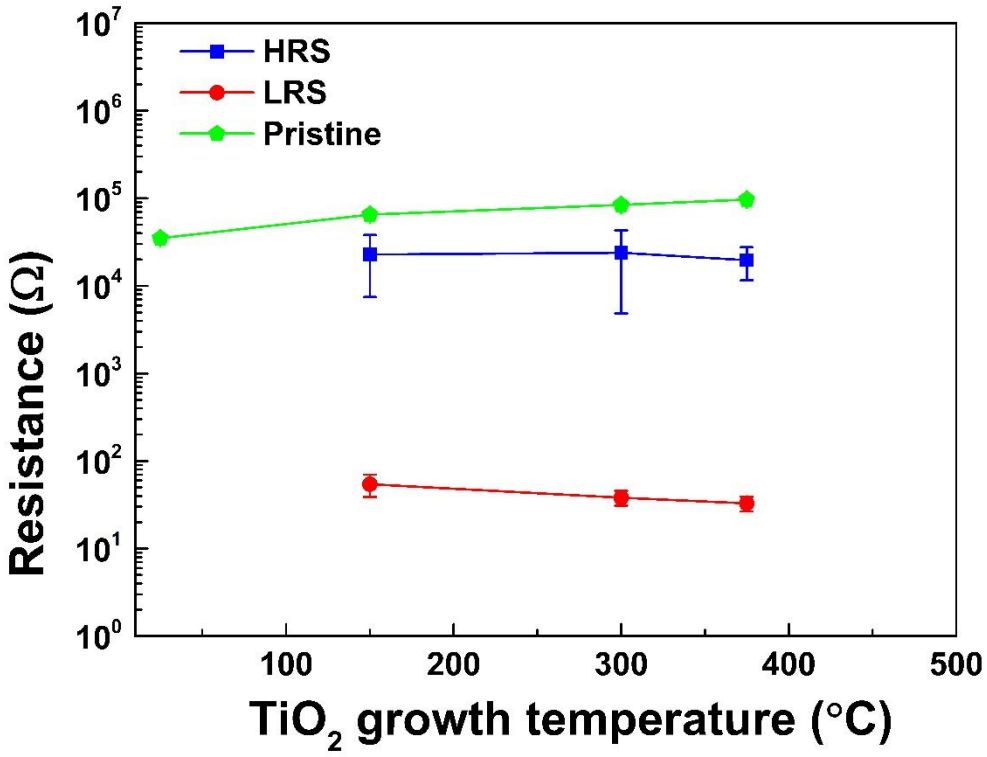


Figure 7-3 Resistance of the Au/CoO/TiO_2/Pt heterojunction structures with different CoO growth temperatures.

(2) TiO_2 growth temperature effect

The impact of TiO_2 growth temperature on the RS property of the Au/CoO/TiO_2/Pt heterojunction is also studied. The growth temperature for TiO_2 thin film varies from 300 ℃, 500 ℃ to 650 ℃, while the CoO growth temperature is kept at 300 ℃.

Figure 7.4 shows the I-V curves of the Au/CoO/TiO_2/Pt heterojunction structures with TiO_2 grown at 300 ℃, 500 ℃ and 650 ℃, respectively. It can be found that all memory devices exhibit reproducible unipolar resistive switching behaviour over 50 sweeping cycles. An electroforming process is needed to start the switching process. The distribution of resistance at HRS and LRS and distribution of set and reset voltages of the Au/CoO/TiO_2/Pt memory cells for 50 successive sweeping cycles are presented in Figure 7.5. All samples demonstrate a large resistance ratio of HRS to LRS, greater than two orders of magnitudes, which is large enough for practical application. The distribution of resistance at HRS gets narrower at higher growth temperature, indicating more stable switching process between HRS and LRS. The distribution of set and reset voltages, however, does not get improved with increased TiO_2 growth temperature.

Figure 7.6 shows the resistance of Au/CoO/TiO_2/Pt memory devices prepared with different TiO_2 growth temperatures. It can be seen that resistance at the pristine state increases with increasing TiO_2 growth temperature. Resistance at HRS also increases with increasing growth temperature, which is favourable to enlarge the memory window (resistance ratio of HRS to LRS). Resistance at LRS does not increase too much with increasing growth temperature.

Based on the above results, it can be inferred that Au/CoO/TiO_2/Pt memory devices with higher TiO_2 growth temperatures are more favourable to get larger memory window and more stable switching process.

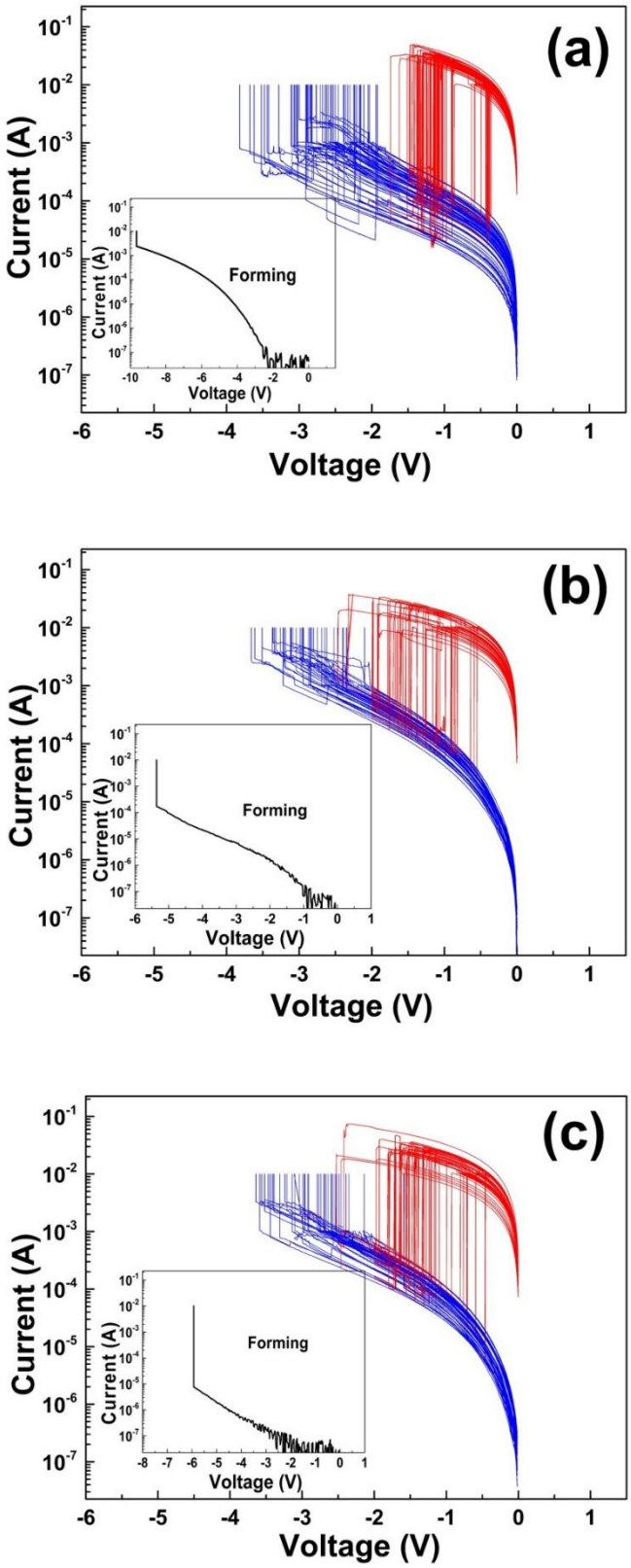


Figure 7-4 I-V curves of Au/CoO/TiO_2/Pt heterojunction structures with TiO_2 growth temperature of (a) 300 ℃, (b) 500 ℃ and (c) 650 ℃.

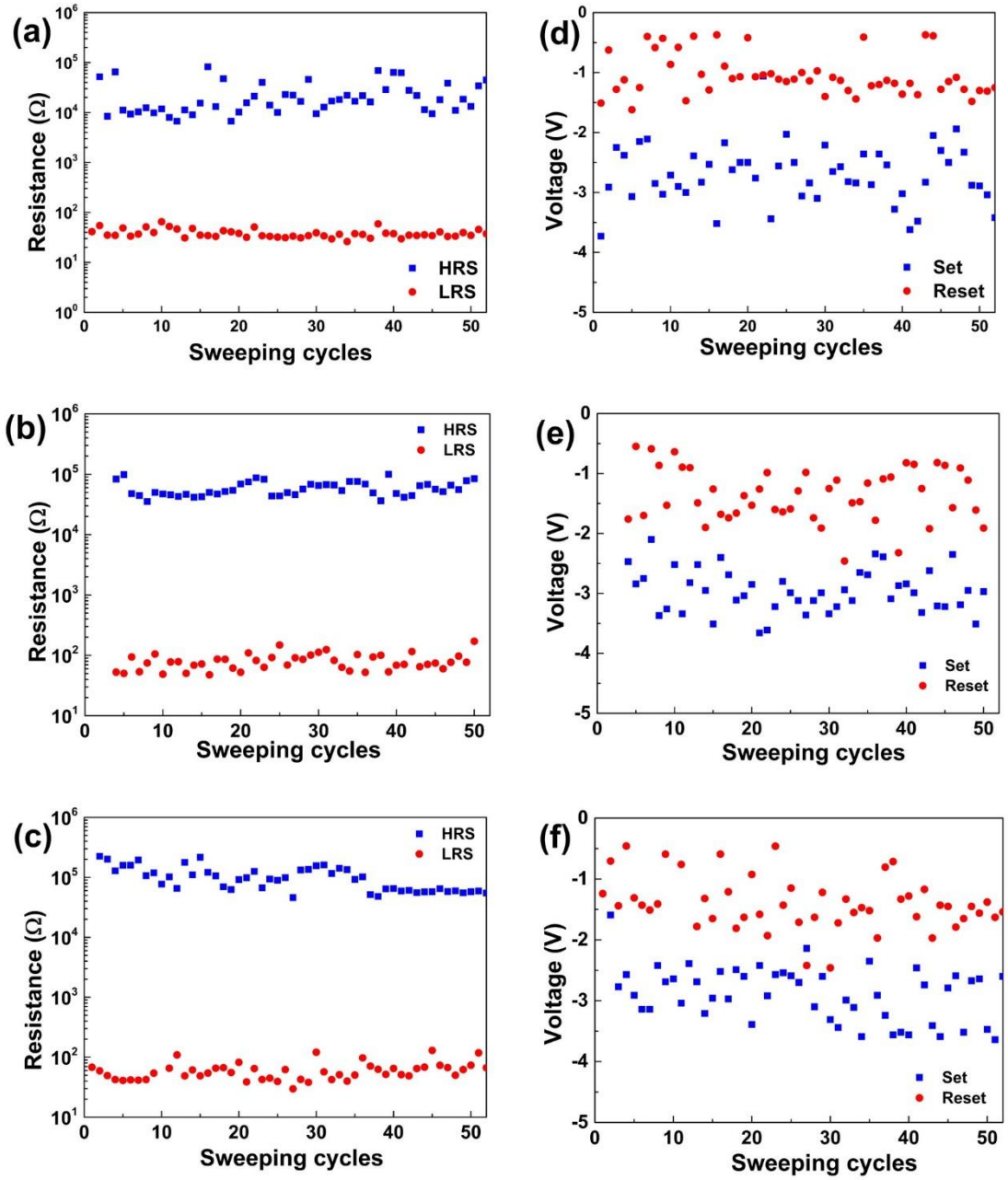


Figure 7-5 Left column: distribution of resistance at HRS and LRS; Right column: distribution of set and reset voltage in Au/CoO/TiO_2/Pt memory device for 50 sweeping cycles; (a)(d): TiO_2 grown at 300 ℃, (b)(e): TiO_2 grown at 500 ℃, (c)(f): TiO_2 grown at 650 ℃.

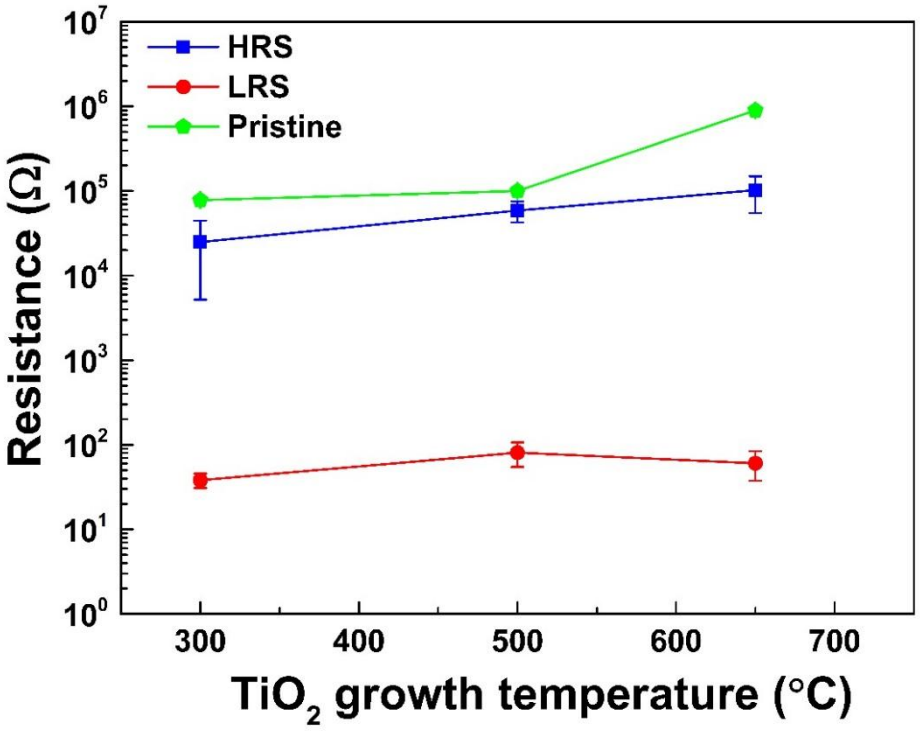


Figure 7-6 Resistance of the Au/CoO/TiO_2/Pt heterojunction structures with different TiO_2 growth temperatures.

Au/CoO/TiO_2/Pt memory devices with higher CoO deposition temperature (≥450 ℃) are also prepared. It is found that devices with CoO growth temperature higher than 450 ℃ show no RS behaviour. Figure 7.7 summarizes the film growth temperatures used to prepare the Au/CoO/TiO_2/Pt memory devices, and the corresponding RS properties are also indicated (Squares denote good RS property, while crosses denote poor or no RS property).

Based on this graph, we can find the growth temperature range which leads to good RS property in the Au/CoO/TiO_2/Pt memory devices. RT growth usually results in amorphous oxide, of which the resistance is relatively low. As can be seen from Figure 7.1(a), it shows no RS behaviour if the resistance is too low. Therefore, RT growth is discarded for film fabrication. In our sample preparation process, the deposition of TiO_2 is ahead of CoO growth. To avoid the annealing effect during CoO growth on the microstructure of TiO_2 beneath, the growth temperature of TiO_2 is set to no lower than 300 ℃. The shadowed area in Figure 7.7 indicates the growth temperature range which gives good RS property in the Au/CoO/TiO_2/Pt memory devices. From the discussion in

the part (1) and (2), it can be found that higher growth temperature leads to higher resistance in the memory device, which is favourable to the start of RS process and the enlargement of memory window. In addition, devices fabricated under high temperatures show more stable resistive switching process. Therefore, higher growth temperature range is suggested as preferable preparation temperature range for our Au/CoO/TiO_2/Pt memory devices.

The RS property is closely related to the microstructure of the oxide layers. The difference in RS properties may come from the variation in microstructures under different growth temperatures. Therefore, the microstructure of the oxide layers would be investigated.

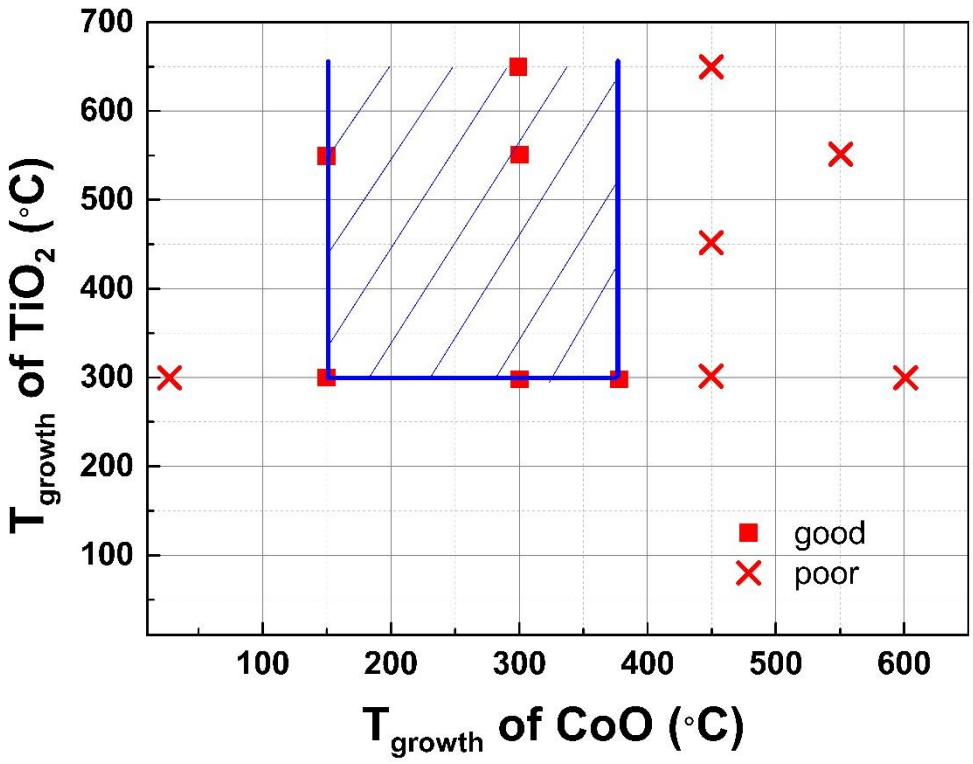


Figure 7-7 Growth temperature range for preparing Au/CoO/TiO_2/Pt heterojunction structures with good RS properties. Squares denote growth temperatures producing good RS property, while crosses denote growth temperatures resulting in poor RS property.

7.3.2. Structural characterization

The variation in RS properties of the Au/CoO/TiO_2/Pt heterojunction structures prepared with different deposition temperatures may come from the variation in their microstructures. In this part, XRD is used to check the crystallinity of the prepared samples; SEM is used to examine the sample surface morphology; SIMS is used to investigate the film composition in depth profile.

The crystalline structures of the as-prepared CoO/TiO_2/Pt/Ti/SiO_2/Si (001) thin films (S-RT, S-150, S-300, S-375, S-450 and S-600) were investigated by XRD, seen in Figure 7.8. When growth temperature is lower than 375 ℃, in addition to diffraction peaks for Pt and Si from the substrate, only peaks at 36.6 ° and 77.5 ° (corresponding to CoO (111) and (222) planes, respectively) can be found in the XRD patterns. The CoO phase exhibits a textured structure with a preferential growth orientation of [111]// [001] Si. It can also be found that as growth temperature increases from RT to 375 ℃, the intensities of CoO (111) and (222) peaks become stronger at higher growth temperatures, which indicates that the crystallinity of CoO phase increases with increased growth temperature. However, no diffraction peaks are found for TiO_2 phase. This means that the TiO_2 phase is amorphous or only partially crystallized but beyond the detection limit of our XRD. No impurity phases can be detected in the XRD patterns. Further increasing the growth temperature of CoO (>450 ℃) leads to phase transformation in the films (Figure 7.8(a) and (b)) and the resistive switching property disappears. Figure 7.9 displays the XRD patterns of CoO/TiO_2/Pt/Ti/SiO_2/Si (001) thin films with different TiO_2 growth temperature (300 ℃, 500 ℃ and 650 ℃). It can be seen that the XRD patterns look the same as in Figure 7.8, in which only CoO phase can be identified.

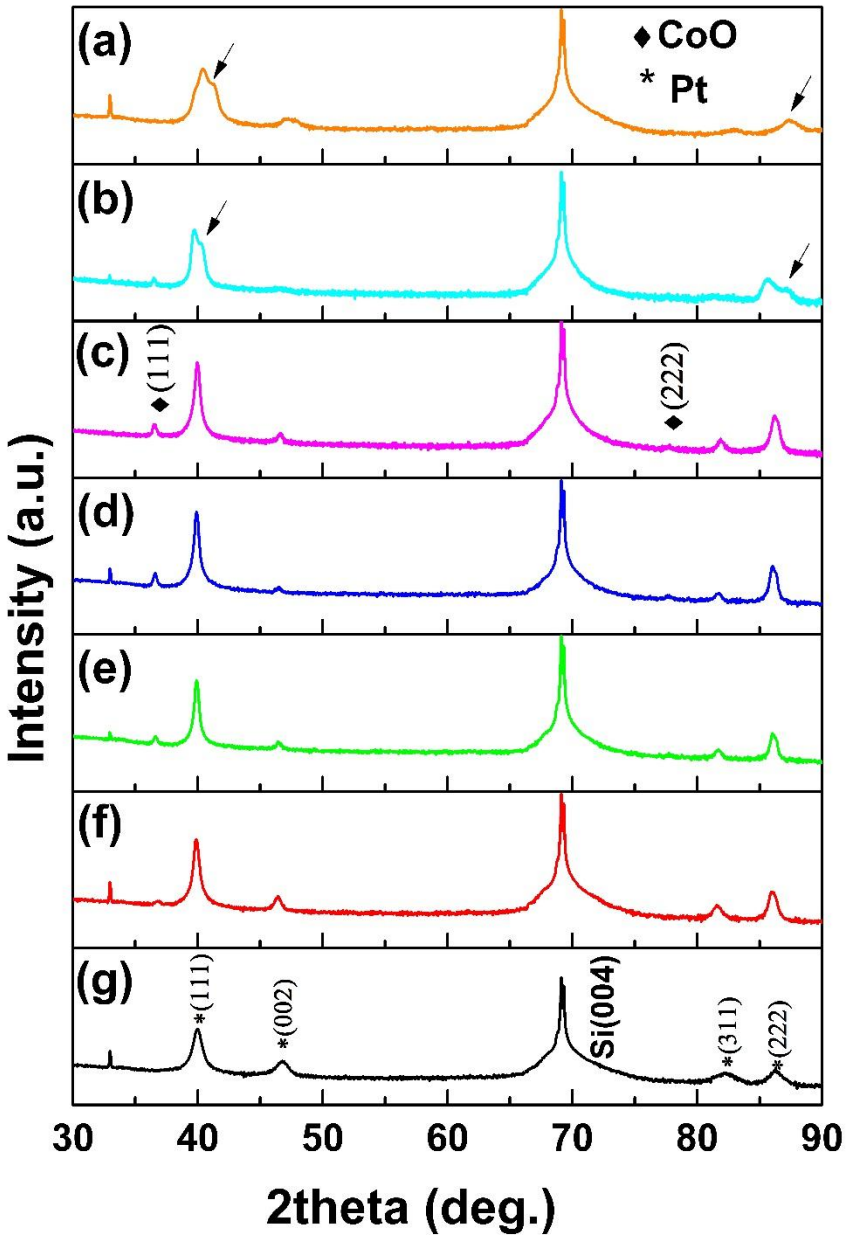


Figure 7-8 XRD patterns of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films, (a) S-600, (b) S-450, (c) S-375, (d) S-300, (e) S-150, (f) S-RT and (g) Pt/Ti/SiO2/Si (001) substrate. Arrows indicate phase transformation.

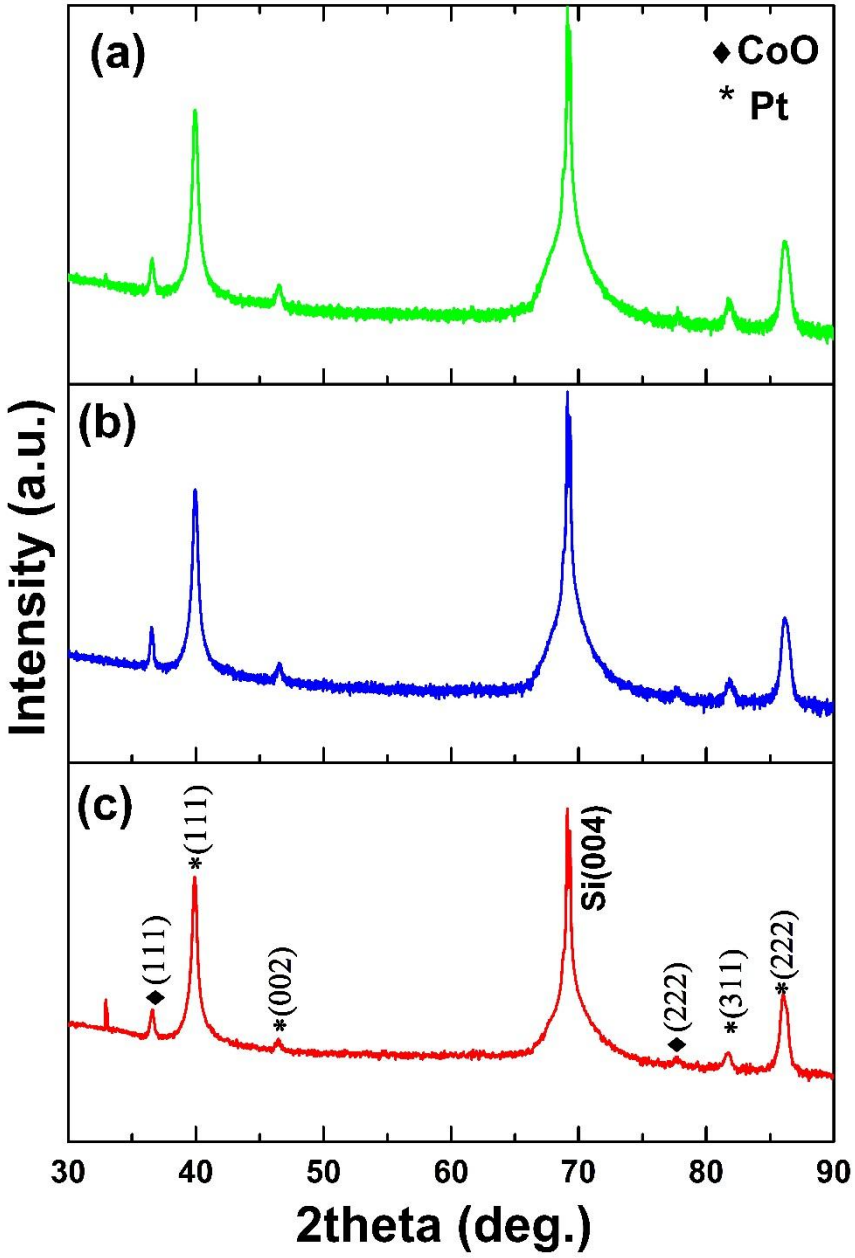


Figure 7-9 XRD patterns of CoO/TiO_2/Pt/Ti/SiO_2/Si (001) thin films with TiO_2 prepared under (a) 650 ℃, (b)500 ℃ and (c) 300 ℃

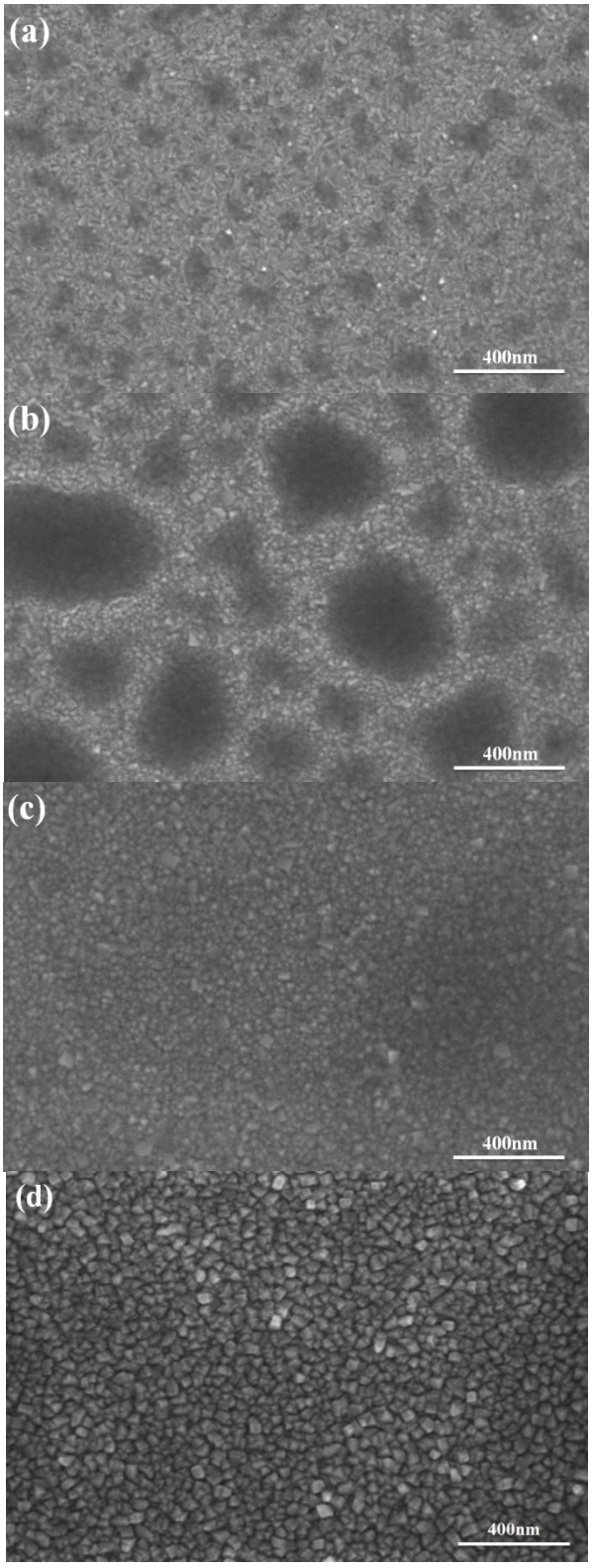
Figure 7.10 shows the microstructures of the CoO phase prepared under different substrate temperatures. It can be seen that as growth temperature increases, the size of the CoO grains becomes larger and the grain shape transforms from irregular shape to more regular cubic shape. At higher deposition temperature, the CoO phase exhibits homogeneous cubic shape and ordered arrangement, indicating very good crystallinity. However, when temperature is higher than 450 ℃, as indicated by XRD results, phase transformation occurs and the grains becomes less regular than at lower temperatures. The dark regions may come from the contrast difference on the sample surface. This may result from the sample preparation process.

Figure 7.11 presents the SIMS elements depth profile of the $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with CoO prepared under 600 ℃, 450 ℃ and 300 ℃, respectively. It can be found that under lower growth temperature (Figure 7.11(a)) the prepared thin films exhibit a clear stacked structure ($CoO\text{-}TiO_2\text{-}Pt\text{-}Ti\text{-}Si$). As the growth temperature increases, however, metal element diffusion could be observed. There is a trend that cobalt would diffuse towards inside at higher temperatures. It can be clearly seen in Figure 7.11(a) that cobalt has diffused into inner Pt layer. Titanium could even be found near the surface layer. This may be caused by the diffusion of cobalt and reaction with Ti or Pt that cause the aggregation of cobalt-related species and leave titanium exposed on the surface. The element depth profiles are consistent with the XRD results which also indicate phase reaction at higher growth temperature.

Figure 7.12 shows the SEM surface morphology of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with TiO_2 prepared under 300 ℃, 500 ℃ and 650 ℃, respectively (CoO growth temperature is kept at 300 ℃). It can be seen that the underlying TiO_2 layer has an impact on the morphology of CoO phase. Higher preparation temperature leads to more homogeneous distribution of crystal size. Figure 7.13, however, indicates that higher TiO_2 growth temperature has no obvious influence on the chemical distribution in depth profile.

Based on the above microstructural and compositional characterization of the $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) heterojunction structures prepared under different temperatures, it can be inferred that the degradation of RS properties prepared at higher temperature may be ascribed to cobalt-related diffusion and phase transformation. While increasing TiO_2 growth temperature to as high as 650 ℃ does not lead to phase

transformation when CoO growth temperature is low, growing CoO at higher temperatures (>450 ℃) leads to phase transformation and RS property degradation. Therefore, the growth temperature of CoO should be limited below 450 ℃.



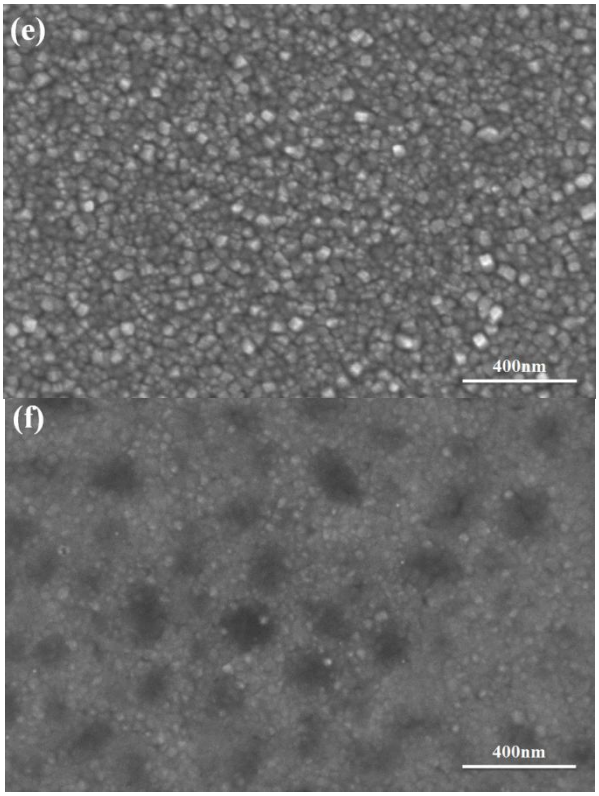


Figure 7-10 SEM surface morphology of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with CoO prepared under (a) RT, (b) 150 ℃, (c) 300 ℃, (d) 375 ℃ (e) 450 ℃ and (f) 600 ℃

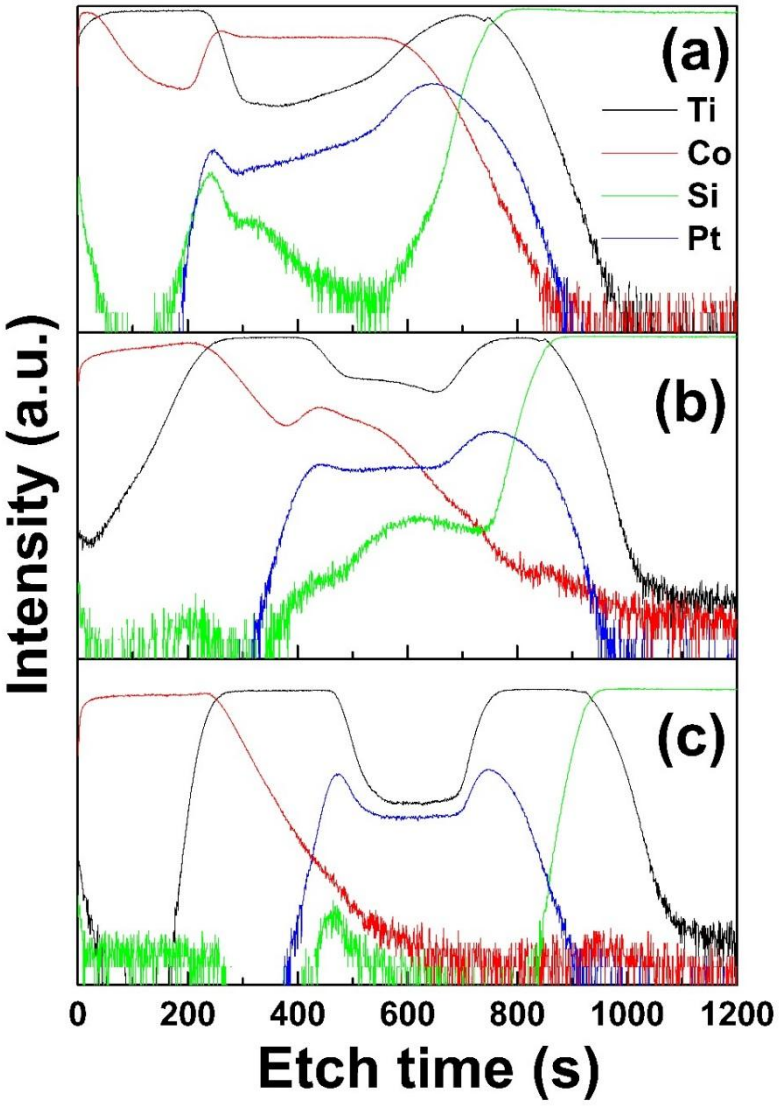


Figure 7-11 SIMS elements depth profile of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with CoO prepared under (a) 650 ℃, (b) 450 ℃ and (c) 300 ℃

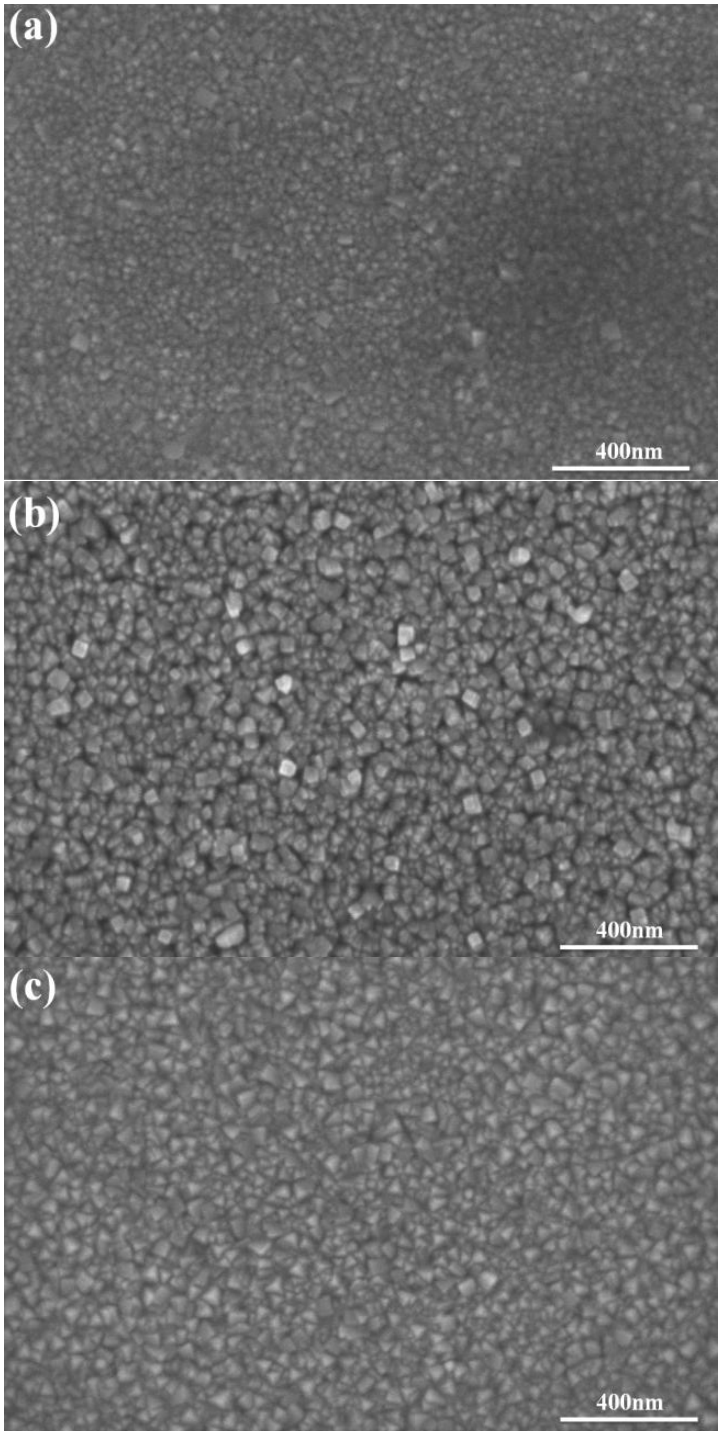


Figure 7-12 SEM surface morphology of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with TiO_2 prepared under (a) 300 ℃, (b)500 ℃ and (c) 650 ℃

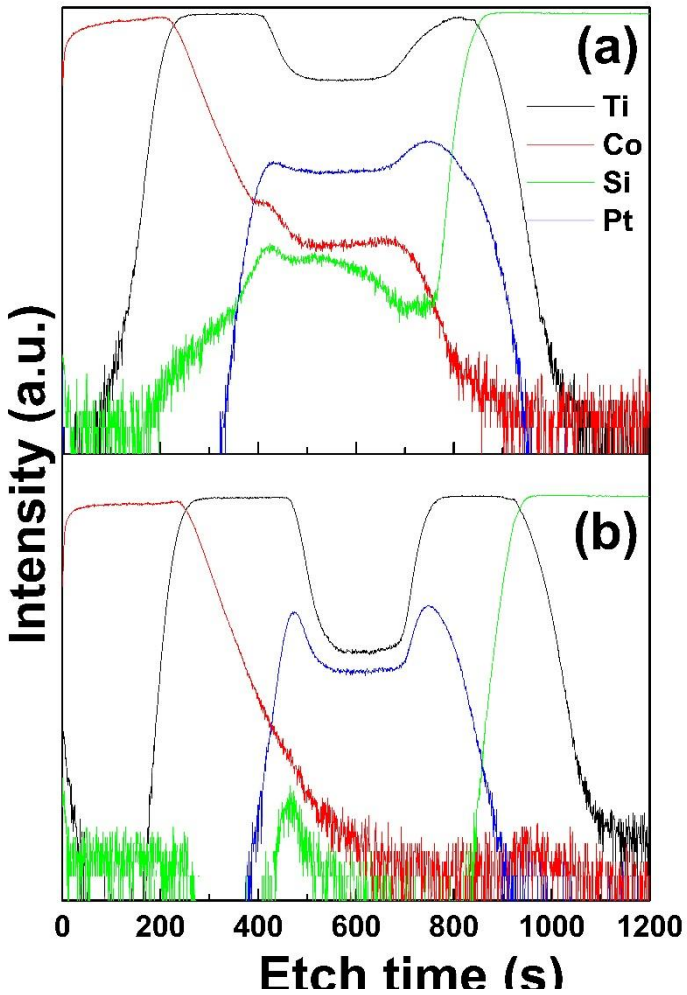


Figure 7-13 SIMS elements depth profile of $CoO/TiO_2/Pt/Ti/SiO_2/Si$ (001) thin films with TiO_2 prepared under (a) 650 ℃ and (b) 300 ℃

7.4. Discussions

The enhanced resistive switching performance (stable distribution of resistance and set and reset voltages during sweeping cycles) with increased film growth temperature of the $Au/CoO/TiO_2/Pt$ memory device may result from the more orderly arranged microstructure.

At low growth temperature, the film crystallinity is low and the less ordered structure contains high defect density. The high-density defects provide easy pathway for electrons to flow, leading to lower resistance of the film with lower growth temperature. At room temperature, the defect density is so high that percolated conductive path has already formed in the film which leads to low resistive state in the original film. There

is no resistive switching behaviour in this film. As growth temperature increases, the phase crystallinity becomes better. More atoms arrange in the lattice in an ordered way, leaving fewer defects in the film. The phase grains exhibit more regular shapes. The defects disperse in the film and it requires an external electric filed to align the defects and form a conductive path penetrating the film bulk. In film prepared at lower temperature (such as 150 ℃ and 300 ℃), the defect density is quite high and several different conductive paths may form in the film bulk simultaneously. And the conductive paths may also contain many branches. During the consecutive switching cycles, the rupture of the conductive filaments may be incomplete and this may lead to variation in set and reset voltages of the following switching cycles. As with the incomplete rupture of conductive filaments, the resistance of the memory device may also vary from cycle to cycle.

Too high growth temperature may make resistive switching property deteriate. The degradation of RS property at higher CoO growth temperature (>450 ℃) may be attributed to cobalt diffusion and phase transformation, as can be seen in XRD (Figure 7.8) and SIMS measurement (Figure 7.11). When it comes to TiO_2 phase, increasing growth temperature to 650 ℃ does not lead to phase transformation or obvious element diffusion. Actually in the investigated temperature range , no TiO2 phase change has been detected and no obvious degradation of RS property is observed with increasing TiO_2 growth temperature.

The impact of TiO_2 growth temperature on the RS property of the Au/CoO/TiO_2/Pt memory device may come from a similar reason as CoO. Though the crystallinity of TiO_2 on Pt cannot be recognized from XRD directly (Figure 7.9), its effect on surface morphology of CoO phase can be checked (Figure 7.12). Higher preparation temperature leads to more homogeneous distribution of crystal size, which is favourable to getting more stable RS process.

Based on the above discussions, an optimized growth temperature region is suggested for the CoO/TiO_2/Pt/Ti/SiO_2/Si (001) heterojunction structure (shadowed area in Figure 7.7). It should be noted that 450 ℃ may be the threshold temperature of second phase transformation, as in the SIMS depth profile of S-375 sample, diffusion can be recognized already, though no serious resistive switching degradation is observed.

7.5. Summary

The impact of thin film growth temperature on the RS properties of the Au/CoO/TiO_2/Pt p-n heterojunction structure was investigated. It is found that higher growth temperature is favourable to get better RS performance with larger memory window and more stable RS process. However, too high CoO growth temperature (≥450 ℃) may result in secondary phase precipitation and degradation in RS properties. Therefore, an optimized growth temperature range is suggested for fabrication of the CoO/TiO_2 p-n heterojunction RS memories.

Chapter 8 Effect of CoO thin film thickness on the resistive switching stability of Au/CoO/TiO_2/Pt heterojunction structure

8.1. Introduction

The stability of the resistive switching memory devices during consecutive operation is an important issue in the practical applications. Cycle-to-cycle variation of the switching parameters, such as the resistance at HRS and LRS, as well as the set and reset voltages, may bring problems in reproducibility of the memory device, or even failure during the operation. Many methods have been proposed to improve the uniformity of resistive switching parameters, such as element doping[256, 257], interlayer insertion between the electrodes and insulating film[258-260] and nano-metal embedding[219, 261]. Quite few works have been performed on studying the relationship between layer thickness and resistive switching uniformity. As conductive filaments are widely accepted to play the role in the RS process and different connection and rupture behaviour may happen in insulating layers with different thickness[262], the stability of resistive switching performance in thin films with different thickness may be different[263].

In this study, the effect of CoO layer thickness on the resistive switching stability of Au/CoO/TiO_2/Pt heterostructure is investigated. The thickness impact on the cycle-to-cycle variation in resistance at HRS and LRS and set and reset voltages is evaluated.

8.2. Experimental details

The p-type CoO/n-type TiO_2 thin film heterojunction structures were fabricated on a Pt/Ti/SiO_2/Si(001) substrate by an oxygen-plasma-assisted molecular beam epitaxy (OPAMBE) method. SiO_2 (50nm), Ti (20nm) and Pt (100nm) layers were successively deposited on the Si (001) substrate by means of electron beam evaporation at room temperature. Pt works as the bottom electrode in the memory cell. The TiO_2 and CoO thin films were deposited on the Pt layer successively in the MBE chamber. During the deposition, the substrate temperature was 300 ℃ and gas pressure was 5×10^{-6} Torr with an oxygen plasma power of 300W. The effusion cell temperatures for Ti and Co were 1580 ℃ and 1450 ℃, respectively. The thickness of TiO_2 layer was kept constant of

30nm, while CoO thickness time varied from 10nm, 30nm, 60nm to 100nm. Gold top electrodes with a diameter of 200μm were coated on top of the CoO layer by DC magnetron sputtering at room temperature through a metal shadow mask. X-ray diffraction (XRD) was used to examine the crystalline structure of the CoO/TiO_2 bilayer. To investigate the resistive switching behaviour of the $Au/CoO/TiO_2/Pt$ memory cell, the current versus voltage (I-V) curves were measured at room temperature in a voltage-sweeping mode using a Keithley 2400C source meter.

8.3. Results and discussion

The crystalline structures of the prepared $CoO/TiO_2/Pt$ heterostructures were investigated by XRD. As shown in Figure 8.1, the diffraction peaks at 36.6 °, 42.4 ° and 77.5 ° correspond to the CoO (111), (200) and (222) planes, respectively, indicating a polycrystalline nature of the as-grown CoO thin films. The diffraction peaks of TiO_2, however, cannot be found in the XRD patterns, which indicate that the prepared TiO_2 thin film is amorphous, or only partially crystallized but beyond the detection limit of our XRD. No impurity phase peaks except for those from $Pt/Ti/SiO_2/Si$ substrate can be detected in the XRD patterns. As can also be seen, the intensity of the diffraction peaks of CoO phase increases with increasing film thickness.

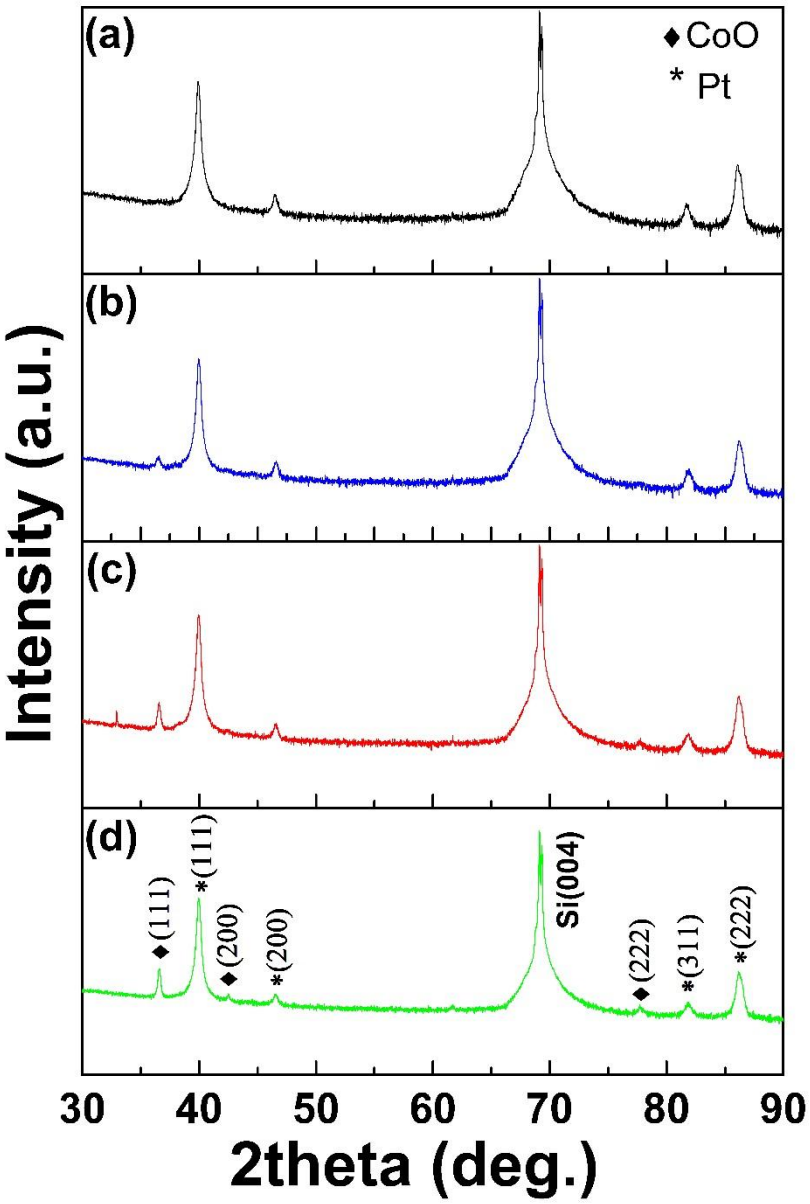


Figure 8-1XRD patterns of the $CoO/TiO_2/Pt/Ti/SiO_2/Si$ heterostructures with CoO layer thickness of (a) 10nm, (b) 30nm, (c) 60nm and (d) 100nm.

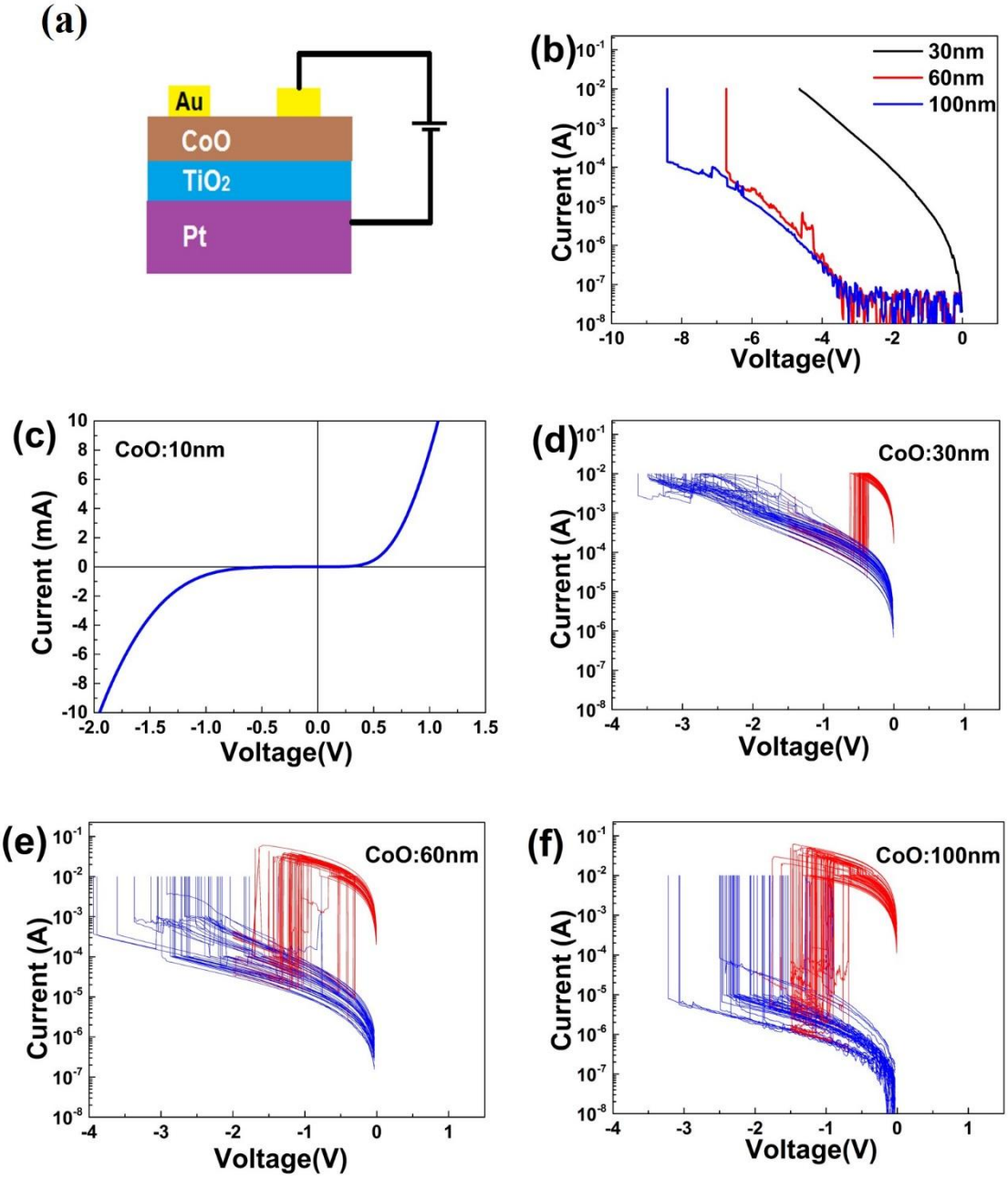


Figure 8-2 (a)schematic stack structure of the Au/CoO/TiO_2/Pt memory device, (b) I-V curves of the electroforming process. I-V curves in 50 consecutive sweeping cycles of the Au/CoO/TiO_2/Pt with CoO thickness of (c) 10nm, (d) 30nm, (e) 60nm and (f) 100nm.

The resistive switching behaviour of the Au/CoO/TiO_2/Pt memory devices with different CoO layer thickness is investigated by measuring the I-V curves in a voltage sweeping mode. Figure 8.2(a) displays the schematic diagram of I-V curve measurement setup. These memory devices need an electroforming process to activate the resistive switching process. Sweeping the applied voltage to a high value can set the device from the pristine high resistive state to a low resistive state. In Figure 8.2(b), the I-V curves of the electroforming process in different Au/CoO/TiO_2/Pt memory cells are presented. It should be pointed out that the Au/CoO(10nm)/TiO_2/Pt sample shows no resistive switching behaviour. During the voltage sweeping process, the current increases fast to the compliance current. Figure 8.2(c) shows the I-V curve of the Au/CoO(10nm)/TiO_2/Pt sample, which presents a rectifying characteristic, showing the p-n junction feature formed in the CoO/TiO_2 interface. From Figure 8.2(b) it can be found that as the thickness of CoO layer increases, the electroforming voltage of the device increases. During the electroforming process, a certain electric field is needed to generate intrinsic defects and form conductive paths that connect the top and bottom electrodes. In the thicker film, a higher voltage is needed to generate the same electric field as compared to thinner film. Therefore, the electroforming voltage increases with increasing film thickness. The Au/CoO/TiO_2/Pt samples with CoO thickness of 30nm, 60nm and 100nm all shows resistive switch behaviour. Figure 8.2(d), (e) and (f) present the I-V curves in 50 consecutive sweeping cycles. As can be found, all samples exhibit reproducible resistive switching performance.

In order to illuminate the effect of the thickness of CoO layer on the resistive switching behaviour of the Au/CoO/TiO_2/Pt heterojunction structure, the resistance at HRS and LRS and reset and set voltage during the 50 sweeping cycles are demonstrated in Figure 8.3 and Figure 8.4, respectively.

Figure 8.3 (a), (b) and (c) shows the resistance of the Au/CoO/TiO_2/Pt memory cells at HRS and LRS during 50 sweeping cycles, with CoO layer thickness of 30nm, 60nm and 100nm, respectively. As can be seen, the resistance at HRS and LRS for all three samples are quite stable in 50 consecutive sweeping cycles. The resistance at HRS increases with the increased thickness of CoO layer, while the resistance at LRS stays as no obvious change for different-thickness samples. The ratio of resistance at HRS to LRS (the memory window) is larger than two orders of magnitude for all three samples and the memory window enlarges with increasing CoO thickness, seen in Figure 8.3(d).

In a comparative view, however, it can be found that the fluctuation of resistance during the sweeping cycles becomes larger in memory cells with thicker CoO layers.

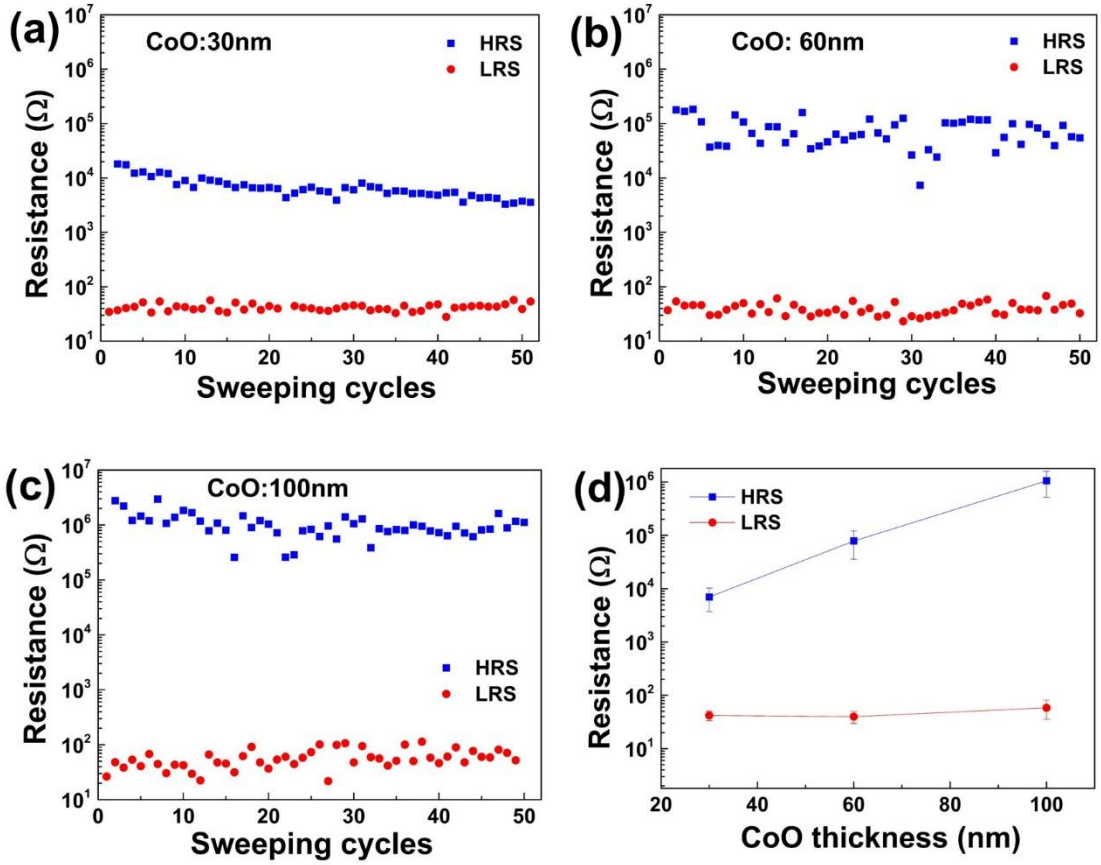


Figure 8-3 The resistance at HRS and LRS during 50 sweeping cycles of the Au/CoO/TiO_2/Pt memory devices with CoO layer thickness of (a) 30nm, (b) 60nm, (c) 100nm; the reading voltage is -0.2V. (d) the average resistance at HRS and LRS during 50 sweeping cycles

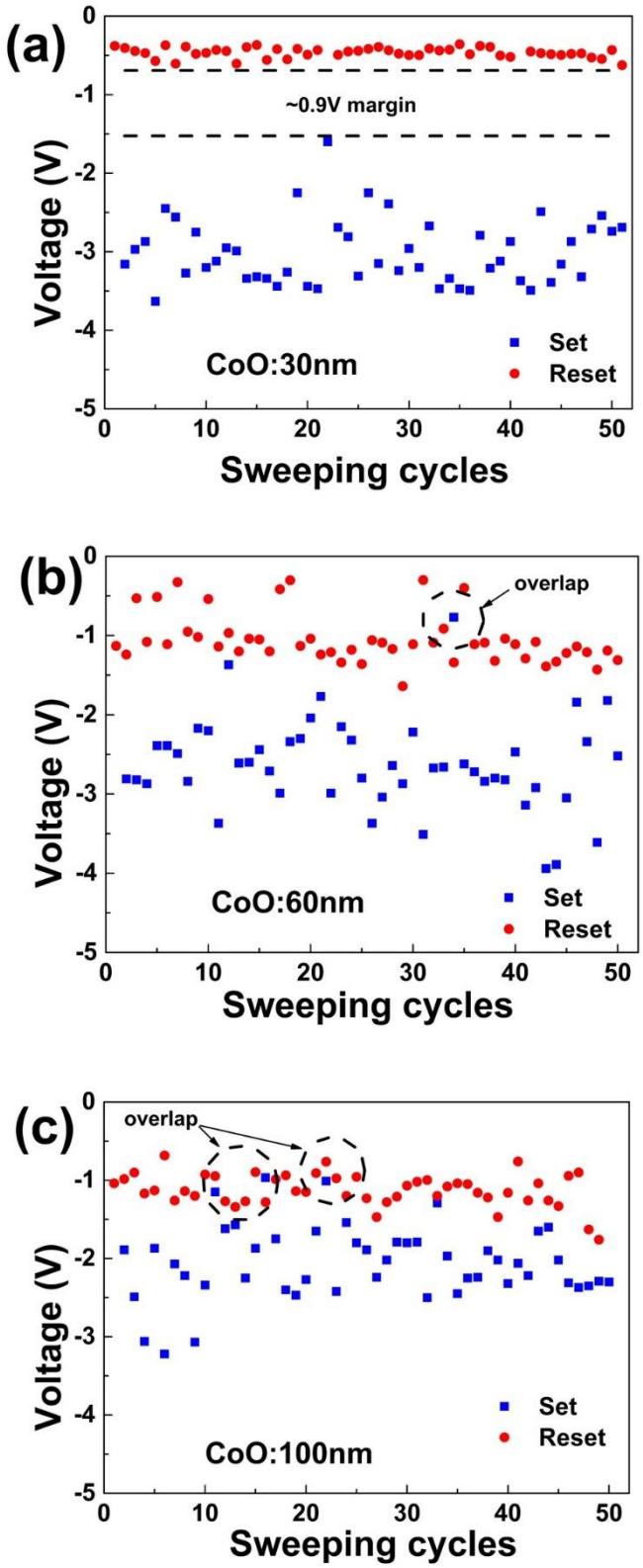


Figure 8-4 The set and reset voltages during 50 sweeping cycles of the Au/CoO/TiO_2/Pt memory devices with CoO layer thickness of (a) 30nm, (b) 60nm, (c) 100nm, respectively

The variation of set and reset voltages as a function of sweeping cycles in the Au/CoO/TiO_2/Pt memory devices is shown in Figure 8.4. There is a large enough margin of ~0.9V between the set and reset voltage in the Au/CoO(30nm)/TiO_2/Pt sample (Figure 8.4(a)). This is important for the correct operation of memory cells during consecutive switch on and off process. In the Au/CoO/TiO_2/Pt samples with thicker CoO layers (Figure 8.4(b) and (c)), however, there are occasional overlaps between the set and reset voltages during the consecutive sweeping cycles. This may increase the possibility of failure during the operation of memory device. Moreover, it can be found that the dispersion of set and reset voltages during the consecutive sweeping cycles becomes larger in the Au/CoO/TiO_2/Pt sample with thicker CoO layers.

From the results discussed above, the ideal thickness for CoO layer is found to be about 30nm. Several reasons have been proposed. Firstly, when the CoO layer is very thin (10nm), the Au/CoO/TiO_2/Pt heterostructure exhibits no resistive switching behaviour. This may be attributed to the low resistance of the structure at this thickness. The current increases very fast to the compliance current. No change in the resistive state of the structure could occur. Secondly, the memory window (ratio of resistance of HRS to LRS) of the Au/CoO/TiO_2/Pt structure increases with increased CoO layer thickness. The increase mainly comes from the increase of resistance at HRS. As discussed in the previous chapter, the conduction mechanism at HRS in the Au/CoO/TiO_2/Pt heterostructure is dominated by the space charge limited conduction (SCLC) model. As the thickness of CoO layer increases, the distance for the charge hopping is increased. The resistance of the structure gets larger for thicker sample. Thirdly, the fluctuation of resistance at HRS and LRS during consecutive sweeping cycles gets worse in the thicker samples than in thinner sample. In the thicker samples, it is expected that the conductive paths or filaments formed in the forming or set process is relatively longer than in thinner samples. During the reset process, there would be more sites for the rupture of the filaments. This may lead to different HRS after the reset process, so the resistance at HRS can be more disperse in thicker samples. It is also possible that more branches of conductive filaments formed during the set process in the thicker samples. Then this may result in more fluctuation in resistance at LRS. Finally, the variation of set and reset voltage during cycling sweeping is larger in the thicker samples. In the thinner sample (CoO=30nm), there is a quite big margin between the set and reset voltage, which is good for the correct and reproducible operation of the memory device.

Whereas in the thicker samples, occasional overlaps between set and reset voltage occur during consecutive sweeping cycles, which may lead to fault in the memory cell operation. It is supposed that in the thicker films, more branches of conductive filaments may form during the electroforming or set process. This may affect the voltage needed to form and rupture the filaments and thus increase the possibility of fluctuation in the set and reset voltages. To conclude, with a relatively thinner CoO layer (30nm), both good stability of the resistive switching parameters and large memory window in Au/CoO/TiO_2/Pt heterostructure can be achieved.

8.4. Summary

The film thickness effect on the RS property of the Au/CoO/TiO_2/Pt heterostructure was investigated. There is no resistance switching behaviour occurring in Au/CoO/TiO_2/Pt heterostructure with too thin CoO layer thickness. The memory window (ratio of resistance of HRS to LRS) of the Au/CoO/TiO_2/Pt structure increases with increased CoO layer thickness. The fluctuation of resistance at HRS and LRS during consecutive sweeping cycles is worse in the thicker samples than in thinner ones. The variation of set and reset voltage during cycling sweeping is larger in the thicker samples. Therefore, with a relatively thinner CoO layer, the stability of the resistive switching performance in Au/CoO/TiO_2/Pt heterostructure can get improved. An ideal thickness of CoO layer (30nm) is found for this Au/CoO/TiO_2/Pt heterostructure.

Chapter 9 Conclusion

Cobalt oxide (CoO), which is a p-type binary transition metal oxide, has shown great potential as switching material for application in RRAMs, which are considered as excellent candidate for next-generation non-volatile memories. This research studies the RS properties of OPA-MBE fabricated cobalt oxide thin films and related p-n heterojunction structures with both conventional cyclic voltammetry measurement and CAFM methods. The RS performance, such as endurance and retention, as well as switching mechanism, is checked. The major findings of this study are as following:

A combination of conventional I-V characterization and CAFM method was used to study the bipolar resistance switching process and mechanism in a CoO/Pt memory device. Good resistive switching properties, such as excellent reproducibility and stability, are demonstrated. The Ohmic conduction at LRS indicates the formation of metallic conductive filaments in the set process, which is well consistent to the results in CAFM experiment, in which formation and rupture of conductive filaments are observed in a writing-erasing process. The results not only demonstrate the good potential of cobalt oxide thin films for non-volatile memory application, but also provides more evidence in understanding the bipolar resistive switching mechanism.

The RS phenomenon in oxides is closely related to the internal defects (e.g. oxygen vacancies in n-type oxide, and metal vacancies in p-type oxide). The oxygen partial pressure during deposition process play a key role in determining the defect concentration in oxide thin films. We used CAFM and KPFM to investigate the resistance switching behaviour of CoO thin films prepared under different oxygen partial pressures. CAFM study shows bipolar resistive switching characteristic in both CoO samples, with CoO sample prepared in higher oxygen partial pressure presenting higher conducting filament density, which is attributed to higher intrinsic defects concentration in this p-type film. KPFM measurement illustrates that the surface potential state of CoO thin film could be switched by charge injections with different electrical bias. The stability of CoO surface potential is related to the internal defects concentration. A charge injection combined with conductive filamentary model is proposed to explain the bipolar resistive switching mechanism in the Pt-tip/CoO/LSMO system.

From the results obtained in Chapter 4 and 5, one can find that different bottom electrodes may play different roles in the resistive switching process. The Pt bottom electrode usually acts as the conduction contact and the resistive switching process occurs in the film bulk. The LSMO bottom electrode, however, may serve as the oxygen reservoir which accepts and donates the oxygen ions from and to the CoO film bulk during the resistive switching process. Therefore, different resistive mechanisms may be proposed for the RS process in memory cells with different bottom electrodes.

RRAM devices, composed of multilayered structures, may exhibit excellent resistive switching properties. We fabricated a CoO/TiO_2 p-n heterojunction structure and studied its RS properties. Different from the previously reported p-n junction RS devices, a unique nonpolar RS behaviour is observed in our Au/p-type CoO/n-type TiO_2/Pt memory cell. The polarity independent RS behaviour can be explained by a filament formation and disruption model. This study demonstrates good RS application potential in CoO-based p-n junction memory cells and provides more insight in understanding the RS mechanism in p-n heterojunction structures.

Thin film deposition parameters, such as growth temperature and oxygen partial pressure, will affect the microstructure as well as defect concentration in the oxide thin films. Adjusting the thin film growth parameters would be an effective approach to tune the defect concentration and microstructural uniformity in the film bulk and thus find the suitable growth conditions that leads to good RS properties in oxide thin film memory devices. In this study, the impact of growth temperature on the RS property of the Au/CoO/TiO_2/Pt p-n heterojunction structure is investigated. An optimized growth temperature range is suggested for fabrication of the CoO/TiO_2/Pt/Ti/SiO_2/Si (001) heterojunction structure to get better RS performance.

The stability of the switching parameters, such as the resistance at HRS and LRS, as well as the set and reset voltages, in RS memory devices is an important issue in the practical applications. Large cycle-to-cycle variation of the switching parameters may bring problems in reproducibility of the memory device, or even failure during the operation. The thickness of oxide thin film may affect the connection and rupture of conductive filaments in the bilayer RS memory structures. In this study, the effect of CoO layer thickness on the resistive switching stability of Au/CoO/TiO_2/Pt heterostructure is investigated. The thickness impact on variation in resistance at HRS

and LRS and set and reset voltages is evaluated. It is found that enhancement of the stability of the RS performance occurs in Au/CoO/TiO_2/Pt heterostructure with a relatively thinner CoO layer.

In this thesis and other previously reported work, cobalt oxide (CoO) thin film has exhibited great potential as candidate for next-generation non-volatile memories. However, there are still some problems remaining to be further investigated.

First, the nature of the conductive filaments in cobalt oxide (CoO) remains to be clarified. Though conductive filamentary RS mechanism has been revealed in our CoO thin films by CAFM current mapping, the composition and microstructure of these conductive filamentary are still unknown. In-situ high-resolution TEM and EELS are powerful techniques for investigating microstructures in nanoscale. They can be used to find out the structure and composition of the conductive filaments in cobalt oxide RRAMs.

Second, testing on operation speed and fabrication of RRAM cross-bar arrays remain to be explored. Our work is mainly focusing on the reliability issue of CoO-based RRAMs. Other issues, such as writ/read speed and memory cell density, remain to be investigated. These works may provide more evidence in its potential for practical applications.

In addition, different CoO-based multilayer structure RRAMs can be made to find better RS uniformity in switching parameters. Our work has demonstrated CoO/TiO_2 bilayer structure showing good RS performance by adjusting the growth parameters as well as film thickness. Some other combinations, such as CoO/WO_x and CoO/FeO_x, etc., is also worth being investigated.

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