The use of silicon diodes in direct current modulators and their application to drift-correcting amplifiers

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THE USE OF SILICON DIODES IN DIRECT CURRENT MODULATORS AND THEIR APPLICATION TO DRIFT-CORRECTING AMPLIFIERS.

by

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THESIS SUBMITTED TO THE NEW SOUTH WALES UNIVERSITY OF TECHNOLOGY AS PARTIAL REQUIREMENT FOR THE DEGREE OF MASTER OF ENGINEERING.

D E C L A R A T I O N

I certify that the work described in this thesis has not been submited to any other University or Institution for Higher Degree.

31st. December 1957.

(T.Glucharoff)

SUMMARY

Electronic analogue computers use voltages to represent the variable to be studied and their basic computing element is the high gain D.C. amplifier. The inherent drift of this amplifier however, may limit the accuracy of certain computations and the reduction of drift is one of the most difficult design problems. Drift-correctors can be used but none of the existing types is completely satisfactory.

The work described in this thesis is mainly concerned with the development and design of a silicon diode modulator for use in drift-correctors for computing amplifiers. After a brief description of the various computing errors and requirements for a drift-corrector the diode modulator is described in detail. Also, a drift-corrector which employs this modulator is described and its performance assessed: the zero-stability obtainable is comparable with that given by the conventional relay modulator, but has the advantages of high frequency response and unlimited life.

FOREWORD

During the development and construction of a D.C. Analogue Computer at the N.S.W. University of Technology it was agreed that unless a better drift-corrector than the existing types could be developed, the D.C. amplifier alone would be used. Although mechanical modulators can be made to give good performance, the relay itself is not completely satisfactory and its working life is limited. It is therefore natural that attempts have been made to replace it by a non-mechanical device. Magnetic modulators, germanium diode modulators and more recently photo-electric choppers have been developed, but their performance if inferior to that of the mechanical modulator.

At the beginning of 1956 silicon diodes become available in Australia and a limited number were obtained. Preliminary tests were conducted with very encouraging results and it was decided to investigate their possible use in low drift D.C. modulators. Delivery of a larger number of diodes was delayed and in the mean time a paper was published by N.F. Moody on the use of silicon diodes in modulators for servo applications. Normally the modulator has been used at 50 c/s but switching frequencies of up to 100 kc/s have been employed with little detoriation in performance. This modulator, however, is quite unsuitable for computer applications mainly because of lack of complete balance; the requirements of a drift-corrector are far more stringent. In view of this and as a result of the preliminary investigations, it was decided to develop a new modulator with a switching frequency of 10 kc/s; this frequency

will permit making full use of the existing frequency response of UTAC (University of Technology Analogue Computer) high gain D.C. amplifier. The first quantity of diodes received, were quite unsuitable for the modulator and a new order was placed for a type which was believed to have the required properties. In the mean time the design and construction of 10 drift-correctors were completed, which were designed to particularly suit the requirements of UTAC. After the arrival of the required type of diode (HD6007) the work was concluded successfully.

This thesis presents the considerations involved in the design of the modulator and the drift-corrector and the investigations carried out during their development. Section 1 serves as an introduction and review of the basic principles of drift-correction. In Section 2 computing errors and the requirements for the drift-corrector are discussed in some detail. In Section 3 main attention is devoted to the conditions for balance and zero-stability of the silicon diode modulator. The complete drift-corrector is described in Section 4, where the emphasis is on the requirement for stability in feedback circuits. In Section 5 the effects upon computation of the particular drift-corrector described in this thesis is examined and the more important results of the work are presented in Section 6. To the author's knowledge the use of silicon diode modulators in drift-correcting amplifiers for computer applications is new.

List of principal symbols.

$K_1G_1(p)$ - transfer function of the D.C. amplifiers.

$K_2G_2(p)$ - transfer function of the Drift-Corrector.

$KG(p)$ - transfer function of the Drift-Corrected Amplifier.

Z_f - the feedback element of the computing components.

Z_i - the input element of the computing components.

Z_o - amplifier or drift-corrector input impedance.

R_o - amplifier or drift-corrector input impedance when purely resistive or modulator input resistance.

e - amplifier input voltage or base of the natural logarithm.

u - amplifier output

v - circuit input voltage or diode voltage.

i_g - grid current

f - drift voltage.

e_i -.modulator input voltage

e_o - modulator output voltage

e_{oc} - modulator output voltage due to unbalance in the conducting direction

e_{on} - modulator output voltage due to unbalance in the nonconducting direction in the absence of capacitive effects.

e_t -modulator output voltage due to unbalance in the nonconducting direction in the presence of balancing capacitors.

m -amplitude of the switching voltage.

i -current

i_s - diode reverse saturation current

i_L - diode leakage current

T - absolute temperature or a time constant

A - a constant

$w, w_m, w_c, w_u, w_v \ldots$ - angular frequencies

$T_u, T_v, T_o, T_i \ldots\ldots$ - time constants

R_1, R_2, R_3, R_4 - modulator bridge resistances

R_p - the parallel combination of the diode back-resistances

R_T - the parallel combination of R_o and R_p.

C_p - the parallel combination of the capacitances across the two diodes

a - resistance ratio of the modulator balancing arm

b - diode branch resistance ratio during conduction

c - diode branch resistance ratio during nonconduction

s - periodic switch representing the action of the diodes.

p - laplacian operator (a capital letter of a variable indicates its Laplace Transform)

C O N T E N T S.

1. INTRODUCTION.

1.1 General.

The use of a drift-corrector is the only effective method to reduce drift in D.C. amplifiers. Broadly speaking drift is a spurious output of low frequency in the absence of an input signal and in computer applications this output may lead to large errors in the computation. D.C. amplifiers alone are unsatisfactory even using well regulated power supplies, carefully selecting electronic tubes and taking other elaborate precautions. The cause of drift has been extensively described in the literature [1] but it is mainly due to change of emission in the electronic tubes, temperature effect on tubes and components, ageing and power supply fluctuations. Most of these factors are not under complete control and can not be eliminated.

The amount of unbalance due to drift is conveniently measured by the value of input D.C. voltage needed to cancel the unbalance and bring the output voltage back to the desired reference level; this input voltage is said to be the drift refered to the input of the amplifier. The short term drift in D.C. amplifiers i.e. the drift which may arise in the course of a computation may be 0.1 mV or more and the long term drift i.e. drift may arise in the period of weeks or months may be anything between 10 mV and 100 mV depending on the amplifier used. Hand balancing is required before commencement of a computation and in large scale computers this maybe a serious problem.

There are several types of drift-correctors: all use a modulator to convert the input signal into an alternating voltage

of higher frequency which, after amplification, is demodulated to obtain an amplified version of the input signal.

Most widely used is the mechanical modulator[1,3] which employs a vibrating relay at some frequency below 400 c/s, It will limit the drift to less than 0.5 mV over long periods of time but has the inherent disadvantage of limited life. In addition the noise level may be up to 5 mV r.m.s. and occasionally peaks of much larger amplitudes have been observed.

Another type of drift-corrector employs a magnetic Modulator[4] utilizing the second harmonic principle in magnetic amplifiers. Long term drift smaller than 1 mV can be obtained but has been found that production models will not remain within the above figure. In addition, after somewhat longer 'off' periods the modulator may settle to a different output value and rebalancing may be required. The noise voltage may be in excess of 1 mV and the drift-corrector is quite difficult to set up in operation.

An experimental photoelectric modulator[5] has been recently developed with a reported long term drift of less than 1 mV. However no detailed information is available and such a modulator requires specially prepared photo-cells and its development is difficult[1].

Diode modulators[3] have not been used in analoque computers. The performance of thermionic diodes is marred by contact and thermal emission potentials, which may introduce changes of tenths of a volt. Germanium diodes will give better performance but due to the low blocking resistance, the input

impedance of such modulators is low; Lange and Lonegan have reported drifts of 10 mV for short periods of time[2].

An important feature of the mechanical, magnetic and photoelectric modulators is the low switching frequency and hence limited band width. The silicon diode modulator described in this thesis however, permits a much higher switching frequency to be used and its zero-stability is comparable with that of the mechanical modulator.

1.2 Basic principle of drift-correction

The basic method of drift-correction is due to Goldberg[6]. Consider a high gain D.C. amplifier and a drift-corrector, with respective transfer functions $K_1G_1(p)$ and $K_2G_2(p)$, connected in a computing circuit as shown in Fig. 1, and assume that the circuit is stable. The D.C. amplifier has two independent inputs one each for the error voltage 'e' and the output of the drift-corrector. Drift which may arise in the D.C. amplifier is represented by an equivalent input voltage 'f' as shown in Fig.1. Since drift contains only low frequency components the gains of the D.C. amplifier and the drift-corrector are K_1 and K_2 and hence for $v = 0$ the output becomes

$$-u = K_1\left[(1+K_2)e + f\right] \qquad \text{but since} \qquad e = \frac{R_i}{R_i+R_f}u$$

$$-u = u\,\frac{R_i}{R_i+R_f}K_1(1+K_2) + fK_1 \qquad \text{or}$$

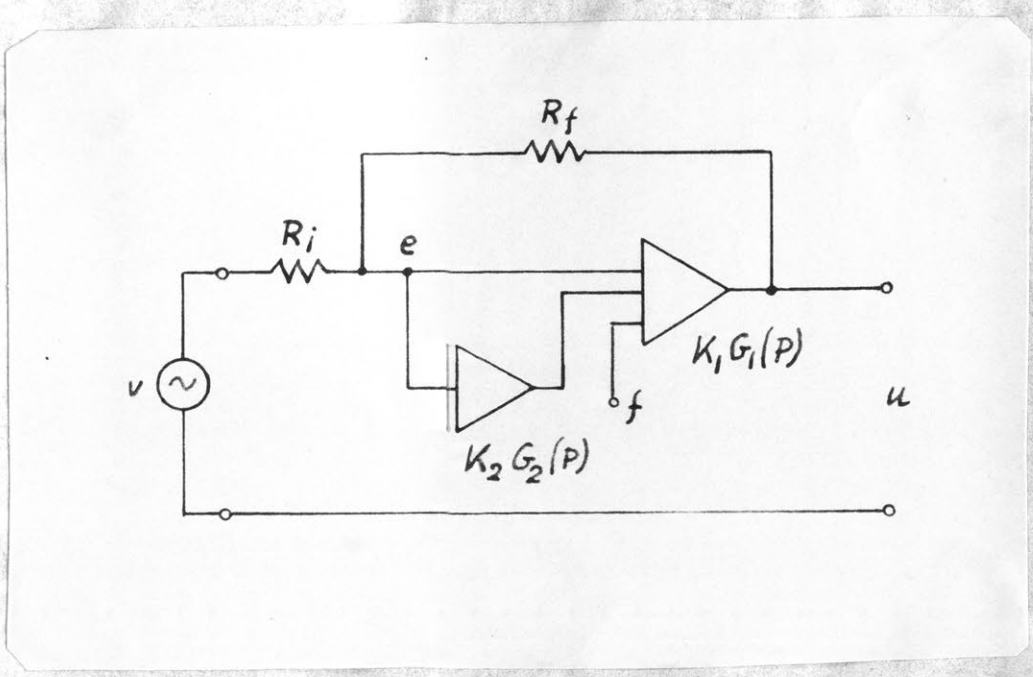


Fig. 1. Basic method of drift-correction

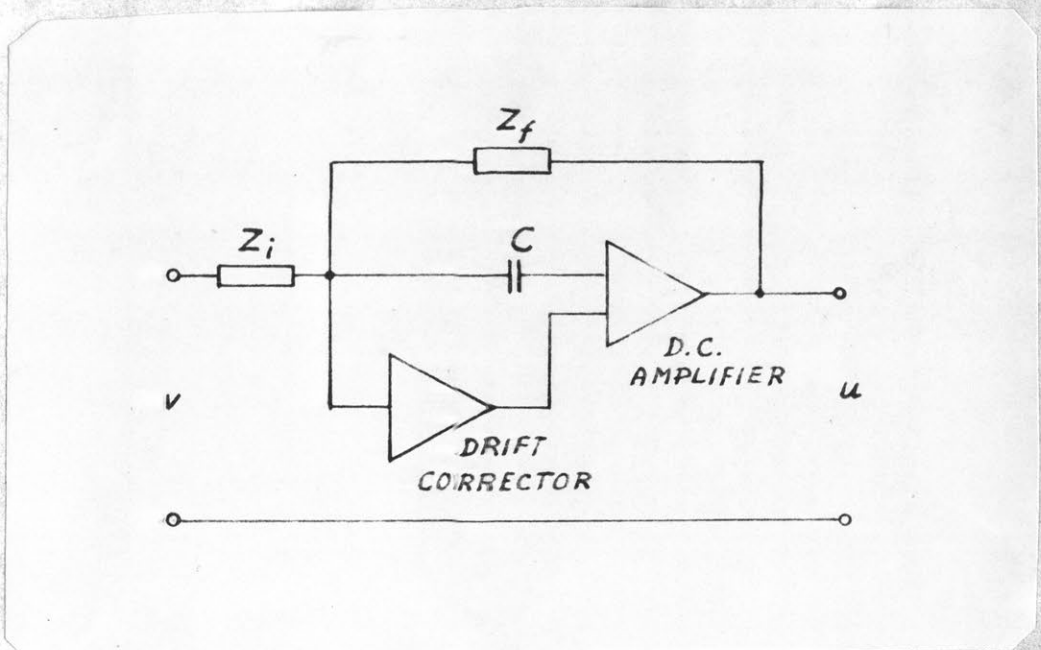


Fig. 2. The use of a series capacitor eliminates the effects of grid current arising in the D.C. amplifier.

$$-u\left[\frac{1}{K_1}+\frac{R_i}{R_i+R_f}(1+K_2)\right]=f \quad \text{and for } K_1 \text{ very large}$$

$$-u=f\frac{1}{1+K_2}\left(1+\frac{R_f}{R_i}\right)$$

It is seen that the output 'u', due to a drift voltage 'f' in the D.C. amplifier, is reduced by the factor $(1+K_2)$. For a sufficiently high gain K_2 the output will be very small and the drift of the drift-corrector alone will be of importance which, of course, is not reduced by this circuit.

The use of a drift-corrector will not only reduce the drift but also increase the total gain of the combined amplifier. From Fig. 1 it follows that the total transfer function is

$$KG(p)=K_1G_1(p)\left[1+K_2G_2(p)\right] \quad \ldots\ldots\ldots\ldots (1)$$

The D.C. gain is $K=K_1(1+K_2)$ i.e. an increase by the factor $(1+K_2)$ and this will result in considerable improvement in the accuracy of certain computations. However the high frequency response is the same as that of the D.C. amplifier since, as will be shown later, the gain of the drift-corrector neccessarily must become less than unity at a comparatively low frequency. Thus, the effect of the drift-corrector is to increase the D.C. gain without affecting the high frequency response i.e. the unity gain frequency is the same as that of the D.C. amplifier (Fig. 3).

Grid current effects can be eliminated by inserting a capacitor in series with the input of the D.C. amplifier as shown in Fig. 2. The total D.C. gain is then $K = K_1 K_2$ and the input time constant is chosen so that all input frequencies above the unity gain frequency of the drift-corrector are not attenuated.

In addition, the use of a drift-corrector will reduce the input impedance of the drift-corrected amplifier and also increase the noise level considerably.

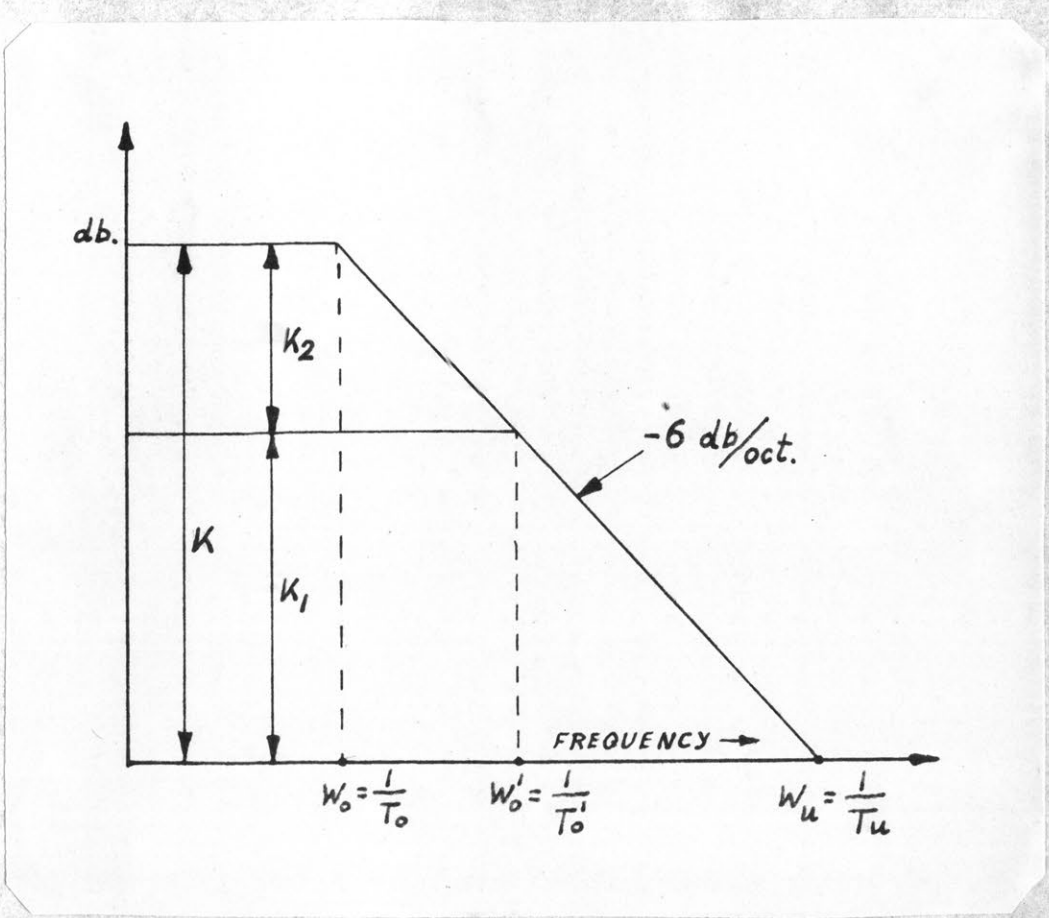


Fig. 3 Attenuation characteristic illustrating how a drift-corrector with a low frequency gain K_2, working with a D.C. amplifier of gain K_1, will increase the total gain to $K = K_1K_2$. However the unity gain frequency w_u is not altered sihce

$$w_u = \frac{w_o}{K} = \frac{w'_o}{K_1}$$

i.e. the unity gain frequency of the drift-corrected amplifier is equal to that of the D.C. amplifier.

2. ERRORS IN COMPUTING AMPLIFIERS.

2.1 General

In this section a description of the various amplifier imperfections is made, and the main effects of the drift-corrector examined. For the purpose of this analysis the frequency response of the computing amplifier is assumed to have a single break of -6 db/oct. Consider such an amplifier as shown in Fig. 4 where Z_i and Z_f are the computing components, Z_o is the input impedance and $KG(p) = K/(pT_o+1)$ is the transfer function of the amplifier. Also i_g is the grid current and f is the drift voltage refered to the input. Then, using Laplace Transform notation, it follows from Fig. 4 that :-

$$\frac{V-U}{Z_i} = \frac{E-U}{Z_f} + \frac{E}{Z_o} \pm i_g \qquad \text{and that} \quad E \pm F = \frac{-U}{KG}$$

$$\frac{V + \frac{U}{KG} \pm F}{Z_i} = \frac{-\frac{U}{KG} - U \pm F}{Z_f} + \frac{-\frac{U}{KG}}{Z_o} \pm \frac{F}{Z_o} \pm I_g$$

$$\frac{V}{Z_i} - \frac{U}{Z_i KG} \pm \frac{F}{Z_i} = -\frac{U}{Z_i KG} - \frac{U}{Z_f} \pm \frac{F}{Z_f} - \frac{U}{Z_o KG} \pm I_g$$

$$V\frac{Z_f}{Z_i} = -U - \frac{U}{KG}\left(1+\frac{Z_f}{Z_i}+\frac{Z_f}{Z_o}\right) \pm F\left(1+\frac{Z_f}{Z_i}+\frac{Z_f}{Z_o}\right) \pm I_g Z_f \quad \ldots\ldots (2)$$

The last equation completely describes the operation of any computing amplifier since no restriction is imposed upon the computing components Z_i and Z_f. All imperfections which are directly concerned with the operation of the drift-corrector are also represented. The first term on the right is the desired output and the other terms are the errors due to finite gain, drift and grid currect respectivelly.

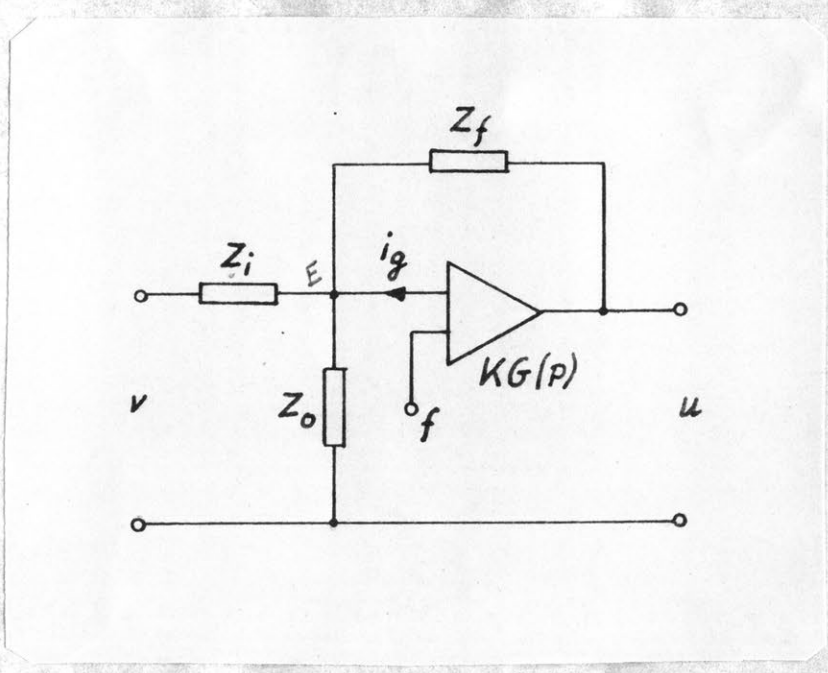
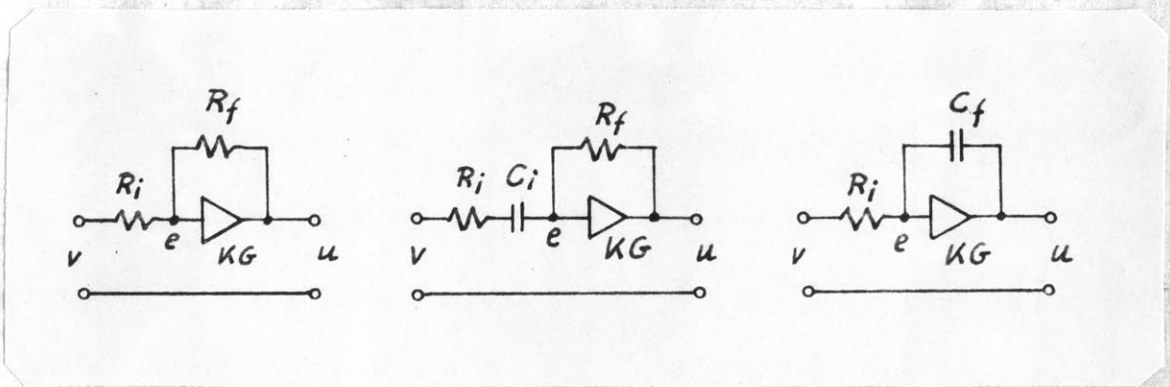


Fig. 4. Circuit to study the imperfections of a computing amplifier.



5a.Adder. 5b. Differentiator 5c. Integrator

Fig. 5. A computing amplifier in various computing circuits.

2.2 Errors due to drift.

The output due to drift is $F(1 + \frac{Z_f}{Z_i} + \frac{Z_f}{Z_o})$ and is independent of the gain K: if f is large a considerable error may result.

In the case of adders and differentiators a constant drift voltage will cause only a fixed output voltage; this error is generally not significant except in cases where R_f/R_i or R_f/R_o are large i.e. a large forward gain is required or the input resistor R_o is too low.

For an integrator with $Z_i = R_i = 1$ MΩ, $Z_o = R_o = 1$ MΩ, and $C_f = 1\ \mu F$, the output due to a constant drift voltage is:-

$$\frac{f}{p}\left(1 + \frac{1}{pC_f}\ \frac{R_i + R_o}{R_i R_o}\right) \quad \text{or}$$

$$f\left(1 + \frac{t}{C_f \frac{R_i R_o}{R_i + R_o}}\right) \quad \text{as a function of time.}$$

For the above values and f= 10 mV this output term will change at a rate of 20 mV per second. If a maximum output of 100 volts and an accuracy of 0.1% is required the integrating time must be limited to only 5 second. This is very serious since considerably larger computing times are normally required. Errors of this type are usually by far the largest, and this is where the main improvement in accuracy can be obtained by the use of drift-correctors.

2.3 Errors due to grid current.

Again, adders and differentiators will have a constant error output, now defined as $i_g R_f$.

The error output of an integrator due a constant grid current i_g, however, is :-

$\frac{i_g}{p}\frac{1}{pC_f}$ or $i_g \frac{t}{C_f}$ as a function of time.

For $i_g = 10^{-9}$ amp. and $C_f = 1\mu F$ a rate of change of output of 1 mV per second is present. This may itself limit the integration time for a given accuracy. Clearly, in order to obtain the full benefit of reduced drift, the grid current must be kept low. Electrometer tubes are normally employed giving grid currents of less than 10^{-10} ampere. A more effective method is to use a capacitive input to the D.C. amplifier to eliminate its effects:- this, however, is possible only if a drift-corrector is employed. A serious objection to this circuit may be the discharge time of the capacitor, which can be kept small only if the unity gain frequency of the drift corrector is high, as will be explained later.

2.4 Effect of amplifier input impedance.

It was already shown that Z_o will increase the error term due to drift and examination of equation (2) shows that the effect of Z_o on the finite GAIN error term is to effectively reduce the gain of the amplifier and thus increase the error.
The input impedance Z_o apears always in paralel with the input impedance Z_i, which seldom exceeds 1 MΩ, and in order that the contribution of Z_o is not excessive, it is desirable that its value should be at least 1 MΩ.

2.5 Effect of noise.

The noise voltage is always increased by the use of drift-correctors and may be as large as 5 mV refered to the

input. In equation (2) it can be considered as part of the drift voltage f and its effect upon the output is readily found for any type of computing circuit. Unless the noise is excessive it has little effect upon adders or integrators, the latter tending to cause a reduction in noise level. In differentiators, however, the reverse is true, and a very large noise output may result. For this reason it is desirable to keep the combined amplifier noise level to a minimum.

2.6 Errors due to finite gain.

In the following assume that f=0, $i_g = 0$ and $Z_o = \infty$. Under these conditions equation (2) becomes :-

$$V \frac{Z_f}{Z_i} = -U - \frac{U}{KG(p)} \left(1 + \frac{Z_f}{Z_i}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

It is immediately apparent that the error due to finite gain can be made as small as desired by making K sufficiently large. It may be noted that K is the low frequency gain only, and that at some higher frequency the gain of the amplifier will begin to fall, causing the error to increase. Clearly in order to keep the error small, a good high frequency response is required. The transient response of a computing circuit, however, can not be deduced from the above equation and a complete solution in the time domain is required.

There is an extensive literature covering this field, but the frequency response of the computing amplifier is assumed as being perfect. i.e. the gain is constant for all frequencies. In actual practice this is not the case: all amplifiers contain resistive as well as capacitive components and the gain will begin to fall at some higher frequency. Usually a single break is present,

the gain falling off at a rate of less than 9 db/ oct. This is required in order that the amplifier is stable for all types of feedback. The use of drift-correctors may introduce additional break frequencies, but the silicon diode modulator permits the frequency response of the drift-corrected amplifier to have a single break: thus, the frequency and the transient analysis of a drift-corrected amplifier is the same as that of a conventional D. C. amplifier.

In the course of studying the effect of gain and frequency response of the drift-corrector, the steady state and the transient solutions for various computing circuits were obtained.

2.7 Transient response of an adder.

The transfer function of the amplifier is assumed to be $KG(p) = K/(pT_o + 1)$ and its attenuation chracteristic is shown in Fig. 3 where.

$w_o = \frac{1}{T_o}$ is the angular frequency at which the gain is reduced by 3 db.

$w_u = \frac{1}{T_u}$ is the unity gain frequency i.e. the frequency for which the amplifier gain is one.

For an adder $Z_i = R_i$ and $Z_f = R_f$ (Fig.5a) and so from equation (3)

$$V\frac{R_f}{R_i} = -U - \frac{U}{K/(pT_o+1)}\left(1+\frac{R_f}{R_i}\right) = -U\left[1+\frac{pT_o+1}{K}\left(1+\frac{R_f}{R_i}\right)\right]$$

$$-\frac{U}{V} = \frac{R_f}{R_i}\frac{K}{\left[K+1+pT_o+p\frac{R_f}{R_i}T_o+\frac{R_f}{R_i}\right]} = \frac{R_f}{R_i}\frac{K}{\left[K+1+\frac{R_f}{R_i}\right]}\frac{1}{\left[1+pT_o\left(1+\frac{R_f}{R_i}\right)/\left(K+1+\frac{R_f}{R_i}\right)\right]}$$

Put $T_u \cong \frac{T_o}{K+1}$ and for $K+1 \gg \frac{R_f}{R_i}$, which is normally the case, the transfer function of the adder becomes :-

$$-\frac{U}{V} = \frac{R_f}{R_i} \frac{K}{(K+1)\left[1+ pT_u(1+ \frac{R_f}{R_i})\right]} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

For a step input $V = \frac{v}{p}$ and the output is

$$-u = v \frac{R_f}{R_i} \frac{K}{K+1} \left[1 - e^{-\frac{t}{T_u(1+R_f/R_i)}}\right] \ldots\ldots\ldots\ldots (5)$$

From equations (4) and (5) it is apparent that increased gain will improve the accuracy by making $K/(K+1)$ much closer to unity. The transient response however is not affected since it is only a function of the unity gain frequency, which is not altered by the use of a drift-corrector.

2.8 Transient response of a differentiator

For a differentiator $Z_i = R_i + \frac{1}{pC_i}$ and $Z_f = R_f$ (Fig. 5b), and substitution in equation (3) yields

$$V \frac{R_f pC_i}{pC_i R_i + 1} = -U\left[1 + \frac{pT_o + 1}{K}\left(1 + \frac{R_f pC_i}{pC_i R_i + 1}\right)\right]$$

put $T_d = R_f C_i$ and $T_b = R_i C_i$ and so

$$-\frac{U}{V} = \frac{K}{K+1} \frac{pT_d}{T_u(T_d+T_b)\left[p^2 + \frac{p(T_o+T_d+T_b+KT_b)}{T_u(T_d+T_b)(1+K)} + \frac{1}{T_u(T_d+T_b)}\right]}$$

For critical damping normally used in differentiators

$$-\frac{U}{V} = \frac{K}{K+1}\,\frac{pT_d}{T_u(T_d+T_b)\,(p+w_r)^2} \qquad \text{.....(6)}$$

$$w_r^2 = 1/(T_d+T_b)T_u$$

and the solution for a step input is immediately apparent as:-

$$-u = v\,\frac{K}{K+1}\,\frac{R_f}{T_u(R_f+R_i)}\,t\,e^{-w_r t} \qquad \text{.....(7)}$$

It may be seen from equations (6) and (7) that improved differentiation in the steady state is obtained if K is large i.e. the ratio K/(K+1) close to unity. The transient response is again not affected, since the time constant involved is $w_r^2 = 1/\,T_u C_i(R_f+R_i)$ i.e. a function of the unity gain frequency only.

2.9 Transient response of an integrator

For a integrator $Z_i = R_i$ and $Z_f = \frac{1}{pC_f}$ (Fig.5c) and so

$$\frac{V}{pC_fR_i} = -U\left[1 + \frac{T_o p + 1}{K}\left(1 + \frac{1}{pC_fR_i}\right)\right] \quad \text{put} \quad T_i = R_iC_f$$

$$-\frac{U}{V} = \frac{1}{pT_i\left[1 + \frac{pT_o+1}{K}\left(1+\frac{1}{pT_i}\right)\right.} = \frac{K}{T_iT_o}\,\frac{1}{\left[p^2+p\,\frac{T_i(K+1)+T_o}{T_iT_o} + \frac{1}{T_iT_o}\right.}$$

$$-\frac{U}{V} = \frac{K}{T_iT_o}\,\frac{1}{(p-p_1)(p-p_2)}$$

$$p_{1,2} = \frac{1 \pm \sqrt{1-\frac{4T_o}{(1+K)^2\,T_i}}}{\frac{2T_o}{K+1}}$$

provided that $T_o \ll T_i(K+1)$ which is normally the case.

$$p_1 = \frac{-1 + \sqrt{1-4T_o/(1+K)^2T_i}}{2T_o/(1+K)} = \frac{-1}{(1+K)T_i} \quad \text{since} \quad \frac{T_o}{K+1} \text{ very small}$$

$$p_2 = \frac{-1 - \sqrt{1-4T_o/(1+K)^2T_i}}{2T_o/(1+K)} = -\frac{1+K}{T_o} \quad \text{and hence}$$

$$-\frac{U}{V} = \frac{K}{T_iT_o} \frac{1}{\left[p+\frac{1}{(1+K)T_i}\right]\left(p+\frac{1+K}{T_o}\right)} \qquad \text{put} \quad T_u = T_o/(K+1)$$

$$T_v = (K+1)T_i = (K+1)C_fR_i$$

$$-\frac{U}{V} = \frac{K}{(pT_v+1)(pT_u+1)} \quad \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

For an input $v = h \cos wt$

$$-U = \frac{Kh}{T_uT_v} \frac{p}{(p^2+w^2)(p+\frac{1}{T_v})(1+\frac{1}{T_u})} = \frac{hK}{T_uT_v}\left[\frac{A}{p+jw} + \frac{B}{p-jw} + \frac{C}{p+w_v} + \frac{D}{p+w_u}\right]$$

where $w_v = 1/T_v$ and $w_u = 1/T_u$

$$A = \frac{K\,h}{T_uT_v}\left[\frac{p}{(p-jw)(p+w_v)(p+w_u)}\right]_{p=-jw} = \frac{-hK\,e^{-j\alpha}}{2j\sqrt{(1+\frac{w^2}{w_v^2})(1+\frac{w^2}{w_u^2})}}$$

$$B = \frac{hK\,e^{+j\alpha}}{2j\sqrt{(1+\frac{w^2}{w_v^2})(1+\frac{w^2}{w_u^2})}} \qquad tg\,\alpha = (w_vw_u - w^2)/w(w_v+w_u)$$

$$C = \frac{hK}{T_uT_v}\left[\frac{p}{(p^2+w^2)(p+w_u)}\right]_{p=-w_v} = \frac{-hK}{(1+w^2/w_v^2)(1-w_v/w_u)}$$

$$C = \frac{-hK}{1+w^2/w_v^2} \quad \text{since} \quad \frac{w_v}{w_u} = \frac{T_o}{(K+1)^2\,T_i} \text{ is very small}$$

$$D = \frac{hK}{T_uT_v}\left[\frac{p}{(p^2+w^2)(p+w_v)}\right]_{p=-w_u} = \frac{-hK}{(1+w^2/w_u^2)(1-w_u/w_v)} \quad \text{or}$$

$D = 0$ or very small since $\frac{w_u}{w_v} = \frac{(K+1)^2\;T_i}{T_o}$ is very large

Thus the output as a function of time becomes:-

$$u = -hK\left[\frac{\sin(wt+\alpha)}{\sqrt{(1+\frac{w^2}{w_v^2})(1+\frac{w^2}{w_u^2})}} - \frac{e^{-w_v t}}{(1+\frac{w^2}{w_v^2})}\right] \quad \ldots\ldots\ldots (9)$$

The output for a step input is obtained by letting $w \to 0$:-

$$u = -hK\,(1 - e^{-w_v t}) = -hK\left[1 - e^{-\frac{t}{C_f R_i (K+1)}}\right] \quad \ldots\ldots (10)$$

Examination of the transfer function of an integrator, equation (8), reveals that accurate integration in the steady state is only possible in the frequency range well below $w_u = 1/T_u$ and well above $w_v = 1/T_v$. However, examination of equation (9), which contains the steady state and the transient solution for a simusoidal input in the time domain, indicates that due to the large time constant T_v integration is possible well below the angular frequency w_v, if the time of computation is limited. The limiting case is when a D.C. input is applied and the solution is given by equation (10). The time constant involved is $T_v = (K+1)C_f R_i$ i.e. directly proportional to the gain K of the computing amplifier.

As an indication of the size of errors involved consider an amplifier with $K = 10^5$ and $R_i C_f = 1$ second; then for a step input and an accuracy of 0.1% the computing time must be limited to only 200 sec. A higher gain will reduce the error for a given computing time or extend the time for a given error.

An effective low frequency gain much in excess of 2×10^6 is difficult to obtain mainly due to leakage in the feedback capacitor. Also, for this size of gain, the errors due to other imperfections may be much larger.

2.10 Drift-corrector requirements.

The above discussion indicates that the desirable features of a drift-corrector are:-

(1) Low drift

(2) High input impedance

(3) Low noise

(4) D.C. gain large enough to bring the total gain to at least 2×10^6 and also large enough to reduce the drift due to the D.C. amplifier to less than the inherent drift of the modulator.

(5) High frequency response. The advantages of a high frequency response are :-

(i) The drift-corrector will increase the accuracy of all computing operations over the useful frequency range.

(ii) The size of the series capacitor used to remove grid current effects (Fig.2) can be reduced to reasonable proportions; the amplifier input time constant can now be kept small, thus removing the main objection to this type of circuit.

(iii) In general a higher carrier frequency will permit considerable reduction in the physical size of some of the components used.

3. THE SILICON DIODE MODULATOR.

3.1 Preliminary investigations.

If two diodes are connected as shown in Fig. 6 and an alternating voltage is applied, the diodes will alternately conduct or block during each half cycle. The switching voltage is balanced to ground by two low resistances R_1 and R_2 so that if the characteristics of the diodes are identical over the whole operating region, their junction point will remain at zero potential at every instant. If now a direct voltage e_i is applied to the diode junction via a resistor R_o, then, provided that R_o is much larger than the forward resistance and much smaller than the backward resistance of the diodes, the voltage e_o at the junction point will be a square wave alternating between zero and e_i. Thus a direct voltage is converted into a pulsating voltage which can now be amplified by a conventional A.C. amplifier.

This is the basic principle of operation and requires only two silicon diodes. Tests were conducted to determine the performance of such a modulator for various switching frequencies and in the course of development a number of additional components and controls had to be added to the basic circuit of Fig. 6. Initially only two silicon diodes type ZS 10 were available and at a later stage a second pair, type HD6007, was obtained.

Operation at a switching frequency of 50 c/s was very satisfactory and it became immediately apparent that drift will remain within 1 millivolt over long periods of time. However a minimum of two controls was required to obtain satisfactory

balance but, even so, the residual voltage was about two millivolts equivalent input. During the transit period. i.e. the intermediate period between full conduction and nonconduction, a pulse in the form of a transient appears with a magnitude of several millivolts as shown in Fig. 7. It was found that in order to keep the residual voltage and the transit pulse to a minimum the switching voltage should be as small as possible and also, that drift will increase with increased input resistor R_o. The type of output obtained from the modulator for a D.C. input voltage is shown in Fig. 8.

At switching frequencies of 1 kc/s some difficulties were encountered. Balance was difficult and a third control (capacitive) had to be introduced but the residual voltage was still several millivolts and the transit pulses in the order of tens of millivolts. Drift could be 2 or 3 mV over a period of a few days but sometimes much less than that figure: in general the drift was quite unpredictable particularly of the pair of diodes ZS 10. This led to the use of a tuned circuit in the following A.C. amplifier, which considerably reduced the residual voltage (refered to the input) and almost removed all transit pulses. The result was a reduction of drift to less than 1 mV but the diodes HD6007 were easier to balance and the drift smaller than that of ZS 10. In fact the performance of the diodes HD6007 under these conditions was comparable with the performance at 50 c/s and thus the switching frequency was increased to 10 Kc/s.

Again, at a switching frequency of 10 kc/s, the diodes HD6007 gave a performance similar to that at low frequencies but ZS 10 performed very badly. At this stage it was clear that drift

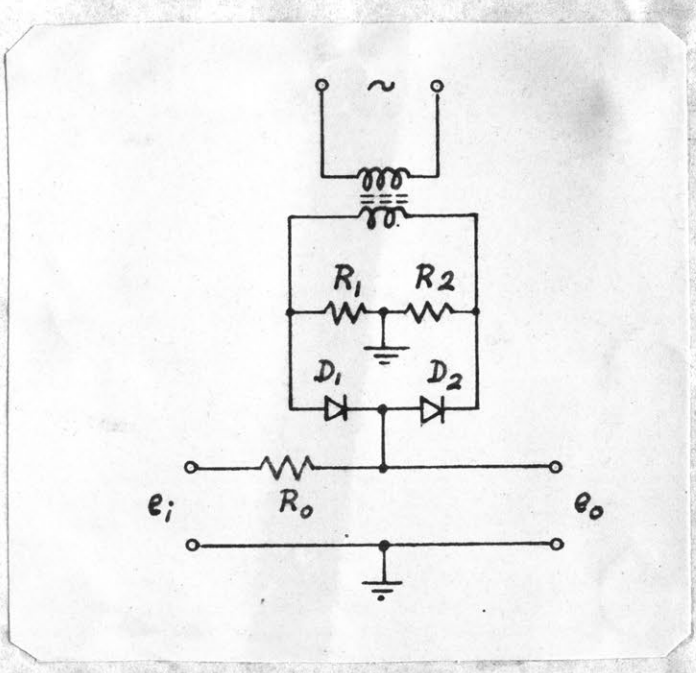


Fig. 6 Basic modulator circuit.

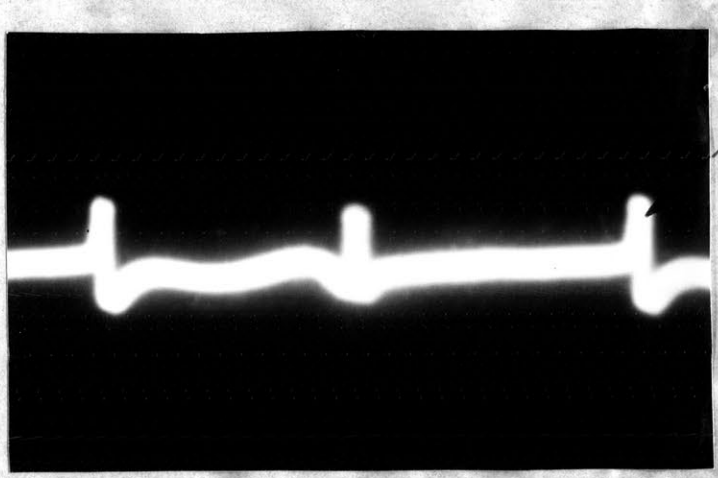


Fig. 7 Residual voltage at a switching frequency of 50 c/s

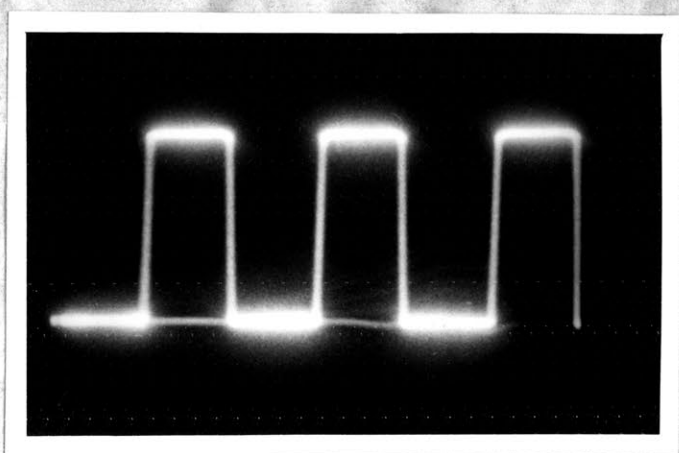


Fig. 8 Modulator output for a D.C. input and a switching frequency of 50c/s.

is mainly due to some type of unbalance during the transit period and a detailed investigation of the diode properties was conducted. As a result it was found that the diodes D.C. forward characteristics must follow a logarithmic law for satisfactory operation.

Finally it was decided to build drift-correctors operating at 10 Kc/s and to obtain diodes which would fulfil our requirements. No attempt was made to increase the switching frequency above 10 kc/s for reasons given in the following sections. Thus all investigations and design criteria relate directly to the application of a 10 kc/s modulator in a drift-corrector which has been built to suit the ITAC high gain D.C. amplifier.

As a first step it was required to obtain a clear understanding of the operation of the modulator and in the following Section the output of a diode modulator is derived for a sinusoidal input voltage.

3.2 Modulator with capacitive load.

The diode modulator may be represented as a periodic switch 's' with zero resistance during the conducting period and a very large resistance R_p during the nonconducting period (Fig. 9). The equivalent diagram is then as shown in Fig. 10.

where e_i is the input voltage

e_o - the output voltage.

s - the periodic switch.

C - the total capacitance across the output including the input capacitance of the following valve amplifier, stray capacitance and capacitance required for balancing

and it follows that

$$\frac{e_i - e_o}{R_o} = \frac{e_o}{s} + C\frac{de_o}{dt} \quad \text{or} \quad e_o + \frac{e_o}{R_o}s + sC\frac{de_o}{dt} = \frac{e_i}{R_o}s\,dt$$

Multiply by e^{-pt} and integrate to obtain the Laplace Transform

$$\int_o^\infty e^{-pt}e_o dt + \int_o^\infty e^{-pt}\frac{e_o}{R_o}s\,dt + \int_o^\infty e^{-pt}sC\frac{de_o}{dt} = \int_o^\infty e^{-pt}\frac{e_i}{R_o}s\,dt$$

$$\int_o^\infty e^{-pt}e_o dt = E_o$$

$$\int_o^\infty e^{-pt}\frac{e_o}{R_o}s\,dt = \frac{R_p}{R_o}\left[\int_o^{\pi/w_c} e^{-pt}e_o dt + \int_{2\pi/w_c}^{3\pi/w_c} e^{-pt}e_o dt + \ldots.\right] = \frac{R_p}{R_o}E_o$$

since for $s = 0$ also $e_o = 0$

$$\int_o^\infty e^{-pt}sC\frac{de_o}{dt}\,dt = pCR_pE_o$$ obtained in a similar manner as above

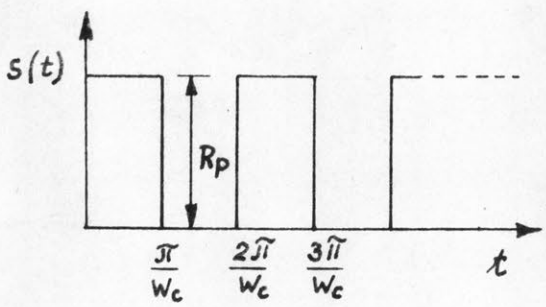


Fig. 9. The modulator switch as a function of time: w_c is the angular frequency of the switching voltage.

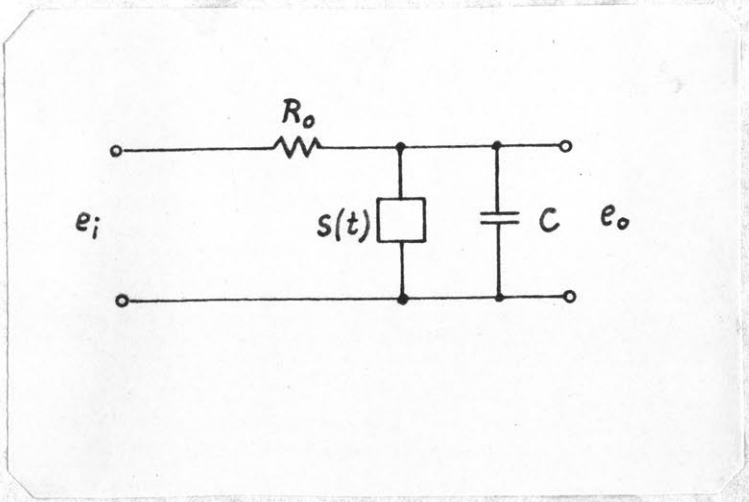


Fig. 10. Equivalent diagram of the diode modulator with capacitive load.

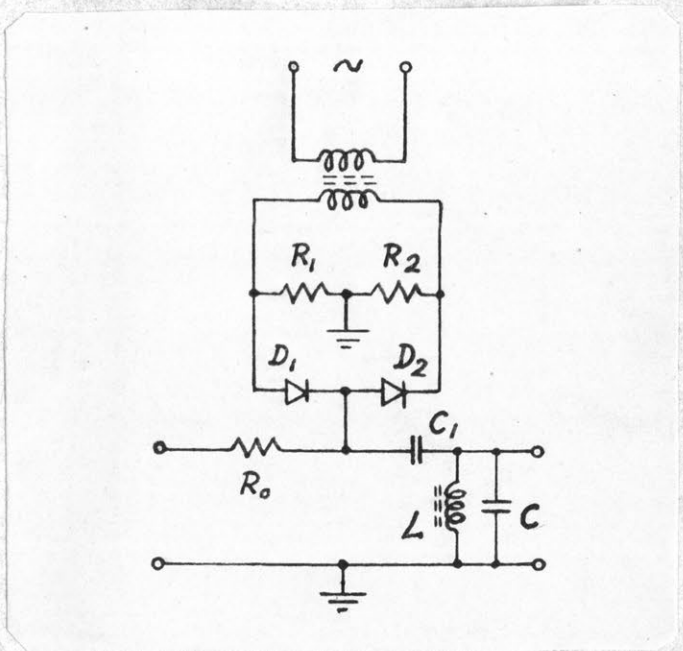


Fig. 11. The modulator working into a tuned circuit.

For a complex input $e_i = e^{-jw_m t}$

$$\int_0^\infty e^{-pt}\frac{e_i}{R_o}\,sdt = \frac{R_p}{R_o}\left[\int_0^{\pi/w_c} e^{-(p+jw_m)t}dt + \int_{2\pi/w_c}^{3\pi/w_c} e^{-(p+jw_m)t}dt \ldots\ldots\right] =$$

$$= \frac{R_p}{R_o}\left[\frac{1}{p+jw_m} - \frac{e^{-(p+jw_m)\pi/w_c}}{p+jw_m} + \frac{e^{-(p+jw_m)2\pi/w_c}}{p+jw_c} - \ldots.\right] =$$

$$= \frac{R_p}{R_o}\,\frac{1}{(p+jw_m)(1 - e^{-(p+jw_m)\pi/w_c})}$$

Substitution yield

$$E_o + \frac{R_p}{R_o}E_o + pCR_pE_o = \frac{R_p}{R_o}\,\frac{1}{(p+jw_m)(1+ e^{-(p+jw_m)\pi/w_c})} \quad \text{or}$$

$$E_o = \frac{R_p}{R_o+R_p}\,\frac{1}{(1+pCR_T)(p+jw_m)(1+e^{-(p+jw_m)\pi/w_c})} \quad \text{where } R_T = \frac{R_oR_p}{R_o+R_p}$$

To obtain e_o as a function of time the inverse laplace Transform is used. There are poles at:-

$$p = -\frac{1}{CR_T}, \quad p = -jw_m \quad \text{and} \quad p = -j\left[(2n-1)w_c + w_m\right]$$

$$n = 0, \pm 1, \pm 2, \ldots\ldots$$

Residue at $p = \frac{-1}{CR_T}$

$$\frac{R_p}{R_o+R_T}\left[\frac{1}{CR_T(p+jw_m)(1+e^{-(p+jw_m)\pi/w_c})}\right]_{p=\frac{-1}{CR_T}} =$$

$$= \frac{R_p}{R_o+R_p}\,\frac{-1}{(1-jw_mCR_T)\left[1-e^{-(jw_m-1/CR_T)\pi/w_c}\right]}$$

Residue at $p = -jw_m$

$$\frac{R_p}{R_o+R_p}\left\{\frac{1}{(1+pCR_T)\quad 1+e^{-(p+jw_m)\pi/w_c}}\right\}_{p=-jw_m} = \frac{R_p}{(R_o+R_p)}\,\frac{1}{2(1-jw_mCR_T)}$$

Residue at $p = -j\left[(2n-1)w_c + w_m\right]$

$$\frac{R_p}{R_o+R_p}\left\{\frac{1}{(p+pCR_T)(p+jw_m)\left[-\frac{\pi}{w_c}e^{-(p+jw_m)\pi/w_c}\right]}\right\}_{p=-j\left[(2n-1)w_c+w_m\right]}$$

$$= \frac{j}{\pi(2n-1)\left[1-j\left\{(2n-1)w_c+w_m\right\}CR_T\right]} \quad \text{and hence}$$

$$e_o = \frac{R_p}{R_o+R_p}\left\{\frac{e^{-jw_m t}}{2(1-jw_m CR_T)} - \frac{e^{-t/CR_T}}{(1-jw_m CR_T)\left[1+e^{-(jw_m - 1/CR_T)\pi/w_c}\right]} + \right.$$

$$\left. + \sum_{n=-\infty}^{+\infty} \frac{j\, e^{-j\left[(2n-1)w_c+w_m\right]t}}{\pi(2n-1)\left[1-j\left\{(2n-1)w_c+w_m\right\}CR_T\right]}\right\}$$

For $R_T = 1\ M\Omega$ and $C = 50\times10^{-12}$ Farad, $CR_T = \frac{1}{2}\,10^{-4}$ sec. and for all input frequencies well below 1 kc/s the transient (second) term can be neglected.

The steady state response for $w_m \ll w_c$ is:-

$$e_o = \frac{R_p}{R_o+R_p}\, e^{-jw_m t}\left[\frac{1}{2(1+jw_m CR_T)} + \frac{j\, e^{-jw_c t}}{\pi(1-jw_c CR_T)} - \frac{j\, e^{+jw_c t}}{\pi(1+jw_c CR_T)} + \ldots\ldots\right]$$

$$e_o = \frac{R_p}{R_o+R_p}\, e^{-jw_m t}\left[\frac{1}{2(1-jw_m CR_T)} + \frac{2}{\pi}\sum_{n=1}^{\infty} \frac{\mathrm{Sin}\left[(2n-1)w_c t - \beta\right]}{(2n-1)\sqrt{1+\left[(2n-1)w_c CR_T\right]^2}}\right]$$

where $\quad tg\,\beta = (2n-1)w_c CR_T$

For w_m at least 10 times smaller than w_c the first term in the brackets can be neglected since it is normally filtered out in the following A.C. amplifier. The output for a sinusoidal input can be obtained by taking the real or the imaginary part of the complex output since $e_i = e^{-jw_c t} = \mathrm{Cos}\, w_c t - j\mathrm{Sin}\, w_c t$. Then, by considering the fundamental term only the output for an input $e_i = \mathrm{Cos}\, w_c t$ becomes :-

$$e_o = \frac{2}{\pi}\frac{R_p}{(R_o+R_p)} \cos w_m t \; \frac{\sin (w_c t - \beta)}{\sqrt{1 + (w_c C R_T)^2}} \qquad \text{.....(11)}$$

$$tg\,\beta = w_c C R_T$$

which is the equation of a suppressed carrier amplitude modulated wave.

The above equation shows that the capacitor C will not affect the input signal but it will alter the phase of the carrier frequency only. In this case a time constant is defined by the input resistor $R_T = R_o$ (R_p very large) and the total capacitance C. Assuming $R_o = 1\ M\Omega$ and $C = 50\ \mu\mu F$ a break-frequency of 3.1 kc/s is obtained, which implies that for a switching frequency of 3.1 kc/s the carrier will suffer a phase shift of 45^o and a attenuation of 3 db.

Phase shift of this size is very undesirable since the output of the demodulator following the A.C. amplifier is proportional to the Cosine of this phase angle. Also, the attenuation will reduce the efficiency of the modulator.

3.3 Modulator working into a tuned circuit.

To eliminate the effect of the capacitance an inductance L is used to tune the circuit as shown in Fig. 11 , in which C_1 is only a sufficiently large capacitor to pass the carrier frequency. Obviously for satisfactory operation the impedance of the tuned circuit at resonance should be several times larger than the input resistor R_o. In this case a suppressed carrier amplitude modulated wave is applied to a resonant circuit tuned to the carrier frequency, and a well known network theorem[7,8] states that the effect of such a circuit upon the signal frequency w_m is the same as that of a single R.C. lag network

whose break frequency is $1/2\pi R_2C$; above this frequency the signal voltage will be attenuated at 6 db/oct. However, this theorem would apply only if the modulator and the tuned circuit do not interact. If the coupling capacitor C_1 is made too small phase shift and attenuation of the carrier frequency may occur when the impedance of the tuned circuit at resonance and the reactance of the capacitor become comparable. If the coupling capacitor is large it was found experimentally that phase shift of the input signal may take place. The mathematical analysis of such circuit becomes very difficult, but for suitable values of C_1 the above network theorem is applicable as will be shown when the actual modulator is described.

For the modulator, R may be assumed to be equal to the input resistor R_o, provided that the losses in the resonant circuit are small. The minimum value of the load capacitance is about 50$\mu\mu$F, and so for R_o = 1 MΩ, the break frequency is 1600 c/s. Signal inputs of higher frequencies will be subject to a phase shift greater than 45^0 and this may be unacceptable from the overall stability point of view. This shows that the requirement for high input resistance limits the frequency response to little over 1000 c/s., Additional damping may be used but this will reduce the gain of the modulator. Since a carrier wave may be modulated with signals having frequency components of up to 1/10 of the carrier frequency, there is little to be gained, in this type of application , by increasing the switching frequency above 10 kc/s.

The tuned circuit also acts as band pass filter : it tends to reduce:-

(i) Any components of the input signal which are not superimposed on the carrier; if present they may appear at the output of the drift-corrector and cause unstability.

(ii) Transit pulses and switching transients and thus reduce drift in the modulator.

(iii) Power frequency pick-up which will result in reduced noise level.

3.4 The silicon diode

In the previous sections it was assumed that two identical diodes were used allowing perfect balance to be obtained at the diode junction point (Fig.6). In practice the characteristics of the diodes will vary widely and several adjustments may be required to obtain a satisfactory balance and also, drift is largely dependent upon the diodes used. Thus,a study of the diodes properties become necessary.

3.4.1 D.C. properties. The D.C. characteristic of a silicon diode for a few tenth of a volt in the forward and in the backward direction is well defined by the relation[9,10]

$$i = i_s \left(e^{\frac{v}{AT}} - 1\right) + i_L\left(e^{\frac{v}{AT}} - \frac{v}{AT} - 1\right)^{\frac{1}{2}} \quad \ldots\ldots\ldots\ldots (12)$$

where i is the voltage across the diode

i_s - reverse saturation current

i_L - leakage current

T - absolute temperature

A - a constant

To determine the D.C. characteristic of a diode the circuit shown in Fig. 12 can be used, which can measure currents down to 10^{-10} ampere. The operational amplifier X which has as input computing element the diode to be investigated, must have a low grid current valve and the amplifier Y should have low short time drift or be drift corrected. Then the current is given in terms of the output voltage v_2 and the gain K_Y of amplifier Y by

$$i = v_2 / K_Y \, 10^{-7} \text{ ampere.}$$

and the diode voltage is $v = v_1$.

A typical semilogarithmic plot in the forward direction is shown in Fig. 15. The plot consists of two straight lines each corresponding to i_s and i_L, and their actual values can be found by extending the lines down to $v = 0$.

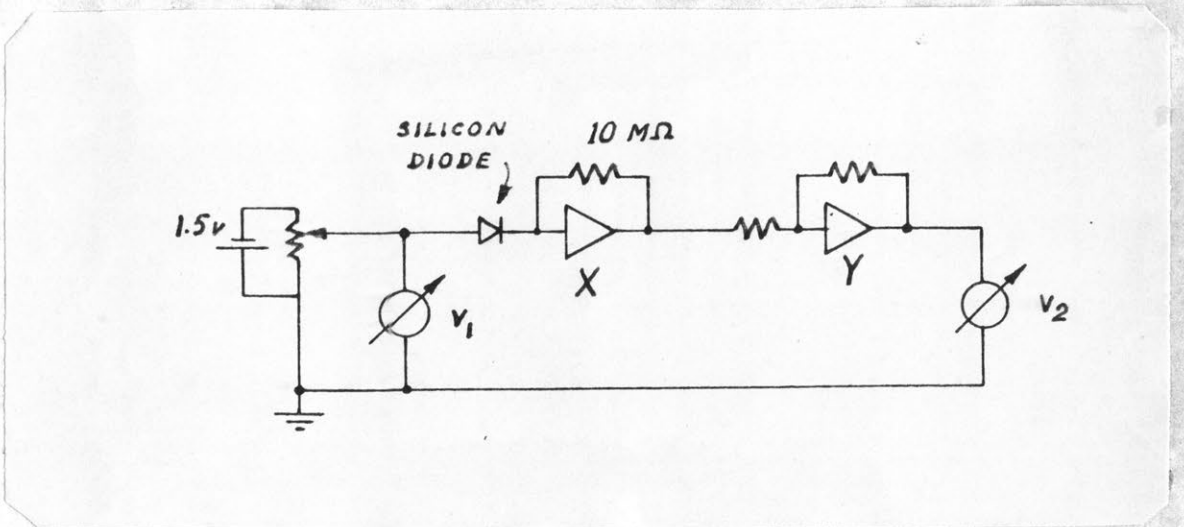


Fig. 12. Circuit to measure the D.C. characteristic of a diode.

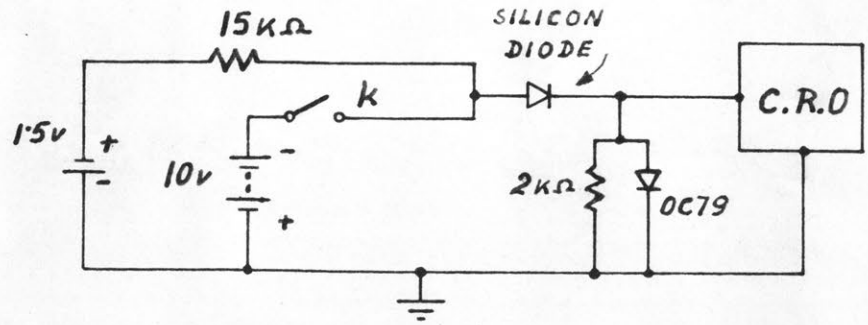


Fig. 13. Circuit to measure recovery time.

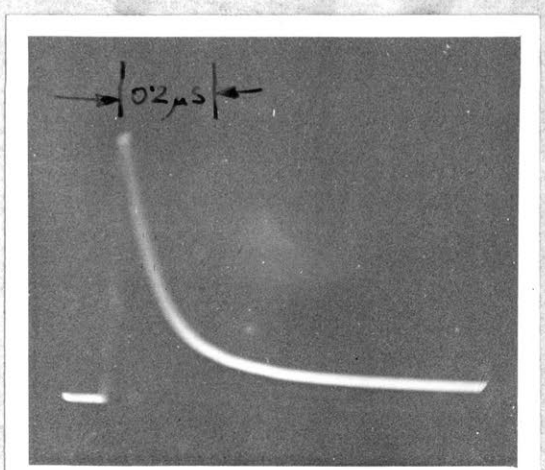


Fig. 14. A typical recovery characteristic of a silicon diode.

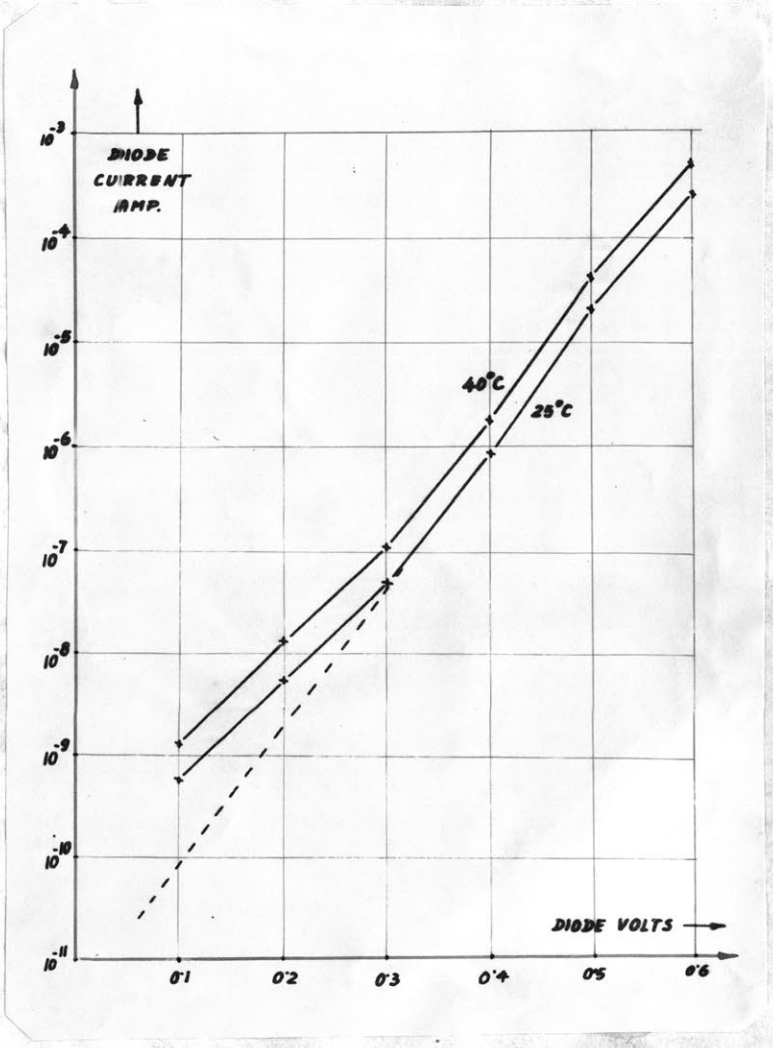


Fig.15. A typical forward characteristic of a silicon diode.

Examination of the diode equation (12) shows that there are 3 parameters to be considered i_s, i_L and A.

i_s varies considerably from diode to diode but may be as small as 10^{-14} amp. Its effect is to give logarithmic behaviour of the diode up to 0.5 volts in the forward direction: above this voltage large deviations from the logarithmic law can be expected.

i_L is of the order of 10^{-8} to 10^{-12} amp. and will determine the current in the forward direction up to the point where saturation and leakage current effects become comparable. In Fig. 15 this is shown as a change in slope of the logarithmic characteristic to roughly $\frac{1}{2}$ of the original value below 0.3 volts In the reverse direction the total reverse current is determined by i_L, the effect of i_s being negligible. Diodes with low leakage current are characterized by excellent logarithmic characteristic in the range of +0.1 to +0.5 volts and very high resistance in the nonconducting direction.

Table 1 gives the number of diodes with logarithmic behaviour for various types of diodes measured by the above method :-

TABLE 1.

Type	Total number	Number of diodes log. in the range +.1 to +0.5 volts.
Ferranti ZS10	20	2
Philips OA200	20	2
Hues HD6007	30	16

A recent publication [11] presents data on Raytheon silicon diodes. In a similar manner as above the number of diodes is listed for various types, but in terms of decades of current with logarithmic bevavior. Also, the same conclusion is reached i.e. only certain types will have a reasonable proportion of diodes which are logarithmic down to +0.1 volts.

The constant A determines the slope of the logarithmic curve and is reasonably constant for a given make of diode as a rule.

Equation (12) also shows that the diode current is a logarithmic function of temperature. This temperature effect appears to differ only slightly for all the diodes examined and typical curves are given in Fig. 15 for two values of temperature.

3.4.2. A.C. properties. The A.C. properties of semiconducting diodes are usually characterized by their capacitance, recovery time and rectification efficiency.

The capacitance can be measured by the substitution method using a standard Q- meter. All the diodes listed in Table 1 have a value of capacitance between 1$\mu\mu$F and 10$\mu\mu$F.

Reverse recovery time of a diode is the time required to regain a specified back-resistance (or back current) after the application of a reverse voltage pulse. Since it was established that drift and balance are largely dependent upon the behaviour of the diodes in the transit period the recovery times of various diodes were compared. Reverse performance of diodes is characterized by a fairy high surge of current which decays (roughly, exponentially) as the carriers disappear and the back resistance is restored. Values of reverse recovery time are affected by the

initial forward current, the circuit resistance and by the reverse voltage applied. There is no fixed standard of measurement of recovery time and various manufactures have adopted different methods. A simple method is shown in Fig. 13 : the switch k is closed and the voltage observed on a C.R.O. with short rise time (Tektronix.). A photograph is shown in Fig. 14. In the present application the absolute value is of no interest but it was found that the diodes ZS 10 whose performance is far worse than that of the diodes HD6007, have slightly shorter recovery times. Thus, it was concluded that, the recovery time is not an important factor at least for switching frequencies up to 10 kc/s.

The rectification efficiency is mainly a function of the forward resistance and the capacitance of the diode. Its effect becomes critical only for very high frequency applications i.e. well above 1 Mc/s and no attempt was made to measure it.[12]

3.5 Balance in practical modulaters.

3.5.1 Low frequency switching voltage. The modulator of Fig. 16 is balanced if, in the presence of a switching voltage, there is no potential difference between the diode junction and ground. For a switching voltage of square wave form and low repetition rate the condition for zero output during the conducting period. is that (Fig. 16.) :-

$$\frac{R_1}{R_2} = \frac{R_3 + \text{Resistance of diode 1}}{R_4 + \text{Resistance of diode 2}} \quad \text{or} \quad a = b$$

For a sufficiently large switching voltage of amplitude 'm' the diode resistance can be smaller than R_3 and R4 and

hence the ratio b will depend mainly upon these two resistors. If $a \neq b$ an unbalance voltage e_{oc} is developed where

$$e_{oc} = m \left(\frac{R_2}{R_1+R_2} - \frac{R_4}{R_3+R_4}\right) \quad \text{for} \quad R_o = \infty$$

but since R_o is normally much larger than $\left(\frac{R_3R_4}{R_3+R_4} + \frac{R_1R_2}{R_1+R_2}\right)$, which is the internal resistance of the open circuit voltage, the unbalance (R finite) is very nearly as above and can be rewritten as

$$e_{oc} = m \left(\frac{1}{1+a} - \frac{1}{1+b}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (13)$$

During the <u>nonconducting period</u> the condition for zero output is

$$\frac{R_1}{R_2} = \frac{R'}{R''} \quad \text{or} \quad a = c$$

since R' and R", the blocking resistances of the diodes, are much larger than R_3 and R_4.

If $a \neq c$ an unbalance voltage e_{on} is developed such that

$$e_{on} = m \frac{R_o}{R_o+R_p} \left(\frac{1}{1+a} - \frac{1}{1+c}\right) \quad \ldots\ldots\ldots\ldots\ldots (14)$$

where $R_p = R'R''/(R'+R'')$ is the internal resistance of the output voltage for $R_o = \infty$, and the above result follows from Thevenin's theorem. It is seen that if R_p is large the unbalance voltage e_{on} will be very small and also, that the unbalance is largely dependent upon the input resistor R_o; this is in agreement with experimental results which indicate that modulators with a lower input resistor will have smaller drift.

If the ratio a is made variable the conditions of interest which may arise are:-

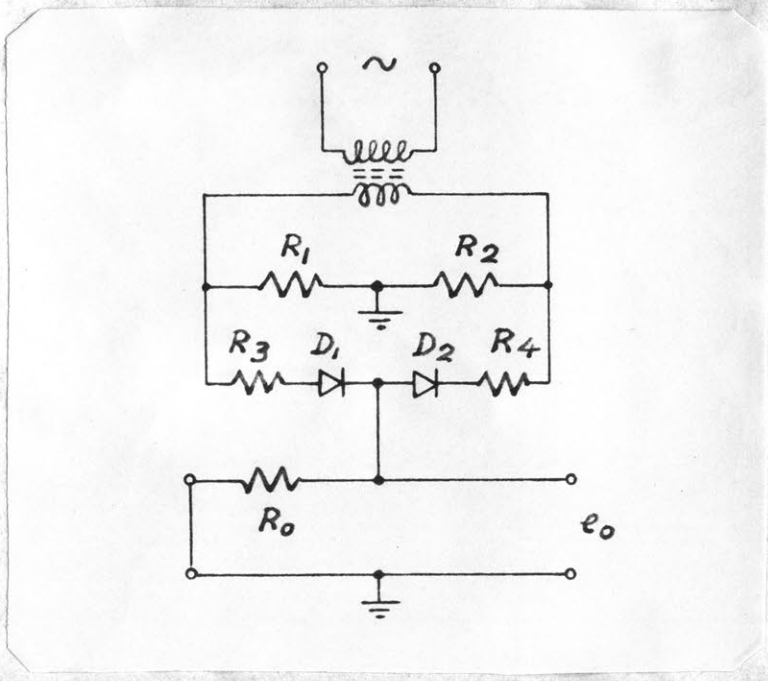


Fig. 16 Circuit illustrating balance and modulator drift.

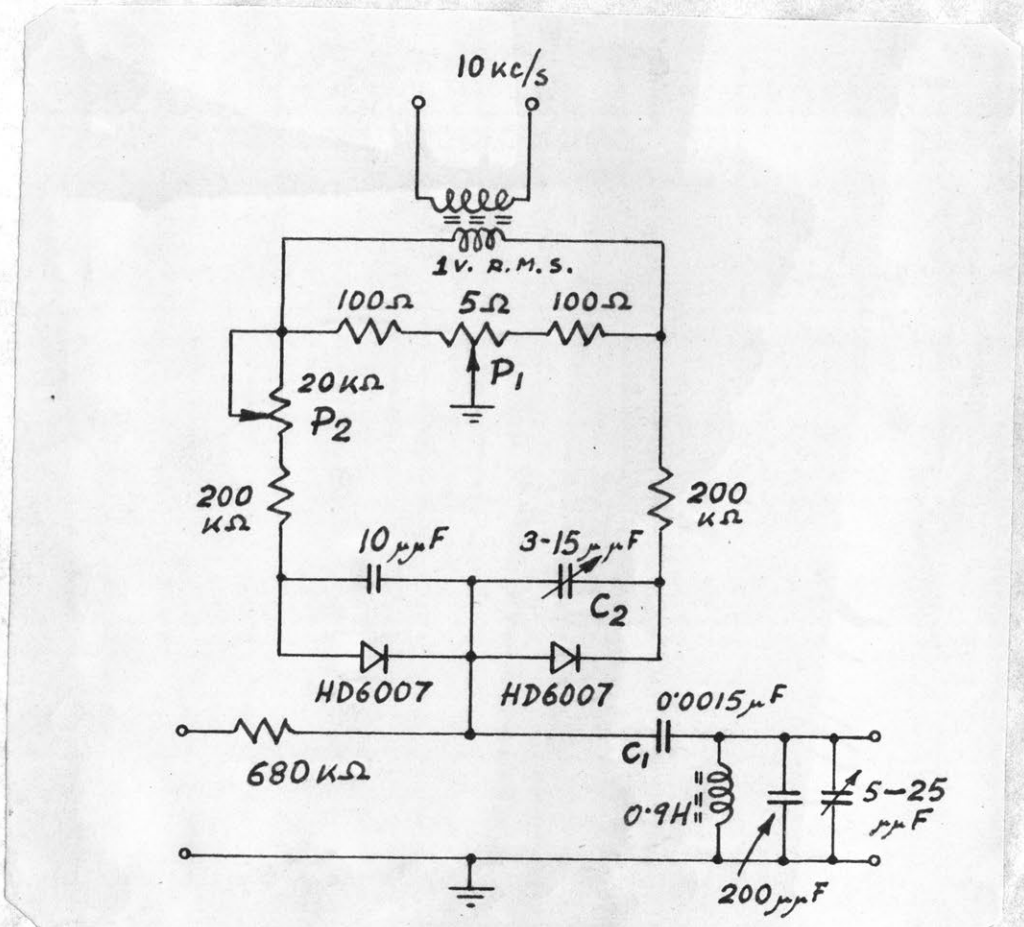


Fig 17 Complete modulator circuit

(i) $e_{oc} = e_{on}$ i.e. the voltages at the diode junction point during both conducting and nonconducting periods are the same. For this type of unbalance there is no alternating voltage at the diode junction but only a direct voltage of magnitude $e_{oc} = e_{on}$ which causes a current to flow in the input resistor. If, as in computing amplifiers, high impedances are involved this is very undesirable.

(ii) $e_{oc} = - e_{on}$. In this case a pure alternating voltage appears at the diode junction having no direct component. The main process of balancing however, is to reduce this voltage to a minimum: if present it will give rise to a spurious output and, as will be explaned later, may cause drift due to gain changes of the following A.C. amplifier.

(iii) $e_{on} \neq e_{oc}$. This condition is also undesirable since both D.C. and A.C. components will exist simultaneously.

The only case in which the potential difference between the diode junction and ground will remain zero at all times is when $e_{on} = e_{oc} = 0$ and examination of the equations (13) and (14) reveals that this condition can only be met if

$$a = b = c.$$

Clearly, a control must be introduced to vary either b or c, in addition to that required to vary a, in order to meet this requirement.

3.5.2. Higher frequency switching voltage.

Consider now a switching voltage of higher frequency of either square or sinusoidal waveform. Capacitive and transit effects i.e. the behaviour of the diodes in the intermediate

condition between fully conducting and fully nonconducting, should be examined.

During conduction the condition remains as before (a=b)

During the nonconducting period the capacitive reactance may be many times smaller then the resistance of the diodes and so the condition for balance is

$$a = \frac{\text{Impedance of diode 1.}}{\text{Impedance of diode 2.}}$$

thus both the phase and magnitude of the diode branch impedances should be controlled.

To ensure complete balance during the transit period it is required that the incremental resistance dv/di of the diodes should be equal at every point of their characteristic.[13] If the current-voltage relation is $i = i_s e^{v/AT}$, which is true for a small leakage current i_L and a sufficiently large diode voltage v (see equation 12) then :-

$$\frac{di}{dt} = i_s \frac{e^{v/AT}}{AT} = \frac{i}{AT} \quad \text{or} \quad \frac{dv}{di} = \frac{AT}{i}$$

i.e. for every current i and temperature T the incremental resistance is a function of A only. Since the current i is common for the two diodes the requirement for balance is that the diode constants A should be equal, which means, equal slope of the two logarithmic curves. There is no apparent reason why the actual shape of the characteristic should be critical but in practice it is difficult to achive satisfactory balancing unless both diodes follow a logarithmic law over the

whole operating region. (Fig. 15 dotted line).

Generally the constant A will not vary widely for a given type of diode but it was found that matching in pairs is very helpful . The D.C. characteristics are determined by the method described in Section 3.4, and pairs of diodes with logarithmic behaviour and similar slopes or possibly completely equal characteristics are selected. The work involved is relatively small and this will ensure best performance in the modulator.

3.6. Final modulator circuit.

The considerations in the last section led to the development of a modulator circuit as shown in Fig. 17. The switching voltage is 1 volt r.m.s. of 10 kc/s. supplied from a potcore transformer.

The potentiometer P_1 is used to obtain a suitable ratio 'a' and C_2 and P_2 are used to qualize the phase and magnitude of the diode branch impedances during the nonconducting period. Using these three controls a balance can quickly be obtained by trial and error. To check that not only A.C. balance is obtained but also that no D.C. voltage exists at the diode junction, the input resistor (680 KΩ) is disconnected or connected to ground and its effect on the A.C. balance is observed: the desired balance is obtained when no change takes place and the A.C. residual voltage is a minimum.

The resistive balancing arm consists of a potentiometer P_1 (5 ohms) and of two resistances of only 100Ω in order to

reduce the effect of capacitive coupling between the primary and the secondary windings of the supply transformer and to keep other pick-up voltages to a minimum. The series resistors of the diode branches have a value of 200 kΩ but these were used mainly because such wire wound resistors were available : a value of 100 kΩ would be preferable. These resistors are kept sufficiently high to ensure that operation is limited to the logarithmic region of the diodes but yet they are several times smaller than the input resistor R_o = 680 kΩ. There is a 10 kΩ potentiometer in only one of the diode branches and during the process of balancing a reversal of diode position may be required.

The balancing capacitor is only 10 μμF. but this has been proved adequate. A much larger value can not be tolerated since the capacitor is part of the tuned circuit and also in series with the resistors (200 kΩ) in each diode branch: this will increase the losses of the circuit and may reduce the modulator gain. The variable capacitor will balance capacitive differences and as will be shown later, reduce the effect of variations of diode resistance in the nonconducting direction.

The tuned circuit consists of an inductance of 0.9.Henry (Q = 40) and a capacitance of 200 μμF plus the tuning capacitor, the input capacitance of the valve amplifier and the balancihg capacitors. The total capacitance would be about 270 μμF. Then assuming that the losses in the circuit are determined by the input resistor only and that there is no interaction between the modulator and the tuned circuit a signal break frequency is

defined, as shown in Section 3.3, as :-

$$\frac{1}{2\pi R2C} = \frac{1}{2\pi \times 680 \times 2 \times 270 \times 10^{-12} \times 10^{3}} = 424 \text{ c/s.}$$

In fact it was found that for certain values of coupling capacitor C_1 the above result is very nearly obtained. In Fig. 18. is shown the experimental attenuation characteristic of the input signal for various values of C_1. It is seen that for C_1 = 200$\mu\mu$F the break frequency is 400 c/s and for C_1= 1500$\mu\mu$F F it is about 250 c/s. For larger values of coupling capacitor additional attenuation is introduced at the lower frequencies of somewhat less than 6 db/oct. The attenuation characteristic above 800 c/s was difficult to measure but the attenuation slope appeared to be more than 6 db/oct. In the present application a coupling capacitor 1500$\mu\mu$F or less can be used and it will be shown later that the drift-corrected amplifier will be stable.

In computer applications the input voltage to the modulator will be very small, except in cases of heavy overload, and the linearity of the modulator for a few millivolts is excellent. For input voltages smaller than 1 mV the gain may be slightly less, depending upon the residual voltage, but this is of no consequence since the modulator is in a feedback circuit and small variations in gain will not affect the operation. A D.C. input voltage of 1 mV will result in a 10 k c/s sinusoidal output voltage of appox. 0'9 mV peak to peak.

Fig. 19. shows the type of residual voltage which remains after the best possible balance has been obtained in the modulator; it is mainly the second harmonic of the switching

frequency and may be 0.1 mV or many millivolts depending on the diodes used. Normally, a residual voltage larger than 1 mV can not be tolerated. Fig 20. shows the output wave form of the modulator for an input frequency of 50 c/s and 500 c/s.

3.7. Modulator drift.

Since the modulator is essentially a bridge circuit, a change in any of the branches will disturb the balance. Only wire wound resistors are used and all capacitors are mica or air insulated. Under these conditions the drift due to changes in the diode characteristics is far larger than that due to changes in the other components. This was verified by recording the output for variable ambient temperature and over long periods of time when the diodes in the modulator were disconnected. Also, in bridge circuits the ouput due to unbalance is proportional to the applied voltage, and so, the switching voltage is kept as small as possible, and yet sufficiently large to cause conduction in the forward direction.

During the conducting period drift due to changes in diode resistance is considerably reduced by the large fixed resistors in series with the diodes. In fact if the voltage applied in sufficiently large this change can be made as small as desired, but this will increase the drift in the nonconducting and transit periods. The only significant cause of variations of diode characteristics is temperature changes and measurements have shown that the drift is less than 0.02 per ^{o}C for all pair of diodes examined at a forward voltage of 1 volt.

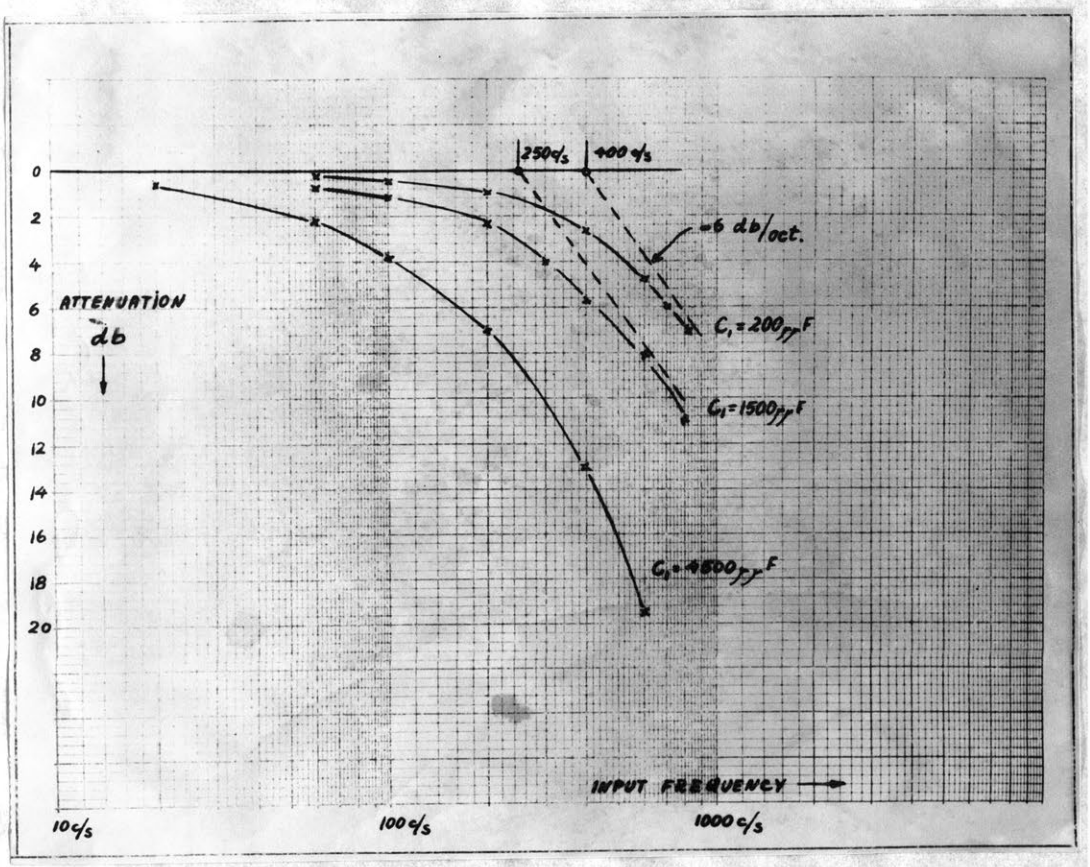


Fig. 18. The attenuation characteristic of the modulator of Fig. 17 for various values of coupling capacitor C_1.

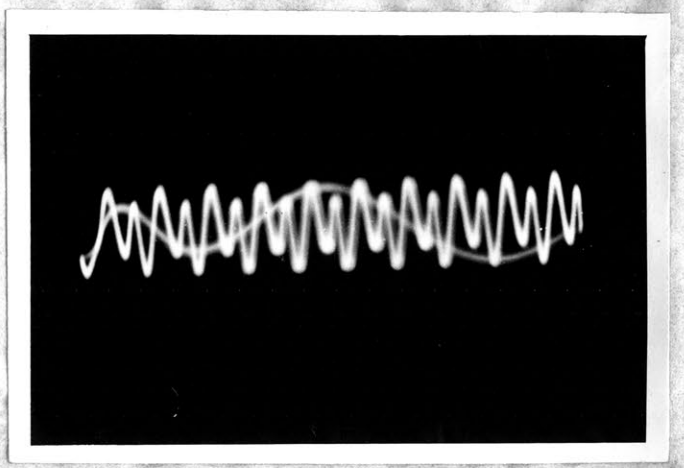
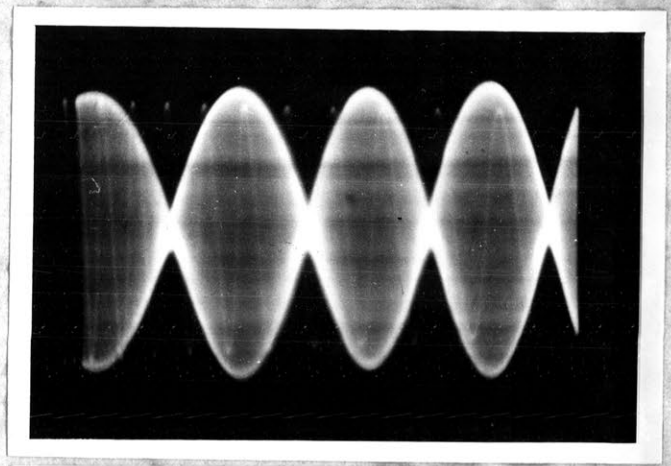


Fig.19. Residual voltage in the modulator after the best possible balance has been obtained.



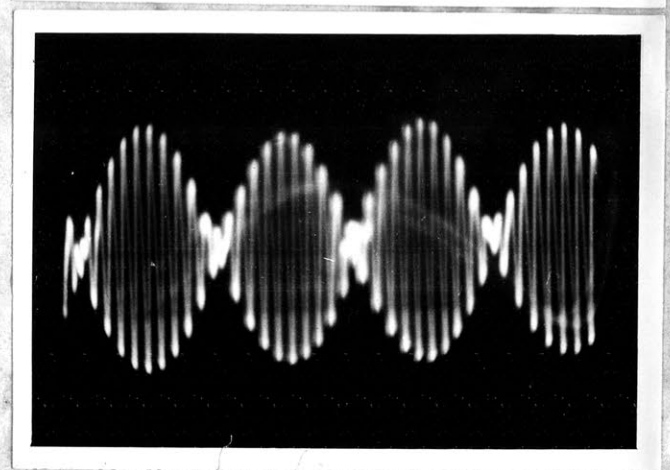


Fig.20. Modulator output for an input frequency of 50 c/s and 500 c/s.

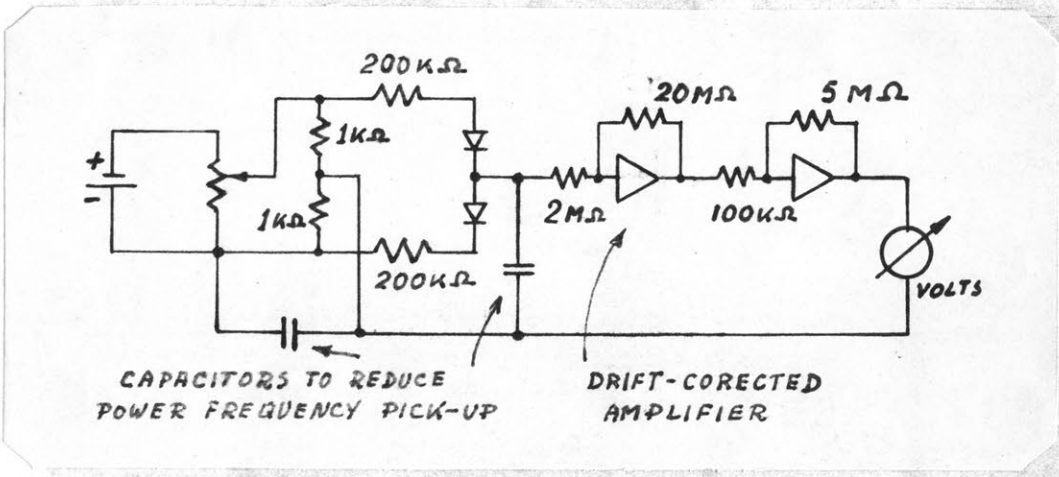


Fig. 21. Circuit to measure modulator drift in the conducting direction

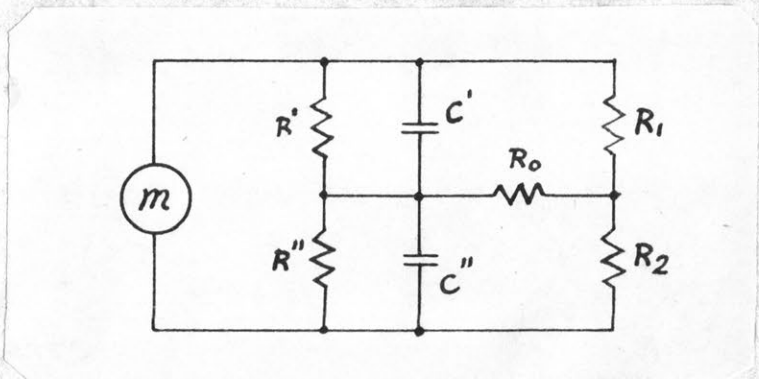


Fig. 22. Simplified modulator circuit applicable only when the diodes are not conducting.

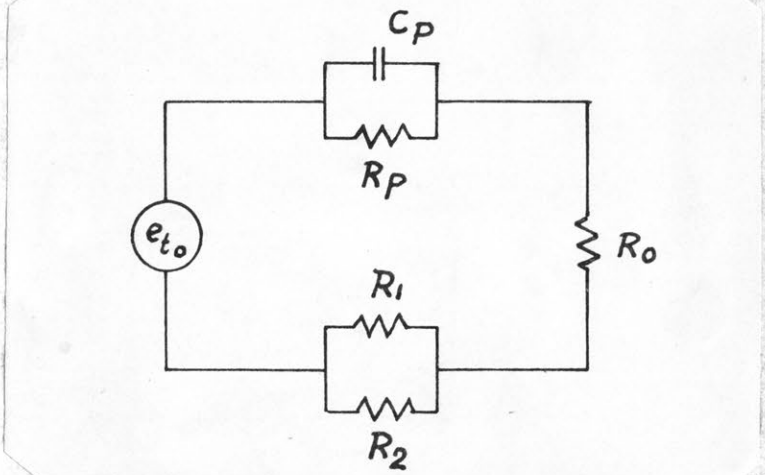


Fig. 23. Equivalent modulator circuit for a step input of switching voltage in the nonconducting direction.

The simple set-up of Fig. 21. was used: basicly it is the same modulator circuit but a D.C. voltage is applied instead of an A.C. switching voltage. The diode junction is connected to the input of an operational amplifier and its output measured. The diodes are kept in a metal container and heat is applied from outside. Any direct application of heat will result in an unbalance larger than the above figure, and the following conclutions were reached for the modulator :-

(i) The diodes should be kept in a closed compartment.

(ii) They should not be widely separated

(iii) They should not be located close to walls or other components which are subject to wide temperature variations.

(iv) Air drafts should be avoided.

During the nonconducting period capacitive as well as resistive components are of importance. Since the balancing capacitor is several times larger than the capacitance of the diode, the total capacitance is effectively constant and only changes in resistance need be considered. To show that the diode capacitance does not affect the stability, the value of the balancing capacitor was increased, but this resulted in no improvement. Thus , in the following only unbalance in diode resistance is investigated.

Consider the modulator unbalanced in the nonconducting direction to such an extend that an unbalance voltage e_{on} would appear at the diode junction in the absence of all capacitive effects. Then with a suddenly applied blocking voltage 'm' it was shown in section 3.5. that

$$e_{on} = m \frac{R_o}{R_o+R_p} \left(\frac{1}{1+a} - \frac{1}{1+c}\right) \quad \ldots\ldots(14)$$

The circuit capacitance, however, will considerably affect this unbalance. The time constant of the series resistor (200 kΩ) and the balancing capacitors (10 μF) is only 2×10^{-6} seconds, and in the following analysis can be neglected. Thus the modulator circuit can be simplified as shown in Fig.22 where R',R" and C',C" are the respective resistances and capacitances of the two diodes. The conditions for balance can be stated as

$$a = \frac{R_1}{R_2} = \frac{R'}{R''} = \frac{C''}{C'}$$

In the following it is assumed that $a = R_1/R_2 = C''/C'$ but $R'/R'' = c \neq a$, and the output e_t developed across R_o is derived for a suddenly applied blocking voltage of magnitude m.

The open circuit value of e_t is given in Laplace Transform notation by

$$E_{to} = M\left[\frac{R_2}{R_1+R_2} - \frac{\frac{1}{\frac{1}{R''}+pC''}}{\frac{1}{\frac{1}{R''}+pC''}+\frac{1}{\frac{1}{R'}+pC'}}\right] =$$

$$= M\left[\frac{R_2}{R_1+R_2} - \frac{R''(1+pC'R')}{(R'+R'')\left\{1+p\frac{R'R''}{R'+R''}(C'+C'')\right\}}\right]$$

$$E_{to} = M\left[\frac{R_2}{R_1+R_2} - \frac{R''}{R'+R''}\,\frac{(1+pC'R')}{(1+pC_pR_p)}\right] \quad \text{where} \quad R_p = \frac{R'R''}{R'+R''}$$

$$\text{and} \quad C_p = C'+C''$$

For a step input $M = \frac{m}{p}$

$$E_{to} = m\left[\frac{R_2}{p(R_1+R_2)} - \frac{R''}{p(R'+R'')}\frac{(1+pC'R')}{p(1+pC_pR_p)}\right] =$$

$$= m\left[\frac{R_2}{p(R_1+R_2)} - \frac{R''}{p(R'+R'')} + \frac{R''}{(R'+R'')(1+\frac{1}{C_pR_p})} - \right.$$

$$\left. - \frac{R''C'R'}{(R'+R'')C_pR_p(1+\frac{1}{C_pR_p})}\right]$$

$$E_{to} = m\,(\frac{1}{1+a} - \frac{1}{1+c})(\frac{1}{p} - \frac{1}{p+\frac{1}{C_pR_p}})$$

The circuit can now be represented as in Fig.23. Assuming that $R_o >> \frac{R_1R_2}{R_1+R_2}$ the voltage developed across R_o is given by:-

$$E_t = E_{to}\frac{R_o}{R_o+\frac{1}{\frac{1}{R_p}+pC_p}} = E_{to}\frac{R_o}{R_o+R_p}\frac{(1+pC_pR_p)}{(1+pC_pR_T)} \quad \text{where } R_T = \frac{R_oR_p}{R_o+R_p}$$

$$E_t = m\,(\frac{1}{1+a} - \frac{1}{1+c})(\frac{1}{p} - \frac{1}{p+\frac{1}{C_pR_p}})\frac{R_o}{R_o+R_p}\frac{(1+pC_pR_p)}{(1+pC_pR_T)} \quad \text{or}$$

$$E_t = e_{on}\frac{1}{p(1+pC_pR_T)}$$

The solution as a function of time is :-

$$e_t = e_{on}(1 - e^{-t/C_pR_T}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (15)$$

The initial rise of voltage per second is then:-

$$\frac{e_{on}}{C_pR_T} = \frac{m}{C_pR_p}(\frac{1}{1+a} - \frac{1}{1+c})$$

and is independent of the input resistor R_o.

Thus, for a sufficiently high switching frequency, the unbalance in the nonconducting direction is mainly determined by the time constant C_pR_p and can only be improved by increasing this term. C_p is part if the tuned circuit and cannot be increased indefinitely but R_p is a property of the particular diode used and should be as high as possible. It is interesting to compute the unbalance at the end of a blocking period for the modulator of Fig.17 for both $R_o = 1\ M\Omega$ and $R_o = \infty$. With a switching frequency of 10 kc/s, $t = 1/20{,}000$; also if $R_p = 10^9\Omega$ and $C_p = 30\times10^{-12}$ F:-

$e_t = m\left(\frac{1}{1+a} - \frac{1}{1+c}\right) 0.812 \times 10^{-3}$ volts . . . . .for $R_o = 1\ M\Omega$

$e_t = m\left(\frac{1}{1+a} - \frac{1}{1+c}\right) 1.66 \times 10^{-3}$ volts . . . . . for $R_o = \infty$

It is clear that at 10 kc/s the unbalance due to changes in diode resistance in the nonconducting direction is reduced by a factor of about 1000 and is almost independent of the input resistor R_o.

The effect of drift arising in the transit period is not reduced by the modulator circuit as are those which occur during the period of full conduction and complete nonconduction. Experimental results tend to show that this effect can be made small only by using diodes whose characteristics are essentially logarithmic, as mentioned in Section 3.5.

In conclusion it may be said that the modulator output due to unbalance is mainly due to changes in diode characteristics with temperature, but fortunately such changes are completely reversible and give rise to no long term drift.

4. THE DRIFT-CORRECTOR

4.1 General

The modulator described in Section 3 was used to build drift-correctors specifically designed to work in conjunction with the high gain D.C. amplifier used in UTAC.[16] They consist of an input filter, modulator, A.C. amplifier, demodulator, output filter, monitor and cathode follower as shown in Fig. 24. The modulated carrier is amplified in the A.C. amplifier and then rectified in the phase sensitive demodulator to obtain an amplified version of the input signal. The total D.C. to D.C. gain is 400 and since the drift of the D.C. amplifier used does not exceed 40 mV this now corresponds to a maximum drift of only 0.1 mV; ~~since~~ the reduction of the D.C. amplifier drift is proportional to the gain of the drift-corrector. This is smaller than the long term zero stability of the modulator, and so there is no reason to use a higher value of drift-corrector gain. The individual sections of the drift-corrector are described below.

4.2 The input filter.

Its main purpose is to shape the frequency response of the drift-corrector but it will also reduce the carrier frequency leak back to the input of the D.C. amplifier, which however, even without a filter is negligible.

Consider the input filter on its own (Fig. 25), and neglect the effect of the modulator input resistor R_o. Then, its transfer function is

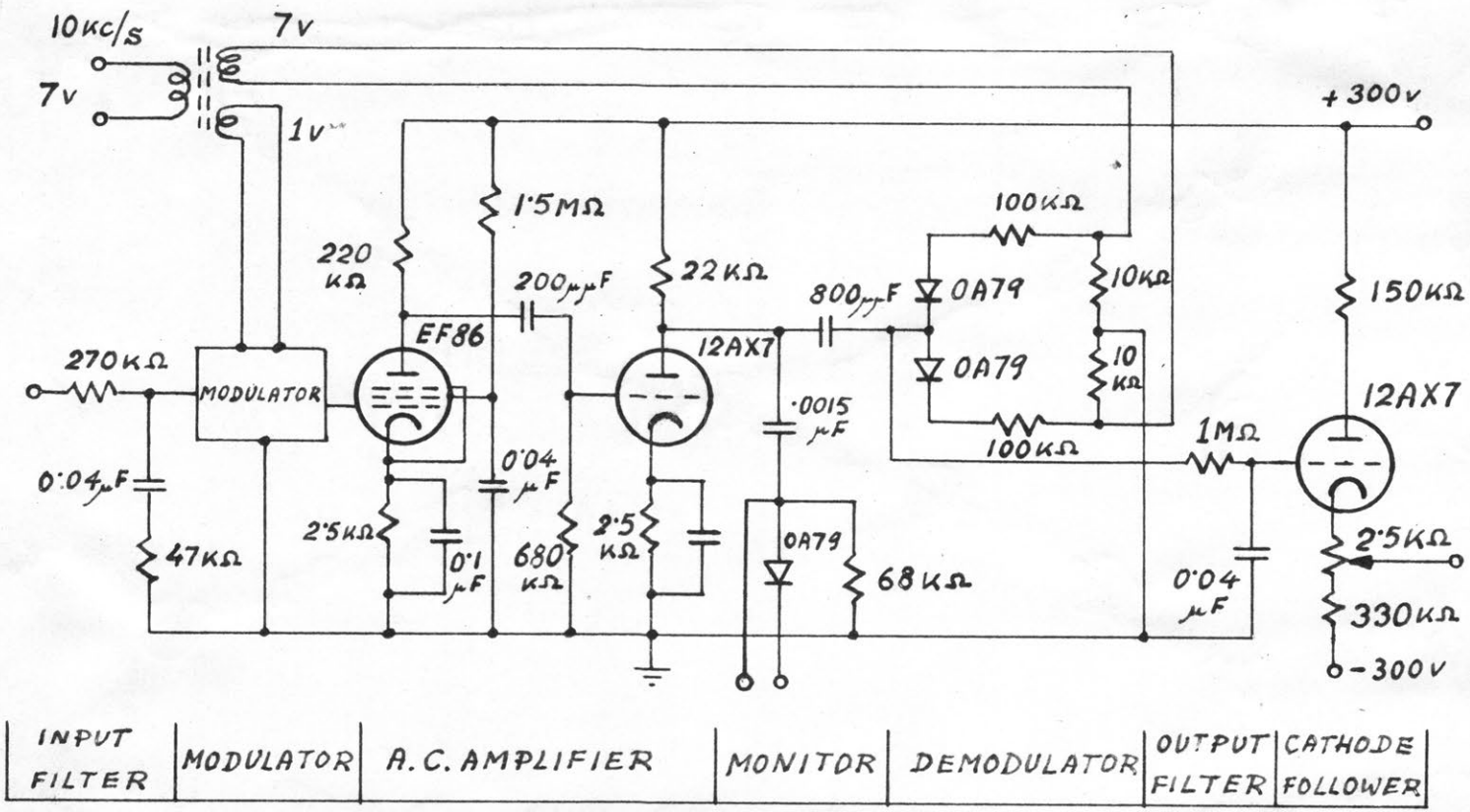


Fig. 24. Circuit diagram of the complete drift-corrector.

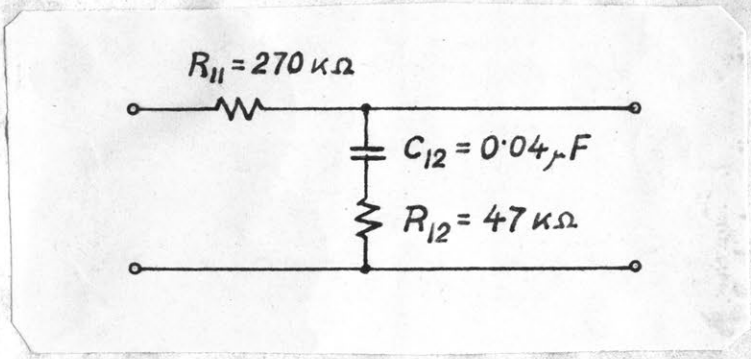


Fig.25. The input filter

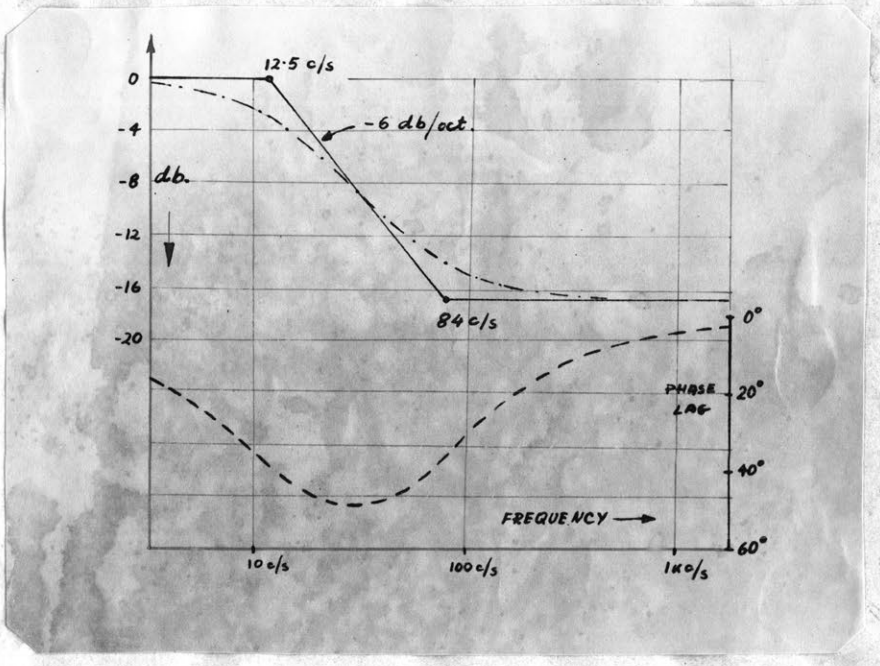


Fig.26. Attenuation and phase characteristics of the input filter

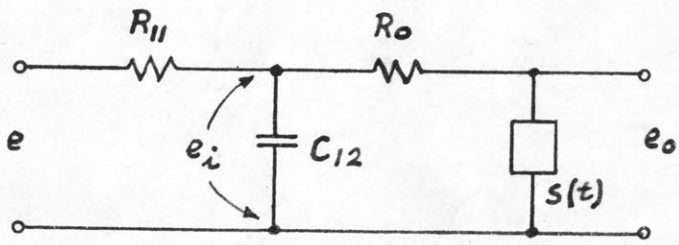


Fig.27. Circuit to explain the additional attenuation due to the input filter.

$$\frac{R_{12} + \frac{1}{pC_{12}}}{R_{12}+R_{11}+\frac{1}{pC_{12}}} = \frac{pC_{12}R_{12} + 1}{pC_{12}(R_{12}+R_{11}) + 1}$$

Clearly there are two break frequencies

$$\frac{1}{2\pi C_{12}(R_{11}+R_{12})} = 12.5 \text{ c/s} \quad \text{and}$$

$$\frac{1}{2\pi C_{12}R_{11}} = 84 \text{ c/s}$$

The attenuation-phase characteristic is shown in Fig.26. The use of the input filter permits obtaining a slope of - 9 db/oct and thus increasing the first break frequency of the drift-corrector by about 3 octaves.

If now the input resistor of the modulator R_o is considered, but the resistor in the parallel branch is neglected, the circuit becomes as shown in Fig. 27, where 's' is a periodic switch and represents the action of the diodes. The output of such a modulator is zero when the switch is closed and is equal to the voltage e_i' across the parallel capacitor when the switch is open. The voltage e_i' however will rise exponentially with a time constant $R_{11}C_{12} = 0.27\text{x}10^{6}\text{x}0.04\text{x}10^{-6} = 0.011$ seconds, when the switch is open, and will fall with a time constant $C_{12}R_{11}R_o/(R_{11}+R_o) = 0.008$ seconds when the switch is closed. The period for which the switch is open or closed is $0.5\text{x}10^{-4}$ seconds i.e. about 200 times smaller than the above time constants and hence the voltage e_i' is a D.C. voltage (or a low frequency voltage depending on the input signal) with a very small ripple of 10 kc/s.

The D.C. current which flows through the input resistor R_o is $e_i/2R_o$ and the same current must flow through the resistor R_{11} which is given by $(e - e_i)/R_{11}$ or

$$\frac{e - e_i}{R_{11}} = \frac{e_i}{2R_o} \qquad \text{and} \qquad e_i = e\,\frac{2R_o}{R_{11}+2R_o}$$

Now, since e_i is effectively the output voltage when the switch is open, the input filter will reduce the gain of the modulator by the factor

$$\frac{2R_o}{R_{11}+2R_o} = \frac{2\text{x}0.68\text{x}10^6}{10^6(0.27 + 2\text{x}0.68)} = 0.84$$

The resistor in the parallel branch will slightly alter this result but the main purpose of this discussion was to show that all input signals will suffer a constant attenuation in addition to the normal frequency attenuation due to the input filter.

The effect of the input filter on the input impedance Z_o is to effectively reduce its value for all frequencies above 12.5 c/s; this is discussed in detail in Section 5.1.

4.3 The A.C. amplifier

An R.C. coupled amplifier is used having as an input stage a pentode with a gain of 140. This is followed by a triode which works directly into the demodulator. The total A.C. gain is 1800. The design of this amplifier is not critical, however the following points have been considered:-

(i) The input stage may affect the operation of the modulator. Should the capacitance of the input valve change

in operation, the resonant circuit will not be tuned to the carrier frequency and this will result in loss of gain, phase shift of the carrier frequency, distortion of the envelope of the modulated signal and may also disturb the balance of the modulator. Most serious could be the Miller capacitance i.e. the effective capacitance which appears at the input of an electronic valve due to the feedback action of the grid-plate capacitance and the stage gain. If a triode is used with a grid-plate capacitance of 1.7$\mu\mu$F and a stage gain of 50, the valve will have an equivalent input capacitance of about

1.7 x 50 = 85$\mu\mu$Farad.

This is nearly half the value of the tuning capacitor of the modulator (Fig. 17) and thus, the modulator performance will depend upon the stability of the input valve.

To avoid this a pentode is used which with a stage gain of 140 and grid-plate capacitance of 0.025$\mu\mu$F has a Miller capacitance of only 0.025 x 140 = 3.5$\mu\mu$F.

(ii) Care was taken to keep all break frequencies of the amplifier higher than 10 kc/s, the frequency of the switching voltage. Consider the equivalent diagram of a R.C. coupled valve amplifier as shown in Fig. 28, where

e' is the input voltage

e" - the output voltage

R_a - the plate resistance of the electronic valve

R_L - the load resistance

R_g - the grid resistor of the following valve

C - the total capacitance, including plate and stray capacitance and the input capacitance of the following valve.

μ - the amplification factor

The transfer function of such an amplifier is

$$-\frac{E''}{E'} = \frac{\mu R_L R_g}{(R_L R_g + R_a R_L + R_a R_g)} \frac{1}{\left(1 + \frac{R_L R_g R_a}{R_L R_g + R_a R_L + R_a R_g} pC\right)} = \frac{h}{1 + pT}$$

In Section 3.2 it was shown that the voltage to be amplified is a suppressed carrier amplitude modulated wave. The effect of a filter upon such a voltage can be examined using Bifid operators[14] and to find the output e" of a four-terminal network having a transfer function $G = 1/(1+pT)$, when the input is $e' = f(t) \cos w_c t$, where $f(t)$ can be any function of time, one writes

$$G = \frac{1}{1+pT} = \frac{1}{1+p_m T + p_c T} = \frac{1 + p_m T - p_c T}{(1 + p_m T)^2 - p_c^2 T^2}$$

but since $p_c^2 = - w_c^2$ hence

$$G = \frac{(1 + p_m T) - p_c T}{(1 + w_c^2 T^2) + 2p_m T + p_m^2 T^2}$$ and the output will be

$$\left[\frac{(1+p_m T)\, F(p_m)}{(1+w_c^2 T^2)+2p_m T+p_m^2 T^2}\right] \cos w_c t + \left[\frac{w_c T\, F(p_m)}{(1+w_c^2 T^2)+2p_m T+p_m^2 T^2}\right] \sin w_c t$$

The quantities in the square brackets are functions of p_m and can be evaluated by Laplace Transforms for any given modulating voltage $f(t)$. Before operating on p_m however, consider the denominator of the above expression. For all frequencies $w_c \gg w_m$ one has $2p_m T + p_m^2 T^2 \ll (1 + w_c^2 T^2)$

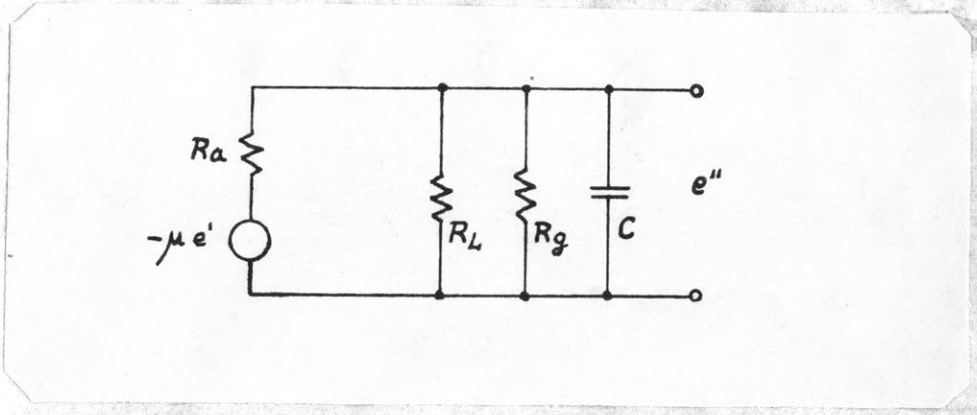


Fig. 28. Equivalent diagram of a R.C. coupled A.C. amplifier

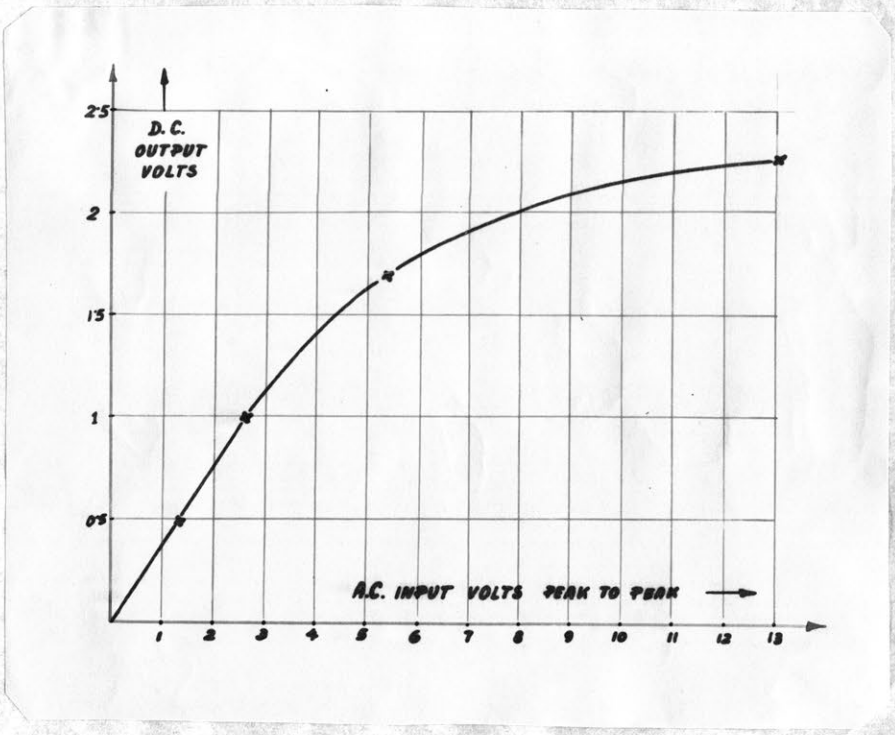


Fig. 29. Input versus output characteristic of the demodulator

and for $e' = f(t) = \text{Sin } w_m t$ the output becomes

$$e'' = \frac{\text{Sin } w_m t}{1+ w_c^2 T^2} \text{Cos } w_c t + \frac{w_m T \text{ Cos } w_m t}{1+ w_c^2 T^2} \text{Cos } w_c t + \frac{w_c T \text{ Sin } w_m t}{1+ w_c^2 T^2} \text{Sin } w_c t$$

The second term can be neglected, since for $w_c T < 1$ it is much smaller than the first term and for $w_c T > 1$ it is much smaller than the third term, provided that $w_m \ll w_c$.

Thus the output becomes

$$e'' = \frac{\text{Sin } w_m t}{1+ w_c^2 T^2} \text{Cos } w_c t + \frac{w_c T \text{ Sin } w_m t}{1+ w_c^2 T^2} \text{Sin } w_c t \quad \text{or}$$

$$e'' = \text{Sin } w_m t \; \frac{\text{Cos } (w_c t - \gamma)}{\sqrt{1 + w_c^2 T^2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (16)$$

$$\text{tg } \gamma = w_c T$$

The last equation indicates that only the carrier will suffer phase shift and that the signal frequency is not affected, provided that $w_m \ll w_c$.

The Miller capacitance of the triode amplifier following the pentode, with a gain of 13 and a grid-plate capacitance of $1.7 \mu\mu F$ is $12 \times 1.7 = 22 \mu\mu$Farad. The total capacitance, including plate and stray capacitance, will be about $30 \mu\mu F$. Then with $R_a = 2$ MΩ (for the valve EF86), $R_L = 220$ kΩ and $R_g = 680$ kΩ the time constant of the input stage becomes

$$T = C \frac{R_L R_g R_a}{R_L R_g + R_a R_g + R_L R_a} = 0.45 \times 10^{-5} \text{ seconds.}$$

It follows from equation (16) that a carrier frequency of 10 kc/s will suffer a phase shift of

$$\gamma = \text{tg}^{-1} w_c T = \text{tg}^{-1} 2\pi \times 10^4 \times 0.45 \times 10^{-5} = 16^\circ$$

The time constant of the triode amplifier is very small, since the plate load resistance is only 22 kΩ, and the phase shift introduced is negligible.

Phase shift of the carrier frequency is not important from the stability point of view in a feedback circuit and its only effect is to reduce the effective gain of the demodulator.

(iii) Since the modulator balance can never be perfect there is always some residual A.C. voltage at the amplifier input ; thus even when the modulator input is zero there is an output from the phase sensitive demodulator. Should the gain of the A.C. amplifier change under this circumstances a form of drift arises. In practice the residual voltage may be equivalent to up to 1 millivolt D.C. input and so a 10% change in amplifier gain will cause a drift of 0.1 mV.

4.4 The demodulator

Any type of phase sensitive demodulator can be used whose long term drift is smaller than 40 mV ; this will correspond to an equivalent modualtor drift of 0.1 mV for a drift-corrector gain of 400. In this case two germanium diodes are employed in the same type of bridge circuit as is used in the modulator. No adjustment is required here and normal 10% carbon resistances are satisfactory. The switching voltage is provided from the same transformer which supplies the modulator (Fig. 24).

The action of the demodulator is simple. The diodes will alternately block or conduct and thus pass or attenuate

alternately half cycles of the input alternating voltage in a similar manner as the modulator. The output will depend upon the phase relation between the input voltage and the switching voltage. For a suppressed carrier modulated volatge input $\text{Sin } w_m t \text{ Cos } (w_c t + \gamma)$ and a switching voltage $\text{Cos } w_c t$ the output will contain the term[15]

$$\text{Sin } w_m t \text{ Cos } \gamma \quad \ldots\ldots\ldots\ldots\ldots\ldots (17)$$

which is the desired output. The carrier frequency term and the higher harmonics, which will also be present, are greatly attenuated in the following R.C. low pass filter and can be neglected.

Equation (17) shows that the demodulator gain is proportional to the Cosine of the phase angle between the carrier and the switching frequency and for $\gamma = 90^\circ$ the output is zero. Thus, care was taken to keep the carrier phase shift, which may occur in the modulator or in the A.C. amplifier, to a minimum. Since the modulator employs a tuned circuit here the carrier phase shift is zero but it was shown that the input stage of the A.C. amplifier will shift the phase of the carrier by 16°. However $\text{Cos } 16^\circ = 0.96$ which is very close to unity.

The demodulator switching voltage is 7 volts r.m.s. and the input versus output relation is shown in Fig. 29; it is seen that the demodulator is linear for signal inputs of up to 4 volts peak to peak, and that the output can never exceed 2.5 volts. This however is ample, since in normal operation the A.C. input is the residual voltage only, which

should not exceed 1.5 volts peak to peak, the actual signal being many times smaller.

The bridge resistances are 10 kΩ, and the series resistance of the diode branches is 100 kΩ in order to keep the switching power low. The coupling capacitor (800 μμ Farad) is chosen so that no phase shift of the modulating signal takes place. A similar effect as in the modulator was observed; for a large value of coupling capacitor the gain of the modulator will begin to fall at some frequency, which also depends on the diode series resistances. For the above values (C = 800 μμF and R = 100 kΩ) the signal frequency for which the gain will begin to fall is well outside the frequency region of interest.

4.5 The output filter and cathode follower

The primary purpose of the output filter is to shape the frequency response of the drift-corrector and to remove the carrier frequency and higher harmonics from the output. It is a simple R.C. lag network with a break frequency of 4 c/s; its attenuation-phase characteristic is given in Fig. 30.

The cathode follower is used because of the requirement of the UTAC D.C. amplifier for a low output impedance. The output impedance of a cathode follower is very nearly $1/g_m$, where g_m is the mutual conductance. In this case g_m = 1.5 mA/V and the output impedance is only 670 ohms. The output potentiometer (total value 2,5 kΩ) will increase the output impedance of the circuit but this has been proved

to be of no consequence. The drift of the cathode follower was found to be much smaller than the required minimum of 40 mV.

The output potentiometer controls the D.C. level of the drift-corrector output and when used in conjunction with a D.C. amplifier it is effectively the balance control i.e. the control required to obtain zero output for zero input of the combined amplifier.

4.6 The monitor

Before demodulation a small portion of the A.C. signal is rectified (Fig. 24) and the voltage obtained is a measure of the A.C. amplifier output ; this is displayed on a output meter for monitoring purposes. In the absence of an input signal the monitor indicates the residual voltage of the modulator. Under these conditions the A.C. output can change only due to drift in the modulator or due to change in amplifier gain; normally a change in modulator balance will cause an increased meter reading and a change in amplifier gain a reduction in meter reading. Also, an overload or equipment failure is immediately apparent.

4.7 Balancing and testing of the drift-corrector.

The balancing , testing and setting-up can only be done if a suitable test rack is available. The complete test procedure as adopted for this unit is presented in Appendix A. Once the drift-corrector has been set-up the only control which requires adjustment is the output potentiometer; such an adjustment only becomes necessery

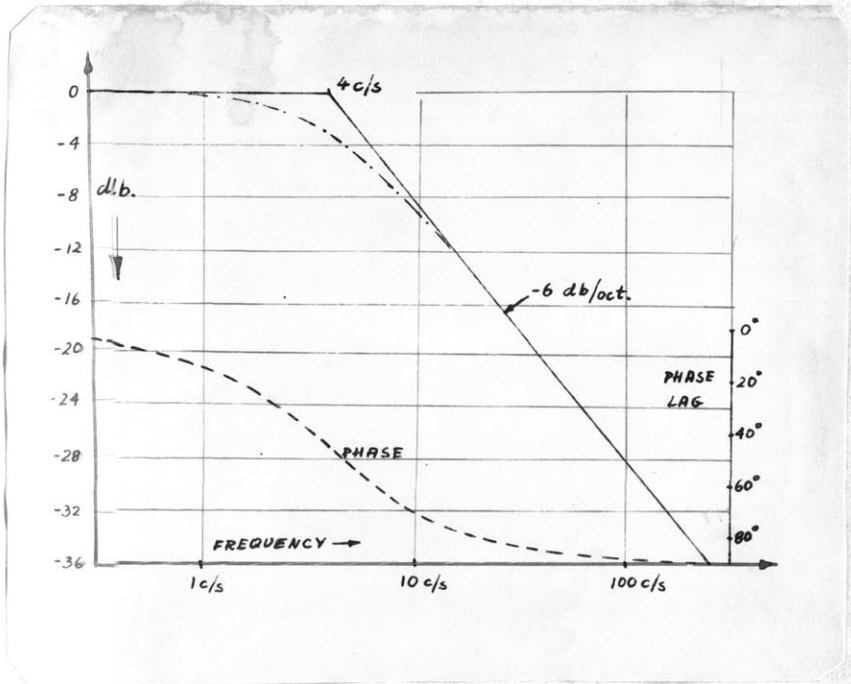


Fig. 30. Attenuation-phase chracteristic of the output filter

when a different D.C. amplifier is used or some of the drift-corrector components have been replaced.

4.8 Frequency response.

As was pointed out in Section 1.2, the drift-corrector is connected so that at low frequencies it is in series with the D.C. amplifier and at higher frequencies the D.C. amplifier alone is used. This is achieved by having a second input to the input stage of the D.C. amplifier and this is shown in a simplified form in Fig. 31. Under these conditions the transfer function of a drift-corrected amplifier is given by equation (1) and the frequency response function is

$$KG(jw) = \left[1 + K_2G_2(jw)\right] K_1G_1(jw)$$

The attenuation-phase characteristic of $K_1G_1(jw)$, the frequency response function of the D.C. amplifier, is given in Fig. 32. The low frequency gain is 100,000 up to 400 c/s and then falls off at a rate of 9 db/oct, with a minimum phase margin of 40°

So that the combined amplifier is stable in the presence of feedback, the overall phase lag must be less than 180° at all frequencies at which the combined gain is greater than unity, but normally a phase margin of 40° is required. For this to be so for the given D.C. amplifier, the phase shift due to the term $\left[1 + K_2G_2(jw)\right]$ should be zero for all frequencies above the lowest break frequency of the D.C. amplifier, which is 400 c/s. This will be the case if the gain of the drift-corrector $K_2G_2(jw)$ is small compared

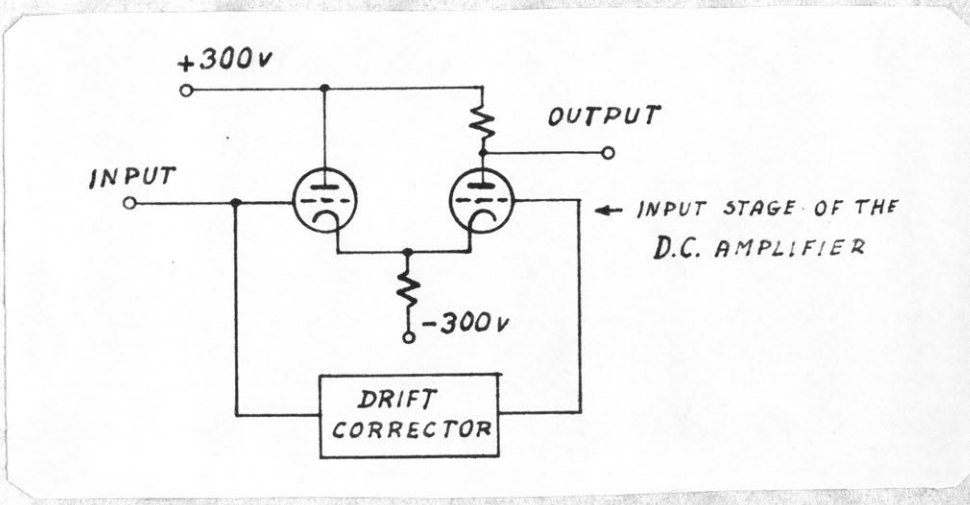


Fig. 31. Basic method used to connect a drift-corrector to the input stage of a D.C. amplifier

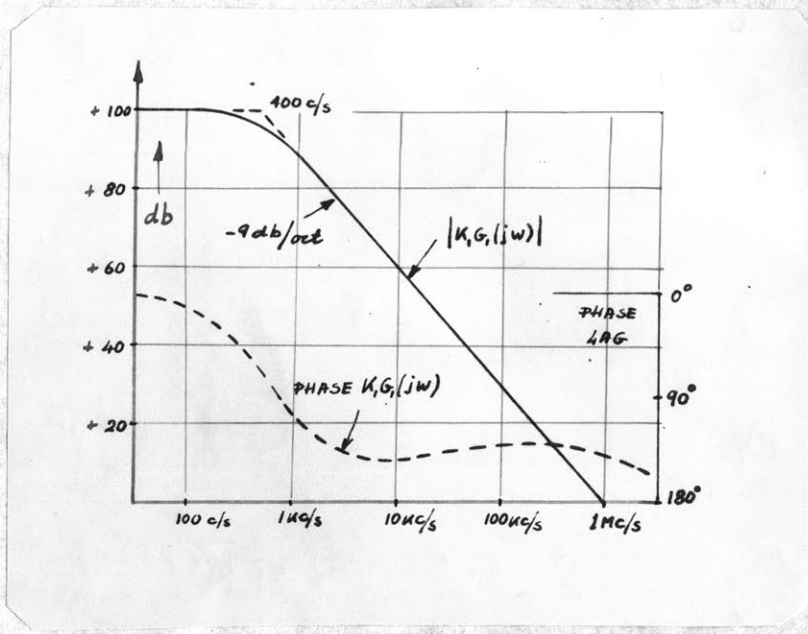


Fig. 32. The attenuation-phase characteristic of the high gain D.C. amplifier used in UTAC.

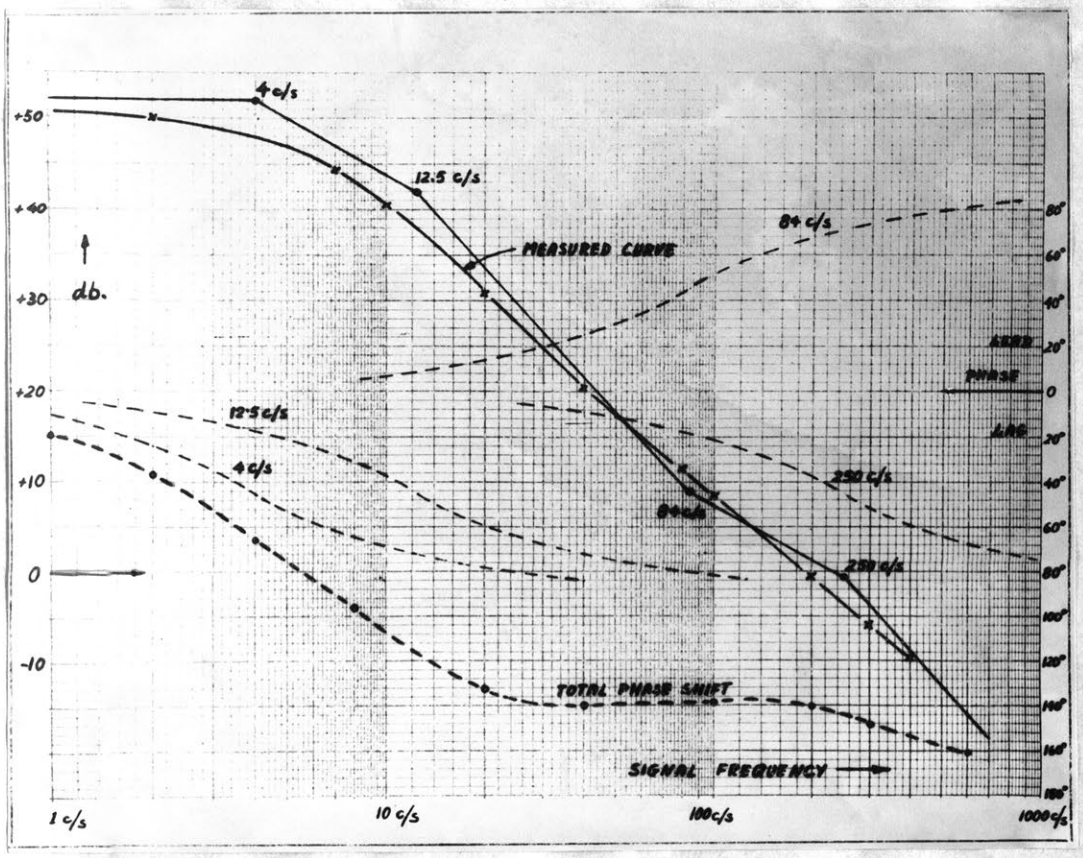


Fig. 33. The attenuation-phase characteristic of the complete drift-corrector.

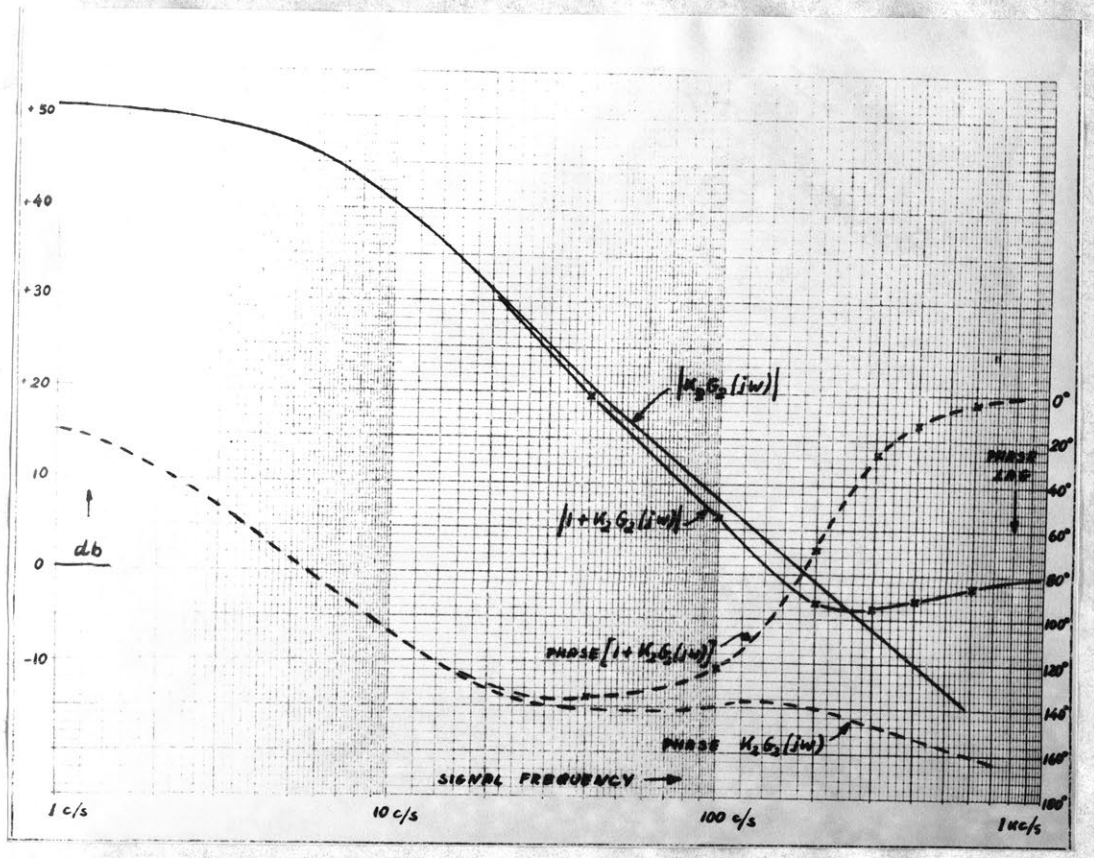


Fig. 34. The attemuation- phase characteristics of $K_2G_2(jw)$ and $[1 + K_2G_2(jw)]$

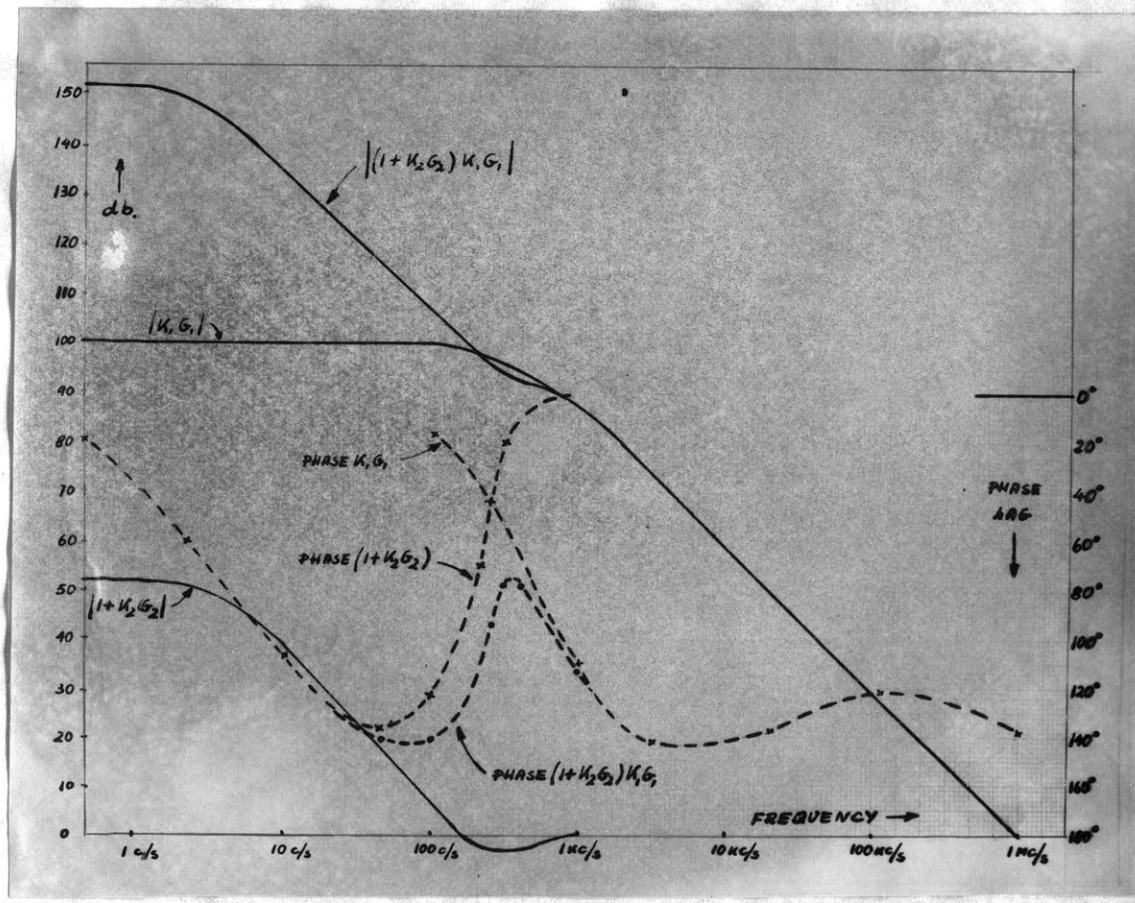


Fig. 35. The attenuation-phase characteristic of the drift-corrected amplifier

with unity for all frequencies higher than 400 c/s, and so the design criteria for the frequency response of the drift-corrector are :-

(i) Gain to be less than unity for all frequencies greater than 400 c/s.

(ii) Phase shift to be less than 180° at all lower frequencies.

The input and the output filters have been designed to meet these requirements. From Fig. 18, Fig. 26, and Fig. 30 which are the attenuation - phase plots of the modulator, the input filter and the output filter respectively, the attenuation-phase characteristic of the complete drift-corrector can be constructed by simple addition of the logarithmic slopes and the phase angles. This is done in Fig. 33 and in the same Figure is plotted the measured attenuation curve of the drift-corrector of Fig. 24. It is seen that there is an excellent agreement between theoretical and experimental results. A general slope of -9 db/oct is present and the unity gain frequency is 200 c/s. For this frequency the phase margin is 40° and is no less than this figure for all lower frequencies.

To calculate $[1 + K_2G_2(jw)]$ the value of $K_2G_2(jw)$ is obtained from Fig. 33 and added to one. The necessary computation is done in Table 2. The attenuation-phase characteristics of $K_2G_2(jw)$ and $[1 + K_2G_2(jw)]$ are plotted in Fig. 34 for comparison.

Table 2.

Frequency c/s	$\lvert K_2G_2(jw)\rvert$ db.	$K_2G_2(jw)$	$1 + K_2G_2(jw)$	$\lvert 1 + K_2G_2(jw)\rvert$ db.
30	+21	$11\angle -140^\circ$	$9.39\angle -136^\circ$	+19.5
100	+9	$2.8\angle -140^\circ$	$2.14\angle -122^\circ$	+6.5
200	0	$1\angle -140^\circ$	$0.68\angle -70^\circ$	-3.5
300	-6	$0.5\angle -140^\circ$	$0.63\angle -25^\circ$	-4
400	-10	$0.32\angle -152^\circ$	$0.72\angle -14^\circ$	-3
600	-15	$0.18\angle -160^\circ$	$0.84\angle -4^\circ$	-1.5

To obtain the attenuation-phase characteristic of the complete drift-corrected amplifier the characteristic of $K_1G_1(jw)$ and that of $[1 + K_2G_2(jw)]$ are combined in Fig. 35. This plot shows that the low frequency gain is 40×10^6 or +152 db. up to 4 c/s, and then falls off at a rate of 9 db/oct. It may be seen, that the phase margin is 40° at the unity gain frequency and is never less than 38° for all lower frequencies; thus the combined amplifier will be stable in all normal computing circuits. The effect of increased phase shift at the lower frequencies is discussed in Section 5.3.

4.9 The switching voltage supply

The preliminary investigations, conducted to determine the performance of the silicon diode modulator for various switching frequencies, indicated that the wave form of the switching voltage is not critical and square-wave or sine-wave can be used. The wave form, however, should remain constant in operation and so the sine-wave was chosen because it is

easier to generate and distribute without distortion.

Since the modulator employs a resonant circuit the frequency of the switching voltage must be kept constant; its effect is shown in Fig. 36. It is seen that an increase in switching frequency will result in a larger unbalance than a reduction in switching frequency, but no adequate explanation has been found. Also, a change in its magnitude will disturb the balance (Fig. 37), and if a large number of drift-correctors are to supplied from the same generator a low source impedance is required. In UTAC a 10 kc/s crystal oscillator is available for timing purposes and this is used to supply a simple A.C. regulator as shown in Fig. 38. In this regulator a portion of the A.C. output is rectified and compared in the feedback path with a constant voltage derived from a reference tube (85A2); any difference voltage is used to control the gain of a pentode (EF86) and thus maintain the output voltage constant in spite of input and load variations. The tuned CIRCUIT which forms the pentode load at 10 kc/s ensures a sinusoidal output free from distortion.

The switching power required in the modulator (Fig. 17) is very nearly

$$\frac{1^2}{100 + 100} = 5 \times 10^{-3} \text{ watts.}$$

The switching power required in the demodulator (Fig.24) is approximately

$$\frac{7^2}{10^4 + 10^4} \cong 2.5 \times 10^{-3} \text{ watts.}$$

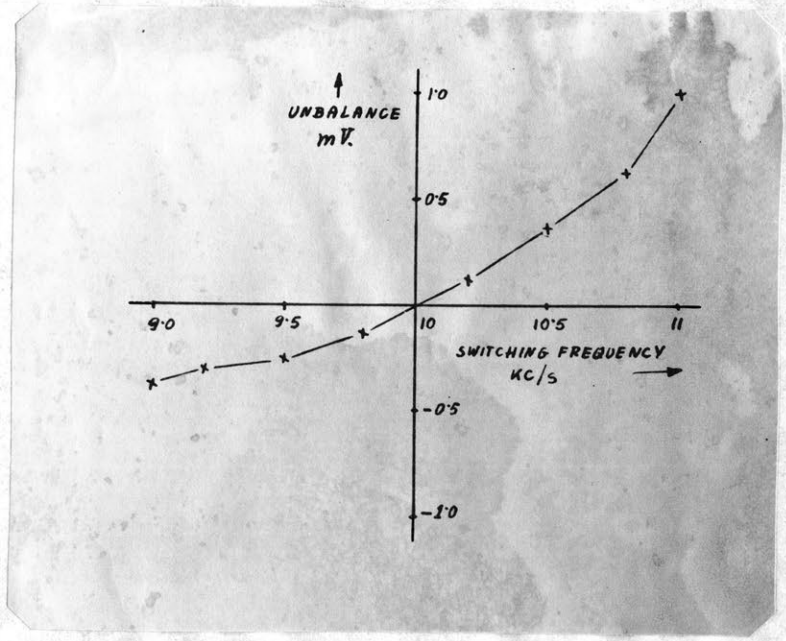


Fig. 36. Typical unbalance caused by change in frequency of the switching voltage.

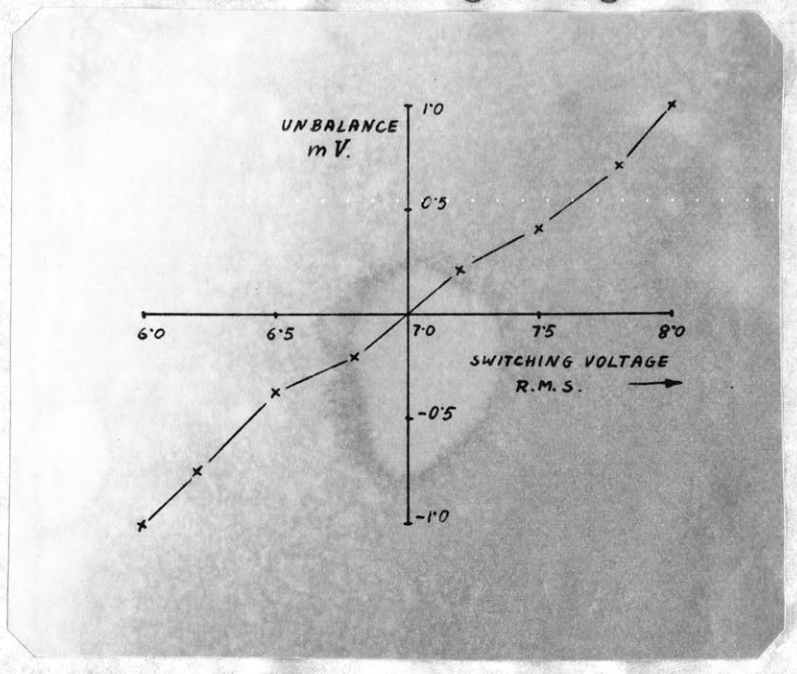


Fig. 37. Typical unbalance caused by change in magnitude of the switching voltage.

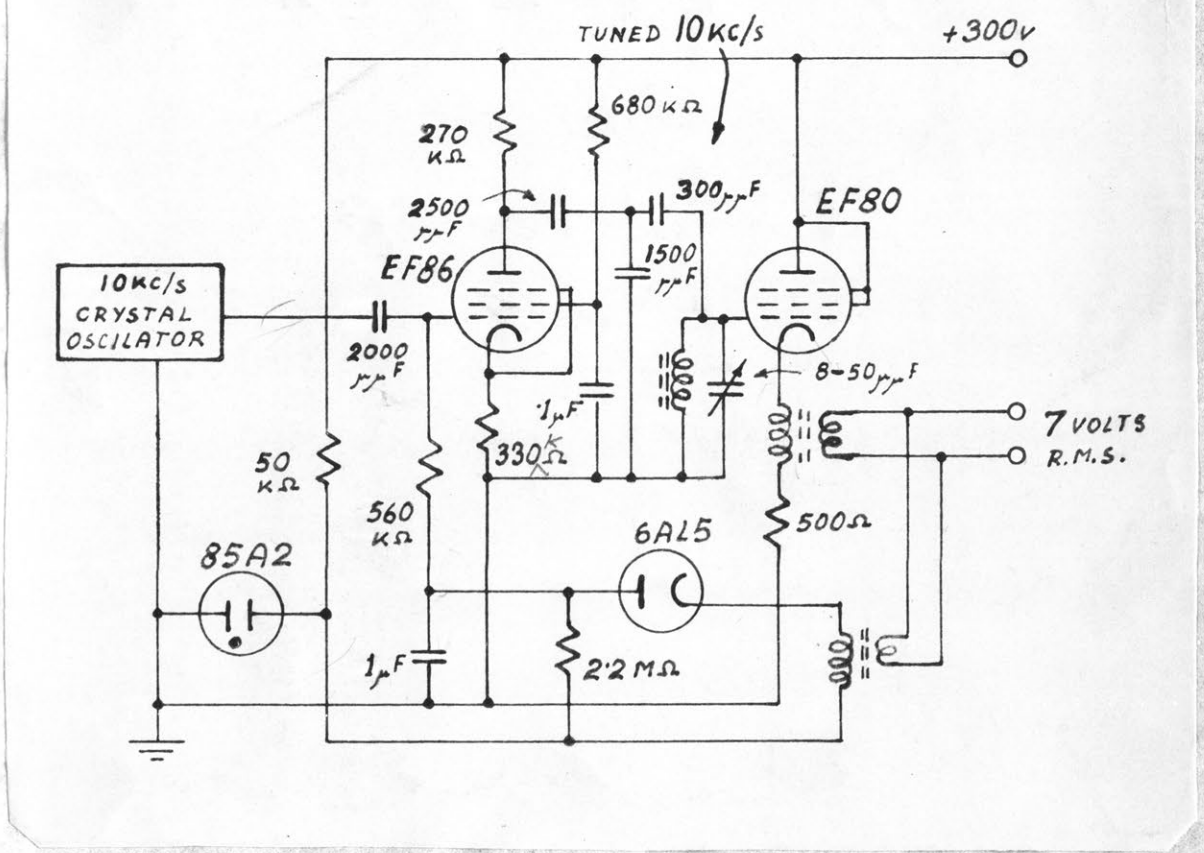


Fig. 38. Circuit diagram of the switching voltage regulator.

Allowing for the additional losses in the transformer and the approximations made the total switching power becomes about 10 milliwatts. Thus, the regulator of Fig. 38 with a power output of 200 mW can supply up to 20 drift-correctors.

The use of a crystal oscillator and a regulator is certainly justified in an analogue computer since, with the addition of a few valves only, all drift which may arise from changes in switching frequency, voltage amplitude or wave-form are completely eliminated.

4.10 Mechanical construction.

The form and shape of the drift-corrector was determined by the space alocated in the amplifier panel of UTAC; a 12 pin plug (Jones plug) is available which provides all the required voltage supplies and interconnections. A general view of the amplifier panel with the drift-corrector in its appropriate position is given in Fig. 41 . A switch at the rear of the panel can connect the drift-corrector to one D.C. amplifier only. The output potentiometer is accessible from the front of the panel and is used as balance control of the drift-corrected amplifier. A wander lead connects the input of the drift-corrector directly with the input of the D.C. amplifier to avoid leakage in the Jones plug.

The drift-corrector consists of a vertical section, which contains the input filter and the modulator, and a horizontal section , which contains the A.C amplifier,

the demodulator, the output filter and the cathode follower. Fig. 39 and Fig. 40 show the location of the various components in the drift-corrector. All components are standard manufactured products and only the switching voltage transformer and the tuning coil were wound to suit our requirements.

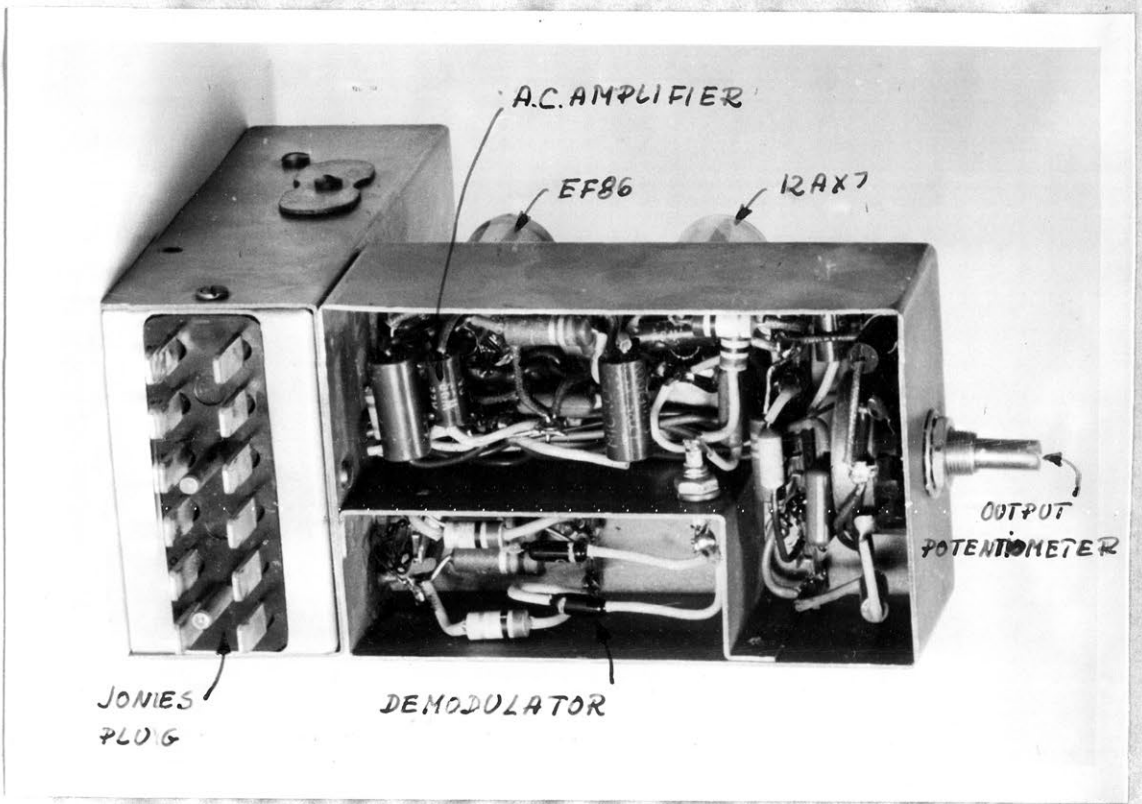


Fig. 39 The horizontal section of the drift-corrector.

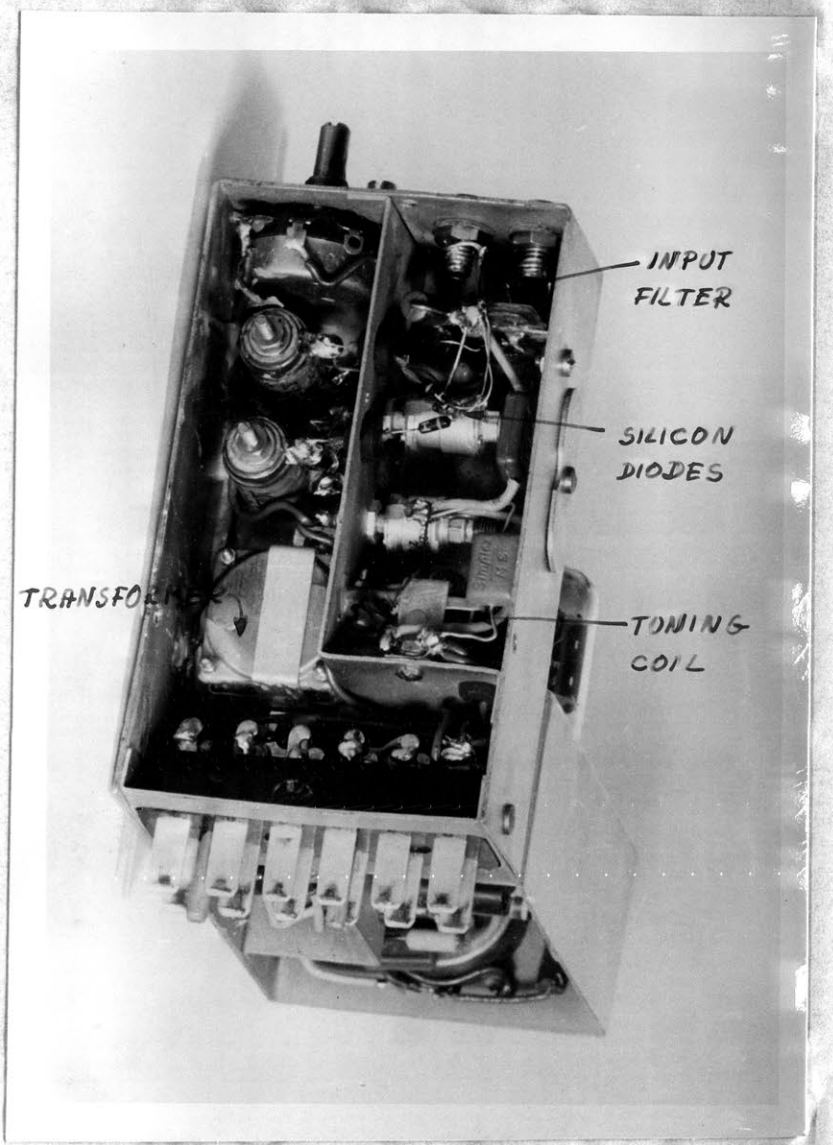


Fig. 40. The vertical section of the drift-corrector.

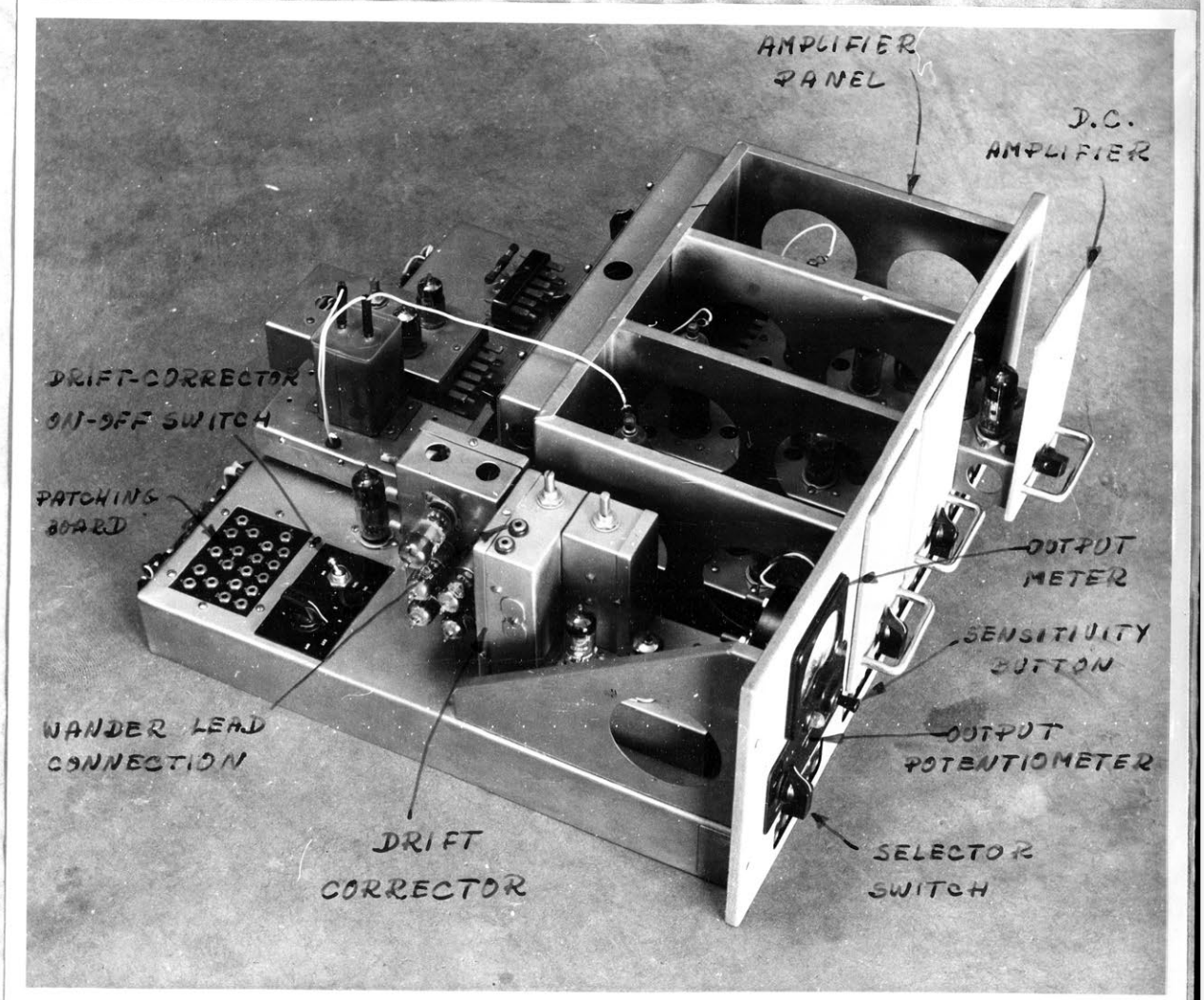


Fig. 41. The amplifier panel with the drift-corrector in its normal position.

5.0 THE DRIFT-CORRECTED AMPLIFIER AS A COMPUTING ELEMENT.

This Section deals with the effects upon computation of the particular drift-corrector described in this thesis.

5.1 Input impedance.

With the drift-corrected amplifier used in a circuit as shown in Fig. 42, for any input voltage 'v' an output voltage 'u' will be established; its size will depend upon the computing components Z_i and Z_f. Also an error voltage 'e' will be set up at the input of the amplifier. For low input frequencies the current which flows into the drift-corrector is $i = \frac{e - e_i}{R_{11}}$; this was derived in Section 4.2 (fig. 27). Also, the same current is $i = \frac{e_i}{2R_o}$ and hence $e_i = i2R_o$ and substitution yields

$$i = \frac{e - i2R_o}{R_{11}} \quad \text{or} \quad i = \frac{e}{R_{11} + 2R_o} \quad \ldots\ldots (18)$$

This shows that the input resistance for all low frequencies is $[R_{11} + 2R_o]$. However, to the value of R_o the resistance of the parallel combination of the diode branches during conduction should be added; this resistance will depend upon the diodes used, the series resistances and the magnitude of the switching voltage applied. For the modulator in question each branch is about 400 kΩ, and the parallel combination 200 kΩ. Then, the total value of the input impedance at low frequencies is

$$R_{11} + 2(R_o + 200\text{x}10^3) = 270\text{x}10^3 + 2\text{x}10^3(680 + 200) \cong 2\ \text{M}\Omega.$$

For all input frequencies higher than 12.5 c/s (the

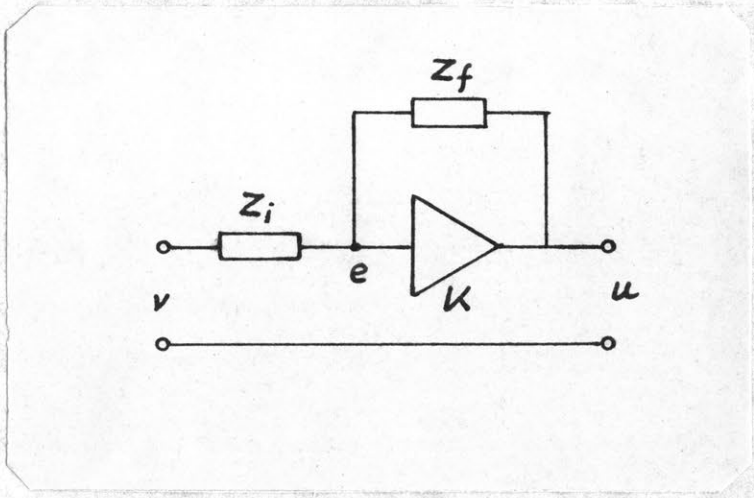


Fig. 42. A drift-corrected amplifier in a normal computing circuit.

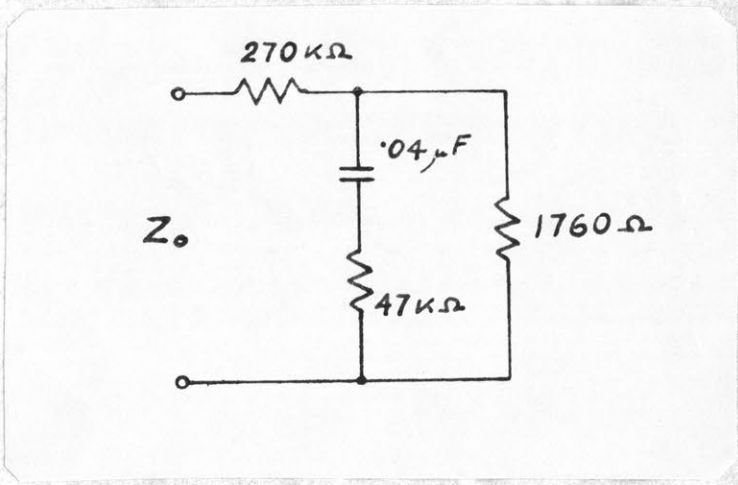


Fig. 43. Circuit equivalent to the drift-corrector input impedance.

the first break frequency of the input filter), the parallel branch of the filter becomes effective and at frequencies well above 84 c/s(the second break frequency of the input filter) the input impedance again becomes resistive, the approximate value being given by $Z_o = (270+47)\ 10^3 = 0.3$ MΩ. It is seen from these considerations that the input impedance at any frequency is given by the equivalent circuit of Fig. 43 and its effect may be investigated, for any computing circuit, using equation (2).

5.2 Effect of modulator drift.

The discussion in this Section is somewhat idealized since, in practice, the precise origin of drift is difficult to locate. However an attempt was made to analize the effect of drift upon the operation of a drift-corrected amplifier. Consider again such an amplifier as in Fig. 42 but with the input lead connected to earth. Then, in the absence of drift, $v = u = 0$. If now a drift voltage appears at the diode junction (Fig. 16) it will give rise to an output voltage 'u' which in turn will set up an error volatge 'e' tending to reduce the effect of the drift. For a sufficiently large amplifier gain it can be seen that the combined amplifier input is now effectively zero. Since drift contains only low frequency components the amplifier gain is simply K and the input filter, which will only slightly attenuate the input voltage, can be neglected.

(i) Drift in the conducting direction. For a modulator drift voltage e_{oc}, the error voltage required to counteract

its effect is given by $e = e_{oc}$. During the conducting period no current will flow through the input resistor R_o because equal voltages exist at either end. During the nonconducting period 'e' will work into a very high impedance and will set up the same voltage 'e' at the diode junction point; thus, a D.C. voltage $e = e_{on}$ will exist at all times and hence 'e' will effectively work into a very high impedance. It also follows that this form of modulator drift has the same effect as that arising in a conventional D.C. amplifier having a large input resistance.

(ii) Drift in the nonconducting direction. During the conducting period the voltage at the diode junction will be very small or zero since e_{oc} is zero and 'e' will be attenuated due to the low resistance of the diode branches: a current will flow through the input resistor R_o. Then, in order that the effective input to the drift-corrector is reduced by the error voltage 'e', the voltage at the diode junction during the nonconducting period must also be equal to the voltage during the conducting period, and again a current will flow of the same magnitude. For a drift voltage e_t in the nonconducting direction only, the error voltage required to counteract its effect will be $e = -e_{tm}$, where e_{tm} is the mean value of e_t during one period. This is the case since e_t is quite independent of 'e'; the rate of change of voltage in equation (15) will not be greatly modified by the introduction of an additional small voltage 'e'.

For such unbalance a mean current will flow of equal magnitude during the conducting and nonconducting periods. The effective input resistance is then the sum of the input filter resistor R_{11}, the modulator resistor R_o and the parallel resistance of the diode branches i.e.

$$(270 + 680 + 200)10^3 = 1.15 \text{ M}\Omega.$$

Normally the situation is more complicated since unbalance will arise in both conducting and nonconducting direction simultaneously and because transit effects should also be considered. The effect of the resonant circuit and its losses have been neglected, but their inclusion in the above reasoning makes the analysis quite complicated. However, the purpose of the above discussion is to merely emphasize the fact that drift in the diode modulator will have the same effect as drift in a normal D.C. amplifier.

Experimentally it would be expected that if e_{oc} existed on its own the drift error term $F(1 + Z_f/Z_i + Z_f/Z_o)$ in equation (2) would reduce to the form

$$E_{on}(1 + Z_f/Z_i)$$

whereas if e_{tm} existed on its own, this term would be

$$E_{tm}\left(1 + \frac{Z_f}{Z_i} + \frac{Z_f}{1.15 \times 10^6}\right)$$

Tests were conducted to verify the above statement and to find the actual value of Z_o, and in fact the drift is intermediate between this two expressions. For example consider an adder with an input computing component $R_i = 0.1$ MΩ and a feedback resistor $R_f = 1$ MΩ (Fig.5a) and so

$$u_1 = f(1 + \frac{R_f}{R_i}) = f(1 + 10) = 11f$$

since $R_i \gg Z_o$ and hence the output is independent of Z_o.

Consider now the same adder with an input resistor $R_i = \infty$ and a feedback resistor $R_f = 10\ M\Omega$. In this case the output is

$$u_2 = f(1 + \frac{R_f}{Z_o}) = f\ (1 + \frac{10^7}{Z_o})$$

From these two measurements a value of Z_o can be evaluated and it was found to be always larger than $2\ M\Omega$.

5.3 The stability of the drift-corrected amplifier in computing circuits.

The transient analysis of a computing amplifier, as presented in Section 2, is done under the assumption that the amplifier gain falls off at a rate of 6 db/oct. Equations (5), (7) and (10) clearly indicate the stability of an adder, integrator or differentiator. However, the gain of the drift-corrected amplifier described in this thesis, falls off at a rate of 9 db/oct (Fig. 35) and it still remains to be seen how this will affect the stability of computing circuits.

The stability of an adder (Fig. 5a) can simply be examined by considering the amplifier frequency response and the response of the feedback circuit. The feedback path is a simple resistive voltage divider; no additional phase shift is introduced and hence the circuit will be stable for all values of R_i and R_f.

In the case of an integrator (Fig. 5b) the feedback path consists of a capacitor followed by a resistor i.e. a simple lead network. Such a lead network will tend to reduce the lagging phase shift of the amplifier and in fact make the circuit more stable.

The feedback path of a differentiator (Fig. 5c) consists of a resistor followed by a capacitor i.e. a lag network and its phase shift added to the phase shift of the amplifier can make the circuit unstable. This is the only case of interest and will be examined in some detail.

As a specific example consider a differentiator with $R_i = 10\ k\Omega$, $C_i = 0.1\mu F$ and $R_f = 1\ M\Omega$. The value of R_i has normally no bearing upon the computation and is usually chosen so that the system is stable for given values of R_f and C_i. The transfer function of the feedback path alone is

$$\frac{E}{U} = \frac{R_i + 1/pC_i}{R_i + R_f + 1/pC_i} = \frac{1 + pC_iR_f}{1 + pC_i(R_i + R_f)}$$

For the above values the attenuation-phase characteristic of this circuit is given in Fig. 44. The inverted attenuation -phase plot of the feedback circuit is superimposed upon the attenuation-phase plot of the drift-corrected amplifier, as shown in Fig. 45, to determine the stability of the closed loop.

Examination of Fig. 45 reveals that the phase margin is positive for all low frequencies, then becomes negative for frequencies between 10c/s and 100c/s, and again positive for higher frequencies. The phase margin is positive when the

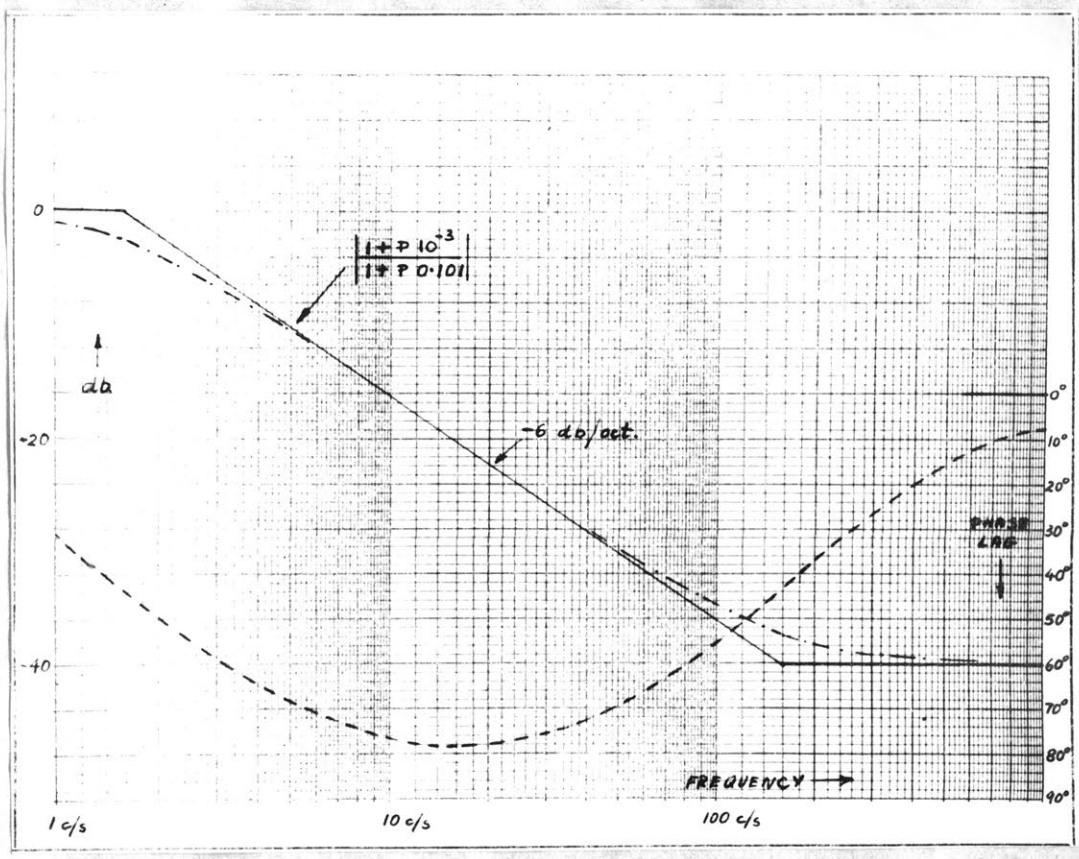


Fig. 44. The attenuation-phase characteristic of the feedback circuit of a differentiator.

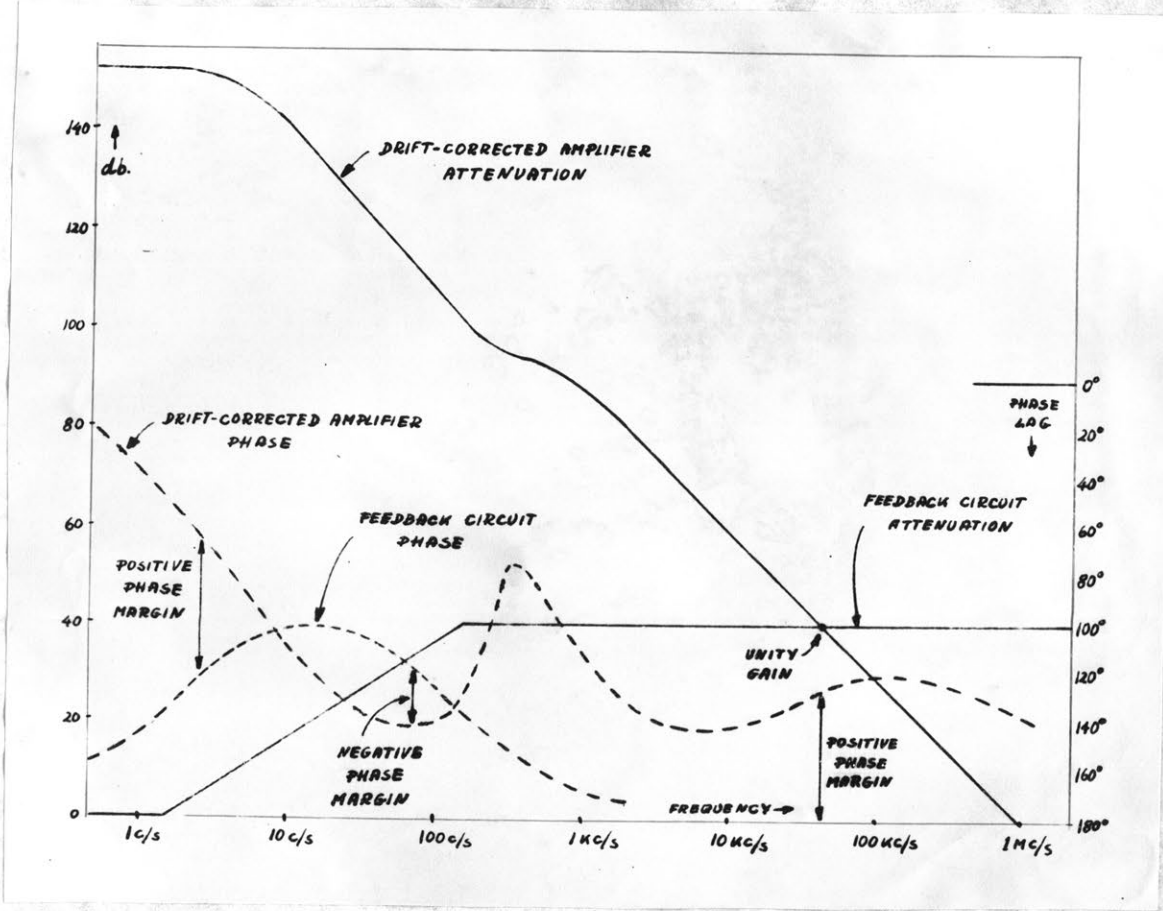


Fig. 45. The attenuation-phase characteristic of a conditionally stable differentiator.

loop gain is unity at 40 kc/s and so the system is conditionally stable. If a drift-corrector is not used the system would be absolute stable since the D.C. amplifier alone has no phase shift below 400 c/s.

This example clearly indicates that the drift-corrected amplifier can be used as differentiator almost equally well as the D.C. amplifier alone, if it is realized that the circuit may be conditionally stable. Tests were conducted to verify this.

5.4 Elimination of grid current

Grid current from the input valve of the D.C. amplifier may cause considerable errors in integrators, but the use of a drift corrector allows insertion of a capacitor in series with the input of the D.C. amplifier and hence eliminates all grid current effects (Fig. 2). A suitable resistor must be connected between the grid of the input valve and ground to pass the grid current. If the resistor is 5 MΩ and the grid current 10^{-8} amp., which is normal for a conventional valve, the capacitor must have a leakage resistance of at least 5,000 MΩ in order to limit the current through the capacitor and the computing components to less than 10^{-11} amp. Polystyrene (plastic) capacitor may have to be used to obtain such high leakage resistance. The UTAC D.C. amplifier has at its input a low grid current valve (ME1400) giving a grid current of 10^{-10} amp. ; thus, a normal mica capacitor is satisfactory if further reduction of grid current effects is desired.

The break frequency of the input capacitor and the grid leak resistor is chosen so that it is at least equal to the unity gain frequency of the drift-corrector. This follows directly from the requirement for stability in a feedback circuit, since the transfer function of the drift-corrected amplifier is now

$$KG(p) = \left[\frac{pT}{1 + pT} + K_2G_2(p)\right] \quad K_1G_1(p)$$

where T is the time constant defined by the series capacitor and the grid leak resistor of the input valve. If $K_2G_2(jw)$ is large compared with $jwT/(1+jwT)$ at the unity gain frequency of the drift-corrector, then for the given frequency response of the D.C. amplifier (Fig. 32) and that of the drift-corrector (Fig. 33) the system would be unstable (see Section 4.8). In the present drift-corrected amplifier it was found that for satisfactory operation the break frequency must be at least 25 c/s i.e. about 3 octaves below tha unity gain frequency of the drift-corrector.

An undesirable feature of this method is the time required to elapse, after a heavy overload, for the amplifier output to return to its reference level, normally zero. If the absolute value of the output voltage of an operational amplifier exceeds a certain permissible level, the amplifier will saturate and can no longer reduce the error voltage at the input of the amplifier. The now large error voltage

will saturate the drift-corrector and charge the input capacitor of the D.C. amplifier.

If the overload is removed there are a number of possible conditions depending upon the type of overload and computing circuit used. In general, however, the rate at which the output will fall is directly proportional to the input time constant T. The time constant of the output filter of the drift-corrector will also have some bearing upon the recovery time and may become critical if too large. The high switching frequency of the silicon diode modulator permits keeping these two time constants small, and this results in considerable improvement compared with the mechanical modulator.

6. PERFORMANCE.

It was shown in Section 2 that errors in the computation due to drift are by far the largest in normal computing circuits and thus, the most important feature of a drift-corrector is its inherent drift. It was also shown that the effect of drift in the diode modulator is the same as that of a conventional D.C. amplifier. Drift can be conveniently measured by using an amplifier as an adder and from equation (2) it follows that for $v = 0$, the output due to drift is

$$u = f\left(1 + \frac{R_f}{R_i} + \frac{R_f}{Z_o}\right) \quad \text{but if} \quad R_i \gg Z_o$$

$$f = \frac{u}{1 + \frac{R_f}{R_i}}$$

All drift measurements were done with $R_f = 1\ M\Omega$ and $R_i = 100k\,\Omega$ and hence $f = u/11$, where 'u' is the output of the amplifier in the absence of an input signal.

The performance of the silicon diode modulator is largely dependent upon the diodes used, but no sharp distinction between 'good' or 'bad' diodes can be made. Thus, no absolute figures can be stated, which would be applicable for all silicon diodes, and an average or a maximum value is more suitable. A total of 8 drift-correctors were built using the best diodes i.e. the diodes with logarithmic characteristics of type HD6007 (see Table 1). The performance

of these drift-correctors was observed over a long period of time when used in conjunction with UTAC high gain D.C. amplifier under normal operating conditions.

The residual A.C. voltage of the modulators and the noise voltage and the D.C. gain of the drift-correctors are listed in Table 3. It is seen that the residual voltage can vary considerably, but the gain and the noise voltage are very nearly constant. The noise level was measured by exactly the same method as the drift in a computing amplifier. A typical noise voltage is shown in Fig. 46 ; it consists mainly of 50 c/s and 100 c/s, the 10 kc/s component being very small.

Table 3

Serial number	2	3	4	5	6	7	8	9	aver age
Residual voltage in mV equivalent input	0.3	0.4	0.4	0.6	0.5	0.1	0.2	0.3	0.35
Noise voltage in mV equivalent input	1.0	0.8	0.7	1.1	1.2	0.7	0.7	1.3	0.94
D.C. gain	400	400	410	390	400	380	400	400	396

The drift of the drift-corrected amplifiers under various conditions is shown in Table 4, where

(i) is the drift voltage after operation of over 4 months ; these values were measured after the computer has reached a steady operating temperature.

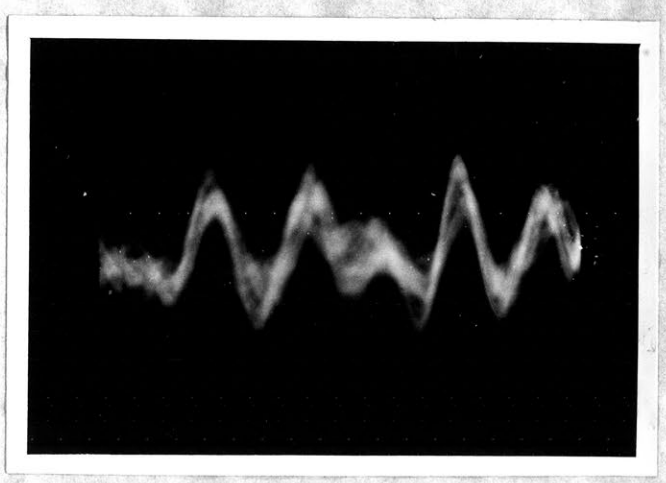


Fig. 46. A typical noise voltage of the drift-corrected amplifier

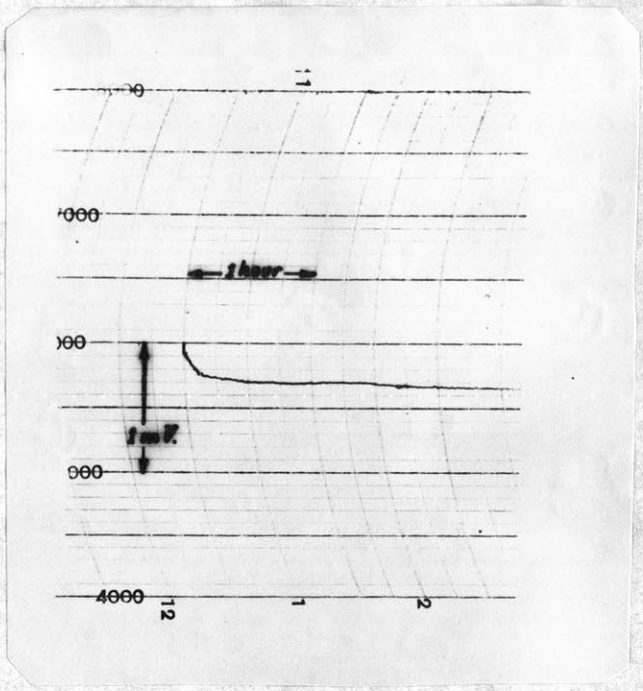


Fig. 47. A typical warming up record of the output of a drift-corrected amplifier in UTAC; the temperature in the modulator compartment has changed by 20°C.

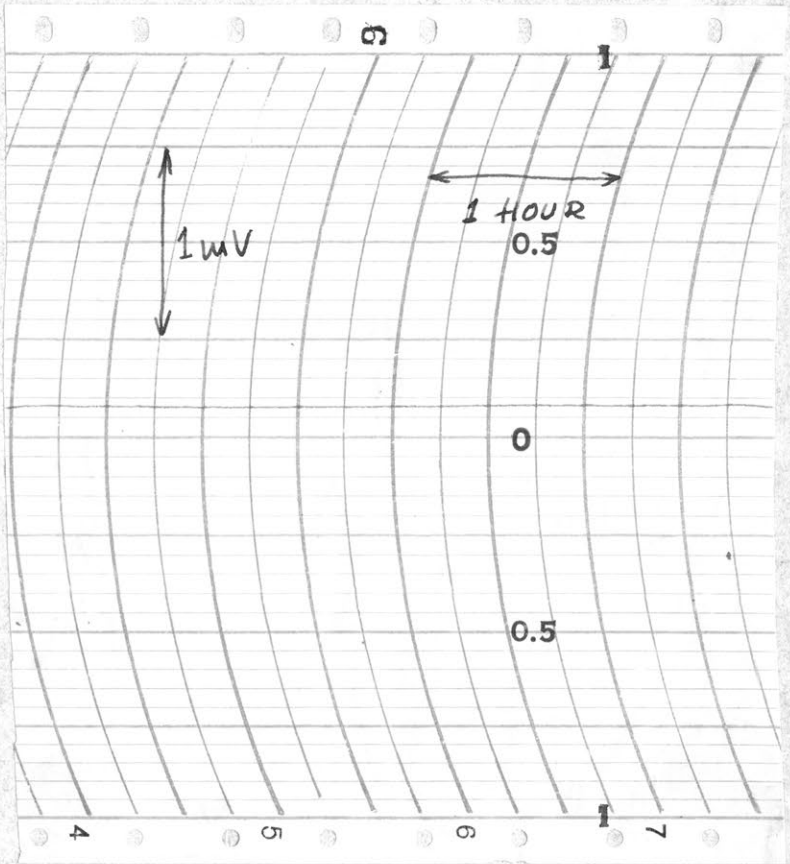


Fig. 48. A record of the output of a drift-corrected amplifier under steady operating conditions.

(ii) is the drift voltage at first switching 'on' after the computer has been completely switched 'off' for at least one day.

(iii) is the drift voltage at first switching 'on' but if the heater power was left 'on' when the rest of the computer was switched 'off'.

(iv) is the temperature coefficient in mV/°C of the drift-corrector on its own, the temperature being measured within the modulator compartment.

Table 4.

Serial number	2	3	4	5	6	7	8	9	average
i	0.2	0.1	0.1	0.1	0.2	0.1	0.15	0.1	0.13
ii	1.2	0.7	0.1	0.2	0.6	0.8	0.6	0.4	0.58
iii	0.1	0.2	0.1	0.1	0.3	0.2	0.2	0.1	0.165
iv	0.06	0.035	0.005	0.01	0.03	0.04	0.03	0.02	0.03

The above Table clearly shows the effect of temperature and it is thought that even better performance could be obtained if some form of temperature control were to be employed. No significant long term drift has been observed, the effect of temperature being completely reversible. A record for a sudden change in temperature is given in Fig. 47 and a record under steady operating conditions in Fig. 48. The last Figure shows that the short term drift is very small and certainly no more than 0.02 mV.

Diodes whose forward characteristics are not logarithmic are difficult to balance and also the drift will be in excess

of that listed in Table 4, but if larger drift can be tolerated they could equally well be used. In some cases the effect of temperature is not completely reversible and this is particularly true if low ~~low~~ back-resistance diodes are used. The switching voltage may also affect the balance; a suddenly applied switching voltage may give rise to a drift similar to that due to a temperature change. Its average effect however, is only about 0.1 mV.

During four months of continuous operation the drift of the cathode follower and that of the demodulator have remained within the desired limits but the A.C. amplifier was not completely satisfactory. Its gain did not change by much more than 10%, but the input valve EF86 exibited a considerable change in input capacitance, in some cases by as much as $10_{\mu\mu}$ Farad. This caused unbalance in the modulator, phase shift of the carrier and general loss of gain: as a result half of the valves EF86 had to be replaced. This was not expected when the amplifier was designed and in the future more attention should be paid to the input stage of the A.C. amplifier.

The more important feature of the drift-corrector are:-

(i) Drift less than 1 mV under all normal operating conditions in UTAC, if logarithmic diodes are used ; a detailed information is given in Table 3.

(ii) Input impedance 2 MΩ up to 12 c/s and is never less than 0.3 MΩ for all higher frequencies.

(iii) D.C. gain is 400 and when working with the UTAC high gain D.C. amplifier a total gain of 40×10^6 is obtained.

(iv) Noise level about 1 mV peak to peak mainly 50 c/s.

(v) Frequency response flat up to 4 c/s and then the gain is falling off at a rate of 9 db/oct.

(vi) The switching frequency is 10 kc/s.

(vii) The switching power required is only 10 milliwatts per drift-corrector.

7. CONCLUSIONS

The work described in this thesis shows that silicon diode modulators can be used successfully in drift-correctors for computing amplifiers. The circuit developed tends to reduce all drift except that arising during the transit period from full conduction to nonconduction; this can be kept small only by using diodes with logarithmic characteristics. Only a limited number of diodes were available but almost certainly there are other types which will exhibit a better logarithmic behaviour than the diodes examined. Also, with improved production methods and a possible preselection by the manufacturer it is believed that the number of diodes unsuitable for the modulator can be reduced to much less than 50%.

The drift of the silicon diode modulator is comparable with that of the mechanical modulator and has the advantages of higher frequency response, low noise level, low switching power requirement and a operational life limited only by the electronic valves. As a result of this develeopment all future D.C. amplifiers in UTAC will be drift-corrected; a drift-corrector and a simple D.C. amplifier will be combined into one unit.

8. ACKNOWLEDGMENTS.

The writer is especially indebted to Professor R.E. Vowels for the constant encouragement of the project described in this thesis. Thanks is also due to Mr. C.P. Gilbert for the cooperation and the facilities provided in the computer laboratory, Mr. R.M. Duffy for the many valuable dicussions, and Mr. R.E. Huey, whose criticism of the manuscrpt was very helpful.

The writer is also grateful to the wokshop staff and in particular Mr. P. Callanan for his willing assistance. All photographs appearing in this thesis are the work of Mr. N. VanVucht from the School of Electrical Engineering.

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16. GILBERT, C.P., GLUCHAROFF, T. and DUFFY, R.N. -"Some Aspects of the Design of D.C. Computing Amplifiers, with particular Reference to the Amplifier used in UTAC". To be published in Proc. I.E.E.

10. APPENDICES

10A. Drift-corrector test procedure.

Equipment required: test rack, cathode-ray oscillograph, AVO 8 multimeter, alignment tool, screwdriver, one wander lead.

Before commencing the testing ensure that:-

(a) The 10 kc/s regulator delivers an undistorted output of 6.7 volts r.m.s. - measured with AVO 8, voltage range 10 V. If a vacuum-tube voltmeter is used the output should be 7 volts.

(b) Connect one lead of the AVO 8 meter to the banana plug terminal designated D.C. (drift-corrector output) on the small patching board at the rear of the amplifier panel (Fig.41). The other lead is to be connected to ground.

(c) Connect a component plug to the first D.C. amplifier (the amplifier to be drift-corrected) with a forward gain of 10 (R_f= 1 MΩ and R_1 = 0.1 MΩ). Make sure that the test rack and the amplifier are in good order ; balance the amplifier for zero output. Switch H.T. off.

(d) Put the drift-corrector switch off and also switch off the 10 kc/s supply at the regulator.

The testing should be done in the following order :-

1. Insert only the valve 12AX7 into the appropriate socket in the drift-corrector unit to be tested and plug it into the amplifier panel. Connect the C.R.O. lead to the monitoring terminal of the drift-corrector. Plug one end of the wander lead into the input terminal of the drift-corrector and clip the other end to the chassis.

2. Switch H.T. on. Using a screwdriver rotate the output potentiometer of the drift-corrector and observe the AVO 8; it must indicate between ± 1 volt. Adjust for zero output.

3. Switch the 10 kc/s supply on. The reading of the AVO 8 should not change by more than 0.2 volts and the noise level as indicated on the C.R.O. should not exceed 200 mV. If these figures are exceeded the demodulator circuit should be examined and possibly the germanium diodes replaced.

4. Switch H.T. off. Switch 10 kc/s off. Insert the valve EF86 and after some warming up, switch H.T. on. Disconnect the wander lead from the chassis and connect it to the regulator terminal marked 20 mV peak to peak. Using the alignment tool vary the tuning capacitor in the drift-corrector and observe the output on the C.R.O. A broad resonance will be obtained and the C.R.O. should indicate about 4 volts peak to peak.

5. Connect the wander lead to the chassis. Switch 10 kc/s supply on. Using the alignment tool and a screwdriver vary the 3 balancing controls of the modulator and observe the C.R.O. Balance should be obtained with a A.C. output voltage of much less than 0.5 volts p.p.

6. Solder two silicon diodes into their appropriate position. Vary the three balancing controls and by trial and error obtain a balance such that:-

(i) the voltage indicated on the C.R.O. does not exceed 1 volt p.p.

(ii) disconnecting and connecting the wander lead to the chassis does not affect the A.C. balance i.e. no change in output takes place as indicated on the C.R.O. and the AVO 8 meter.

Balance should be obtained with a residual voltage as small as possible and a reversal of diode position may be advisable. Check that by pressing the selevtivity button, on the front of the amplifier panel (Selector in D.C. position), a deflection is obtained on the panel meter not exceeding 10 (5 divisions). Put the cover on and rebalance.

7. Connect the wander lead to the terminal under the multi-position switch on the test rack marked input(this provides a calibrated D.C? voltage to the input of the drift-corrector). Put the multi-position switch in position +1 mV or -1 mV. Press the push-button marked input (mounted on the test rack) and observe its effect on the C.R.O. and the AVO 8 meter. The C.R.O. should indicate an output of about 1.5 volts p.p. and the AVO 8 should deflect o.4 volts in such a direction as to have the opposite polarity of the input signal. If this is not the case reverse the 10 kc/s supply leads to the demodulator.

8. Repeat (4) with the silicon diodes in position. Repeat (6) and then (7). The balancing is completed.

9. Switch H.T. off. Connect the wander lead to the input of the D.C. amplifier and put the drift-corrector switch on. Switch H.T. on; the drift-corrector is now working with thw D.C. amplifier.

10. Put the selector switch in position 1 (output of the drift-corrected amplifier). Press the sensitivity button

and using a screwdriver vary the output potentiometer of the drift-corrector until zero output is obtained. Vary the balancing control of the D.C. amplifier and see that the output does not change by more than 2 (one division on the output meter). Put the selector switch in position D.C. (monitoring terminal of the drift-corrector) and press the sensitivity button; a deflection not larger than 10 should be obtained.

11. Connect the C.R.O. to the output of the drift-corrected amplifier and see that the noise level is about 10 mV p.p.

12. It is advisable to leave the drift-corrector switched on for at least one hour and check the balance again.

10B. Summary of papers submitted to the Institution of Electrical Engineers London for publication.

1. GILBERT, C.P., DUFFY, R.N. and GLUCHAROFF, T. - " The N.S.W. University of Technology Analogue Computer (UTAC)".

Summary.

This paper is a general description of UTAC, a 'real time' electronic analogue computer designed for University use. At present UTAC contains 24 amplifiers.

Flexibility of operation is achived by allowing any amplifier to perform any operation, either linear or nonlinear, and this is facilitated by the use of plug-in computing components. A method of amplifier control which allows all normal modes of operation and employs only one relay per amplifier is described.

The flexibility is enhanced by allowing a timing unit, or variable in the computation to operate the control relays.

A simple system of overall calibration making use of comparative measurements of voltages and time ensures that the accuracy is as high as possible for this type of computer.

A new type of generator for producing voltages which are arbitrary functions of time is also described.

2. GILBERT, C.P., GLUCHAROFF, T. and DUFFY, R.N. - "Some Aspects of the Design of D.C. Computing Amplifiers with particular Reference to the Amplifier Used in UTAC.

Summary

This paper deals with the main considerations involved in the design of D.C. amplifiers for use in 'real time' analogue computers: the discussion applies to general purpose amplifiers, and unless otherwise stated it is assumed that drift-correctors are not employed, although most of the conclusions would still be valid.

It is shown that the limiting factor on the accuracy of a computing amplifier are its gain and frequency response, and a method is suggested which allows the stability of normal computing circuits to be investigated conveniently.

There are also a number of practical features which affect the performance of computing amplifiers. Of these, drift is by far the most important, and a new desgn of input stage which has proved successful is put forward. The

UTAC amplifier, which employs this input stage, is described in some detail, the effect upon performance of wide tolerance, unselected components being examined.

3. GLUCHAROFF, T., GILBERT, C.P. - "The Use of Silicon Diodes in D.C. Modulators and their Application to Drift Correctors for Computing Amplifiers".

Summary

The basic computing element of an analogue computer is the high gain D.C. amplifier, but in order to overcome its inherent drift some form of auxiliary drift correcting amplifier is frequently used.

This paper describes a silicon diode modulator for use in such drift correctors, and shows that the zero stability which can be achieved is comparable with that given by the conventional relay modulator. It is shown that the use of the diode circuit results in a number of improvements in the overall drift corrector performance, such as higher frequency response and practically unlimited life; the design of such a drift corrector for use with a given D.C. amplifier is described in detail, and the resulting performance is assessed.