Digital Harmonic-Cancelling Sinusoidal Signal Synthesis

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# Digital Harmonic-Cancelling Sinusoidal Signal Synthesis

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Sinusoidal signal synthesizers are essential modules in a variety of electronic applications, such as communication systems, and calibration and verification of analog/mixed-signal integrated circuits (ICs). For decades, researchers have developed different types of sine-wave synthesizers. However, improving the balance between spectral purity, area and power costs, and programmability of sine-wave synthesizers remains an intriguing research problem. The first publication of a digital harmonic-cancelling sine-wave synthesizer (DHSS), which is the subject of this thesis, was in 1969. However, due to the overshadowing popularity of direct digital frequency synthesizers (DDFSs), the development of DHSSs had been stalled until a revival in recent years. DHSSs offer a better compromise between spectral purity, and area and power costs, compared to DDFSs. On the other hand, DHSSs lag behind DDFSs in terms of programmability. We envisage a future in which DHSSs replace DDFSs in electronic applications where area and power cost efficiency is the primary requirement. With this vision in mind, I worked in this research towards improving the programmability as well as the area and power cost effectiveness of DHSSs. In doing so, this research has resulted in three main contributions to the DHSS technology. The first contribution is a DHSS hardware architecture, which supports phase programmability. The second contribution is a method of designing DHSSs, such that the resulting DHSSs break the 6 dB/bit rule, which governs the compromise between spectral purity, and area and power costs in DDFSs. The third contribution is a dynamic element matching (DEM) technique to reduce the effect of mismatch while preserving the area and power cost efficiency of DHSSs. The theoretical proposals made in this thesis have been verified by implementing and testing two DHSS IC prototypes. One prototype was designed to be phase programmable, and it has been used to demonstrate the usability of DHSSs in communication applications. The other prototype used the proposed DEM technique, which improved the figure of merit of the DHSS by $40\ \%$. Both DHSS prototypes utilized the design method presented in this thesis, and they have broken the 6 dB/bit rule by performing at 8 dB/bit and 10 dB/bit.



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# Abstract

Sinusoidal signal synthesizers are essential modules in a variety of electronic applications, such as communication systems, calibration and verification of analog/mixed-signal integrated circuits (ICs), and lab-on-chip medical/material analyzers. For several decades, researchers have worked on developing different types of sine-wave synthesizers. However, improving the balance between spectral purity, area cost, power consumption, and programmability of sine-wave synthesizers remains an intriguing research problem. The subject of this thesis is digital harmonic-cancelling sine-wave synthesizers (DHSSs). The first publication of a DHSS was in 1969. However, due to the overshadowing popularity of direct digital frequency synthesizers (DDFSs), the development of DHSSs had been stalled until a revival in recent years. DHSSs offer a better compromise between spectral purity, and area and power costs, compared to DDFSs. On the other hand, DHSSs lag behind DDFSs in terms of programmability. We envisage a future in which DHSSs replace DDFSs in applications where area and power cost efficiency is the primary requirement. With this vision in mind, we have worked in this research towards improving the programmability as well as the area and power cost effectiveness of DHSSs. In doing so, this research has resulted in three main contributions to the DHSS technology. The first contribution is a DHSS hardware architecture, which supports phase programmability. Phase programmability opens the door for DHSSs to be used in phase-shift keying (PSK) communication applications. The second contribution is a method of designing DHSSs, such that the resulting DHSSs break the 6 dB/bit rule. The 6 dB/bit rule governs the compromise between spectral purity, and area and power costs in DDFSs. Furthermore, previous DHSS related work have not explored the design space of DHSSs enough to realize that DHSSs could break the 6 dB/bit rule. The third contribution is a dynamic element matching (DEM) technique to reduce the effect of mismatch while preserving the area and power cost efficiency of DHSSs. The theoretical proposals made in this thesis have been verified by implementing and testing two DHSS IC prototypes. One prototype was designed to be phase programmable, and it has been used to demonstrate the usability of DHSSs as PSK modulators. The other prototype utilized the proposed DEM technique. Activating DEM improved the figure of merit of the DHSS by 40 %, compared to the same DHSS with DEM deactivated. Both DHSS prototypes used the design method presented in this thesis, and they have broken the 6 dB/bit rule by performing at 8 dB/bit and 10 dB/bit.

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# Abbreviations

**AMS** Analog/mixed-signal

**BIST** Built in self testing

**DAC** Digital-to-analog converter

**DAE** Differential amplitude error

**DDFS** Direct digital frequency synthesizer

**DEM** Dynamic element matching

**DHSS** Digital harmonic-cancelling sine-wave synthesizer

**DPG** Digital pattern generator

**DUT** Device under test

**EVM** Error vector magnitude

**FIR** Finite impulse response

**HC-DAC** Harmonic-cancelling digital-to-analog converter

**IA** Instrumentation amplifier

**IAE** Integral amplitude error

**IC** Integrated circuit

**IF** Intermediate frequency

**ILA** Individual level averaging

**IQ** Quadrature

**LF** Linear fit

**LPF** Low-pass filter

**LTI** Linear time-invariant

**PA** Phase accumulator

**PAC** Phase-to-amplitude converter

**PCB** Printed circuit board

**PF** Pareto front

**PLL** Phase-locked loop

**PSK** Phase-shift keying

**RF** Radio frequency

**ROM** Read-only memory

**SDR** Signal-to-distortion ratio

**SDR**$_{90\%}$ SDR with 90 % yield

**SFDR** Spurious free dynamic range

**SIN-DAC** Sinusoidal digital-to-analog converter

**SPI** Serial peripheral interface

**SQNR** Signal-to-quantization-noise ratio

**SoC** System-on-chip

**Tx** Transmitter

**VCO** Voltage-controlled oscillator

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# Part I

# The Past, the Present, and the Forgotten

# Chapter 1

# Introduction

## 1.1 Sinusoidal Signal Synthesizers

Why are sinusoidal signals the most fundamental class of signals used in electronic engineering? Is it because we can decompose a given signal to a linear combination of sinusoidal signals using the Fourier transform? Yes, however, that is only part of the reason. If a sinusoidal signal is provided as the input to a linear time-invariant (LTI) system, the output is also a sinusoidal signal of the same frequency and possibly different amplitude and phase, compared to the input signal. In other words, sinusoidal signals are eigenfunctions of LTI systems. Electronic systems are often modelled as LTI systems. Consequently, when analyzing the response of such an electronic system to an arbitrary input signal, we decompose the input signal to a linear combination of sinusoidal signals using the Fourier transform to simplify the analysis. Furthermore, when an electronic system is nonlinear, which most practical circuits are, or time-variant, such as a mixer, providing sinusoidal input signals to the system makes it easier to analyze the nonlinear distortion and frequency translational characteristics of the system.

Figure 1.1: A generic sinusoidal signal synthesizer

Sinusoidal signals are utilized in a wide variety of electronic engineering applications, such as communication systems [SK04], calibration, testing, and evaluation of analog/mixed-signal (AMS) electronic systems [ESS10, SBT+10, BLVR14, SSS15], and lab-on-chip spectral analyzers [RLYM09]. The empirical influence of sinusoidal signals in the field of electronics makes sinusoidal signal synthesizers one of the key components in a variety of electronic systems.

A generic sine-wave signal synthesizer is illustrated in Fig. 1.1. As shown, a generic sine-wave synthesizer may take inputs which define the amplitude, frequency, and phase of the sine-wave signal produced at the output. A digital sine-wave synthesizer will also receive a reference clock signal.

An ideal sine-wave synthesizer would produce a spectrally pure sine-wave signal. However, a sine-wave signal generated by a practical sine-wave synthesizer circuit would contain spectral impurities, which are called distortions, as illustrated in Fig. 1.2. A key performance demand placed on sine-wave synthesizers is to compose sine-wave signals with low signal-to-distortion power ratio (SDR). Fast programmability, low area cost, low power consumption, wide output frequency bandwidth, and low output phase-noise are other performance requirements of sine-wave synthesizers. Here, fast programmability means having short response time when pro-

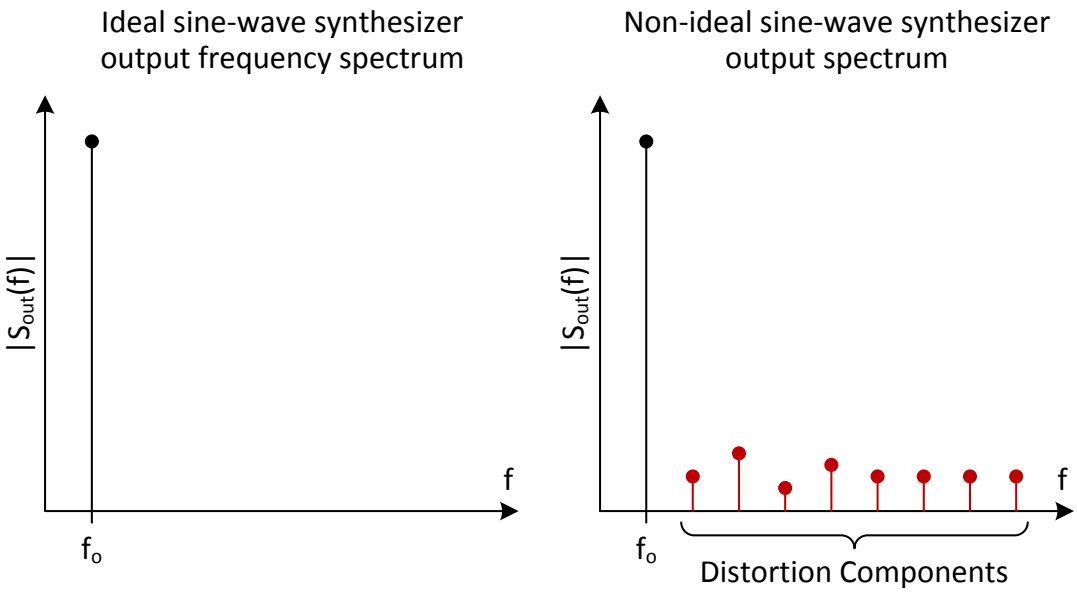


Figure 1.2: Frequency spectrum of the output signal of an ideal sine-wave synthesizer and a non-ideal sine-wave synthesizer

gramming the amplitude, frequency, and phase of the output signal. The specific performance demands placed on a sine-wave signal synthesizer varies from one application to another.

Two key application areas for sine-wave synthesizers, which this thesis will focus on, are communication systems, and built-in-self-testing (BIST) of AMS integrated circuits. All electronic communication systems currently in use, both wired and wireless, rely on encoding information in the phase, frequency, and amplitude of a sine-wave carrier signal. Consequently, sine-wave signal synthesizers are essential components in electronic communication systems, from the chip-set in our mobile phones which connects us to the internet, to the chip-set in a spacecraft which enables images to be sent to earth from deep space. For a sine-wave synthesizer used in a communication application, the key performance criteria are to have low phase noise, fast programmability, low distortion, low area cost, and low power consumption.

BIST is a mechanism for testing chips, where the equipment required to test a chip are built-in to the system-on-chip itself [HSK93, KKCL95]. Most AMS integrated circuits rely on expensive external equipment for testing. The advantages of increasing AMS BIST coverage are the reduction in the production cost related to testing and the simplified test procedure. When implementing a BIST scheme for an AMS chip, one of the key on-chip test equipment required is a sine-wave signal synthesizer. A sine-wave synthesizer used in a BIST application is required to have low output distortion and low area cost.

## 1.2 Forgotten History

Early sine-wave signal synthesizers were realized as analog sine-wave synthesizers or in other words analog oscillator circuits. Then, around four and a half decades ago, digital sine-wave synthesizers started becoming popular. Among different classes of digital sine-wave synthesizers, direct digital frequency synthesizers (DDFSs) have been the overwhelmingly popular category. In terms of programmability, DDFSs have held a distinct advantage against analog sine-wave synthesizers. Furthermore, as semiconductor technologies scaled down, the area and power costs of DDFSs have improved compared to analog sine-wave synthesizers.

Two years prior to the first publication of a DDFS [TRG71], digital harmonic-cancelling sine-wave synthesizers (DHSSs) were introduced in [Dav69]. However, possibly due to the overshadowing popularity of DDFSs, DHSSs became a forgotten piece of sine-wave synthesizer history for nearly four decades. In recent years there has been a revitalization of DHSSs with the publication of [ESS10, SBT+10, BLVR14, SSS15].

DHSSs use a signal synthesis technique that is tailor made for sine-wave signal generation. Therefore, DHSSs are capable of producing sine-wave signals with low distortion, with higher area and power cost efficiency, compared to DDFSs [ESS10, SSS15]. However, when it comes to fast programmability, DHSSs are considerably behind DDFSs. We envisage a future in which DHSSs replace DDFSs in electronic applications where area and power cost efficiency is the primary requirement. Realizing our vision requires research and development work to make DHSSs more programmable and to further improve the area and power cost efficiency of DHSSs.

## 1.3 Scope of the Thesis

The scope of this thesis is to reduce the programmability gap between DHSSs and DDFSs and to widen the area and power cost efficiency advantage DHSSs hold over DDFSs. More specifically, this thesis aims to address the following research sub-topics.

1. Proposing a hardware architecture for DHSSs that improves programmability
2. Studying the effect amplitude resolution, mismatch, and timing errors of the summing circuit (please see Chapter 2 for more details on the summing circuit) have on the spectral purity of the output sine-wave signal
3. Using the understanding of the summing circuit gained from (2) to improve the area and power cost efficiency of DHSSs
4. Proposing an area and power cost efficient dynamic element matching algorithm to manage the effect of mismatch errors in the summing circuit
5. Designing, implementing, and testing integrated circuit (IC) prototypes of DHSSs to practically verify the theoretical outcomes of (1), (2), (3), and (4).

## 1.4 Contributions Made to the DHSS Technology

While working towards the goals outlined above, this research has made the following contributions to the digital harmonic-cancelling sine-wave synthesis technology.

1. Proposal of a hardware architecture for DHSSs, which supports fast programmability of the phase of the output signal. A phase programmable DHSS can perform phase-shift keying (PSK) in communication applications. This thesis demonstrates the usage of a DHSS as both a baseband digital-to-analog converter (DAC) and an intermediate frequency polar modulator, for PSK communication applications, using a phase-programmable DHSS IC prototype.

2. Showing both theoretically and practically that with careful design the summing circuit in a DHSS can perform with better area and power cost efficiency than a regular DAC. The relationship between amplitude resolution and spectral purity in a conventional DAC is estimated using the "6 dB/bit rule". Theoretical findings in this research show that the summing circuit in a DHSS can be designed to perform significantly better than 6 dB/bit. Furthermore, this thesis presents test results from a DHSS prototype IC, which demonstrates 10 dB/bit performance.

3. Proposal of a partial dynamic element matching (DEM) technique, which combats mismatch errors in the summing circuit, while preserving the area and power cost efficiency of DHSSs. Test results presented in this thesis from a DHSS IC prototype show that the proposed partial DEM technique increased the figure-of-merit (taking into account output frequency, spectral purity, power, and area) of the DHSS by 40%

The research contributions summarized above have led to the following publications,

parts of which have been used in this thesis.

[1] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "A simple digital architecture for a harmonic-cancelling sine-wave synthesizer," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* 2014, pp. 2113–2116.

[2] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Design of a digital harmonic-cancelling sine-wave synthesizer with 100 MHz output frequency, 43.5 dB SFDR, and 2.26 mW power," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* 2015, pp. 3052–3055.

[3] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "The effect of amplitude resolution and mismatch on a digital-to-analog converter used for digital harmonic-cancelling sine-wave synthesis," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* 2016, pp. 2018–2021.

[4] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Partial dynamic element matching technique for digital-to-analog converters used for digital harmonic-cancelling sine-wave synthesis," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 2, pp. 296–309, 2017.

## 1.5 Anatomy of the Thesis

The rest of this thesis is structured as follows. Chapter 2 provides a review of the existing literature related to this work. In Chapter 3 we go into the theoretical details of harmonic-cancelling sine-wave synthesis, introduce the DHSS hardware architecture used in this project, and outline the applications targeted by the DHSSs developed in this research. The design of the digital pattern generator, which facilitates

phase programming in the proposed DHSS architecture, is discussed in Chapter 4. In Chapter 5 we study the effect of amplitude resolution, mismatch, and timing errors of the harmonic-cancelling digital-to-analog converter (summing circuit), on the spectral purity of the DHSS output signal. Then, in Chapter 6 we propose a partial DEM technique to reduce the effect of mismatch errors in HC-DACs. Chapter 7 discusses the development of a test-chip with two DHSS prototypes to verify the theoretical findings of this research, while Chapter 8 presents test results from the two DHSS prototype circuits. Finally, in Chapter 9 we conclude the thesis and propose potential avenues for exploration in future research work.

# Chapter 2

# Literature Review

*"If I have seen further, it is by standing upon the shoulders of giants"*

— Issac Newton

## 2.1 Overview

This chapter explores the existing literature on the topic of sinusoidal signal synthesizers. The classic sinusoidal signal synthesizers were based on analog oscillator circuits. As digital electronic circuits became popular, digital sine-wave synthesizers gained prominence. Chief among such digital sine-wave synthesizers was the direct digital frequency synthesizer. In 1969, a couple of years before the invention of the DDFS, digital harmonic-cancelling sine-wave synthesis was invented as a digital technique for sine-wave synthesis, which forms the basis of this research. The remaining sections survey these different types of sine-wave synthesizers as follows: Section 2.2 discusses analog sine-wave synthesizers, Section 2.3 looks into digital sine-wave synthesizers, and Section 2.4 explores digital harmonic-cancelling sine-wave synthesizers. Finally, Section 2.5 summarizes the literature review.

## 2.2 Analog Sine-Wave Synthesis

### 2.2.1 Theoretical Background

An analog sine-wave synthesizer is an oscillator circuit that is aimed at synthesizing sinusoidal signals, rather than a spectrally impure signal, such as square-waves or triangular-waves. In general, an analog sinusoidal oscillator circuit consists of an amplifier stage, a positive feedback network, a gain limiter, a frequency selective network, and an output filter stage. To simplify the theoretical analysis, let us consider a basic oscillator, where the amplifier provides gain limitation, and the feedback network performs frequency selection. Figure 2.1 illustrates a block diagram of such a basic oscillator. Note that $S_{\text{in}}(t)$ is drawn only to make sense of the closed-loop transfer function derived later and that the oscillator does not have an input signal.

The closed-loop transfer function, $G_{\text{CL}}(s)$, of the oscillator circuit shown in Fig. 2.1 can be expressed as folows:

$$G_{\text{CL}}(s) = \frac{A(s)}{1 - H(s)A(s)} \tag{2.1}$$

An oscillator produces an output signal without an input signal. Such a situation is possible if the denominator of $G_{\text{CL}}(s)$ reaches zero. Therefore, for the closed-loop

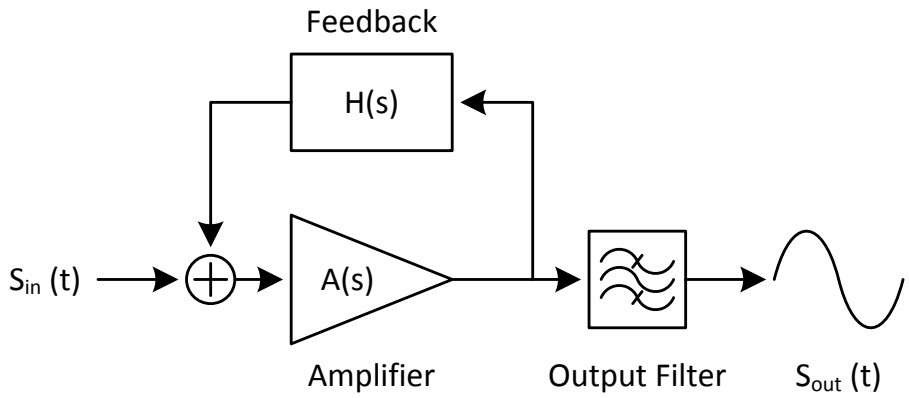


Figure 2.1: Block diagram of a basic analog oscillator

circuit to oscillate at $\omega_0$, the following conditions need to be satisfied.

$$|H(j\omega_0)A(j\omega_0)| = 1 \tag{2.2}$$

$$\arg\left[H(j\omega_0)A(j\omega_0)\right] = 0 \tag{2.3}$$

The conditions in Eq. 2.2 and Eq. 2.3 are called the Barkhausen criteria for oscillation [Col04, SS04, Gon07]. The Barkhausen criteria can be rephrased by stating that for the closed-loop system to oscillate at $\omega_0$, two poles of $G_{\mathrm{CL}}(s)$ must fall at $\pm j\omega_0$. However, in practice, the poles should be in the right half of the complex $s$ plane. Poles on the right half plane make the system unstable. In such an unstable system, noise generated when switching the power on results in an exponentially growing output signal. The output signal will continue to increase in amplitude until being limited by gain compression in the amplifier or by a separate gain limiter. When the gain is limited to the point where the Barkhausen criterion is satisfied, the system will settle to provide a stable oscillating signal.

### 2.2.2 Issues with Analog Sine-Wave Synthesizers

#### Harmonic Distortion

The output signal of an empirical oscillator circuit contains harmonic frequency content in addition to the desired fundamental frequency. Such harmonics originate through nonlinearities in the closed-loop system. In an oscillator aimed to be used as a sine-wave synthesizer, these harmonic distortions must be attenuated.

As mentioned earlier, nonlinearities or saturation of the amplifier can be utilized for gain limiting in an oscillator [Gon07]. However, the use of amplifier saturation causes clipping. Consequently, the output sinusoidal signal is distorted by harmonics. Thus, high Q band-pass feedback circuits and high order output filter circuits

are required to attenuate the harmonic content in the output signal. Such high Q, high order frequency selective circuits increase the hardware complexity, cost area and power, and they might also be incompatible with semiconductor integration.

### Phase Noise and Frequency Stability

Phase noise is fluctuations in output signal phase that occur in an oscillator [Raz96, HL98]. Such variations in output signal phase can be caused due to thermal noise, shot noise, and flicker noise generated in the oscillator circuit devices. Fluctuations in output signal phase cause changes in output signal frequency, as frequency is the derivative of phase. Therefore, phase noise can also be considered as a short-term frequency instability.

To reduce phase noise and to increase frequency stability, high Q resonant circuits (e.g. LC tank) can be used in the oscillator's frequency selective feedback network [Col04, Gon07]. The Q factors of on-chip LC resonators are typically low [Lee04]. Also, note that an on-chip sine-wave signal synthesizer, whether it is used in a built-in-self-test application, a communication application, or otherwise, is only one block in a larger system-on-chip (SoC). Thus, allocating expensive chip area for a dedicated high-Q LC tank in the on-chip sine-wave synthesizer will not be possible in most cases. Increasing supply current can also reduce phase noise in oscillators [Raz96, HL98]. However, increasing supply current also swells the power consumption.

Embedding the oscillator in a phase-locked loop (PLL) is another method of improving frequency stability. A PLL makes a voltage-controlled oscillator (VCO) track the phase of a crystal oscillator running at a stable, fixed, and much lower frequency [Gup75, LC81, HH96]. However, adding a PLL increases the design complexity, area cost, and power cost of a sine-wave synthesizer.

**Programmability**

Programmability or tunability of amplitude, frequency, and phase of the output signal is a desired characteristic of sine-wave signal synthesizers. Analog oscillators have limited tuning capability in general [TI113]. Even with programmable oscillators, response time tends to be slow [TI113]. In programmability lies the most significant disadvantage of analog oscillators compared to their digital counterparts.

### 2.2.3 Advances in Analog Sine-Wave Synthesizers

Oscillators are a popular research topic among analog/RF integrated circuit designers. The reason being the use of VCOs in wireless communication applications, and the rapid growth of the wireless communications industry. Developments in VCO designs for communication applications have mainly focused on improving the phase noise, reducing the power consumption, and widening the frequency tuning range [MM15, SNM+16].

Mainly with the aim of using analog oscillators for BIST applications, researchers have also focused on reducing the harmonic distortion of conventional analog oscillators. Authors in [BSS07] and [PABSS07] proposed an improvement to the gain limiting mechanism in oscillators. Instead of using a two level limiter such as a standalone op-amp, [BSS07] and [PABSS07] proposed the use of a multi-level limiter, that eliminates lower order harmonics of the oscillator output signal. A discrete implementation of an analog harmonic-cancelling oscillator was published in [VSCG13], where the output signal phases of a phase-shift oscillator were amplitude scaled and summed to eliminate harmonic distortion. An open-loop, switched-capacitor amplifier based oscillator was published in [BVRH06]. Later, in [BLVR14] the same authors published a modified version of the oscillator in [BVRH06] with better

harmonic distortion by using a harmonic-cancelling technique. At their core, the harmonic-cancelling techniques utilized in [BSS07, PABSS07, VSCG13, BLVR14] are inspired by [Dav69], which also forms the basis of this research. However, [BSS07, PABSS07, VSCG13, BLVR14] considers harmonic-cancelling sine-wave synthesis as an analog technique, while this thesis studies harmonic-cancelling sine-wave synthesis as a digital method.

Although advances have been made, analog sine-wave synthesizers remain behind digital sine-wave synthesizers in several aspects. Limited tuning capability and slow response time to programming inputs are two key disadvantages of analog sine-wave synthesizers, compared to their digital counterpart. Furthermore, as integrated circuit technologies scale, analog sine-wave synthesizers become increasingly less area and power cost efficient compared to digital sine-wave synthesizers.

## 2.3 Digital Sine-Wave Synthesis

### 2.3.1 Different Digital Techniques of Sine-Wave Synthesis

Several digital techniques for sine-wave signal synthesis are found in the literature. Closed-loop digital oscillator circuits were proposed and analyzed in [AEHAI86a, AEHAI86b, AI01]. A closed-loop digital oscillator circuit employs a second order recursive digital filter with poles on the unit-circle of the complex $z$ plane. In [DR99, RMPB04] sine-wave signals were produced by low-pass filtering a periodically played out bitstream. The bitstream played in [DR99, RMPB04] had been prepared by sigma-delta modulating a sine-wave signal. Digital harmonic-cancelling sine-wave synthesis, which is the focus of this thesis, is also a digital technique for synthesizing analog sine-wave signals. The first publication of a digital harmonic-cancelling sine-wave synthesis technique was in [Dav69]. Two years later [TRG71]

proposed the technology of direct digital frequency synthesis, which is currently the most popular method for sine-wave signal synthesis. Due to the overwhelming popularity of DDFSs over the other types of digital sine-wave synthesizers, we take a closer look at DDFSs in the following subsections.

### 2.3.2 Theoretical Background into DDFSs

The general hardware architecture of a DDFS is illustrated in Fig. 2.2 along with the output signals of each stage of the DDFS architecture [Van00]. In a DDFS, digital sine-wave samples are stored in a read-only memory (ROM). The ROM acts as a phase to amplitude converter by taking the phase of the sine-wave as a digital input and providing the corresponding amplitude of the sine-wave as a digital output. Digital amplitude samples output by the ROM are converted to the analog

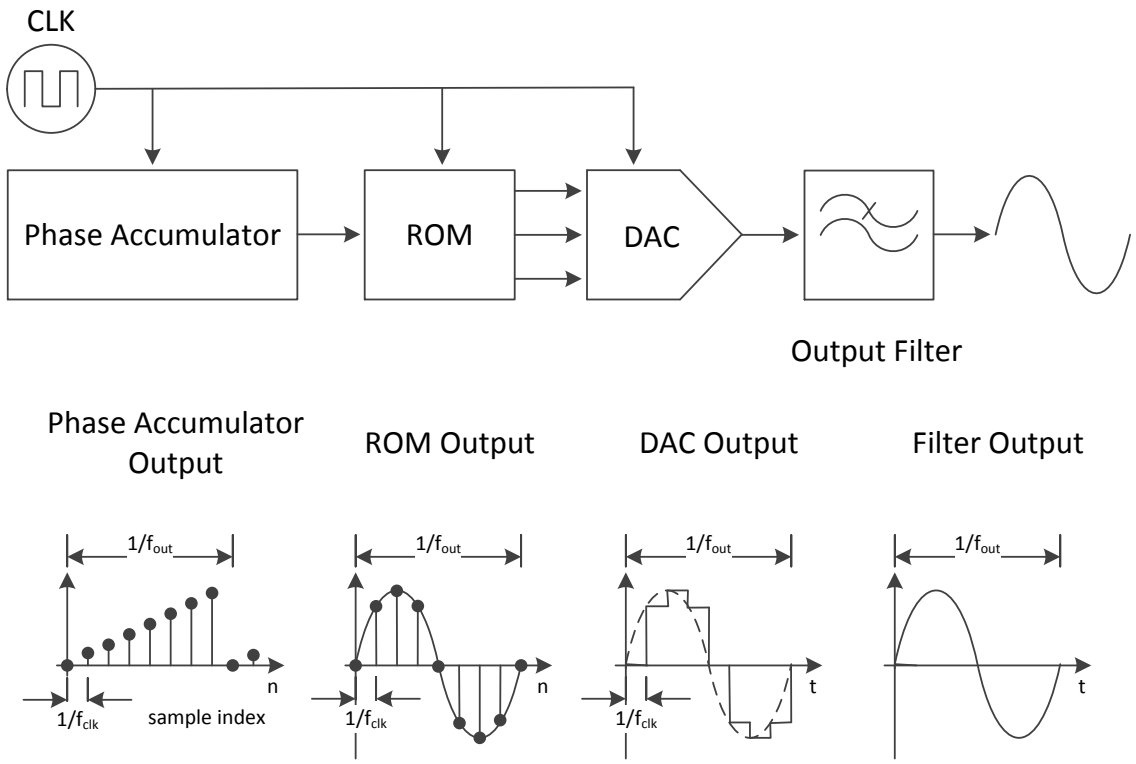


Figure 2.2: DDFS hardware architecture and signal flow

domain via a DAC. The DAC output will contain the fundamental frequency $f_{\text{out}}$, plus image frequencies at $nf_{\text{clk}} \pm f_{\text{out}}$, where $n \in \{x \mid x \in \mathbb{Z}\}$, $f_{\text{clk}}$ is the input clock frequency, and $f_{\text{out}}$ is the output sine-wave frequency. The magnitudes of the frequency contents of the output will be scaled by a sinc function due to the sample-and-hold nature of the DAC output. An analog low-pass filter is used to improve output signal spectrum purity by attenuating image frequencies and other spurs that fall beyond the desired frequency, $f_{\text{out}}$.

### 2.3.3 Programmability of DDFSs

Variation of amplitude, frequency, and phase of sinusoidal signals is utilized to modulate carrier signals with baseband signals in communication applications. In the following discussion, we will look into how amplitude, frequency, and phase of a DDFS output signal are programmed.

#### Amplitude Programmability

Samples stored in the ROM of a DDFS are of a sine-wave signal with constant and known amplitude. Therefore, the amplitude of a sine-wave output can be varied by having a digital multiplier between the ROM and the DAC, as shown in

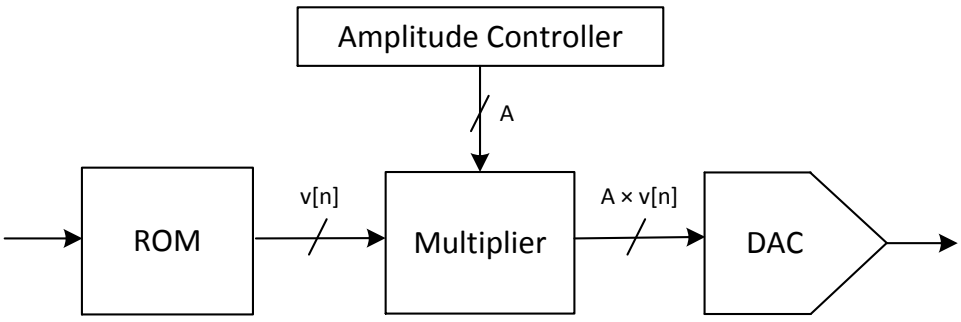


Figure 2.3: Programing the amplitude of the DDFS output signal

Fig. 2.3 [Van00]. As illustrated, the multiplier scales the ROM output $v[n]$ by the value of $A$. The value of $A$ can be programmed to vary the amplitude of the sine-wave output.

### Frequency and Phase Programmability

In order to understand how frequency and phase of a DDFS output signal are programmed, we should first understand the functionality of the phase accumulator block in Fig. 2.2. Figure 2.4 illustrates the design of the phase accumulator [Van00]. Based on the illustrated design, the output of the phase accumulator, $P_{\text{out}}$, is given in the following equation.

$$P_{\text{out}} = P + P_{\text{offset}} = (P_{\text{prev}} + \Delta P) + P_{\text{offset}} \tag{2.4}$$

where $P_{\text{out}}$, $P$, $P_{\text{offset}}$, $P_{\text{prev}}$, and $\Delta P$ are digital signals represented with $n$ bits each. Note that $\Delta P$ determines the rate of change of phase of the DDFS output signal, and $P_{\text{offset}}$ determines the relative phase. The frequency of a signal can be defined as the rate of change of phase of that signal. Therefore, the frequency of the DDFS

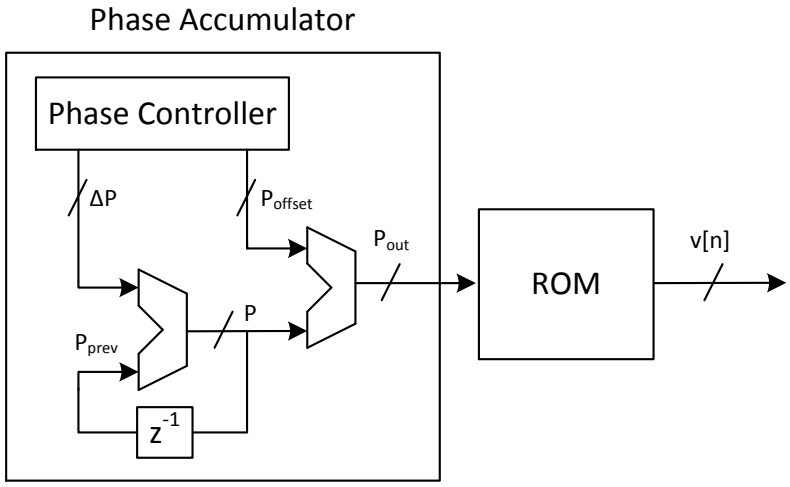


Figure 2.4: Phase accumulator design

output signal is programmed by adjusting $\Delta P$. The phase of the DDFS output signal is programmed by setting $P_{\text{offset}}$.

As $P_{\text{out}}$ is an $n$–bit digital word, for a given value of $\Delta P$, the output signal frequency is given by the following equation.

$$f_{\text{out}} = \frac{\Delta P}{2^n} \times f_{\text{clk}} \tag{2.5}$$

Since the lowest increment which can be made to $\Delta P$ is 1, the resolution with which the output signal frequency can be programmed is given below.

$$\Delta f = \frac{f_{\text{clk}}}{2^n} \tag{2.6}$$

$P_{\text{offset}}$ can take $2^n$ values. Thus, the resolution with which the output signal phase can be programmed is given in radians as follows.

$$\Delta p = \frac{\pi}{2^{n-1}} \text{ rad} \tag{2.7}$$

Finally, note that because DDFS is a digital open-loop technique, it can maintain a fast response time to amplitude, frequency, and phase changes. The response time will be dominated by the settling time of the analog output filter, which filters the DAC output.

### 2.3.4 Issues Associated with DDFSs

#### Phase Noise

Phase noise in a DDFS output signal originates from phase noise in the input clock signal. A phase noise model for DDFSs was presented in [Van00] based on the work in [Lee66]. According to the model published in [Van00], the phase noise of

the output signal ($\mathscr{L}_{\text{out}}(f)$) depends on the phase noise of the input clock signal ($\mathscr{L}_{\text{clk}}(f)$) and the ratio $f_{\text{clk}}/f_{\text{out}}$ as shown in the following equation.

$$\mathscr{L}_{\text{out}}(f) = \mathscr{L}_{\text{clk}}(f) - 20 \times \log_{10}\left(\frac{f_{\text{clk}}}{f_{\text{out}}}\right) \tag{2.8}$$

Note that $\mathscr{L}_{\text{out}}(f) \leq \mathscr{L}_{\text{clk}}(f) - 6$ dB, because $f_{\text{out}} \leq f_{\text{clk}}/2$ according to the Nyquist sampling theorem. Usually a DDFS is used in a SoC that consists of global PLLs. Then, a low phase noise clock signal for the DDFS can be derived from one PLL output, thus improving the phase noise of the DDFS output signal.

### Spurious Signals

Spurious signals in a DDFS output can originate from several sources [Van00]. Let us look into two primary sources of DDFS spurs. Due to the finite number of bits used to store each sine-wave amplitude sample in the ROM, the digital sine-wave samples contain quantization errors. When the sine-wave samples are periodically played out of the DAC, the quantization errors associated with the sine-wave samples cause spurious tones to appear at the DAC output. Such spurious contents are also called quantization noise in the context of a DDFS.

Non-ideal DAC characteristics are another source of DDFS spurs. A real DAC suffers from many types of errors [TI995]. DC errors are caused by non-idealities in the transfer function between the digital input and the analog output. AC errors in a DAC are caused due to finite slew rate, finite settling time, and glitches in the DAC output signal [Van00]. Both AC and DC errors in the DAC result in spurs at the DDFS output.

#### Area and Power Consumptions

The main culprits in area and power consumptions of a DDFS are the ROM and the DAC. For a DDFS to reach high frequencies with low spur levels at the output, a higher clock frequency is required. However, as the clock frequency increases, so does the power consumption of the ROM and the DAC. Furthermore, the area and power consumptions of the ROM and the DAC increase with ROM depth and resolution. According to Eq. 2.6 and Eq. 2.7, more depth in the ROM (higher $n$) is required for finer resolution in frequency and phase programmability.

Higher resolution in the ROM and the DAC is required for higher signal-to-quantization-noise ratio (SQNR) in the DDFS output signal. The amplitude resolution of the DAC affects the SQNR of the DAC output signal according to the '6 dB/bit rule' [Ben48]. The 6 dB/bit rule means that to increase the SQNR of the DAC output signal by 6 dB, the amplitude resolution of the DAC should be increased by 1 binary bit. As the DAC takes its inputs from the ROM in a DDFS, the resolution of the digital samples stored in the ROM should also be increased by 1 bit. Increased resolution in the ROM and the DAC comes with the cost of increased area and power consumptions. Therefore, there is a compromise between area and power consumptions, finer programmability, and spectral purity in a DDFS design.

### 2.3.5 Advances in DDFS Technology

Due to the popularity of DDFSs, many researchers have worked on reducing the spur levels as well as area and power consumptions of DDFSs. Methods of reducing spurs in the DDFS output signal were discussed and compared in [Van96].

Different techniques for phase-to-amplitude conversion (traditionally done with a ROM) in DDFSs were discussed in [Van97]. A commonly used technique is stor-

ing only one quarter of the sine-wave samples, and then utilizing the quarter-wave symmetry of the sinusoidal signal to reproduce the whole sine-wave [Van97]. Sine-wave sample memory compression techniques include the sine-phase difference algorithm [Van97], the Sunderland architecture [SSW+84], and the Nicholas architecture [NSK88]. In the sine-phase difference algorithm, $\sin(\pi\theta/2) - \theta$ is stored in the ROM instead of $\sin(\pi\theta/2)$. The Sunderland architecture utilizes trigonometric identities for lossy compression of sine-wave sample data, and a segmented ROM, one high precision and the other low precision, to store the compressed samples. The Nicholas architecture is a version of the Sutherland architecture optimized for higher compression ratio and better accuracy. Other approaches to designing the phase-to-amplitude converter include using the Cordinate Rotation algorithm [GD98], Taylor series approximation [PN03], and linear interpolation [LAK03]. The techniques discussed above are effective in decreasing the area and power consumptions of the phase-to-amplitude converter. However, this area and power saving comes at the cost of lower precision in the digital sine-wave samples, which increases the quantization noise level in the DDFS output.

A ROM-less DDFS design was first introduced in [ML99] to reduce the area and power consumptions of DDFSs. In a ROM-less DDFS, the ROM and DAC functionality of a conventional DDFS are combined to a nonlinear DAC. The non-linear DAC takes in the phase of the sine-wave signal as a digital input signal and outputs the corresponding sine-wave amplitude as an analog signal. ROM-less DDFS designs with non-linear DACs have been used in some of the recent DDFS related work [ZR08, GDIJ10, YYJ+14].

A method of reducing DAC errors in a DDFS using closed-loop feedback was presented in [LMC08]. The design proposed in [LMC08] used an ADC and a DSP block to implement closed-loop feedback. Therefore, the reduction in spur level at the DDFS output of [LMC08] came at significant area and power costs.

Despite the advances made in DDFS technology, even state-of-the-art DDFS related work perform worse in terms of area and power consumptions, compared to DHSSs [SSS15]. However, the advantage DDFSs hold over DHSSs is the programmability of phase and frequency of the output signal with very fine resolution.

## 2.4 Digital Harmonic-Cancelling Sine-Wave Synthesis

### 2.4.1 Background and Related Work

The concept of digital harmonic-cancelling sine-wave synthesis was first proposed close to forty-seven years ago in [Dav69]. Despite being published two years prior to the first publication of a DDFS [TRG71], DHSSs have been overshadowed by DDFSs as the most popular digital sine-wave signal synthesis technology throughout the past four and a half decades. However, in recent years there has been a renaissance in DHSSs with the publication of [ESS10, SBT+10, BLVR14, SSS15].

Figure 2.5 illustrates the digital harmonic-cancelling sine-wave synthesis technique first proposed in [Dav69]. The technique involves scaling and summing a set of phase shifted square-wave signals to produce a step-wise approximation of a sine-wave signal. It can be mathematically proven (see Section 3.2) that the synthesized step-wise sine-wave signal does not contain lower order harmonics from $HD_2$ to $HD_{2k}$, where $k$ is the number of square-wave signals summed, as shown in Fig. 2.5.

The generic hardware architecture of a DHSS is illustrated in Fig. 2.6. The square-wave generator synthesizes the required set of phase shifted square-wave signals as 1-bit digital signals. The summing circuit performs the harmonic-cancelling operation by scaling and summing the set of digital square-wave signals. The optional

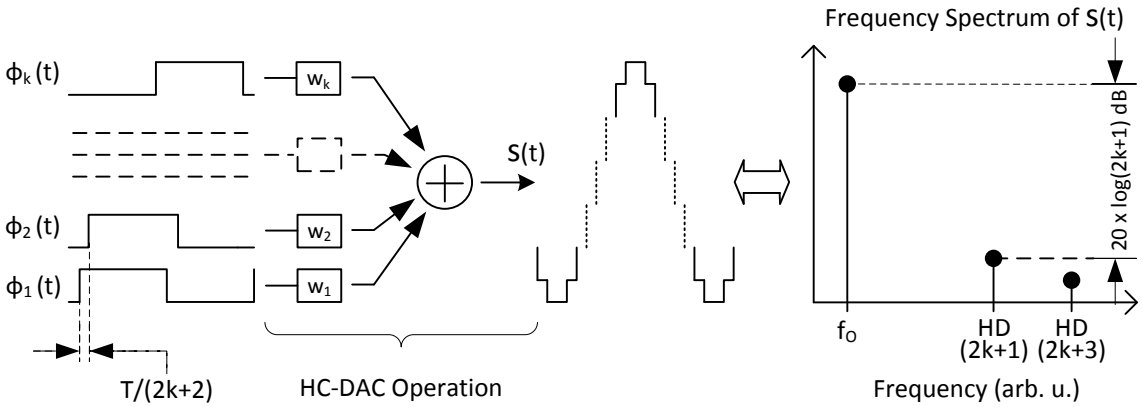


Figure 2.5: Digital harmonic-cancelling sine-wave synthesis technique

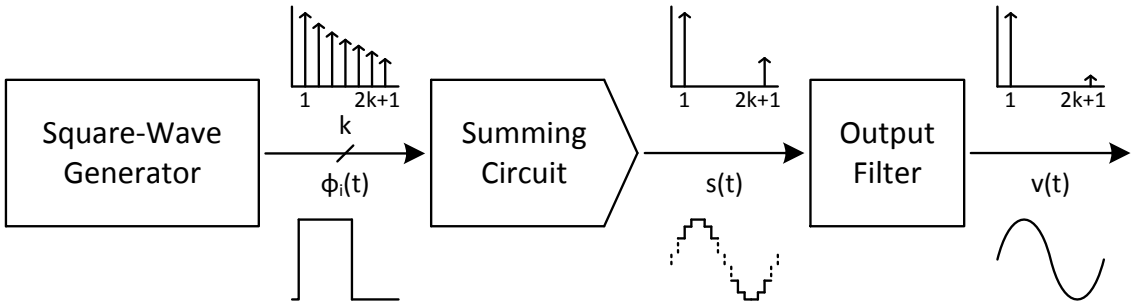


Figure 2.6: Generic DHSS hardware architecture

output filter is used to further reduce the harmonic distortion by attenuating residual harmonics which remain after the harmonic-cancelling operation.

Among DHSS implementations found in the literature, [SBT+10, SSS15] utilized CMOS ring oscillators for the square-wave generator, while [Dav69, ESS10] realized the square-wave generator as a sequential logic circuit. The summing circuit was implemented as a summing amplifier in [Dav69], while [SBT+10] used a current steering architecture, and [ESS10, SSS15] went with a resistor adder network.

It should be noted that although [ESS10] has been put in the same category with [Dav69, SBT+10] in this discussion, the digital harmonic-cancelling sine-wave synthesis technique proposed in [ESS10] is slightly different from the technique first published in [Dav69]. Both methods compose a sine-wave signal by adding a set

of phase-shifted square-wave signals. However, [Dav69] used a set of square-wave signals with differing amplitudes and equal phase-shifts, while [ESS10] used a set of square-wave signals with equal amplitude and differing phase-shift.

### 2.4.2 The Advantage of DHSSs

At first glance, the DHSS architecture in Fig. 2.5 looks similar to the DDFS architecture in Fig. 2.3. The square-wave generator outputs a set of digital signals corresponding to the sine-wave signal amplitude, which is similar to the task carried out by the phase accumulator in combination with the ROM. The summing circuit takes in a set of digital signals, scales their amplitudes, and sums them, which is the same as the underlying operation of a DAC.

One way to understand the difference between DHSSs and DDFSs is as follows. The signal synthesis technique used in DDFSs, which is to save digital samples of the signal in a ROM and play the analog signal via a DAC, is not unique to sine-wave signals. In other words, any given periodic signal can be synthesized using a DDFS. On the other hand, the signal synthesis technique employed in DHSSs is custom-made for sine-wave signals. Therein lies the reason why DHSSs are more area and power cost efficient compared to DDFSs.

The hardware complexity of the square-wave generator in a DHSS is significantly less compared to the combined hardware complexity the phase accumulator and the ROM in a DDFS. Furthermore, the summing circuit used in a DHSS is more area and power cost efficient compared to a regular DAC utilized in a DDFS. Using figures-of-merit, which took into account the output frequency, harmonic distortion, power cost, and area cost, the results published in [ESS10, SSS15] have confirmed that state-of-the-art DHSSs outperform state-of-the-art DDFSs by a factor of at least four in each comparison.

### 2.4.3 Deficiencies in DHSSs

#### Phase Noise

Phase noise in a DHSS output signal depends on how the square-wave generator is implemented. Ring oscillators generate notoriously high amounts of phase noise [Raz96]. Thus, using ring oscillators to produce the square-wave signals, as was the case in [SBT+10, SSS15], can significantly increase the phase noise in the DHSS output. On the other hand, if a clocked circuit is used as the square-wave generator, the phase noise in the DHSS output can be described by Eq. 2.8, similar to a DDFS. Therefore, by using a clock signal with low phase noise, possibly derived from an on-chip global PLL output, DHSSs with clocked square-wave generators can produce output signals with low phase noise.

#### Limited Programmability

Programmability of amplitude, frequency, and phase of the output sine-wave signal is the characteristic which makes DHSSs pale in comparison to DDFSs. Amplitude programming with the same agility as DDFSs is simply not possible with DHSSs.

Frequency programming in a DHSS is done by changing the clock frequency, if the square-wave generator is implemented as a clocked circuit [Dav69, ESS10]. In such a case, while the DHSS itself can have a fast response time to a change in clock frequency, changing the clock frequency might be a slow process. On the other hand, if the square-wave generator is implemented as a ring oscillator [SBT+10, SSS15], frequency programming is done by tuning the frequency of the ring oscillator. Then, the response time of the DHSS itself will be slow, because of the settling time of the ring oscillator to a change in frequency.

The DHSS designs published in [Dav69, ESS10, SBT+10, SSS15] do not support phase programmability. However, as it will become evident from this thesis, DHSSs can be designed to be phase programmable.

### Limited Understanding of the Summing Circuit

The accuracy of the summing circuit determines the amount of harmonic cancellation that occurs in a DHSS. As discussed in detail later, the summing circuit can be considered as an unorthodox DAC circuit. Moreover, the summing circuit is the most area and power hungry block in a DHSS. However, several fundamental questions regarding the summing circuit have been left unasked in existing DHSS related publications [Dav69, ESS10, SBT+10, SSS15]:

1. How does amplitude resolution of the summing circuit affect the spectral purity of the DHSS output signal? Does the relationship between amplitude resolution and spectral purity follow the 6 dB/bit rule [Ben48], which exists for conventional DACs?

2. How does component mismatch in the summing circuit affect the spectral purity of the DHSS output signal?

3. Can dynamic element matching techniques be cost effectively used in the summing circuit to mitigate the effect of component mismatch?

Seeking the answers to these questions can lead to improvements in the performance of DHSSs, as it will become evident from this thesis.

## 2.5 A Path Forward

In this literature review, we have studied three types of sine-wave signal synthesizers. Analog sinusoidal signal synthesizers, the classic choice for sine-wave synthesis, were the first to be explored. Then, the discussion moved to direct digital frequency synthesizers, which are the most popular group of digital sine-wave synthesizers. Finally, digital harmonic-cancelling sine-wave synthesizers, a forgotten piece of history until a recent renaissance, were discussed.

The future of sinusoidal signal synthesis lies in the digital domain, as analog sine-wave synthesizers cannot match the programmability and technology scaling-friendly nature of digital sine-wave synthesizers. After having a close look at digital sine-wave synthesizers, several key points can be highlighted. DDFSs are the superior approach in terms of programmability. On the other hand, to achieve high spectral purity in the output signal a DDFS requires high area and power consumptions. DHSSs can maintain a better compromise between output spectral purity, and area and power costs, compared to DDFSs. However, DHSSs pale in comparison to DDFSs when it comes to programmability.

A path forward for sinusoidal signal synthesizers is to improve DHSSs so that the programmability gap between DHSSs and DDFSs is narrower, and the advantage in area and power cost effectiveness DHSSs hold over DDFSs is wider, compared to the state-of-the-art. In this research we have trodden along this path forward, by studying the following research sub-topics:

1. Designing DHSSs that support programmability of the phase of the output sine-wave signal

2. Understanding how amplitude resolution and mismatch of the summing circuit affect the spectral purity of the output signal

3. Applying the understanding gained from (2) to improve the area and power cost efficiency of DHSSs

4. Applying cost effective dynamic element matching techniques to reduce the effect of mismatch in the summing circuit

# Chapter 3

# Digital Harmonic-Cancelling Sine-Wave Synthesizers

## 3.1 Overview

In this chapter, we first describe the theory of digital harmonic-cancelling sine-wave synthesis, which is the foundation of this thesis. We explain the theory from three different points of view. Next, we propose a hardware architecture for Digital Harmonic-Cancelling Sine-Wave Synthesizers, which is one of the contributions of this thesis. Finally, we discuss potential application scenarios for DHSSs, which utilize the proposed DHSS architecture.

## 3.2 Digital Harmonic-Cancelling Sine-Wave Synthesis

The theory of digital harmonic-cancelling sine-wave synthesis can be explained from several viewpoints. When DHSSs were first introduced in [Dav69], Davies delineated the method of digital harmonic-cancelling sine-wave synthesis as a finite impulse response (FIR) filter based technique by using both time domain and frequency domain approaches. In recent work, [SBT+10] described the same theory by using example phasor diagrams to illustrate how harmonics are canceled, while [SSS15] used a similar approach to [Dav69]. This thesis explicates the theory of digital harmonic-cancelling sine-wave synthesis using three different methods in the following subsections.

### 3.2.1 Composing a Sampled Sine-Wave out of Square-Waves

One way to perceive digital harmonic-cancelling sine-wave synthesis is as a technique in which a sampled continuous-time sine-wave signal is synthesized out of

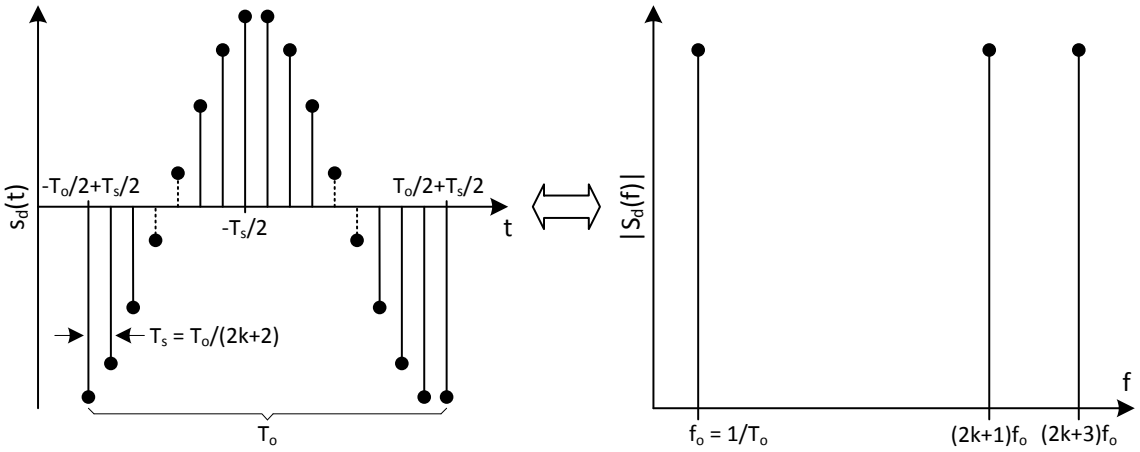


Figure 3.1: Sampled discrete-time sine-wave in time domain and frequency domain

square-wave signals. Let us first understand the time-domain and frequency domain characteristics of sampled sine-waves, and then discuss how square-waves can be used to generate a sampled continuous-time sine-wave. We begin the discussion by considering the sampled discrete-time sine-wave, which is drawn in both time domain and frequency domain in Fig. 3.1.

The sine-wave is sampled at a period of $T_\mathrm{s}$, which is defined as follows

$$T_\mathrm{s} \;=\; \frac{T_\mathrm{o}}{2k+2} \tag{3.1}$$

where $T_\mathrm{o}$ is the period of the sine-wave and $k \in \{x \mid x \geq 3,\ x \in \mathbb{Z}^+\}$. The use of $k$ in Eq. 3.1 will be made clear as this discussion moves forward. Based on Eq. 3.1, the relationship between the sampling frequency ($f_\mathrm{s}$) and the sine-wave frequency ($f_\mathrm{o}$) is delineated by

$$f_\mathrm{s} \;=\; (2k+2) \times f_\mathrm{o} \tag{3.2}$$

The time domain description of the sampled discrete-time sine-wave is given by

$$s_\mathrm{d}(t) \;=\; A\,\cos\left(2\pi f_\mathrm{o} t\right) \times \sum_{n=-\infty}^{\infty} \delta\left[t - (nT_\mathrm{s} - T_\mathrm{s}/2)\right] \tag{3.3}$$

where $A$ is an arbitrary constant, $\delta$ is the unit impulse function, and $n \in \mathbb{Z}$. Note that adding a time shift of $T_\mathrm{s}/2$ to the unit impulse function makes the analog sine-wave signal's peaks and troughs to occur right in the middle of a sample period, which is a useful property as highlighted later.

The frequency domain description of the sampled discrete-time sine-wave is given by the Fourier transform

$$S_\mathrm{d}(f) \;=\; \mathcal{F}\left\{s_\mathrm{d}(t)\right\} \tag{3.4}$$

As proven in Appendix A, by evaluating the Fourier transform given in Eq. 3.4, $S_\mathrm{d}(f)$ can be expressed as follows:

$$S_\mathrm{d}(f) \;=\; \frac{A\,e^{-j\pi f/f_\mathrm{s}}}{2\,T_\mathrm{s}} \sum_{m=-\infty}^{\infty} \delta\left(f - \left[m\left(2k+2\right) - 1\right] f_\mathrm{o}\right) + \delta\left(f - \left[m\left(2k+2\right) + 1\right] f_\mathrm{o}\right) \tag{3.5}$$

where $j$ is the imaginary unit and $m \in \mathbb{Z}$.

According to Eq. 3.5, $S_{\mathrm{d}}(f)$ consists of the frequency content of the ideal sinusoidal signal, $A\cos(2\pi f_{\mathrm{o}}t)$, and images of it at integer multiples of $(2k+2)f_{\mathrm{o}}$. Figure 3.1 illustrates the positive frequency spectrum of $S_{\mathrm{d}}(f)$ upto the first two image frequencies around $(2k+2)f_{\mathrm{o}}$.

Let us now consider the sampled continuous-time sine-wave illustrated in Fig. 3.2, which can be obtained by applying a zero-order-hold on $s_{\mathrm{d}}(t)$. Thus, $s_{\mathrm{c}}(t)$ is defined as follows:

$$s_{\mathrm{c}}(t) \;=\; \mathrm{rect}\left(\frac{t - T_{\mathrm{s}}/2}{T_{\mathrm{s}}}\right) * s_{\mathrm{d}}(t) \tag{3.6}$$

where $\mathrm{rect}(x)$ is the rectangular function.

Utilizing Eq. 3.6 and the convolution theorem [CF48, Kam04] to derive the Fourier transform of $s_{\mathrm{c}}(t)$ gives

$$S_{\mathrm{c}}(f) \;=\; \mathcal{F}\{s_{\mathrm{c}}(t)\} \;=\; \mathcal{F}\left\{\mathrm{rect}\left(\frac{t - T_{\mathrm{s}}/2}{T_{\mathrm{s}}}\right)\right\} \times \mathcal{F}\{s_{\mathrm{d}}(t)\} \tag{3.7}$$

With the use of Fourier transform identities published in [CF48, Kam04], and sub-

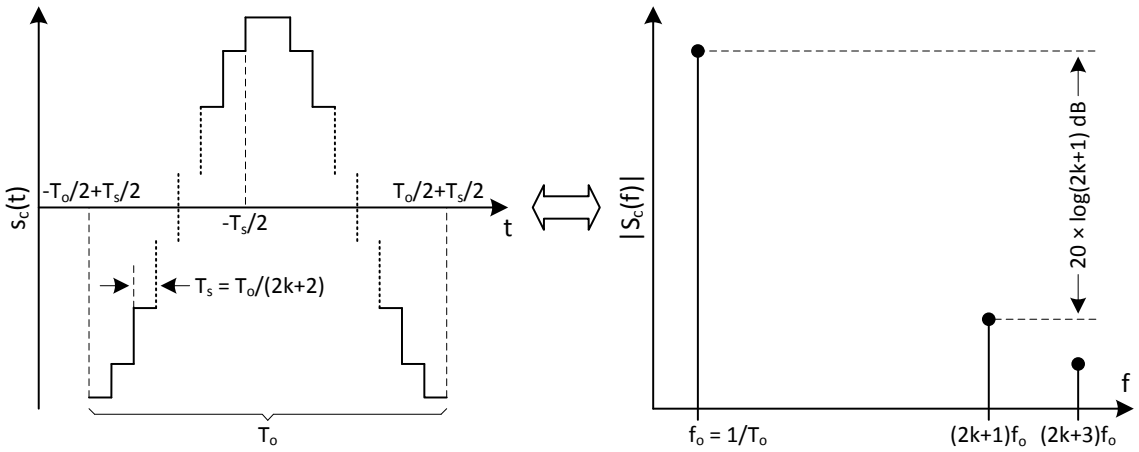


Figure 3.2: Sampled continuous-time sine-wave in time and frequency domains

stituting for $\mathcal{F}\{s_{\mathrm{d}}(t)\}$ from Eq. 3.4 we obtain

$$S_{\mathrm{c}}(f) \;=\; e^{-j\pi f/f_{\mathrm{s}}} \times T_{\mathrm{s}}\,\mathrm{sinc}\left(\frac{f}{f_{\mathrm{s}}}\right) \times S_{\mathrm{d}}(f) \tag{3.8}$$

where $\mathrm{sinc}\,(x)$ is the normalised sinc function.

A segment of $S_{\mathrm{c}}(f)$ is visually represented in Fig. 3.2, which can be construed as the frequency spectrum of the ideal sine-wave signal, $A\cos(2\pi f_{\mathrm{o}}t)$, distorted by harmonics. From Fig. 3.2 note that the frequency spectrum of $s_{\mathrm{c}}(t)$ does not contain lower order harmonic distortions from the second harmonic distortion ($\mathrm{HD}_2$) up to and including the $(2k)^{\mathrm{th}}$ harmonic distortion ($\mathrm{HD}_{2k}$).

The amplitude of $\mathrm{HD}_{2k+1}$, which is the existing harmonic with the lowest order, is calculated as follows:

$$\mathrm{HD}_{2k+1} \;=\; 20\log\left|\frac{S_{\mathrm{c}}\left([2k+1]\,f_{\mathrm{o}}\right)}{S_{\mathrm{c}}(f_{\mathrm{o}})}\right| \;\mathrm{dBc} \tag{3.9}$$

Substituting for $S_{\mathrm{c}}(f)$ from Eq. 3.8 and simplifying the equation gives

$$\mathrm{HD}_{2k+1} \;=\; -\,20\log\left(2k+1\right)\;\mathrm{dBc} \tag{3.10}$$

The lack of lower order harmonics from $\mathrm{HD}_2$ to $\mathrm{HD}_{2k}$ and the attenuated higher order harmonics make sampled continuous-time sine-waves useful. Assume that we have a system which can synthesize $s_{\mathrm{c}}(t)$. For applications in which the attenuated higher order harmonic distortions can be tolerated, $s_{\mathrm{c}}(t)$ can be used as it is. Alternatively, a low-pass filter (LPF) can be used to produce a purer sine-wave by attenuating the higher order harmonics further.

Let us now look into the digital harmonic-cancelling sine-wave synthesis technique, which is a method for synthesizing a sampled continuous-time sine-wave signal using square-wave signals. Figure 3.3 illustrates how $s_{\mathrm{c}}(t)$ is synthesized. The number of square-waves required to synthesize $s_{\mathrm{c}}(t)$ is equal to $k$, which is a variable that has

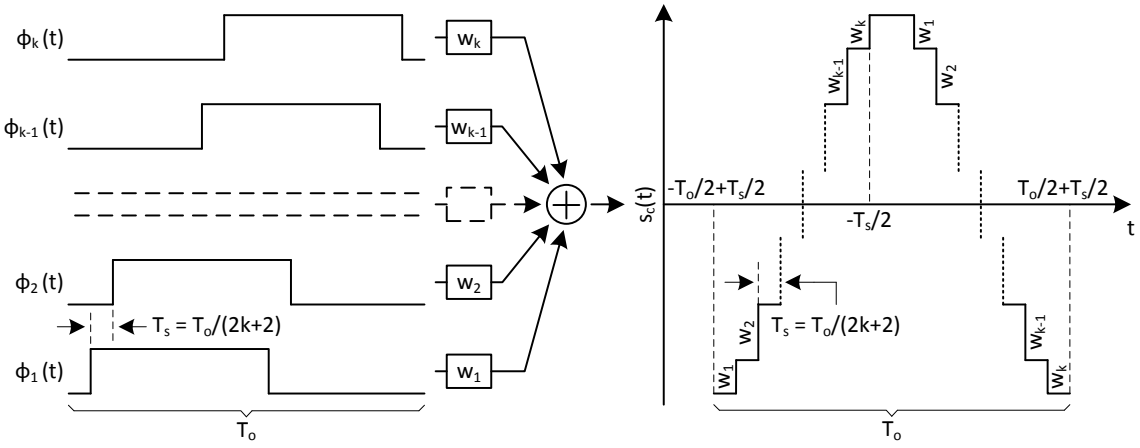


Figure 3.3: Synthesizing a sampled continuous-time sine-wave out of square-waves

been part of this discussion since the definition of Eq. 3.1. It is interesting to note that if the time-shift of $T_\mathrm{s}/2$ was not included in the unit impulse function in Eq. 3.3, then we would require $k+1$ number of square-waves to synthesize $s_\mathrm{c}(t)$.

The square-wave signals are denoted by $\phi_i(t)$, where $i \in \{x \mid x \leq k,\ x \in \mathbb{Z}^+\}$. Without loss of generality, let us assume that each square-wave signal has a unit amplitude. The square-waves are shifted in time, such that the time-shift of $\Delta t_i$ between square-waves $\phi_i(t)$ and $\phi_1(t)$ is given by

$$\Delta t_i \ = \ (i-1)\, T_\mathrm{s} \tag{3.11}$$

Amplitude of square-wave $\phi_i(t)$ is scaled by a factor of $w_i$ prior to the square-waves being summed, such that the amplitude transitions of each square-wave correspond to specific amplitude transitions of $s_\mathrm{c}(t)$. As shown in Fig. 3.3, transitions of square-wave $\phi_i(t)$ correspond to the transitions of $s_\mathrm{c}(t)$ at $t = nT_\mathrm{o}/2 + (2i+1)T_\mathrm{s}/2$, where $n \in \mathbb{Z}$. Thus, the square-wave amplitude scaling factors are defined as follows:

$$w_i \ = \ s_\mathrm{c}\,(i\,T_\mathrm{s}) - s_\mathrm{c}([i+1]T_\mathrm{s}) \tag{3.12}$$

Substituting first for $s_\mathrm{c}(t)$ from Eq 3.6, then for $s_\mathrm{d}(t)$ from Eq. 3.3, and simplifying the equation gives

$$w_i \ = \ 2\,A\,\sin(T_\mathrm{s}/2) \times \sin\left(\frac{i\pi}{k+1}\right) \tag{3.13}$$

Noting that the relative values of the amplitude scaling factors are of more importance, than their absolute value, and defining $B = 2A\sin(T_s/2)$ as an arbitrary constant, which is independent of $i$, we can rewrite Eq. 3.13 as

$$w_i = B \times \sin\left(\frac{i\pi}{k+1}\right) \tag{3.14}$$

In summary, this subsection looks at digital harmonic-cancelling sine-wave synthesis as a technique for composing a sampled continuous-time sine-wave signal using square-wave signals. We first looked at the characteristics of sampled sine-wave signals in both time and frequency domains, to understand the reasons which make sampled continuous-time sine-waves useful in applications which require sinusoidal signals. Then, we outlined how a set of time-shifted square-wave signals can be amplitude scaled and summed to produce a sampled continuous-time sine-wave signal. The time-shift and amplitude scaling factor of each square-wave required in the digital harmonic-cancelling sine-wave synthesis technique have been analytically defined in this subsection.

### 3.2.2 FIR Filter for Square-Waves - Time Domain Approach

Another way to perceive digital harmonic-cancelling sine-wave synthesis is as a technique which filters a square-wave signal using an FIR filter to produce a sine-wave signal with low harmonic distortion. The design of such a filter can be considered in either the time domain or the frequency domain. In this subsection, we focus on the time-domain.

Figure 3.4 illustrates the concept of putting a square-wave signal through an FIR filter to produce a sine-wave signal, where $z$ denotes

$$z = e^{j2\pi T_s f} \tag{3.15}$$

Please note that all variables reused in this subsection retain their original definitions, unless stated otherwise. The square-wave signal provided to the FIR filter is defined as follows:

$$\phi_1(t) = \begin{cases} +1 & 0 \leq t < T_o/2 \\ -1 & T_o/2 \leq t < T_o \\ \phi_1(t - T_o) & t \geq T_o \\ \phi_1(t + T_o) & t < 0 \end{cases} \tag{3.16}$$

To produce a pure sine-wave signal out of $\phi_1(t)$, the FIR filter should have the ideal

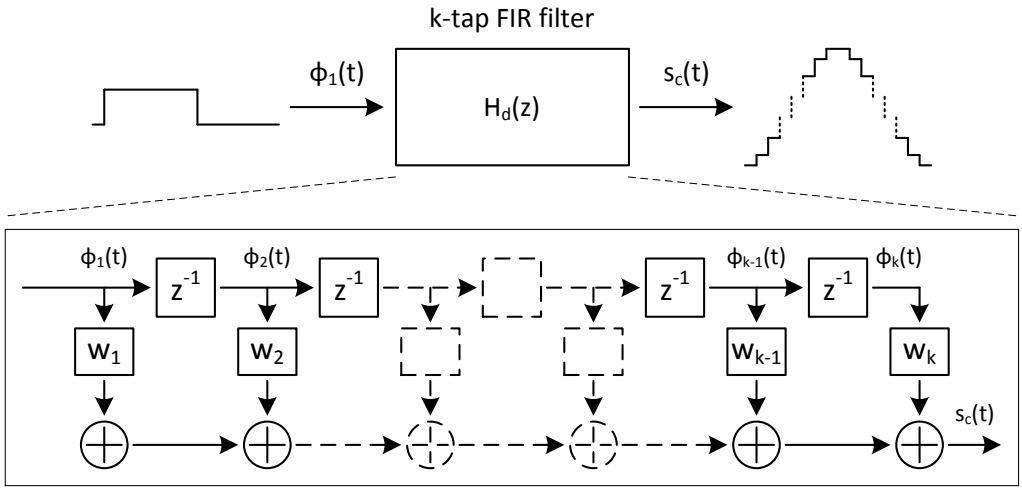


Figure 3.4: Putting a square-wave through a $k$-tap FIR filter to produce a sine-wave

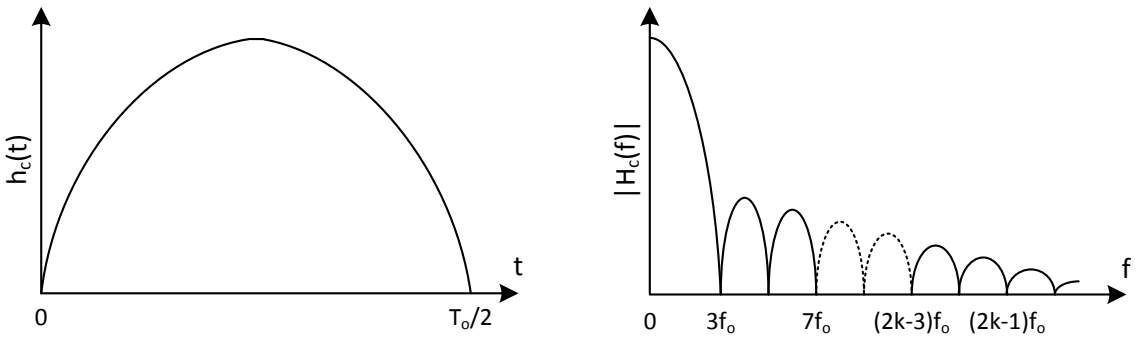


Figure 3.5: Ideal impulse response of the FIR filter with infinite number of taps, in the time domain (left) and the frequency domain (right)

impulse response given by

$$h_{\mathrm{c}}(t) \;=\; B\,\sin\left(2\pi f_{\mathrm{o}} t\right) \times \mathrm{rect}\left(\frac{t - T_{\mathrm{o}}/4}{T_{\mathrm{o}}/2}\right) \tag{3.17}$$

where $B$ is an arbitrary constant. Thus, the ideal transfer function of the FIR filter is given by

$$H_{\mathrm{c}}(f) \;=\; \mathcal{F}\left\{h_{\mathrm{c}}(t)\right\} \tag{3.18}$$

$$\;=\; \left\{\frac{B}{2}\left[\delta\left(f - f_{\mathrm{o}}\right) + \delta\left(f + f_{\mathrm{o}}\right)\right]\right\} * \left\{\frac{e^{-j\pi f/2f_{\mathrm{o}}}\,T_{\mathrm{o}}}{2}\,\mathrm{sinc}\left(\frac{f}{2f_{\mathrm{o}}}\right)\right\} \tag{3.19}$$

For mathematical proof that the convolution of $\phi_1(t)$ and $h_{\mathrm{c}}(t)$ produces a sine-wave signal, and a derivation of $H_{\mathrm{c}}(f)$, please refer to Appendix A. The ideal impulse response of the FIR filter is visualised in both time and frequency domains in Fig. 3.5. Although an FIR filter having $h_{\mathrm{c}}(t)$ as its impulse response is capable of producing a pure sine-wave signal out of a square-wave signal, implementing $h_{\mathrm{c}}(t)$ requires an infinite number of filter taps. With a finite number of filter taps, we can implement a sampled discrete approximation to $h_{\mathrm{c}}(t)$.

Let us consider a $k$-tap FIR filter with a sampling period of $T_{\mathrm{s}}$, as delineated in

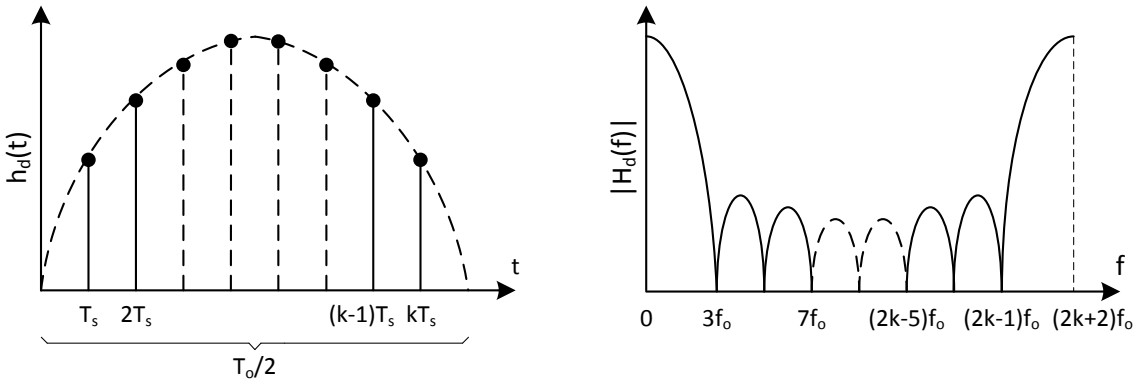


Figure 3.6: Discrete impulse response of the FIR filter with finite number of taps, in the time domain (left) and the frequency domain (right)

Fig. 3.4, with the impulse response defined by

$$h_{\mathrm{d}}(t) = \sum_{i=1}^{k} B \sin\left[2\pi f_{\mathrm{o}}(iT_{\mathrm{s}})\right] \delta\left(t - iT_{\mathrm{s}}\right) \tag{3.20}$$

$$= h_{\mathrm{c}}(t) \times \sum_{n=-\infty}^{\infty} \delta\left(t - nT_{\mathrm{s}}\right) \tag{3.21}$$

As delineated in Fig. 3.6, $h_{\mathrm{d}}(t)$ contains $k$ number of samples of the half sine pulse in $h_{\mathrm{c}}(t)$. As the samples cover the entire half sine pulse, and are equally spaced in time, the relationship between $T_{\mathrm{s}}$ and $k$ can be derived as follows:

$$T_{\mathrm{s}} = \frac{T_{\mathrm{o}}/2}{k+1} = \frac{T_{\mathrm{o}}}{2k+2} \tag{3.22}$$

which reiterates the relationship defined in Eq. 3.1.

The transfer function of the $k$-tap FIR filter, $H_{\mathrm{d}}(f)$, can be derived using two methods, each of which provides a different perspective on the FIR filter. The first approach to deriving $H_{\mathrm{d}}(f)$ uses Eq. 3.21 as follows:

$$H_{\mathrm{d}}(f) = \mathcal{F}\left\{h_{\mathrm{d}}(t)\right\} = \mathcal{F}\left\{h_{\mathrm{c}}(t)\right\} * \mathcal{F}\left\{\sum_{n=-\infty}^{\infty} \delta\left(t - nT_{\mathrm{s}}\right)\right\} \tag{3.23}$$

Using the Fourier transform identities in [CF48, Kam04] to calculate the Fourier transform of the impulse train, and solving the convolution operation gives

$$H_{\mathrm{d}}(f) = \frac{1}{T_{\mathrm{s}}} \sum_{m=-\infty}^{\infty} H_{\mathrm{c}}(f - mf_{\mathrm{s}}) \tag{3.24}$$

A visual representation of $H_{\mathrm{d}}(f)$ is presented in Fig. 3.6. According to Eq. 3.24, $H_{\mathrm{d}}(f)$ contains images of $H_{\mathrm{c}}(f)$ at integer multiples of $f_{\mathrm{s}}$. Thus, as illustrated in Fig. 3.6, $H_{\mathrm{d}}(f)$ contains consecutive zeros at each odd harmonic of $f_{\mathrm{o}}$, from $3f_{\mathrm{o}}$ up to $(2k-1)f_{\mathrm{o}}$. Consequently, when the square-wave signal, $\phi_1(t)$, which only contains odd order harmonics due to its half-wave symmetry, is put through the $k$-tap FIR filter, the output signal, $s_{\mathrm{c}}(t)$, does not contain harmonic distortions from $\mathrm{HD}_2$

to $\mathrm{HD}_{2k}$. Note that as $k$ increases, $h_\mathrm{d}(t)$ approaches $h_\mathrm{c}(t)$, and $\mathrm{HD}_{2k}$ is pushed higher in frequency, making $s_\mathrm{c}(t)$ approach a pure sine-wave.

The second approach to deriving $H_\mathrm{d}(f)$ makes use of Eq. 3.20 as follows:

$$H_\mathrm{d}(f) \;=\; \mathcal{F}\left\{h_\mathrm{d}(t)\right\} \;=\; \sum_{i=1}^{k} B\,\sin\left[2\pi f_\mathrm{o}(iT_\mathrm{s})\right] \times \mathcal{F}\left\{\delta\left(t - iT_\mathrm{s}\right)\right\} \tag{3.25}$$

Substituting for the Fourier transform of the time shifted delta function from the Fourier transform identities found in [CF48, Kam04], we obtain

$$H_\mathrm{d}(f) \;=\; e^{-j2\pi T_\mathrm{s} f} \times \sum_{i=1}^{k} B\,\sin\left[2\pi f_\mathrm{o}(iT_\mathrm{s})\right] \times e^{-j2\pi(i-1)T_\mathrm{s} f} \tag{3.26}$$

Note that the term $e^{-j2\pi T_\mathrm{s} f}$ time-shifts the FIR filter output by $T_\mathrm{s}$. Thus, we can drop $e^{-j2\pi T_\mathrm{s} f}$ from the definition of $H_\mathrm{d}(f)$ without affecting the zeros of the transfer function. Then, using Eq. 3.15 to rewrite Eq. 3.26 as a function of $z$ gives

$$H_\mathrm{d}(z) \;=\; \sum_{i=1}^{k} B\,\sin\left[2\pi f_\mathrm{o}(iT_\mathrm{s})\right]\, z^{-(i-1)} \tag{3.27}$$

The $z$ domain representation of the transfer function given in Eq. 3.27 is used to implement the FIR filter. According to the $k$-tap FIR filter architecture illustrated in Fig. 3.4, the transfer function of the FIR filter can be defined as follows:

$$H_\mathrm{d}(z) \;=\; \sum_{i=1}^{k} w_i\, z^{-(i-1)} \tag{3.28}$$

By comparing Eq. 3.28 with Eq. 3.27, we define the scaling factors required in the FIR filter as

$$w_i \;=\; B\,\sin\left[2\pi f_\mathrm{o}(iT_\mathrm{s})\right] \tag{3.29}$$

Substituting for $T_\mathrm{s}$ from Eq. 3.22 gives

$$w_i \;=\; B \times \sin\left(\frac{i\pi}{k+1}\right) \tag{3.30}$$

In conclusion, this subsection described digital harmonic-cancelling sine-wave synthesis as a technique in which a $k$-tap FIR filter with sampling period $T_\mathrm{s}$ is used to filter a square-wave signal with period $T_\mathrm{o}$ to produce a sine-wave signal with period $T_\mathrm{o}$. The harmonics canceled have been delineated using the transfer function of the FIR filter. The required sampling period of the FIR filter has been specified in Eq. 3.22, while the scaling factors needed in the FIR filter have been defined in Eq. 3.30.

### 3.2.3 FIR Filter for Square-Waves - Frequency Domain Approach

In this subsection, we use $z$ domain techniques to elucidate the FIR filter based approach to describing digital harmonic-cancelling sine-wave synthesis. Let us reconsider the $k$-tap FIR filter illustrated in Fig. 3.4 from a frequency domain perspective. The purpose of the FIR filter is to process a square-wave signal of frequency $f_\mathrm{o}$, to produce a sine-wave signal of the same frequency with low harmonic distortion. Let us denote the sampling frequency of the FIR filter by $f_\mathrm{s}$, and define the relationship between $f_\mathrm{s}$ and $f_\mathrm{o}$ by

$$f_\mathrm{s} \;=\; (2k+2)f_\mathrm{o} \tag{3.31}$$

Please note that any variables reused in this subsection carry their original definitions, unless specified otherwise.

Figure 3.7 illustrates the frequency spectrums of the input signal and the desired output signal of the FIR filter. The frequency spectrum of $\phi_1(t)$, which is the input signal provided to the FIR filter, is defined by

$$\Phi_1(f) \;=\; \mathcal{F}\left\{\phi_1(t)\right\} \;=\; \sum_{m=-\infty}^{\infty} \frac{\left[1-\cos\left(m\pi\right)\right]}{m\pi j} \times \delta\left(f - mf_\mathrm{o}\right) \tag{3.32}$$

where $m \in \{x \mid x \in \mathbb{Z},\ x \neq 0\}$. Please refer to Appendix A for a derivation of the Fourier transform of $\phi_1(t)$. In Eq. 3.32, $[1 - \cos(m\pi)] = 0$ for even values of $m$. Thus, $\Phi_1(f)$ only contains odd harmonics of $f_o$, as illustrated in Fig. 3.7.

The FIR filter should cancel the odd order harmonics which exist in the square-wave signal to produce a sine-wave signal. To eliminate a given harmonic of the input signal, the transfer function of the FIR filter should contain a zero at the relevant harmonic frequency.

Let us consider the FIR filter transfer function in the $z$ domain, where $z$ is defined as follows:

$$z = e^{j2\pi f/f_s} \tag{3.33}$$

The harmonics of $f_o$, when mapped to the $z$ domain, constitute the zeros of $\left[1 - z^{-(2k+2)}\right]$, as illustrated in Fig. 3.8. By extension, the odd harmonics of $f_o$, which are of interest to us, constitute the zeros of $\left[1 + z^{-(k+1)}\right]$. However, we can-

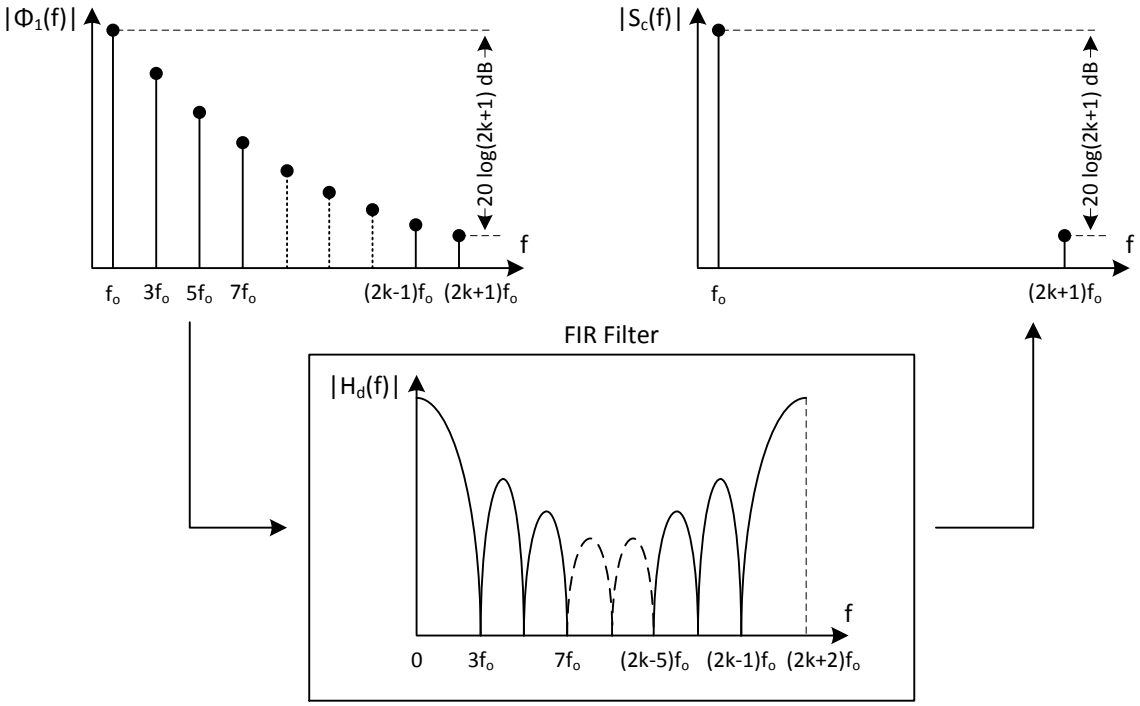


Figure 3.7: Harmonic cancelling via an FIR filter

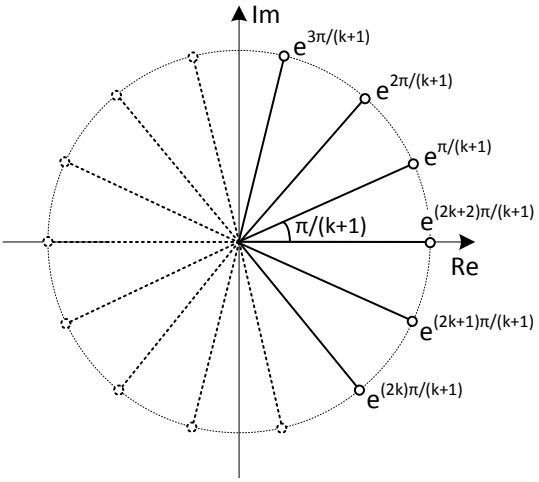


Figure 3.8: Harmonics in the $z$ domain - $(2k+2)^{\text{th}}$ roots of unity

not define the FIR filter transfer function by $\left[1+z^{-(k+1)}\right]$, because $\left[1+z^{-(k+1)}\right]$ also contains a zero at $f_{\text{o}}$, which is the frequency of the sine-wave we desire to produce. In order to remove the zero at $f_{\text{o}}$, $\left[1+z^{-(k+1)}\right]$ should be divided by $\left[1-z^{-1}\,e^{\,j\pi/(k\,+\,1)}\right]$. As the transfer function of the FIR filter needs to consist of real coefficients, we need to divide $\left[1+z^{-(k+1)}\right]$ by $\left[1-z^{-1}\,e^{\,-\,j\pi/(k\,+\,1)}\right]$ as well. Thus, we define the transfer function of the FIR filter as

$$H_{\text{d}}(z) \;=\; \frac{1+z^{-(k+1)}}{\left[1-z^{-1}\,e^{\,j\pi/(k\,+\,1)}\right]\left[1-z^{-1}\,e^{\,-\,j\pi/(k\,+\,1)}\right]} \tag{3.34}$$

Note that diving by $\left[1+z^{-1}\,e^{\,-\,j\pi/(k\,+\,1)}\right]$ removes the zero at $(2k+1)f_{\text{o}}$. Thus, the frequency response $H_{\text{d}}(f)$ takes the form illustrated in Fig. 3.7.

As a consequence of $H_{\text{d}}(z)$ having zeros at odd harmonics of $f_{\text{o}}$ from $3f_{\text{o}}$ up to $(2k-1)f_{\text{o}}$, the FIR filter cancels odd harmonic distortions of the square-wave signal from $\text{HD}_3$ up to $\text{HD}_{2k-1}$. Hence, the frequency spectrum of the FIR filter output does not contain lower order harmonics from $\text{HD}_2$ to $\text{HD}_{2k}$ as delineated in Fig. 3.7.

The first harmonic distortion remaining in the frequency spectrum, $S_{\text{c}}(f)$, of the FIR output signal is $\text{HD}_{2k+1}$. As $|H_{\text{d}}(f_{\text{o}})| = |H_{\text{d}}((2k+1)f_{\text{o}})|$, the amplitude of $\text{HD}_{2k+1}$ (in units of dBc) in $S_{\text{c}}(f)$ remains equal to the amplitude of $\text{HD}_{2k+1}$ (in

units of dBc) in $\Phi_1(f)$. Thus, the amplitude of $\mathrm{HD}_{2k+1}$ is derived as follows:

$$\mathrm{HD}_{2k+1} \;=\; 20\log\left|\frac{\Phi_1\left[(2k+1)f_\mathrm{o}\right]}{\Phi_1(f_\mathrm{o})}\right| \;\mathrm{dBc} \;=\; -\,20\log\left(2k+1\right)\;\mathrm{dBc} \tag{3.35}$$

The transfer function $H_\mathrm{d}(z)$ cannot be used to implement the FIR filter in its current form given in Eq. 3.34. The definition of $H_\mathrm{d}(z)$ can be simplified down to the standalone polynomial given below

$$H_\mathrm{d}(z) \;=\; \sum_{i=1}^{k} w_i\, z^{-(i-1)} \tag{3.36}$$

where

$$w_i = B \times \sin\left(\frac{i\pi}{k+1}\right) \tag{3.37}$$

and $i \in \{x \mid x \leq k,\ x \in \mathbb{Z}^+\}$. A mathematical proof that Eq. 3.36 can be obtained starting from Eq. 3.34 has been provided in [Dav69]. In Appendix A we present an alternative proof, where Eq. A.34 and Eq. A.35 correspond to Eq. 3.37 and Eq. 3.36, respectively. The FIR filter can be implemented using the standalone polynomial form of the transfer function delineated by Eq. 3.36 and Eq. 3.37.

In conclusion, this subsection construes digital harmonic-cancelling sine-wave synthesis as a method of filtering a square-wave signal with frequency $f_\mathrm{o}$, using a $k$-tap FIR filter with sampling frequency $f_\mathrm{s}$, to produce a sine-wave with frequency $f_\mathrm{o}$. In particular, this subsection describes the theory behind the required FIR filter by considering the placement of zeros in the transfer function of the FIR filter. The relationship required between $f_\mathrm{o}$, $f_\mathrm{s}$, and $k$ is defined in Eq. 3.31, while the filter transfer function and coefficients are given by Eq. 3.36 and Eq. 3.37, respectively.

In this section, the theory behind digital harmonic-cancelling sine-wave synthesis has been described from three viewpoints: as a technique for synthesizing sampled continuous-time sine-waves; as an FIR filter based method, using a time domain approach; and again as an FIR filter based method, using a frequency domain approach. Regardless of how we explain the underlying theory, the operation of a

DHSS involves amplitude scaling and summing a set of time-shifted square-wave signals. By using three different theoretical approaches, this section derives the same definitions for the time shift required between the square-wave signals, and for the square-wave amplitude scaling factors.

## 3.3 Digital Harmonic-Cancelling Sine-Wave Synthesizers

A digital harmonic-cancelling sine-wave synthesizer is an electronic circuit which implements the sine-wave generation technique expounded in Section 3.2. In this section, we propose a hardware architecture for DHSSs, which supports programmability of the output sine-wave signal's phase. Different hardware architectures have been used in previous work related to DHSSs [Dav69, SBT+10, SSS15]. However, all existing DHSS architectures can be represented by the generic diagram shown in Fig. 3.9.

The first stage of a generic DHSS is the square-wave generator, which as the name suggests, produces the set of time-shifted square-wave signals required for sine-wave synthesis. In [Dav69] the square-wave generator took the form of a Johnson counter, which was made up of flip-flop circuits, while ring oscillators were utilized as square-

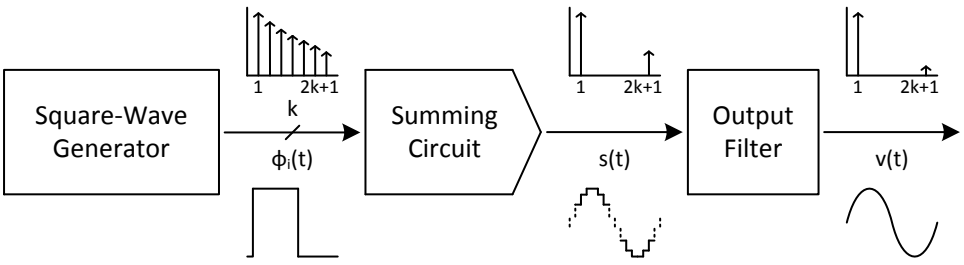


Figure 3.9: Generic DHSS hardware architecture

wave generators in [SBT+10] and [SSS15].

The second stage is the summing circuit, which scales the amplitudes of the square-wave signals and sums them to affect harmonic cancellation. Among the existing DHSS architectures, [Dav69] used an inverting amplifier to implement the summing circuit, [SBT+10] utilized a current-steering circuit, and [SSS15] used a resistor network.

The third stage of a DHSS architecture is the output filter. Note that the output filter is not a part of the harmonic cancelling process. The purpose of the output filter is to reduce the harmonic distortion of the signal produced via digital harmonic-cancelling sine-wave synthesis, by further attenuating the residual harmonics. If the harmonic distortion of the signal generated by the summing circuit is sufficiently low for a given application, then the output filter can be eliminated. The use of an output filter was not discussed in the original publication of a DHSS [Dav69]. In recent work, [SBT+10] and [SSS15] have used passive, RC, low-pass, output filters.

The work by [Dav69, SBT+10, SSS15] were aimed at developing DHSSs to be used as signal synthesizers in electronic circuit testing applications. Thus, the output sine-wave frequency was allowed to be changed. In [Dav69] the output frequency could be tuned by programming the frequency of the reference clock provided to the square-wave generator, while in [SBT+10, SSS15] altering the ring oscillator frequency was the means by which the output frequency was programmed.

One of the primary purposes of this research is to expand the application range of DHSSs to include communication applications. Therefore, *we propose a DHSS with the ability to program the phase as well as the frequency of its output sine-wave signal.*

The DHSS hardware architecture proposed in this thesis is depicted in Fig. 3.10. Similar to [Dav69] a clocked digital logic circuit, which we call the Digital Pattern

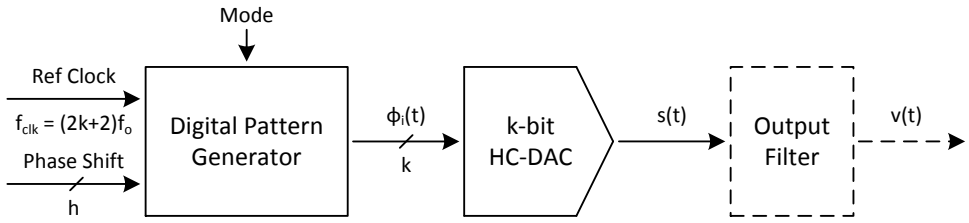


Figure 3.10: DHSS hardware architecture proposed in this thesis

Generator (DPG), is used to generate the square-wave signals. The DPG takes in three digital inputs: the Reference Clock (CLK), the Phase (P), and the Mode (MDE), where CLK runs at a rate of $f_{\text{clk}}$, P is a multi-bit signal, and MDE is a single bit signal. We refer to the summing circuit, which scales and sums $k$ number of square-wave signals, as the $k$-bit Harmonic-Cancelling Digital-to-Analog Converter (HC-DAC). The HC-DAC derives its name from the amplitude scaling and summing operation it performs on its input signals, which is essentially similar to the functionality of a regular DAC. The optional output filter follows the HC-DAC.

The output signal of the HC-DAC, $s(t)$ is defined as follows:

$$s(t) \;=\; \begin{cases} A\sin\left(2\pi f_{\text{o}} t + P + \theta\right) & \text{MDE} = 0 \\ A\sin\left(P\right) & \text{MDE} = 1 \end{cases} \tag{3.38}$$

where $A$ is the amplitude of the sine-wave which depends on the HC-DAC design and $\theta$ describes the initial phase deviation from P at $t = 0$. In Mode Zero (MDE = 0) the DHSS produces a sine-wave signal of frequency $f_{\text{o}}$. The phase of the sine-wave signal is shifted using the digital input P. The frequency of the sine-wave is set by tuning the input clock frequency according to the following equation:

$$f_{\text{o}} \;=\; \frac{f_{\text{clk}}}{2k+2} \tag{3.39}$$

In Mode One the DHSS functions as a sinusoidal digital-to-analog converter (SIN-DAC), which outputs the analog sinusoidal amplitude corresponding to the digital

phase input P. The SIN-DAC operates at a sampling rate of $f_{\text{clk}}$.

The purpose of this section was to introduce the DHSS hardware architecture used in our work. We will take a closer look at the design of the DPG and the HC-DAC blocks of the DHSS architecture in Part II of this thesis.

## 3.4 Potential Applications

Existing work on DHSSs has only focused on test signal synthesis applications [Dav69, SBT+10, SSS15]. In this thesis, we consider three potential applications for DHSSs: as 1) on-chip test-signal synthesizers, 2) PSK polar modulators, and 3) PSK baseband IQ DACs. The last two applications, which are associated with communication systems, are only possible with a DHSS using the phase-programmable hardware architecture proposed in this thesis. The following subsections detail each of the three applications.

### 3.4.1 On-Chip Test Signal Synthesizer

In a system-on-chip project, a major portion of the production cost is allocated to mixed-signal test and verification [PDAO10, MBM15]. The traditional method of chip testing is to create an off-chip test setup, which accesses the individual devices under test (DUTs) inside the SoC and verifies the performance of each DUT. However, as an SoC increases in complexity, it becomes more challenging and costly to provide off-chip access to individual DUTs within the chip. Built-in self-test is a chip testing scheme, where some of the test equipment required to test the chip are built into the SoC itself [HSK93, KKCL95]. Thus, BIST makes the SoC self-testable, simplifies the test procedure, and reduces the production cost related

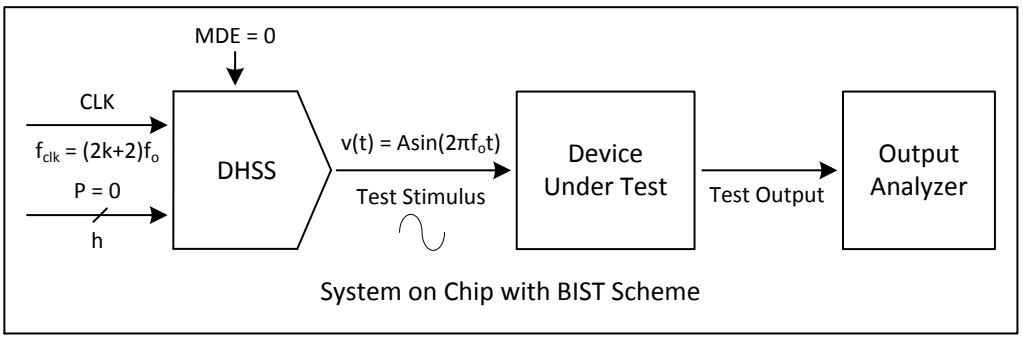


Figure 3.11: Application 1 - on-chip test signal synthesizer

to testing.

An on-chip sinusoidal test signal synthesizer is an essential component of a mixed-signal BIST scheme. Sine-wave synthesizer circuits of different types, including analog feedback oscillators, digital feedback oscillators, DDFSs, as well as harmonic-cancelling sine-wave synthesizers have been proposed to be used in BIST schemes [TLLC05, DADCT06, BVRH06, SBT+10, ESS10, VSCG13, SSS15].

A conceptual diagram of a BIST system, which utilizes the DHSS proposed in this thesis as an on-chip test signal synthesizer, is illustrated in Fig. 3.11. When used as a test signal synthesizer the DHSS must be set to Mode Zero to produce a continuous sine-wave signal. If the phase of the test stimulus is not of interest, P can be adjusted to zero. The frequency of the test stimulus is programmed by changing the input clock frequency according to Eq. 3.39.

Let us briefly discuss the desired characteristics of a DHSS, which is to be used as an on-chip test signal synthesizer. To be suitable for use as a test stimuli generator the DHSS should produce sinusoidal signals with low harmonic distortion. The level of signal-to-distortion ratio expected from the DHSS will depend on the intended linearity of the DUT. As a test signal synthesizer in an SoC is only used when the SoC needs to be evaluated, it is desired that the DHSS occupies a low area in the chip, so that the silicon cost of having a built-in test signal synthesizer is justified.

Finally, the DHSS should meet the frequency bandwidth requirement of the test application. The required frequencies of a test stimulus may defer from one DUT to another, as well as from one test case to another.

### 3.4.2 PSK Polar Modulator

The DHSS hardware architecture proposed in this thesis, which enables phase programmability, opens new doors towards DHSSs being used in PSK communication applications. PSK modulation encodes digital data into the phase of an analog carrier signal. Due to the simplicity of PSK modulation, it is used in low throughput, low power radio standards, such as Bluetooth, ZigBee, and RFID [SGR02, BT110, ZBS11]. PSK modulation is also popularly used in satellite television communication [TAW02, IRS+04, MM06, DVB14].

In a radio transmitter (Tx) a polar modulator is one hardware architecture which can be used to modulate a baseband PSK signal on to a carrier signal. According to existing literature on polar PSK modulators for Bluetooth and ZigBee applications [Gro07, HSW+09, KKYH11, LLF+12, LIYH14], polar modulation of a PSK signal is done using a PLL running at the desired radio frequency (RF). In this thesis, we propose the alternative polar PSK modulator based radio architecture depicted in Fig. 3.12.

In the radio structure illustrated in Fig. 3.12, the two DHSSs are used to polar modulate the baseband PSK signal on to two quadrature intermediate frequency (IF) carriers. Then an image rejection mixer [Vil48, Wea56] is used to up-convert the IF signal to the desired RF signal. The two DHSSs work in Mode Zero in order to produce continuous sine-wave signals. The frequency of the input clock signal provided to the DHSS is decided based on the desired IF ($f_{\mathrm{IF}}$) according to the

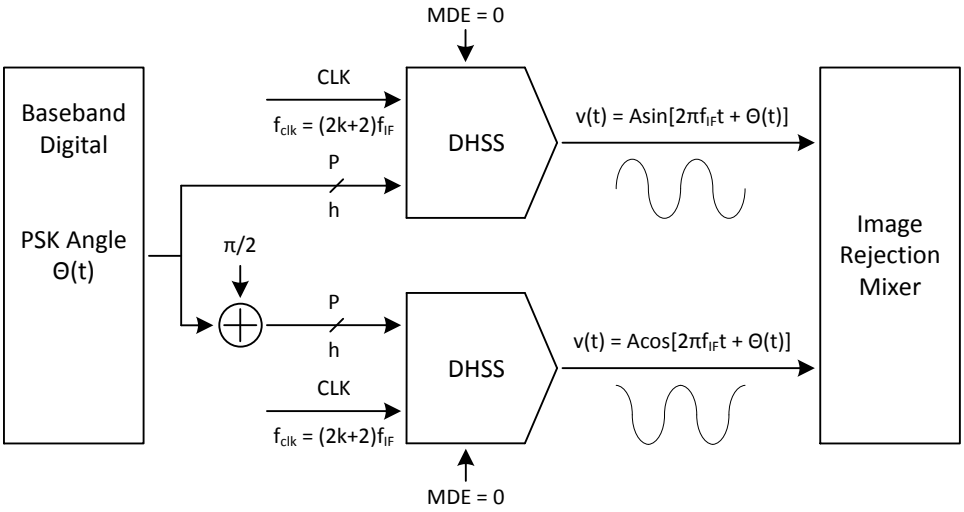


Figure 3.12: Application 2 - PSK polar modulator

following equation:

$$f_{\text{clk}} = (2k+2) \times f_{\text{IF}} \tag{3.40}$$

Each DHSS receives a baseband PSK signal via input P. The baseband PSK input received by one of the DHSSs is phase shifted by $\pi/2$ radians to produce quadrature IF carriers.

The main advantage of using a DHSS as an IF polar modulator, compared to a PLL, is the low harmonic distortion of the DHSS output, which relaxes the linearity requirement of the mixer and the power amplifier stages. To be used as an IF polar modulator, a DHSS should be able to operate at the IF. The IF defers from one radio architecture to another, but the minimum IF which can be used is equal to the channel bandwidth. For example, Bluetooth uses 1 MHz and 2 MHz channel bandwidths [BT110]. The DHSS will also be required to perform phase shift keying with high accuracy in order to attain a low Error Vector Magnitude (EVM) while maintaining low area and power costs.

### 3.4.3 PSK Baseband IQ DAC

A quadrature (IQ) modulator is another hardware architecture which can be used in a Tx to modulate a baseband PSK signal onto a carrier signal [Abi95, CCK+14]. In IQ modulation, the digital baseband PSK signal is converted to analog baseband IQ signals, which subsequently get used by an IQ up-conversion mixer to modulate the desired RF carrier signal. Figure 3.13 illustrates an IQ modulation based radio architecture for modulating PSK signals.

The illustrated radio design utilizes DHSSs as IQ DACs, which convert the digital baseband PSK signal into analog baseband IQ signals. The DHSSs operate in Mode One to function as SIN-DACs. Each DHSS receives a digital baseband PSK angle signal as input P and outputs the corresponding sinusoidal amplitude as an analog signal. An angle of $\pi/2$ radians is added to the digital baseband PSK angle received by one DHSS to produce the quadrature baseband signals. The DHSSs operate at an input clock frequency which is at least equal to the desired baseband frequency ($f_{\mathrm{BB}}$) as defined by the following equation:

$$f_{\mathrm{clk}} \geq f_{\mathrm{BB}} \tag{3.41}$$

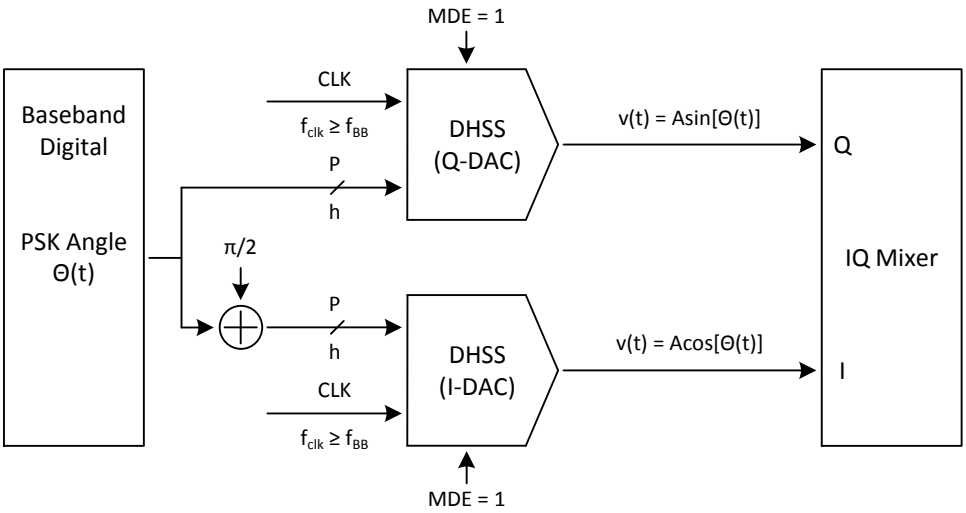


Figure 3.13: Application 3 - baseband IQ DAC for PSK quadrature modulation

The main advantage of using DHSSs as IQ DACs, compared to regular DACs, is the ability of DHSSs to perform better than 6 dB/bit, as discussed in Chapter 5. Thus, DHSSs can make more efficient use of area and power costs compared to conventional DACs. To be used as IQ DACs, the DHSSs should be able to operate at least at the baseband frequency; at a given instance in time the baseband frequency is equal to the channel bandwidth of transmission.

## 3.5 Summary

In this chapter, we had a detailed look at the theoretical background of harmonic-cancelling sine-wave synthesis. In doing so, we have described digital harmonic-cancelling sine-wave synthesis from two distinct perspectives: as a technique for composing a sampled sine-wave signal out of square-wave signals, and as a technique where a square-wave signal is put through an FIR filter to produce a sine-wave signal. While describing the latter perspective, we have used two approaches to derive the FIR filter characteristics; one using time domain techniques and the other using frequency domain techniques. Next, we introduced the DHSS hardware architecture utilized in this research, which supports phase programmability. The DHSS hardware architecture consists of the DPG, the HC-DAC, and the optional output filter. Finally, we proposed the use of DHSSs developed through this work, as on-chip test signal synthesizers, as baseband DACs for PSK communication applications, and as IF polar modulators also for PSK communication.

# Part II

# Designing DHSSs

# Chapter 4

# Digital Pattern Generator

## 4.1 Overview

In this chapter, we focus on the DPG, which is the first block of the DHSS hardware architecture proposed in Section 3.3. First, we present two hardware designs for the DPG; one for DHSSs which do not require phase programmability, and another for DHSSs which require phase programmability. While introducing the hardware designs, the number of square-wave signals ($k$) produced by the DPG is kept as a variable. Next, we discuss how the choice of $k$ affects the DHSS output signal and the DHSS hardware design.

## 4.2 DPG without Phase Programmability

A DPG synthesizes the square-wave signals required to perform the harmonic-cancelling sine-wave synthesis technique. A $k$-bit DPG is illustrated in Fig. 4.1, where $k$ denotes the number of square-wave signals ($\phi_i$) synthesized by the DPG.

CLK is the reference clock signal used by the DPG. MDE is a 1-bit digital signal, which defines whether the DHSS operates as a continuous sine-wave signal synthesizer, or as a SIN-DAC. P is a $h$-bit digital signal, which defines a phase angle.

This section discusses a hardware design for a DPG to be utilized in a DHSS which does not support phase programmability. In such a DPG, inputs P and MDE are unused. Each output signal of the DPG is a continuous square-wave signal of frequency $f_o$, which is also the desired output frequency of the DHSS. As elaborated in Section 3.3, the relationship between the input clock frequency ($f_{clk}$), $f_o$, and $k$ is defined by

$$f_{clk} = (2k + 2) \times f_o \tag{4.1}$$

.

A timing diagram depicting the relationship between the input clock signal and the output square-wave signals is given in Fig. 4.2. By studying the signal traces illustrated in Fig. 4.2, we can conclude that the DPG should be a clock divider circuit, which provides time-shifted versions of the output. In the first article which introduced digital harmonic-cancelling sine-wave synthesis, Davies used a Johnson counter made out of JK flip-flops to implement such a DPG circuit [Dav69]. In this thesis, we use the same concept. However, we implement the Johnson counter with D flip-flops, as illustrated in Fig. 4.3. The Johnson counter is initialised by either setting all the D flip-flops or by resetting all the D flip-flops.

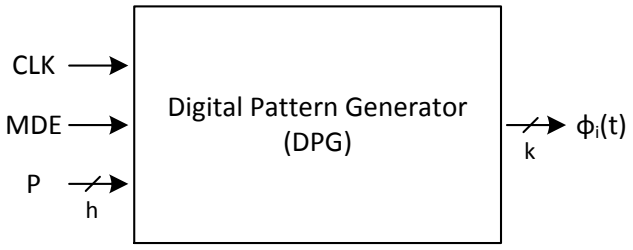


Figure 4.1: A $k$-bit DPG

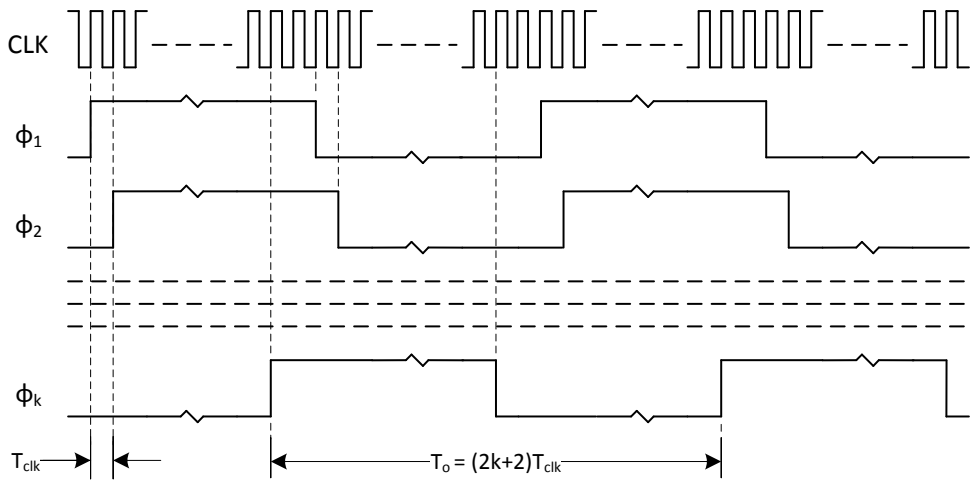


Figure 4.2: Timing diagram of DPG input and output signals

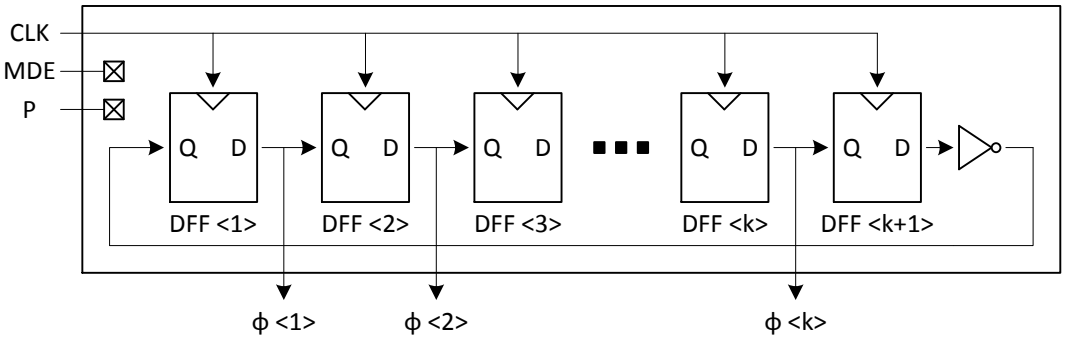


Figure 4.3: Johnson ring counter based $k$-bit DPG hardware design

## 4.3 DPG with Phase Programmability

In this section, we propose a hardware design for a DPG which supports phase programmability. As the concept of phase programmable DHSSs is a contribution of this thesis, so is the DPG hardware design proposed in this section.

Figure 4.4 illustrates the proposed $k$-bit DPG hardware design, where $\Theta$ and $\Theta_a$ are $h$-bit digital signals representing the phase of the sinusoidal signal desired at the output of the DHSS. The Phase-to-Amplitude Converter (PAC) takes in $\Theta$ and outputs the corresponding digital state of each square-wave signal, $\phi_i$. When the DHSS is operating in Mode Zero, $\Theta$ is equal to $\Theta_a$, which is the output of the Phase

Accumulator (PA) circuit. In Mode One, input signal P is passed on as $\Theta$.

The mapping between $\Theta$ and the digital states of the square-wave signals is delineated in Fig. 4.5. A $k$-bit DHSS has a phase resolution of $2k+2$ discrete phase states. Thus, $h$ is given by

$$h = \lceil \log_2 (2k+2) \rceil \tag{4.2}$$

The hardware design of the PAC circuit is shown in Fig. 4.7, in which the mapping between $\Theta$ and the square-wave signal states is implemented via a combinational logic circuit. In the case of a 7-bit DPG with 4-bit phase resolution ($k = 7$, $h = 4$) the logic circuit should implement the following Boolean expressions:

$$\phi_1 = \bar{\Theta}_3 \oplus \left(\bar{\Theta}_2 \cdot \bar{\Theta}_1 \cdot \bar{\Theta}_0\right) \tag{4.3a}$$

$$\phi_2 = \bar{\Theta}_3 \oplus \left(\bar{\Theta}_2 \cdot \bar{\Theta}_1\right) \tag{4.3b}$$

$$\phi_3 = \bar{\Theta}_3 \oplus \left[\bar{\Theta}_2 \cdot \left(\bar{\Theta}_1 + \bar{\Theta}_0\right)\right] \tag{4.3c}$$

$$\phi_4 = \Theta_3 \oplus \Theta_2 \tag{4.3d}$$

$$\phi_5 = \Theta_3 \oplus [\Theta_2 \cdot (\Theta_1 + \Theta_0)] \tag{4.3e}$$

$$\phi_6 = \Theta_3 \oplus (\Theta_2 \cdot \Theta_1) \tag{4.3f}$$

$$\phi_7 = \Theta_3 \oplus (\Theta_2 \cdot \Theta_1 \cdot \Theta_0) \tag{4.3g}$$

The hardware design of the PA is shown in Fig. 4.7. When the DHSS is operating in Mode Zero, the $h$-bit PA output signal, $\Theta_a$ defines the instantaneous phase of

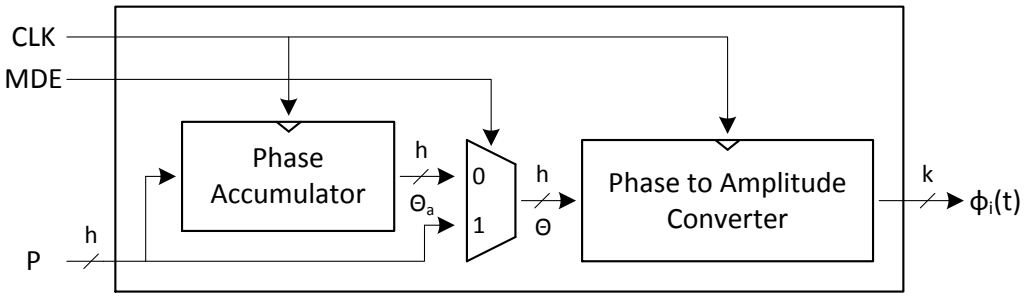


Figure 4.4: Phase programmable $k$-bit DPG hardware design

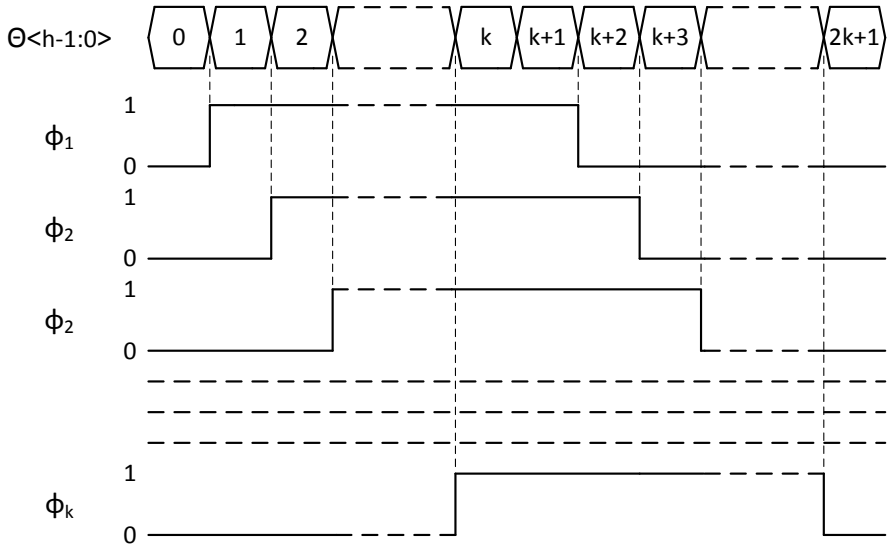


Figure 4.5: PAC input to output mapping

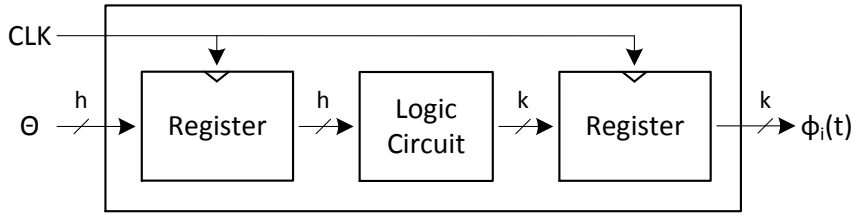


Figure 4.6: PAC hardware design

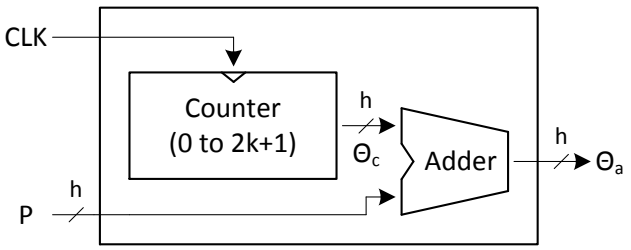


Figure 4.7: PA hardware design

the sinusoidal signal synthesized by the DHSS. The $h$-bit input signal, P, defines the phase offset to be added to the sinusoidal signal. The PA consists of a counter and an adder. The counter outputs the $h$-bit digital word, $\Theta_c$, which loops through

the $2k + 2$ phase states of a continuous sinusoidal signal, while the adder outputs $\Theta_a = (\Theta_c + P) \bmod (2k + 2)$.

## 4.4 Choosing the Number of Square-Waves ($k$)

The number of square-waves ($k$) used in the DHSS has been kept as a variable while presenting the DPG hardware designs in previous sections. The choice of $k$ affects two main features of a DHSS: 1. the number of lower order harmonics cancelled when operating in Mode Zero, and 2. the phase resolution of the output sinusoidal signal produced in either mode.

A $k$-bit DHSS operating in Mode Zero produces a sampled sine-wave, which does not contain lower order harmonics from $HD_2$ to $HD_{2k}$, a theoretical explanation of which was given in Section 3.2. The relationship between phase resolution ($h$) and $k$ was defined in Eq. 4.2. Based on the specifications of a given DHSS and the information given in this section, a designer can choose an appropriate value for $k$.

## 4.5 Summary

We have looked into the design of the DPG in this chapter. Two different designs for the DPG have been presented; one that doesn't support phase programmability, and another that does. The DPG design that doesn't support programmability consists of only a ring counter built with D flip-flop circuits. The phase programmable DPG includes a PA and a PAC, the designs of which have also been presented. Finally, to close out the chapter we looked into how the number of square-wave signals ($k$) used in the DHSS affects the number of eliminated harmonics, and the phase resolution of the DHSS output sine-wave signal. A higher value of $k$ increases the number of

harmonics cancelled and the phase resolution. However, a larger $k$ also adds to the area and power consumptions of the DHSS.

# Chapter 5

# Harmonic-Cancelling Digital-to-Analog Converter

## 5.1 Overview

In this chapter, we discuss the HC-DAC, which is the second block in the DHSS hardware architecture proposed in Section 3.3. The operation of an HC-DAC is to scale the amplitudes of the digital input signals it receives and to sum them together, which is fundamentally similar to the functioning of a conventional DAC. However, while a regular DAC scales its input signals by powers of two, an HC-DAC scales its input signals by a set of amplitude weights defined by a sinusoidal function, as given in Eq. 3.14. *Thus, the conventional knowledge gathered from designing regular DACs does not apply to HC-DACs.*

The rest of this chapter is organized as follows. First, we present the HC-DAC hardware architecture used in this thesis. Next, we analyze the impact of finite amplitude resolution and mismatch on the performance of an HC-DAC. Then, based

on the knowledge of how amplitude resolution affects HC-DAC performance, we show that HC-DACs can be systematically designed to break the 6 dB/bit rule. Finally, we analyze the effect of timing non-idealities on HC-DAC performance.

## 5.2 Hardware Architecture

Let us denote the square-wave input signals received by a generic HC-DAC by $\phi_i(t)$, where $i \in \{x \mid x \leq k,\ x \in \mathbb{Z}^+\}$. An expression for $\phi_i(t)$ can be given as follows:

$$\phi_i(t) = \phi_1\left(t - \frac{(i-1)T_o}{2k+2}\right) \tag{5.1}$$

where $\phi_1(t)$ was previously defined in Eq. 3.16, and $T_o$ is the period of the square-wave signals as well as the desired sine-wave signal. The purpose of an HC-DAC is to scale the amplitude of each input signal $\phi_i(t)$ by an amplitude weight of $w_i$, which was defined in Eq. 3.14, and sum the resulting signals together. Thus, the ideal output signal of an HC-DAC is given by:

$$s(t) = \sum_{i=1}^{k} w_i \times \phi_i(t) \tag{5.2}$$

In Section 3.2, it was theoretically proven that $s(t)$ does not contain lower order harmonic distortion up to and including $HD_{2k}$.

In the first publication of a DHSS circuit, Davies [Dav69] suggested the use of a summing amplifier with scaled resistor values to implement the HC-DAC circuit. Since then, [SBT+10] proposed the use of a current-steering circuit with scaled current switches, and [SSS15] proposed the use of a resistor network with weighted resistors to implement the HC-DAC. A common drawback of previous approaches is the use of scaled circuit components, as opposed to unit-circuit-elements. The use of unit-elements can improve the amplitude scaling accuracy of an HC-DAC in

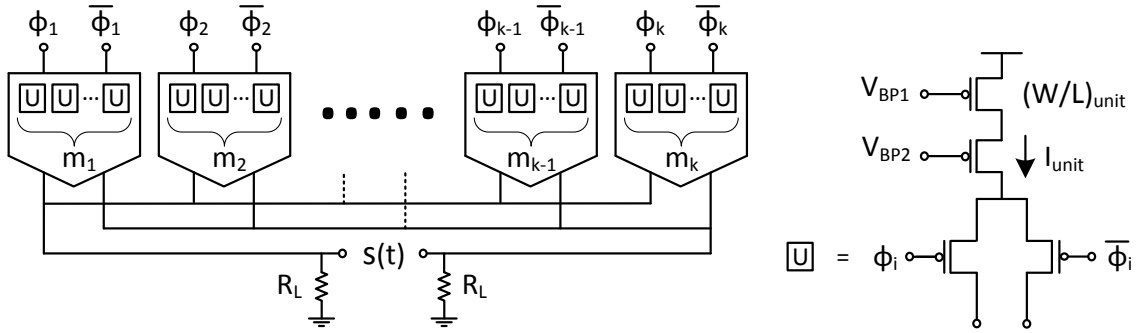


Figure 5.1: Hardware architecture of the HC-DAC

the presence of circuit mismatch. Moreover, the use of unit-elements aides us to systematically define the hardware cost of the circuit.

The hardware architecture employed in this work to implement a generic $k$–bit HC-DAC is shown in Fig. 5.1. As shown, we use a current steering architecture based on unit-current switches, where each input signal $\phi_i$ controls an $m_i$ number of unit-current switches. Depending on the state of $\phi_i$, the total current from the set of $m_i$ number of unit-current switches is directed into one of the two differential current output paths. Thus, $m_i$ represents the scaling factor by which the amplitude of signal $\phi_i$ is scaled in the HC-DAC operation.

Let us denote the total number of unit-current switches used in an HC-DAC by $M$. In this work, we also use $M$ as the measure of amplitude resolution of the HC-DAC. While choosing a higher value for $M$ improves the amplitude resolution of the HC-DAC, a higher value of $M$ also results in increased area and power consumptions. Thus, choosing the required minimum value of $M$ for a given HC-DAC design is critical. Once a value for $M$ is selected, unit-current switches can be allocated to each input signal by choosing $m_i$ according to the following equations:

$$o_i = \left\lfloor \frac{w_i \times M}{\sum_{l=1}^{k} w_l} + \frac{1}{2} \right\rfloor \tag{5.3}$$

$$m_i = \begin{cases} o_i & i \neq \lceil \frac{k}{2} \rceil \\ o_i + \left( M - \sum_{l=1}^{k} o_l \right) & i = \lceil \frac{k}{2} \rceil \end{cases} \tag{5.4}$$

which ensure $\sum_{i=1}^{k} m_i = M$, while reducing signal scaling error.

## 5.3 Effect of Amplitude Resolution and Mismatch

### 5.3.1 Ideal HC-DAC vs. Non-Ideal HC-DAC

An ideal HC-DAC outputs the signal $s(t)$, as defined in Eq. 5.2. However, a practical HC-DAC with non-ideal characteristics is only capable of producing an approximation to $s(t)$. Let us denote the output signal of a non-ideal HC-DAC by $s_{\text{ni}}(t)$.

Figure 5.2 depicts the output signal spectrums of an ideal HC-DAC and a non-ideal HC-DAC, where $S(f)$ and $S_{\text{ni}}(f)$ are the frequency spectrums of $s(t)$ and $s_{\text{ni}}(t)$, respectively. As theoretically proven in Section 3.2, $S(f)$ does not contain lower order harmonic distortions from $\text{HD}_2$ to $\text{HD}_{2k}$. In $S_{\text{ni}}(f)$, $\text{HD}_2$ to $\text{HD}_{2k}$ are attenuated, but not completely eliminated. In contrast, $\text{HD}_{2k+1}$ will remain at

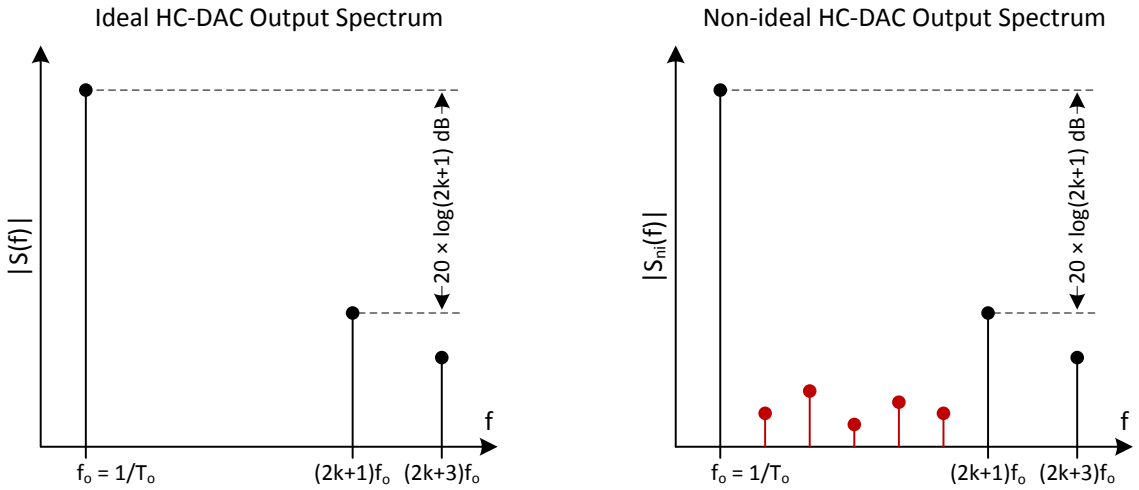


Figure 5.2: Ideal HC-DAC output vs. non-ideal HC-DAC output

$20 \times \log(2k+1)$ dBc in both ideal and non-ideal HC-DACs, as shown in Fig. 5.2. $\mathrm{HD}_{2k+1}$ can be perceived as an image frequency created by the HC-DAC, while synthesizing a sine-wave signal of frequency $f_\mathrm{o}$, using a set of square-wave signals sampled at a clock frequency of $(2k+2) \times f_\mathrm{o}$. Considering the information above, we define the signal-to-distortion ratio and the spurious free dynamic range (SFDR) in the following equations, as measures of the amount of harmonic cancellation attained from an HC-DAC.

$$\mathrm{SDR} = \frac{|S_\mathrm{ni}(f_\mathrm{o})|^2}{\sum_{n=2}^{2k} |S_\mathrm{ni}(nf_\mathrm{o})|^2} \tag{5.5}$$

$$\mathrm{SFDR} = \frac{|S_\mathrm{ni}(f_\mathrm{o})|^2}{\max_{n=2}^{2k} |S_\mathrm{ni}(nf_\mathrm{o})|^2} \tag{5.6}$$

where $f_\mathrm{o} = 1/T_\mathrm{o}$, is the fundamental frequency of the sampled sine-wave signal synthesized by the HC-DAC. In this thesis, we will focus more on the SDR of HC-DACs, as the SDR accounts for the accumulated power of all harmonic distortions from $\mathrm{HD}_2$ to $\mathrm{HD}_{2k}$.

### 5.3.2 Non-Ideal Characteristics

The non-ideal characteristics associated with a practical HC-DAC can be categorized into two groups. They are amplitude scaling errors and timing errors. In this section, we focus on amplitude scaling errors.

The two causes of amplitude scaling errors in a practical HC-DAC are finite amplitude resolution (or finite availability of unit-elements) and mismatch between unit-elements. From Eq. 3.14 it can be noted that most amplitude scaling factors required to be implemented by a given HC-DAC will be irrational. Thus, to implement an HC-DAC with 100% amplitude scaling accuracy, the amplitude resolution of the HC-DAC must be infinite, or in other words, the total number of unit-current

switches used in the HC-DAC must be infinite. Hence, an HC-DAC implemented with any finite value for $M$ will suffer from amplitude scaling errors, and mismatch between unit-current switches will make the errors worse. Such amplitude scaling errors translate into residual harmonic distortion at the HC-DAC output.

As mentioned previously, minimizing the amplitude resolution is essential when designing an area and power cost effective HC-DAC. In order to do so, the designer must understand how the amplitude resolution of a given HC-DAC affects the SDR of the HC-DAC output signal. The mismatch between unit-elements of an HC-DAC can be reduced by increasing the area of the unit-elements. However, larger unit-elements swell the area cost of an HC-DAC. Thus, a designer must understand how mismatch affects the SDR of an HC-DAC in order to find the minimum tolerable mismatch level. In the following discussion, this thesis builds up a mathematical model which describes the relationship between the amplitude resolution and mismatch of a generic $k$–bit HC-DAC, and the SDR of the HC-DAC.

### 5.3.3 Mathematical Modelling

Consider a $k$–bit HC-DAC that has an amplitude resolution of $M$. Let $I_{\mathrm{u}}(i,l)$ denote the current flowing through the $l^{\mathrm{th}}$ unit-current switch controlled by input signal $\phi_i$, where $l \in \{x \mid x \leq m_i,\ x \in \mathbb{Z}^+\}$. With no mismatch, each unit-current switch conducts the same current, $I_{\mathrm{u}}(i,l) = I_{\mathrm{unit}}$, as shown in Fig. 5.1. In an HC-DAC affected by mismatch, $I_{\mathrm{u}}(i,l)$ can be expressed as

$$I_{\mathrm{u}}(i,l) = I_{\mathrm{unit}} + E_{\mathrm{u}}(i,l) \tag{5.7}$$

where $E_{\mathrm{u}}(i,l)$ is the current mismatch error in the $l^{\mathrm{th}}$ unit-current switch controlled by input signal $\phi_i$. Let us assume that the mismatch error is modelled by a Gaussian normal distribution, with zero mean and a standard deviation of $\sigma$. Then, $E_{\mathrm{u}}(i,l)$

can be expressed as follows:

$$E_{\mathrm{u}}(i,l) \sim \mathcal{N}\left(0,\sigma^2\right) \tag{5.8}$$

Based on Eq. 5.7, the total current switched by each input signal $\phi_i$, denoted by $I_{\mathrm{ni}}(i)$, is given as follows:

$$I_{\mathrm{ni}}(i) = \sum_{l=1}^{m_i} I_{\mathrm{u}}(i,l) \tag{5.9}$$

In the HC-DAC architecture shown in Fig. 5.1, each input signal $\phi_i$ is effectively scaled by a factor of $R_{\mathrm{L}} \times I_{\mathrm{ni}}(i)$. Thus, the non-ideal HC-DAC output, $s_{\mathrm{ni}}(t)$, is defined by,

$$s_{\mathrm{ni}}(t) = \sum_{i=1}^{k} R_{\mathrm{L}} \times I_{\mathrm{ni}}(i) \times \phi_i(t) \tag{5.10}$$

Using Eq. 5.10, the complex Fourier coefficient of the $n^{th}$ harmonic of $s_{\mathrm{ni}}(t)$ can be derived to be as given below.

$$S_{\mathrm{ni}}(nf_{\mathrm{o}}) = \frac{R_{\mathrm{L}} \times [1-\cos(n\pi)]}{n\pi j} \times \sum_{i=1}^{k} I_{\mathrm{ni}}(i) \times \exp\left[\frac{n\pi j}{k+1} \times (1-i)\right] \tag{5.11}$$

Please refer to Appendix B for a derivation of Eq. 5.11. The expression for $S_{\mathrm{ni}}(nf_{\mathrm{o}})$ provided in Eq. 5.11 is used to calculate the SDR of a given HC-DAC according to Eq. 5.5. Thus, the combination of equations, Eqns. 5.3–5.11, model the relationship between amplitude resolution ($M$), mismatch ($\sigma$), and SDR of a generic $k$–bit HC-DAC.

### 5.3.4 Breaking the 6 dB/bit Rule

Several key characteristics of the relationship between finite amplitude resolution and mismatch, and SDR of an HC-DAC can be understood through the mathematical model defined in the previous section. In order to evaluate the model, a MATLAB script was written based on Eqns. 5.3–5.11 to calculate the SDR, given a

set of values for $k$, $M$, and $\sigma$. Let us first concentrate on the relationship between amplitude resolution and SDR. For this purpose, mismatch was set to zero by making $\sigma = 0$ in the model. The variation of SDR against $M$ of a 4–bit HC-DAC ($k = 4$) and a 7–bit HC-DAC ($k = 7$) are plotted in Fig. 5.3 and Fig. 5.4, respectively.

As the linear fit to the data in each figure indicates, the average variation of SDR against $M$ happens at a rate of 6 dB/bit. This observation is consistent with the '6 dB/bit rule', first proposed in [Ben48], which is commonly used to estimate the signal-to-quantization-noise ratio in conventional DACs. However, it is also evident from Fig. 5.3 and Fig. 5.4 that the value of SDR varies significantly against $M$ around the 6 dB/bit estimated value. Consequently, it is clear that a carefully informed decision should be made regarding the value $M$ to achieve a given SDR target while minimizing $M$.

A critical information which can be gathered from Fig. 5.3 and Fig. 5.4 is that a higher value of $M$ does not always result in a higher SDR. The Pareto Front highlighted in each figure is a unique subset of data points for which a higher value of $M$ always results in a higher SDR.

The existence of such a Pareto Front with high SDR can be understood as follows. As previously noted, the signal amplitude weights used in an HC-DAC are mostly irrational. Thus, no finite value of $M$ can result in an HC-DAC with 100% scaling accuracy. However, for certain values of $M$, local maxima occur in the scaling accuracy of the HC-DAC, which create the Pareto Front. The exact values of $M$ at which the local maxima in accuracy occur depend on the scaling factors used in the HC-DAC, and consequently, the value of $k$.

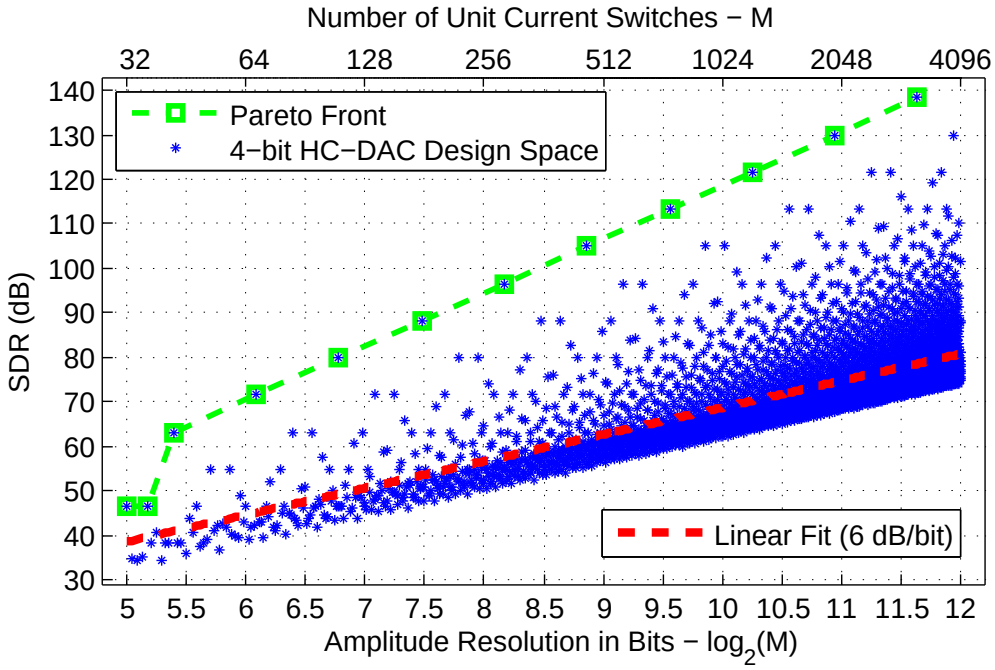


Figure 5.3: SDR against amplitude resolution of a 4–bit HC-DAC

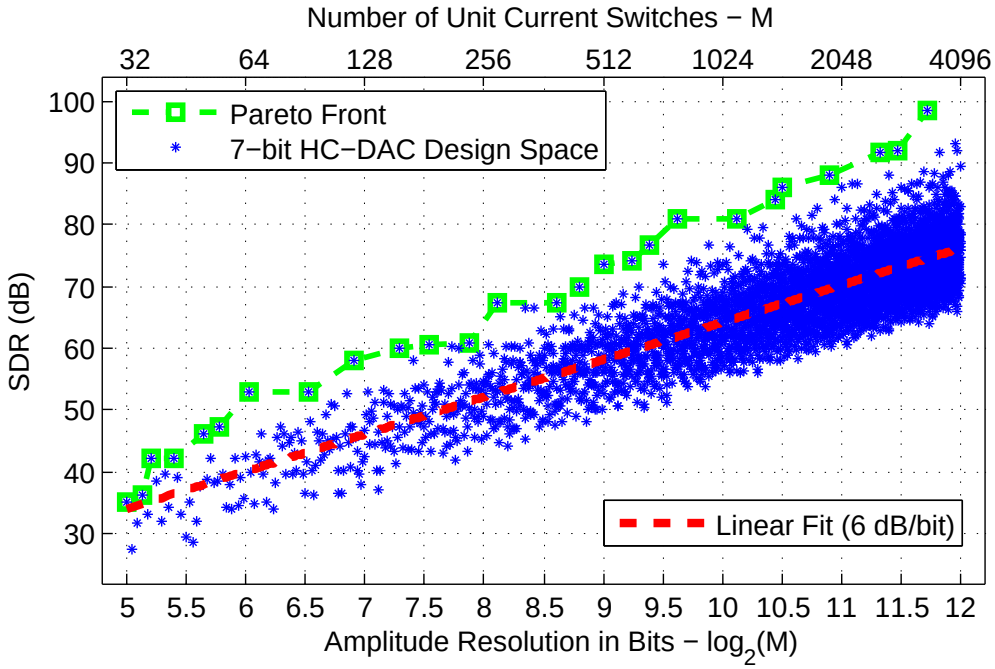


Figure 5.4: SDR against amplitude resolution of a 7–bit HC-DAC

It is important to note that in each design space the Pareto Front lies significantly higher in the SDR scale compared to the 6 dB/bit linear fit. Thus, the Pareto Front in the design space of a given HC-DAC allows the HC-DAC to break the '6 dB/bit rule'. Consequently, a DHSS with an HC-DAC which breaks the '6 dB/bit rule' can be designed to be more area and power cost-efficient, compared to a DDFS, which uses a regular DAC governed by the '6 dB/bit rule'. Performance comparison between DHSSs and DDFSs is discussed further with measurement results in Chapter 8.

A Pareto optimal method for designing an HC-DAC by utilizing the Pareto Front in its design space is described as follows. Consider a designer who is given the value of $k$, and asked to find the minimum amplitude resolution required for a $k$–bit HC-DAC with a minimum signal-to-distortion ratio of $\mathrm{SDR}_{\mathrm{min}}$. Such a designer should first use the mathematical model presented in this thesis to find the Pareto Front associated with the design space of the given HC-DAC. Then, if the Pareto Front design points are sorted in ascending order of SDR, the first design point to result in a higher signal-to-distortion ratio than $\mathrm{SDR}_{\mathrm{min}}$ provides the solution to the design problem.

### 5.3.5 Effect of Mismatch on the Design Spaces

Let us now take into account the impact of unit-current switch mismatch on the relationship between SDR and amplitude resolution using the following approach. For each set of given values for $k$, $M$, and $\sigma$, a Monte Carlo simulation with $10,000$ iterations was conducted. Results of the Monte Carlo simulation were used to construct a statistical distribution of SDR. Then, the lower bound of SDR with a 90% yield ($\mathrm{SDR}_{90\%}$) was noted down from the statistical distribution.

For $\sigma$ values of 0%, 0.5%, and 1%, Fig. 5.5 and Fig. 5.6 plot the Pareto Fronts

and Linear Fits associated with the relationship between $SDR_{90\%}$ and $M$ in a 4-bit HC-DAC, and a 7-bit HC-DAC, respectively. Both figures illustrate that even at $\sigma = 1\%$, design points in the Pareto Front result in significantly higher SDRs compared to the Linear Fit. Thus, it is evident that identifying the Pareto Front in a given HC-DAC design space is a critical step in designing area and power efficient HC-DACs.

The characteristics of the relationship between SDR and $M$ discussed above are consistent with all values of $k$, even though the above discussion is based on a 4–bit HC-DAC and a 7–bit HC-DAC. Please refer to Appendix B for plots of SDR against $M$ of HC-DACs from 3–bit to 14–bit input bit-width.

### 5.3.6 Application to Circuit Design

Two DHSS design examples are used when discussing various aspects of DHSSs throughout this thesis. One is a 4–bit DHSS with an HC-DAC designed using 110 unit-current switches (6.8–bit amplitude resolution), and the other is a 7–bit DHSS with an HC-DAC designed using 37 unit-current switches (5.2–bit amplitude resolution). In each DHSS, the amplitude resolution of the HC-DAC has been chosen using the Pareto optimal design method established in this section.

According to Fig. 5.3, a 4–bit HC-DAC with 6.8–bit amplitude resolution is a Pareto optimal design, which will result in an SDR of 79.9 dB. Also, according to Fig. 5.4, a 7–bit HC-DAC with 5.2–bit amplitude resolution is a Pareto optimal design, which will result in an SDR of 42.1 dB. To verify that the SDR predicted by the mathematical model presented in this section agrees with circuit simulations, each HC-DAC circuit was designed and simulated in Cadence 5.10.41 using an STMicroelectronics 130 nm CMOS technology.

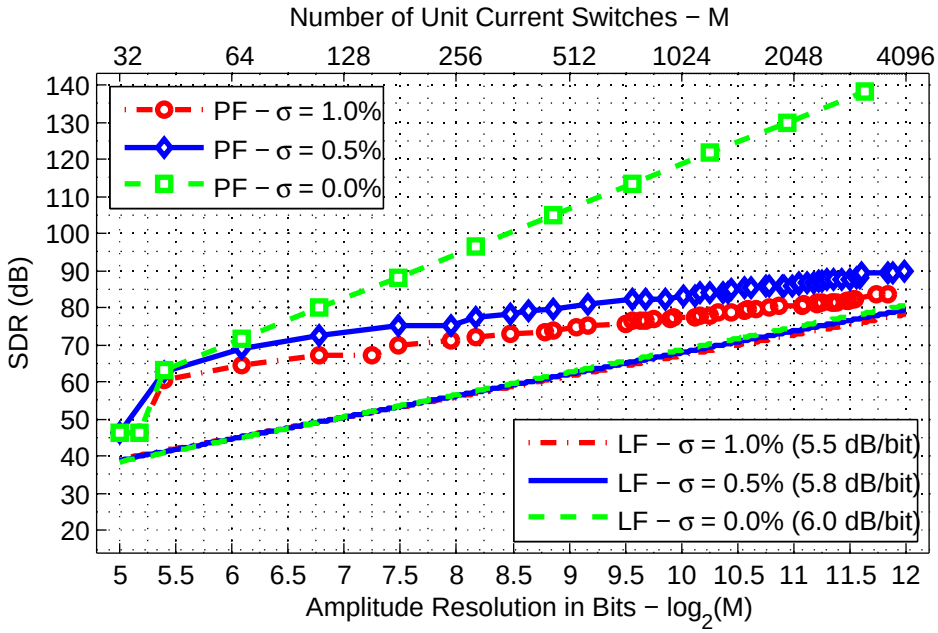


Figure 5.5: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 4-bit HC-DAC

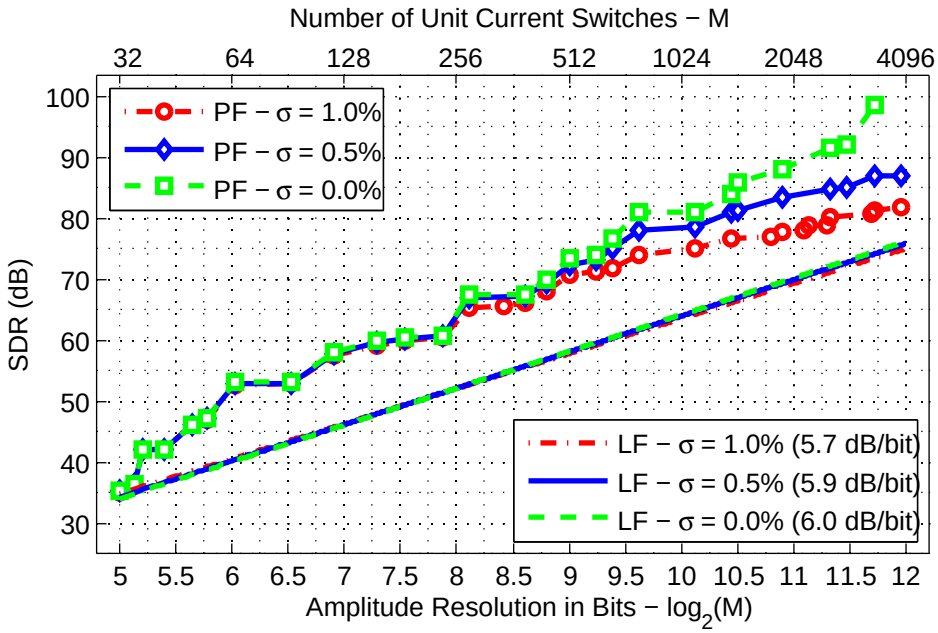


Figure 5.6: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 7-bit HC-DAC

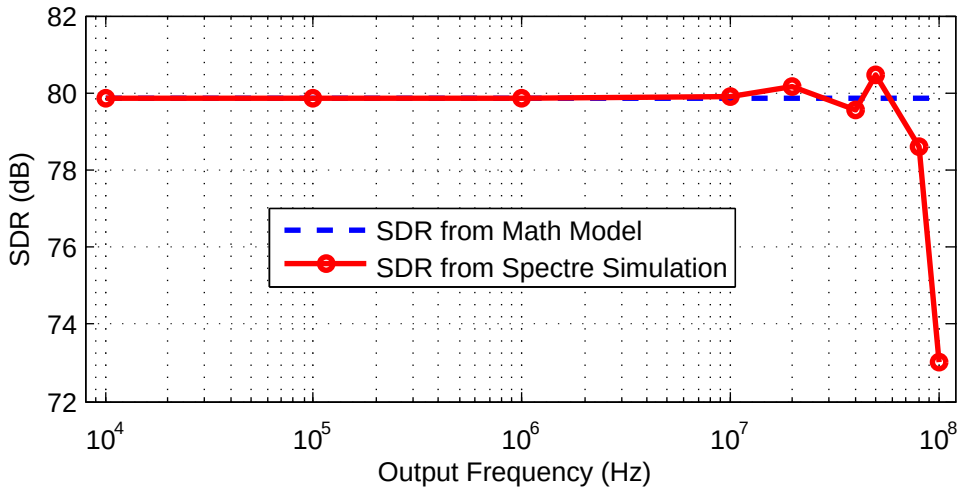


Figure 5.7: Frequency sweep of SDR of a 4-bit HC-DAC with 110 unit-current switches

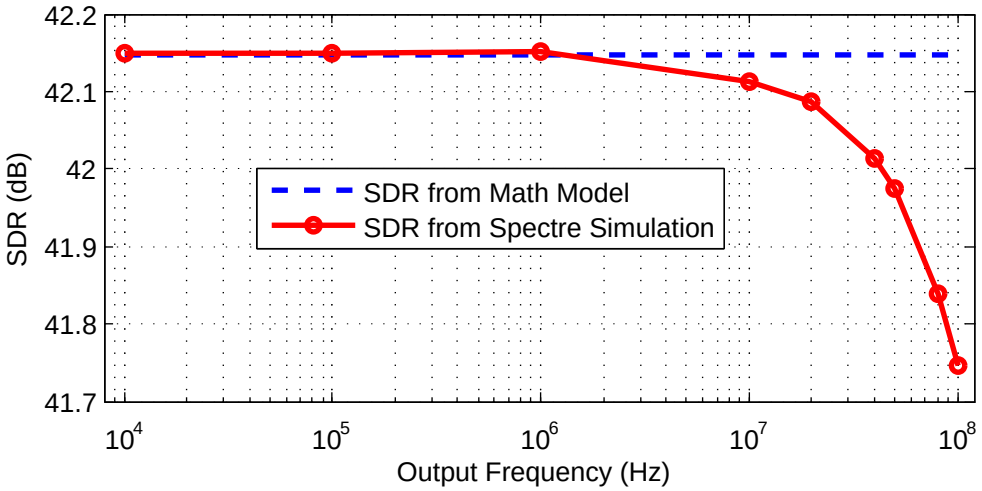


Figure 5.8: Frequency sweep of SDR of a 7-bit HC-DAC with 37 unit-current switches

Figure 5.7 and Fig. 5.8 plot circuit simulation results for frequency sweeps of SDR of the 4–bit HC-DAC design, and the 7–bit HC-DAC design, respectively. In each plot, at lower frequencies, the circuit simulation results for SDR agree with the SDR result predicted by the mathematical model. At higher frequencies, timing errors become more prominent, which causes the circuit simulation results for SDR to decrease. In the next section, we elaborate on the impact of timing errors.

## 5.4 Effect of Timing Non-Idealities

### 5.4.1 Defining Timing Non-Idealities

The theory of harmonic-cancelling sine-wave synthesis as considered thus far, assumes the availability of an ideal set of square-waves, with precise phases and zero transition times. Needless to say, it is impossible to synthesize such square-waves with ideal timing characteristics. Therefore, it is important to look into the impact of timing errors on the output of an HC-DAC.

First, let us define the two categories of timing errors considered in this thesis. Figure 5.9 illustrates an ideal square-wave ($\phi_i(t)$), as defined in Eq. 5.1, and its timing error affected counterpart, $\hat{\phi}_i(t)$. As illustrated, $\hat{\phi}_i(t)$ suffers from a time-shift error of $\Delta t(i)$, a rise time of $t_{\mathrm{r}}(i)$, and a fall time of $t_{\mathrm{f}}(i)$. Time-shift errors in square-wave signals are caused by differences in the delay experienced by each square-wave, from the last set of D flip-flops which clock the square-waves to the input of the HC-DAC. Non-zero transition times in the square-wave signals are inevitable, as it takes a finite time to charge and discharge the parasitic capacitors present in the circuit.

The complex Fourier coefficients of $\hat{\phi}_i$ can be expressed as follows:

$$\hat{\Phi}_i(nf_{\mathrm{o}}) = \left(\frac{T_{\mathrm{o}}}{2n^2\pi^2}\right) e^{\left[\frac{n\pi j}{k+1}(1-i)-2n\pi j\frac{\Delta t(i)}{T_{\mathrm{o}}}\right]} \left[\frac{1}{t_{\mathrm{r}}(i)}\left(1-e^{-2n\pi j\frac{t_{\mathrm{r}}(i)}{T_{\mathrm{o}}}}\right) - \frac{e^{n\pi j}}{t_{\mathrm{f}}(i)}\left(1-e^{-2n\pi j\frac{t_{\mathrm{f}}(i)}{T_{\mathrm{o}}}}\right)\right] \tag{5.12}$$

Please refer to Appendix B for a derivation of Eq. 5.12. Using the knowledge from Section 5.3, the HC-DAC output signal in the presence of time erred square-wave

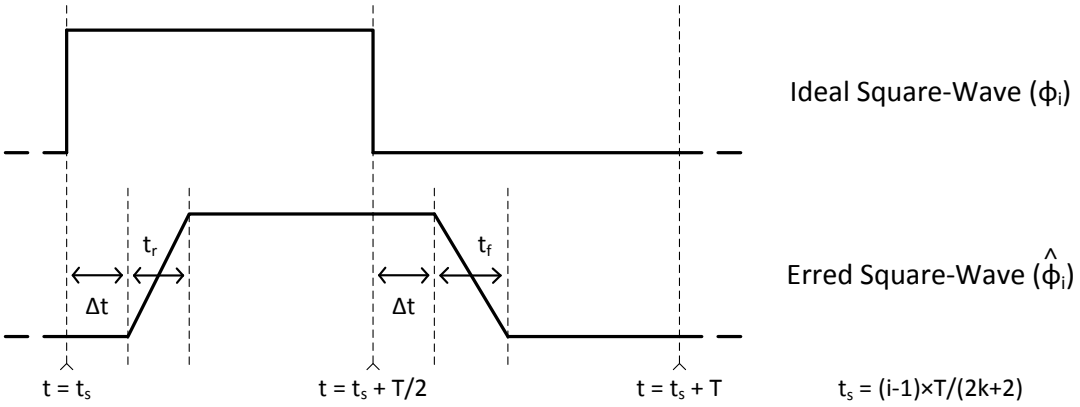


Figure 5.9: Timing non-idealities present in square-waves

signals is defined below.

$$\hat{s}(t) = R_{\mathrm{L}} \times I_{\mathrm{unit}} \times \sum_{i=1}^{k} m_i \times \hat{\phi}_i(t) \tag{5.13}$$

Note from Eq. 5.13 that a matched HC-DAC is assumed while analyzing the effect of timing non-idealities. Deriving from Eq. 5.13, the complex Fourier series of the HC-DAC output is given by the following equation.

$$\hat{S}(nf_{\mathrm{o}}) = R_{\mathrm{L}} \times I_{\mathrm{unit}} \times \sum_{i=1}^{k} m_i \times \hat{\Phi}_i(nf_{\mathrm{o}}) \tag{5.14}$$

The following sections will discuss the effect of timing non-idealities on an HC-DAC output. The discussions will be aided by results of simulations conducted in MATLAB using Eqns. 5.12–5.14. The simulations will be based on a 4–bit HC-DAC designed with 110 unit-elements.

### 5.4.2 Effect of Time-Shift Errors

The time-shift between each square-wave, $\phi_i$, and square-wave $\phi_1$ should ideally be $(i-1) \times T/(2k+2)$, as per the theory of harmonic-cancelling sine-wave synthesis presented in Section 3.2. This work models $\Delta t(i)$ as a random variable following a normal distribution with zero mean and a standard deviation of $\sigma_{\Delta t}$.

Monte Carlo simulations, with 10 000 samples for each value of $\sigma_{\Delta t}$, have been utilised to simulate the effect of time-shift errors on the HC-DAC output signal for a given value of $\sigma_{\Delta t}$.

To focus the analysis only on time-shift errors, near zero, equal transition times were assumed by setting, $t_{\mathrm{r}}(i) = t_{\mathrm{f}}(i) = 10^{-10} \times T$ for all $i$. Note that with rise-times and fall times assumed to be equal, the erred square-waves maintain half-wave symmetry regardless of the time-shift errors. Thus, the erred square-waves will not contain even order harmonics. Consequently, time-shift errors in the input square-waves do not affect even harmonic distortion in an HC-DAC output signal.

The harmonic cancellation operation suppresses the odd-harmonic distortion in an HC-DAC output signal. As proper operation of the harmonic cancelling technique requires precise time shifts between the square-wave signals, time-shift errors affect odd harmonic distortions in an HC-DAC output signal.

Figure 5.10 illustrates the mean SDR values obtained via Monte Carlo simulations with varying $\sigma_{\Delta t}$. Note that up to around $\sigma_{\Delta t} = 0.001$ %, SDR remains approximately equal to 79.9 dB, which is the ideal SDR of the HC-DAC considered in the simulation. In contrast, for $\sigma_{\Delta t}$ values higher than 0.001 %, the SDR drops at a rate of 20 dB per decade.

Figure 5.11 explains how each odd harmonic contributes to the degradation observed in SDR. Recall from previous discussions that a $k$–bit HC-DAC cancels lower order harmonics from $\mathrm{HD}_2$ to $\mathrm{HD}_{2k}$. As we are considering odd order harmonic cancellation in a 4-bit HC-DAC, only $\mathrm{HD}_3$, $\mathrm{HD}_5$, and $\mathrm{HD}_7$ are plotted in Fig. 5.11.

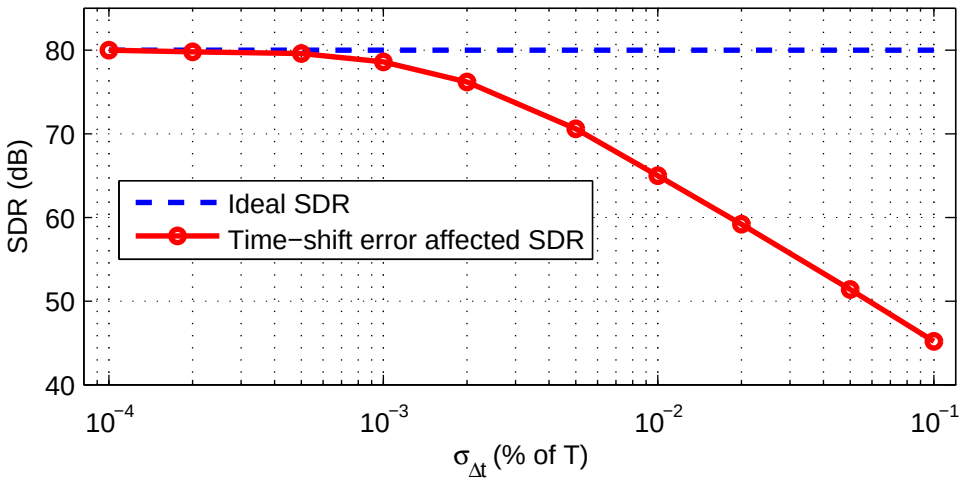


Figure 5.10: Mean SDR plotted against $\sigma_{\Delta t}$ for a 4-bit HC-DAC with $M = 110$

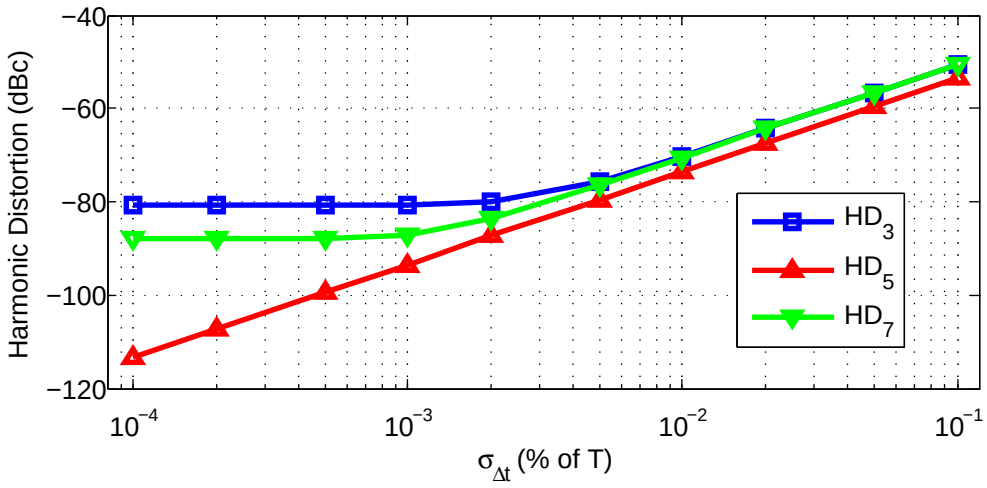


Figure 5.11: Mean odd harmonic distortions plotted against $\sigma_{\Delta t}$

### 5.4.3 Effect of Non-Zero Transition Times

Discussing the effect of non-zero transition times requires the consideration of two orthogonal issues. The following discussion tackles these two problems one at a time.

The effect of inequality between rise time and fall time is discussed first. In order to focus only on the difference between rise and fall times, it is assumed that, although

the rise time and fall time are unequal for a given square-wave, all square-waves experience the same rise time and the same fall time. For the same purpose, time-shift errors are assumed to be zero.

A contour plot illustrating the effect of rise-time and fall-time on HC-DAC output SDR is shown in Fig. 5.12. A cross-cut of the same results at $t_f = 0.5\%$ is plotted in Fig. 5.13 to further clarify the change in SDR against rise time. As apparent from the two figures, SDR of the HC-DAC output reaches its ideal value when the rise time and the fall time are equal. As the inequality between rise and fall times increases, SDR drops nonlinearly with decreasing rate.

Inequality between rise time and fall time of the square-wave signals affects both odd and even harmonics of the square-wave signals. However, as it is assumed that the rise time is the same for each square-wave signal, the fall time is the same for each square-wave signal, and that the time-shift errors are zero, suppression of odd harmonics due to the harmonic-cancelling technique remains unaffected. Thus, it can be deduced that the decrease in SDR observed in Fig. 5.13 is due to the increase in even harmonic distortion in the HC-DAC output signal.

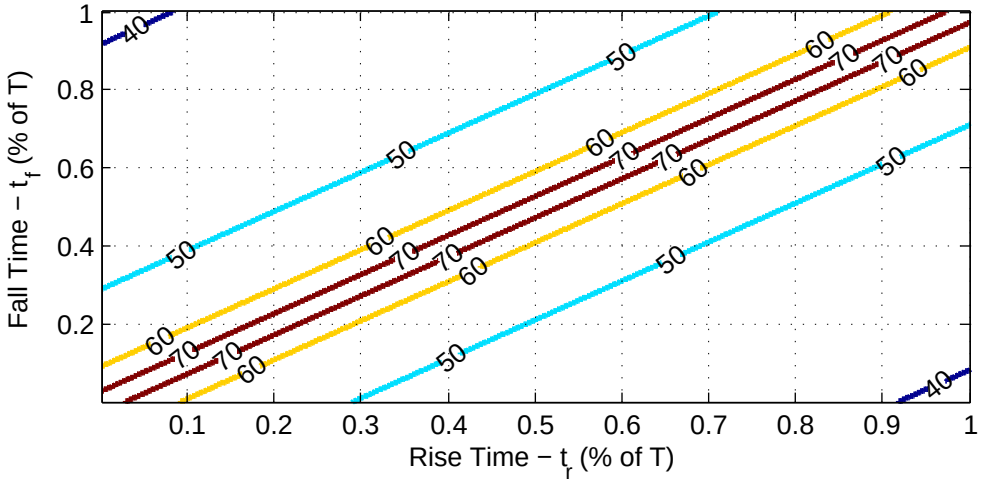


Figure 5.12: Contour plot of SDR against rise time and fall time for a 4-bit HC-DAC with $M = 110$

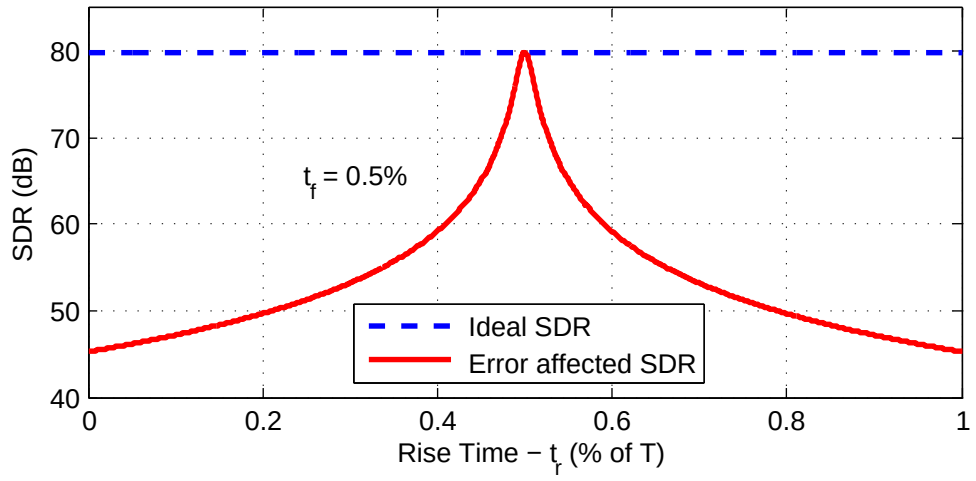


Figure 5.13: Cross-cut of Fig. 5.12 at $t_{\mathrm{f}} = 0.5\%$

Figure 5.14 illustrates the effect of rise time on even harmonic distortion in the HC-DAC output signal when fall time is kept at 0.5 %. It can be noted that, as the rise time approaches the fall time, all even harmonic distortions reduce towards negative infinity on the decibel scale. In contrast, as rise time and fall time grow apart, even harmonic distortions reach notably high values. Comparing Fig. 5.13 with Fig. 5.14 confirms that the change in SDR is caused due to the changes in even harmonic distortions.

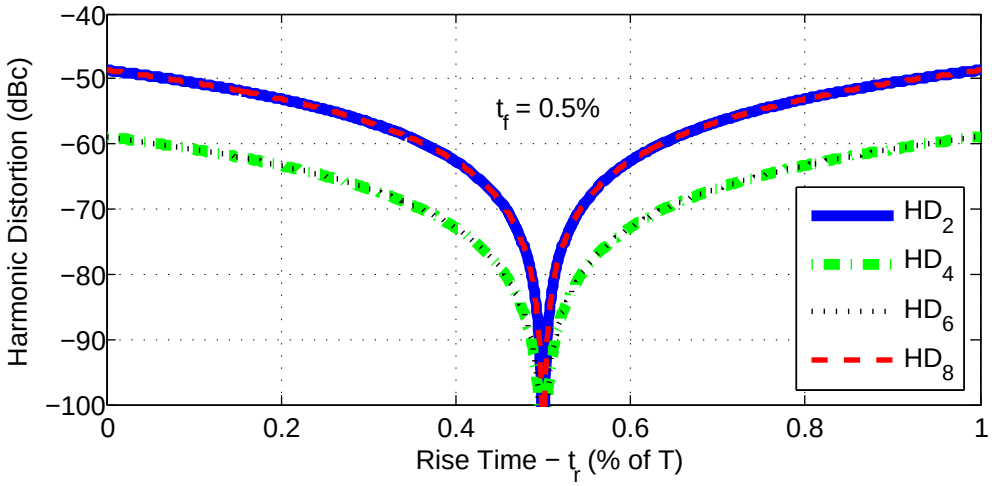


Figure 5.14: Cross-cut of even harmonic distortion of the HC-DAC output at $t_{\mathrm{f}} = 0.5\%$

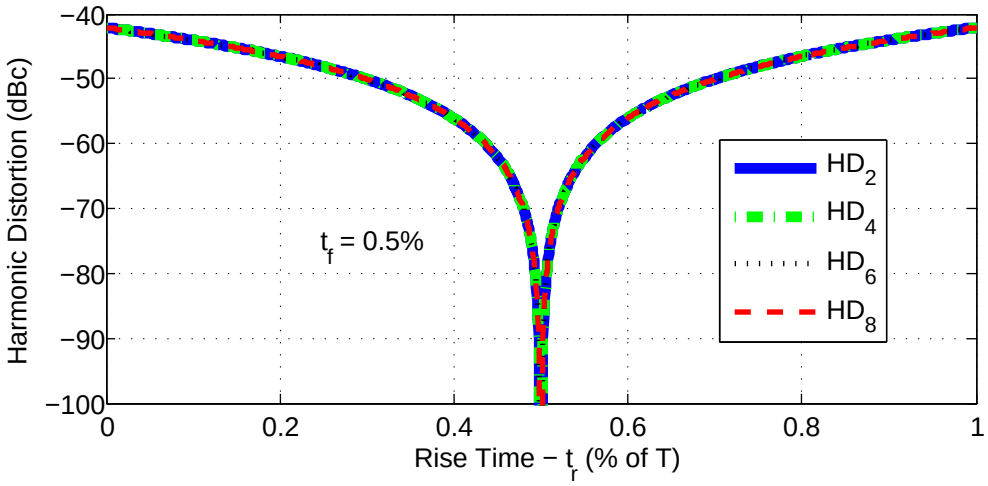


Figure 5.15: Cross-cut of even harmonic distortion of a square-wave signal at $t_\mathrm{f} = 0.5\%$

Figure 5.15 illustrates the effect of rise time on even harmonic distortion in a square-wave signal. When rise time and fall time differ from each other, the square-waves loose half-wave symmetry, which causes even harmonic distortion. The even harmonics of the square-wave signals fall in the middle of the side-lobes of the HC-DAC transfer function, as illustrated in Fig. 3.6. Thus, the even harmonics of the square-wave signals make their way into the HC-DAC output with only a small amount of attenuation.

Now let us focus on transition times differing from one square-wave to the other. In the following discussion we assume that the time shift errors are zero and that for a given square-wave signal, the rise time and the fall time are equal.

There is more than one way in which the transition times could be dependent on the square-wave signals. In this study, we assume a direct proportionality between transition times and the number of unit-elements driven by the square-wave signal, as defined by the following equation.

$$t_\mathrm{r}(i) = t_\mathrm{f}(i) = \alpha_\mathrm{tt} \times m_i \tag{5.15}$$

where $\alpha_\mathrm{tt}$ is the proportionality constant in units of % of $T$ per unit-element. The

number of unit-elements controlled by a given square-wave signal determines the capacitive load, which needs to be driven by the square-wave signal at the HC-DAC input. Assume that all square-wave signals are driven by buffers of the same size before reaching the HC-DAC input. Then, it is reasonable to deduce that the transition times of a given square-wave are proportional to the load to be driven at the HC-DAC input, and thereby, proportional to the number of unit-elements driven.

Figure 5.16 illustrates the variation of SDR at the output of the HC-DAC when $\alpha_{tt}$ is swept from 0.0001 % to 0.1 %. When $\alpha_{tt}$ is close to 0.0001 %, SDR remains near its ideal value of 79.9 dB. However, as $\alpha_{tt}$ increases, SDR starts dropping at a rate of 20 dB per decade.

As it is assumed that in each square-wave signal the rise time is equal to the fall time, the square-wave signals retain half-wave symmetry. Thus, it can be concluded that the increase in SDR evident from Fig. 5.16 is caused by odd harmonic distortions. The effect of signal dependent transition times on $HD_3$ and $HD_7$ of the HC-DAC output signal is shown in Fig. 5.17. As $\alpha_{tt}$ is increased, both $HD_3$ and $HD_7$ deviate from their ideal values and start rising at a rate of 20 dB per decade. Note that the

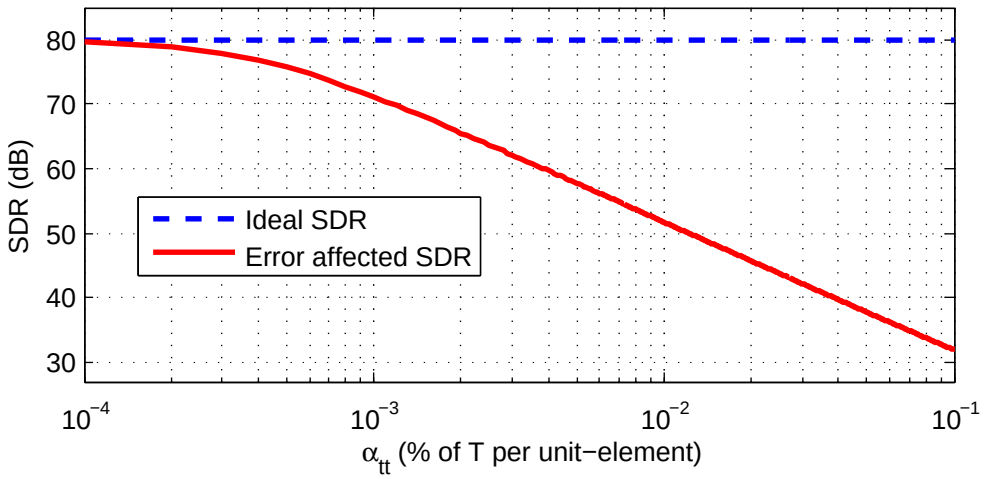


Figure 5.16: SDR change with signal dependent transition times

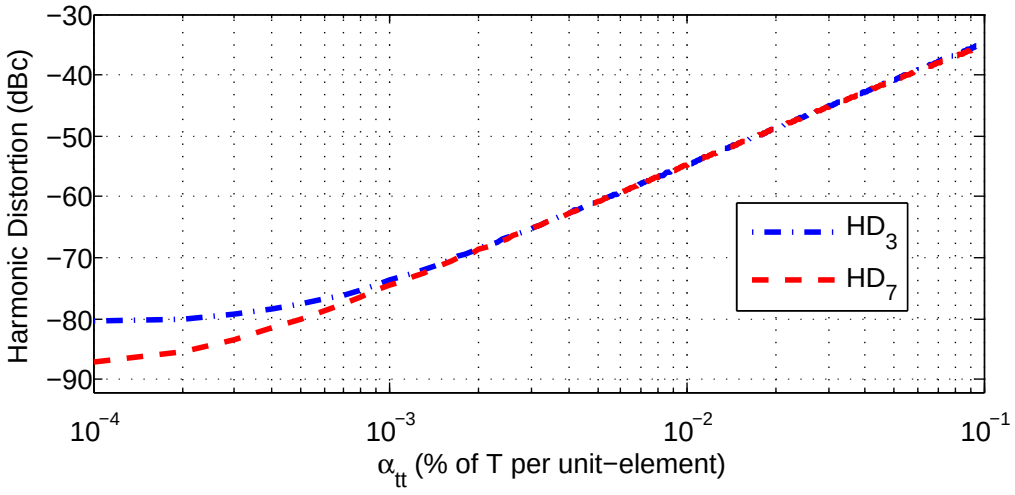


Figure 5.17: $HD_3$ and $HD_7$ change with signal dependent transition times

behaviour of $HD_3$ and $HD_7$ observed in Fig. 5.17 is consistent with the behaviour of SDR seen in Fig. 5.16.

The harmonic-cancelling sine-wave synthesis technique relies on each square-wave having the same frequency spectrum, except for the difference in phase. Transition times differing from one square-wave to another makes the frequency spectrums of the square-waves different from one another, which affects the cancellation of the odd harmonics. Thus, the odd harmonic distortion of the HC-DAC output signal increases and the SDR decreases, as observed in Fig. 5.16 and Fig. 5.17.

### 5.4.4 Application to Circuit Design

Two aspects of the DHSS circuit architecture, which affect the timing errors in square-wave signals, are discussed here. The use of a differential HC-DAC architecture, as depicted in Fig. 5.1, aids in reducing the effect of unequal rise and fall times in square-waves. Designing a circuit that produces a single-ended square-wave signal with symmetrical edges over process, voltage, and temperature corners, and mismatch is not practical. On the other hand, producing a differential square-

wave signal with nearly symmetrical edges is more feasible. Thus, using a differential HC-DAC in a DHSS reduces the inequality between rise and fall times of the square-waves signals, and thereby, reduces the even harmonic distortion in the HC-DAC output signal.

Time-shift errors and square-wave dependent transition times in the square-wave signals are caused due to the buffer circuits which drive the current switches in the HC-DAC. The role of square-wave buffers in a DHSS is illustrated in Fig. 5.18. Ideally, designing each buffer to have a drive strength that is proportional to the number of unit-current switches driven should ensure that the time-shift errors are zero and that the transition times are the same for each square-wave signal. However, in this research, we have not been able to observe this outcome in circuit simulations. Therefore, we have focused on making the buffers fast. Faster buffers reduce the timing errors which originate from them, and as evident from Fig. 5.10 and Fig. 5.16, for small enough timing errors the change in SDR is negligible.

Figure 5.19 plots circuit simulation results for frequency sweeps of a 4-bit HC-DAC designed with 110 unit-current switches. Circuits were developed and simulated in Cadence 5.10.41 using an STMicroelectronics 130 nm CMOS technology. The line plotted with circular markers illustrates the SDR of a differential HC-DAC circuit

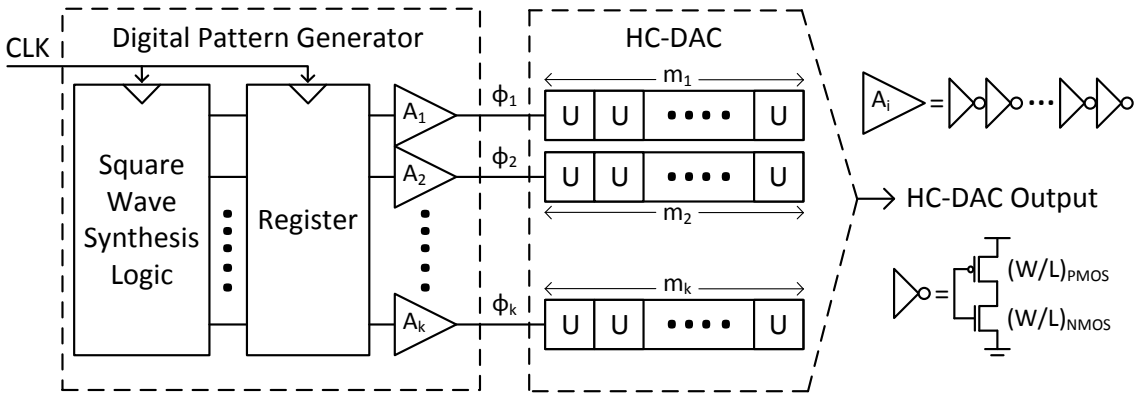


Figure 5.18: The role of square-wave signal buffers in a DHSS

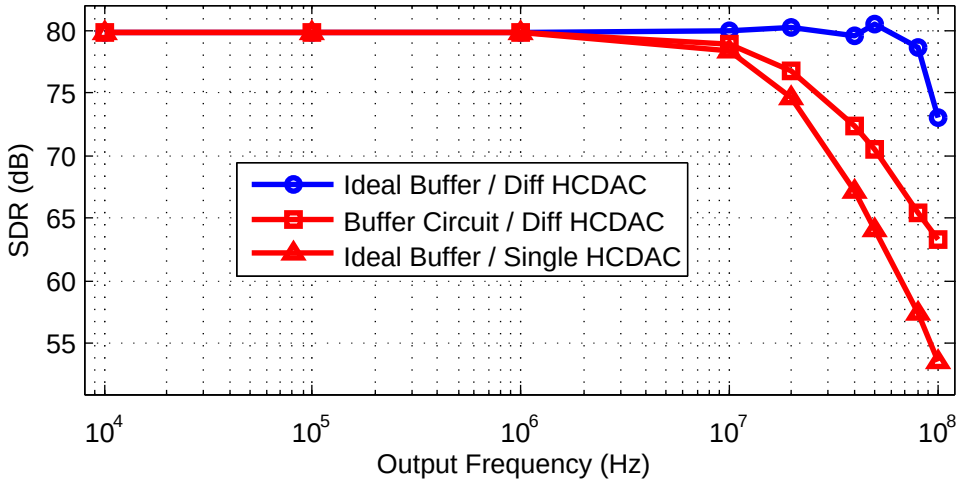


Figure 5.19: Circuit simulation results from a 4-bit HC-DAC with $M = 110$

driven with ideal buffers, where the buffers are represented by behavioral models. In contrast, the line with square markers plots the SDR of a differential HC-DAC circuit driven by buffer circuits, and the line with triangular markers plots the SDR of a single-ended HC-DAC circuit driven by ideal buffers. Each line deviates from the ideal SDR value of 79.9 dB at higher frequencies due to the effect of timing errors. The three frequency sweeps illustrate the effect of having a differential HC-DAC design, and better buffer circuits, in reducing the effect of timing errors.

## 5.5 Summary

In this chapter, we analyzed the HC-DAC used in a DHSS. First, a current-steering architecture was proposed for HC-DACs. Instead of scaled current switches, the use of unit-current switches in the HC-DAC was proposed to improve mismatch tolerance and to systematically define the amplitude resolution of the HC-DAC. Next, we analyzed the effect of amplitude resolution and mismatch of the HC-DAC on the SDR of the HC-DAC output signal. It was shown that HC-DACs could be designed with Pareto optimal values of amplitude resolution, at which the HC-

DACs break the 6 dB/bit rule. Then, we discussed the effect of timing related non-idealities on the SDR of the HC-DAC output. Time-shift errors and non-zero transition times were identified as timing non-idealities, and their effect on SDR was analyzed separately. Finally, the impact of square-wave signal buffer circuits and differential HC-DAC design on timing non-idealities was also discussed. It was shown through circuit simulations that fast buffers and differential HC-DAC designs reduce the effect of timing non-idealities.

# Chapter 6

# Dynamic Element Matching

## 6.1 Overview

There are two orthogonal factors which affect the signal-to-distortion ratio of an HC-DAC output signal. These factors are amplitude scaling errors and timing errors. Amplitude scaling errors are caused by finite amplitude resolution and mismatch between unit-elements. The effects of timing nonidealities and finite amplitude resolution on HC-DACs have been addressed in Chapter 5. The effect of mismatch [STK84, LHC86, PDW89, BSR+95, BSGS96, Kin05, Bak10a, YSM+11], which was only briefly discussed in Chapter 5, is the problem addressed here.

Design time decisions can never prevent mismatch. However, there are techniques which can be used to manage the effect of mismatch. Dynamic element matching [dP76, dPG79, Sto92, GC95, JG98, Gal10] is one such technique. Although HC-DAC like circuits have been used in previous work related to harmonic-cancelling sine-wave synthesis [ESS10, SBT+10, BLVR14, SSS15], DEM has not been considered as a solution to counter mismatch errors in HC-DACs. Thus, to the best of our

knowledge, this work is the first to propose the use of DEM techniques in HC-DACs.

A completely scrambled DEM technique can entirely eradicate the effect of mismatch in an HC-DAC, as discussed in detail later. However, the digital hardware complexity of implementing a complete DEM method is significantly high. The hallmark of a DHSS is its simple hardware design. Therefore, *this chapter proposes a partially scrambled DEM technique tailored for HC-DACs, which reduces the effect of mismatch while requiring lower hardware cost compared to a complete DEM technique.*

The rest of this chapter is structured as follows. Section 6.2 provides a theoretical background into the mismatch issue in HC-DACs. Section 6.3 introduces the concept of DEM in the context of HC-DACs, and discusses the effect of implementing a complete DEM technique in an HC-DAC. Section 6.4 proposes a partial DEM technique, and discusses its effect on mismatch errors. Section 6.5 presents simulation results based on a MATLAB model to evaluate the effectiveness of the proposed partial DEM technique. Section 6.6 describes the design of the circuits required to implement DEM. Finally, Section 6.7 concludes the chapter.

## 6.2 Background

A mathematical model for the behaviour of a current-steering $k$-bit HC-DAC has been derived in Section 5.3, which will be used as a starting point in this chapter to discuss the mathematics of DEM. Based on Eq. 5.9, Eq. 5.10, and Eq. 5.11, the following equations have been defined to describe the behaviour of a matched (i.e. having zero mismatch between unit-elements) $k$-bit HC-DAC:

$$I_{\mathrm{m}}(i) \;=\; m_i \times I_{\mathrm{unit}} \tag{6.1}$$

$$s_{\mathrm{m}}(t) = R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{m}}(i) \times \phi_i(t) \tag{6.2}$$

$$S_{\mathrm{m}}(nf_{\mathrm{o}}) = R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{m}}(i) \times \Phi_i(nf_{\mathrm{o}}) \tag{6.3}$$

where $I_{\mathrm{m}}(i)$ is the total current controlled by HC-DAC input signal $\phi_i(t)$, $s_{\mathrm{m}}(t)$ is the output voltage signal of the HC-DAC, $S_{\mathrm{m}}(nf_{\mathrm{o}})$ denotes the complex Fourier coefficients of $s_{\mathrm{m}}(t)$, and $\Phi_i(nf_{\mathrm{o}})$, which denotes the Fourier coefficients of $\phi_i(t)$, is defined below.

$$\Phi_i(nf_{\mathrm{o}}) = \frac{[1 - \cos(n\pi)]}{n\pi j} \times \exp\left[\frac{n\pi j}{k+1} \times (1-i)\right] \tag{6.4}$$

Please refer to Appendix B for a derivation of Eq. 6.4.

Let us now consider a current steering $k$-bit HC-DAC, in which there is mismatch between the currents conducted through different unit-current switches. Using the definition of $I_{\mathrm{u}}(i,l)$ given in Eq. 5.7, the total current, $I_{\mathrm{mm}}(i)$, controlled by each input signal $\phi_i(t)$ is defined as follows:

$$I_{\mathrm{mm}}(i) = \sum_{l=1}^{m_i} I_{\mathrm{u}}(i,l) = I_{\mathrm{m}}(i) + E_{\mathrm{mm}}(i) \tag{6.5}$$

where $E_{\mathrm{mm}}(i)$ is the mismatch error current controlled by $\phi_i(t)$. Using the definition of $I_{\mathrm{mm}}(i)$, the output signal of a mismatched HC-DAC is defined below.

$$\begin{aligned} s_{\mathrm{mm}}(t) &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{mm}}(i) \times \phi_i(t) \\ &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{m}}(i) \times \phi_i(t) + R_{\mathrm{L}} \times \sum_{i=1}^{k} E_{\mathrm{mm}}(i) \times \phi_i(t) \\ &= s_{\mathrm{m}}(t) + s_{\mathrm{e}}(t) \end{aligned} \tag{6.6}$$

Note that according to Eq. 6.6, the output signal of a mismatched HC-DAC can be considered as a combination of the output of the corresponding matched HC-DAC,

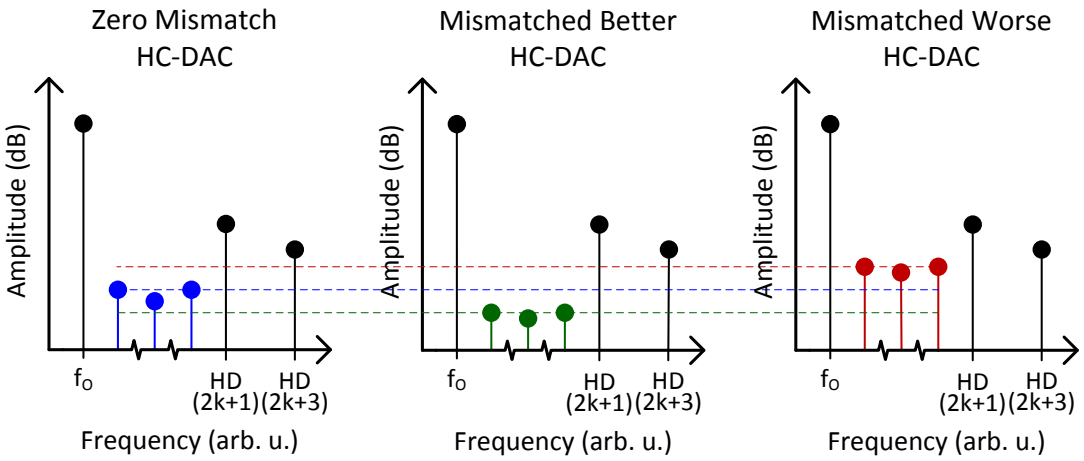


Figure 6.1: Spectrums of matched and mismatched $k$-bit HC-DACs

and the mismatch error signal $s_{\mathrm{e}}(t)$. Following on from Eq. 6.6, the complex Fourier coefficients of the mismatched HC-DAC output signal is given by:

$$\begin{aligned} S_{\mathrm{mm}}(nf_o) &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{mm}}(i) \times \Phi_i(nf_{\mathrm{o}}) \\ &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{m}}(i) \times \Phi_i(nf_{\mathrm{o}}) + R_{\mathrm{L}} \times \sum_{i=1}^{k} E_{\mathrm{mm}}(i) \times \Phi_i(nf_{\mathrm{o}}) \\ &= S_{\mathrm{m}}(nf_{\mathrm{o}}) + S_{\mathrm{e}}(nf_{\mathrm{o}}) \end{aligned} \tag{6.7}$$

As both $s_{\mathrm{m}}(t)$ and $s_{\mathrm{e}}(t)$ are periodic signals with frequency $f_{\mathrm{o}} = 1/T_{\mathrm{o}}$, $S_{\mathrm{m}}(nf_{\mathrm{o}})$ and $S_{\mathrm{e}}(nf_{\mathrm{o}})$ in Eq. 6.7 have the same fundamental frequency and harmonics. Even though mismatch is seen in general as a nuisance, in the case of a mismatched HC-DAC it is possible for the combination of $S_{\mathrm{m}}(nf_{\mathrm{o}})$ and $S_{\mathrm{e}}(nf_{\mathrm{o}})$ to have a better, equal, or worse SDR compared to $S_{\mathrm{m}}(nf_{\mathrm{o}})$, as illustrated in Fig. 6.1. However, in a vast majority of cases, mismatch has a negative effect on SDR. The following discussions aim to improve the SDR of HC-DACs which are negatively affected by mismatch.

## 6.3 Dynamic Element Matching

DEM techniques are popularly utilized in conventional DACs to reduce the effect of mismatch on output spectral purity [dP76, BF95, CL95, GC95, JG98, Gal10, Cla13]. Widely used DEM techniques include mismatch noise shaping algorithms, such as barrel-shift [BF95] and individual level averaging (ILA) [CL95], and mismatch noise scrambling algorithms (random averaging) [GC95, JG98]. Using barrel-shift DEM in an HC-DAC will generate undesirable tones in the output spectrum because the input signals of the HC-DAC are periodic [Cla13]. Implementing ILA DEM requires higher hardware complexity compared to the other DEM algorithms [Cla13], and the focus of this work is to maintain the low hardware complexity of DHSSs. Thus, this chapter focuses on mismatch noise scrambling DEM techniques for HC-DACs.

### 6.3.1 Dynamic Element Matching in HC-DACs

Consider a mismatched $k$-bit HC-DAC which employs a mismatch scrambling DEM technique. Each input signal $\phi_i(t)$ will continue to control $m_i$ number of unit-current switches, yet the physical set of unit-current switches controlled by each input signal will be pseudo-randomly altered with time. Thus, the total current, $I_{\mathrm{dm}}(i,t)$, controlled by input signal $\phi_i(t)$ will have an error, $E_{\mathrm{dm}}(i,t)$, which is a pseudo-random signal, as defined below:

$$I_{\mathrm{dm}}(i,t) = I_{\mathrm{m}}(i) + E_{\mathrm{dm}}(i,t) \tag{6.8}$$

The stochastic error signal can be elaborated as follows:

$$E_{\mathrm{dm}}(i,t) = \overline{E}_{\mathrm{dm}}(i) + \Delta E_{\mathrm{dm}}(i,t) \tag{6.9}$$

where $\overline{E}_{\mathrm{dm}}(i)$ is the mean of $E_{\mathrm{dm}}(i,t)$, and $\Delta E_{\mathrm{dm}}(i,t)$ is the deviation of $E_{\mathrm{dm}}(i,t)$ from its mean at time $t$. Note that by definition, $\Delta E_{\mathrm{dm}}(i,t)$ is a zero-mean pseudo-random signal. Based on Eq. 6.8 and Eq. 6.9, the output signal, $s_{\mathrm{dm}}(t)$, of an

HC-DAC employing a DEM technique can be defined as follows:

$$\begin{aligned} s_{\mathrm{dm}}(t) &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{dm}}(i,t) \times \phi_i(t) \\ &= R_{\mathrm{L}} \sum_{i=1}^{k} I_{\mathrm{m}}(i) \times \phi_i(t) + R_{\mathrm{L}} \sum_{i=1}^{k} \overline{E}_{\mathrm{dm}}(i) \times \phi_i(t) + R_{\mathrm{L}} \sum_{i=1}^{k} \Delta E_{\mathrm{dm}}(i,t) \times \phi_i(t) \\ &= s_{\mathrm{m}}(t) + s_{\bar{\mathrm{e}}_{\mathrm{dm}}}(t) + s_{\Delta \mathrm{e}_{\mathrm{dm}}}(t) \end{aligned} \tag{6.10}$$

As shown above, the HC-DAC output signal can be separated into three parts: $s_{\mathrm{m}}(t)$, $s_{\bar{\mathrm{e}}_{\mathrm{dm}}}(t)$, and $s_{\Delta \mathrm{e}_{\mathrm{dm}}}(t)$, where $s_{\mathrm{m}}(t)$ is the output signal of the corresponding matched HC-DAC.

As $\overline{E}(i)$ are DC terms, if at least one $\overline{E}(i)$ term is non-zero, signal $s_{\bar{\mathrm{e}}_{\mathrm{dm}}}(t)$ will be a periodic signal with frequency $f_{\mathrm{o}} = 1/T$. It can be understood that the addition of $s_{\bar{\mathrm{e}}_{\mathrm{dm}}}(t)$ to $s_{\mathrm{m}}(t)$ could have a negative impact, a positive impact or no impact on the overall SDR of the signal, similar to the case discussed in Section 6.2. For a given value of $i$, the spectrum of $\Delta E(i,t)$ is a white noise spectrum with zero DC component, as $\Delta E(i,t)$ is a zero-mean pseudo-random signal. The convolution of a white noise spectrum having zero DC component with the spectrum of a square-wave will lead to another white noise spectrum. Thus, the spectrum of $s_{\Delta \mathrm{e}_{\mathrm{dm}}}(t)$ will be white noise.

In summary, Eq. 6.10 delineates that in the output signal of a DEM employed HC-DAC, part of the mismatch error may remain as harmonic distortion in the form of $s_{\bar{\mathrm{e}}_{\mathrm{dm}}}(t)$, while the remaining portion of the mismatch error gets spread across the spectrum as white noise in the form of $s_{\Delta \mathrm{e}_{\mathrm{dm}}}(t)$. The portion of mismatch error carried in each error signal depends on the particular DEM technique utilized.

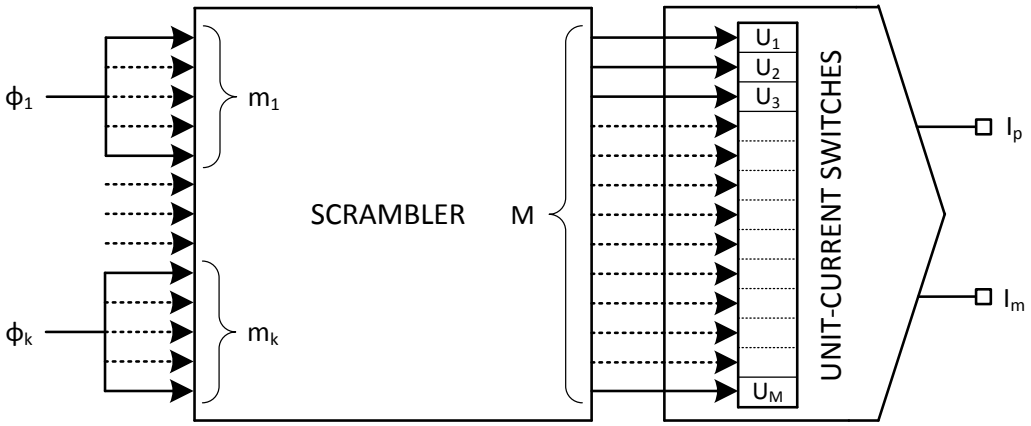


Figure 6.2: HC-DAC using a completely scrambled DEM technique

### 6.3.2 Completely Scrambled DEM Technique for HC-DACs

A completely scrambled DEM technique ensures that there is a uniform probability of any given unit element being controlled by a given input signal at a given time. An HC-DAC implementing a completely scrambled DEM technique is shown in Fig. 6.2.

The core operation of DEM is carried out by the scrambler, which is a digital circuit. The scrambler has $M$ number of inputs ($\sum m_i = M$), and an equal number of outputs. Each square-wave signal $\phi_i(t)$ provides $m_i$ number of inputs to the scrambler, while each output of the scrambler controls a distinct unit-current switch, $\mathrm{U}_x$, where $x \in \{y \mid y \leq M,\ x \in \mathbb{Z}^+\}$. At any given time, the scrambler links the inputs to the outputs with a 1-to-1 mapping, and at a pre-defined frequency ($f_{\mathrm{dem}}$) the scrambler pseudo-randomly alters the mapping between the inputs and the outputs. By switching between mappings such that every distinct 1-to-1 mapping between inputs and outputs has the same probability of occurring, the scrambler implements a complete DEM technique.

Two 1-to-1 mappings in the scrambler are considered to be distinct, only if the sets of physical unit-current switches controlled by at least two of the input signals are different, by at least one unit-current switch, between the two mappings. Therefore,

the mapping of inputs to the outputs of the scrambler can be considered as a combinations problem. Let us denote the total number of distinct 1-to-1 mappings in the scrambler by $C_{\mathrm{T}}$. There are $M!$ number of ways in which the inputs and the outputs of the scrambler can be 1-to-1 mapped. However, among those $M!$ mappings, in $M! \times (m_i! - 1)/m_i!$ number of mappings, signal $\phi_i(t)$ is controlling the same set of physical unit-elements. Thus, $C_{\mathrm{T}}$ is defined as given below.

$$C_{\mathrm{T}} = \frac{M!}{m_1! \times m_2! \times \cdots \times m_k!} \tag{6.11}$$

Next, let us denote the number of mappings, in which a given unit-current switch $\mathrm{U}_x$ is controlled by a given square-wave $\phi_i(t)$, by $C_i$. In this scenario, $M-1$ number of inputs need to be 1-to-1 mapped to $M-1$ outputs, and signal $\phi_i(t)$ connects to only $m_i - 1$ number of inputs. Thus, similar to the way $C_{\mathrm{T}}$ was derived, $C_i$ can be derived to be as follows:

$$C_i = \frac{m_i \times (M-1)!}{m_1! \times m_2! \times \cdots \times m_k!} \tag{6.12}$$

Let us denote the current flowing through each unit-current switch $\mathrm{U}_x$ by $I_{\mathrm{u}}(x)$, and the summation of currents flowing in all unit-current switches by $I_\Sigma = \sum_{x=1}^{M} I_{\mathrm{u}}(x)$. Then, the average current controlled by a given input square-wave signal $\phi_i(t)$ in a complete DEM HC-DAC can be defined as follows:

$$\overline{I_{\mathrm{cdm}}}(i) = \frac{\sum\limits_{x=1}^{M} C_i \times I_{\mathrm{u}}(x)}{C_{\mathrm{T}}} = m_i \times \frac{I_\Sigma}{M} = m_i \times \hat{I}_{\mathrm{unit}} \tag{6.13}$$

where $\hat{I}_{\mathrm{unit}}$ denotes the average current per unit-current switch in the mismatched HC-DAC. Following on from the definition of $\overline{I_{\mathrm{cdm}}}(i)$, the total current controlled by input signal $\phi_i(t)$ at time $t$ is defined below.

$$I_{\mathrm{cdm}}(i,t) = \overline{I_{\mathrm{cdm}}}(i) + \Delta E_{\mathrm{cdm}}(i,t) \tag{6.14}$$

Note that by definition $\Delta E_{\mathrm{cdm}}(i,t)$ is a zero-mean pseudo-random signal.

The output signal, $s_{\mathrm{cdm}}(t)$, of a complete DEM HC-DAC can be derived as follows:

$$\begin{aligned} s_{\mathrm{cdm}}(t) &= R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{cdm}}(i,t) \times \phi_i(t) \\ &= R_{\mathrm{L}} \times \sum_{i=1}^{k} \overline{I_{\mathrm{cdm}}}(i) \times \phi_i(t) + R_{\mathrm{L}} \times \sum_{i=1}^{k} \Delta E_{\mathrm{cdm}}(i,t) \times \phi_i(t) \\ &= \left( \frac{\hat{I}_{\mathrm{unit}}}{I_{\mathrm{unit}}} \right) \times s_{\mathrm{m}}(t) + s_{\Delta \mathrm{e}_{\mathrm{cdm}}}(t) \end{aligned} \tag{6.15}$$

By comparing Eq. 6.15 with Eq. 6.10, it can be noted that in the case of a complete DEM HC-DAC, the addition of $s_{\mathrm{m}}(t)$ and $s_{\bar{\mathrm{e}}_{\mathrm{cdm}}}(t)$ yields a signal which only has a constant gain error of $\hat{I}_{\mathrm{unit}}/I_{\mathrm{unit}}$ compared to $s_{\mathrm{m}}(t)$. Further, as discussed previously, $s_{\Delta \mathrm{e}_{\mathrm{cdm}}}(t)$ will have a white noise spectrum. Consequently, the SDR of a complete DEM HC-DAC will be equal to the SDR of the corresponding matched HC-DAC.

The theoretical discussion conducted above concludes that a complete DEM technique can entirely eradicate the effect of mismatch in an HC-DAC. However, implementing the scrambler in a complete DEM HC-DAC significantly complicates the otherwise simple hardware architecture of a DHSS. Consider the example of a 4-bit HC-DAC with $M = 110$ number of unit-current switches. According to Eq. 6.11, the scrambler in the example HC-DAC should alter between 70 novemdecillion ($10^{60}$) mapping combinations. The given example makes it clear that the complexity of the digital hardware required in the scrambler makes the implementation of a complete DEM technique impractical. To solve this problem, the following section proposes a partially scrambled DEM technique, which is simpler to implement.

## 6.4 Partially Scrambled DEM Technique

### 6.4.1 A Partially Scrambled DEM Technique for HC-DACs

A partially scrambled DEM technique scrambles the usage of unit elements by input signals in such a way that, there is a non-uniform probability of any given unit element being controlled by a given input signal at a given time. The advantage of using a partial DEM technique is the reduced hardware complexity of implementation. On the other hand, a partial DEM method may not completely mitigate the effect of mismatch. An HC-DAC, which implements the partial DEM technique proposed in this thesis, is illustrated in Fig. 6.3.

According to Eq. 5.3 and Eq. 5.4, input square-wave signals $\phi_i(t)$ and $\phi_{k+1-i}(t)$ control the same number of unit-current switches, which means:

$$m_i = m_{k+1-i} \tag{6.16}$$

The partial DEM technique proposed in this chapter takes advantage of this relationship. The DEM technique is implemented using multiple scramblers: $S_p$,

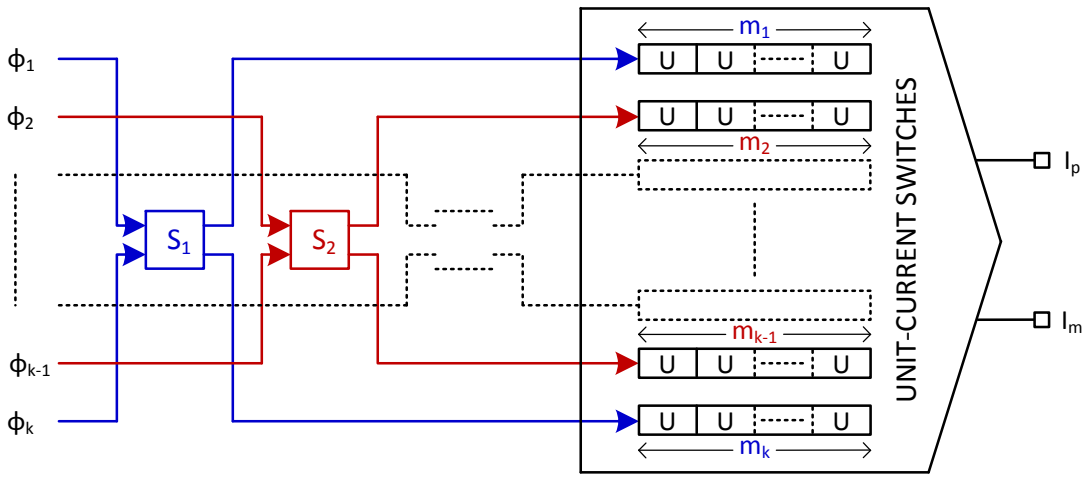


Figure 6.3: HC-DAC using a partially scrambled DEM technique

where $p \in \{x \mid x \leq \lfloor k/2 \rfloor,\ x \in \mathbb{Z}^+\}$, each of which takes in two inputs and provides two outputs. At a predefined frequency of $f_{\text{dem}}$ each scrambler randomly alters the 1-to-1 mapping between its inputs and outputs. Scrambler $\text{S}_p$ takes in $\phi_p(t)$ and $\phi_{k+1-p}(t)$ as inputs, while its outputs control two sets of $m_p$ $(= m_{k+1-p})$ number of unit-current switches. Note that when $k$ is odd, $\phi_{\lceil k/2 \rceil}(t)$ will control the same set of $m_{\lceil k/2 \rceil}$ number of unit-current switches, without being affected by the DEM operation.

The output signal of a partial DEM HC-DAC can be derived as follows. First, recall that Eq. 6.5 defines the total current controlled by input signal $\phi_i(t)$ in a mismatched HC-DAC that does not use DEM. Then, the average current controlled by $\phi_i(t)$ in a partial DEM HC-DAC can be described as follows:

$$\begin{aligned}
\overline{I_{\text{pdm}}}(i) &= \frac{I_{\text{mm}}(i) + I_{\text{mm}}(k+1-i)}{2} \\
&= I_{\text{m}}(i) + \frac{E_{\text{mm}}(i) + E_{\text{mm}}(k+1-i)}{2} \\
&= I_{\text{m}}(i) + \overline{E}_{\text{pdm}}(i)
\end{aligned} \tag{6.17}$$

Based on the above equation, the total current controlled by $\phi_i(t)$ at time $t$ in a partial DEM HC-DAC is given by

$$\begin{aligned}
I_{\text{pdm}}(i,t) &= \overline{I_{\text{pdm}}}(i) + \Delta E_{\text{pdm}}(i,t) \\
&= I_{\text{m}}(i) + \overline{E}_{\text{pdm}}(i) + \Delta E_{\text{pdm}}(i,t)
\end{aligned} \tag{6.18}$$

where $\Delta E_{\text{pdm}}(i,t)$ is a zero-mean pseudo random signal. Using Eq. 6.18, the output signal of a partial DEM HC-DAC is derived in the following manner:

$$\begin{aligned}
s_{\text{pdm}}(t) &= R_{\text{L}} \times \sum_{i=1}^{k} I_{\text{pdm}}(i,t) \times \phi_i(t) \\
&= R_{\text{L}} \sum_{i=1}^{k} I_{\text{m}}(i) \times \phi_i(t) + R_{\text{L}} \sum_{i=1}^{k} \overline{E}_{\text{pdm}}(i) \times \phi_i(t) + R_{\text{L}} \sum_{i=1}^{k} \Delta E_{\text{pdm}}(i,t) \times \phi_i(t) \\
&= s_{\text{m}}(t) + s_{\bar{\text{e}}_{\text{pdm}}}(t) + s_{\Delta \text{e}_{\text{pdm}}}(t)
\end{aligned} \tag{6.19}$$

For the sake of future discussions, let us also define the complex Fourier series of the partial DEM HC-DAC output signal. Considering that a Fourier series can only be defined for the periodic portion of $s_{\text{pdm}}(t)$, which results from the square-waves being scaled by the average currents they control, we derive the following equation for $\overline{S}_{\text{pdm}}(nf_{\text{o}})$:

$$\begin{aligned}\overline{S}_{\text{pdm}}(nf_{\text{o}}) &= R_{\text{L}} \times \sum_{i=1}^{k} \overline{I_{\text{pdm}}}(i) \times \Phi_i(nf_{\text{o}}) \\ &= R_{\text{L}} \times \sum_{i=1}^{k} I_{\text{m}}(i) \times \Phi_i(nf_{\text{o}}) + R_{\text{L}} \times \sum_{i=1}^{k} \overline{E}_{\text{pdm}}(i) \times \Phi_i(nf_{\text{o}}) \\ &= S_{\text{m}}(nf_{\text{o}}) + S_{\bar{\text{e}}_{\text{pdm}}}(nf_{\text{o}}) \end{aligned} \tag{6.20}$$

Note that Eq. 6.19 takes a similar form to Eq. 6.10, which has already been discussed in Section 6.3. The first term $s_{\text{m}}(t)$ is the output of the corresponding matched HC-DAC. The partial DEM technique converts a portion of the mismatch error to white noise in the form of $s_{\Delta\text{e}_{\text{pdm}}}(t)$, while the residual mismatch error continues to produce harmonic content in the form of $s_{\bar{\text{e}}_{\text{pdm}}}(t)$. The existence of $s_{\bar{\text{e}}_{\text{pdm}}}(t)$ could improve, degrade, or have no effect on the overall HC-DAC output SDR.

### 6.4.2 The Effect on Mismatch Errors

Let us consider an HC-DAC affected by random mismatch. When the mismatch errors are random, the quantitative effect of applying the proposed partial DEM technique is also random. However, the following discussion deduces that the proposed partial DEM method always has a positive qualitative impact on the HC-DAC output SDR.

In order to understand the effect of the proposed partial DEM technique, the operation of an HC-DAC needs to be looked at from the point of view of phasors. Consider

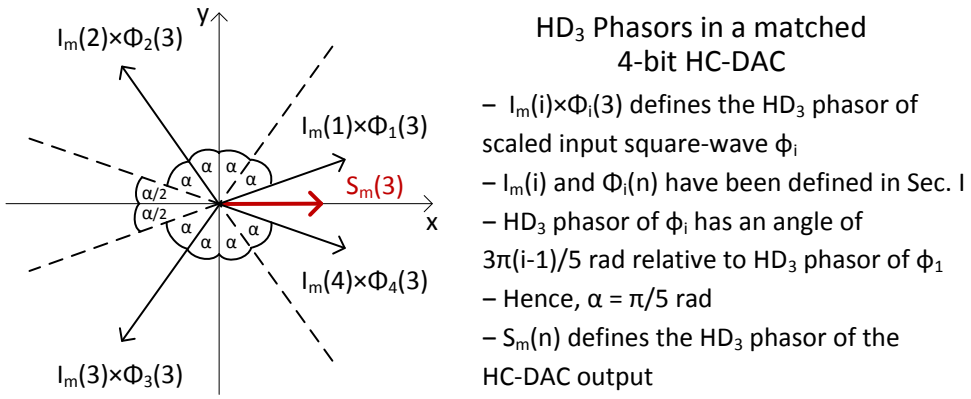


Figure 6.4: HD$_3$ phasors involved in a matched 4-bit HC-DAC

the effect of the scaling and summing operation of an HC-DAC on a given $n^{\text{th}}$ harmonic, HD$_n$. An HC-DAC scales and sums the HD$_n$ phasors of the input square-wave signals to produce the HD$_n$ phasor of the HC-DAC output signal. HC-DAC amplitude scaling factors are set according to Eq. 3.14 such that, for $n \in \{3, 5, ..., 2k-1\}$, the scaling and summing operation causes attenuation of the HD$_n$ phasor in the HC-DAC output signal, thus, resulting in harmonic cancellation.

Figure 6.4 illustrates a phasor diagram depicting the HD$_3$ phasors involved in the operation of a matched 4-bit HC-DAC. Another way to look at the phasor diagram in Fig. 6.4 is as a visual representation of Eq. 6.3, when $k = 4$ and $n = 3$. In the phasor diagram, $I_{\text{m}}(i) \times \Phi_i(3f_{\text{o}})$, where $i \in \{1, 2, 3, 4\}$, is the scaled HD$_3$ phasor of the input square-wave signal $\phi_i(t)$.

According to Eq. 6.4, $\Phi_i(3)$ is at an angle of $3\pi(i-1)/5$ rad relative to $\Phi_1(3)$. Thus, the angle denoted by $\alpha$ in the phasor diagram is equal to $\pi/5$ rad. Using the knowledge from Eq. 6.1 and Eq. 6.16, phasors $I_{\text{m}}(i) \times \Phi_i(3)$ and $I_{\text{m}}(5-i) \times \Phi_{5-i}(3)$ are drawn with equal magnitude.

In Fig. 6.4, the phasor denoted by $S_{\text{m}}(3)$ is the residual HD$_3$ phasor of the matched HC-DAC output signal, as defined in Eq. 6.3. The x-axis of the diagram is chosen to align with the HC-DAC output phasor, in order to make the diagram easier

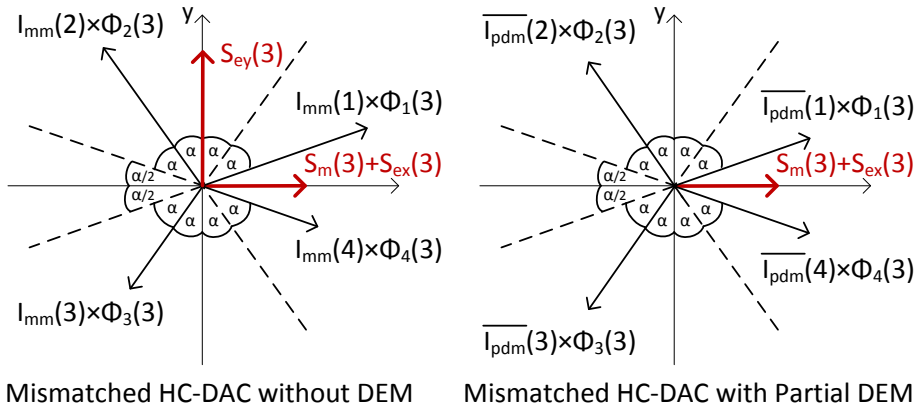


Figure 6.5: $HD_3$ phasors involved in the operation of a mismatched 4-bit HC-DAC - without and with partial DEM

to visualize. Thus, the x-axis does not necessarily reference the real axis. It is important to note that the symmetrical relationship between amplitudes of the scaled square-wave phasors affects the direction of $S_{\mathrm{m}}(3)$.

The phasor diagram on the left in Fig. 6.5 illustrates the $HD_3$ phasors involved in the operation of a mismatched 4-bit HC-DAC, which does not employ a DEM technique. Thus, the phasor diagram could be considered as a visual representation of Eq. 6.7, when $k = 4$ and $n = 3$. As shown in the phasor diagram, in the mismatched HC-DAC, each $HD_3$ phasor $\Phi_i(3)$ is scaled by $I_{\mathrm{mm}}(i)$, which has been defined in Eq. 6.5. The scaling mismatch errors cause an error phasor with x-axis and y-axis components, $S_{\mathrm{ex}}(n)$ and $S_{\mathrm{ey}}(n)$, to appear at the HC-DAC output. In relation to Eq. 6.7, $S_{\mathrm{e}}(n) = S_{\mathrm{ex}}(n)+S_{\mathrm{ey}}(n)$. It is important to note from Fig. 6.5 that even with mismatch, if the mismatched currents follow the symmetrical relationship, $I_{\mathrm{mm}}(i) = I_{\mathrm{mm}}(5-i)$, then $S_{\mathrm{ey}}(n)$ will be zero.

The phasor diagram on the right in Fig. 6.5 depicts the deterministic $HD_3$ phasors involved in a mismatched 4-bit HC-DAC, which utilizes the proposed partial DEM technique. An alternative angle to perceive the phasor diagram is as a visualization of Eq. 6.20. When the DEM technique is applied, the amplitude of the scaled

$HD_3$ phasor of each square-wave varies randomly with time. In Fig. 6.5 the mean amplitude of the scaled $HD_3$ phasor of input square-wave $\phi_i(t)$ is given by $\overline{I_{\text{pdm}}}(i) \times \Phi_i(3)$.

According to the definition of $\overline{I_{\text{pdm}}}(i)$ in Eq. 6.17, the symmetrical relationship, $\overline{I_{\text{pdm}}}(i) = \overline{I_{\text{pdm}}}(5-i)$, is satisfied. Thus, as drawn in Fig. 6.5, phasor pairs $\overline{I_{\text{pdm}}}(i) \times \Phi_i(3)$ and $\overline{I_{\text{pdm}}}(5-i) \times \Phi_{5-i}(3)$ have equal amplitude. Consequently, the y-axis mismatch error component does not exist at the HC-DAC output, while the x-axis component remains unchanged. However, the spectral energy which composed $S_{\text{ey}}(3)$ does not disappear from the HC-DAC output spectrum. Instead, when the partial DEM technique is applied, the spectral energy in $S_{\text{ey}}(3)$ gets spread into a white noise spectrum.

In summary, at the output of the HC-DAC, the proposed partial DEM technique spreads the y-axis mismatch error component of the $HD_3$ phasor into a white noise spectrum, while keeping the x-axis error component unchanged. Even though this discussion focused on $HD_3$ of a 4-bit HC-DAC, a similar case can be made for $HD_n$ of a $k$-bit HC-DAC, where $HD_n$ is a harmonic attenuated by the operation of the $k$-bit HC-DAC. Thus, it is clear that the proposed partial DEM technique has a positive qualitative effect on HC-DAC output SDR. The quantitative effect depends on the y-axis mismatch error component of each $HD_n$, which gets spread when the DEM technique is applied. As the y-axis mismatch error component of each $HD_n$ is a random variable depending on the random mismatch errors in a given HC-DAC, the quantitative effect of the partial DEM technique is also a random variable.

## 6.5 Behavioural Simulation Results

Numerical simulation results showing the effect of the proposed partial DEM technique are presented in this section. Simulations have been conducted using a behavioural model of an HC-DAC written in MATLAB. A 4-bit HC-DAC which uses 110 unit-current switches ($k = 4$, $M = 110$) was considered during simulations.

A 4-bit HC-DAC cancels lower order harmonics from $HD_2$ to $HD_8$. Moreover, according to the mathematical model presented in Chapter 5, for a 4-bit HC-DAC, $M = 110$ is a Pareto optimal amplitude resolution which theoretically results in an SDR of 79.9 dB for a matched HC-DAC.

When simulating mismatch affected HC-DACs, four values of unit-element mismatch standard deviation, $\sigma = \{0.1\ \%, 0.5\ \%, 1\ \%, 2\ \%\}$, were considered. For each value of $\sigma$, 1000 Monte Carlo samples of the HC-DAC were simulated with and without DEM. In each instance of simulating a Monte Carlo sample of the HC-DAC with partial DEM, 10 000 cycles of the HC-DAC output signal trace were used to calculate the SDR.

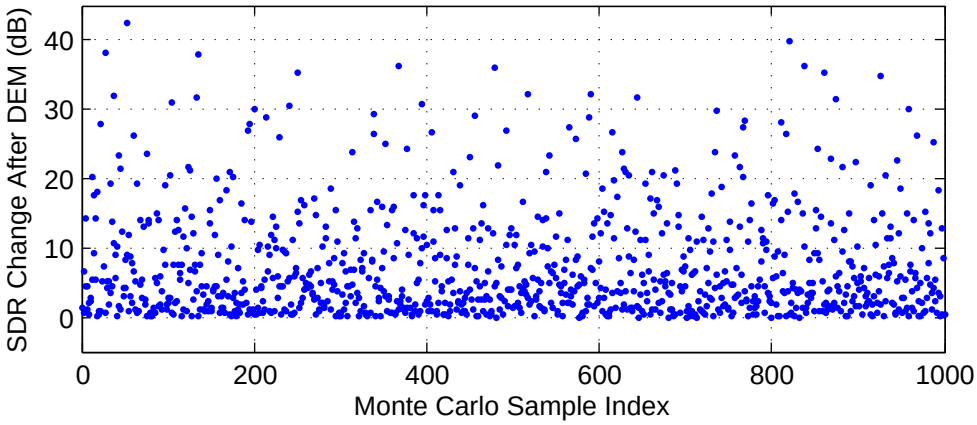


Figure 6.6: MC simulation results for change in SDR when DEM was applied to an HC-DAC ($k = 4$, $M = 110$) with 1% random mismatch

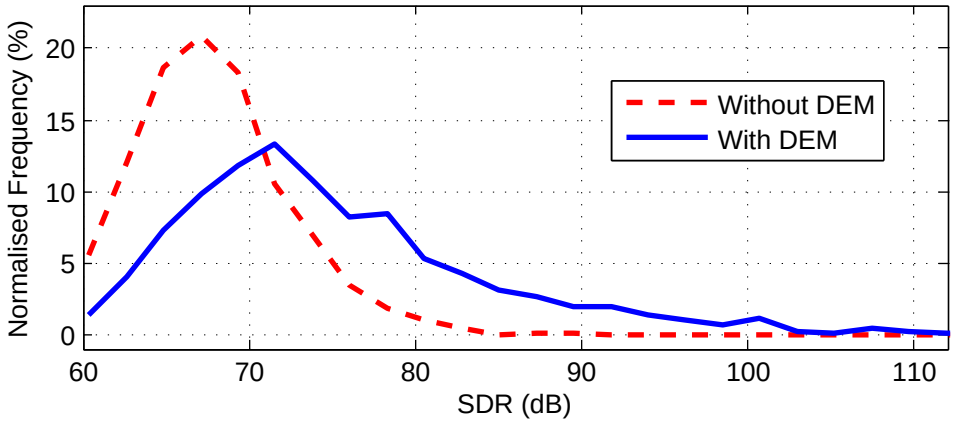


Figure 6.7: Histogram depicting MC simulation results for the effect of DEM on the SDR of an HC-DAC ($k = 4$, $M = 110$, $\sigma = 1\%$)

Figure 6.6 plots the change in SDR observed after applying the partial DEM technique to 1000 Monte Carlo samples of the HC-DAC with 1% mismatch. Note that the SDR change caused by the partial DEM technique was randomly distributed. Furthermore, all Monte Carlo samples of the HC-DAC experienced a positive change in SDR when the partial DEM technique was applied. The two observations made above agree with the conclusions made in Section 6.4.

Table 6.1 summarizes the statistics of SDR results obtained via Monte Carlo simulations. In the table, $N$ is the number of Monte Carlo samples considered, $\overline{X}_{\mathrm{SDR}}$ is the mean SDR, and $S_{\mathrm{SDR}}$ is the standard deviation of SDR for each case. For $\sigma = 1$ %, the Monte Carlo results obtained are illustrated as histograms in Fig. 6.7. The higher negative skew in the histogram of SDR results when DEM was active, compared to when DEM was inactive, reiterates the improvement in SDR caused by the application of the partial DEM technique.

Table 6.1: Statistics of SDR results obtained via Monte Carlo simulations of the HC-DAC with random mismatch

| $I_{\text{unit}}$ Mismatch ($\sigma$) | N | SDR Results Without DEM | | SDR Results With Partial DEM | |
|---|---|---|---|---|---|
| | | $\overline{X}_{\text{SDR}}$ | $S_{\text{SDR}}$ | $\overline{X}_{\text{SDR}}$ | $S_{\text{SDR}}$ |
| 0.1 % | 1000 | 79.8 dB | 2.9 dB | 80.6 dB | 3.8 dB |
| 0.5 % | | 73.2 dB | 4.4 dB | 79.2 dB | 8.5 dB |
| 1.0 % | | 68.0 dB | 4.6 dB | 75.1 dB | 9.1 dB |
| 2.0 % | | 61.9 dB | 4.5 dB | 69.3 dB | 9.5 dB |

## 6.6 Circuit Design

The design of the scrambler circuit is described in this section. As illustrated in Fig. 6.3, the scrambler circuits, which implement the partial DEM technique, are placed right before the HC-DAC in the DHSS architecture.

The circuit design of a single scrambler is illustrated in Fig. 6.8. Each scrambler uses a 1–bit pseudo-random signal to switch the 1–to–1 mapping between its inputs and outputs. The pseudo-random signals required for the scramblers can be provided using an m-sequence LFSR [Tsa64]. Then, the sampling frequency of the LFSR output signal determines the rate at which the scramblers perform DEM.

## 6.7 Summary

In this chapter, we presented an area and power cost efficient DEM technique custom made for HC-DACs. First, the effect of mismatch errors on the SDR of an HC-DAC output signal was discussed in detail. It was shown that mismatch errors could have a positive, negative, or no impact on the SDR of the HC-DAC output, but in a vast majority of cases, the impact will be negative. Next, the effect of applying a

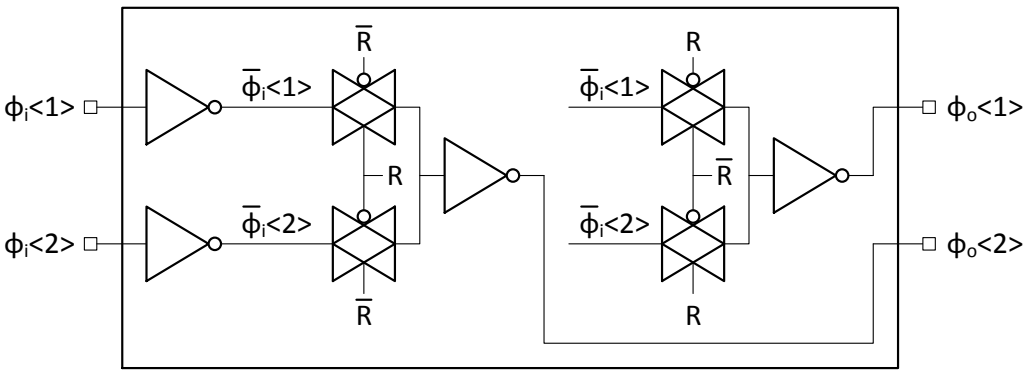


Figure 6.8: Scrambler circuit design

generic DEM technique in HC-DACs was discussed, and then the effect of a complete mismatch scrambled DEM technique was considered. It was shown mathematically, that a complete DEM technique could entirely eradicate the effect of mismatch errors, but the cost of implementing a complete DEM technique is impractical. Then, we proposed a partial mismatch scrambled DEM technique, which reduces the influence of mismatch while preserving the area and power cost efficiency of DHSSs. Providing theoretical discussions as well as simulation results from a behavioural HC-DAC model, it was shown that the partial DEM technique always has a positive impact on SDR. We also pointed out that the absolute effect of the partial DEM technique on SDR is a random variable, which depends on the mismatch error profile of each HC-DAC. Finally, we discussed the design of the scrambler circuit, which is used to scramble two square-wave signals in the partial DEM technique. Each scrambler circuit consists of four inverters and four transmission gates.

# Part III

# Integrated Circuit Implementation and Test Results

# Chapter 7

# Test-Chip Development

## 7.1 Overview

Thus far in this thesis, we have proposed a DHSS hardware architecture that supports phase programmability, an HC-DAC design method which breaks the 6 dB/bit rule, and a DEM technique which reduces the impact of mismatch in HC-DACs. Furthermore, we have listed one known application and proposed two new applications for DHSSs. The purpose of this chapter is to describe the development of a test chip to verify these theoretical proposals in silicon.

The test chip was designed and implemented using an STMicroelectronics 130 nm CMOS technology. The IC design work was conducted mainly using Cadence ICFB 5.1.41, while Mentor Graphics' Calibre tools and the StarRC tool by Synopsys were used for physical verification and parasitic extraction, respectively.

The rest of the chapter is structured as follows. Section 7.2 describes the content of the test chip. Section 7.3 and Section 7.4 detail the integrated circuit design of the two DHSS prototypes included in the test chip. Section 7.5 discusses top-level design

of the test chip, while Section 7.6 delineates the design of the printed circuit board (PCB) on which the test chip was mounted. Section 7.7 details the measurement setup used for the test chip. Finally, Section 7.8 summarizes the chapter.

## 7.2 Content of the Test-Chip

### 7.2.1 The DHSS Prototypes

Two DHSS prototypes were fabricated as part of the test chip. The characteristics of the two DHSS prototypes were chosen such that measurement results from the two DHSSs could verify the theoretical proposals made in this thesis. Table 7.1 summarizes the design characteristics selected for each DHSS prototype.

DHSS–1 was aimed to be used as an on-chip test signal synthesizer, as described in Section 3.4. It was chosen to be a 4–bit DHSS, such that harmonics from $HD_2$ to $HD_8$ are cancelled. According to Section 5.3, a Pareto optimal amplitude resolution of 110 (6.8–bit), which results in an ideal SDR of 79.9 dB, was selected for the HC-DAC inside DHSS–1. Furthermore, the DEM technique proposed in Section 6.4 was implemented in DHSS–1 to reduce the impact of mismatch in the HC-DAC.

DHSS–2 was directed to be utilized as a PSK polar modulator or as a PSK baseband IQ DAC according to Section 3.4. It was chosen to be a 7–bit DHSS, and the DPG was designed as described in Section 4.3, such that the phase programming resolution

Table 7.1: Design characteristics of the two DHSS prototypes

| Name | $k$ | $M$ | DEM | Phase Programmable | $SDR_{ideal}$ |
|---|---|---|---|---|---|
| DHSS–1 | 4–bit | 110 (6.8–bit) | Yes | No | 79.9 dB |
| DHSS–2 | 7–bit | 37 (5.2–bit) | No | Yes | 42.1 dB |

is 4–bit. Also, the 7–bit DHSS–2 is capable of cancelling lower order harmonics from $HD_2$ to $HD_{14}$, while being used as a PSK polar modulator. A Pareto optimal amplitude resolution of 37 (5.2–bit) was selected for the HC-DAC inside DHSS–2 by using the mathematical model proposed in Section 5.3, such that the ideal SDR of the DHSS-2 output is equal to 42.1 dB.

### 7.2.2 The Supporting Circuits

In addition to the two DHSSs, supporting circuit blocks were included in the test-chip as illustrated in Fig. 7.1. A bias current synthesizer was used to generate the reference currents for unit-current switches in the two DHSSs, while the option of providing an off-chip reference current was also made available. The clock manager inside the test-chip contained a voltage controlled ring oscillator and clock dividers. The option of providing an external clock signal was also made available. A 15-bit m-

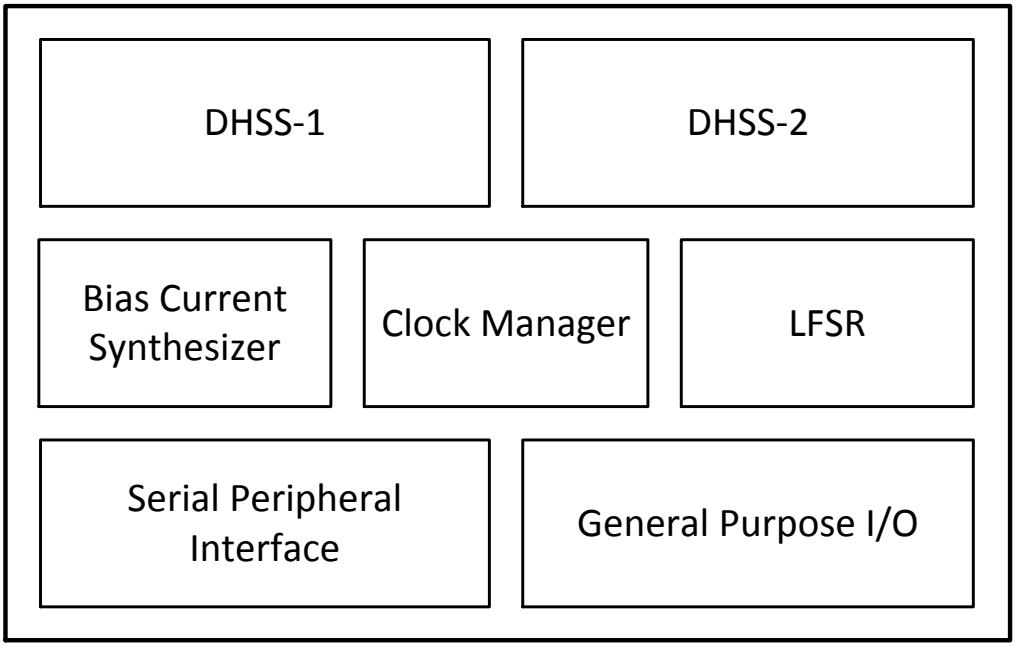


Figure 7.1: Main circuit blocks in the test-chip

sequence LFSR [Tsa64] was included in the test chip to generate a pseudo random signal for DEM in DHSS–1 and to provide a pseudo-random baseband signal for PSK modulation in DHSS–2. A serial peripheral interface (SPI) was implemented in the chip to program the chip into different test modes, while a general purpose input/output interface was implemented to support off-chip access to on-chip signals.

## 7.3 DHSS–1: Integrated Circuit Design

The integrated circuit design of DHSS–1, consisting of a 4-bit HC-DAC which uses 110 unit-current switches (6.8-bit amplitude resolution), and a 4-bit DPG which enables partial DEM, is presented in this section. Figure 7.2 illustrates the integrated circuit architecture of DHSS–1.

In the 4-bit DPG, the four phase shifted square-waves were synthesized as 1-bit digital signals using a ring counter as delineated in Section 4.2. The shift register was clocked at a rate of $10f_{\mathrm{o}}$, where $f_{\mathrm{o}}$ is the desired sine-wave frequency. Thus, the square-wave outputs from the shift register had a frequency of $f_{\mathrm{o}}$, and the time-shift between two consecutive square-waves was $T/10$, where $T = 1/f_{\mathrm{o}}$.

The second stage of the DPG contained the scramblers, the design of which has been described in Section 6.6. The pseudo-random signals required for the scramblers were provided using an on-chip 15–bit m-sequence LFSR [Tsa64]. The LFSR was run at a clock frequency of $f_{\mathrm{dem}}$, which determined the rate at which the scramblers operated.

The outputs from the scramblers were clocked by a 4-bit register to align the timing of signal transitions, which helped reduce timing errors at the HC-DAC input. At the register output, both true and complimentary signals are taken, as the HC-DAC was designed differentially.

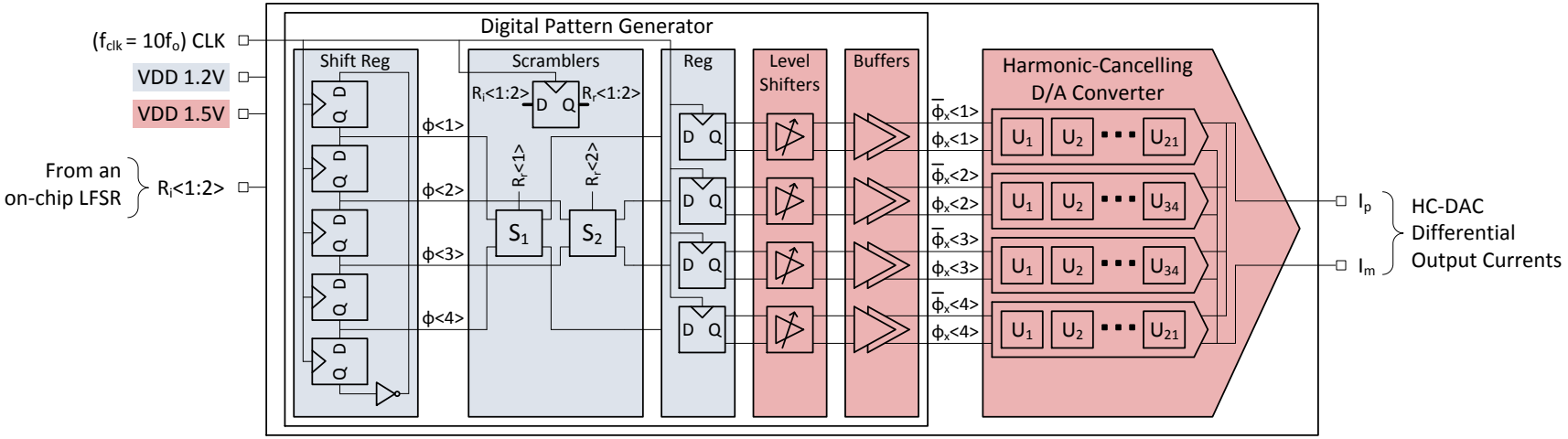


Figure 7.2: DHSS–1 IC architecture including the 4-bit DPG, and the 4–bit, 110 (6.8-bit) amplitude resolution HC-DAC

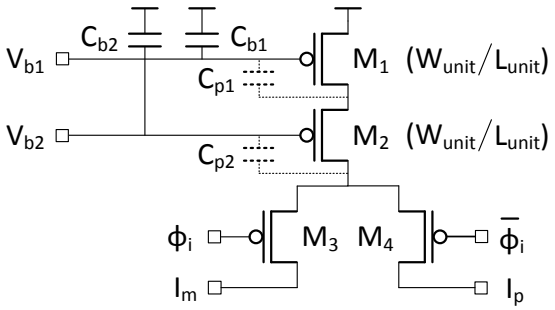


Figure 7.3: Unit-current switch design

The shift register, the scramblers, and the register worked with a 1.2 V power supply, while the level-shifters, the buffers, and the HC-DAC worked with a 1.5 V power supply. The circuits working at 1.5 V were implemented with dual-oxide transistors. The level-shifters were designed with the conventional differential topology [dRdSCL08], while the buffers were designed using scaled inverter stages.

As the HC-DAC in Fig. 7.2 illustrates, out of the 110 total unit-current switches used in the HC-DAC, 21 each were allocated to $\phi_1(t)$ and $\phi_4(t)$, while 34 each were allocated to $\phi_2(t)$ and $\phi_3(t)$. The unit current switch allocations were calculated using Eq. 5.3 and Eq. 5.4.

The unit-current switch design used in the HC-DAC is shown in Fig. 7.3. Transistors $M_1$ and $M_2$ form a cascode PMOS current source, which was designed to supply a unit-current of 5 uA. During the circuit design, dimensions of $M_1$ and $M_2$ were scaled to keep the unit-current mismatch standard deviation ($\sigma$) to 1 %. In order to improve the output resistance of the unit-current switches, and consequently, the output resistance of the HC-DAC, dual-oxide transistors were used for $M_1$ and $M_2$. As illustrated in Fig. 7.3, the two nets that supply bias voltages to the unit-current sources are coupled to the power supply using capacitors, $C_{b1}$ and $C_{b2}$. The purpose of $C_{b1}$ and $C_{b2}$ is to reduce the effect of the gate-drain parasitic capacitors, $C_{p1}$ and $C_{p2}$, which couple input dependent distortions into the bias voltage nets.

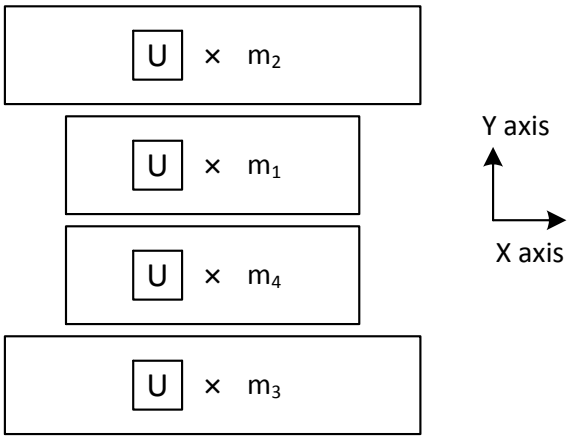


Figure 7.4: A simple layout structure for the HC-DAC in DHSS–1

A simple layout structure for the HC-DAC is proposed in Fig. 7.4. Each set of unit elements controlled by a given input signal were placed in sequence parallel to the x-axis, making signal routing simpler, thus leading to a compact layout. Assuming a linear process gradient, as each row of unit elements share a common vertical axis of symmetry, the proposed layout structure can eliminate the effect of the x-axis component of the process gradient.

The partial DEM technique can eliminate the y-axis component of the process gradient related mismatch. Note that the layout structure is symmetrical around a horizontal axis in the middle between the $m_1$ unit row and the $m_4$ unit row. Thus, $E_{\mathrm{mm}}(i) = -E_{\mathrm{mm}}(5-i)$, where $i \in \{1,2,3,4\}$ and $E_{\mathrm{mm}}(i)$ was defined in Eq. 6.5. Consequently, when the partial DEM technique is applied, $\overline{E}_{\mathrm{pdm}}(i) = 0$, according to Eq. 6.17.

Figure 7.5 shows the integrated circuit layout of DHSS–1. Note that the total area of DHSS–1 was 0.066 $\mathrm{mm}^2$.

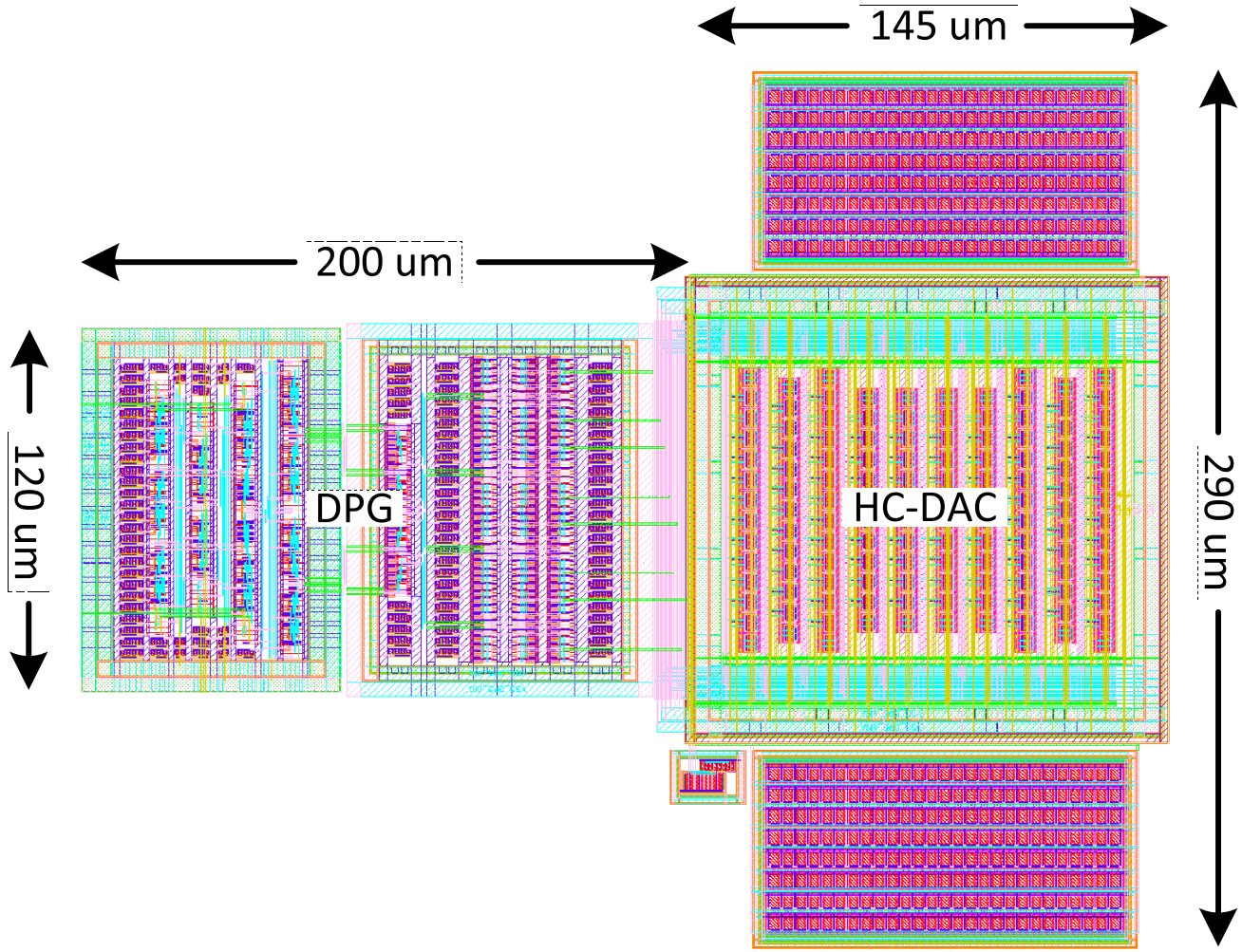


Figure 7.5: DHSS–1 integrated circuit layout

## 7.4 DHSS–2: Integrated Circuit Design

The integrated circuit design of DHSS–2, consisting of a 7-bit DPG which enables phase programmability with 4-bit phase resolution, and a 7-bit HC-DAC which uses 37 unit-current switches (5.2-bit amplitude resolution), is presented in this section. Figure 7.6 illustrates the integrated circuit architecture of DHSS–2.

The 7-bit, phase programmable DPG was designed as discussed in Section 4.3. At the phase-to-amplitude converter output, both true and complimentary signals were taken, as the HC-DAC required differential input signals. The buffers were designed using scaled inverter stages.

In the HC-DAC, out of the 37 unit-current switches, 3 each were allocated to $\phi_1(t)$ and $\phi_7(t)$, 5 each were allocated to $\phi_2(t)$ and $\phi_6(t)$, and 7 each were allocated to $\phi_3(t)$, $\phi_4(t)$, and $\phi_5(t)$. The allocation of unit current switches was calculated using Eq. 5.3 and Eq. 5.4.

The unit-current switches employed in the HC-DAC were designed to supply 10 uA of current using a similar design to Fig. 7.3. The area of the cascode current mirror was scaled for 1% mismatch. However, thin-oxide transistors were used in the current mirror design, and $C_{b1}$ and $C_{b2}$ were omitted. The main reasons for using thin-oxide devices instead of thick-oxide devices were that the higher output resistance of thick-oxide devices was not necessary to reach the 44.5 dB target SDR of DHSS–2, the reduction in HC-DAC power consumption, and the increase in HC-DAC operating speed. The rationale for omitting the bias coupling capacitors was that the distortions coupled into the bias voltage nets via the gate-drain capacitors were not limiting us from reaching the 44.5 dB target SDR of DHSS–2. A layout structure similar to the one illustrated in Fig. 7.4 was used for the HC-DAC, even though DHSS–2 did not implement DEM. Figure 7.7 shows the integrated circuit layout of DHSS–2. Note that the total area of DHSS–2 was 0.046 $mm^2$.

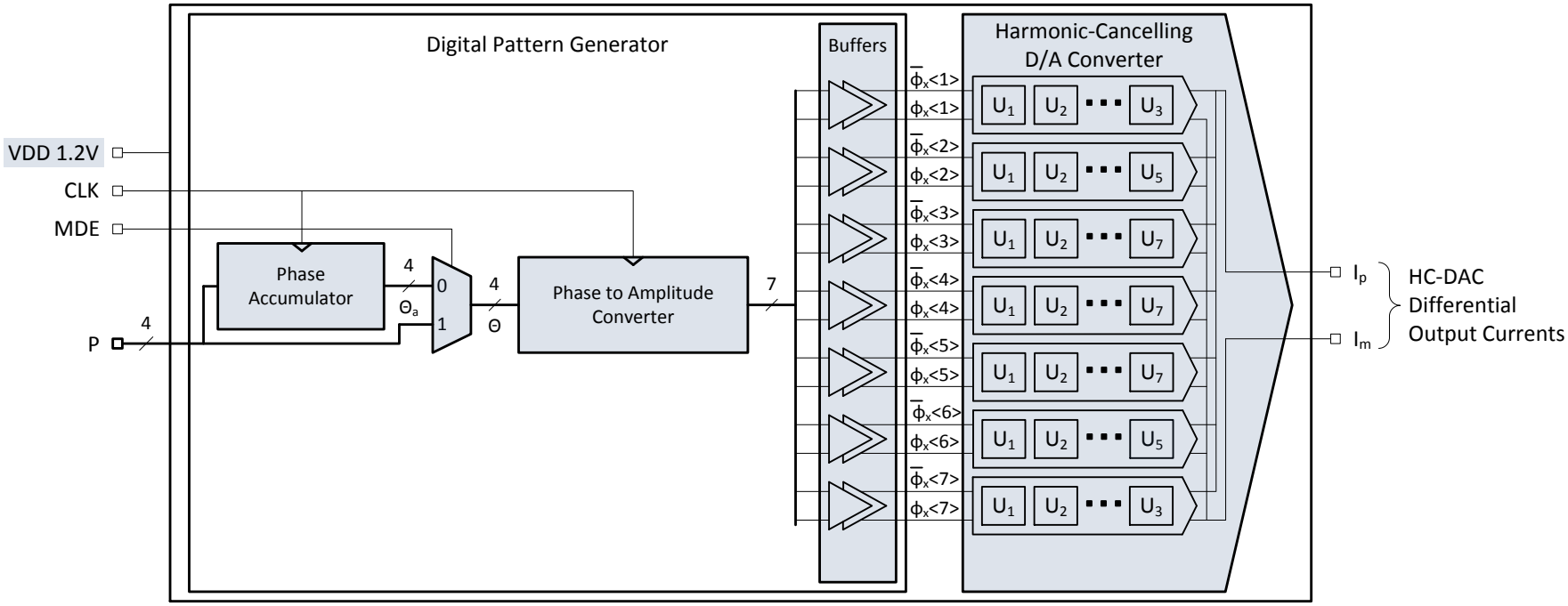


Figure 7.6: DHSS–2 IC architecture including the 7-bit DPG, and the 7–bit, 37 (5.2-bit) amplitude resolution HC-DAC

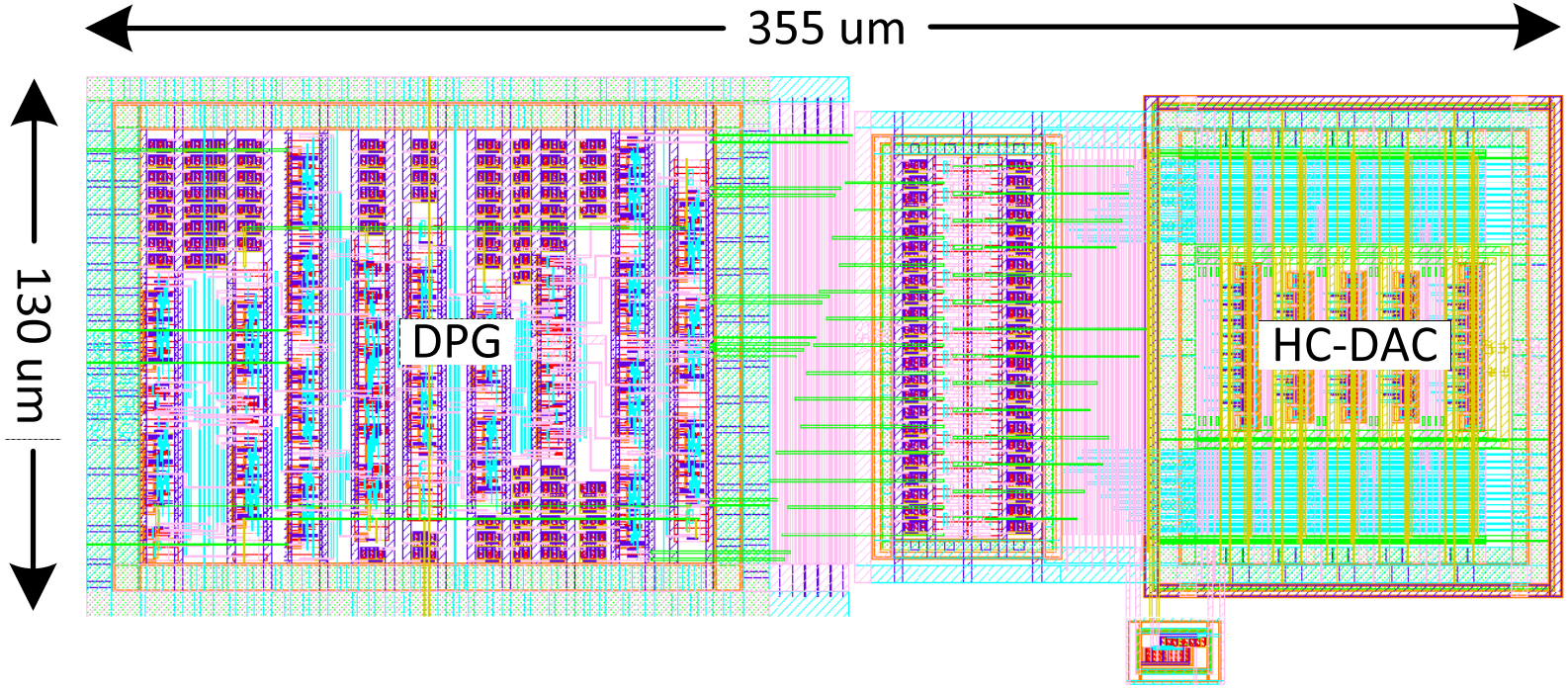


Figure 7.7: DHSS–2 integrated circuit layout

## 7.5 Top Level Chip Design

Design decisions taken regarding the test-chip top-level are discussed in this section. Figure 7.8 illustrates the top-level layout of the test-chip, while Fig. 7.9 annotates different blocks in the top-level test-chip layout. A micrograph of the fabricated test-chip is shown in Fig. 7.10. The total area of the test-chip was 1.2 $mm^2$.

The test-chip consisted of five VDD inputs: 1.2 V digital, 1.2 V analog, 1.2 V bias, 1.5 V analog, and 1.5 V bias, and three separate VSS connections: digital, analog, and bias. Out of the 32 bond pads of the test-chip, 16 pads were allocated to VDD and VSS connections.

As a general rule, the top-level floorplan of the test-chip was designed such that sensitive analog circuit blocks and bond pads were placed in the upper portion of the layout, and noisy digital circuit blocks and pads were put in the lower portion. The HC-DACs of the DHSSs were placed close to the pads which take out the DHSS output currents, so that the parasitic resistance, capacitance, and inductance of the on-chip signal paths were reduced. The same principal was applied to other circuit blocks, which connect to the remaining input/output pads. The bias circuits and the bias input/supply pads were placed in the upper left corner of the layout, away from the noisy circuitry and pads. However, the placement of the bias circuit meant that the bias current signals had to travel a relatively long distance to reach the DHSSs. To protect the bias references, the metal wires carrying the bias currents were shielded.

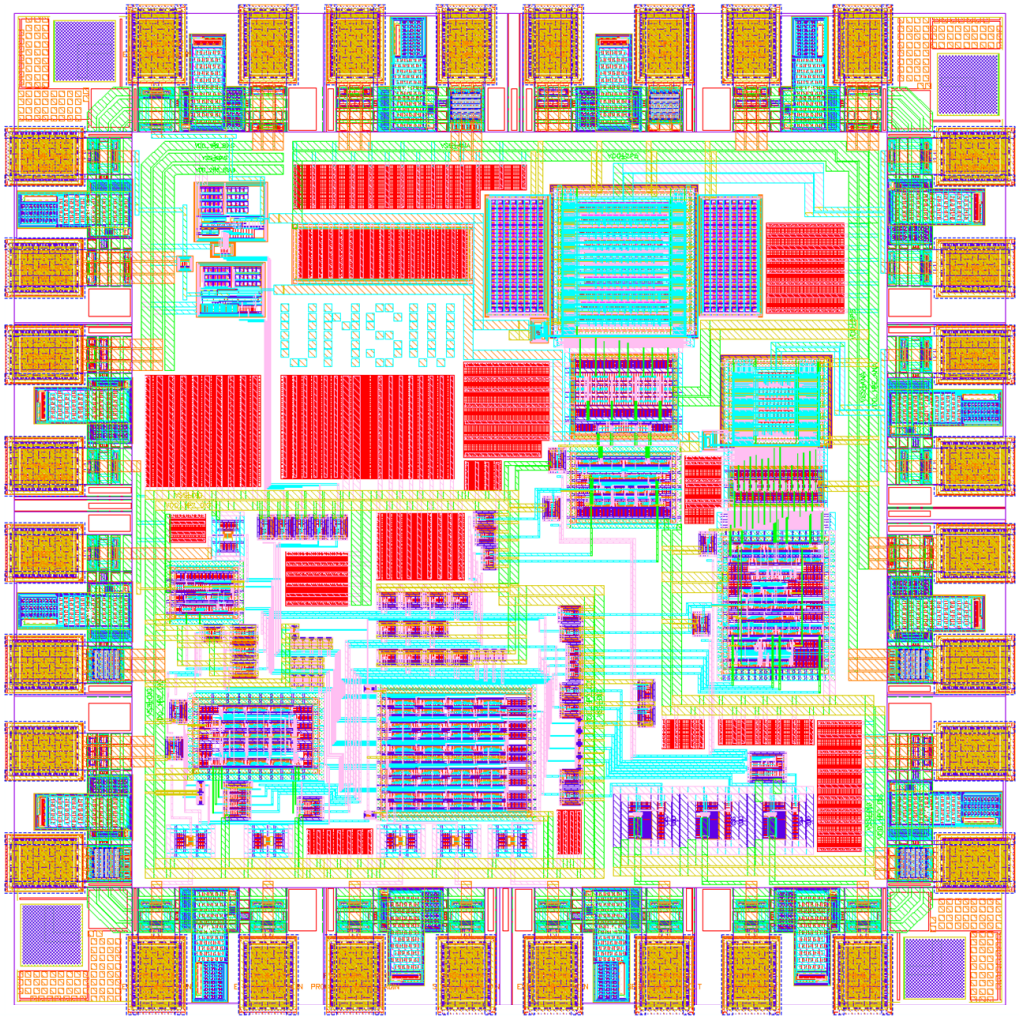

Figure 7.8: Top-level test-chip integrated circuit layout

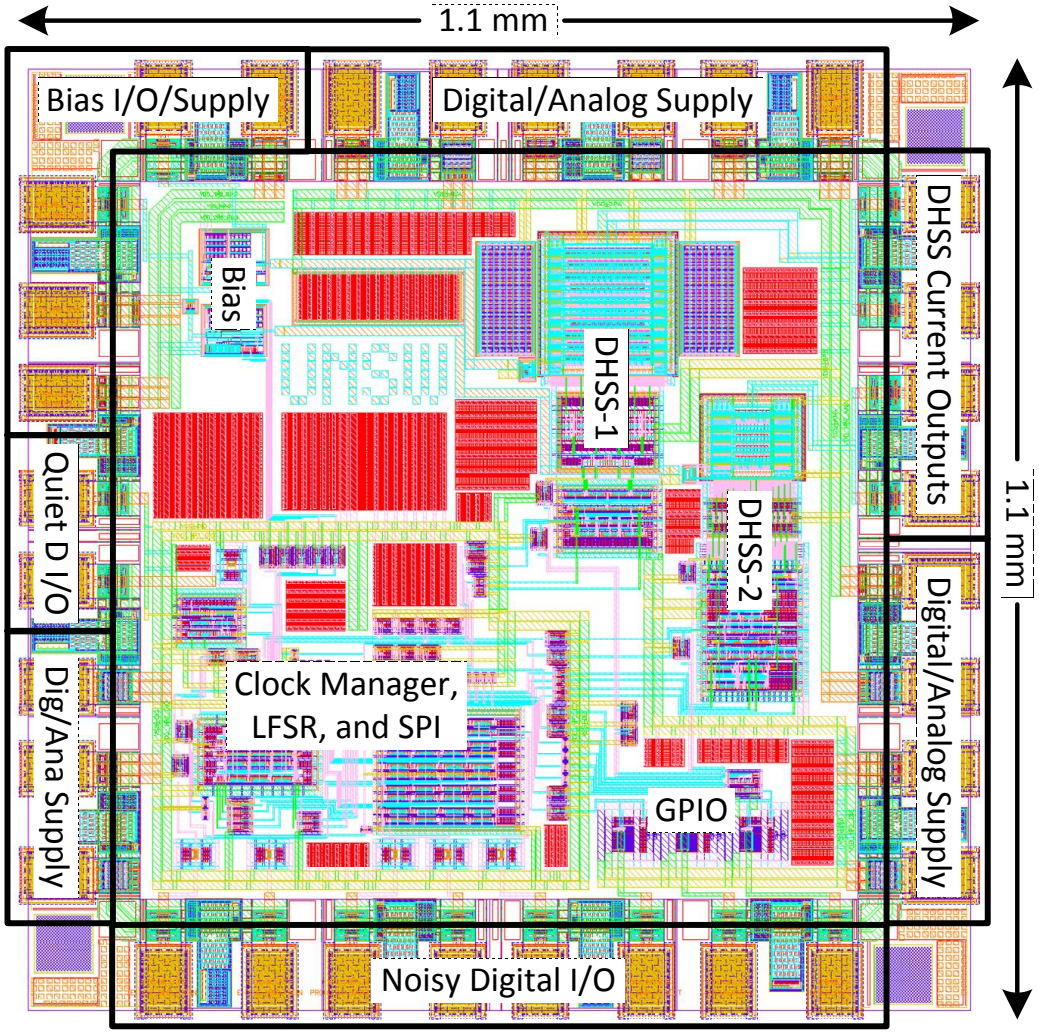


Figure 7.9: Top level test-chip integrated circuit layout with annotations

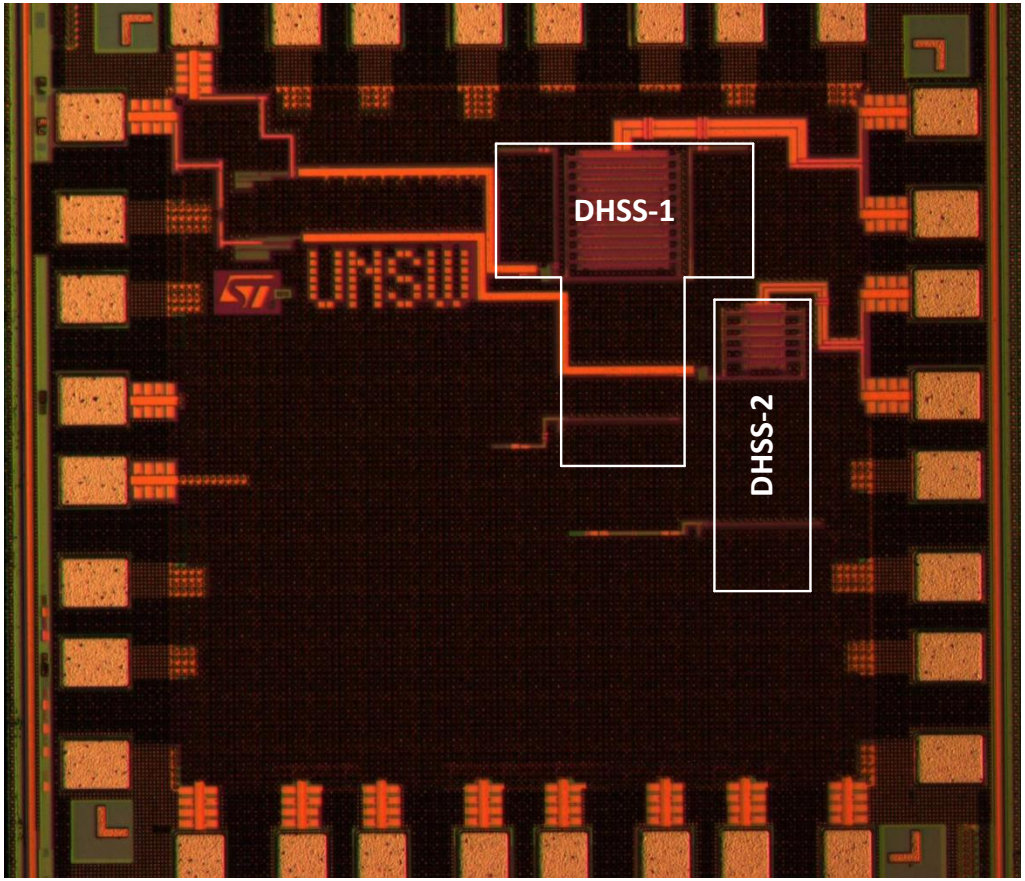


Figure 7.10: Micrograph of the fabricated test-chip

## 7.6 PCB Design

The design of the PCB, on which the test-chip was mounted, is shown in Fig. 7.11. A 4–layer PCB (signal, VSS, VDD, signal) was designed, with dedicated VDD and VSS planes to reduce parasitic inductances and to improve power supply decoupling.

As shown in the left side image in Fig. 7.11, the VSS layer was divided into three regions: VSS digital, VSS analog, and VSS bias, with a star connection underneath the test-chip. As the image on the right side shows, the VDD layer was divided into six isolated domains: 1.2 V digital, 1.2 V analog, 1.2 V bias, 2.5 V analog, 2.5 bias, and 5 V digital. Note that the 5 V digital supply was only used by on-board level shifters (5 V to 1.2 V).

Each signal trace was routed directly above the corresponding VSS and VDD regions in order to keep the return current path directly underneath the signal trace, thereby reducing the parasitic inductance associated with the signal trace. Note that no signal trace crosses a VSS region boundary. To further improve signal integrity, the high-frequency signal traces routed to and from the SMA (SubMiniature version A) connectors (DPG clock, LFSR clock, DHSS–1 differential outputs, and DHSS–2 differential outputs) were impedance controlled to 50 Ω, and properly terminated at each end.

## 7.7 The Measurement Setup

The testing setup used for the test-chip is depicted in Fig. 7.12. The SPI inputs to the test-chip were provided using an Arduino UNO board. The configuration of the DPG clock, LFSR clock, and the bias current will be detailed in Chapter 8 while discussing different measurements.

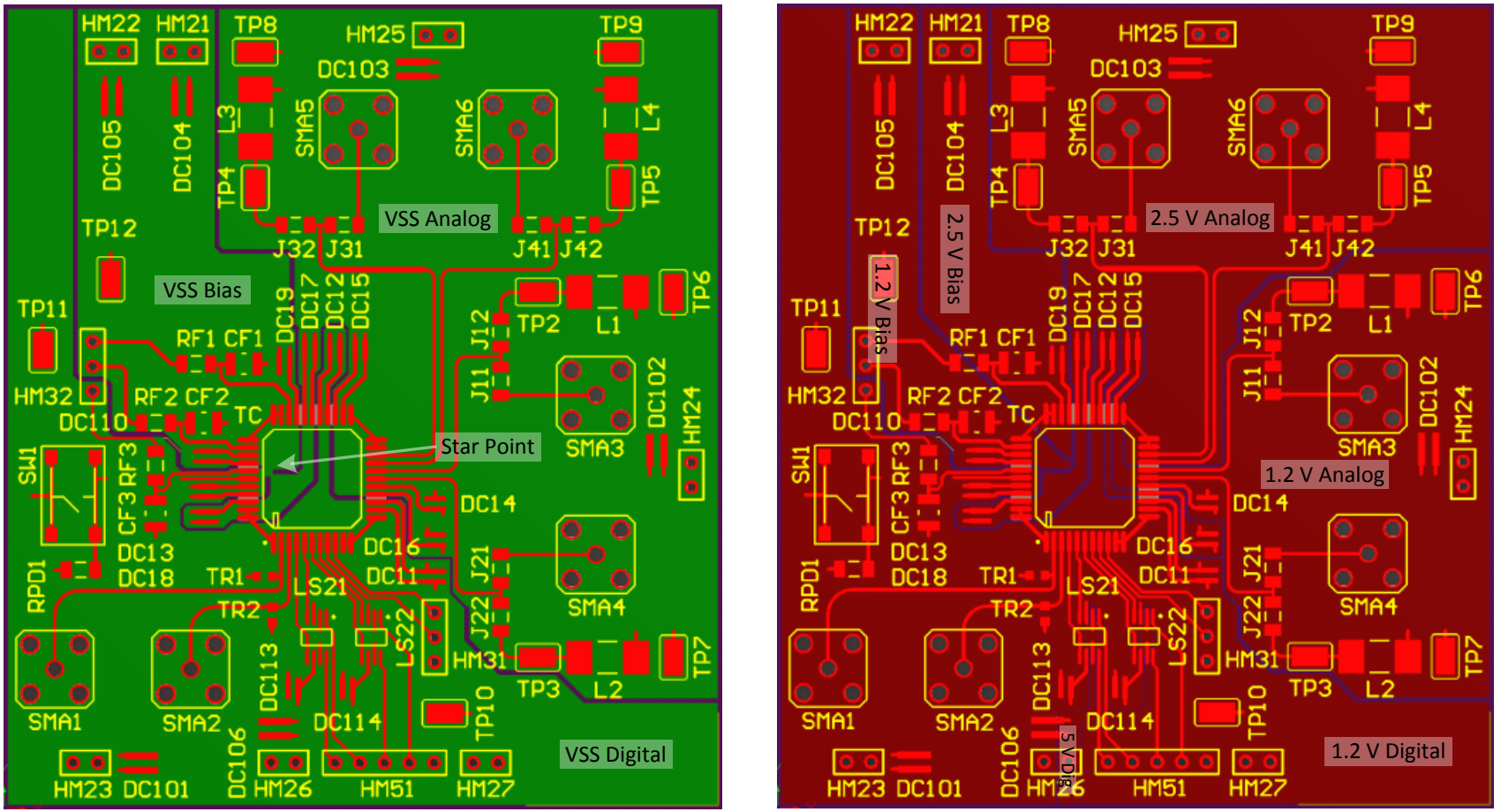


Figure 7.11: PCB layout with annotations. Left: signal layer (red) and the VSS layer (green), right: signal layer and the VDD layer (maroon)

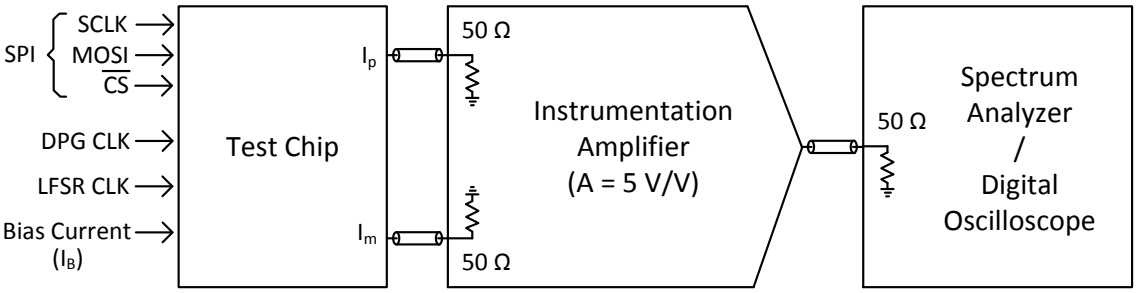


Figure 7.12: The test setup

The differential current outputs of the DHSS being measured, $I_{\mathrm{p}}$ and $I_{\mathrm{m}}$, were taken off-chip and fed into an Instrumentation Amplifier (IA) with 50 Ω input impedance. The IA was required because the spectrum analyzer accepted single-ended inputs. The CN-0273 Circuit Evaluation Board by Analog Devices [AD112] was used as the IA in this work. The output of the IA was measured using the spectrum analyzer [KS114] or the digital oscilloscope [NIA05] depending on the nature of the experiment.

## 7.8 Summary

In this chapter, we discussed the test-chip which was developed to empirically verify the theoretical findings of this research. First, we reviewed the contents of the test-chip. Two DHSS prototype circuits were included in the chip. The first DHSS prototype (DHSS–1) was a 4–bit DHSS with 6.8–bit amplitude resolution, DEM, and an ideal SDR of 79.9 dB. DHSS–1 was targeted for on-chip test signal generation applications. The second DHSS prototype (DHSS–2) was a 7–bit DHSS with 5.2–bit amplitude resolution, phase programmability, and an ideal SDR of 42.1 dB. DHSS–2 was targeted for use as a baseband IQ DAC or as a polar IF modulator in a PSK communication application. Then, we looked into the design of the two DHSS prototype circuits. As part of discussing the design, we went through the

detailed architecture of each DHSS, the design of the unit-current cell, and the layout structure of the HC-DAC. Next, we discussed the design decisions made at the chip top-level, and in the PCB. Finally, we detailed the measurement setup used for the test-chip.

# Chapter 8

# Test-Chip Measurements and Discussions

## 8.1 Overview

This chapter presents and discusses measurements related to DHSS–1 and DHSS–2 obtained from the fabricated test-chip. The rest of the chapter is structured as follows. Section 8.2 presents and discusses DHSS–1 measurements. Measurement results obtained from DHSS–1 practically verify the applicability of DHSS–1 as an on-chip sinusoidal test signal synthesizer, the effectiveness of the Pareto optimal HC-DAC design method proposed in Chapter 5, and the effectiveness of the DEM technique proposed in Chapter 6. Section 8.3 propounds and analyzes measurement results from DHSS–2. DHSS–2 measurements empirically evaluate the dual usage of DHSS–2 as a PSK IQ DAC and as a PSK polar IF modulator as proposed in Chapter 3, the phase-programmable DPG design proposed in Chapter 4, and again the Pareto optimal HC-DAC design technique presented in Chapter 5. Finally, Section 8.4 summarizes the chapter.

## 8.2 DHSS–1 Measurements and Discussion

### 8.2.1 Measurement Results

DHSS-1 measurements were conducted by setting the DPG clock signal frequency to $10f_o$, given a desired DHSS-1 output frequency $f_o$. The external bias current input was set to 5 uA to bias the unit-current switches used in the HC-DAC of DHSS-1. The internal LFSR was clocked using an on-chip voltage-controlled ring oscillator based clock synthesizer. The LFSR clock frequency, which was also the DEM switching frequency, was kept between $3f_o$ and $4f_o$.

Figure 8.1 charts SDR measurements from four test-chips at 1 MHz output frequency ($f_o$ = 1 MHz) with and without DEM activated. To create an output signal with 1 MHz frequency, $f_{clk}$ was set to 10 MHz. Deactivation of DEM was done by grounding $R_i$<1:2>, which was the signal controlling the scrambling operation, as shown in Fig. 7.2. As illustrated in Fig. 8.1, each test-chip clearly demonstrated an improvement in SDR when DEM was activated. Between the four test-chips, the SDR improvement ranged from 2 dB to 5 dB. Such variation in the quantitative effect of the partial DEM technique was theoretically explained in Section 6.4.

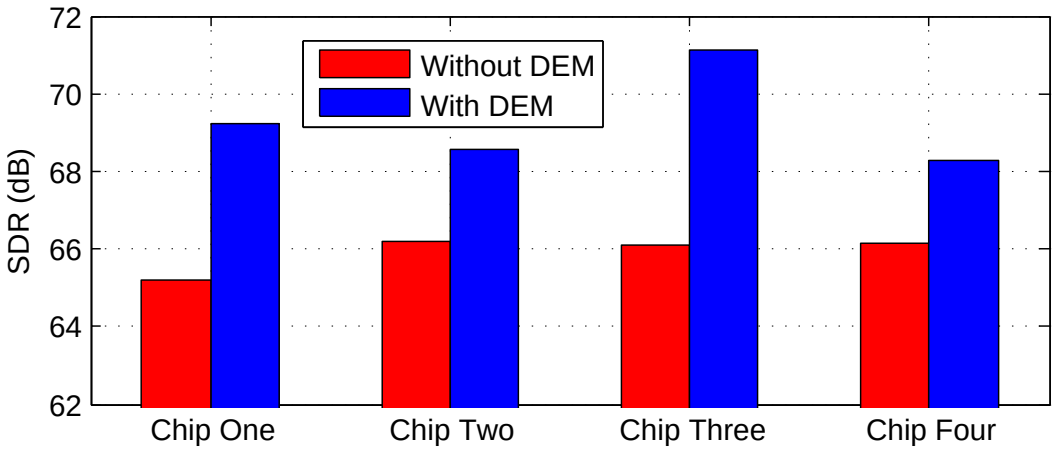


Figure 8.1: DHSS–1 output SDR results at 1 MHz output frequency from four test-chips

The DHSS–1 output spectrums from Chip One at 1 MHz output frequency, without DEM activated, and with DEM activated are shown in Fig. 8.2 and Fig. 8.3, respectively. By comparing the two spectrums, it can be noted that when the DEM technique was applied, there was a significant reduction in $HD_3$ and $HD_5$.

In both spectrums, note that $HD_9$ is close to $-19$ dBc. As discussed in Section 3.2, in a $k$-bit HC-DAC output, $HD_{2k+1}$ should theoretically be $-20 \times \log(2k+1)$ dBc, regardless of the amplitude scaling accuracy of the HC-DAC. Although $HD_{2k+1}$ is not part of the SDR calculation, it is a useful indication of the amount of filtering applied to the HC-DAC output. In the 4-bit HC-DAC implemented in this work, $HD_9$ is expected to be $-19.1$ dBc, which is consistent with the $HD_9$ measurements in Fig. 8.2 and Fig. 8.3. Thus, it is clear that at 1 MHz, the HC-DAC output signal had not undergone any parasitic filtering prior to being measured by the spectrum analyzer. At higher frequencies, it was observed that the limited bandwidth of the IA was attenuating harmonics at higher frequencies. As a solution, the frequency response of the IA was measured, and the impact of the IA was calibrated out from each affected harmonic before calculating the SDR.

Measured SDR variation against output frequency from Chip One is illustrated in Fig. 8.4. The output frequency range considered was from 500 kHz to 20 MHz. Measurements below 500 kHz were affected by the low-frequency noise floor of the spectrum analyzer, which is noted in Fig. 8.2. Figure 8.4 shows that at lower output frequencies, applying the partial DEM technique increased the SDR. In contrast, at higher frequencies, the partial DEM technique was not able to make a positive impact on SDR. These observations will be discussed further in the next subsection.

The measured power consumption of DHSS–1 against output frequency is plotted in Fig. 8.5. At 2 MHz and 20 MHz output frequencies, activating the partial DEM technique increased the power consumption by approximately 1 % and 4 %, respectively. The breakdown of power consumption between the two power supplies and

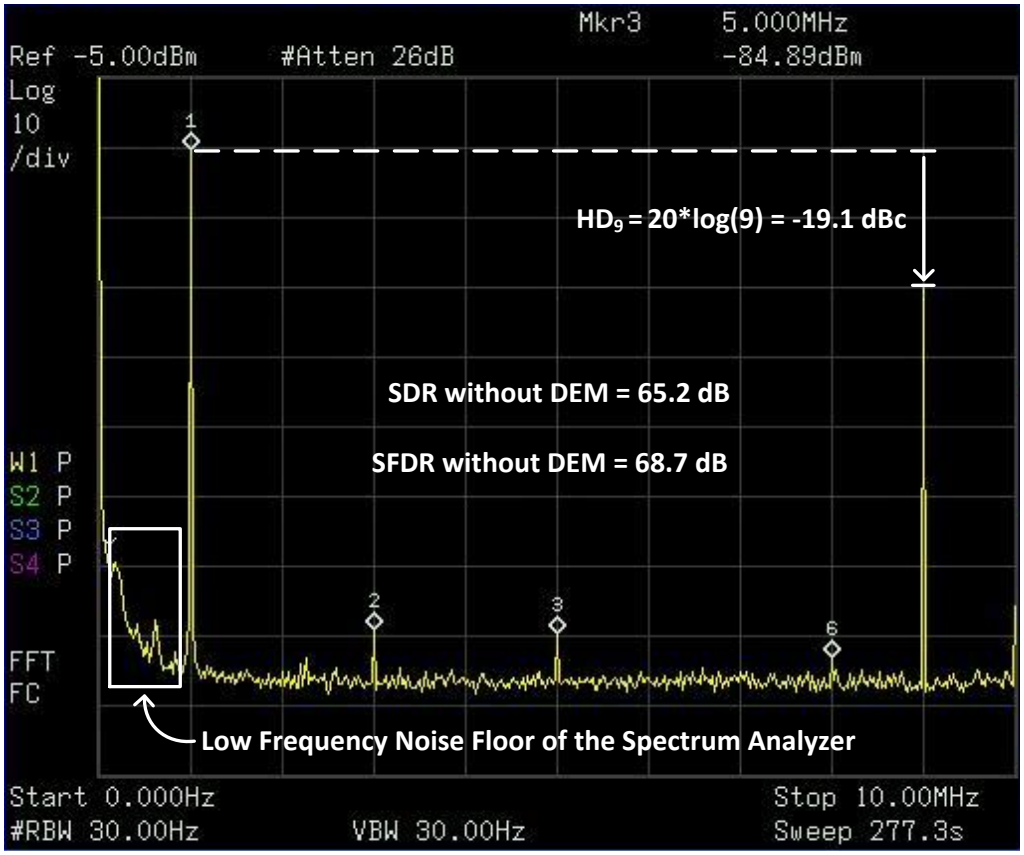


Figure 8.2: DHSS–1 output spectrum from Chip One at 1 MHz output frequency without DEM

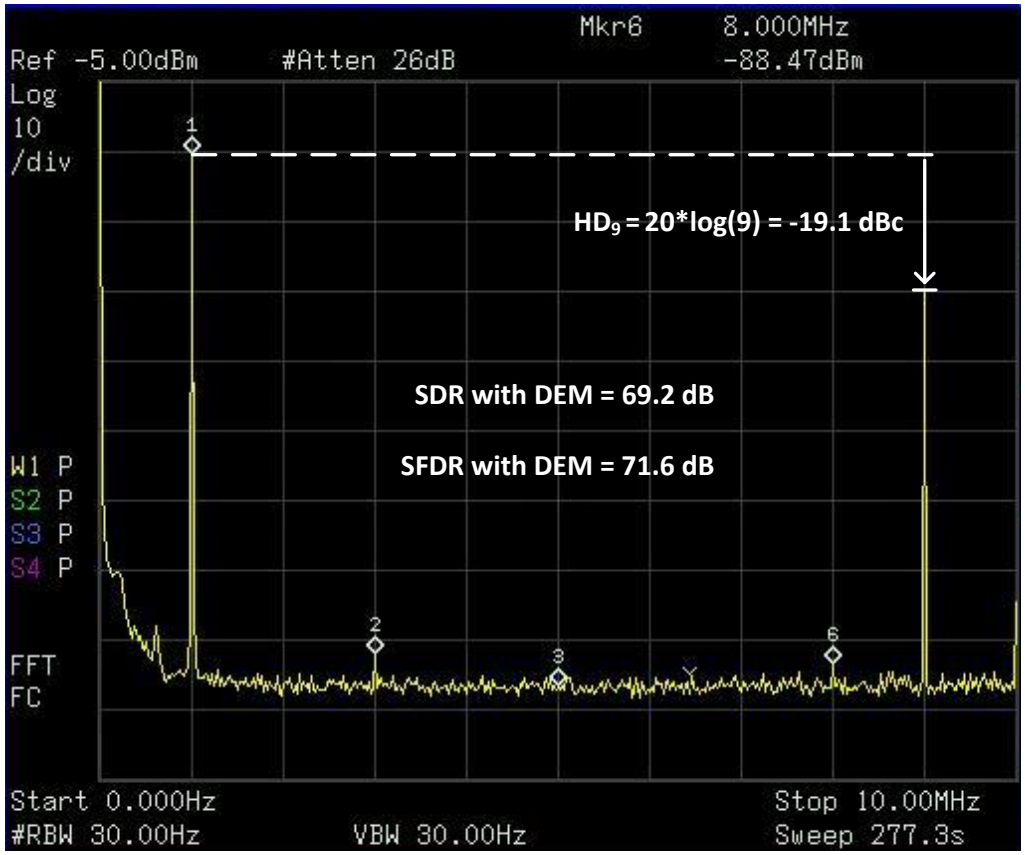


Figure 8.3: DHSS–1 output spectrum from Chip One at 1 MHz output frequency with DEM

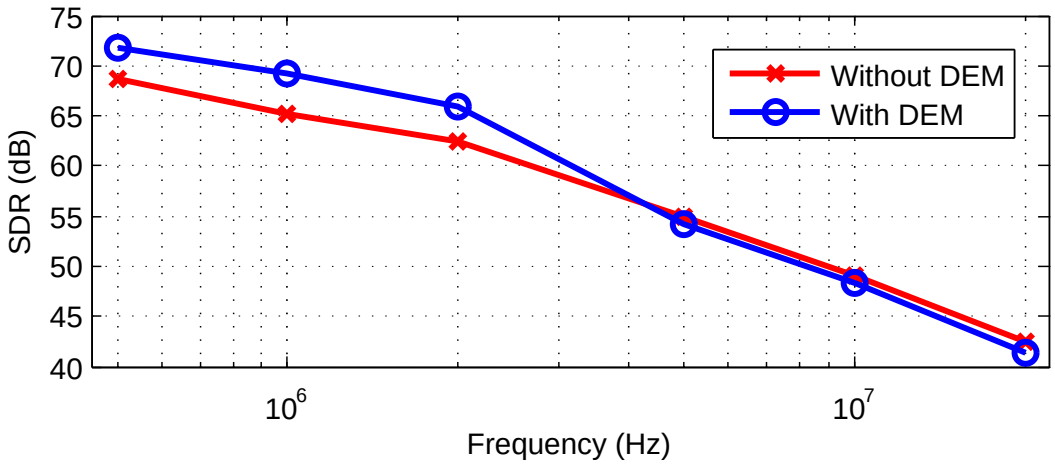


Figure 8.4: SDR versus output frequency with and without DEM

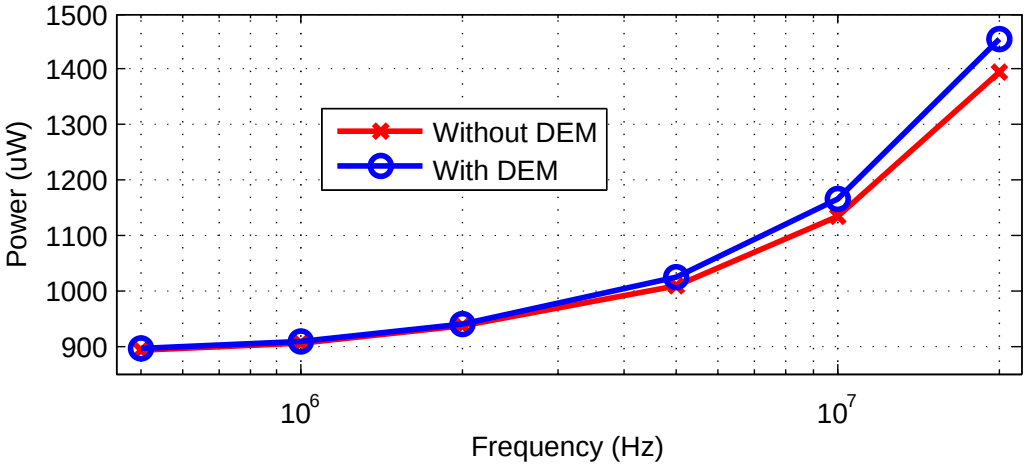


Figure 8.5: Power versus output frequency with and without DEM

between the two main circuit sub-systems, at 1 MHz output frequency with DEM activated, are illustrated in Fig. 8.6. It can be noted that among the two power supplies, 98 % of the total power was provided by the 1.5 V power supply, and between the DPG and the HC-DAC, 91 % of the total power was consumed by the HC-DAC. The HC-DAC required high power consumption due to its current-steering architecture.

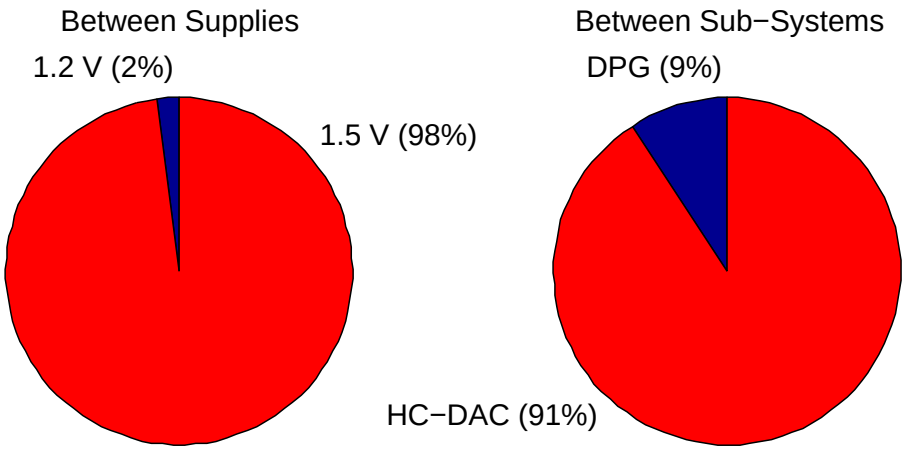


Figure 8.6: Power consumption breakdown at 1 MHz with DEM

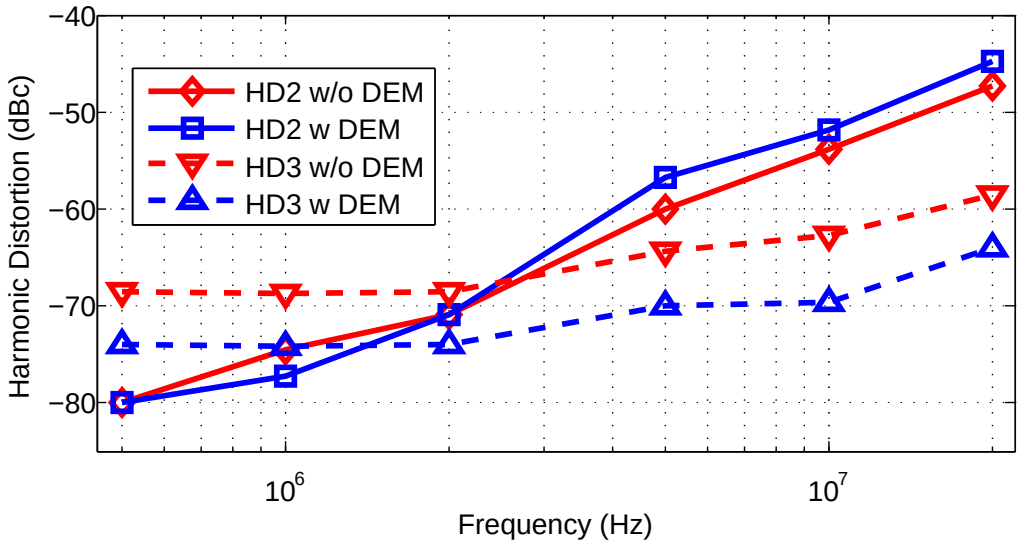


Figure 8.7: $HD_2$ and $HD_3$ measurements

### 8.2.2 Discussion on the Variation of SDR against Frequency

The variation of SDR against the output frequency observed in Fig. 8.4 can be understood by considering the change of even and odd harmonic distortions against output frequency. Figure 8.7 plots $HD_2$ and $HD_3$ measurements representing even and odd harmonics. Across the measured frequency range, applying the partial DEM technique consistently decreased $HD_3$, as theoretically expected. At lower frequencies, $HD_3$ dominates over $HD_2$. Therefore, at lower frequencies, the reduction

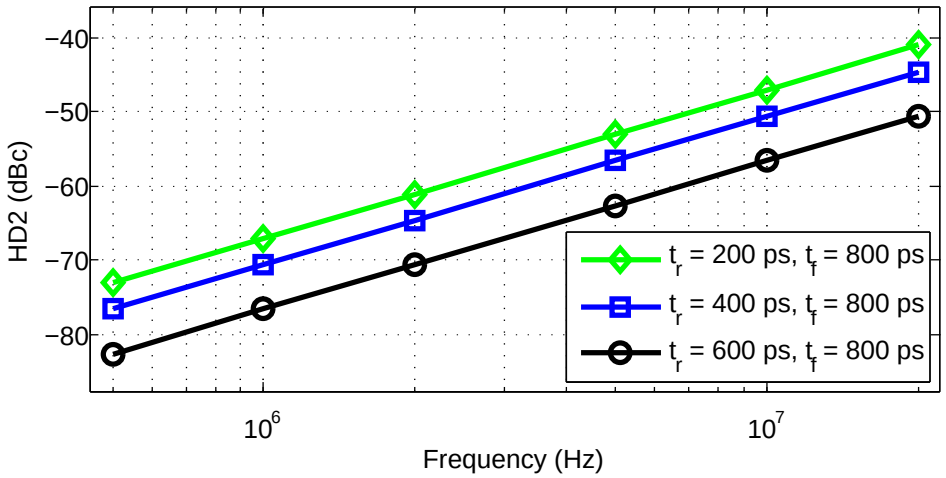


Figure 8.8: Simulated $HD_2$ when rise-time and fall-time are mismatched

in $HD_3$ gained from the partial DEM technique made a positive impact on the SDR, as observed in Fig. 8.4. In contrast, due to the dominance of $HD_2$ and the other even harmonic distortions at higher frequencies, the impact of the partial DEM technique on the SDR was diminished.

Measured results in Fig. 8.7 show $HD_2$ increasing against frequency at a rate of approximately 20 dB/dec. The rise in even harmonic distortion at the HC-DAC output can be understood by revisiting the discussion on timing nonidealities in Section 5.4. A practical square-wave signal suffers from non-zero rise-time ($t_r$), and fall-time ($t_f$). When $t_r$ and $t_f$ are not equal, the square-wave signals loose half-wave symmetry, which causes the square-wave signals to contain even order harmonics. The harmonic cancellation technique does not cancel even order harmonics. Thus, even order harmonics present in the square-wave signals make their way into the HC-DAC output.

A behavioural model for the HC-DAC in DHSS–1 was written in MATLAB based on Eq. 5.12 to describe the time erred square-wave signals. Figure 8.8 plots the simulated variation of $HD_2$ against frequency, according to the behavioural model, for three different sets of mismatched rise-time and fall-time. Note that the simu-

lated $HD_2$ curves have a positive slope of 20 dB/dec against frequency, which we also observed in the measured $HD_2$ results plotted in Fig. 8.7.

Mismatch errors, which are addressed in this research with the proposed DEM technique, and inequality between rise-time and fall-time, which causes even harmonic distortion, are two orthogonal problems affecting HC-DACs. The results in Fig. 8.7 show that future work on an HC-DAC design, which combines the DEM technique proposed in this thesis with a solution to correct the inequality between transition times, could have significantly improved SDR at higher frequencies. Even without addressing the transition time inequality, the work in this thesis can be used in low-bandwidth applications, such as on-chip test signal synthesis for audio ADCs [SP14] and mobile communication ADCs [NUO+14].

### 8.2.3 Figures of Merit and Comparison with Related Work

Two figures of merit will be used in this section to evaluate the performance of DHSS–1. The first figure of merit ($FoM_1$) is defined below.

$$\mathrm{FoM}_1 = \frac{\mathrm{SDR\ (dB)}}{M\ \mathrm{(bit)}} \text{ or } \frac{\mathrm{SFDR\ (dB)}}{M\ \mathrm{(bit)}} \tag{8.1}$$

The purpose of $FoM_1$ is to evaluate the trade-off between spectral purity and hardware cost in the HC-DAC circuit and compare the HC-DAC with other DAC circuits used for sine-wave synthesis in the existing literature. The hardware cost of a DAC is traditionally measured using area and power consumptions. However, the area and power costs of a DAC depend on the DAC architecture (current-steering, resistor string, charge scaling, etc.) [Bak10b]. By using the amplitude resolution to measure the hardware cost of implementing a DAC, $FoM_1$ transcends different DAC architectures. On the downside, $FoM_1$ cannot be applied to the sigma-delta family of DACs, as sigma-delta DACs do not have an explicit definition of amplitude resolution. However, sigma-delta DACs are not commonly used for sine-wave synthesis.

Table 8.1: Comparison of results based on $FoM_1$

| | This Work | [YYJ+14] | [YJJB10] | [ZR08] |
|---|---|---|---|---|
| CMOS Process (nm) | 130 | 55 | 90 | 350 |
| $f_o$ (MHz) | 2 | 200 | 130 | 60 |
| $f_{clk}$ (MHz) | 20 | 2000 | 1300 | 600 |
| SFDR (dB) | 69 | 58 | 54 | 53 |
| Amplitude Resolution - $M$ (bit) | 6.8 | 9 | 11 | 12 |
| $FOM_1$ (dB/bit) | 10.1 | 6.4 | 4.9 | 4.4 |

Table 8.1 summarises the comparison of $FoM_1$. Existing digital harmonic-cancelling sine-wave synthesis related work [ESS10, SBT+10, SSS15] do not use unit-element based architectures to implement the HC-DAC circuit. Hence, they do not specify the amplitude resolution used in the HC-DAC. Thus, the comparison of $FoM_1$ in Table 8.1 focuses only on existing work related to DACs used in DDFSs. Unlike in DHSSs, output frequency of a DDFS is controlled using a digital input word (Frequency Control Word or FCW), while keeping the clock frequency unchanged [ZR08, YJJB10, YYJ+14]. For fair comparison with this work, in which the ratio $f_{clk}/f_o$ is always 10, SFDR measurements from [ZR08, YJJB10, YYJ+14] were taken at output frequencies when $f_{clk}/f_o = 10$.

The $FoM_1$ values in Table 8.1 show that the 10.1 dB/bit performance of the HC-DAC used in DHSS–1 is more than 55 % higher compared to the existing DACs used in DDFSs. The general trade-off between amplitude resolution and output spectral purity of a conventional DAC is defined by the "6 dB/bit rule" [Ben48]. As shown in Table 8.1, $FoM_1$ of [YYJ+14] agrees with the 6 dB/bit rule, while the performances of [YJJB10] and [ZR08] fall below the 6 dB/bit rule. HC-DACs can be designed to perform better than 6 dB/bit by using the Pareto optimal design method and the partial DEM technique proposed in this thesis. The capability of HC-DACs to

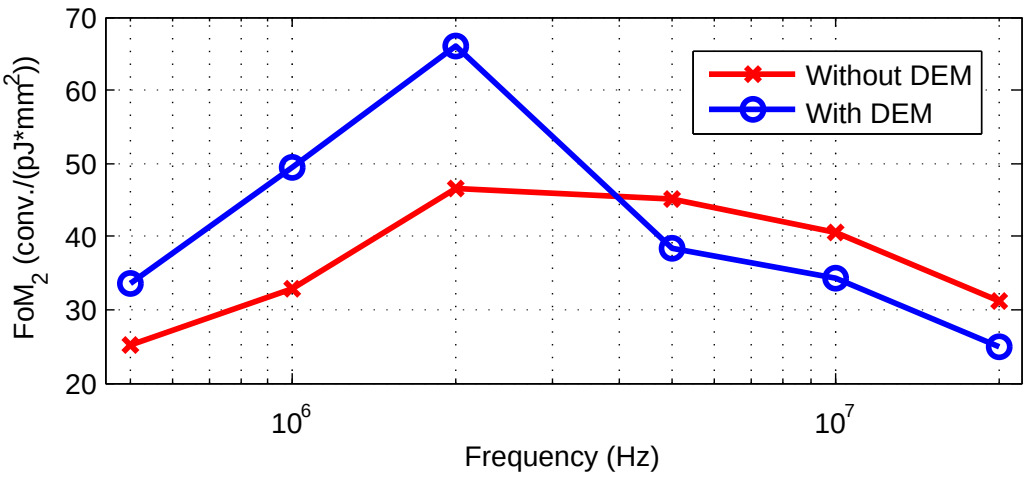


Figure 8.9: $FoM_2$ versus output frequency with and without DEM

perform better than 6 dB/bit is one of the reasons why DHSSs are more area and power cost efficient compared to DDFSs.

The second figure of merit ($FoM_2$) is defined in the following equation, based on the figures of merit used in [YYJ+14, SSS15].

$$\text{FOM}_2 = \frac{f_o \text{ (MHz)} \times 2^{[(\text{SDR (dB)})/6]}}{\text{Power (uW)} \times \text{Area (mm}^2\text{)}} \tag{8.2}$$

The purpose of $FoM_2$ is to evaluate the DHSS–1 circuit as a whole, including both the DPG and the HC-DAC. Based on DHSS–1 measurements reported earlier, the variation of $FoM_2$ against output frequency is plotted in Fig. 8.9. When calculating $FoM_2$ values for cases where DEM is deactivated, DHSS–1 area cost was taken to be 0.062 $mm^2$, without including the area of the scrambler and the register, which are only required if DEM is implemented. It is evident from Fig. 8.9 that at 2 MHz output frequency, activating the partial DEM technique increased $FoM_2$ by 40%.

Table 8.2 summarizes a $FoM_2$ based comparison of DHSS–1 against existing sine-wave synthesis related work. Note that $FoM_2$ values for [ZR08, YJJB10, YYJ+14] were calculated using SFDR instead of SDR, as [ZR08, YJJB10, YYJ+14] only report SFDR. In the table, [ESS10, SBT+10, SSS15] represent work related to digital

Table 8.2: Comparison of results based on $FoM_2$

| | This Work | [ESS10]$^\star$ | [ESS10] | [SBT$^+$10]$^\star$ | [SSS15]$^\star$ | [YYJ$^+$14] | [YJJB10] | [ZR08] |
|---|---|---|---|---|---|---|---|---|
| CMOS Process (nm) | 130 | 130 | 130 | 90 | 180 | 55 | 90 | 350 |
| $f_{clk}$ (MHz) | 20 | 1160 | 1160 | – | – | 2000 | 1300 | 600 |
| $f_o$ (MHz) | 2 | 10 | 10 | 100 | 750 | 200 | 130 | 60 |
| SDR (dB) | 66 | 72 | 59 | – | 63 | – | – | – |
| SFDR (dB) | 69 | – | – | 45 | – | 58 | 54 | 53 |
| Power (mW) | 0.94 | 4.04 | 4.04 | 1.68 | 57 | 130 | 350 | 480 |
| Area ($mm^2$) | 0.066 | 0.186 | 0.066 | 0.0455 | 0.08 | 0.1 | 2 | 5 |
| Sine-Wave Synthesizer Type | DHSS | DHSS | DHSS | DHSS | DHSS | DDFS | DDFS | DDFS |
| DPG Architecture | Clocked | Clocked | Clocked | Ring Osc. | Ring Osc. | – | – | – |
| HC-DAC Architecture$^\dagger$ | CS | RS | RS | CS | RS | – | – | – |
| $FOM_2$ [SDR] (conversion-steps/(pJ·$mm^2$)) | 66 | 55 | 34 | – | 238 | – | – | – |
| $FOM_2$ [SFDR] (conversion-steps/(pJ·$mm^2$)) | 93 | – | – | 237 | – | 12.5 | 0.1 | 0.01 |

$^\star$ Output filter included

$^\dagger$ CS = Current Steering, RS = Resistor String

harmonic-cancelling sine-wave synthesis. The DHSS circuits presented in [ESS10, SBT+10, SSS15] include output filters, while DHSS–1 in this work and the DDFS circuits presented in [ZR08, YJJB10, YYJ+14] do not include output filters. An output filter used in a DHSS is not part of the core harmonic-cancelling operation. The purpose of the output filter is to attenuate the harmonic distortions which remain after the harmonic-cancelling procedure. Thus, for a fair comparison, $FoM_2$ for [ESS10, SBT+10, SSS15] should be calculated without taking into account the effect of the output filter on SDR as well as area. However, only [ESS10] provides enough test result details to calculate $FoM_2$ without the effect of the output filter.

According to $FoM_2$ results in Table 8.2, this work outperforms the sine-wave synthesizers in [ZR08, YJJB10, ESS10, YYJ+14], while faring worse against [SBT+10, SSS15]. The higher output frequency in [SBT+10, SSS15], compared to this work and [ESS10], can be attributed to the use of ring oscillator based DPGs in [SBT+10, SSS15] to generate the square-waves. However, the downside of using ring oscillators is their poor phase noise, which can affect the phase noise of the synthesized sine-waves, as discussed in Section 2.4. The high SDR results obtained in [SSS15] are mainly due to a technique which reduces the phase errors between square-waves, which is orthogonal to the work presented in this thesis. Thus, there is an opportunity to combine the techniques presented in this thesis and [SSS15] for future work, which can lead to improved DHSSs.

Comparing the $FoM_2$ results of DHSSs versus DDFSs in Table 8.2 makes it evident that DHSSs are more area and power cost efficient compared to DDFSs. As discussed in Chapter 2, the advantage DDFSs hold over DHSSs is the ability of DDFSs to digitally program the frequency and the phase of the output sine-wave signals with fine resolution. Nevertheless, for sine-wave synthesizer applications where fine frequency and phase programmability is not a requirement, the results in Table 8.2 suggest that DHSSs are the more attractive solution.

## 8.3 DHSS–2 Measurements and Discussion

### 8.3.1 Measurement Results – PSK IQ DAC Mode

In IQ DAC mode (MDE = 1), both static and dynamic measurements were taken from DHSS–2. Static measurements were taken by slowly looping through the 16 different phase states, such that a slow step-wise sine-wave was played at the output of DHSS–2, and by measuring the output voltage level corresponding to each phase state.

As illustrated in Fig. 3.13, the phase signal input provided to a $k$–bit DHSS in IQ DAC mode is an unsigned $h$–bit binary word, $P$, which can take integer values from 0 to $2k+1$. The relationship between $P$ and $\Phi$, which is the phase of the DHSS output signal in radians, depends on the mapping between $P$ and the square-wave signals, and whether the DHSS output signal is considered a sine signal or a cosine signal. Utilizing the relationship between $P$ and the square-wave amplitudes defined in Fig. 4.5, and defining the output signal of DHSS–2 as a cosine signal, the mapping between $P$ and $\Phi$ is defined as follows:

$$\Phi = \frac{\pi}{2k+2} \times (2P - 2k - 1) \tag{8.3}$$

For the 7–bit DHSS–2 considered here, the above equation simplifies to the following.

$$\Phi = \frac{\pi}{16} \times (2P - 15) \tag{8.4}$$

In the following discussion, the phase input to DHSS-2 in IQ DAC mode will be specified using $\Phi$.

Figure 8.10 illustrates the measured static output of the DHSS–2 circuit operating in IQ DAC mode. The errors of the static output measurements compared to the corresponding ideal cosine amplitudes are plotted in Fig. 8.11 using two metrics:

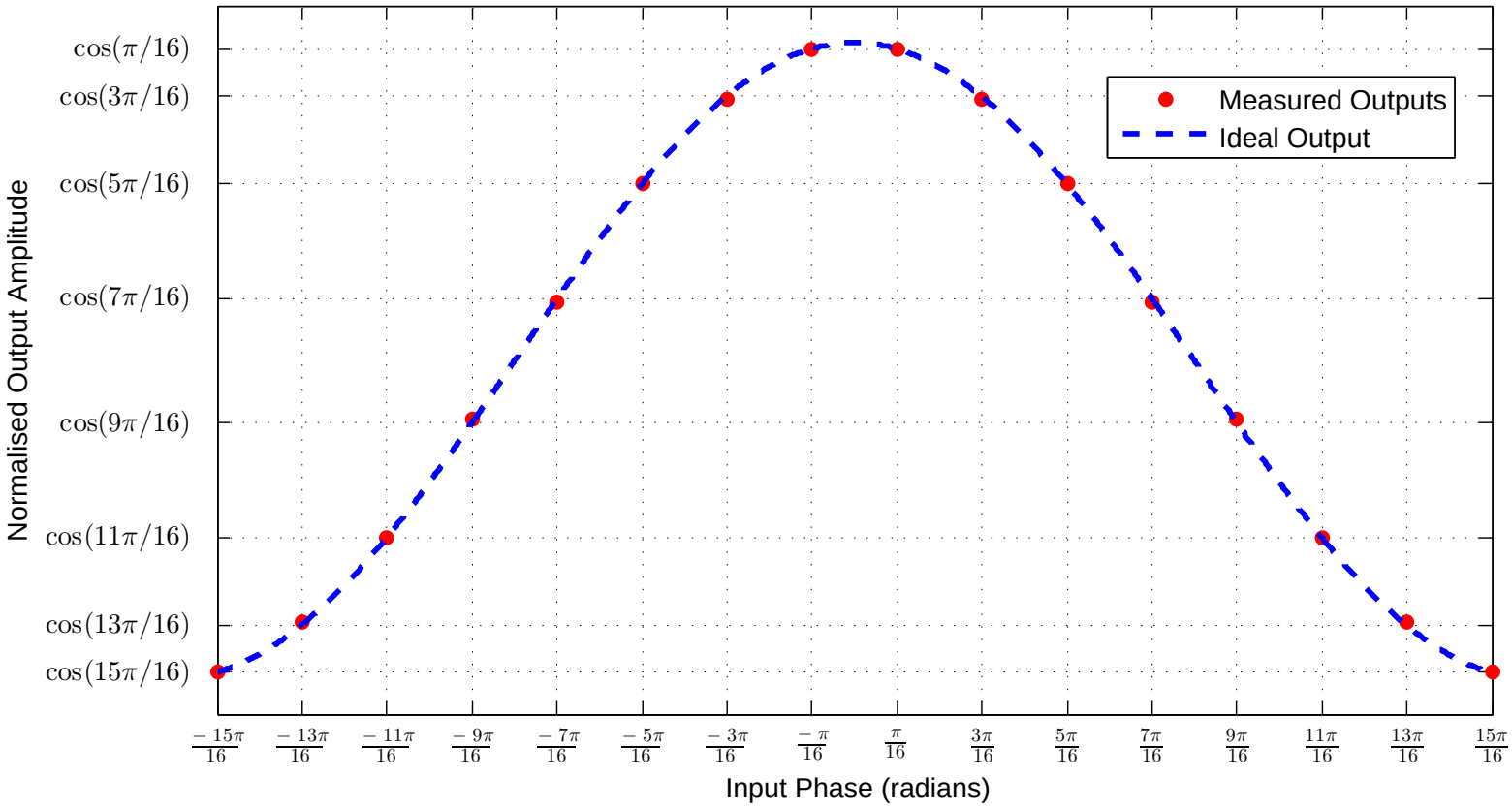


Figure 8.10: Static output measurements and ideal output for DHSS–2 operating as an IQ DAC

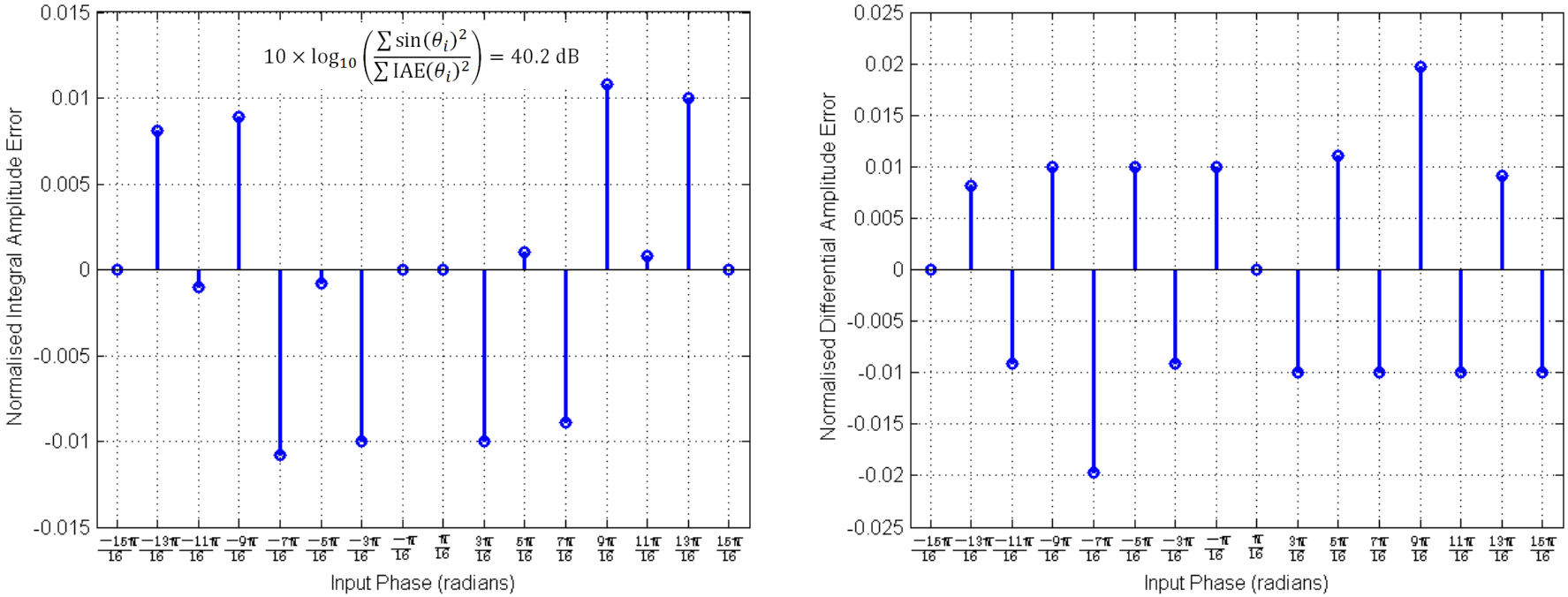


Figure 8.11: Integral amplitude error and differential amplitude error of DHSS–2 functioning as an IQ DAC

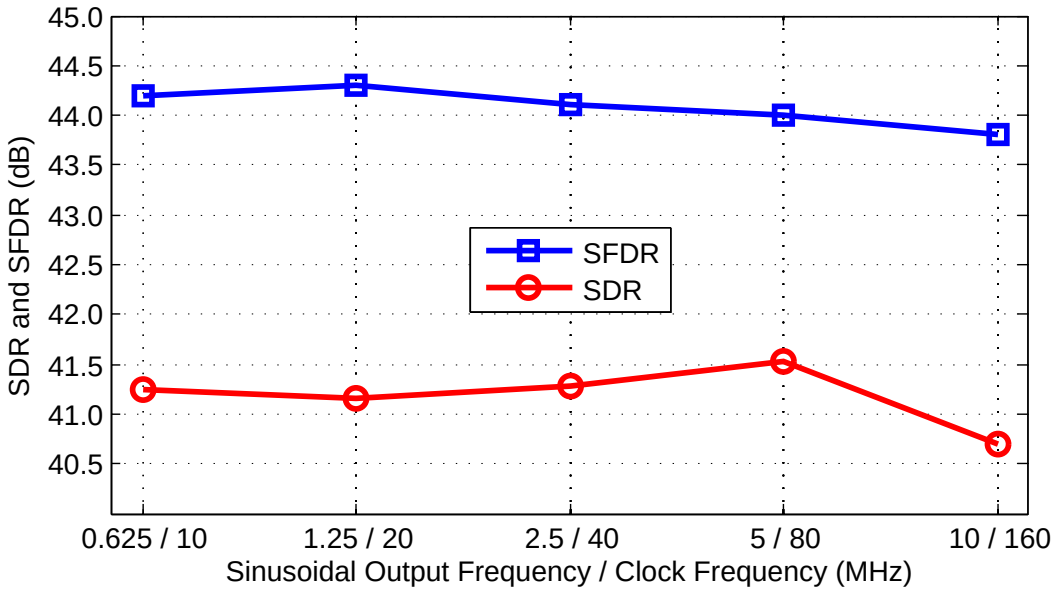


Figure 8.12: SDR and SFDR of the IQ DAC output against varying frequency

integral amplitude error (IAE) and differential amplitude error (DAE). IAE and DAE are calculated similar to the way integral non-linearity and differential non-linearity are calculated for a regular DAC [Kes05]. However, since DHSS–2 is not a linear DAC, but a sine weighted DAC when operating in IQ DAC mode, the term "non-linearity" has been replaced with "amplitude error' in this thesis.

The dynamic performance of the DHSS–2 circuit in IQ DAC mode was gauged by playing sine-wave signals out of DHSS–2 at different frequencies. SDR and SFDR of the output sine-wave signal were used as the metrics for dynamic performance. Note that SDR and SFDR of a DHSS output were defined in Section 5.3. Figure 8.12 plots SDR and SFDR of DHSS–2 against varying output/clock frequency. The clock frequency here is the sampling frequency of the IQ DAC. To form a link between dynamic and static measurements, note that the 40.2 dB signal-to-IAE power ratio noted in Fig. 8.11 matches the SDR measurements in Fig. 8.12 within 1.5 dB.

The power consumption of the IQ DAC while playing a sine-wave signal is plotted in Fig. 8.13 against varying clock frequency. Furthermore, the breakdown of power

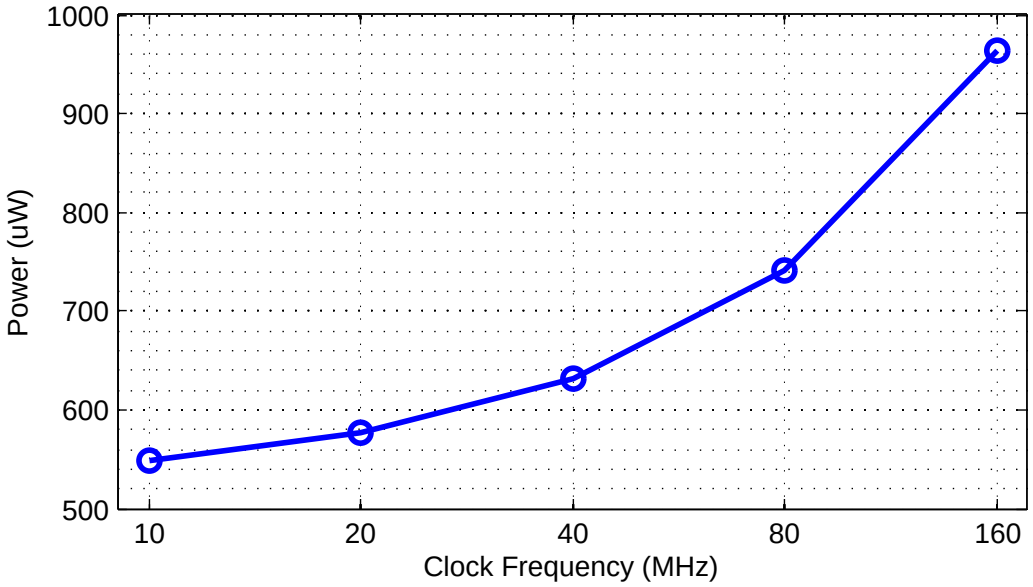


Figure 8.13: Power consumption of the IQ DAC against varying frequency

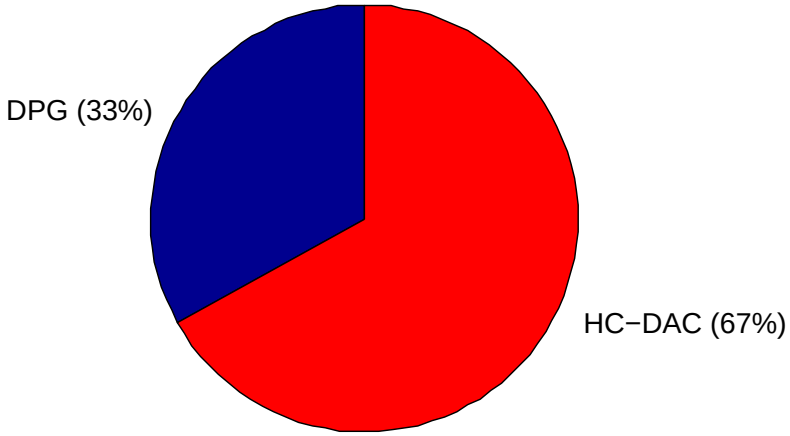


Figure 8.14: Distribution of power consumption in the IQ DAC at $f_{\text{clk}} = 160$ MHz

consumption between the DPG and the HC-DAC of DHSS–2 at 160 MHz clock frequency is illustrated in Fig. 8.14. Note that at 160 MHz clock frequency the IQ DAC consumed a total power of 0.96 mW.

### 8.3.2 Analysis of Results – PSK IQ DAC Mode

The HC-DAC inside DHSS–2 is of 5.2–bit amplitude resolution, and Fig. 8.12 shows the SDR measured around 41 dB. Thus, DHSS–2 in IQ DAC mode yields close to 8 dB/bit, which is well over the 6 dB/bit yield theoretically expected from a conventional DAC.

The lower bound for EVM of a PSK signal, which is modulated by using two DHSS–2 circuits as IQ DACs, can be calculated using the IAE measurements as follows:

$$\mathrm{EVM} = 10 \times \log_{10} \left( \frac{2 \times \sum_{i=-7}^{8} \mathrm{IAE}\left[(2i-1)\frac{\pi}{16}\right]}{16} \right) = -40.2 \text{ dB} \tag{8.5}$$

Note that the EVM and the signal-to-IAE power ratio given in Fig. 8.11 are reciprocals of each other. Let us compare this EVM measurement with the EVM requirements in ZigBee (IEEE 802.15.4) and Bluetooth, which are two established wireless standards that use PSK modulation. The ZigBee standard [ZB111] specifies a −9.1 dB (35%) EVM upper bound on BPSK and QPSK modulated signals. The Bluetooth standard [BT110] specifies a −14.0 dB (20%) EVM upper bound on QPSK modulated signals, and a −17.7 dB (13%) EVM upper bound on 8PSK modulated signals. Thus, the DHSS–2 based IQ DAC has more than 22 dB EVM margin against each specification.

The figure of merit ($\mathrm{FoM_{IQDAC}}$) used in this thesis to evaluate the overall performance of DHSS–2 as an IQ DAC is given below.

$$\mathrm{FoM_{IQDAC}} = \frac{\sqrt{f_\mathrm{o}\ (\mathrm{MHz}) \times f_\mathrm{s}\ (\mathrm{MHz})} \times 2^{[(\mathrm{SFDR\ (dB)})/6]}}{\mathrm{Power\ (uW)} \times \mathrm{Area\ (mm^2)}} \tag{8.6}$$

where $f_\mathrm{o}$ is the frequency of the sine-wave signal played during the measurement, and $f_\mathrm{s}$ is the sampling frequency, or the clock frequency, of the IQ DAC. Both

Table 8.3: Comparison of IQ (baseband) DAC results based on $\text{FoM}_{\text{IQDAC}}$

| | This Work | [TFW11] | [TC14] | [LYSL14] | [SB14] |
|---|---|---|---|---|---|
| CMOS Process (nm) | 130 | 90 | 20 | 180 | 180 |
| DAC Type | Nyquist | Nyquist | Nyquist | OS & MS$^\star$ | Nyquist |
| Amplitude Resolution (bits) | 5.2 | 12 | 10 | 6 | 8 |
| $f_s$ (MHz) | 160 | 1250 | 960 | 6 | 100 |
| $f_o$ (MHz) | 10 | 80 | 0.235 | 3 | 6.25 |
| SDR (dB) | 41 | – | – | – | – |
| SFDR (dB) | 44 | 75 | 80 | 70 | 47 |
| Power (mW) | 0.96 | 128 | 9 | 1.72 | 20.7 |
| Area ($\text{mm}^2$) | 0.046 | 0.825 | 0.01 | 0.07 | –$^\dagger$ |
| $\text{FOM}_{\text{IQDAC}}$ (conversion-steps/(pJ·$\text{mm}^2$)) | 142 | 17 | 1762 | 115 | –$^\dagger$ |

$^\star$ Oversampled and mismatch shaped

$^\dagger$ Area not provided

$f_o$ and $f_s$ have been taken into account, as related literature on IQ (baseband) DACs [TFW11, TC14, LYSL14, SB14] indicated that SFDR measurements were dependent on both played sine-wave signal frequency and sampling frequency. SFDR was used as the metric for DAC output spectral purity, as most of the related literature [TFW11, TC14, LYSL14, SB14] only provided SFDR measurements.

Table 8.3 compares the measurement results from DHSS–2 working in IQ DAC mode against results from state-of-the-art work in the literature related to IQ (baseband) DACs. Note that the ZigBee baseband DAC published in [LYSL14] uses a sigma-delta mismatch noise shaping algorithm. Thus, $f_s$ quoted here for [LYSL14] is the Nyquist sampling frequency instead of the oversampling clock frequency. According to the comparison of $\text{FoM}_{\text{IQDAC}}$ values given in Table 8.3, DHSS–2 working as an IQ DAC outperforms [TFW11, LYSL14, SB14], while fairing worse against [TC14]. Note that the $\text{FoM}_{\text{IQDAC}}$ advantage of a factor of 10 held by [TC14] is aided by the 20 nm CMOS technology used in [TC14], which is five generations ahead of the 130 nm CMOS technology used in this work.

### 8.3.3 Measurement Results – PSK IF Polar Modulator Mode

A major advantage of using a DHSS as a PSK IF polar modulator, as discussed in Section 3.4, is low distortion at harmonics of the IF carrier. Harmonic distortion of the DHSS–2 output has already been characterized in Fig. 8.12 using SDR and SFDR. In the $x$–axis of Fig. 8.12, "Sinusoidal Output Frequency" corresponds to the IF carrier frequency when DHSS–2 is operating in the IF polar modulator mode (MDE = 0). The results indicate that DHSS-2 can maintain an SDR above 40.5 dB up to a carrier frequency of 10 MHz when operating as an IF polar modulator.

To test the PSK polar modulation capability of DHSS–2, and thereby the proper operation of the phase programmable DPG, the test setup illustrated in Fig. 8.15 was

used. To produce an IF carrier signal with frequency $f_{IF}$, the DPG clock frequency was set at $16 \times f_{IF}$. The baseband PSK signal was provided by the LFSR on chip. Thus, the LFSR clock frequency was set to the baseband frequency, $f_{BB}$. The differential current output signal of DHSS-2 was put through the IA to convert the signal to a single-ended voltage. The ADC used to digitize the IA output was NI PXI-5114 [NIA05]. The ADC was operated at a sampling frequency of 250 MHz, a dynamic range of 8–bit, and a full-scale input voltage range of 1 V. A 5 ms long signal trace captured using the ADC was used as the input to a MATLAB model of an IF receiver, which consisted of a quadrature mixer to down-convert the signal from IF to baseband, baseband filters, and decimators.

The power consumption of DHSS–2 while operating as a PSK IF modulator at 10 MHz IF frequency (160 MHz clock frequency) was 0.97 mW. The effect of the baseband frequency on the PSK IF modulator power consumption was negligible.

Figure 8.16 illustrates the constellation diagrams for two sets of demodulated baseband PSK symbols captured using the test-setup in Fig. 8.15. In both test cases, the IF frequency was set at 10 MHz, while baseband frequencies of 100 kHz and 400 kHz were used in the two cases. At 100 kHz baseband frequency, the EVM of the captured symbols was −62 dB over 499 symbols, and at 400 kHz baseband frequency, the EVM of the 1996 symbols captured was −59 dB.

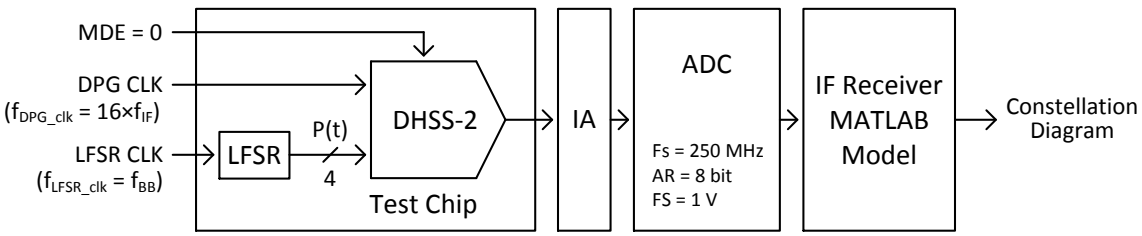


Figure 8.15: Test setup to evaluate the PSK IF polar modulation capability of DHSS–2

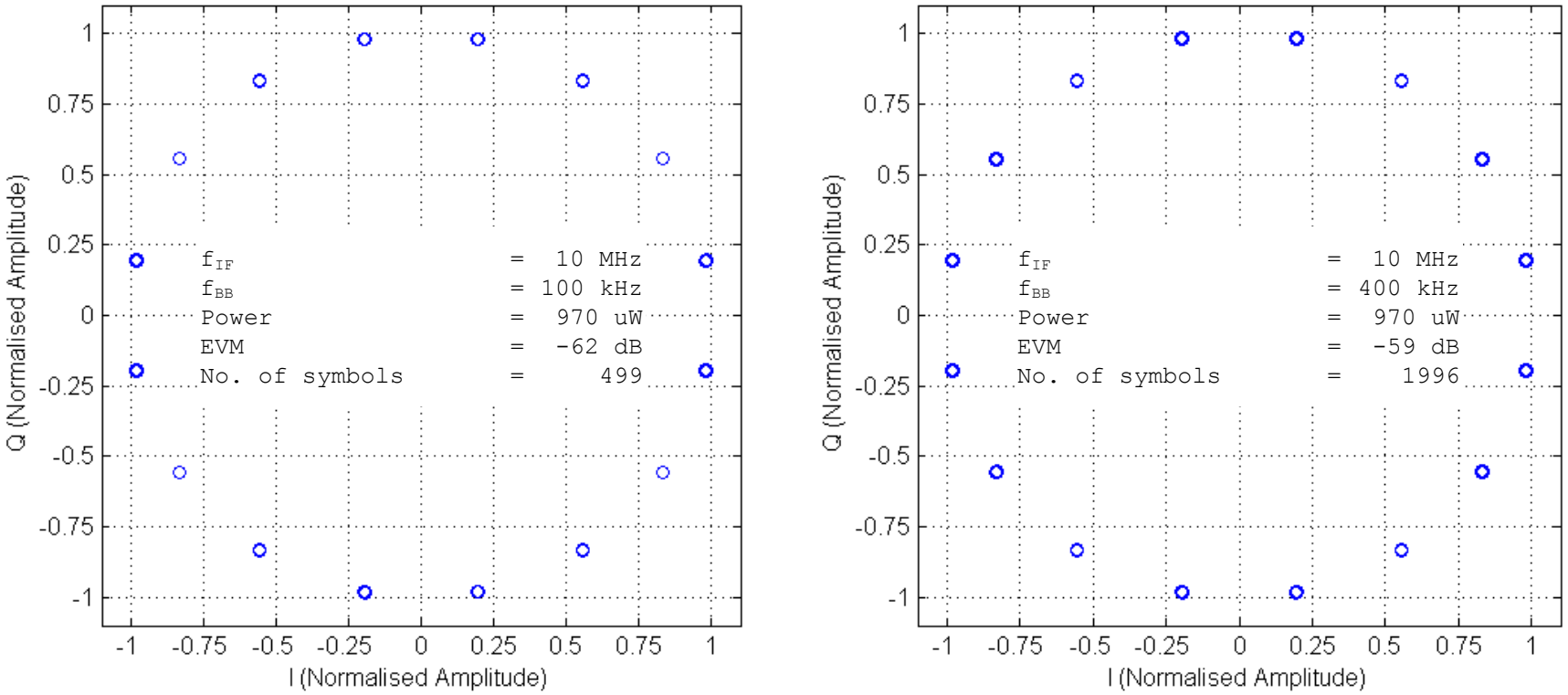


Figure 8.16: Constellation diagrams obtained from the test-setup in Fig. 8.15

### 8.3.4 Analysis of Results – PSK IF Polar Modulator Mode

A question that comes up when comparing the measurement results of DHSS–2 in IQ DAC mode against IF polar modulator mode is why the EVM in IF polar modulator mode is lower than the EVM in IQ DAC mode. When DHSS–2 is used as an IQ DAC to convert a digital baseband PSK signal to an analog baseband PSK signal, the EVM is affected by the amplitude errors in the IQ DAC (DHSS–2) output. In contrast, when DHSS–2 is used to polar modulate an IF carrier with a PSK baseband signal, the EVM is affected by timing errors in the polar modulator (DHSS–2) output. Ideally, given that the phase programmable DPG design used inside DHSS–2 is functionally correct, and that the clock signal provided to DHSS–2 has zero timing jitter, the EVM of the polar modulator output will be $-\infty$. Practically, the finite EVM measurements reported in Fig 8.16 are caused by clock jitter and imperfections in the test-setup. In comparison with the EVM requirements of ZigBee and Bluetooth reported in the previous subsection, measured EVM of the DHSS-2 based PSK IF polar modulator has more than 40 dB margin.

The figure-of-merit used in this thesis to evaluate the performance of DHSS–2 in PSK IF polar modulator mode is as follows:

$$\text{FOM}_{\text{PolMod}} = \frac{f_c\ (\text{MHz}) \times 2^{[(\text{SFDR}\ (\text{dB}))/6]}}{\text{Power}\ (\text{uW}) \times \text{Area}\ (\text{mm}^2)} \tag{8.7}$$

where $f_c$ is the frequency of the sinusoidal carrier signal. Table 8.4 compares the performance of DHSS–2 in PSK IF polar modulator mode against two state-of-the-art DDFSs [YYJ+14, YZS15], and a DDFS inspired BFSK modulator [RS15]. The two DDFSs in [YYJ+14] and [YZS15] have not been demonstrated as PSK polar modulators. However, the fast phase programmability of DDFSs makes [YYJ+14] and [YZS15] candidates for operating as PSK polar modulators, in a similar manner to DHSSs. The results comparison in Table 8.4 shows that DHSS–2 in PSK polar modulator mode outperforms all of [YYJ+14], [YZS15], and [RS15].

Table 8.4: Comparison of PSK IF polar modulator results based on $\text{FoM}_{\text{PolMod}}$

| | This Work | [YYJ+14] | [YZS15] | [RS15] |
|---|---|---|---|---|
| CMOS/BiCMOS Process (nm) | 130$^{\star}$ | 55$^{\star}$ | 130$^{\star}$ | 180$^{\dagger}$ |
| $f_c$ (MHz) | 10 | 125 | 62 | 23.2 |
| SFDR (dB) | 44 | 58 | 51 | 33 |
| Power (mW) | 0.97 | 130 | 300 | 14 |
| Area ($\text{mm}^2$) | 0.046 | 0.1 | 0.87 | 0.08 |
| $\text{FOM}_{\text{PolMod}}$ (conversion-steps/(pJ·$\text{mm}^2$)) | 36 | 8 | 0.09 | 0.9 |

$^{\star}$ CMOS process
$^{\dagger}$ BiCMOS process

## 8.4 Summary

In this chapter, we presented and reviewed the measurement results from DHSS–1 and DHSS–2. Measurement results show that at 2 MHz output frequency DHSS–1 has an SDR to amplitude resolution ratio of 10 dB/bit. Furthermore, the results prove that at 2 MHz the FoM of DHSS–1, which accounts for SDR, output frequency, power, and area, increased by 40 % when the DEM technique was activated. DHSS–2 was measured to access its capability of being used as both a baseband IQ DAC and an IF polar modulator for PSK communication applications. Measurement results show that in IQ DAC mode, DHSS–2 demonstrated more than 22 dB EVM margin against the EVM requirements for PSK modulated signals in Bluetooth and ZigBee standards. In IF polar modulator mode, the EVM margin exhibited by DHSS–2 was more than 40 dB against Bluetooth and ZigBee standards. Furthermore, the test results show that the FoM of DHSS–1 was at least four times higher compared to state-of-the-art DDFSs.

# Chapter 9

# Conclusion

In this research, we have sought to improve the programmability, the area cost efficiency, and the power cost efficiency of DHSSs. The goal in doing so was to make DHSSs the most attractive digital sine-wave synthesizer solution when it comes to applications where area and power cost efficiency is the key requirement. While paving the way towards its goal, this research has made three main contributions to the advancement of DHSS technology, which were studied in detail in this thesis.

The first contribution of this research towards DHSS technology was the proposal, design, and verification of phase programmable DHSSs. A DHSS hardware architecture that supports programming of the phase of the sinusoidal output signal was proposed in Chapter 3. Then, in Chapter 7, we studied the design of an IC prototype of a phase programmable DHSS (DHSS–2). Measurement results taken from the phase programmable DHSS were presented and discussed in Chapter 8. The phase programmable DHSS prototype was measured to verify its usability as a PSK baseband DAC as well as a PSK IF polar modulator. Measurement results confirmed that in the PSK baseband DAC use case, the DHSS exhibited more than 22 dB EVM margin, in comparison to the EVM specifications for PSK modulated

signals in Bluetooth and ZigBee standards. In the PSK IF polar modulator use case, the phase programmable DHSS prototype demonstrated over 40 dB EVM margin compared to Bluetooth and ZigBee specifications. Analyzing the measurement data also showed that the FoM of the phase programmable DHSS prototype was more than four times better compared to state-of-the-art DDFSs.

The work published in this thesis has opened the doors for DHSSs to be used as PSK modulators in area and power costs aware communication applications. However, there is still a long way to go before we see a DHSS being used for PSK modulation in a communication system-on-chip. The next significant step forward would be to develop a complete PSK modulating transmitter using DHSSs for PSK modulation. The targeted applications could be Bluetooth, ZigBee, or any other wired or wireless communication standard that supports PSK modulation. In addition to the DHSSs, the transmitter circuit would contain an upconversion mixer and RF gain stages. By using measurement results from a complete transmitter prototype, the performance advantage gained by using DHSSs for PSK modulation could be quantified. Such analysis could then help to make a strong case for the use of DHSSs in future PSK modulating communication applications.

The second contribution of this work was the proposal and verification of a Pareto optimal design method for the HC-DAC circuits used inside DHSSs. In Chapter 5, we studied the relationship between the amplitude resolution of an HC-DAC and the SDR of the HC-DAC output signal. In a conventional DAC, this relationship is governed by the 6 dB/bit rule. The study presented in Chapter 5 showed the existence of Pareto optimal amplitude resolutions, for which the HC-DAC performance breaks the 6 dB/bit rule. By utilizing these Pareto optimal design points, we proposed a Pareto optimal design method for HC-DACs. As described in Chapter 7, the proposed Pareto optimal design method was used when developing the two DHSS prototypes. Measurement results presented in Chapter 8 showed the HC-DAC in

DHSS–1 yielded 10 dB/bit, while the HC-DAC in DHSS–2 returned 8 dB/bit.

The third contribution of this thesis was the proposal and validation of a partial DEM technique, which was custom made for HC-DACs used in DHSSs. In Chapter 6, we discussed why the area and power cost of implementing a complete DEM technique in an HC-DAC is unrealistic. Then, we proposed a partial DEM technique, which reduced the effect of mismatch errors in HC-DACs, while preserving the area and power cost efficiency of DHSSs. Furthermore, a study presented in Chapter 6 theoretically validated the effectiveness of the proposed partial DEM technique. Later, in Chapter 7, the partial DEM method was implemented in the first DHSS prototype IC (DHSS–1). Measurement results for DHSS–1 given in Chapter 8 showed that activating the partial DEM technique improved the FoM of DHSS–1 by 40%, thus, empirically verifying the cost effectiveness of the partial DEM method.

The second and third contributions of this research have improved the area and power cost efficiency of DHSSs. Furthermore, the performance comparison between DHSSs and DDFSs discussed in Chapter 8 showed that DHSSs are a long way ahead of DDFSs in terms of area and power cost efficiency. Thus, there is already enough evidence to suggest that DHSSs are the most attractive digital sine-wave synthesizer solution when it comes to applications that are area and power cost sensitive. Nevertheless, many avenues of research remain unexplored in the field of digital harmonic-cancelling sine-wave synthesis. One such avenue that was suggested in Chapter 8 was to develop a DHSS that combines the Pareto optimal design method and the partial DEM technique proposed in this work along with the timing error correction technique published in [SSS15]. Another interesting idea to investigate would be developing a sine-wave synthesizer that can play multiple sine-wave signals added together. Such a sine-wave signal synthesizer could be useful to generate multiple tone test signals for certain test cases (e.g., measuring intermodulation

products of a non-linear circuit). The task of generating multiple sine-wave signals involves solving some interesting problems. First, the square-waves based signal synthesis technique used in this work may not be the best method, or it may not even apply to synthesize multiple tone signals. Thus, one problem would be to find the best technique for synthesizing multiple tone signals. Second, in combination with the search for the most suitable signal synthesis technique, the HC-DAC amplitude resolution must be optimized for multiple tone signal synthesis. Third, due to changes made to the signal synthesis technique, the DEM technique may also need an update. Another avenue of research for DHSSs would be to utilize cutting edge process technologies to push the output sine-wave frequencies to the GHz range, while keeping the area and power consumptions down. Process variation and switch leakage at small process nodes will create new challenges in designing DHSSs. For example, making the digital circuits in a DHSS work at GHz frequencies in the slow process corner while expending the minimum required amount of area and power resources would be one challenge. Also, leakage in the HC-DAC current-steering switches could cause linearity degradation, which would require a creative solution.

This research has continued the renaissance of DHSSs and improved the programmability, area cost effectiveness, and power cost effectiveness of DHSSs. It is a fact of academic life that only a fraction of research projects make a lasting impact on the course of their respective subjects. The author remains optimistic.

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# Appendix A

# Mathematics of Harmonic-Cancelling Sine-Wave Synthesis

## A.1 Deriving the Expression for $S_{\mathrm{d}}(f)$

Let us begin the derivation by restating Eq. 3.4, which defines $S_{\mathrm{d}}(f)$ as follows:

$$S_{\mathrm{d}}(f) \;=\; \mathcal{F}\left\{s_{\mathrm{d}}(t)\right\} \tag{A.1}$$

where $s_{\mathrm{d}}(t)$ is the sampled discrete-time sine-wave signal defined in Eq. 3.3. Substituting for $s_{\mathrm{d}}(t)$ from Eq. 3.3 and using the convolution theorem [CF48, Kam04] gives

$$S_{\mathrm{d}}(f) \;=\; \mathcal{F}\left\{A\,\cos\left(2\pi f_{\mathrm{o}} t\right)\right\} * \mathcal{F}\left\{\sum_{n=-\infty}^{\infty} \delta\left[t-\left(nT_{\mathrm{s}}-T_{\mathrm{s}}/2\right)\right]\right\} \tag{A.2}$$

in which the individual Fourier transforms can be calculated using the Fourier transform identities provided in [CF48, Kam04] to obtain

$$S_{\mathrm{d}}(f) \;=\; \left\{\frac{A}{2}\left[\delta\left(f-f_{\mathrm{o}}\right)+\delta\left(f+f_{\mathrm{o}}\right)\right]\right\} * \left\{\frac{e^{-j\pi f/f_{\mathrm{s}}}}{T_{\mathrm{s}}}\sum_{m=-\infty}^{\infty}\delta\left[f-mf_{\mathrm{s}}\right]\right\} \tag{A.3}$$

where $j$ is the imaginary unit and $m \in \mathbb{Z}$. Solving the convolution operation in Eq. A.3 produces the following outcome:

$$S_{\mathrm{d}}(f) \;=\; \frac{A\,e^{-j\pi f/f_{\mathrm{s}}}}{2\,T_{\mathrm{s}}}\sum_{m=-\infty}^{\infty}\delta\left[f-\left(mf_{\mathrm{s}}-f_{\mathrm{o}}\right)\right]+\delta\left[f-\left(mf_{\mathrm{s}}+f_{\mathrm{o}}\right)\right] \tag{A.4}$$

Finally, substituting for $f_s$ from Eq. 3.2 provides

$$S_d(f) = \frac{A\, e^{-j\pi f/f_s}}{2\, T_s} \sum_{m=-\infty}^{\infty} \delta\left(f - [m\,(2k+2) - 1]\, f_o\right) + \delta\left(f - [m\,(2k+2) + 1]\, f_o\right) \tag{A.5}$$

## A.2 Convolution of $\phi_1(t)$ with $h_c(t)$

The definition of the square-wave signal $\phi_1(t)$, originally defined in Eq. 3.16, is given as follows:

$$\phi_1(t) = \begin{cases} +1 & 0 \le t < T_o/2 \\ -1 & T_o/2 \le t < T_o \\ \phi_1(t - T_o) & t \ge T_o \\ \phi_1(t + T_o) & t < 0 \end{cases} \tag{A.6}$$

It has been asserted in Section 3.2 that in order to produce a pure sine-wave signal out of $\phi_1(t)$, an FIR filter with the following impulse response is required

$$h_c(t) = B \sin(2\pi f_o t) \times \text{rect}\left(\frac{t - T_o/4}{T_o/2}\right) \tag{A.7}$$

where rect $(x)$ is the rectangular function and $B$ is an arbitrary constant. The following discussion proves that the assertion is correct by showing that the convolution of $\phi_1(t)$ with $h_c(t)$ results in an ideal sine-wave signal.

Let us define the convolution of $\phi_1(t)$ with $h_c(t)$ as follows:

$$(\phi_1 * h_c)(t) = \int_{-\infty}^{\infty} h_c(\tau) \times \phi_1(t - \tau)\, d\tau \tag{A.8}$$

As $\phi_1(t)$ is a periodic signal with a time period of $T_o$, so will $(\phi_1 * h_c)(t)$ be. Thus, let us first define $(\phi_1 * h_c)(t)$ for a whole period from $t = 0$ to $t = T_o$.

First, consider $(\phi_1 * h_c)(t)$ during the time interval, $0 \le t < T_o/2$. According to Eq. A.7 $h_c(\tau)$ is non-zero only when $0 \le \tau < T_o/2$. Thus, we can narrow the limits of the convolution integral in Eq. A.8 down to the same interval as follows

$$(\phi_1 * h_c)(t) = \int_0^{T_o/2} B \sin(2\pi f_o \tau) \times \phi_1(t - \tau)\, d\tau \tag{A.9}$$

By expanding $\phi_1(t - \tau)$ using Eq. A.6 we get

$$(\phi_1 * h_c)(t) = \int_0^t B \sin(2\pi f_o \tau)\; d\tau + \int_t^{T_o/2} -B \sin(2\pi f_o \tau)\; d\tau \tag{A.10}$$

*Appendix A*

*Mathematics of Harmonic-Cancelling Sine-Wave Synthesis*

Using trigonometric identities and integration techniques, the integral in Eq. A.10 is solved as follows:

$$\begin{aligned}
(\phi_1 * h_c)(t) &= \int_{T_o/2}^{T_o/2+t} -B \sin(2\pi f_o \tau)\ \mathrm{d}\tau + \int_{t}^{T_o/2} -B \sin(2\pi f_o \tau)\ \mathrm{d}\tau \\
&= \int_{t}^{T_o/2+t} -B \sin(2\pi f_o \tau)\ \mathrm{d}\tau \\
&= \left[\frac{B}{2\pi f_o} \cos(2\pi f_o \tau)\right]_{t}^{T_o/2+t} \\
&= \frac{B}{2\pi f_o}\left[\cos(\pi + 2\pi f_o t) - \cos(2\pi f_o t)\right] \\
&= \frac{-B}{\pi f_o} \cos(2\pi f_o t)
\end{aligned} \tag{A.11}$$

Next, let us consider $(\phi_1 * h_c)(t)$ during the time interval, $T_o/2 \leq t < T_o$, as follows:

$$(\phi_1 * h_c)(t) = \int_{0}^{T_o/2} B \sin(2\pi f_o \tau) \times \phi_1(t-\tau)\ \mathrm{d}\tau \tag{A.12}$$

In the specified interval of $t$, by expanding $\phi_1(t-\tau)$ we get

$$(\phi_1 * h_c)(t) = \int_{0}^{t-T_o/2} -B \sin(2\pi f_o \tau)\ \mathrm{d}\tau + \int_{t-T_o/2}^{T_o/2} B \sin(2\pi f_o \tau)\ \mathrm{d}\tau \tag{A.13}$$

The integral in Eq. A.13 is solved as follows:

$$\begin{aligned}
(\phi_1 * h_c)(t) &= \int_{T_o/2}^{t} B \sin(2\pi f_o \tau)\ \mathrm{d}\tau + \int_{t-T_o/2}^{T_o/2} B \sin(2\pi f_o \tau)\ \mathrm{d}\tau \\
&= \int_{t-T_o/2}^{t} B \sin(2\pi f_o \tau)\ \mathrm{d}\tau \\
&= \left[\frac{-B}{2\pi f_o} \cos(2\pi f_o \tau)\right]_{t-T_o/2}^{t} \\
&= \frac{-B}{2\pi f_o}\left[\cos(2\pi f_o t) - \cos(2\pi f_o t - \pi)\right] \\
&= \frac{-B}{\pi f_o} \cos(2\pi f_o t)
\end{aligned} \tag{A.14}$$

By combining Eq. A.11, which holds for $0 \leq t < T_o/2$, and Eq. A.14, which holds for $T_o/2 \leq t < T_o$, we define $(\phi_1 * h_c)(t)$ for the time interval, $0 \leq t < T_o$, as follows:

$$(\phi_1 * h_c)(t) = \frac{-B}{\pi f_o} \cos(2\pi f_o t) \tag{A.15}$$

As $(\phi_1 * h_c)(t)$ and $\cos(2\pi f_o t)$ both have the same period of $T_o$, it can be deduced that Eq. A.15 holds for all values of $t$. Thus, it is proven that the convolution of $\phi_1(t)$ with $h_c(t)$ results in an ideal sinusoidal signal.

## A.3 Deriving the Expression for $H_c(f)$

The ideal transfer function of the FIR filter discussed in Section 3.2 is defined as follows:

$$H_c(f) = \mathcal{F}\{h_c(t)\} \tag{A.16}$$

where $h_c(t)$ is defined in Eq. A.7. Substituting from Eq. A.7 and using the convolution theorem [CF48, Kam04] we get

$$H_c(f) = \mathcal{F}\{B \sin(2\pi f_o t)\} * \mathcal{F}\left\{\text{rect}\left(\frac{t - T_o/4}{T_o/2}\right)\right\} \tag{A.17}$$

Using the Fourier transform tables in [CF48, Kam04] to evaluate Eq. A.16 we obtain

$$H_c(f) = \left\{\frac{B}{2}\left[\delta(f - f_o) + \delta(f + f_o)\right]\right\} * \left\{\frac{e^{-j\pi f/2f_o}\, T_o}{2} \text{sinc}\left(\frac{f}{2f_o}\right)\right\} \tag{A.18}$$

## A.4 Deriving the Expression for $\Phi_1(f)$

The Fourier transform of the square-wave signal, $\phi_1(t)$, is defined as follows:

$$\Phi_1(f) = \mathcal{F}\{\phi_1(t)\} = \int_{-\infty}^{\infty} \phi_1(t) \times e^{-j2\pi f t}\, dt \tag{A.19}$$

In order to evaluate Eq. A.19, we should first calculate the complex Fourier series of $\phi_1(t)$, which is defined below

$$\phi_1(t) = \sum_{m=-\infty}^{\infty} c_m\, e^{j2\pi m f_o t} \tag{A.20}$$

where $m \in \mathbb{Z}$ and $c_m$, which denotes the complex Fourier series coefficients, is defined according to the following equation

$$c_m = \frac{1}{T_\mathrm{o}} \int_{-T_\mathrm{o}/2}^{T_\mathrm{o}/2} \phi_1(t) \times e^{-j2\pi m f_\mathrm{o} t} \, \mathrm{d}t \tag{A.21}$$

Let us find an expression for $c_m$ by solving the integral in Eq. A.21. Substituting for $\phi_1(t)$ from Eq. A.6 the integral can be solved for $m \neq 0$ as follows:

$$\begin{aligned} c_m &= \frac{1}{T_\mathrm{o}} \int_{-T_\mathrm{o}/2}^{0} (-1) \times e^{-j2\pi m f_\mathrm{o} t} \, \mathrm{d}t - \frac{1}{T_\mathrm{o}} \int_{0}^{T_\mathrm{o}/2} (1) \times e^{-j2\pi m f_\mathrm{o} t} \, \mathrm{d}t \\ &= \frac{1}{T_\mathrm{o}} \left( \left[ \frac{T_\mathrm{o}}{2\pi m j} \, e^{-j2\pi m f_\mathrm{o} t} \right]_{-T_\mathrm{o}/2}^{0} + \left[ \frac{-T_\mathrm{o}}{2\pi m j} \, e^{-j2\pi m f_\mathrm{o} t} \right]_{0}^{T_\mathrm{o}/2} \right) \\ &= \frac{1}{m\pi j} \left[ 1 - \cos\left( m\pi \right) \right] \end{aligned} \tag{A.22}$$

Solving the integral for $m = 0$ gives $c_m = 0$.

Coming back to the Fourier transform definition in Eq. A.19, let us substitute for $\phi_1(t)$ from Eq. A.20 to get

$$\Phi_1(f) = \int_{-\infty}^{\infty} \left( \sum_{m=-\infty}^{\infty} c_m \, e^{j2\pi m f_\mathrm{o} t} \right) \times e^{-j2\pi f t} \, \mathrm{d}t \tag{A.23}$$

The integral in Eq. A.23 can be solved using the following steps

$$\begin{aligned} \Phi_1(f) &= \int_{-\infty}^{\infty} \sum_{m=-\infty}^{\infty} c_m \, e^{-j2\pi (f - m f_\mathrm{o}) t} \, \mathrm{d}t \\ &= \sum_{m=-\infty}^{\infty} c_m \int_{-\infty}^{\infty} e^{-j2\pi (f - m f_\mathrm{o}) t} \, \mathrm{d}t \\ &= \sum_{m=-\infty}^{\infty} c_m \, \delta\left( f - m f_\mathrm{o} \right) \end{aligned} \tag{A.24}$$

Finally, substituting for $c_m$ from Eq. A.21 we arrive at the following expression

$$\Phi_1(f) = \sum_{m=-\infty}^{\infty} \frac{\left[ 1 - \cos\left( m\pi \right) \right]}{m\pi j} \times \delta\left( f - m f_\mathrm{o} \right) \tag{A.25}$$

where $m \in \{ x \mid x \in \mathbb{Z}, \; x \neq 0 \}$.

## A.5 Simplifying the $H_{\mathrm{d}}(z)$ Expression Derived Using the Frequency Domain Approach

The transfer function $H_{\mathrm{d}}(z)$ given in Eq. 3.34 cannot be used to implement the FIR filter. Thus, we need to simplify the definition of $H_{\mathrm{d}}(z)$ to a standalone polynomial.

First, let us rewrite Eq. 3.34 as follows:

$$H_{\mathrm{d}}(z) \;=\; \frac{1+z^{-(k+1)}}{1-2\cos\left(\dfrac{\pi}{k+1}\right)z^{-1}+z^{-2}} \tag{A.26}$$

By considering the order of the polynomials in the numerator and the denominator of Eq. A.26, we can deduce that $H_{\mathrm{d}}(z)$ is a $(k-1)^{\text{th}}$ order polynomial of $z^{-1}$. Thus, let us make an alternative definition of $H_{\mathrm{d}}(z)$ as

$$H_{\mathrm{d}}(z) \;=\; \sum_{i=1}^{k} a_i\, z^{-(i-1)} \tag{A.27}$$

where $i \in \{x \mid x \leq k,\ x \in \mathbb{Z}^{+}\}$. The stand-alone polynomial form of $H_{\mathrm{d}}(z)$ defined in Eq. A.27 can be used to implement the FIR filter if the polynomial coefficients are known. To find the polynomial coefficients let us equate Eq. A.27 to Eq. A.26, and rewrite the resulting equation as follows:

$$\left[a_1 + a_2 z^{-1} + \cdots + a_k z^{-(k-1)}\right]\left[1-2\cos\left(\frac{\pi}{k+1}\right)z^{-1}+z^{-2}\right] = 1+z^{-(k+1)} \tag{A.28}$$

By comparing the coefficient of each term in the two $(k+1)^{\text{th}}$ order polynomials on the left side and the right side of Eq. A.28, we derive the following equation

$$a_i \;=\; \begin{cases} -1+\sum\limits_{u=0}^{i-1}\left[1+\cos\left(u\pi\right)\right]\cos\left(\frac{u\pi}{k+1}\right) & \text{if } i \text{ is odd} \\ \sum\limits_{u=1}^{i-1}\left[1-\cos\left(u\pi\right)\right]\cos\left(\frac{u\pi}{k+1}\right) & \text{if } i \text{ is even} \end{cases} \tag{A.29}$$

where $u \in \mathbb{Z}$. Let us define $b_i$ as

$$b_i = \sin\left(\frac{\pi}{k+1}\right) a_i \tag{A.30}$$

Note that multiplying $H_{\mathrm{d}}(z)$ by $\sin\left(\frac{\pi}{k+1}\right)$ does not affect the placement of the zeros. Substituting for $a_i$ from Eq. A.29 we get

$$b_i = \begin{cases} -\sin\left(\frac{\pi}{k+1}\right)+\sum\limits_{u=0}^{i-1}\left[1+\cos\left(u\pi\right)\right]\cos\left(\frac{u\pi}{k+1}\right)\sin\left(\frac{\pi}{k+1}\right) & \text{if } i \text{ is odd} \\ \sum\limits_{u=1}^{i-1}\left[1-\cos\left(u\pi\right)\right]\cos\left(\frac{u\pi}{k+1}\right)\sin\left(\frac{\pi}{k+1}\right) & \text{if } i \text{ is even} \end{cases} \tag{A.31}$$

Using trigonometric identities we can simplify Eq. A.31 to obtain

$$b_i = \begin{cases} -\sin\left(\frac{\pi}{k+1}\right) + \sum_{u=0}^{i-1} \frac{[1+\cos(u\pi)]}{2} \left(\sin\left[\frac{(u+1)\pi}{k+1}\right] - \sin\left[\frac{(u-1)\pi}{k+1}\right]\right) & \text{if } i \text{ is odd} \\ \sum_{u=1}^{i-1} \frac{[1-\cos(u\pi)]}{2} \left(\sin\left[\frac{(u+1)\pi}{k+1}\right] - \sin\left[\frac{(u-1)\pi}{k+1}\right]\right) & \text{if } i \text{ is even} \end{cases} \tag{A.32}$$

Simplifying the equation further by expanding the summations gives us

$$b_i = \sin\left(\frac{i\pi}{k+1}\right) \tag{A.33}$$

Let us define $w_i$ by

$$w_i = B \times b_i = B \times \sin\left(\frac{i\pi}{k+1}\right) \tag{A.34}$$

where $B$ is an arbitrary constant. Noting that multiplying $H_{\mathrm{d}}(z)$ by an arbitrary constant does not change the zeros of $H_{\mathrm{d}}(z)$ we redefine the transfer function of the FIR filter as

$$H_{\mathrm{d}}(z) \;=\; \sum_{i=1}^{k} w_i \, z^{-(i-1)} \tag{A.35}$$

# Appendix B

# Designing HC-DACs

## B.1 Deriving the Expression for $S_{\mathrm{ni}}(nf_{\mathrm{o}})$

The Fourier transform of $s_{\mathrm{ni}}(t)$ is defined as follows:

$$S_{\mathrm{ni}}(f) \;=\; \mathcal{F}\{s_{\mathrm{ni}}(t)\} \;=\; \mathcal{F}\left\{\sum_{i=1}^{k} R_{\mathrm{L}} \times I_{\mathrm{ni}}(i) \times \phi_i(t)\right\} \tag{B.1}$$

By substituting for $\phi_i(t)$ from Eq. 5.1 and simplifying the expression we get

$$\begin{aligned} S_{\mathrm{ni}}(f) \;&=\; \mathcal{F}\left\{\sum_{i=1}^{k} R_{\mathrm{L}} \times I_{\mathrm{ni}}(i) \times \phi_1\left(t - \frac{(i-1)T_{\mathrm{o}}}{2k+2}\right)\right\} \\ &=\; R_{\mathrm{L}} \times \sum_{i=1}^{k} I_{\mathrm{ni}}(i) \times \Phi_1(f) \times \exp\left[\frac{j\pi f}{(k+1)f_{\mathrm{o}}} \times (1-i)\right] \end{aligned} \tag{B.2}$$

where $\Phi_1(f)$ has been defined in Eq. A.25. Since we are only interested in the complex Fourier coefficients of $s_{\mathrm{ni}}(t)$, by defining $S_{\mathrm{ni}}(nf_{\mathrm{o}})$ and substituting for $\Phi_1(f)$ we arrive at

$$S_{\mathrm{ni}}(nf_{\mathrm{o}}) \;=\; \frac{R_{\mathrm{L}} \times [1 - \cos(n\pi)]}{n\pi j} \times \sum_{i=1}^{k} I_{\mathrm{ni}}(i) \times \exp\left[\frac{n\pi j}{k+1} \times (1-i)\right] \tag{B.3}$$

## B.2 HC-DAC Design Spaces

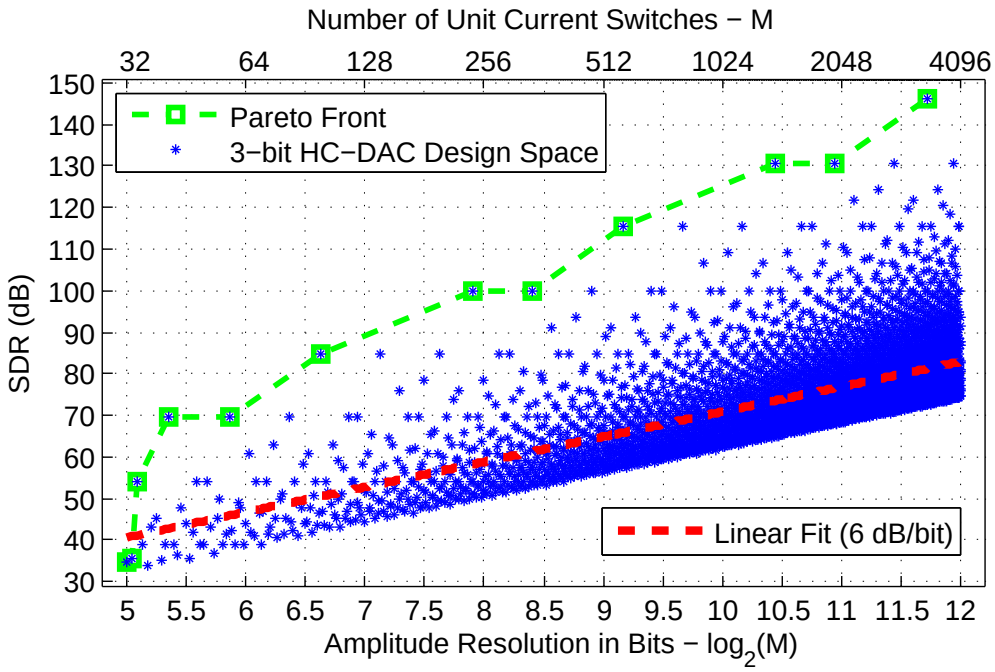


Figure B.1: SDR against amplitude resolution of a 3–bit HC-DAC

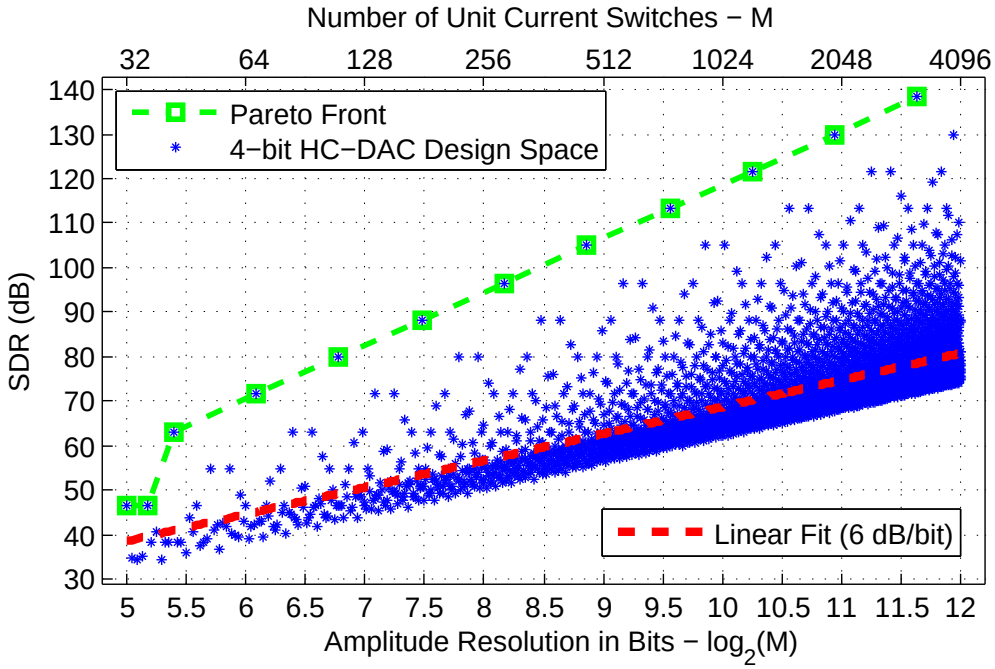


Figure B.2: SDR against amplitude resolution of a 4–bit HC-DAC

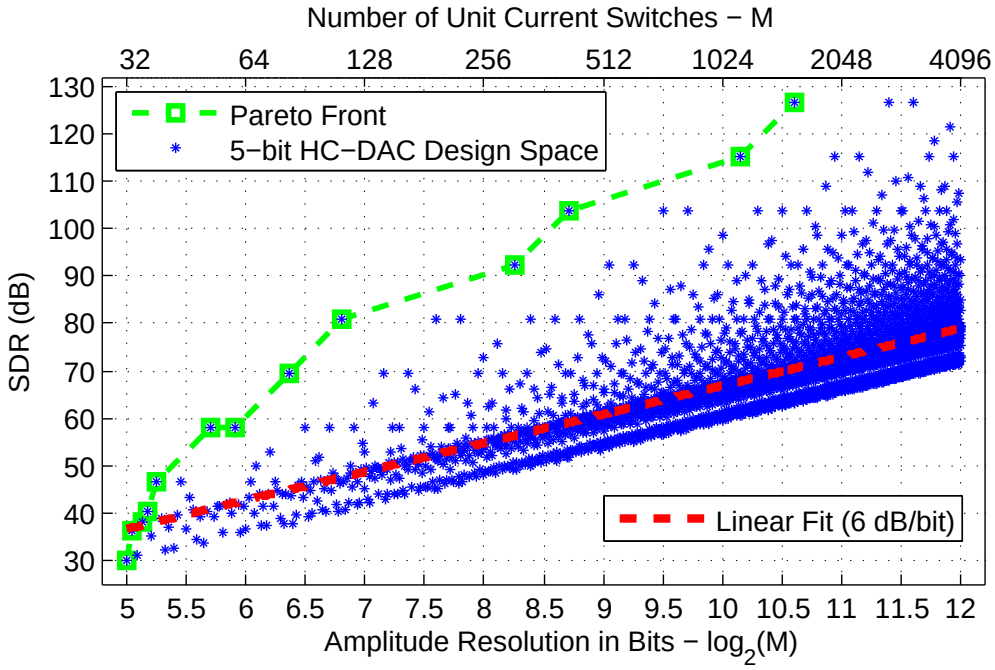


Figure B.3: SDR against amplitude resolution of a 5–bit HC-DAC

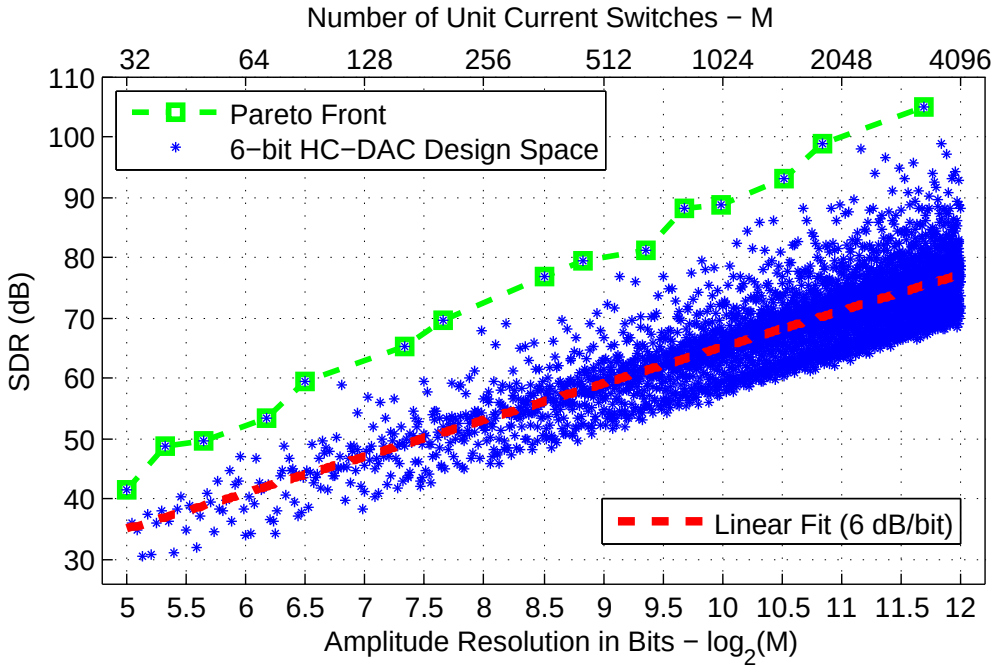


Figure B.4: SDR against amplitude resolution of a 6–bit HC-DAC

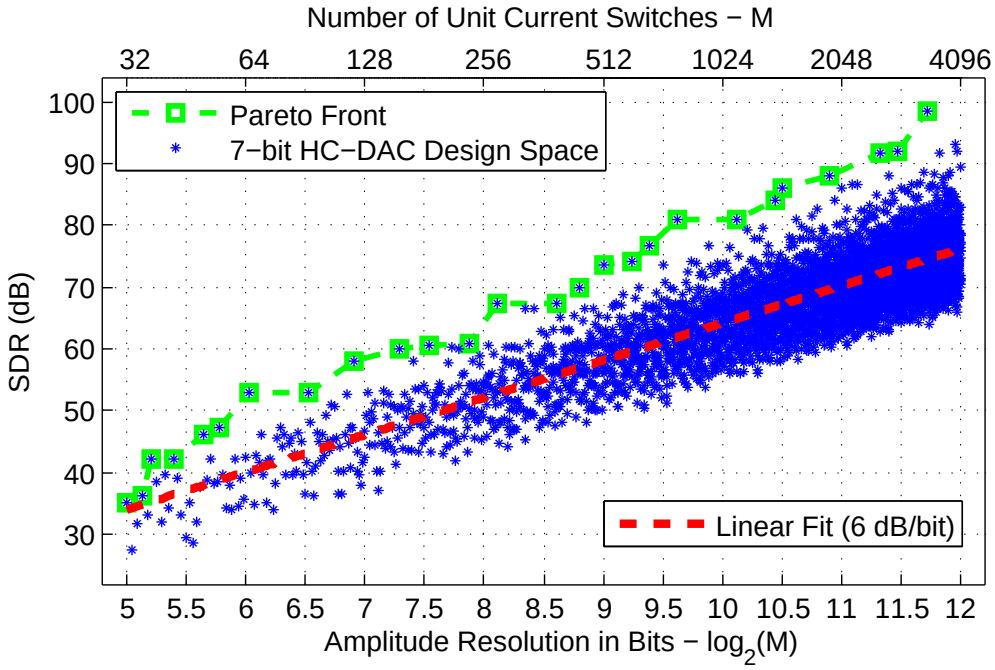


Figure B.5: SDR against amplitude resolution of a 7–bit HC-DAC

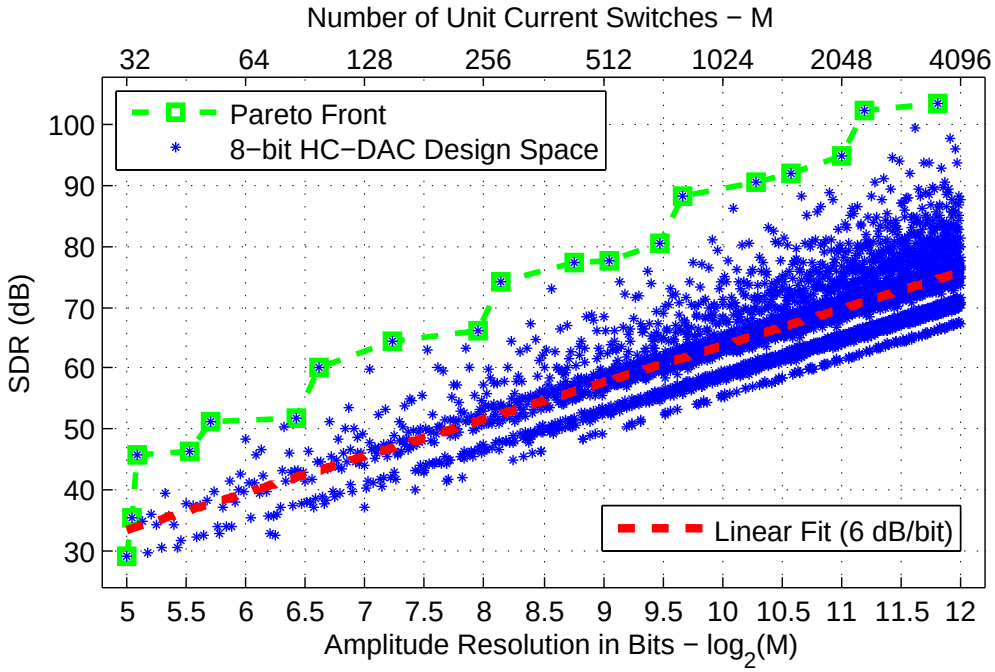


Figure B.6: SDR against amplitude resolution of a 8–bit HC-DAC

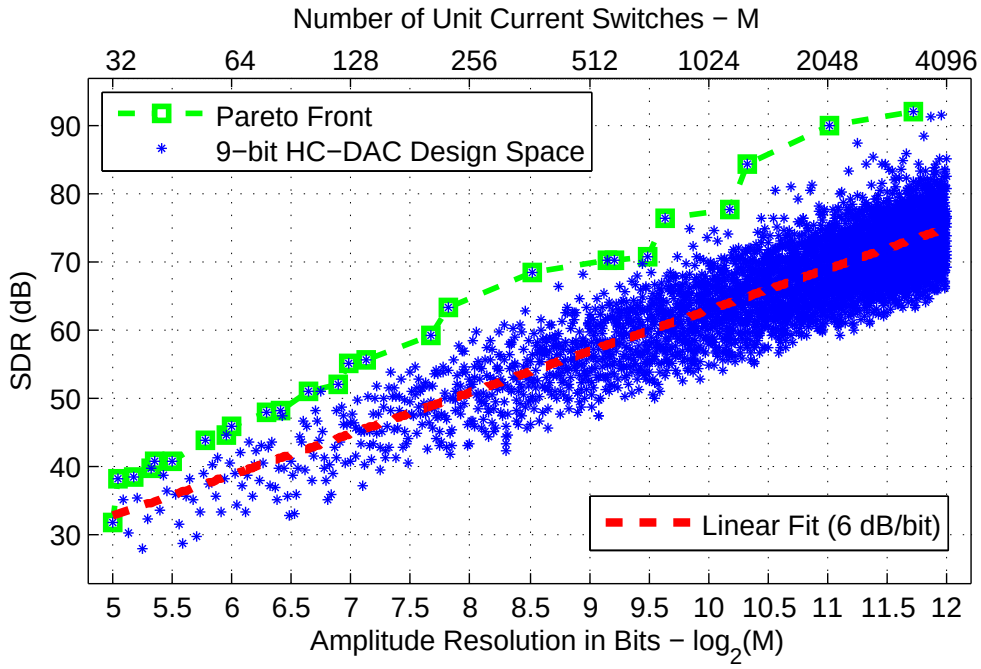


Figure B.7: SDR against amplitude resolution of a 9–bit HC-DAC

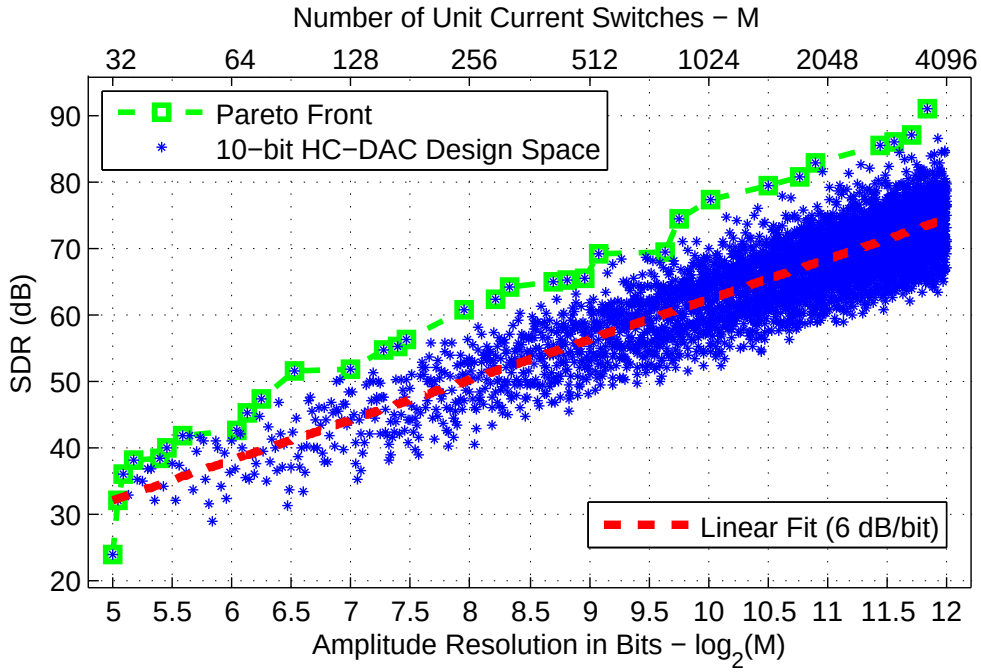


Figure B.8: SDR against amplitude resolution of a 10–bit HC-DAC

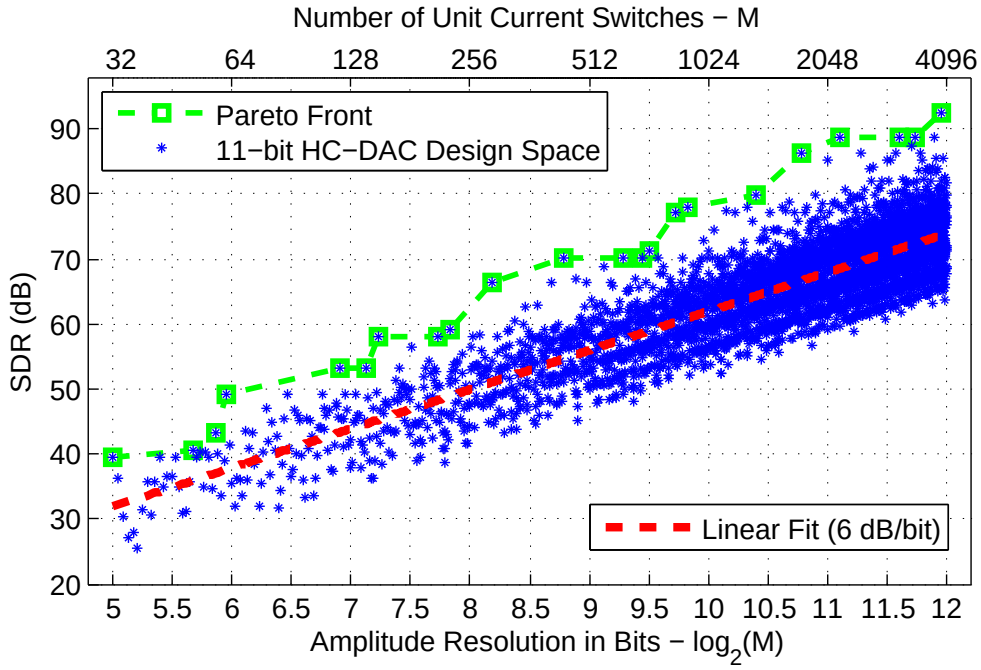


Figure B.9: SDR against amplitude resolution of a 11–bit HC-DAC

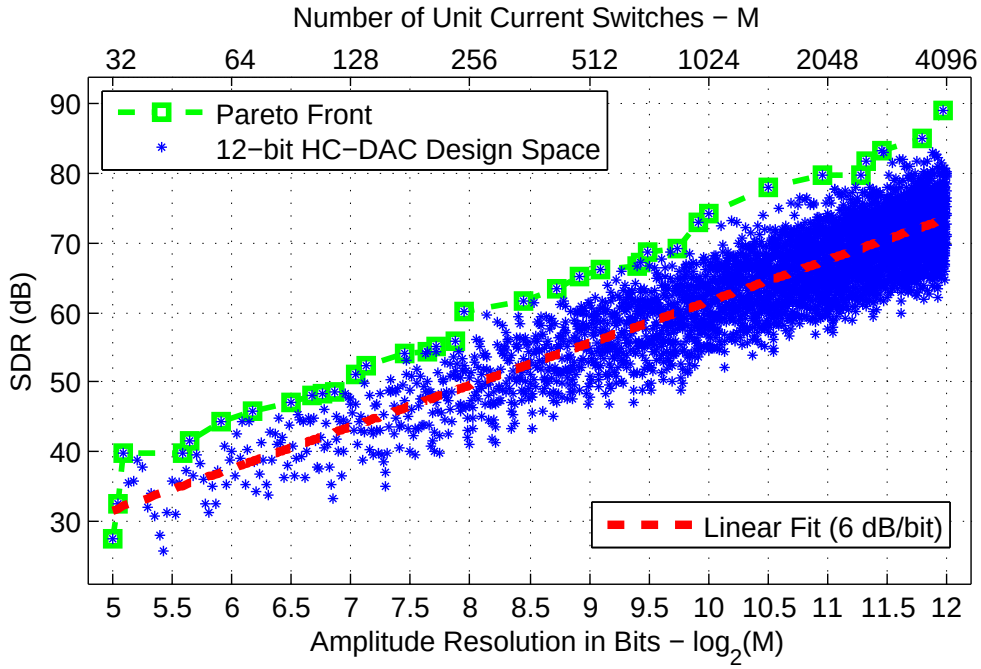


Figure B.10: SDR against amplitude resolution of a 12–bit HC-DAC

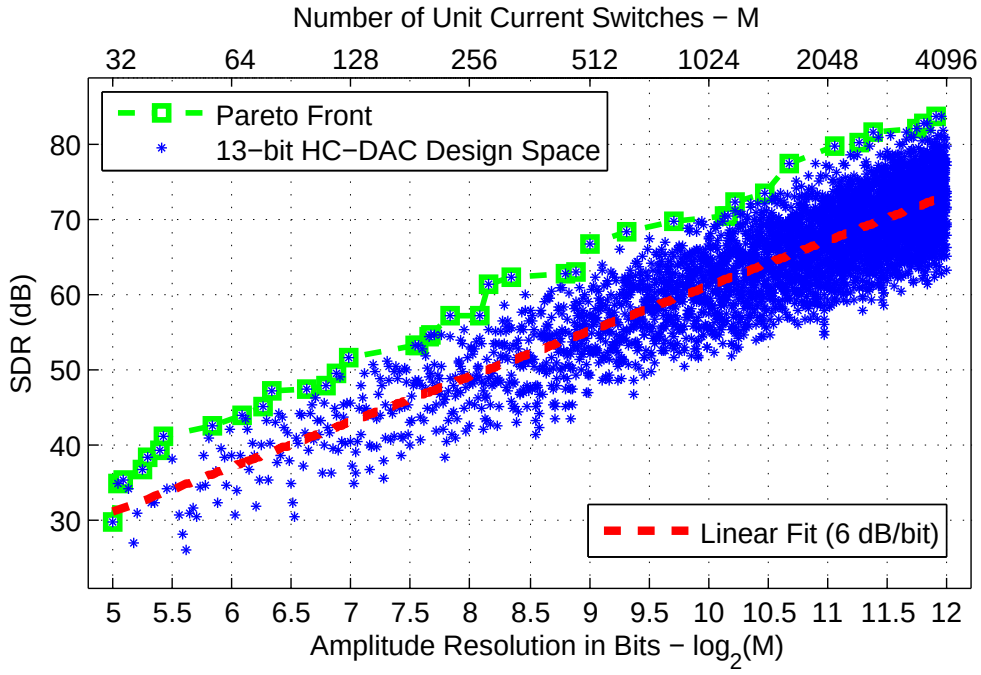


Figure B.11: SDR against amplitude resolution of a 13–bit HC-DAC

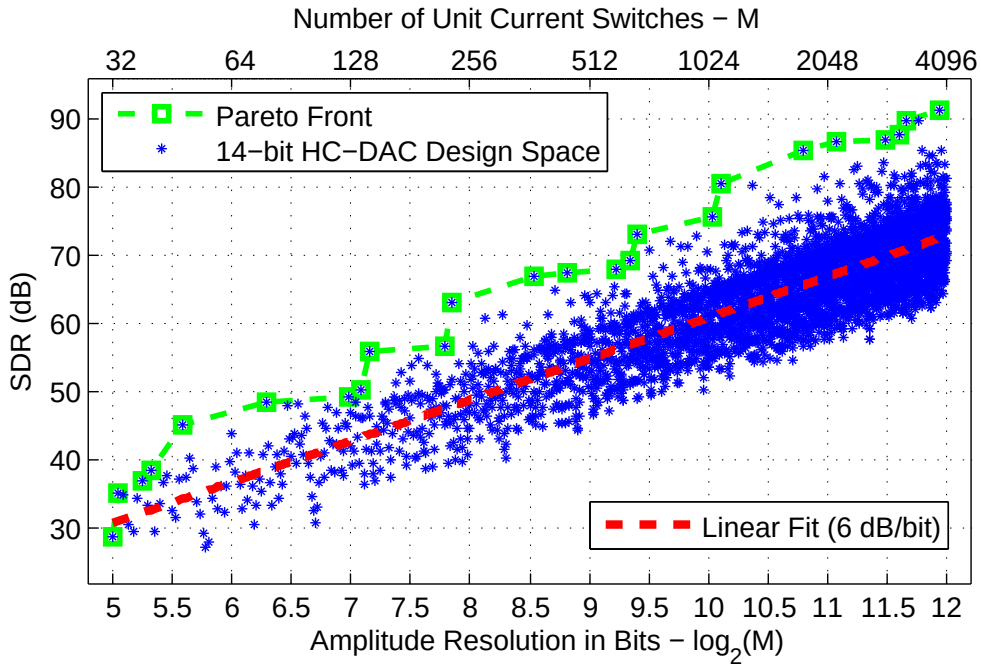


Figure B.12: SDR against amplitude resolution of a 14–bit HC-DAC

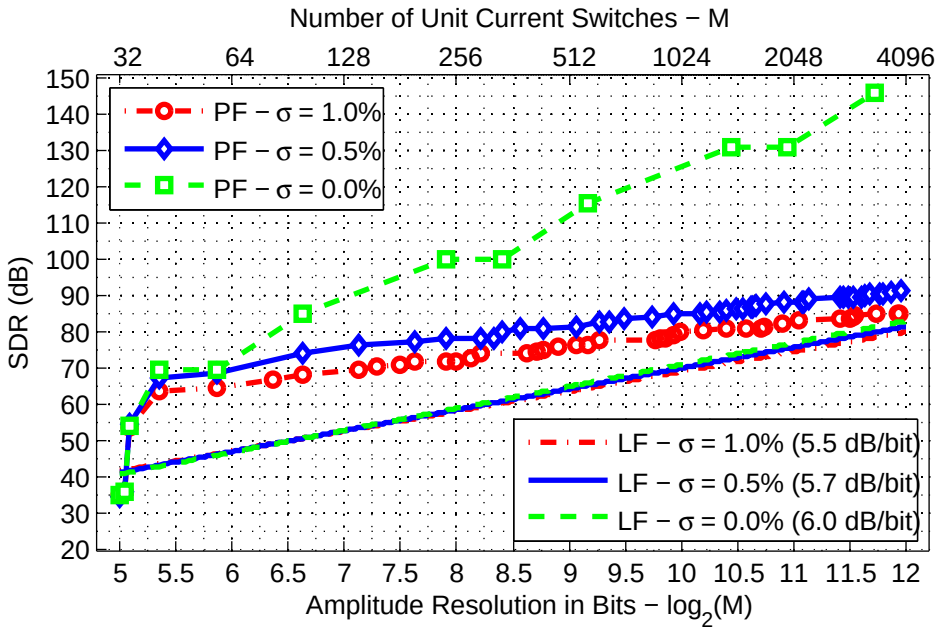


Figure B.13: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 3-bit HC-DAC

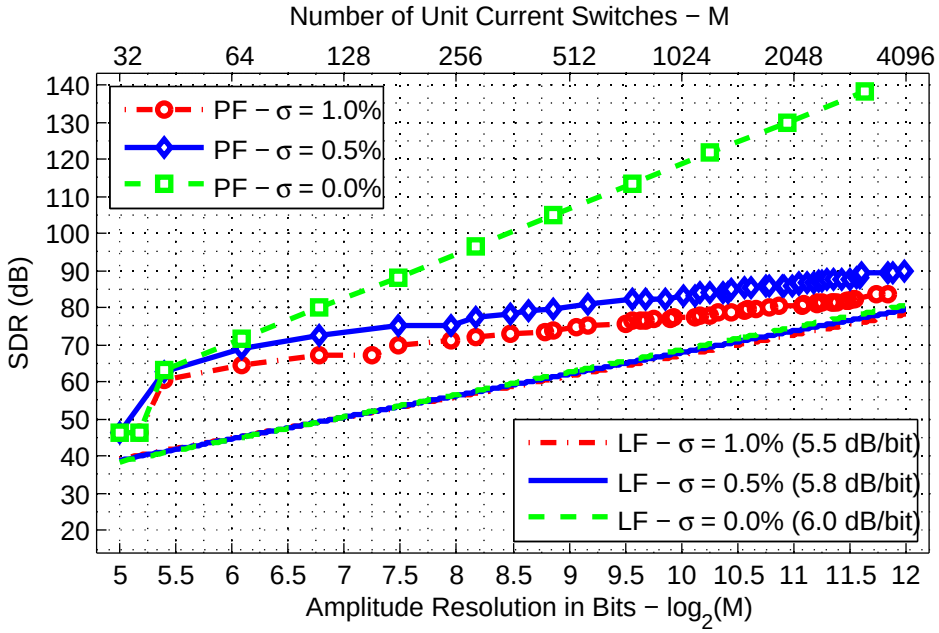


Figure B.14: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 4-bit HC-DAC

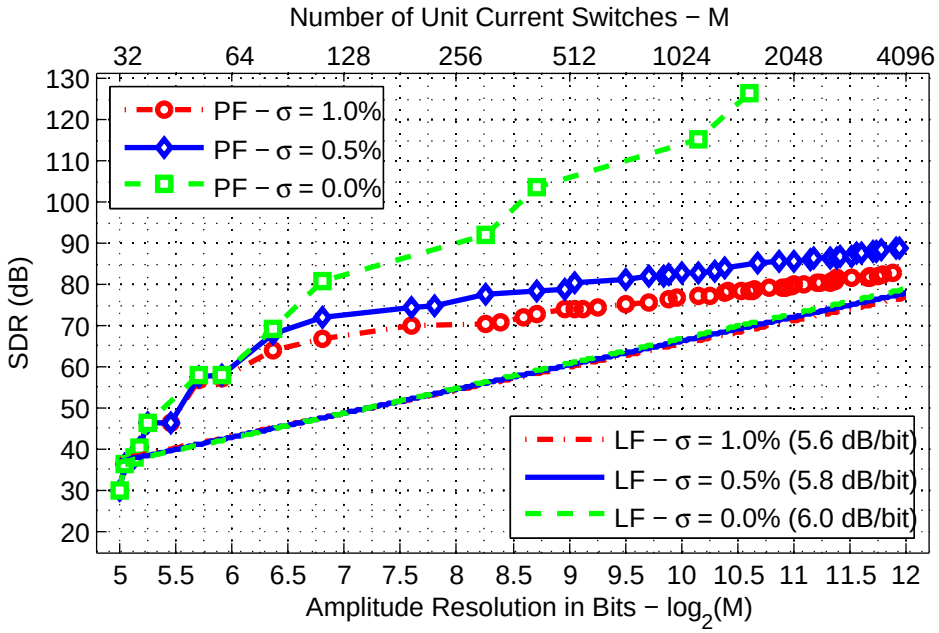


Figure B.15: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 5-bit HC-DAC

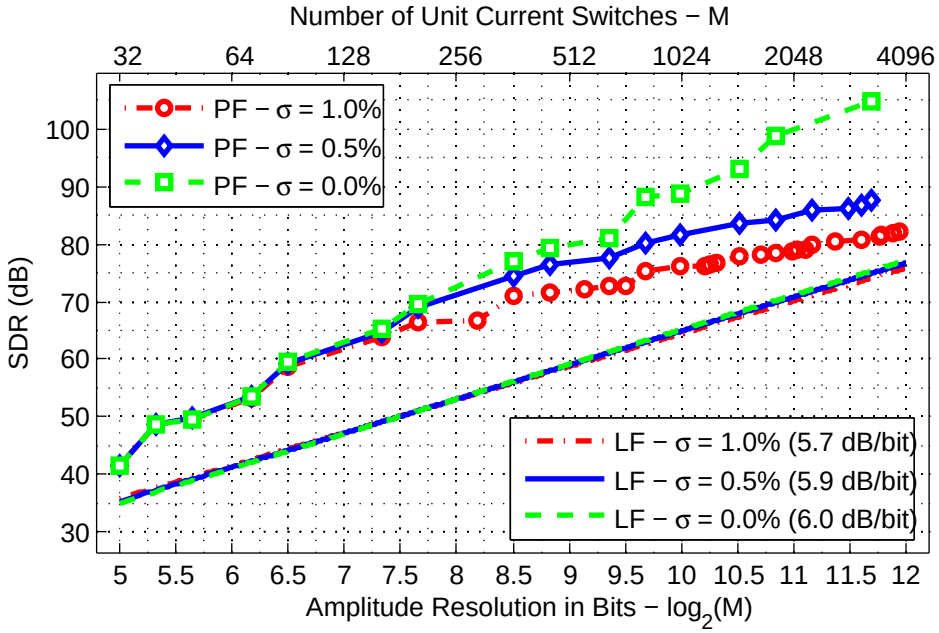


Figure B.16: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 6-bit HC-DAC

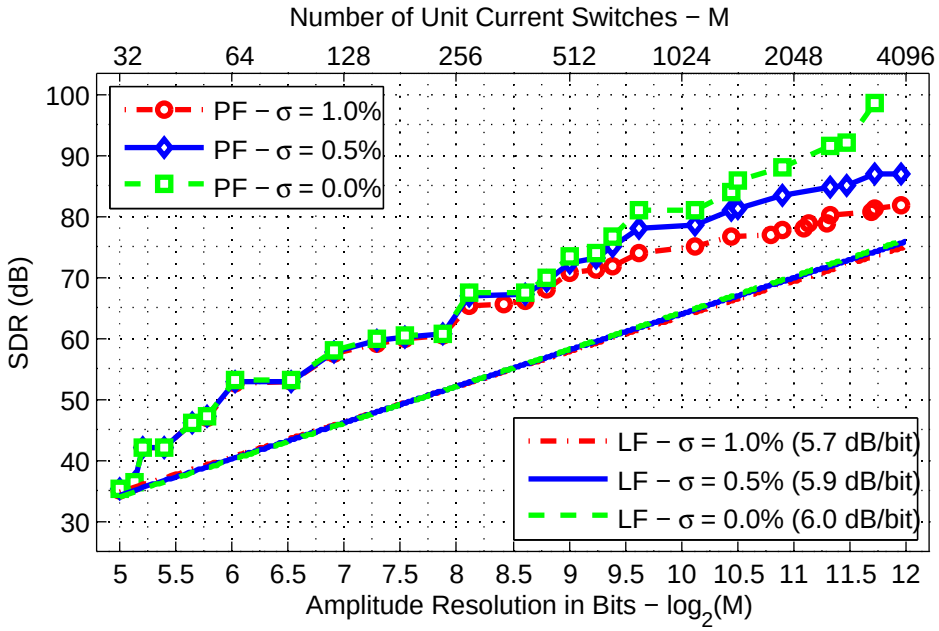


Figure B.17: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 7-bit HC-DAC

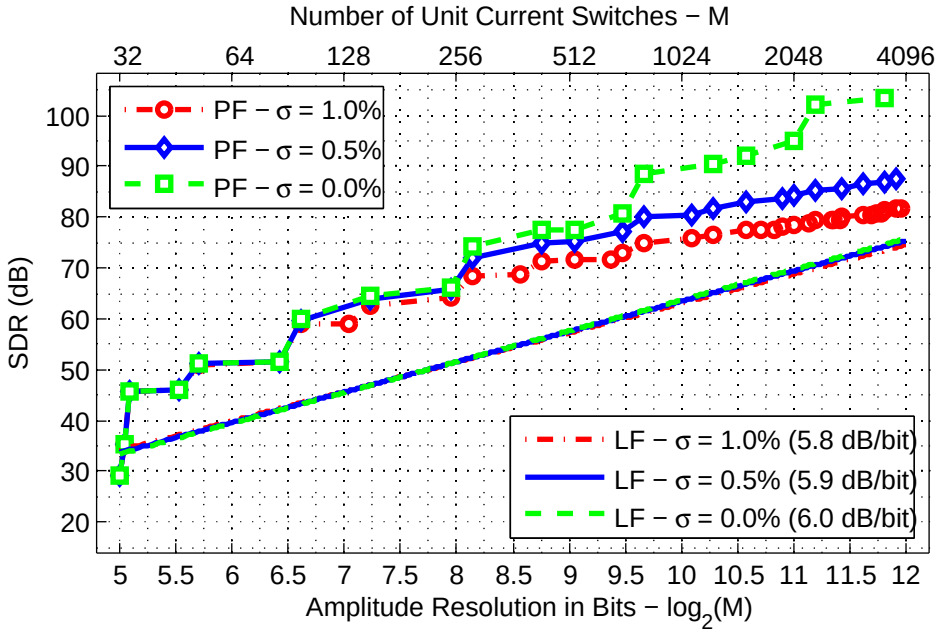


Figure B.18: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 8-bit HC-DAC

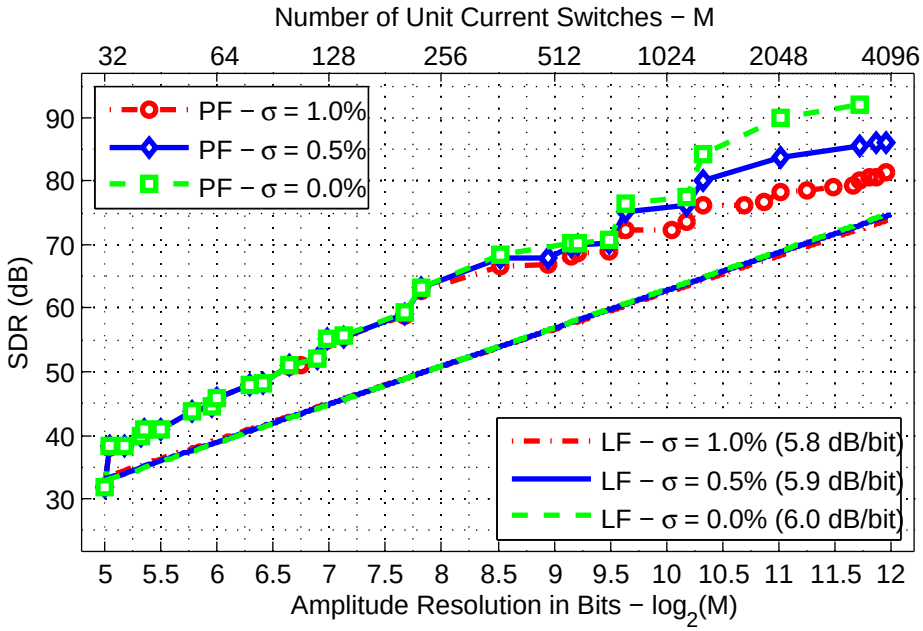


Figure B.19: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 9-bit HC-DAC

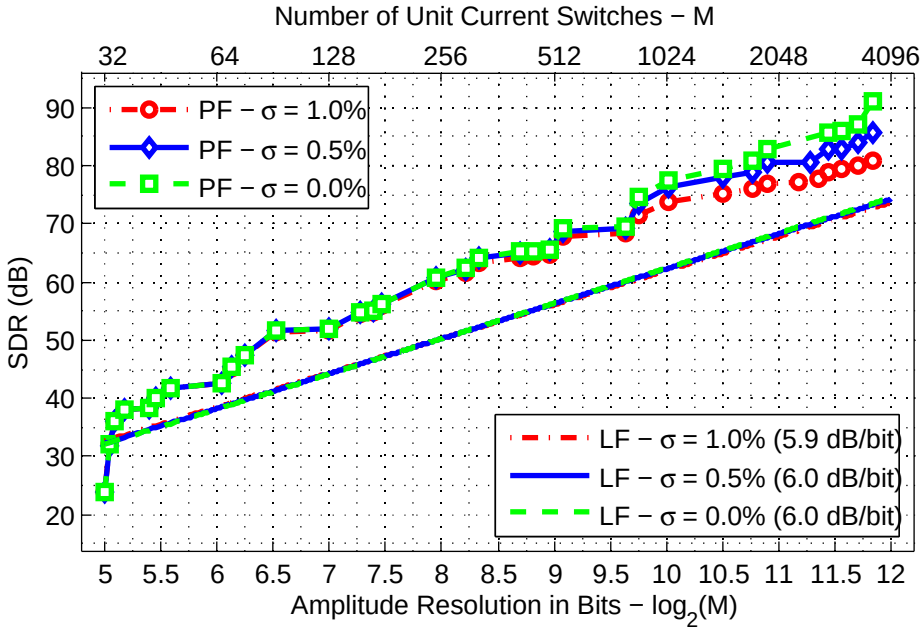


Figure B.20: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 10-bit HC-DAC

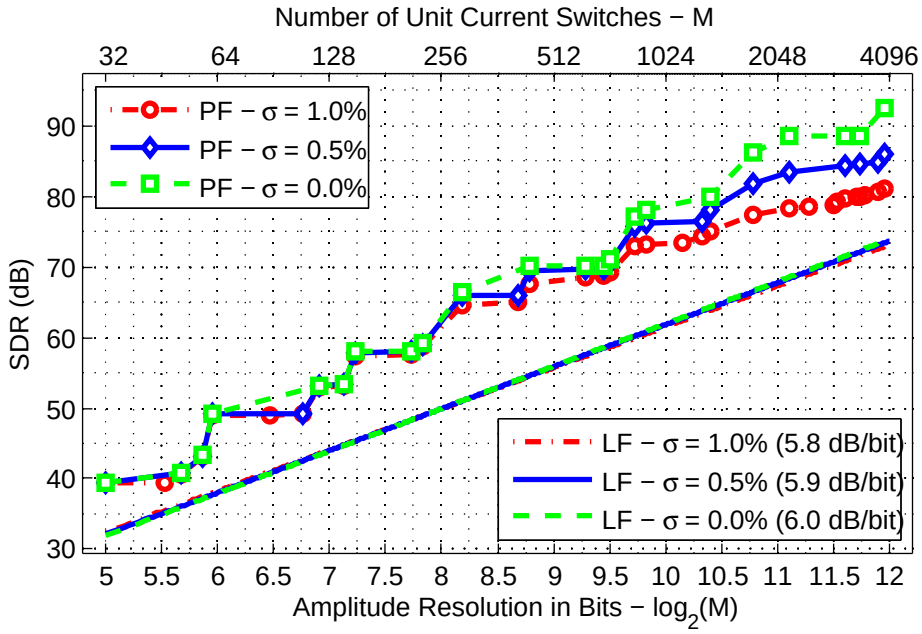


Figure B.21: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 11-bit HC-DAC

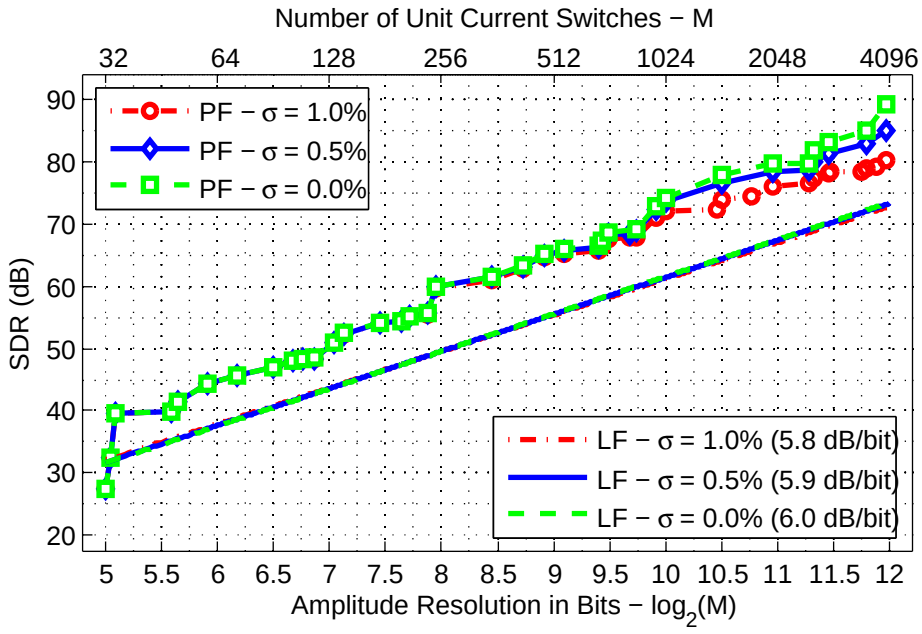


Figure B.22: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 12-bit HC-DAC

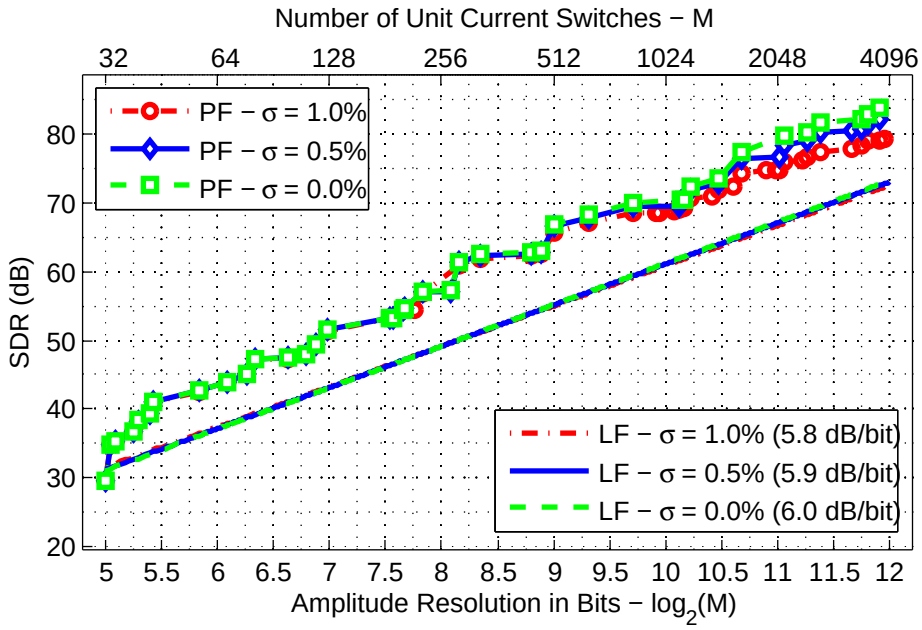


Figure B.23: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 13-bit HC-DAC

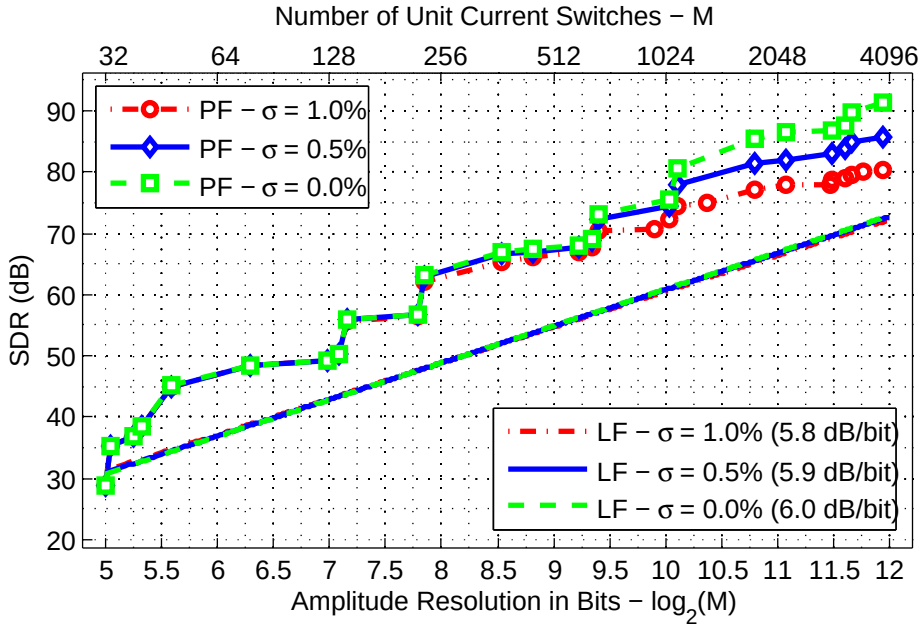


Figure B.24: Pareto Fronts (PFs) and Linear Fits (LFs) of $SDR_{90\%}$ with varying unit-current switch mismatch in a 14-bit HC-DAC

## B.3 Deriving the Expression for $\hat{\Phi}_i(nf_o)$

To begin with, assume that there is zero time-shift between each square-wave signal $\hat{\phi}_i(t)$. Then, $\hat{\phi}_i(t)$ can be mathematically defined as follows:

$$\hat{\phi}_i(t) = \begin{cases} 1 - \frac{2}{t_f(i)}\,(t + T_o/2) & -T_o/2 \le t < -T_o/2 + t_f(i) \\ -1 & -T_o/2 + t_f(i) \le t < 0 \\ -1 + \frac{2}{t_r(i)}\,t & 0 \le t < t_r(i) \\ 1 & t_r(i) \le t < T_o/2 \\ \hat{\phi}_i(t + T_o) & t < -T_o/2 \\ \hat{\phi}_i(t - T_o) & T_o/2 \le t \end{cases} \tag{B.4}$$

The complex Fourier coefficients, $\hat{\Phi}_i(nf_o)$, of $\hat{\phi}_i(t)$ are given by the following equation:

$$\hat{\Phi}_i(nf_o) \;=\; \int_{-T_o/2}^{T_o/2} \hat{\phi}_i(t) \times e^{-j2\pi n f_o t}\,\mathrm{d}t \tag{B.5}$$

Solving the above integral and simplifying the equation gives us

$$\hat{\Phi}_i(nf_o) \;=\; \frac{T}{2n^2\pi^2}\left[\frac{1}{t_r(i)}\left(1 - e^{-2n\pi j\frac{t_r(i)}{T}}\right) - \frac{e^{n\pi j}}{t_f(i)}\left(1 - e^{-2n\pi j\frac{t_f(i)}{T}}\right)\right] \tag{B.6}$$

Now let us take into account the time-shift between each square-wave signal. Ideally, signal $\hat{\phi}_i(t)$ defined in Eq. B.4 should be time-shifted by $(i-1)T_o/(2k+2)$. In the presence of time-shift errors, signal $\hat{\phi}_i(t)$ should be time shifted by $(i-1)T_o/(2k+2) + \Delta t(i)$. Thus, taking into account the error affected time-shifts, Eq. B.6 can be modified as follows:

$$\hat{\Phi}_i(nf_o) = \left(\frac{T_o}{2n^2\pi^2}\right) e^{\left[\frac{n\pi j}{k+1}(1-i) - 2n\pi j\frac{\Delta t(i)}{T_o}\right]}\left[\frac{1}{t_r(i)}\left(1 - e^{-2n\pi j\frac{t_r(i)}{T_o}}\right) - \frac{e^{n\pi j}}{t_f(i)}\left(1 - e^{-2n\pi j\frac{t_f(i)}{T_o}}\right)\right] \tag{B.7}$$

## B.4 Deriving the Expression for $\Phi_i(nf_o)$

First, note that $\Phi_i(nf_o)$ is the $n^{\text{th}}$ complex Fourier coefficient of $\phi_i(t)$. Also, recall that we have already defined the complex Fourier coefficients of $\phi_1(t)$ in Eq. A.22. Then, using the time domain relationship between $\phi_i(t)$ and $\phi_1(t)$ defined in Eq. 5.1, $\Phi_i(nf_o)$ can be defined as follows:

$$\Phi_i(nf_o) = \frac{[1 - \cos(n\pi)]}{n\pi j} \times \exp\left[\frac{n\pi j}{k+1} \times (1-i)\right] \tag{B.8}$$