Metallisation of crystalline silicon thin-film solar cells: power losses, optimisation and interconnection

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Metallisation of Crystalline Silicon Thin-Film Solar Cells: Power Losses, Optimisation and Interconnection

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Abstract

For thin-film crystalline Si solar cells on glass, metallisation is the key to converting what is otherwise a large-area diode, into a true photovoltaic device. The goal of metallisation is to produce devices with as high efficiencies and as little parasitic losses as possible. This is the inspiration here, where the metallisation of crystallised Si material deposited by plasma-enhanced chemical vapour deposition (PECVD) is of particular interest. The metallisation investigated is based on an interdigitated scheme, where the positive and negative electrodes of the device form a comb-like structure on the cell surface. This unique structure allows for a variety of investigations to take place aimed at both improving understanding of the scheme, and exploring methods to further increase efficiencies of metallised devices.

The results are structured into three main parts. In the first part, power loss formulas, both absolute and normalised, were derived for the interdigitated-on-glass device structure. This allows for the characterisation and identification of the various resistive and shadow losses associated with metallisation. Optimal metallisation patterns were then realised by minimising these power losses. The second part involves met-

allisation itself, where device fabrication, sidewall formation, and the impact of thermal annealing were investigated. High-rate PECVD (>200 nm/min) was introduced as a means of combating one of the main drawbacks of PECVD. An efficiency of 5.9 % was obtained on this material - the first reported result for high-rate PECVD poly-Si thin-films on glass. In the third part, the concept of cell tabbing and interconnection using wire-bonding was developed. Both tabbing of individual cells and interconnection to form mini-modules were found to significantly reduce series resistance, boosting fill factors and efficiencies of metallised devices. An 8.05 % efficient individual cell and an 8.28 % two-cell mini-module were fabricated using this technique.

Power loss formulas are derived, further insights into metallisation are presented, and the successful series-interconnection of cells has taken place. There is considerable scope for further improvements in device efficiency from metallisation, via the simultaneous consideration and implementation of multiple results found in this thesis: optimal metallisation patterns, post-metallisation annealing, wire-bonding tabbing/interconnection and encapsulation.

Originality Statement

I hereby declare that this submission is my own work and to the best of knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at UNSW or any other educational institution, except where due acknowledgement is made in the thesis. Any contributions made to the research by others, with whom I have worked at UNSW or elsewhere, is explicitly acknowledged in the thesis. I declare that the intellectual content of this thesis is the product of my own work, except to the extent that assistance from others in the project's design and conception or in style, presentation and linguistic expression is acknowledged.

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Quote

"MEN WANTED for hazardous journey. Small wages, bitter cold, long months of complete darkness, constant danger. Safe return doubtful. Honour and recognition in case of success."

Supposed ad placed by *Ernest Shackleton*, seeking to recruit men for his 1914 Trans-Antarctic Expedition.

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Chapter 1

Introduction

1.1 Motivation

EVER increasing prices for household and commercial electricity on the order of 3 - 4 % per year [1], coupled with the decreasing cost of photovoltaic (PV) module and system prices consistent for the last 30 years [2] present to the author one clear conclusion. Be it 2, 5 or 20 years from now, it is only matter of time before the total cost ($/kWh) of PV electricity for consumers is equal to that of the grid retail electricity price - so called “grid parity” [3]. And should grid parity of PV never be achieved? An alternative electricity generation technology will have been developed that meets most of the advantages of PV, and more - no doubt a requirement for up and coming electricity generation technologies in modern society.

This is seen as a win-win situation. Either PV eventually surpasses grid

parity to become utilised en-masse, or a sustainable, alternative technology with enough advantages to justify wide-scale adoption is developed. Without discounting the author's faith in the ability of science to produce such a technology, it is believed the former scenario is the more likely of the two. It is this belief that has spawned the motivation for contributing towards the advancement of PV technology.

1.2 To the reader

This thesis has been written with the purpose of equipping honours and postgraduate-level students, as well as graduate researchers with the knowledge and tools to analyse, design, and perform the self-aligned metallisation of thin-film poly-Si solar cells.

It is designed to be, in essence, a reference manual, or *handbook* for parties interested in the art of metallisation. Where necessary, additional details are given to allow the reader to expand the concepts for use in the metallisation of other device structures.

A prior knowledge of calculus equivalent to that of a first-year university level would be desired to comprehend the derivations given, however it is not necessarily essential knowledge to gain an appreciation of the principles at work.

1.3 Chapter inspirations

Chapter 3 uses the unit-cell approach to quantify power losses of cells metallised using an interdigitated scheme. The approach to quantifying power losses in this manner is based on that originally brought to the literature in the 1970s by Dr. Harvey Serreze, Dr. Kenneth Heizer, and others. This relatively simple approach to quantifying power losses is particularly relevant to geometric, rectilinear metallisation layouts such as the interdigitated metallisation investigated in this thesis. This was the inspiration and reason for selecting this approach over other methods of quantifying power losses found in the literature.

Chapter 4 investigates, in part, the self-aligned metallisation scheme for forming interdigitated structures. This scheme was originally pioneered and developed circa 2005-2007 by former researchers within the Thin-Film Group at UNSW including Dr. Per Widenborg, Dr. Dengyuan Song, Dr. Tim Walsh and others. The inspiration for the experimental work on the self-aligned metallisation scheme comes from a desire to expand the understanding of this metallisation scheme and enable higher efficiency devices to be fabricated using it.

Chapters 5 and 6 use wire-bonding to form both tabbed individual cells and interconnected mini-modules, respectively. The possibility of using wire-bonding as a method for interconnection thin-film cells on glass was originally raised by Prof. Armin Aberle in a Thin-Film Group meeting in early-mid 2007, at a time when forming successful interconnections of poly-Si devices on glass was proving particularly troublesome.

1.4 Thesis organisation

The structure of this thesis is as follows:

In **chapter 1** the motivation for the advancement of PV technology is given, noting that with increasing electricity prices and the decreasing cost of PV, it is only a matter of time before they cross paths. A note to the reader regarding the purpose of this thesis, and desired pre-requisite knowledge is outlined. Acknowledgement of the people and events that have inspired the core chapters of this thesis is also given.

Chapter 2 gives a brief introduction to the various PV technologies that are either commercially relevant, or currently under the subject of research efforts. Poly-Si material on glass is selected as a technology with future potential to reach the low costs required for the large-scale adoption of PV.

In **chapter 3**, a review of power loss methods is given. The concept of flow current is introduced and power loss derivations, both absolute, and normalised to unit-cell area are then derived. The power loss formulas for the interdigitated metallisation scheme are then summarised.

In **chapter 4** the self-aligned metallisation process is introduced, which is used to produce interdigitated cells. The plasma etching step to form the sidewall is the most critical stage in metallisation, where under-etching causes shunting of the junction and over-etching results in a high series resistance. A post-metallisation thermal anneal step is shown to increase both the voltage and efficiency of devices. In addition, the first

efficiency results for poly-Si cells using a high-rate PECVD absorber on textured glass are reported.

Chapter 5 introduces the concept of forming wire-bond connections from the interdigitated cell's busbars to externally applied tabbing tape ('cell tabbing'). A number of additional investigations are carried out on tabbed devices, including shunt resistance response to wire-bonding, the effect of sequential increases of wire-bonds, and thermal stability. The tabbing technique is then utilised on metallised cells, where high FF (>74 %) and high efficiency (>8 %) tabbed cells are fabricated. The FF is the highest yet reported for a thin-film poly-Si on glass cell metallised at UNSW. No major negative consequences from the wire-bond tabbing of individual cells are found, indicating it's potential as a cell-interconnection technique.

In **chapter 6**, attention turns to the series-interconnection of interdigitated cells to form mini-modules. Interconnection consists of laser isolation scribes, together with wire-bond connections, both between adjacent cells and from the terminal busbars to tabbing tape. The voltage of the mini-modules formed by this technique are over 98% of the voltage sum of the individual cells, indicating successful interconnection has taken place. Large increases in FF and efficiency are reported as a result of the interconnection, leading to the fabrication of an 8.28 % efficient two-cell mini-module, and a 5.63 % efficient four-cell mini-module.

In **chapter 7**, a summary of work covered, a list of original contributions, and an outlook on further work to further advance the metallisation of poly-Si cells on glass is given.

Chapter 2

Background

2.1 PV technologies

AFTER considering the author's motivation and faith in PV technology, the next point is, among the dozens, which specific PV technology? By far the most wide-spread, both commercially and in research are wafer-based silicon solar cells [4]. High record efficiencies, 25.0 % for monocrystalline [5] and 20.4 % for multicrystalline [6] are recorded for wafer-based laboratory cells. In industry, cell efficiencies of 22.9 % are fabricated by SunPower [7], leading to commercially available modules with efficiencies of 20.4 %.

However, one factor that prevents wafer technologies from being adopted on a mass scale is simply the cost of the wafers themselves - almost half the cost of cell fabrication comes from the starting (unprocessed) wafer

[8]. Even with significant cost reductions of other areas of the fabrication and processing of wafer cells, it has only been within the last 12 months that PV electricity is approaching, or in the case of some areas in Australia, has reached grid parity. This has been aided by increasing retail electricity prices and an impending (July 2012) fixed price on carbon emissions [9].

However, if the raw amount of silicon required per cell for wafer technologies is too great, the next logical step that follows is to investigate thinner films with lower material requirements. Thin-films for PV applications are generally grouped into two groups; non-silicon based and silicon-based.

The two most abundant non-silicon based thin-film technologies are cadmium telluride (CdTe), and copper indium galium diselenide (CIGS) cells. CdTe is thought to be a promising thin-film technology due to its optical bandgap (1.5 eV) being very close to that of an ideal solar cell, and it's high optical absorption coefficient [10]. The highest efficiency of 17.3% was recently obtained by First Solar [11] and comes after peak efficiency stagnated for ~10 years [12]. Issues with the technology are related to the materials used: the toxicity of Cd, and the relative scarcity of Te which limits the potential of the technology to a GW_P level. A good review of these issues is given in [13].

CIGS are another strong-absorbing, non-silicon based thin-film technology with potential for efficiencies over 25 %. The issue for this technology is the large gap between laboratory efficiencies obtained on a small scale

(20.3%, cell area ~0.5cm^2) [14] and those attained for modules in a production environment, which are on the order of 15 % [15]. As with CdTe, concerns over the use of Cd and scarcity of elements, in this case indium, is also noted [13].

Among the silicon-based technologies under consideration are amorphous silicon, micromorph (tandem) silicon, and polycrystalline silicon. One of the main problems for these materials entering the market is not the due to the technology itself, but the inintial equipment and capital costs to develop a production environment [16].

Amorphous silicon (a-Si:H) is the oldest and most intensely researched thin-film silicon technology. It is well known as a cheap and versatile material, appearing regularly in consumer electronics such as calculators and watches. From a commercial aspect, a-Si:H is prone to degradation when exposed to light (the Staebler-Wronski effect, SWE, [17]) which forces the differentiation to be made between the as-fabricated efficiency and the 'stabilised' (after light-degradation) efficiency. It is not uncommon for the stabilised efficiency to degrade 20 % (relative) or more beyond the initial efficiency. Additionally, a-Si:H requires the use of a transparent conducting oxide (TCO) to aid in current transport.

Micromorph cells, or tandem *micro*crystalline/a*morph*ous cells have been heavily researched in the past 15 years and show considerable promise with the highest stable efficiency of 11.7 %, reported by Kaneka Corp [18]. The large difference in bandgap between the materials: ~1.1 eV for microcrystalline and 1.7 - 1.8 eV for amorphous makes the materials ideal for tandem structures. The tandem structure also allows for thinner a:Si-H

films, reducing the magnitude of the degradation from the SWE. To keep the a:Si-H film as thin as possible whilst still ensuring sufficient light absorption, an intermediate reflector such as ZnO, or doped silicon-oxide has to be used between the two materials. Furthermore, the thickness of the microcrystalline layer also has to be minimised as a means of reducing the deposition cost [19].

The final silicon-based thin-film technology considered is polycrystalline silicon (poly-Si). This material was previously investigated in depth by Sanyo Electric, where a conversion efficiency of 9.2 % for poly-Si on a metal substrate was reported in 1996 [20]. In recent times, CSG Solar (now: Suntech R&D Australia Pty. Ltd.) have reported an efficiency of 10.4 % for a poly-Si mini-module on a glass superstrate [21]. Due to the high conductivity of doped poly-Si material, no TCO layers are required and light-induced degradation via SWE has not been reported as an issue with the technology [22]. The problem of silicon usage is solved by a combination of thin-films of silicon material (~2 μm) with effective light trapping features, including textured glass and back surface reflectors (BSRs). Poly-Si material is known for it's ability to combine the electronic stability of Si wafers, with the reduced material costs from the use of thin-films [23]. This makes it a possible candidate for a technology capable of breakthroughs in $/kWh in the future.

It is for the above reasons that poly-Si material on glass superstrates is investigated here. Additional details on the deposition and fabrication sequence of the poly-Si on glass technology currently under investigation at UNSW is given in the next section.

2.2 Polycrystalline silicon thin-films on glass

The poly-Si on glass material results from the solid phase crystallisation (SPC) [24] of material deposited via the plasma-enhanced chemical vapour deposition (PECVD) of amorphous silicon.

This PECVD material is in contrast to another thin-film material currently under investigation at UNSW known as EVA [25, 26], which results from the SPC of amorphous material deposited by e-beam *eva*poration under vacuum. The known disadvantage of PECVD as a deposition method is the slow rate (~30 nm/min), which results in through-put issues in an industrial environment.

Until metallisation, diodes of both materials undergo similar processes: SPC for 24 hours at 600 °C in a nitrogen ambient, rapid thermal annealing (RTA) at ~1000 °C for 30 seconds, and hydrogenation (defect passivation) in a hydrogen plasma (~600 °C for 30 minutes). In both cases, the resultant material is a thin (1.5 - 3 μm) film of poly-Si material, containing grain sizes of roughly 0.5 - 2 microns.

The exact deposition and fabrication sequence will be discussed in further detail in chapter 4, however the general structure of a polycrystalline silicon diode consists of: borosilicate glass (3.3 mm thick), SiN (~70 nm) which acts as an antireflection coating and diffusion barrier, n^+ Si (~30 nm), p^- Si (~2000 nm), and p^+ Si (~100 nm). It is the analysis, metallisation, and interconnection of this particular structure of PECVD material that is of particular interest in this thesis.

Chapter 3

Power losses of interdigitated metallisations

"With great power losses come great responsibility."

With apologies to *Stan Lee,* co-creator of Spider-Man.

3.1 Introduction

No body of work on the metallisation and interconnection of semiconductor devices would be complete without careful consideration, and at a minimum, a mention of the various power losses involved. Power losses encompass factors or processes which contribute to the *in*efficiency of photovoltaic devices: absorption of a 700 nm photon (~1.77 eV) by material with a bandgap of 1.12 eV, intra-grain 'trap' defects

of high recombination within the forbidden gap, opaque top-contacts absorbing light, and the series resistance of the metallisation grid-pattern are all some examples of power losses present in photovoltaic devices.

The later two loss mechanisms are of particular interest here. These losses can be summarised as *optical* losses, also referred to as shadow losses, where either metal contacts or etched poly-Si prevents optical absorption, and *electrical* losses, where resistance in the metal contacts and semiconductor material causes the energy to be dissipated as heat.

In this chapter, we will first undertake a review of generic power loss derivations for a standard 'H-design' top-contact design using the unit-cell approach (section 3.2). In section 3.3, the concept of interdigitated top-contact designs is then introduced, noting the differences between interdigitated schemes found in the literature, and that used for the remainder of this thesis. Section 3.4 provides a brief introduction to the formation and structure of the metallisation scheme used to produce the interdigitated metallisation layout investigated here. The unit-cell approach is then used to derive power loss formulas for interdigitated thin-film poly-Si solar cells on glass, which is then expanded to allow for the optimisation of the top contact metallisation of these devices.

3.2 A review: The unit cell approach

3.2.1 Background

The method used to determine power losses in this thesis is based on the unit cell approach given by Serreze [27], although multiple other approaches can be used to analyse power losses due to metallisations. These include the use of 'virtual smearing' [28] and the 'minimum voltage drop' approach [29]. The unit cell approach used here contains a number of assumptions and approximations that need to be recognised; It ignores the influence of high recombination and saturation currents (for example at the cell perimeters [30]); It is assumed that voltage drops due to series resistance are generally small, i.e. $\Delta V \lesssim \frac{kT}{q}$; and it does not take into account the distributed series resistance of photovoltaic devies (see for example [31]). Where $\Delta V > \frac{kT}{q}$, most commonly in concentrator cell applications, but also in devices with high series resistance, this approach leads to an underestimation of power losses [32]. For these high current devices the minimum voltage drop approach is generally preferred.

Whilst the original formulations for the unit cell approach were put forward by Serreze in 1978, applications and modifications are still being contributed to the literature in recent times. Jing [33] (2010) looks at using the unit cell approach for contact optimisation (note that in the paper the unit cell approach has been renamed the 'minimum power loss' (MPL) method). It also lists the 'underestimation of current density in open areas' as a disadvantageous simplifying assumption. The concept

of flow current introduced in section 3.4.2 of this thesis is an attempt to eliminate inaccuracies caused by this assumption. In another paper, Bissels [34] (2011) has applied a similar approach based on unit cell 'segments' to derive power loss formulae for a circular contact grid pattern, as a possible alternative to the more common radial pattern.

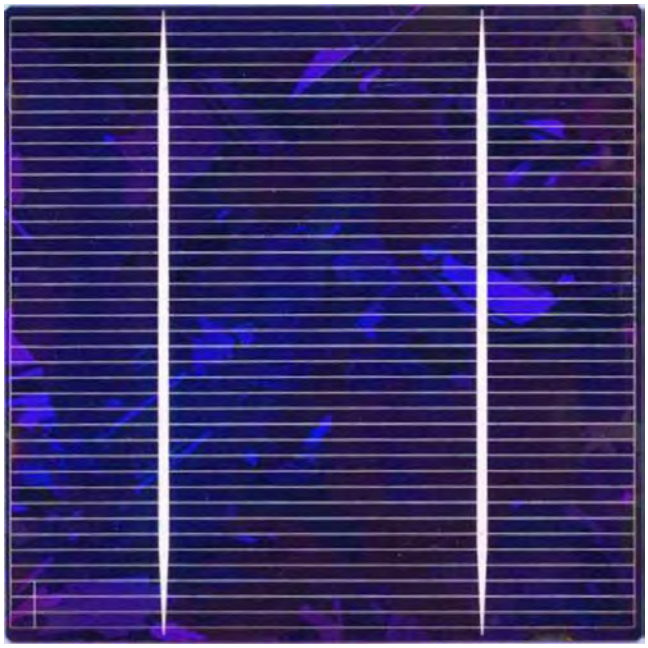


Figure 3.1: A generic, H-design screen-printed wafer cell. The unit cell approach for calculating power losses is highly suited to geometric designs such as this.

What follows in the remainder of section 3.2 are the derivations of power losses using the unit cell approach for a classical H-design, screen-printed solar cell which contains a comb-like front surface contact, and a blanket, full coverage rear contact, such as the generic screen-printed wafer cell in figure 3.1.

The below derivations are used to attain the results given by Serreze [27] and later by Green [35] for this standard, H-design structure.

3.2.2 Lateral resistance of the n-type (emitter) layer

The lateral resistance of the emitter layer refers to the resistance loss as the current travels in a generally perpendicular direction from its point of generation in the semiconductor material to the metal fingers.

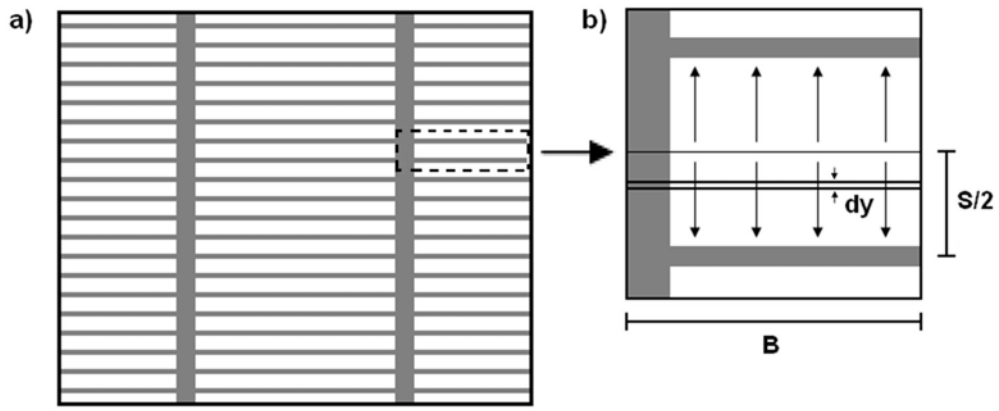


Figure 3.2: a) The H-design grid pattern. b) A segment of the pattern used to derive the power loss in the emitter layer, towards the fingers. The vertical arrows represent the current transport towards the fingers. The unit cell dimensions are B x $\frac{S}{2}$.

A quick look at the geometry in figure 3.2 gives one the impression that the power loss in the region will be strongly dependent on the distance the current has to travel (i.e. finger spacing) and the resistance of the emitter layer.

Firstly, the I^2R resistive power loss towards the finger and along the emitter layer is given by

$$dP_{L,em} = I^2 dR,$$

where the resistance differential dR is equal to $\frac{\rho_{s,em}}{B} dy$.

$\rho_{s,em}$ is the sheet resistivity of the emitter layer with units of $\Omega/\square$, i.e. the resistivity of the layer, ρ, divided by the film thickness. The distance B is the cell width as defined in figure 3.2.

The current at any point along the y-axis is

$$I = JBy,$$

Where y is equal to 0, and hence so is the current, at the midpoint between the fingers, and is maximum (equal to $\frac{S}{2}$) at the edge of the finger. J is the current per unit area of the device, known more commonly as the current density.

By summing the power losses along the current path, the total power loss due to lateral resistance in the emitter layer can be determined. This is given by the integral

$$P_{L,em} = \int_0^{\frac{S}{2}} I^2 dR$$

and upon solving becomes

$$\begin{aligned} P_{L,em} &= \int_0^{\frac{S}{2}} (JBy)^2 \frac{\rho_{s,em}}{B} dy \\ &= \int_0^{\frac{S}{2}} J^2 B y^2 \rho_{s,em} dy \\ &= \frac{1}{3} J^2 B \left(\frac{S}{2}\right)^3 \rho_{s,em} \\ &= \frac{1}{24} S^3 J^2 B \rho_{s,em} \end{aligned}$$

As a means of comparing the relative magnitude of power losses, the *frac-*

tional power loss can be used. This is found by dividing the above power loss ($P_{L,em}$) by the power generated in the relevant cell area it encompasses. This can be done by considering the cell operating under maximum power point conditions (i.e. $J = J_{MP}$), under which the power generated by the cell is equal to $V_{MP} J_{MP} \frac{S}{2} B$.

By dividing the power loss by the power generated we find the fractional power loss ($P_{F,em}$) to be:

$$\begin{aligned} P_{F,em} =& \frac{\frac{1}{24} J_{MP}^2 B S^3 \rho_{s,em}}{V_{MP} J_{MP} \frac{S}{2} B} \\ =& \frac{1}{12} \frac{J_{MP}}{V_{MP}} S^2 \rho_{s,em} \end{aligned}$$

The units of the fractional power loss values are dimensionless, although a meaningful *percentage* power loss (%) can be attained by multiplying the fractional power loss by 100.

3.2.3 Series resistance of the fingers

The fingers are the numerous contact elements that act as an intermediary to transport current from the semiconductor to scarcer (usually 1-4 per solar cell), but larger busbars. Figure 3.3 illustrates the unit cell used to calculate the resistive power losses along the emitter finger. A quick look at the geometry allows one to see that the length, width and thickness of the finger, as well as its resistivity will all play a role in determining the power losses present.

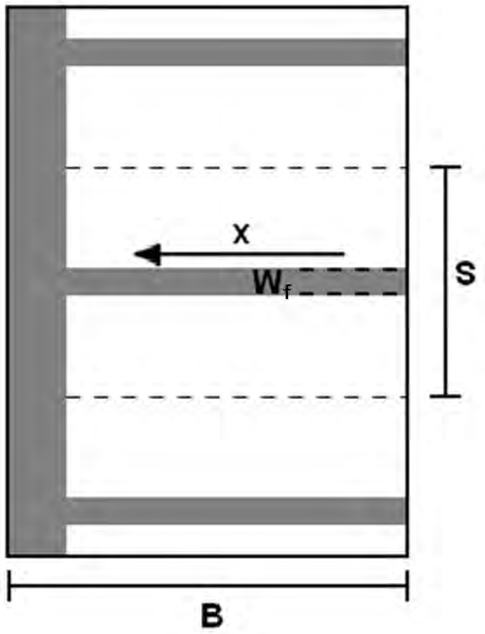


Figure 3.3: A unit cell segment used for calculating the resistive power loss along a finger. The distance S is the finger spacing, B is the cell width and W_f is the finger width. Current flow is along the x-axis towards the busbar on the left.

Once again the resistive I^2R power loss is

$$dP_{L,f} = I^2 dR,$$

where similarly to the above case, dR is $\frac{\rho_{s,f}}{W_f}dx$, in which $\rho_{s,f}$ is the sheet resistivity of the finger. This sheet resistivity value is the resistivity (for example, Ωm) of the finger divided by the thickness, to give a value in ohms per unit square, $\Omega/\square$, as in section 3.2.2. W_f is the width of the finger.

The current at any point along the finger is

$$I = JSx.$$

Where J is the current density, S is the finger to finger distance and x varies from 0, at the far right of the finger, to B. A quick check confirms that the current is 0 at the end of the finger and maximum when it joins the busbar, in which case $I = JSB$.

Summing the power loss along the finger, the integral

$$P_{L,f} = \int_0^B I^2 dR$$

is formed. Filling in the appropriate values and solving, we have

$$\begin{aligned} P_{L,f} &= \int_0^B (JSx)^2 \frac{\rho_{s,f}}{W_f} dx \\ &= \int_0^B J^2 S^2 x^2 \frac{\rho_{s,f}}{W_f} dx \\ &= \frac{1}{3} \frac{\rho_{s,f}}{W_f} B^3 J^2 S^2 \end{aligned}$$

Once again, as a means of enabling comparison between power loss mechanisms, the fractional power loss (here, $P_{F,f}$) is found by dividing the power loss by the power generated in the unit cell area in question. This power, under maximum power point conditions is equal to $J_{MP} V_{MP} SB$. The fractional power loss due to resistance in the fingers is thus

$$\begin{aligned} P_{F,f} &= \frac{\frac{1}{3} B^3 J^2 S^2 \frac{\rho_{s,f}}{W_f}}{J_{MP} V_{MP} SB} \\ &= \frac{1}{3} \frac{J_{MP}}{V_{MP}} \frac{\rho_{s,f}}{W_f} B^2 S. \end{aligned}$$

3.2.4 Series resistance of the busbar

The busbar is the thick contact element that transports current from the numerous fingers to the current extraction point. One can imagine the relevant busbar parameters involved in the resistive power losses along the busbar are similar to those of the fingers - length, width, thickness and resistivity. The derivation of the fractional power loss for the resistance of the busbar is also similar to that of the fingers as thus not as much detail will be provided in this section.

Figure 3.4 shows the previously mentioned H-grid pattern with busbar

length (A), busbar width (W_b) and the example external contacts, which act as the current extraction points, superimposed on the image.

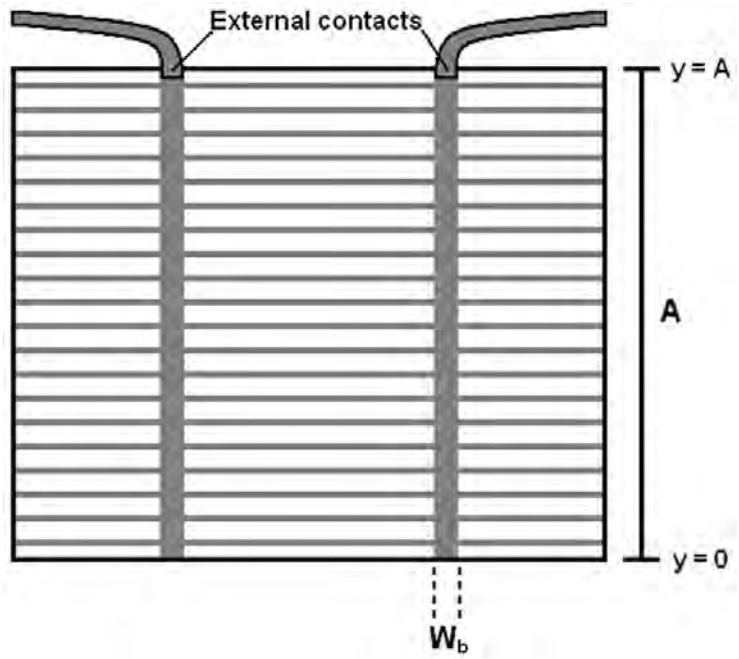


Figure 3.4: The H-grid pattern with busbar length, A, busbar width, W_b and the external contacts shown.

The resistive power loss and dR values are $dP_{L,b} = I^2 dR$ and $dR = \frac{\rho_{s,b}}{W_b} dy$, where $\rho_{s,b}$ is the sheet resistivity of the busbar and W_b is the width of the busbar. The current along the busbar is $I = JBy$, where y ranges from 0 at the bottom of the cell to A, at the points where current is extracted - for instance at a soldered external contact point.

The sum of the resistive power loss along this region is equal to

$$\begin{aligned} P_{L,b} &= \int_0^A J^2 B^2 y^2 \frac{\rho_{s,b}}{W_b} dy \\ &= \frac{1}{3} \frac{\rho_{s,b}}{W_b} A^3 J^2 B^2. \end{aligned}$$

Dividing this by the power generated under maximum power point conditions, we have

$$\begin{aligned} P_{F,b} =& \frac{\frac{1}{3}A^3J^2B^2\frac{\rho_{s,b}}{W_b}}{J_{MP}V_{MP}AB} \\ =& \frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b}A^2B \end{aligned}$$

for the fractional resistance power loss along the busbar, towards the current extraction points.

From figure 3.4 and the above equation, it should be noted that the busbar length, A, can effectively be halved by either adding a second external contact lead at the opposite end of each busbar, or by placing the contact at the halfway point along the busbar. Due to the squared-relationship, reducing the effective busbar length by two times in this manner reduces the fractional resistive power loss along the busbar fourfold.

3.2.5 Shadow losses of the fingers and busbars

The placement of fingers and busbars on the surface of the cell to act as low resistance aids to current transport results in completely opaque areas. These areas that result in no current generation are referred to as 'inactive' layers and their losses as 'shadow' losses.

In the case of fingers, the shadow power loss due to non-absorbed light of a unit cell of dimensions SB is

$$P_{L,sf} = JVBW_f$$

and the fractional power loss resulting from this is

$$P_{F,sf} = \frac{W_f}{S}$$

and is independent of which point along the I-V curve the cell under investigation is operating at.

Similarly, the shadow power loss due to the busbar on an AB-sized unit cell is

$$P_{L,sb} = JVAW_b$$

with a fractional power loss of

$$P_{F,sb} = \frac{W_b}{B}$$

3.2.6 Summary of losses

A summary of the type of loss, the power loss and fractional power loss is given in table 3.1 . When designing solar cells and their metallisation geometries it is clear that particular consideration needs to be given to the largest terms that make up the power loss – namely the length of current travel, which has a cubic dependency.

As mentioned previously, the various 'area-normalised' fractional power losses can be compared and the main areas of power loss for a particular metallisation geometry identified. One further application to assist in

Table 3.1: Summary of key loss areas, quantitative power losses, and the fractional (percentage) power losses, in a typical 'H' design screen-printed solar cell.

Loss area	Power loss [W]	Fractional power loss
Resistive loss in lateral current flow towards fingers	$\frac{1}{24}S^3J^2B\rho_{s,em}$	$\frac{1}{12}\frac{J_{MP}}{V_{MP}}S^2\rho_{s,em}$
Resistance loss in fingers	$\frac{1}{3}\frac{\rho_{s,f}}{W_f}B^3J^2S^2$	$\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,f}}{W_f}B^2S$
Resistance loss in busbar	$\frac{1}{3}\frac{\rho_{s,b}}{W_b}A^3J^2B^2$	$\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b}A^2B$
Shadow loss from fingers	$JVBW_f$	$\frac{W_f}{S}$
Shadow loss from busbar	$JVAW_b$	$\frac{W_b}{B}$

finding the optimal metallisation geometries is to minimise the sum of these fractional power losses. This is discussed below.

3.2.7 Optimisation

For combinations of power losses which contain a common variable, differential calculus can be used to find the point where the sum of losses is at a minimum. The following example is an expanded reproduction from Green [35] and concerns both the resistive power loss and the shadow loss due to the busbar.

The sum of the fractional power losses attributed to the busbar is given by

$$\sum P_{F,b} = \frac{W_b}{B} + \frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b}A^2B.$$

Differentiating this with respect to the busbar width, W_b gives us

$$\frac{d}{dW_b}\left(\frac{W_b}{B}+\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b}A^2B\right)$$

$$=\frac{1}{B}-\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b^2}A^2B.$$

Setting this equal to 0 and solving for W_b will give us the value for the busbar width which corresponds to the minimum sum of fractional power losses. This procedure is carried out below:

$$\begin{aligned}
0 =& \frac{1}{B}-\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,b}}{W_b^2}A^2B \\
W_b^2 =& \frac{1}{3}\frac{J_{MP}}{V_{MP}}A^2B^2\rho_{s,b} \\
W_b =& \sqrt{\frac{1}{3}\frac{J_{MP}}{V_{MP}}A^2B^2\rho_{s,b}} \\
=& AB\sqrt{\frac{1}{3}\frac{J_{MP}}{V_{MP}}\rho_{s,b}}
\end{aligned}$$

Further optimisation steps for other parameters can be carried out, for example, to find the optimal finger spacing corresponding to the minimum power loss. An example of this using an iterative approach is also given by Green in [35].

3.3 Interdigitated metallisations

3.3.1 Introduction

Interdigitated (i.e. interlocking) metallisation patterns are commonly found in both the PV and microelectronics industries. In the PV industry the most abundant interdigitated approach is the interdigitated back contact (IBC) approach, whereby both the positive and negative electrode contacts are placed on the rear of the device.

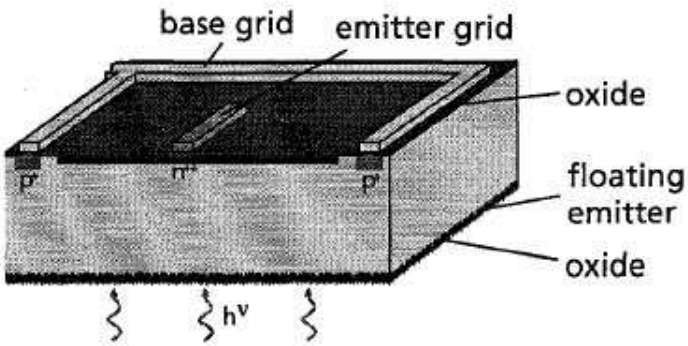


Figure 3.5: A rear-contacted interdigitated cell from [36], with the emitter and base contacts acting as thin 'fingers' on the rear side of the cell.

Figure 3.5 shows an example of the intra-cell doping layout under the grid contacts. Such 'locally diffused' regions within the semiconductor material are a clever way to make use of an interdigitated metallisation scheme.

Figure 3.6 shows a similar isometric view of an interdigitated back contact. In this example, the emitter and base grids are in contact with almost the entire cell surface, which has the effect of reducing resistances

both within the contact materials, and that of lateral current flow within the semiconductor.

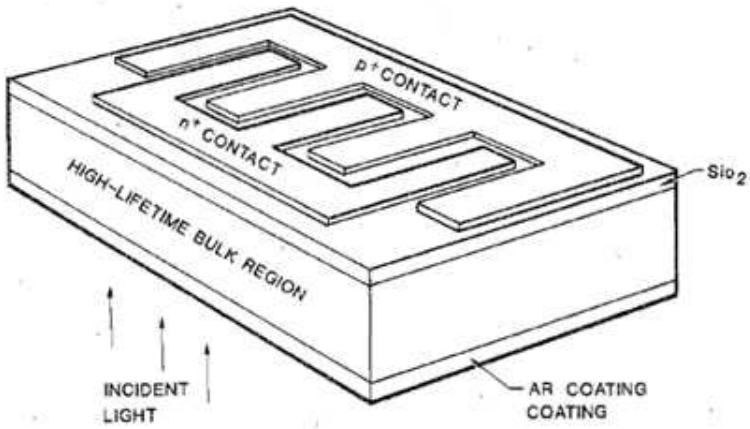


Figure 3.6: Example of a similar, alternate interdigitated metallisation from [37]. The two contacts almost cover the entire cell surface and ensure a low series resistance.

In both cases, light enters from the bottom of the figures, which is by convention named the front side. The lack of metallic contacts on the front side of the cells ensures that no shadow losses are present in the devices. These advantages of IBC-type cells are discussed in further detail in the next section.

3.3.2 Interdigitated back contacts

IBC cells were theorised and developed in the 1970's for use with high efficiency silicon solar cells under high illumination (solar concentrators) [38]. The following four issues were identified as being needed to be addressed with standard cell designs at the time:

1. The shadowing effect from fingers and busbars that lie on the front surface
2. Lateral resistive loss in thin diffused regions at the front of the cell
3. Good lifetimes need to be maintained to prevent the onset of voltage saturation at high concentrations
4. Adoption of an appropriate heat sink

As shown in the previous section, having both contacts on the rear side of the device ensures the front surface is completely illuminated. Although this is particularly important for the case of concentrator solar cells, the minimisation of shadow losses is a requirement for all high efficiency devices. A consequence of IBC-style devices is that the large contact areas between the metallic contacts and the semiconductor material aid in the reduction of contact resistances. Having both contacts on the rear of the cell also allows for virtually no constraints on the aspect ratio of the contacts.

The large contact area of the metallisation contacts may be divided up into closely spaced back-contact fingers, and in combination with localised strips of highly doped material, act to reduce the lateral resistive loss within the device. Figure 3.7 shows an example of multiple, tightly packed locally diffused regions which ensure that the power loss from lateral resistance has a negligible contribution to the internal series resistance of the device: Current flow is almost entirely perpendicular to the surface containing the locally diffused regions.

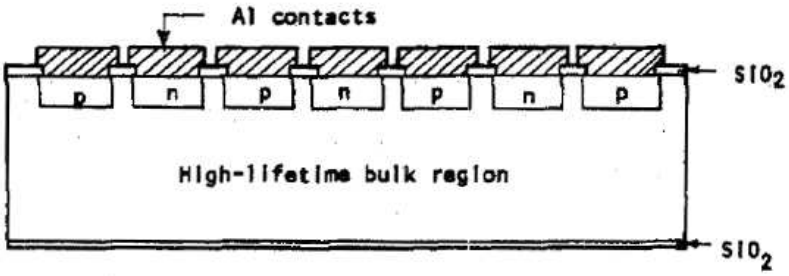


Figure 3.7: A cross section of an IBC cell from [39], showing the Al back contacts and the locally diffused junctions on the rear of the cell.

A high lifetime bulk region, combined with localised n^+ and p^+ regions at the rear of the cell aid in eliminating the occurrence of voltage saturation at high illuminations. The high contact area rear cell-surface of conductive metallic contacts is not ideal for the incorporation of heat sinks, although direct mounting via an epoxy [38] to an electrically insulating material may be used.

Whilst the later two constraints are not applicable to thin-film solar cells, the application of an interdigitated scheme as a means to reduce power losses, both resistive and from shadowing effects, is discussed in the next sections.

3.4 Interdigitated thin-films: Power losses

3.4.1 Introduction

For other silicon thin-film technologies; amorphous (a-Si:H) and micromorph tandem cells, a transparent conducting oxide (TCO, [40]) such as

ZnO:Al or indium-tin oxide (ITO) is used in conjunction with laser scribing to form fully metallised, series-interconnected cells [41][42]. Due to the low electrical conductivity of amorphous and microcrystalline silicon films, a blanket-contact scheme (see for example the continuous ZnO layers present at the top and bottom of the silicon film in figure 3.8) is required, else the device will suffer from large power losses due to lateral resistance in the film.

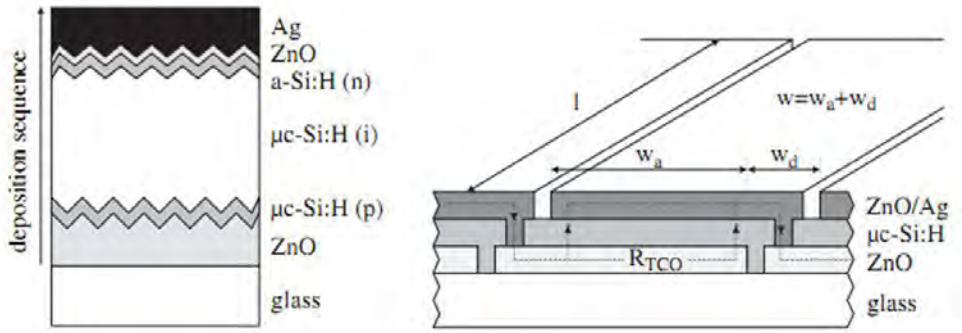


Figure 3.8: A cross section of a metallised microcrystalline p-*i*-n silicon device from [43]. The left image shows the layer structure of the films in a stack (the total thickness is less than 3 μm). The right image shows the interconnection scheme. Separate laser patterning steps have been performed to form the grooves in both the ZnO and μc-Si films.

Recently published results indicate that ZnO:Al-coated glass is compatible with the high post-deposition temperatures (defect anneal and passivation) associated with poly-Si thin-film silicon solar cells formed using the seed layer approach [44]. However, optical absorption within the TCO film still remains a problem [45], whereby a compromise needs to be made between lower series resistance losses resulting from thicker TCO layers, and lower quantum efficiencies and currents due to lower optical transparencies with increasingly thicker layers.

The high lateral conductivity of poly-Si thin-films allows for potentially cheaper schemes where the metallisation does not require the use of a TCO to aid in current transport. One company that makes use of the higher conductivity of poly-Si films is Suntech R&D Australia Pty. Ltd (formerly CSG Solar and Pacific Solar Pty. Ltd.) [46]. The approach used for cell and module-level metallisation involves applying an electrically insulating resin, proprietary patterning processes based on inkjet printing, a silicon etching step, and an Al evaporation step. A cross section of the final metallised device structure is shown in figure 3.9.

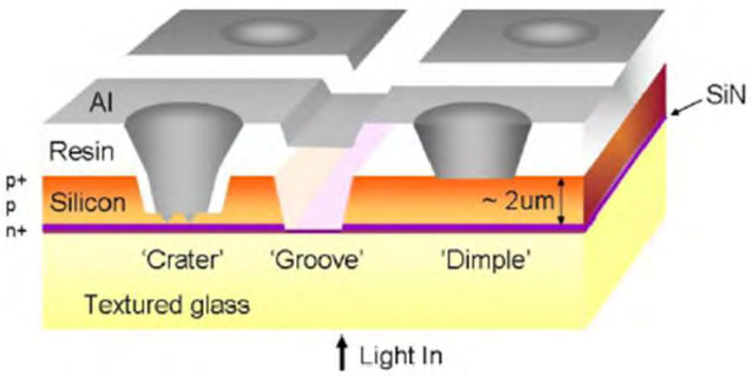


Figure 3.9: A cross section of a metallised Suntech/CSG device structure from [47]. The craters which contact the emitter, and dimples which contact the p^+ back surface field are formed by an inkjet printing based process.

An alternative metallisation scheme first developed by P. Widenborg et al. is currently under continued development at the University of New South Wales [48, 49, 50]. Like that developed by Suntech R&D Australia, no TCO is required in the metallisation, however instead of utilising thousands of point-contact style connections between the polycrystalline thin-film and the metal contacts, continuous grooves (fingers, busbars)

are etched into the silicon material using plasma etching [51, 52]. This results in a comb-like, interdigitated metallisation. Figure 3.10 a) shows a top-down view of the metallised cells, which in this configuration is covered entirely by the metal contacts. Figure 3.10 b) shows a cross section schematic diagram and c), a focused-ion beam (FIB) image of the edge of a plasma-etched groove, where the transition from emitter contact, to bare poly-Si, to airside contact is made.

To facilitate current extraction, the metallisation pattern for the thin-film cells under investigation contain both an emitter-side busbar and an airside busbar, as shown in figure 3.11.

The exact processing sequence of this scheme will be discussed in considerable detail in chapter 4, however it is power losses of this particular interdigitated metallisation (i.e. containing linear grooves that contribute a shadow loss) that are of particular interest for the remainder of this chapter.

3.4.2 The flow current concept

As realised in figure 3.10 b), all areas of emitter features are, in effect, shadow loss areas resulting from the required removal of the poly-Si absorber in these regions. Due to these shadow losses present in the metallisation scheme, a slightly modified version of the short circuit current used in section 3.2 will be required in further calculations.

Let us consider an interdigitated cell with a short-circuit current density of 20 mA/cm^2 and a shading fraction of 10%. With the assumption that

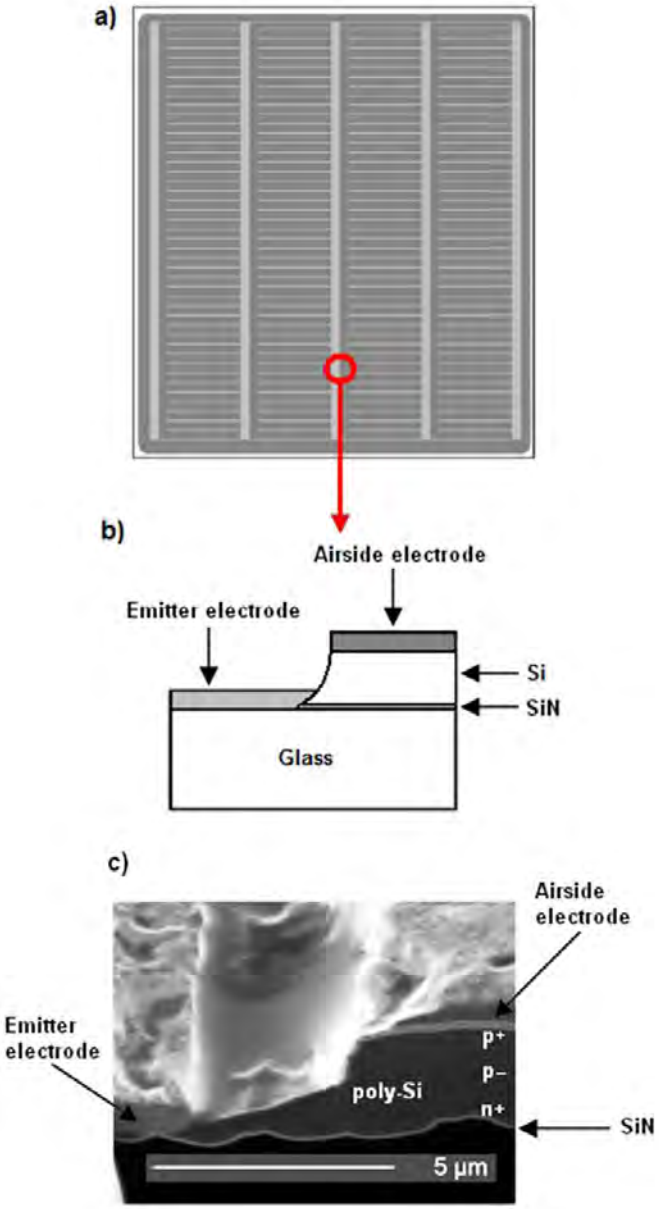


Figure 3.10: Self-aligned interdigitated metallisation of a polycrystalline silicon on glass cell. a) A top-down view of four interdigitated cells. The emitter-side electrode has been etched by plasma etching to the glass and is shown in light grey. The air-side electrode is shown in dark grey. b) A cross section of the emitter/airside sidewall profile of the plasma-etched finger and busbar grooves. Light enters from the bottom of the cell, through the glass. c) A focused-ion beam (FIB) image of the same cross section of a metallised device. A trench has been milled and the sample tilted to 45º to view the cross section. The black area at the bottom of the image is the supporting glass.

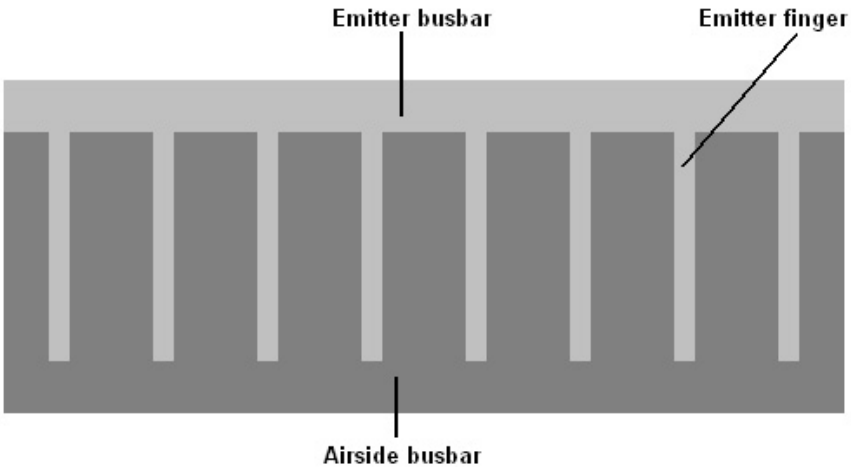


Figure 3.11: A top-down view of a cell segment of an interdigitated thin-film solar cell. The emitter fingers, which contribute to the shadow loss are shown larger for the purpose of clarity.

all light hitting the emitter features (fingers and busbars) is lost, the actual current that flows through the semiconductor material is, in this example, over 22.2 mA/cm^2. This increased current value, proportional to the shading fraction, will be referred to as *flow* current (J_F) for the remainder of this thesis. Quantitatively, the flow current is given by:

$$J_F = \frac{J_{MP}CS}{SW_A + B(S - W_F)} = \frac{J_{MP}}{1 - P_{sh}},$$

where P_{sh} is the fractional shading percentage due to emitter features. The parameters C and S are the unit cell length and width, respectively. B is the finger length, whilst W_A and W_F are the widths of the airside busbar, and emitter fingers, respectively. These parameters are graphically defined in figure 3.12.

The distinction between J_F and J_{MP} becomes more critical as the shading fraction increases - particularly as the current density will be later squared to form resistive (I^{2}R) losses, as in the following sections.

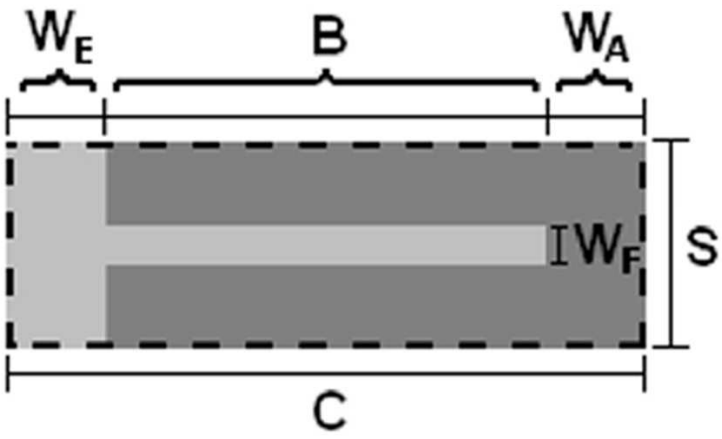


Figure 3.12: A finger unit cell of an interdigitated polycrystalline solar cell. Once again for consistency the lighter grey area corresponds to emitter features, and the dark grey to the airside features. W_E is the width of the emitter busbar, W_F is the emitter finger width, W_A is the airside busbar width, C is the cell length, B is the finger length, and S is the centre to centre finger spacing.

3.4.3 Resistance loss: Emitter layer

Derivation of the power losses in interdigitated silicon thin-film cells is done in the same manner as the unit cell approach given in section 3.2. However, modifications pertaining to the interdigitated air-side/emitter metallisation structure of the thin-film cells, as well as the inclusion of flow current are included to form a more representative view of the power losses in interdigitated cells.

Figure 3.13 (a) shows the relevant geometry regarding the power loss of the emitter layer. Due the particular interdigitated nature of the cells, current is generated wherever there are no emitter features (i.e. under all dark grey air-side features).

There are two areas that contribute to the resistance loss of the emitter

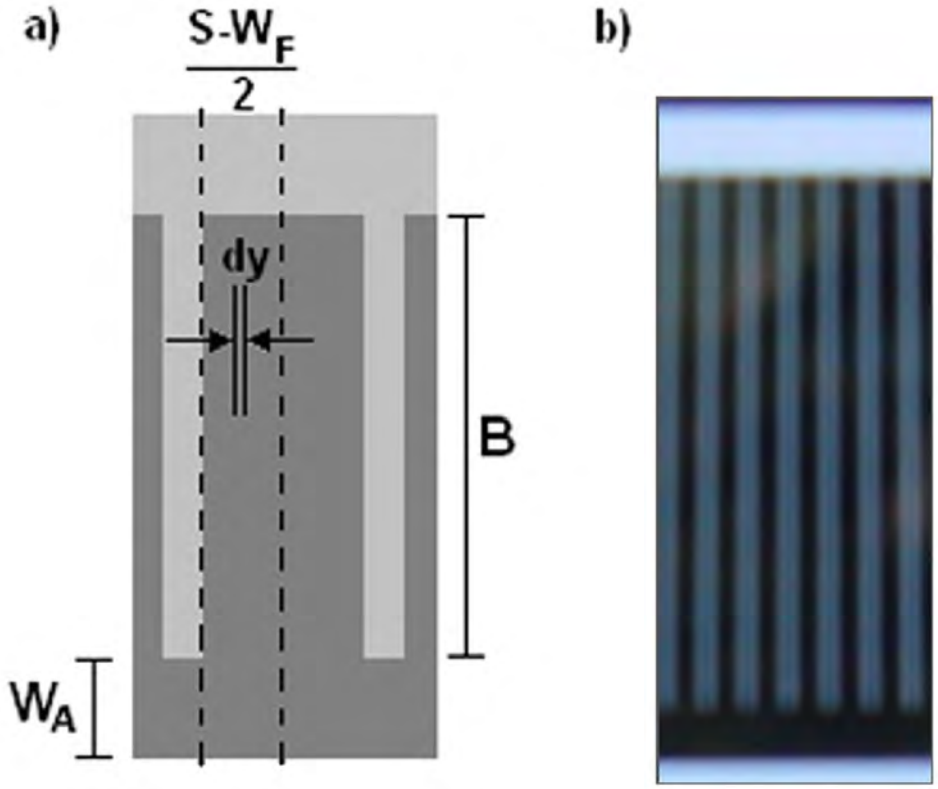


Figure 3.13: a) A schematic of a segments of an interdigitated thin-film cell. Current generated between the (light grey) emitter fingers travels perpendicularly towards the fingers. Current generated under the air-side busbar (shown with width W_A) travels towards the tip of the emitter finger. b) A digital photograph of an actual photomask used to produce emitter features. The lighter regions form emitter features and the black areas form the air-side electrode area. Note that the air-side busbar (thick, black horizontal section at the bottom of the image) is considerably wider than the finger spacing between emitter fingers.

layer - current generated between the emitter fingers, and current generated under the air-side busbar. For a unit cell of dimensions $\frac{CS}{2}$, the current generated in the area bounded by the emitter fingers, I_1 is equal to $J_F y B$, where y varies from 0, at the mid-point in between the emitter fingers, and $\frac{S-W_F}{2}$, at the region along the edge of the emitter finger. The resistance differential, dR_1 is given by $\frac{\rho_{s,em}}{B} dy$, where $\rho_{s,em}$ is the sheet resistivity of the emitter layer.

Figure 3.13 (b) shows an example of a (to-scale) photomask used to produce the interdigitated metallisation pattern. In practice, the airside busbar (of width W_A) is considerably larger than the finger spacing between emitter fingers. This is due to a number of space requirement factors that require the airside busbar to be markedly wide; that for cell interconnection, probing and characterisation, and external (current extraction) contact placement.

For airside busbar widths greater than emitter finger spacing ($W_A > \frac{S}{2}$), all current generated under the airside busbar can be though of as travelling directly towards the terminal of the emitter fingers. Using this approximation, the current generated under the air-side busbar, I_2 is $J_F x \frac{S}{2}$, where x goes from 0 at the end of the cell to W_A at the edge of the emitter finger. The resistance differential in this region, dR_2, is $\frac{\rho_{s,em}}{\frac{S}{2}} dx$.

The total power loss throughout the emitter layer is given by the sum of

power losses in both regions:

$$
\begin{aligned}
dP_{L,em} &= I_1^2 dR_1 + I_2^2 dR_2 \\
&= (J_F y B)^2 \frac{\rho_{s,em}}{B} dy + \left[J_F x \left(\frac{S}{2} \right) \right]^2 \frac{\rho_{s,em}}{\frac{S}{2}} dx \\
P_{L,em} &= \int_0^{\frac{S-W_F}{2}} J_F^2 y^2 B \rho_{s,em} dy + \int_0^{W_A} J_F^2 x^2 (\frac{S}{2}) \rho_{s,em} dx \\
&= \frac{1}{24}(S - W_F)^3 J_F^2 B \rho_{s,em} + \frac{1}{6} W_A^3 J_F^2 S \rho_{s,em} \\
&= \frac{1}{6} J_F^2 \rho_{s,em} \left[\frac{1}{4}(S - W_F)^3 B + W_A^3 S \right]
\end{aligned}
$$

As in the classical unit cell approach detailed in section 3.2, the total power loss is divided by the power generated in the area of the unit cell to give a fractional power loss, so that power losses of different sized unit cells can be compared. For the case of the emitter layer, the unit cell size is $C\frac{S}{2}$, the power generated in this area is $J_{MP} V_{MP} C \frac{S}{2}$, and the fractional percentage power loss, $P_{F,em}$ is thus:

$$
\begin{aligned}
P_{F,em} &= \frac{\frac{1}{6} J_F^2 \rho_{s,em} \left[\frac{1}{4}(S - W_F)^3 B + W_A^3 S \right]}{J_{MP} V_{MP} C (\frac{S}{2})} \\
&= \frac{1}{3} \frac{J_{MP}}{V_{MP}} \frac{1}{(1 - P_{sh})^2} \frac{\rho_{s,em}}{CS} \left[\frac{1}{4}(S - W_F)^3 B + W_A^3 S \right]
\end{aligned}
$$

3.4.4 Resistance loss: Emitter fingers

Figure 3.14 shows a similar unit cell schematic to that required for the emitter layer calculation, with the differential direction along the emitter finger length defined and superimposed on the figure. The power loss differentials in this circumstance are familiar: $dP_{L,ef} = I^2 dR$ and $dR =$

$\frac{\rho_{s,Al}}{W_F}dx$, where $\rho_{s,Al}$ is the sheet resistivity of the Al film and W_F is the width of the emitter finger.

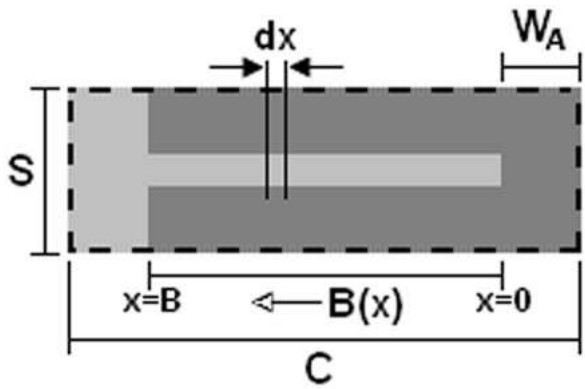


Figure 3.14: An alternate schematic of an emitter finger unit cell, depicting the directional differential along an emitter finger of length B. The emitter finger and emitter busbar are shown in light grey.

In determining the current flowing through the device, it is assumed that current is uniformly generated in the areas where absorbing poly-Si is located - the darker-shade areas of figure 3.14. The total current flow along the finger is equal to the current generated in the area between adjacent emitter fingers, as well as in the airside busbar region - the area bounded by S x W_A.

Mathematically, this current flow this takes the form:

$$I = J_F x(S - W_F) + J_F S W_A$$

where J_F is the flow current density.

A quick substitution confirms the current is equal to $J_F S W_A$ at the end of the finger $(x = 0)$, and $J_F\,[B(S - W_F) + SW_A]$ where the finger joins the

busbar at $x = B$.

Substituting this into the power loss differential and integrating from the end of the finger to the emitter busbar, we find the total power loss solely as a function of J_F and the metallisation parameters:

$$\begin{aligned}
dP_{L,ef} =& I^2 \frac{\rho_{s,Al}}{W_F} dx \\
=& \left[J_F x(S - W_F) + J_F S W_A\right]^2 \frac{\rho_{s,Al}}{W_F} dx \\
P_{L,ef} =& \int_0^B \left[J_F x(S - W_F) + J_F S W_A\right]^2 \frac{\rho_{s,Al}}{W_F} dx \\
=& \int_0^B \left[J_F^2 x^2 (S - W_F)^2 + J_F^2 S^2 W_A^2\right] \frac{\rho_{s,Al}}{W_F} dx \\
=& \frac{1}{3} B^3 J_F^2 (S - W_F)^2 \frac{\rho_{s,Al}}{W_F} + B J_F^2 S^2 W_A^2 \frac{\rho_{s,Al}}{W_F} \\
=& J_F^2 B \frac{\rho_{s,Al}}{W_F} \left[\frac{1}{3} B^2 (S - W_F)^2 + (S W_A)^2\right]
\end{aligned}$$

Once again, dividing this by the power generated in the relevant unit cell under investigation ($J_{MP} V_{MP} C S$), the total fractional power loss along emitter fingers can be found to be:

$$\begin{aligned}
P_{F,ef} &= \frac{P_{L,ef}}{C S J_{MP} V_{MP}} \\
&= \frac{J_{MP}}{V_{MP}} \frac{1}{(1 - P_{sh})^2} \frac{B}{CS} \frac{\rho_{s,Al}}{W_F} \left[\frac{B^2}{3} (S - W_F)^2 + (S W_A)^2\right]
\end{aligned}$$

3.4.5 Resistance loss: Airside fingers

The derivation of the resistance loss along the airside fingers is similar to that of the emitter fingers, with the current component generated under

the airside busbar excluded. The only parametric difference is in the resistive differential, $dR = \frac{\rho_{s,Al}}{S-W_F}dx$, where the airside finger width $(S - W_F)$ has replaced the emitter finger width W_F, which was used in the preceding section.

It follows that the power loss along the air-side fingers is given by:

$$P_{L,af} = \frac{1}{3}B^3 J_F^2 (S - W_F)\rho_{s,Al}$$

and the fractional power loss in the CS-sized unit cell is:

$$P_{F,af} = \frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{B^3}{(1-P_{sh})^2}\frac{(S-W_F)}{CS}\rho_{s,Al}$$

3.4.6 Resistance loss: Emitter and airside busbars

The resistance loss in the both busbar regions is largely dependant on the distance between the edges of the cell and the external contact leads. By considering the geometry of the busbars in the interdigitated scheme in figure 3.15, it should become apparent that the resistance losses along the busbars to their corresponding external contact leads is independent of the finger geometry and emitter shadow fraction - i.e. it is the equivalent case to that of the 'H' cell design derived in section 3.2.4.

It follows that the resistive power loss along the busbars to the external contact can be derived using either the classical unit cell approach derived earlier in section 3.2.4, or by using flow current.

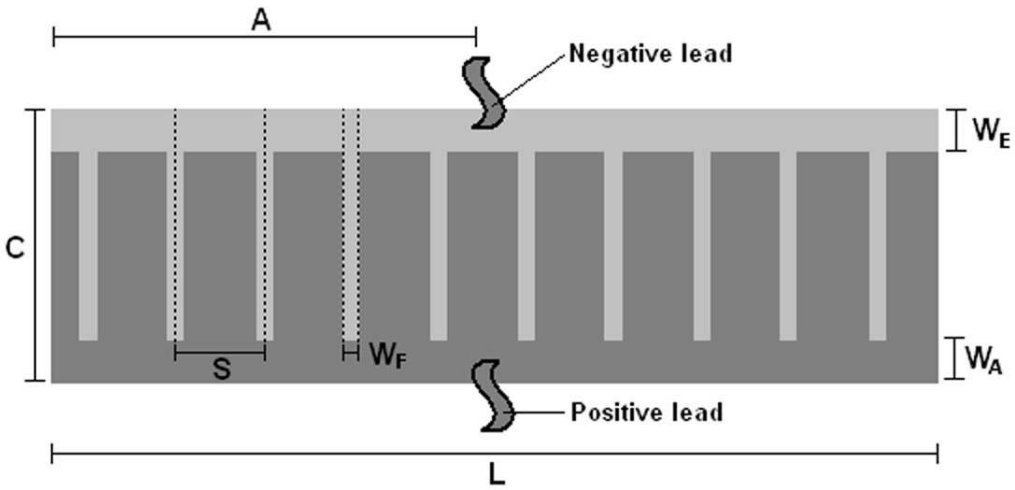


Figure 3.15: A schematic of an interdigitated thin-film cell, showing the emitter (top) and airside (bottom) busbars, with their corresponding external contact leads.

The only modification required from the classical unit cell approach is the replacement of the finger length, B, with the cell width, C. After doing so, the resistance loss of the emitter busbar is now:

$$P_{L,eb} = \frac{1}{3} A^3 J_{MP}^2 C^2 \frac{\rho_{s,eb}}{W_E},$$

By utilising the divided current density, the resistive power loss of the emitter busbar on a unit cell of area AC is found to be:

$$P_{L,eb} = \frac{1}{3} \frac{\rho_{s,eb}}{W_E} A^3 J_F^2 \left(B + W_A - \frac{BW_F}{S} \right)^2,$$

which can be shown to be equivalent to that found by the classical unit cell approach by substituting the equation defining the flow current from section 3.4.2.

Whilst both equations are equivalent, the former, simplified power loss equation containing the maximum power-point current density will be used in further analysis. The fractional power loss, for the unit cell area AC is thus:

$$\begin{aligned} P_{F,eb} =& \frac{P_{L,eb}}{J_{MP}V_{MP}AC} \\ =& \frac{1}{3}A^2\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,eb}}{W_E} \end{aligned}$$

The analog case is true for the airside busbar with the relevant busbar-width value changed:

$$P_{L,ab} = \frac{1}{3}A^3 J_{MP}^2 C^2 \frac{\rho_{s,ab}}{W_A},$$

for the resistive power loss, and

$$P_{F,eb} = \frac{1}{3}A^2\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,ab}}{W_A}$$

for the fractional power loss.

It is important to note that the emitter busbar parameters are not necessarily equal to those of the airside busbar - if the busbars are formed during separate stages in the metallisation, the thickness (and thus sheet resistivity) may vary, and due to the shadow loss that accompanies the emitter features, in optimised cells the emitter busbar will generally be of smaller width than that of the airside busbar.

For the case where the busbars are of equal thickness and width $(W_A =$

W_E), the total resistive power loss (and thus fractional power loss) due to each of the busbars are equal, as expected.

3.4.7 A note on tapered features

Tapered features - those with a gradual decrease in finger or busbar width from one end to the other, are one method to reduce the resistive power loss whilst keeping the shadow loss constant. Figure 3.16 shows an example schematic of linearly tapered emitter finger in a unit cell of dimensions SC.

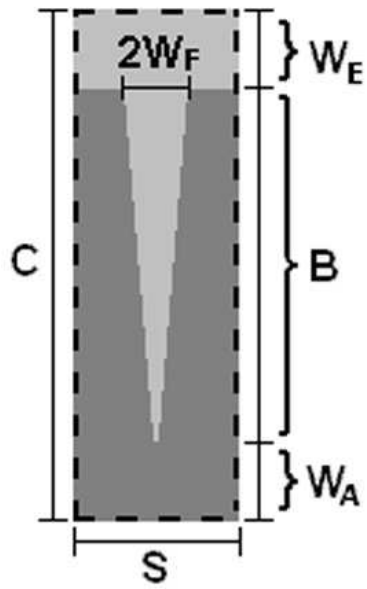


Figure 3.16: A schematic showing the a linearly tapered finger within a unit cell. The width of finger at it's junction with the emitter busbar has been defined as distance $2W_F$.

As expected, the derivation of the resistive power loss of tapered features is similar to that as features of uniform width. Consider the tapered finger shown in figure 3.16, the only difference between this case and that

of fingers of uniform width (section 3.4.6) is the resistance differential, dR.

For the case of the uniformly tapered emitter finger, this value is $dR = \frac{B}{2W_F x}\rho_{s,Al}dx$.

Using this value for dR, and the previously attained value for current, $I = J_F x(S - W_F) + J_F(SW_A)$, the power loss, and fractional power loss for linearly tapered emitter fingers can be found:

$$\begin{aligned}
dP_{L,ef} =& I^2 \frac{B\rho_{s,Al}}{2W_F x}dx \\
=& \left[J_F x(S - W_F) + J_F SW_A\right]^2 \frac{B\rho_{s,Al}}{2W_F x}dx \\
P_{L,ef} =& \int_0^B \left[J_F x(S - W_F) + J_F SW_A\right]^2 \frac{B\rho_{s,Al}}{2W_F x}dx \\
=& \int_0^B \left[\frac{J_F^2 Bx\rho_{s,Al}}{2W_F}(S - W_F)^2\right]dx + \int_0^B \frac{J_F^2 B\rho_{s,Al}}{2W_F x}(SW_A)^2 dx \\
=& \frac{1}{4}\frac{J_F^2 B^3\rho_{s,Al}}{W_F}(S - W_F)^2 + \frac{1}{2}\frac{J_F^2 Bln(B)\rho_{s,Al}}{W_F}(SW_A)^2 \\
=& \frac{1}{2}\frac{J_F^2 B\rho_{s,Al}}{W_F}\left[\frac{1}{2}B^2(S - W_F)^2 + ln(B)(SW_A)^2\right]
\end{aligned}$$

As the unit cell area is CS, the total power out of the unit cell under maximum power point conditions is given by $J_{MP}V_{MP}CS$, and the fractional power loss for tapered emitter fingers is:

$$
\begin{aligned}
P_{F,ef} =& \frac{1}{2}\frac{J_F^2 B\rho_{s,Al}}{J_{MP}V_{MP}CSW_F}\left[\frac{1}{2}B^2(S-W_F)^2 + ln(B)(SW_A)^2\right] \\
=& \frac{1}{2}\frac{J_{MP}}{V_{MP}}\frac{1}{(1-P_{sh})^2}\frac{B}{CS}\frac{\rho_{s,Al}}{W_F}\left[\frac{B^2}{2}(S-W_F)^2 + ln(B)(SW_A)^2\right]
\end{aligned}
$$

Which closely resembles the case for the emitter finger of uniform width.

As for busbars of uniform width, tapered busbars are not dependant on the geometry outside the busbar area, and therefore the same formulation as for the classical unit-cell approach may be used.

For the busbars, a different resistance differential also needs to be used to take the tapered geometry into account. This is given by $dR = \frac{A}{2W_B y}\rho_{s,bb}dy$, where A is the distance from the edge of the cell to the current collection point (see figure 3.15), and W_B is the average width of the relevant busbar - as both emitter and airside busbars follow this formulation.

The full derivation won't be given, however it can be found that for a unit cell of dimensions AC, the current at any point along the busbar is given by $J_{MP}Cy$. Using this and the resistance differential for tapered busbars, the sum of the resistive power loss is:

$$
\begin{aligned}
P_{L,bb} =& \int_0^A (J_{MP}Cy)^2\frac{A}{2W_B y}\rho_{s,bb}dy \\
=& \frac{1}{4}A^3 J_{MP}^2 C^2\frac{\rho_{s,bb}}{W_B}
\end{aligned}
$$

and the fractional power loss is given by:

$$P_{F,bb} = \frac{1}{4} A^2 C \frac{J_{MP}}{V_{MP}} \frac{\rho_{s,bb}}{W_B}$$

It is interesting to note that the power loss for the tapered busbar is equivalent to that of the uniform-width busbar, apart from the constant coefficient, which is $\frac{1}{3}$ in the case of a busbar of uniform width.

3.4.8 Resistance loss: Contact resistance

For standard solar cells with large area contacts, contact resistance can generally be neglected [53], particularly at one sun intensities. However, for metallisations with plasma-etched sidewalls, introduced in section 3.4.1, the contact resistance between the emitter layer and Al emitter finger electrode is not necessarily negligible. This is due to the 'line-contact' style of contact that may be present between the emitter finger and the exposed emitter layer. The specifics of the sidewall contact area of the emitter are discussed in detail in section 4.3. In general, a contact width (E) of ~100 nm is sufficient for the power loss modelling here where interdigitated metallisations are concerned. This value, apart from being a realistic contact area, is large enough for the contact resistance to have an influence on the power loss calculation.

When quantifying the power loss due to contact resistance in this side-

wall region, the power loss is

$$P_{L,ec} = \rho_c J_F^2 \frac{(S - W_F)^2 B}{2E},$$

which is based on an approximation given by Green [35] and has been modified for interdigitated metallisations. ρ_c is the specific contact resistance (of units Ωcm^2) and E is the width of the contact between the emitter layer of the solar cell and the Al emitter finger. For a unit cell of CS following from the fractional power loss can be given as

$$P_{F,ec} = \frac{J_{MP}}{V_{MP}} \frac{\rho_c}{(1 - P_{sh})^2} \frac{(S - W_F)^2}{2E} \frac{B}{CS}$$

3.4.9 Shadow loss: Emitter busbar and fingers

Shadow losses result from light hitting the emitter finger and busbar features instead of entering the silicon film. The total fractional power loss is simply the fractional coverage area of the emitter fingers $(P_{F,sf})$ and busbar $(P_{F,sb})$ together, and are individually given by:

$$P_{F,sf} = \frac{BW_F}{CS}$$

for the emitter fingers, and

$$P_{F,sb} = \frac{W_E}{C}$$

for the emitter busbar.

3.4.10 Summary of losses

Table 3.2 shows a summary of the power losses associated with interdigitated thin-film metallisations, as well as the corresponding unit cell area associated with each loss mechanism. The meaning behind each of the variables used can be found in the subsections of 3.4 pertaining to the relevant loss mechanism.

Table 3.2: Summary of key resistive and shadow power losses associated with an interdigitated thin-film solar cell metallisation. The definitions of the variables are found under the various subsections corresponding to each power loss, found in section 3.4. Note that for tapered features, each of the coefficients of $\frac{1}{3}$ are reduced to $\frac{1}{4}$.

Loss type and location	Power loss	Unit cell area
Emitter layer, resistive loss	$\frac{1}{6}J_F^2\rho_{s,em}\left[\frac{1}{4}(S-W_F)^3B+W_A^3S\right]$	$\frac{CS}{2}$
Emitter fingers, resistive loss	$J_F^2B\frac{\rho_{s,Al}}{W_F}\left[\frac{1}{3}B^2(S-W_F)^2+(SW_A)^2\right]$	CS
Airside fingers, resistive loss	$\frac{1}{3}B^3J_F^2(S-W_F)\rho_{s,Al}$	CS
Emitter busbar, resistive loss	$\frac{1}{3}A^3J_{MP}^2C^2\frac{\rho_{s,eb}}{W_E}$	AC
Airside busbar, resistive loss	$\frac{1}{3}A^3J_{MP}^2C^2\frac{\rho_{s,eb}}{W_A}$	AC
Emitter contact, resistive loss	$\rho_cJ_F^2\frac{(S-W_F)^2}{2E}\frac{B}{CS}$	CS
Emitter fingers, shadow loss	$J_{MP}V_{MP}BW_F$	CS
Emitter busbar, shadow loss	$J_{MP}V_{MP}AW_E$	AC

Table 3.3 shows a summary of the fractional power losses (i.e. power losses normalised to unit area). It is these discrete formulae which allow for the optimisation of the grid pattern for interdigitated metallisations,

via the minimisation of the sum of fractional power losses, which will be investigated in the next section.

Table 3.3: Summary of key resistive and shadow fractional (percentage) power losses associated with an interdigitated thin-film solar cell metallisation. The definitions of the variables are found under the various subsections corresponding to each power loss, found in section 3.4. Note that for tapered features, each of the coefficients of $\frac{1}{3}$ are reduced to $\frac{1}{4}$.

Location and loss type	Fractional power loss
Emitter layer, resistive loss	$\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{1}{(1-P_{sh})^2}\frac{\rho_{s,em}}{CS}\left[\frac{1}{4}(S-W_F)^3B+W_A^3S\right]$
Emitter fingers, resistive loss	$\frac{J_{MP}}{V_{MP}}\frac{1}{(1-P_{sh})^2}\frac{B}{CS}\frac{\rho_{s,Al}}{W_F}\left[\frac{B^2}{3}(S-W_F)^2+(SW_A)^2\right]$
Airside fingers, resistive loss	$\frac{1}{3}\frac{J_{MP}}{V_{MP}}\frac{B^3}{(1-P_{sh})^2}\frac{(S-W_F)}{CS}\rho_{s,Al}$
Emitter busbar, resistive loss	$\frac{1}{3}A^2C\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,eb}}{W_E}$
Airside busbar, resistive loss	$\frac{1}{3}A^2C\frac{J_{MP}}{V_{MP}}\frac{\rho_{s,ab}}{W_A}$
Emitter contact, resistive loss	$\frac{J_{MP}}{V_{MP}}\frac{\rho_c}{(1-P_{sh})^2}\frac{(S-W_F)^2B}{2E}$
Emitter fingers, shadow loss	$\frac{BW_F}{CS}$
Emitter busbar, shadow loss	$\frac{W_E}{C}$

The concept of flow current, example derivation, and summary tables have been published in [54], where the effect of emitter finger width (W_F) and cell area (product of CS) on total fractional power loss is also investigated.

3.5 Optimisation

3.5.1 Introduction

Optimising the cell layout is vital step in producing higher efficiencies for all types of photovoltaic devices. The most straightforward method to perform optimisation of the cell parameters is to use numerical software; one example is by utilising the Goal Seek/Solver functions of Microsoft Excel software package and setting the sum of the fractional power losses to a minimum. In using this approach, and all other optimisation approaches, technical restrictions need to be placed on parameters such as the emitter resistivity (limited by doping density) and finger width (limited by screen-printing, or lithography resolution), for example.

As with the classical unit cell approach in section 3.2.7, the method of minimising the sum of the fractional power losses via the method of calculus may be used to optimise the various cell parameters. However, due to the large number of interdependencies within the fractional power loss formulas for the interdigitated thin-film metallisation, discrete, elegant solutions do not exist for most relevant cell variables required to be optimised.

Discrete solutions may however be generated, provided simplifications to the relevant fractional power losses are introduced. The following example allows for the discrete solution for the optimal emitter finger width, provided the finger spacing is sufficiently larger than the finger width.

3.5.2 Emitter finger optimisation

Consider the case where the centre-to-centre finger spacing is constant, and considerably larger than the emitter finger width (i.e. $S \gg W_F$), which, for reasonable values of emitter resistivity, may generally be regarded as true. In this scheme, power loss equations that involve $(S - W_F)$ simply reduce to S, and the $\frac{-BW_F}{S}$ terms found in emitter and airside busbar power losses formulae drop out.

Thus, provided the finger spacing is markedly greater than the emitter finger width, the only remaining power loss mechanisms that are a function of the emitter finger width are the resistive loss and shadow loss of the emitter fingers. This allows for an elegant analytical solution to be found.

The derivation involving the method of calculus is done as follows: the sum of fractional power losses resulting from the emitter fingers, taking into account the above approximations, is:

$$\sum P_{F,f} = \frac{J_F^2}{J_{MP}V_{MP}} \frac{BS}{C} \frac{\rho_{s,Al}}{W_F} \left[\frac{B^2}{3} + W_A^2 \right] + \frac{BW_F}{CS}$$

To determine the optimal finger width, W_F, the sum of the fractional power losses is then differentiated with respect to the emitter finger width,

set to equal zero, and solved for the finger width:

$$\begin{aligned}
\frac{d}{dW_F}\left(\sum P_{F,ef}\right) &= -\frac{J_F^2}{J_{MP}V_{MP}}\frac{BS}{C}\frac{\rho_{s,Al}}{W_F^2}\left[\frac{B^2}{3}+W_A^2\right]+\frac{B}{CS} \\
0 &= -\frac{J_F^2}{J_{MP}V_{MP}}\frac{BS}{C}\frac{\rho_{s,Al}}{W_F^2}\left[\frac{B^2}{3}+W_A^2\right]+\frac{B}{CS} \\
\frac{B}{CS} &= \frac{J_F^2}{J_{MP}V_{MP}}\frac{BS}{C}\frac{\rho_{s,Al}}{W_F^2}\left[\frac{B^2}{3}+W_A^2\right] \\
W_F^2 &= \frac{J_F^2}{J_{MP}V_{MP}}S^2\rho_{s,Al}\left[\frac{B^2}{3}+W_A^2\right] \\
W_F &= S\sqrt{\frac{J_F^2}{J_{MP}V_{MP}}\rho_{s,Al}\left[\frac{B^2}{3}+W_A^2\right]}
\end{aligned}$$

The fact that the finger width, W_F, above, is only optimal for a given (constant) finger length, B, and airside busbar width, W_A, limits the usefulness of analytical solutions generated in this matter. Ideally, optimal values are to be found via simultaneous consideration of all parameters, which is explained in the next section.

3.5.3 Numerical optimisation

Numerical optimisation involves setting up a system of simultaneous equations and an objective function to be minimised or maximised, subject to a set of constraints on the problem variables, expressed as equalities and inequalities [55]. For this and all further optimisation work carried out in this thesis, the Solver tool from the Microsoft Excel software package will be used, although other more complex software can be used, following the same general method:

- All quantified fractional power losses from table 4.9, and the variable parameters (finger width, W_F, etc.) are inserted into a spreadsheet, matrix, or equivalent.
- A total fractional power losses value is found by summing the individual loss components.
- The total fractional power loss value is set to a minimum by changing the cell's variable parameters, subject to various constraints.
- Constrains are required to be selected based on a number of factors: I) Material constants. Parameters which cannot be altered, for example an emitter layer resistivity confined to 400 $\Omega/\square$. II) Technical limitations. A minimum emitter busbar width, W_E greater than 1000 μm to facilitate cell-characterisation, for instance). III) The interdigitated geometry. For instance, finger spacing S must be greater than emitter finger width W_F.

Examples of using the above methodology to design grid patterns optimised for interdigitated thin-film cells, and interconnected mini-modules are given in sections 4.6 and 6.3, respectively.

3.6 Chapter summary

In this chapter, a review of the unit-cell approach for determining power losses commonly found in literature is given. As the power loss formulas found in this manner are tailored to tradition screen-printed wafer cells,

they are not suited for applying to thin-film on glass devices. This is owing to simplifications used in the derivations, the unique emitter-on-glass nature of the poly-Si thin-film on glass technology, and the interdigitated metallisation pattern containing two parallel busbars of differing polarity - only one of which contributes to shadow losses.

Interdigitated-finger style metallisations are introduced and a summary of the advantages, and eventual use for the metallisation of thin-film photovoltaic devices on glass is given. The concept of flow current is developed, which eliminates one of the main causes of inaccuracy when using the unit-cell approach. Derivations and formulas for the power losses and fractional power losses for interdigitated thin-film metallisations, using the unit-cell approach in combination with the flow current concept are developed. Power loss formulas combining these two aspects allow for a more accurate method to determine the power losses of existing thin-film poly-Si solar cells, as well as for optimising the interdigitated grid pattern for future cells, based on technical and material constraints.

Chapter 4

Cell metallisation

"Whether from clay or from metal, it is in the nature of us to make our own monsters."

– *Sarar Connor*, Terminator: TSCC, s. 1, ep. 4, final scene.

4.1 Introduction

In the previous chapter, the power losses of interdigitated metallisation were discussed and formulated. In section 4.2, the self-aligned metallisation scheme and procedure used to form these interdigitated cells is introduced. The remainder of the chapter aims to expand on other aspects of the scheme: the main cause of variation in metallised devices, post-metallisation thermal treatments, and metallisation of high-rate absorber devices. This is followed by an application of the power loss analysis from the previous chapter.

The formation of the sidewall has proven to be the most critical aspect that influences the final device characteristics of metallised cells. Section 4.3 investigates the sidewall formation as a function of etching time by both optical microscopy and cross-sectional focused-ion beam (FIB) images.

Focus then shifts to the effect of thermal annealing on metallised devices (section 4.4) on both cell voltage and efficiency. Section 4.5 applies the self-aligned metallisation scheme to PECVD devices with absorbers deposited at a considerably higher rate than standard PECVD.

Finally, section 4.6 uses the power loss analysis from chapter 3 to optimise photomasks (i.e. grid patterns) for interdigitated devices, in a step by step process.

4.2 Overview: Self-aligned metallisation

4.2.1 Introduction

As mentioned in section 2.2, the polycrystalline silicon diodes of interest in this thesis result from the solid-phase crystallisation (SPC) of amorphous silicon deposited onto a textured glass substrate by plasma-enhanced chemical vapour deposition. A rapid thermal annealing (RTA) follows, for 30 seconds at 1000 °C, and then the samples undergo hydrogenation at 600 °C for 30 minutes in a hydrogen plasma.

The diode on glass structure, together with typical doping levels and film thicknesses of a crystallised PECV-deposited diode is shown in figure 4.1. Here, the glass is used as a superstrate: light enters the glass first before being absorbed by the solar cell. In the figure, the glass/n^+ emitter interface is shown as being planar (flat), however the glass side of this interface may also be textured to enhance the light trapping capabilities of the device. Textured glass superstates used in this thesis are formed by aluminium-induced texturisation (AIT) [49, 56] and a distinction is made when samples are on either planar or textured glass superstrates.

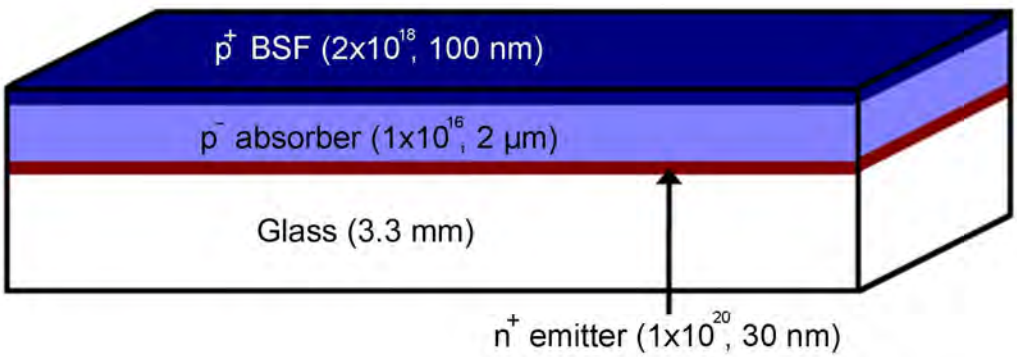


Figure 4.1: The poly-Si thin-film diode stack, consisting of an emitter, absorber and back surface field (BSF). Typical doping levels and thickness of each layer are shown. Glass is used as a superstrate, where light enters the glass first before being absorbed in the cell. The figure is not to scale.

Metallisation, by definition, involves the addition of metal contacts to the diode. Due to the structure of the diodes: the emitter/absorber/BSF stack on a glass superstrate, unique metallisation schemes can be developed. It should also be noted that due to the high lateral conductivity of polycrystalline material, cells can be metallised without any transparent conducting oxide (TCO), one area where the metallisation of poly-Si on

glass material differs from other thin-film technologies.

In this section, the core parts of the self-aligned, interdigitated scheme for metallising material deposited by PECVD, previously developed by researchers at the University of NSW [48, 49, 50] is outlined.

4.2.2 Metallisation sequence

Figure 4.2 shows a step-by-step schematic of the standard, self-aligned metallisation process which begins after hydrogenation of the diode. A brief description of the process is as follows, where the roman numerals represent the corresponding step in the figure:

1) (Optional step, for increased current) Form a SiO_2 back surface reflector that contains point-contact holes (I)

2) Blanket-deposition of the airside Al electrode

3) Lithography step to define locations of emitter-side fingers and busbars (II)

4) Phosphoric (III) and plasma (IV) etches to form the emitter features

5) Blanket-deposition of the emitter-side Al electrode (V)

6) Lift-off to remove the remaining resist layer and Al (VI)

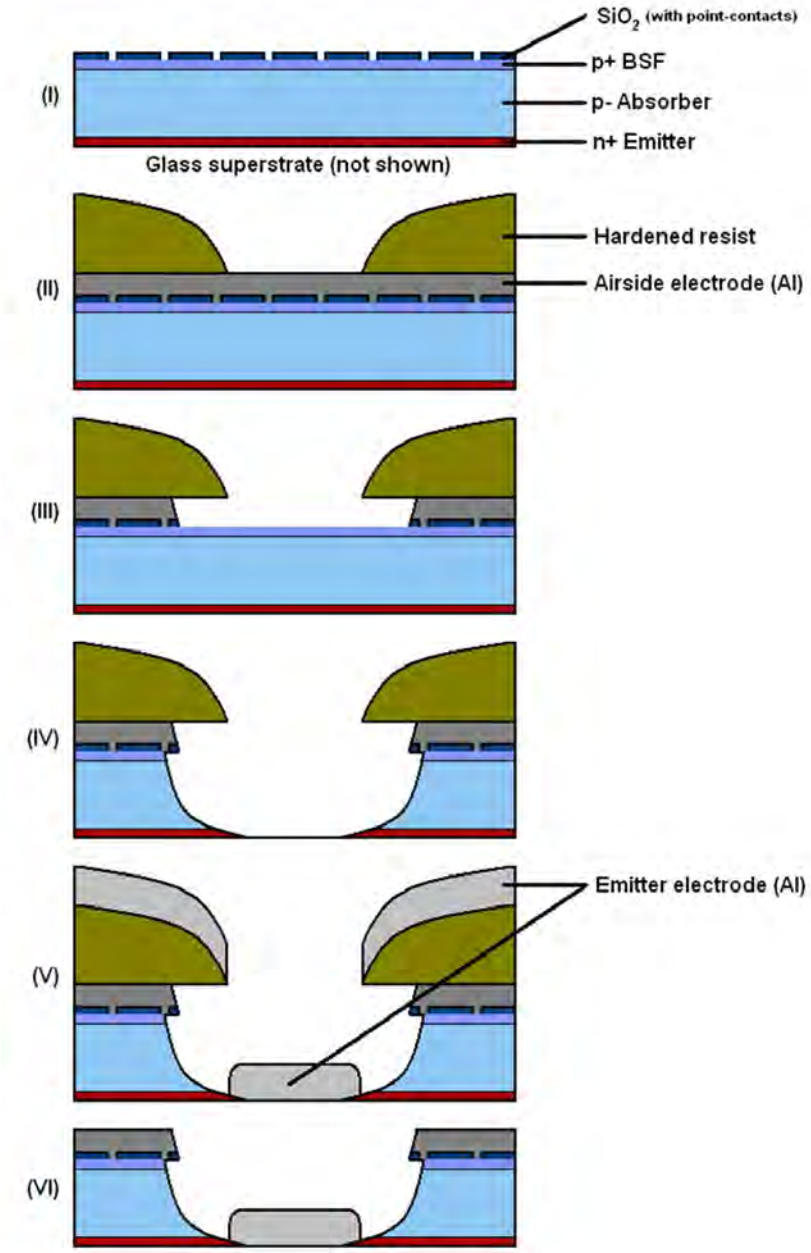


Figure 4.2: A schematic of the standard metallisation sequence for diodes deposited by PECVD, focused on a single emitter finger. The glass superstrate and any texture of the glass surface/poly-Si emitter interface is not shown for simplicity. (I): The stack structure after forming point-contact holes in the SiO_2 film. (II): An Al film is deposited and emitter feature locations are patterned in the resist. (III): Exposed airside Al and underlying SiO_2 is removed. (IV): A plasma etch removes absorber material to expose the glass and emitter. (V): A second Al film is deposited. (VI): Lift-off is used to remove the photoresist and excess emitter Al, revealing the final device structure.

4.2.3 Sample preparation

To begin with, the sample undergoes a piranha etch (1:1 H_2SO_4: H_2O_2) for upwards of 10 minutes to remove any organic residue from the sample surface . The sample then undergoes a dip in hydrofluoric acid solution (4.9% HF, 'HF-dip') until the sample surface is hydrophobic, to remove any surface oxides. This generally takes between 45 and 90 seconds.

The sample is then rinsed for 5 minutes under de-ionised (DI) water. The next step is dependant on whether or not a back surface reflector (BSR) is desired, which is used to increase the light trapping capabilities of the device, and thus increase cell current.

4.2.4 Silicon dioxide back surface reflector

This optional step consists of depositing a thin-film of SiO_2, usually by sputtering. The SiO_2 film (refractive index ~1.46 at 500 nm wavelength) acts as a BSR and thus is required for samples where high current, high efficiency devices are desired.

To maximise the reflectance properties the thickness is intended to be approximately 120 nm and is perceived as a royal blue colour [57]. The SiO_2 is then patterned to form contact holes which allows for a contact path between the p^+ BSF of the diode and the airside Al layer. This is achieved via a lithography process using a photomask containing circular openings, although an alternate approach based on inkjet printing could also be used [58]. Table 4.1 shows the relevant parameters involved. For this

process, Microposit (Shipley) S1818 positive photoresist is used together with Microposit MF-312 developer. An in-house built LED array is used as the UV-source for the exposure step.

Table 4.1: Typical process parameters used in the lithography step during metallisation. Microposit S1818 resist, together with MF-312 developer is used.

Quantity of photoresist	1.5 - 2 mL
Initial spinner speed	500 RPM
Ramp up time	15 s
Final spinner speed	1500 RPM
Soft bake	15 m @ 90° C
Exposure time	440 s
Development time	75 s
Hard bake	20 m @ 120° C

Post-development, the sample is slowly dipped 3x in DI water to remove any excess developer solution, and then dried with a nitrogen gun. The sample is then hard baked for 20 minutes at 120° C to increase the photoresist's adhesion for the following wet etch. After the hard bake, the sample undergoes a HF dip to remove the exposed SiO_2 point contact holes.

The resist is then removed by placing the sample in an acetone solution, followed by cleaning in isopropanol. The sample is then rinsed under DI water for 5 minutes.

4.2.5 Patterned electrode formation

An Al film acting as the airside metallisation features is then blanket-deposited on the sample via thermal evaporation. Lithography, using the

parameters and procedure in table 4.1, is then used to define the location of the emitter features.

A wet etch in phosphoric acid (42.5% H_3PO_4), heated on a hot-plate to ~65°C is used, with the hardened photoresist acting as an etching mask, to remove the airside Al where emitter features are desired. The sample is kept submerged until the Al is no longer visible in the emitter finger and busbar grooves, and an additional ~40 seconds of etching time is added to ensure the Al is slightly over-etched.

If a SiO_2 BSR film is incorporated in the cell structure, a brief HF dip is used to remove the film and reveal the p^+ airside poly-Si layer. If no intra-cell back surface reflector scheme is being used, then the airside poly-Si will already be exposed after the above lithography step.

The exposed poly-Si is then removed via a plasma (dry) etch in a 13.56 MHz parallel-plate plasma etcher, using SF_6 as the etchant gas. Once the absorber layer is removed, glass, in the middle of the etched groove, and highly doped emitter, at the base of the sidewalls is then exposed. Another HF dip is used, until the sample is hydrophobic. This facilitates the formation of the ohmic contact for the exposed poly-Si emitter and the emitter electrode.

A second Al evaporation takes place, contacting the exposed poly-Si emitter film at the bottom of the U-shaped sidewalls. The photoresist and Al film which has been deposited on top is then removed via a lift-off step: the sample is submerged in a beaker of acetone and placed in an ultrasonic bath until all photoresist is stripped off. The sample is then cleaned

by isopropanol and then rinsed in DI water.

Figure 4.3 shows digital photos of a thin-film poly-Si sample after metallisation using the self-aligned interdigitated scheme. Four cells are seen on the sample, each of which is 4 x 1.1 cm^2 in area.

The photos are taken from a) the airside and b) through the glass superstrate. In figure 4.3 a), the light grey areas correspond to emitter Al features and the dark grey areas, the airside Al features. This colour convention is the same as used throughout the interdigitated power loss sections in chapter 3. In b), the poly-Si material is purple, and the emitter features are shown in grey.

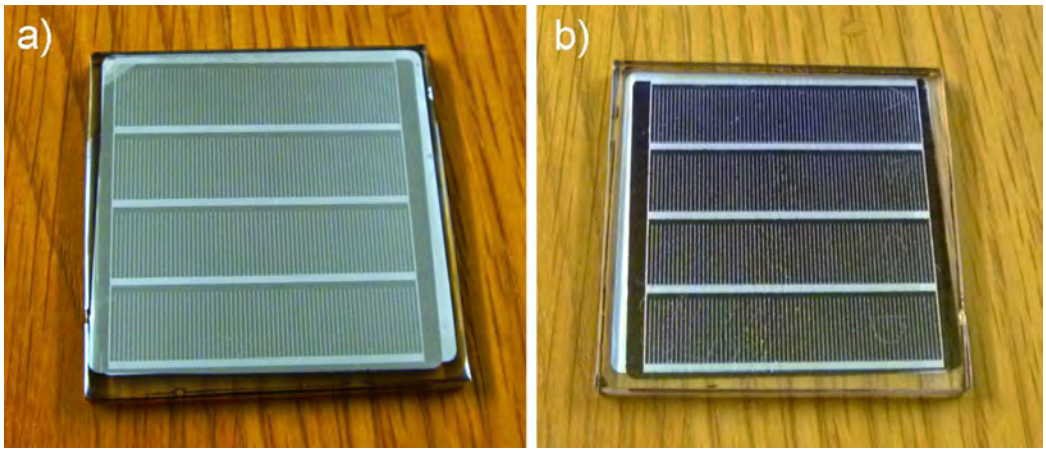


Figure 4.3: Digital phtotos of a 5 x 5 cm thin-film poly-Si sample metallised using the self-aligned interdigitated scheme. The image shows four cells, each 4 cm by 1.1 cm. a) From the airside, showing the emitter features (lighter grey) and the airside features (darker grey) - the same colour convention as used in chapter 3. b) Through the glass superstrate. The poly-Si is the dark purple area and emitter features are grey.

4.3 Sidewall profile: Effect of plasma etch

4.3.1 Introduction and motivation

The plasma etch step is the main cause of discrepancy between final devices metallised by the self-aligned method described in section 4.2. This is due to the large variability of etching depths in individual metallisation runs caused by; (i) Non-uniformities in plasma etching; (ii) The high dependence on user experience and; (iii) Thickness variations of the crystallised poly-Si films.

The etching depth achieved from plasma etching affects the sidewall profile, and ultimately, the final fill factor and degree of series and shunt resistance present in the final metallised cell. In this section, the influence of plasma etch time on the sidewall profile will be investigated.

The focused-ion beam (FIB) image in figure 4.4, taken from top-down perspective, shows the effect of over-etching on the sidewall-emitter electrode interface. In this region, the poly-Si sidewall has been over-etched such that it can no longer be contacted by the evaporated Al emitter electrode. The presence of glass indicates there is no continuous contact between the emitter electrode and n^+ emitter layer of the sidewall in these areas. The white circled area shows a localised 'point-contact' between the emitter electrode and the n^+ poly-Si film, suggesting this particular sample will suffer from high series resistance.

The contrary case is true - should the evaporated Al emitter film overlap across the p-n junction, a clear shunt path is created. The severity

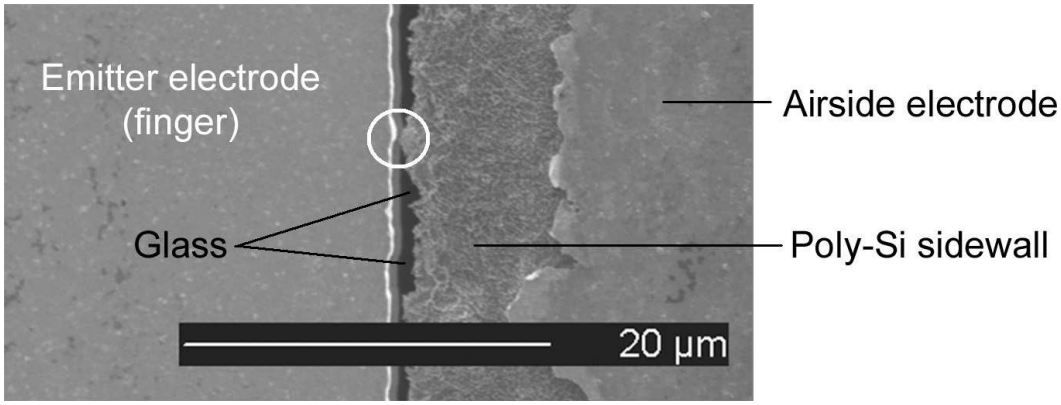


Figure 4.4: An FIB image taken from the top-down (i.e. 0 ° tilt angle) of an emitter electrode-poly-Si sidewall interface after lift-off of the photoresist. The visible glass areas (black) indicate that the sidewall has been overetched no contact is made between the Al emitter electrode and the emitter silicon film in these areas. The circled area shows the location of a localised point-contact between the emitter electrode and the sidewall.

of the shunting depends on the doping densities of the poly-Si emitter and absorber films, the junction location, and the extent that the emitter electrode overlaps the junction.

For most of the diodes investigated in this thesis, the p-n junction is located less than 50 nm from the glass surface, and therefore particular care needs to be taken to prevent the junction being shunted by the evaporated Al emitter electrode. This sections aims to increase understanding of the sidewall etching profile with increasing etch time, as well as determine if the sidewall profile can be understood, or even predicted, by non-destructive (optical microscopy) means.

4.3.2 Method

A 5 x 5 cm^2 sample on planar glass, metallised using the self-aligned method previously discussed, is fabricated up until the plasma etching step (image III in figure 4.2), and then physically separated into eight smaller cells.

One of the samples is removed prior to plasma etching to act as a baseline sample. The remaining 7 samples are placed in a plasma etcher and etched for 3 minutes, after which one sample (sample 1, exposed to 3 minutes of etching) is removed. The remaining samples are etched again for 3 minutes and another sample (sample 2, 6 m etch) removed. This is repeated until the last sample (sample 7, 21 m etch) has been etched. Table 4.2 shows the process gas and typical parameters for the plasma etching process.

Table 4.2: Typical process parameters used in the plasma (dry) etch step. The system incorporates a horizontally aligned parallel-plate setup and the sample sits on the lower electrode.

Processing gas	SF_6
RF Frequency	13.56 MHz
Evacuated pressure	< 2.5 Pa
Processing pressure	40 Pa
Power	80 W

Each 3 minute etch consists of four smaller etches of 45 s duration each, with the orientation of the samples rotated 90° between these 45 s etches. This is done to mitigate the effect of any non-uniformities present in the plasma etching system caused by irregular gas flow or localised variations of voltage within the camber.

After the plasma etching step is complete, optical microscope (reflectance mode) images are taken of the emitter groove of each sample after having been etched for its respective time. The magnification used for the images is 50x.

This is particularly relevant as viewing the sample under an optical microscope at various stages of plasma etching is carried out during the metallisation of real devices. This is the prime method for the user to determine whether to continue or stop etching, depending on the appearance of the poly-Si film (or lack thereof) under an optical microscope.

An Al film is then evaporated on to the samples, as in the standard self-aligned metallisation, and cross-sectional focused-ion beam (FIB) images are then taken to view the sidewall profile of the poly-Si film. The FIB images are taken after milling a trench into the device and tilting the sample to ~45 °, to capture a cross-section across the milled area.

Of particular interest is the shape of the plasma-etched poly-Si sidewall and the contact area the emitter electrode makes with the sidewall.

The reason the Al film is evaporated onto the cell prior to FIB imaging is twofold; (i) The Al evaporation step is the next step in the metallisation process, so the FIB images are a representation of the true device structure at this stage in the metallisation, and (ii) The Al film protects the photoresist from the high energy gallium ions (Ga+) used, which would otherwise etch the photoresist very quickly.

4.3.3 Results

Figure 4.5 a) shows an optical microscope image of an emitter finger (width ~30 μm) of the baseline (no plasma etching) sample, together with b) an FIB image of the same sample after evaporation of an Al film (the emitter electrode). The optical microscope image is equivalent to stage (III) of figure 4.2 - prior to any plasma etching.

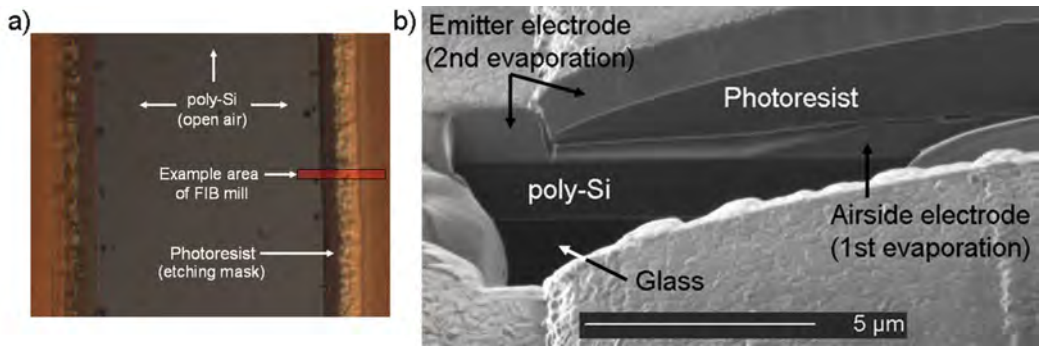


Figure 4.5: a) Optical microscope (reflectance) image of an emitter finger of the baseline (no plasma etching) sample. The width of the finger is ~30 μm and the red-shaded area is the approximate area of the b) FIB cross-section (tilt angle ~45 °) of the same sample at the emitter finger sidewall. The image has been taken after evaporation of the Al emitter electrode.

In the self-aligned metallisation process, the photoresist layer in figure 4.5 b), together with any emitter electrode that lies on top of it is removed using lift-off as the last stage (i.e. acts as a sacrificial layer). The result is an interdigitated pattern with the emitter and airside electrodes taking up the majority of the surface of the cell area.

Figure 4.6 shows the optical microscope (reflectance mode) images of emitter finger after increasing plasma etch times, together with FIB cross sections of the same samples after an Al film (emitter electrode) has been

evaporated onto the sample.

Here, the left-side optical microscope images represent stage (IV) in figure 4.2 - with different amounts of poly-Si material removed from the plasma etch process. The right-side FIB images represent the corresponding cross section of the same areas after evaporation of the Al emitter electrode - stage (V) of figure 4.2.

4.3.4 Discussion: Images

Figure 4.5 shows the optical microscope profile of the baseline sample prior to any plasma etching. The surface of the poly-Si is smooth, as is expected for a sample on a planar glass superstrate.

In figure 4.6 the progressive stages of plasma etching and it's effect on the sidewall profile can be distinguished. In figure 4.6 a), after 3 minutes of etching, a light texture begins to form on the poly-Si, indicating the material has begun to be preferentially etched away. The extent of the etching after this time can be seen in the corresponding FIB image, where the beginning of a small dip from the isotropic plasma etch process can be seen.

In figure 4.6 b), c) and d) (6, 9 and 12 minutes of etching), the texture of the poly-Si film as seen through the optical microscope becomes more prominent with increasing etch time.

Figure 4.6 d) is the first FIB cross-section of particular interest. Although it depends strongly on the exact location of the p-n junction, it is sidewall

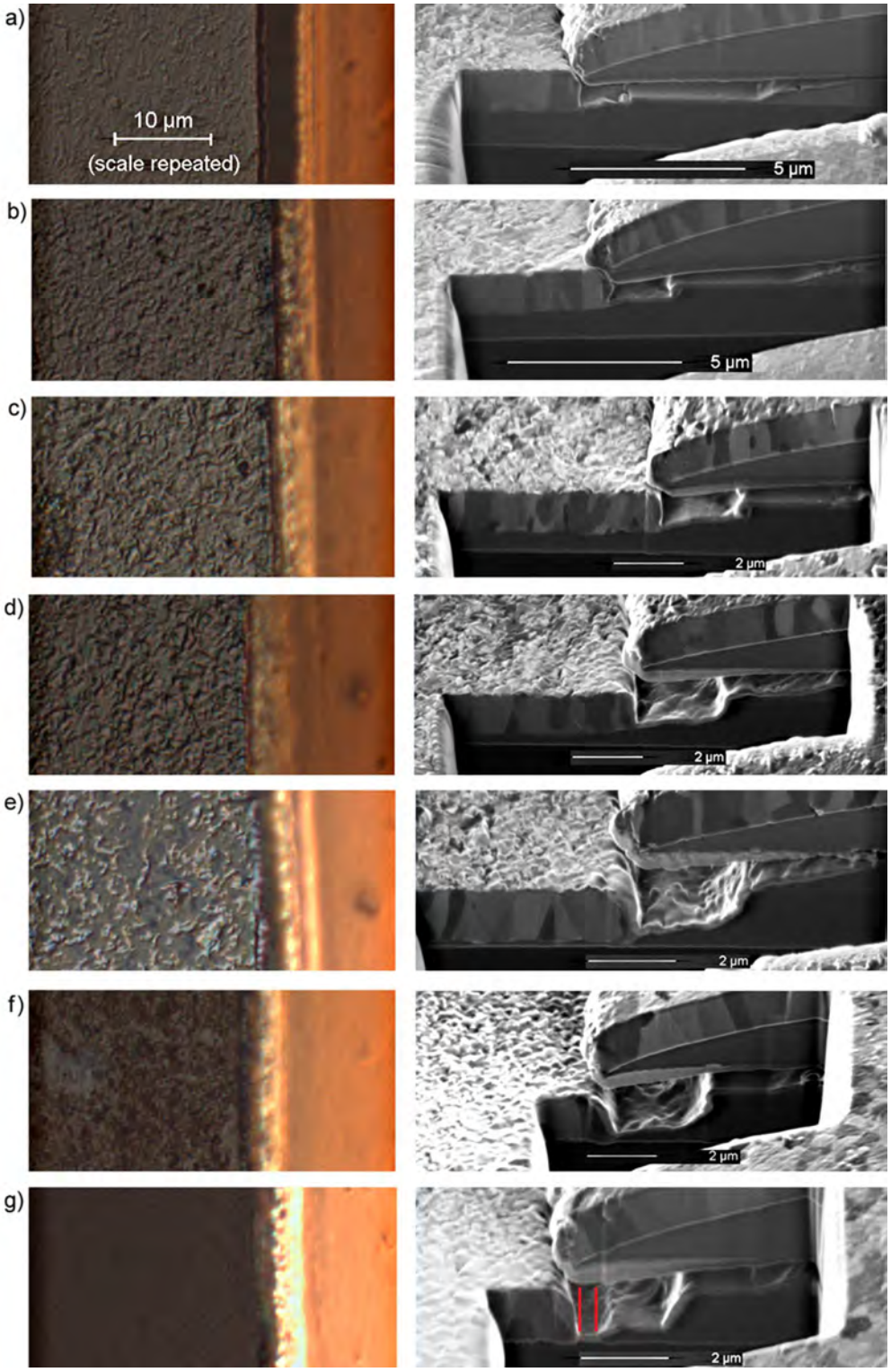


Figure 4.6: Optical microscope (reflectance, left side) and FIB cross sections after emitter Al evaporation (right side) after increasing plasma etching times: a) 3 minutes, b) 6 minutes, c) 9 minutes, d) 12 minutes, e) 15 minutes, f) 18 minutes and g) 21 minutes. The labelling of the FIB images is the same as in figure 4.5 and has not been repeated for clarity.

profiles such as this that are a major cause of shunting in cells metallised using the self-aligned scheme. For a cell with glass-side junction, this sidewall profile would be considered under-etched, and result in a very poor voltage when characterising the final device. The magnitude of the shunting depends on the junction location and local doping densities of the poly-Si material.

The left-side optical microscope image of figure 4.6 e) (15 minute etch time) is notable in that glass - the darker of the two grey shades, is visible for the first time. The corresponding FIB image shows a continuous film of n^+ emitter poly-Si material under the evaporated emitter electrode. The author believes sidewall profiles such as this, with a large contact area between the glass-side poly-Si emitter and the evaporated Al emitter electrode, are most conducive to high FF devices.

The key issue with this declaration however, is that the 'patchy' remnants of emitter poly-Si seen in the optical microscope image are only present for a short fraction of the etching time. Obtaining such an etched emitter film consistently over large (i.e. a few square centimetres) areas is difficult to achieve due to the aforementioned plasma etcher and poly-Si thickness non-uniformity issues. While it is possible to perform multiple, short (~30 second) etches to ensure the desired amount of emitter poly-Si is left remaining in the groove, time constraints from pumping down the chamber reduce the feasibility of this option.

After etching for 18 minutes, shown in figure 4.6 f), only glass is present in the emitter groove of the optical microscope image and the corresponding FIB image shows a line-style contact being made by the Al emitter

electrode along the poly-Si emitter. Such a contact does not result in shunting of the junction, but a higher series resistance is present in devices with this sidewall profile than that found in e), although contacts such as this have still found to produce reasonable devices. This is due to the smaller, yet still intact contact area between the Al emitter electrode and the n^+ poly-Si emitter layer.

In figure 4.6 g), again only glass is shown in the emitter groove of the optical microscope image. In the FIB cross-sectional image, no contact is made between the Al and the poly-Si sidewall. The white film coating the sidewall and adhering to the bottom of the photoresist layer is debris from the milling process. The approximate gap width is shown by the red lines. If no contact at all is made between the emitter electrode and the sidewall, the device will not measure any voltage after metallisation. In the case of multiple small-area point-contacts (e.g. in figure 4.4), the device will have a high series resistance, which in particularly poorly metallised samples will manifest as a severe reduction in output current.

4.3.5 Discussion: Relevance to metallisation

For practical purposes note that the exact individual etching times required for a sample depends on both the thickness of the poly-Si film and the etching times used by the operator - eight separate 45 second etches, for example, will produce a different level of etching than one six minute etch. This makes standardising the etching process difficult.

Procedures such as “for a 2 micron film, etch for 18 minutes” are not

useful since the 18 minutes has to be broken up into multiple shorter etches to combat variations in both the plasma etching profile and poly-Si film uniformity. The shorter etches are used to both rotate and relocate the samples within the chamber to achieve a desired etching profile, and to inspect the current level of etching and mask (for example with scrap pieces of silicon wafer) areas where etching is complete.

The optical microscope and FIB images in figure 4.6 should therefore only be used as a *relative* guide on the difference ~3 minutes of plasma etch time has on the sidewall profile, and not an *absolute* guide on the sidewall profile after (e.g.) 18 minutes of etching time.

From the figure it is clear that there is a trade-off from the plasma etching process. Under-etching the poly-Si leads to shunting of the junction once the Al emitter electrode is deposited. Whilst over-etching of the poly-Si results in high series resistances, or in the case of extreme over-etching, no functioning device at all.

From a metallisation standpoint, how does one go about plasma etching for high FF devices? Some recommendations based on the traits of the plasma etcher used in this investigation and from analysing figure 4.6 are:

- The etch rate is on the order of 110 $\pm$30 nm/min. For time management purposes the operator should aim to remove ~60 % of the cell material using either 2 etches (rotating the sample by 180 ° in between etches) or 4 etches (rotating by 90 °).

- If there is still a blanket film of poly-Si visible in the emitter groove, continue etching for ~1 - 2 minutes, and at most 3 minutes, repeating as necessary.

- The operator should aim for the 'patchy' poly-Si emitter on glass shown in the optical microscope image of figure 4.6 e). As soon as this is present the area should be masked to protect it from further etching, for instance with a piece of silicon wafer.

- Due to the short time period the patchy emitter will be present, chances are it may be already etched away when viewed by the operator (i.e. only glass will be visible in the emitter groove). In this case, the area should be masked immediately.

- As there is a relatively long (~3 minute) window of time between figures e) and f), plasma etching the poly-Si all the way to the glass still results in quite reasonable device performance provided the sidewall has not been over-etched too much beyond that seen in f).

4.3.6 Summary

The most critical aspect of the self-aligned metallisation scheme, the sidewall formation, is systematically investigated as a function of plasma etching time.

Viewing the sample under an optical microscope between etches gives valuable hints as to the status of the sidewall formation. Recommendations are given for plasma etching during the metallisation process and in

summary these are; (i) The operator should aim for a mixture of poly-Si emitter and glass to be visible in the emitter groove when viewed through an optical microscope, and mask this area if present; and (ii) If only glass is visible in the emitter groove, the area should be masked immediately before further etching.

Reasonable Al emitter electrode/n^+emitter layer contacts, and therefore final devices, can still be made even when no emitter film is visible under an optical microscope.

4.4 Improvement from thermal annealing

4.4.1 Review and motivation

This section investigates the effect of thermal annealing on the voltage and efficiency of completely metallised PECVD poly-Si solar cells on glass. The relevant areas are the Al/n^+ poly-Si contact in the emitter groove, and the Al/p^+ poly-Si contact that forms the rear side electrode. Shi [59] has previously investigated the effect of contact annealing on the evaporated Al/BSF p^+ layer, and Al/plasma-etched n^+ emitter layer interfaces of hydrogenated (un-metallised) diodes. Here, we expand Shi's work on the device characteristics of *metallised* cells after thermal annealing.

In Shi's investigation, a PECV-deposited diode undergoes pre-metallisation treatments (crystallisation, RTA and hydrogenation) and was cleaned in a similar manner as in section 4.2, with a piranha clean, a dip in 5% HF

and then rinsed under DI water for 10 minutes. After evaporating a film of Al, the samples are sequentially baked up to 300 °C and contact resistance measured by transmission line measurements (TLM, [60, 61]). It was found that the Al/p^+ poly-Si contact is non-ohmic in it's as-deposited state. The contact remained non-ohmic after an anneal for 30 minutes at 150 °C, whilst further anneals at 200 °C, 250 °C and 300 °C produced improvements in contact resistance from 2.8 x 10^{-2} Ωcm^2, to 5.3 x 10^{-3} Ωcm^2, to 1.8 x 10^{-3} Ωcm^2, respectively.

For similarly cleaned samples that did not undergo any hydrogenation treatments, the Al/p^+ poly-Si contact on the rear surface exhibited an ohmic and homogeneous contact with an as-deposited contact resistance of ~1.0 x 10^{-4} Ωcm^2. This is attributed to; (i) A dopant density reduction on the surface from the hydrogen, which acts as a dopant neutraliser and; (ii) Surface damage from the harsh hydrogen-plasma conditions [62].

In investigating the Al/n^+ poly-Si contact interface, Shi found that after plasma etching to expose the n^+ emitter film, the as-deposited contact was already ohmic. Noting that the plasma etch process is largely a chemical process, not a physical process, and hence is not subject to as much surface damage as for the hydrogenation process on the p^+ BSF layer. Additionally, since the emitter film is buried under the 2+ μm thick absorber, it is not subject to damage from hydrogenation. The effect of thermal annealing on the Al/n^+ poly-Si contact found no significant improvement and results were not published.

At higher temperatures (20 m at 450 °C), contact resistance was found to increase [63], likely due to an alteration of the surface charge distri-

bution. For metallised, post-hydrogenated poly-Si devices, however, such high temperatures are unlikely to be encountered since cell degradation has been reported by thermal anneals as low as 300 °C, in what is effectively a de-hydrogenation process [64, 65].

This section aims to expand on Shi's work and investigate the effect of thermal annealing on V_{OC} and efficiency of completely metallised devices, where the net effect from both contact resistance, and the de-hydrogenation phenomenon can be analysed.

4.4.2 Method and measurement

The pre-metallisation cell fabrication steps for the devices studied here are carried out by a former student in the Thin-Film Group, Guangyao Jin. The PECV-deposited amorphous films undergo SPC for 18 hours at 600 °C, RTA for 1 minute at 1000 °C, and hydrogenation for 30 minutes at ~600 °C, using a plasma power of 3000 W.

The doping concentration and thickness of the cell structure is given in table 4.3. Metallisation, following the self-aligned procedure outlined in section 4.2 is conducted, and no silicon dioxide rear reflector is used, so that the full Al/p^+ BSF contact is present.

The size of each individual cell used is 4.4 cm^2. The I-V data, including V_{OC} and efficiency of the cells is measured after metallisation (no anneal), and then after each successive anneal, after the sample has cooled to room temperature. The data are measured on a computerised I-V testing apparatus under simulated one sun, air mass 1.5 (AM 1.5) radiation.

Table 4.3: Cell-stack structure for the cells used in the thermal anneal, including doping concentrations where relevant, together with thicknesses for each layer.

Layer	Doping concentation	Thickness
Glass (Schott Borofloat 33)	n/a	3 mm
SiN	n/a	~70 nm
n^+ poly-Si emitter	~1 x 10^{20}	30 nm
p^- poly-Si absorber	~1 x 10^{16}	2000 nm
p^+ poly-Si BSF	~2 x 10^{18}	100 nm

The apparatus uses a reference cell measured at the National Renewable Energy Laboratory in the USA. The anneals are carried out sequentially for 30 minutes at 150 °C, 200 °C, and 250 °C in a N_2-purged oven.

Ideally to get a better understanding of the nature of the contacts investigated here, an accurate contact resistance determination model would be used instead of, or in addition to the I-V based approach used here. The most accurate and simple is via transmission line measurements (TLM) [60], where parallel contact bars are positioned on the device and the I-V data between various parallel bars are measured and plotted. The total resistance is equal to the resistance of the semiconductor itself plus double the metal-semiconductor (contact) resistance. The fitted curve is then extended beyond the data to a spacing distance of 0 and contact resistance quantified in this manner. This approach could not be used in this investigated as the photomasks previously developed, and used to produce the cells here did not contain such TLM structures. With regards to emitter contact resistance, the emitter fingers (~30 μm wide) present on the interdigitated cell pattern could be used to approximate a 'ladder' TLM strucutre, however these are too narrow to be properly probed and

characterised.

The author attempted to use Suns-Voc measurements at high illumination densities, where information of the metal-semiconductor contact properties can be found by the location of a reversal point (i.e. decreasing voltage with increasing illumination [66]) on the Suns-Voc curve. However, the highest illumination density attainable was on the order of ~4 suns and no device measured was poor enough for a reversal point to be found. It is espected that illumination densities of >25 suns are required to characterise devices in this matter.

4.4.3 Results and discussion

Figure 4.7 shows the V_{OC} at one sun as measured by the I-V apparatus before, and at various stages of the sequential annealing process. Cell C was damaged whilst measuring the I-V curve after the anneal at 250 °C and a meaningful datum could not be recorded.

It can be seen that annealing at 150 °C improves the V_{OC} on the order of ~10 mV. The anneal at 200 °C has a further positive, but minimal effect on the cells' voltage, whilst cell voltage begins to decline after further annealing for 30 minutes at 250 °C.

The increase in open-circuit voltage resulting from annealing up to 200 °C can be attributed to the increasing penetration depth of the airside Al electrode deeper in to the p^+ poly-Si film as a function of increasing anneal temperature.

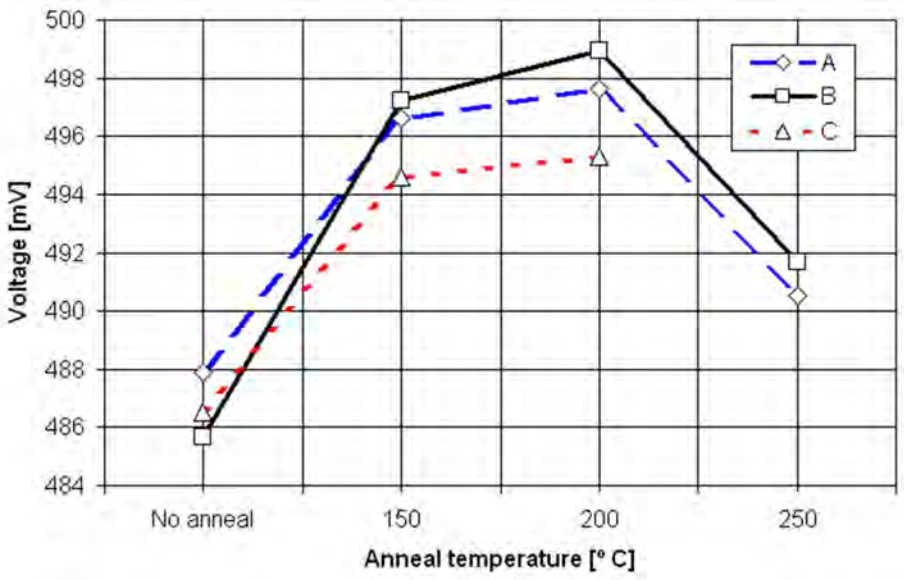


Figure 4.7: The I-V measured V_{OC} of metallised poly-Si on glass cells before, and after sequential 30 minute anneals at increasing temperature. The cells was allowed to cool to room temperature before I-V data were measured. Cell C was damaged while attempting to obtain the post-250 °C anneal measurement and no meaningful datum could be recorded.

Note that during metallisation, this Al/p^+ poly-Si contact undergoes a 'mini-anneal' for 20 minutes at 120 °C during the hard-bake stage of the lithography process prior to the deposition of the emitter Al electrode. It follows that some of the contact improvement annealing up to 120 °C has already been factored in at the conclusion of metallisation, but before sequential annealing begins.

The effect on voltage is explained by the concept of a Schottky barrier contact which acts in series, but in reverse polarity to the cell's p-n junction. Schottky barriers and their presence in metal-semiconductor interfaces has been well studied in the literature [67, 68] and a well-written introduction to the topic of metal-semiconductor contacts is found in Sze [69].

The hydrogenation-induced surface damage on BSF-side poly-Si layer results in a poorer contact between the p^+ poly-Si and the evaporated Al.

For the doping levels found in the p^+ poly-Si layers of the samples used, thermionic-field emission is the dominant transport mechanism for current through the Schottky barrier. As a result of hydrogenation, defects can extend to a depth of 20 - 30 nm under the silicon surface [70]. This combines with the known dopant passivation properties of hydrogen to increase the barrier height, and thus the rectifying effect of the barrier. With increasing thermal anneal temperatures it is thought the Al electrode film locally spikes further through this damaged surface, resulting in a better contact.

The decline in voltage that becomes apparent after the anneal at 250 °C could be attributed to a combination of two effects:

(I) The Schottky barrier at the Al/n^+ poly-Si interface. Due to the high doping present at this interface (~1 x 10^{20}), the barrier width is thin enough for field emission (pure tunnelling) to be the dominant transport mechanism. With increasing anneal temperatures, Al acts as a p-type dopant source within silicon [71, 72], effectively reducing the donor concentration at the surface and widening the barrier width.

(II) The de-hydrogenation phenomenon as discussed in section 4.4.1, although it's relative importance compared to Schottky effects may be quite low at anneal temperatures under 300 - 350 °C.

Irrespective of the effect of annealing on voltage, the effect on efficiency is the true figure of merit for determining an appropriate optimal anneal

temperature for metallised PECV-deposited thin-film solar cells. Figure 4.8 shows the I-V measured one-sun efficiency before, and at various stages of the sequential annealing process. In samples A and C, only a small improvement in efficiency is noted between the 150 and 200 °C anneals, as the bulk of their improvement in efficiency came from the 150°C anneal. The opposite is true for sample B, where the 200 °C anneal resulted in the largest increase in cell efficiency.

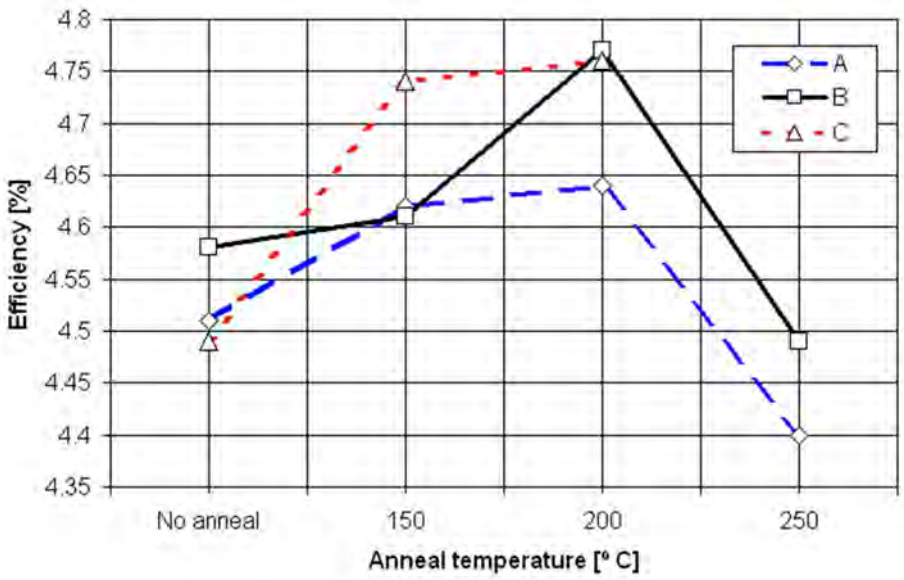


Figure 4.8: The I-V measured one-sun efficiency of metallised poly-Si on glass cells before, and after sequential 30 minute anneals at increasing temperature. The cells were allowed to cool to room temperature before I-V data were measured. Cell C was damaged while attempting to obtain the post-250 °C anneal measurement and no meaningful datum could be recorded.

For both cells A and B, the peak efficiency came after the 200 °C anneal and a sharp drop, beyond the pre-anneal efficiency was present after anneal at 250 °C. Cell C's efficiency could not be measured as it was damaged during the attempt at measurement.

The reason efficiency does not exactly match the gains from V_{OC} in figure 4.7, is that efficiency is ideally a function of not only cell voltage but current and fill factor as well. Taking it one step further, fill factor is a function of parasitic resistances - series and shunt resistance. The fact that the efficiency decreases considerably more than the voltage after the 250 °C anneal (relative to the increase from previous anneals) indicates that the effect of either series or shunt resistance has contributed enough to decrease cell efficiency - even lower than the initial 'no anneal' efficiency.

The optimal thermal anneal for metallised PECV-deposited material is thus found to be 30 minutes at 200 °C, where both the highest V_{OC} and cell efficiencies were found. This is in contrast to e-beam evaporated polycrystalline silicon thin-films, where the greatest increases in voltage and efficiency occur when baked at 250 °C [73, 74].

4.4.4 Summary

Improvements in both one-sun V_{OC} and cell efficiency are realised by thermally annealing cells in a N_2-purged after the metallisation process. This is attributed to the Schottky barrier found at the interface of metal-semiconductor contacts that is well modelled by the literature. The increase and subsequent decrease in cell voltage and efficiency is due to; (i) The surface damage on the p^+ BSF layer caused by the hydrogenation process and; (ii) The different way p-type and n-type polycrystalline silicon material behaves in the presence of an intimate Al contact when annealed.

The optimal post-metallisation thermal anneal temperature for PECV-deposited thin-film material is found to be 200 °C for both device voltage and efficiency. At a higher anneal temperature of 250 °C, voltage and efficiency are found to start degrading, the later of which is reduced below the starting 'no anneal' value, do to a larger influence of parasitic resistances.

4.5 Metallisation of high-rate PECVD material

4.5.1 Introduction

The low deposition rate (~30 nm/min) of the amorphous precursor diode has long been one of the major drawbacks for PECVD material, particularly in the attempt for thin-film solar cell commercialisation [75] - attributed to lower throughput and higher costs. E-beam evaporation [76], capable of deposition rates of 300+ nm/min, and hot-wire CVD (600 nm/min or greater) [77] have been studied increasingly in recent years as an alternative.

Cracks and pinholes through the film have been reported with e-beam evaporation technology when used in combination with textured glass surfaces for solar cell applications [78], due to it's 'line of sight' nature of deposition. While for hot-wire CVD, high nucleation rates have been reported [77], resulting in small grain sizes after crystallisation of the

amorphous film, and no efficiency results for crystallised films have as yet been reported.

High-rate deposition of amorphous silicon films suitable for the fabrication of crystallised poly-Si thin-film cells may also be achieved using PECVD by regulating the deposition pressure and/or RF power [79]. It is noted that most of the research into high-rate PECVD material has been for P-I-N amorphous solar cells and liquid crystal displays, where heavy restrictions are placed on processing parameters such as process temperature due to the substrate used in these technologies. Therefore there is considerable scope for the application of high-rate amorphous PECVD material for thin-film poly-Si solar cell applications, where the amorphous film is deposited on high-temperature Borofloat Glass (BSG) superstrates and then crystallised.

Jin [80] provides an excellent introduction and summary of the fundamentals of high-rate PECVD in the context of thin-film poly-Si cells. In this section, the metallisation of diodes containing a high-rate PECVD absorber (p^- poly-Si layer) is investigated.

4.5.2 Method

Diode fabrication consists of the PECV-deposition of an n^+ emitter (a mixture of pure silane and phosphine in silane) at standard rate (25 nm/min), a p^- absorber (diborane in hydrogen) at **high-rate** (~220 nm/min) and a p^+ back-surface field (diborane in hydrogen) at standard rate (25 nm/min). The high-rate absorber film is deposited in the same conventional 13.56

MHz PECVD, but in a separate chamber to that of the heavily doped n^+ and p^+ films.

An RF power of 100 W, chamber pressure of 0.8 Torr and substrate temperature of 400 °C is used for the deposition of the high-rate absorber film. The post-deposition procedure is similar to that outlined for standard-rate cells in section 2.2: SPC (600 °C for 18 hours), RTA (1100 °C for ~60 s in an N_2 ambient) and hydrogenation (glass temperature ~610 °C for 30 m, plasma power 3500 W). The final cell-stack structure, including doping densities and deposition rates is given in table 4.4.

Table 4.4: Cell-stack structure, including doping density and deposition rate for the high-rate PECVD cell under investigation

Layer	Doping concentation and rate	Thickness
Glass (Schott Borofloat 33)	n/a	3 mm
SiN	n/a	~70 nm
n^+ poly-Si emitter	~1.5 x 10^{20}, 25 nm/min	~25 nm
p^- poly-Si absorber	~1.2 x 10^{16}, 220 nm/min	~2075 nm
p^+ poly-Si BSF	~2.0 x 10^{18}, 25 nm/min	~100 nm

Two metallisation processes are carried out on high-rate absorber material. One metallisation is done on planar glass, without the use of an SiO_2 BSR, and another is done on textured glass using a SiO_2 BSR, to investigate whether high-rate absorber material is compatible with both textured glass and the point-contacted BSR scheme.

Metallisation of the planar, non-SiO_2 BSR is done in accordance with the self-aligned procedure outlined in section 4.2. The thermally evaporated airside Al electrode is ~973 nm thick. The phosphoric etch time is 440 seconds and the exposed poly-Si is removed by plasma etching for a total

etch time of 18 minutes and 30 seconds. The emitter Al film is ~1.675 μm thick.

On the other, glass-textured sample, a SiO_2 film (section 4.2.4) with thickness ~ 120 nm is deposited by PECVD prior to metallisation and contact holes are formed using photolithography. The airside Al electrode thickness for this sample is ~1.330 μm. The phosphoric etch time is 490 seconds, and total plasma etch time is 19 minutes. The emitter Al electrode for this sample is ~1.685 μm thick.

Each sample consists of four cells, each of 4.4 cm^2 in area. Light I-V measurements are then taken on each of the cells at the conclusion of the metallisation process. The I-V data is measured using an in-house built system using approximated 1.5 AM spectrum calibrated with a reference cell measured at the National Renewable Energy Laboratory, USA. All series resistances given in this thesis are calculated by comparing two I-V curves each measured at different light intensities, i.e. $R_S = \frac{\Delta V}{\Delta I_{SC}}$, where ΔJ_{SC} is the difference in short-circuit currents between the two I-V curves measured at different light intensities [81, 82]. The shunt resistance values are given by the inverse of the slope of the I-V curve around the short-circuit current point (V = 0 mV).

4.5.3 Results

The I-V results from the planar sample, without any SiO_2 BSR are shown in table 4.5. Cells are apertured to 4.4 cm^2 using a black flock and the glass-superstate temperature is ~25 °C during measurement.

The results show a remarkable uniformity with regards to voltage across the four cells - indicating the high-rate absorber has not affected the film quality across the sample. The short-circuit current density of ~13.5 mA/cm^2 is somewhat low, even for a planar glass sample without additional light-trapping features. It's believed this is due to the RTA parameters used which were not optimised at the time. This resulted in a higher than desired doping level in the absorber film and resulted in a reduced response in the blue end of the spectrum. This phenomenon was detected on samples deposited with both standard-rate and high-rate absorber films, and thus is not unique to films deposited at faster rates.

The high fill factors of over 72 %, and in one case almost 73 % are among the highest seen in metallised thin-film devices at UNSW. This shows that the high-rate absorber material is conducive to both low series resistance and high shunt resistance devices.

Table 4.5: I-V results for metallised cells with a high-rate absorber. The cells are on planar glass without a SiO_2 BSR. Cells are apertured to 4.4 cm^2 and the glass temperature was ~25 °C during measurement.

Parameter	Cell A	Cell B	Cell C	Cell D
V_{OC} [mV]	487.15	485.25	482.95	479.06
J_{SC} [mA/cm^2]	13.56	13.45	13.65	13.88
FF [%]	72.46	72.63	72.96	71.21
Efficiency [%]	4.79	4.74	4.81	4.74
R_S [Ωcm^2]	1.83	1.65	1.63	1.93
R_{SH}[Ω]	3318.67	2411.68	3644.44	1800.94
Glass temp. [°C]	24.75	25.27	24.98	25.21

Figure 4.9 shows a one-sun I-V curve for cell C, the device with the highest measured fill factor. The shunt resistance is measured to be ~3645 Ω, providing a negligible decrease to the cell's fill factor. Almost all of the

cell's decrease in fill factor is due to series resistance - which is typically the dominant loss mechanism for the self-aligned metallisation scheme described in 4.2.

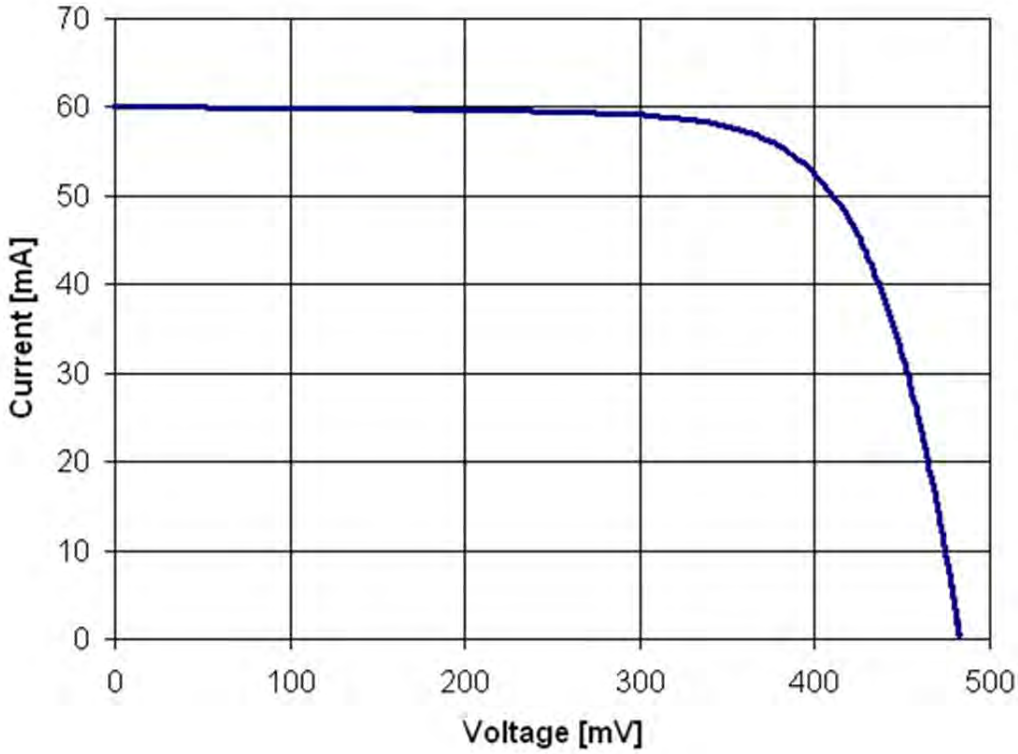


Figure 4.9: 1-sun (AM 1.5 spectrum) I-V curve of the planar cell C, without SiO_2 BSR. The fill factor of this device is 72.96 %. The cell is apertured to an area of 4.4 cm^2 and the glass superstrate temperature is 24.98 °C during measurement.

The I-V results of two cells from the high-rate material deposited on a AIT-glass superstrate and with a SiO_2 BSR are shown in table 4.6. Only the highest efficiency and highest fill factor results are shown.

As with the samples on planar glass, the short circuit current density of these samples is lower than what would be expected with both a textured glass superstrate and an SiO_2 BSR. The reason for this is likely

Table 4.6: I-V results for metallised cells with a high-rate absorber. The cells are on AIT (textured) glass with a SiO_2 BSR. Cells are apertured to 4.4 cm^2 and glass temperature is ~25°C during measurement.

Parameter	Cell B	Cell C
V_{OC} [mV]	490.15	490.17
J_{SC} [mA/cm^2]	17.92	17.17
FF [%]	67.12	69.12
Efficiency [%]	5.90	5.82
R_S [Ωcm^2]	2.50	2.06
R_{SH}[Ω]	685.84	1103.01
Glass temp. [°C]	24.60	24.14

due to the RTA process that was in use at the time, which caused curved and dipped glass surfaces resulting in poor photolithography resolution. This affected the size and density of point-contact holes within the SiO_2 film, causing them to be larger than desired in some areas of the film, and completely vacant in other areas of the film. In addition, the resultant emitter fingers are larger than the photomask fingers due to the additional light entering between the curved glass surface and the photomask. The current difference in these neighbouring cells (> 4%) show the effect the non-uniformities in point-contact size and density have on cell current over a relatively small area of two adjacent cells.

The previously mentioned problems relating to dopant diffusion, also resulting from the RTA process are suspected to be present. A master's student, Fei Lu, investigated the influence of RTA time and temperature and confirmed that a shifting (increase) of the peak EQE wavelength, movement of the junction location towards the air-side of the diode, and in some cases a complete inversion of the absorber to n-type were occurring with an increase in RTA temperature [83].

The shunt resistance is measured the same as for the planar cell, and found to be ~610 Ω for cell B and ~775 Ω for cell C. Although smaller than that of devices on planar superstrates, series resistance is still the dominant mechanism causing a reduction in fill factor. The open-circuit voltage of these devices, however, remains high and is comparable to devices with absorbers deposited at standard-rate.

These results are the first ever for metallised high-rate PECVD SPC poly-Si thin-film solar cells deposited on textured glass and are published in [84], and submitted for publication in [85].

4.5.4 Summary

Using a high-rate absorber, the voltage of metallised cells of between 480 and 490 mV across 5 x 5 cm^2 samples are comparable with cells fabricated with standard-rate devices and show that there is no material fault in the high-rate absorber film to restrict device performance.

The voltage difference across the device area of different cells again is comparable with standard-rate devices, and may even be less variable than standard-rate devices. The fill factors of high-rate devices are among the highest produced for poly-Si thin-film cells on glass, indicating the material allows for high shunt, low series resistance devices.

The current densities of the cells on both planar and textures superstrates are lower than expected and this is thought to be due to the RTA process, which caused the phosphorous-doped emitter layer to transition

towards the airside of the devices, affecting both the doping level of the absorber and the junction location.

The RTA process also causes the glass superstrate to curve upwards towards the edges of the glass, distorting the lithography resolution of both the SiO_2 point-contacts and the emitter finger and busbar features. It's believed this is due to non-optimised RTA parameters and not a result of the high-rate absorber film.

The high one-sun voltages and I-V results of metallised cells on both planar and textured glass superstrates show that one of the main disadvantages of PECVD as a deposition method can be overcome by using a conventional PECVD by increasing RF power and gas pressure. High-rate absorbers on high-temperature glass superstrates for thin-film poly-Si are a promising area for the push towards commercialisation and the author believes they merit further research.

4.6 Interdigitated cells: Design and optimisation

4.6.1 Introduction

In this section, the procedure to design a new photomask for the fabrication of higher efficiency thin-film devices is explained from start to finish, including defining the material and technical limitations to formulate the final mask design. The section is designed to be a guide for

future researchers interested in, or carrying out the process for optimising new cell designs. Where thought to be necessary, justifications and explanations for selections are given.

To facilitate future investigations of BSRs, two different masks are developed. One mask for cells with, and one for cells without a point-contacted SiO_2 BSR scheme as detailed in section 4.2.4.

The approach used is based on the formulations and results found for interdigitated metallisations in chapter 3, and the specific optimisation approach used is the numerical method outlined in section 4.7. Using this approach, material constants, technical constraints, and geometrical limitations from the interdigitated layout are factored, and the optimal mask design is then calculated using the Microsoft Excel Solver function.

4.6.2 Material constants

To begin with, constants need to be determined related to the cell material, metal electrode material and cell output under maximum power point conditions, which are inserted into the spreadsheet formulas and used to determine the optimal mask parameters.

Firstly, the cell's maximum power point values are estimated. This results from the fact that, using the unit-cell approach for optimisation, a mask design can only be optimal for a cell with a certain pre-determined V_{MP} and maximum power point current density (J_{MP}). A photomask mask optimally designed for a cell with a V_{MP} of 350 mV and a J_{MP} of 15 mA/cm^2

will not be optimal for a cell with a $V_{MP}$of 400 mV and a J_{MP} of 25 mA/cm^2. It should be noted, however, that if all other parameters are optimised, then a device will not suffer terribly from any incorrect maximum power point parameters being used.

The maximum power point values are therefore selected somewhat arbitrarily. Previous high efficiency, high FF thin-film poly-Si devices fabricated in the thin-film group at UNSW have a maximum power point voltage (V_{MP}) of between 380 and 390 mV. Since high efficient devices are desired from the new mask design, a V_{MP} of 400mV is selected, being slightly higher than previously fabricated devices to factor in both increased material quality, and the expected reduced series resistance as a result of a new, optimised photomask design.

A similar increase in J_{MP} is also warranted; this is due once again to better material quality, advances in light trapping (textured glass surfaces, for instance), and the reduction in shading losses resulting from the newly optimised photomasks. Here, two different mask designs will be investigated, one designed for use without a BSR, and one incorporating a BSR. The J_{MP} for the cell designed for use without a BSR has been increased by ~16 % over the previous high J_{MP} of ~15.5 mA/cm^2, to 18 mA/cm^2 . It should be noted that almost half of this gain in current can be attributed to an expected reduction in shading losses resulting from the optimised photomask design.

The J_{MP} for the cell designed with the use of a BSR is selected to be 25 mA/cm^2, which corresponds to the J_{MP} of a thin-film (~2.5 μm) cell with

very strong light trapping and high (>70 %) fill factor, of which a short-circuit current density (J_{SC}) of ~30 mA/cm^2 could be expected.

The contact resistance, ρ_c for the Al emitter electrode/n^+ poly-Si contact is assumed to be 1 x 10^{-4} Ωcm^2. The sheet resistivity of the Al electrode contacts is defined as the resistivity of Al film divided by the thickness. Al electrode films can routinely be deposited via thermal evaporation (Varian evaporator) to a thickness of 1.5 μm. Taking 2.8 x 10^{-8} Ωm as the resistivity of Al at room temperature, the sheet resistivity, $\rho_{s,Al}$ is thus approximated as $\frac{2.8x10^{-8}\Omega m}{1.5x10^{-6}m} \approx 0.0187\ \Omega/\square$.

The sheet resistivity of the emitter layer is inversely dependant on the emitter thickness, phosphorous doping density, and electron mobility. For the case of non-uniformly doped emitter films, as can be expected in post-RTA PECVD material, the sheet resistivity can be determined via a four-point probe system. The sheet resistivity of the emitter layer, $\rho_{s,em}$ will be given as 500 $\Omega/\square$, with standard values lying within the range of 300 - 600 $\Omega/\square$.

4.6.3 Technical limitations

Technical limitations cover restrictions placed on parameters that are not due to the properties of the material, but rather the processing and characterisation side. Due to the lithography and lift-off process, a lower limit on the emitter finger width needs to be given. This is because fingers that are too narrow encounter problems during the lift-off process, and if any

problems due to RTA-induced glass curvature (section 4.5.3) are encountered, these are magnified by the light leakage between the photomask and the photoresist layer on the glass surface.

A minimum emitter finger width of 10 μm is chosen, which is smaller than that used for previous photomasks, but large enough such that natural wrinkle-like features or glass variation does not unintentionally increase the finger width. Here, the fingers are kept uniformly wide in shape which allows for a simpler metallisation process with less margin for poor lift-off results. In theory tapered emitter fingers, for instance increasing from 5 μm at the airside busbar, to 15μm at the emitter busbar may be used for slightly less resistive losses along the emitter fingers.

The Al emitter electrode/poly-Si n^+ sidewall contact area, E, is chosen to be 100 nm. This is generally among the smaller possible values for successfully plasma-etched sidewall profiles. However, contact widths such as this are far more likely to be obtained when metallising devices than the optimal large-area contacts discussed in section 4.3.

For sizing the busbars, it is noted that the probe size of the light I-V tester used to contact the cell's busbars is approximately 1 mm x 2 mm. Therefore each busbar should be at least this wide, or have a contactable area this size to allow for characterisation. The emitter busbars are tapered from ~60 μm at the edge of the cell, to 1000 μm in the centre, allowing for a contact pad area which is used as the probing area. For the purpose of calculating the resistive and shadow losses, the effective emitter busbar width is 530 μm.

The cell size is another parameter that needs to be determined prior to optimisation. Generally, for thin-film poly-Si on glass, the smaller the cell size, the less fractional power losses present, even if a non-optimal emitter busbar width is used [54].

For a lower limit on cell size, the value of 1 cm^2 is used. This is small enough to allow for future investigations of non-uniformities in the plasma etching profile, as a large amount of cells can be defined on a 5 x 5 cm^2 superstrate. In addition, it is the smallest cell area accepted for one-sun cell efficiency results in the published solar cell efficiency tables [86], which is a good guide as to the minimum cell area for general publication of cell results.

Table 4.7 shows a summary of the parameters to be held constant for the optimisation, taking into account both material and technical limitations.

4.6.4 Geometric considerations

Geometric considerations that arise from the interdigitated metallisation pattern also need to be noted and defined carefully, particularly when using computer software to assist in the optimisation process to ensure the values attained physically make sense and do not corrupt the optimised parameters attained. What follows is a list of criteria that are required:

- Cell parameters W_A, A, B, C, S all greater than 0.

Table 4.7: Summary of cell parameters (constants) required for optimisation of the metallisation pattern, including both material and technical limitations.

Name	Symbol	Value and unit
Voltage at maximum power-point	V_{MP}	400.0 mV
Current at maximum power-point (no BSR)	J_{MP1}	18.0 mA/cm^2
Current at maximum power-point (with BSR)	J_{MP2}	25.0 mA/cm^2
Al film sheet resistivity	$\rho_{s,Al}$	0.0187 $\Omega/\square$
Emitter layer sheet resistivity	$\rho_{s,em}$	500.0 $\Omega/\square$
Emitter Al/n^+ contact area	E	100 nm
Emitter finger width	W_F	$\geq$10 μm, uniform width
Emitter busbar width	W_E	530 μm, tapered
Cell size	$2AC$	1 cm^2

- Finger spacing S greater than finger width W_F.
- Finger width greater than or equal to the defined minimum finger width.
- The sum of emitter busbar width W_E, finger length B, and airside busbar width W_A is equal to cell length C.
- The product of cell length and width ($2A$ x C) is equal to the desired cell area.

4.6.5 Parameter optimisation

Cell parameters requiring optimisation are the emitter finger spacing (S), the finger length (B), the airside busbar width (W_A) and the cell length

and width, (respectively $2A$ and C) the product of which forms the cell area.

The simplest way to find these optimal values is to enter all fractional (normalised) power losses from chapter 3's summary of losses (table 3.3) into a spreadsheet program. Here, Microsoft Excel is used, however any software package with a solver function is suitable such as OpenOffice Calc.

An additional entry, the sum of all fractional power losses is also entered. The power loss formulas are then filled out using the material and technical constraints identified in the previous sections.

For the parameters that need to be optimised, only approximations need to be entered, since these values will be the subject of the optimisation process. Once all parameters have been inserted into the spreadsheet, the optimisation can begin. Figure 4.10 shows a screen capture of the Microsoft Excel Solver function, with both parameters that require optimisation, and geometric considerations ('constraints') entered.

The target cell (the sum of all fractional losses) is set to equal a minimum by changing only the parameters discussed at the start of this section: emitter finger spacing and length, airside busbar length width, together with the cell dimensions. The geometric considerations discussed in section 4.6.4 are then entered as a series of inequalities in the constraints area of the Solver function.

Upon solving, the desired parameters are optimised to reduce the total power losses, and for this example these are shown in table 4.8, both

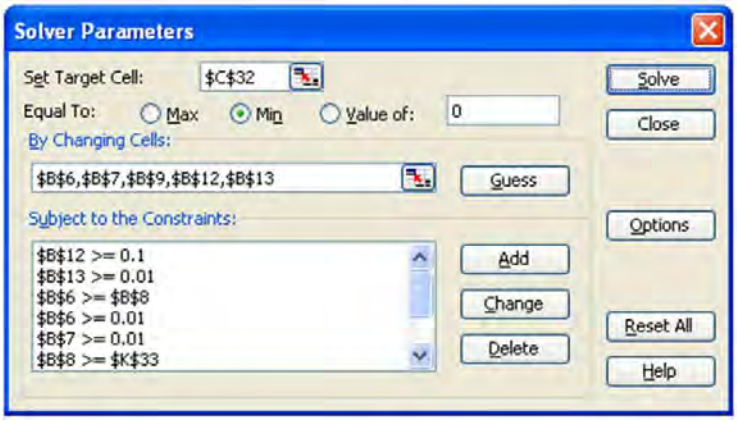


Figure 4.10: A screen capture of Microsoft Excel's Solver function. The target cell is the sum of fractional power losses, the parameters that require optimisation are in the cells to be changed text box. The constraints are simply the geometric considerations discussed previously.

with and without a SiO_2 BSR.

Table 4.8: Summary of the parameters and values that are optimised for both lower current cells (no SiO_2 BSR), and high current cells (SiO_2 BSR).

Parameter and symbol	Optimised value (no BSR)	Optimised value (with BSR)
Finger spacing, S	321 μm	285 μm
Finger length, B	1.23 cm	1.15 cm
Airside busbar width, W_A	660 μm	609 μm
Cell length, $2A$	0.74 cm	0.79 cm
Cell width, C	1.36 cm	1.27 cm

Table 4.9 shows the loss locations and fractional power losses for the low and high current devices. As expected, there are more I^2R resistive losses associated with the use of a BSR, however from an efficiency point of view this is more than made up for by the increased current.

As a comparison, the total resistive and shadow fractional power losses for the 4 x 1.1 cm devices used in this thesis (shown in figure 4.3) are 19.8 % for a no-BSR device (assumed J_{MP} = 18 mA/cm^2) and 22.4 % for a device

Table 4.9: The fractional power losses from each resistive and shadow loss component, with no BSR, and with a BSR for the optimised cell parameters.

Location and loss type	Fractional power loss (no BSR) [%]	Fractional power loss (with BSR) [%]
Emitter layer, resistive loss	0.37	0.42
Emitter fingers, resistive loss	1.76	1.91
Airside fingers, resistive loss	0.06	0.07
Emitter busbar, resistive loss	0.09	0.14
Airside busbar, resistive loss	0.07	0.12
Emitter contact, resistive loss	0.71	0.88
Emitter fingers, shadow loss	2.84	3.19
Emitter busbar, shadow loss	3.91	4.18
Total fractional power loss	9.81	10.91

with a BSR (assumed J_{MP} = 25 mA/cm^2). The fractional power losses for these 4.4cm^2 area cells are mainly from emitter feature shadow losses: ~9 % from the emitter busbar shadow loss, and ~4 % from the emitter finger shadow loss.

Almost all of the remainder of the power losses is divided almost equally between the lateral resistive loss in the n^+ emitter, resistance of the airside and emitter busbars, and the contact resistance at the sidewall. For the no-BSR device these range from 1.32 to 1.59 %, and for the BSR devices these range from 1.84 to 2.21 %.

The excess power losses come from the resistance of the emitter and airside fingers, which contributes less than 1 % to the total fractional power loss.

Due to time constraints, the metallisation of cells using interdigitated patterns with lower fractional power losses could not be fully investigated. The author believes that the large differences in power losses be-

tween optimised photomask designs discussed here, and those used for metallised devices in the remainder of this thesis show the enormous potential for further improvement in device efficiencies and currents.

4.7 Chapter summary

The self-aligned metallisation process to fabricate interdigitated cells is introduced in detail, which is compatible with a SiO_2 BSR for high current devices. The contact between the Al emitter electrode and poly-Si n^+ sidewall is the main cause of variations in the series and shunt resistances of devices metallised using the self-aligned scheme.

Using optical microscopy combined with FIB imaging, a better understanding of the sidewall profile and Al/n^+ layer contact area as a function of plasma etching time is given. If there is an appearance of a textured poly-Si film in the emitter finger groove when viewed through an optical microscope, it is likely the metallised device will suffer from shunting problems. A 'patchy' appearance, comprised of both glass and islands of the poly-Si emitter film appears to be the ideal for fabricated high FF, high efficiency devices. If all the poly-Si emitter film has been etched away and only glass is visible in the finger groove, it is still possible for a reasonable Al/n^+ poly-Si contact to be made.

The effect of thermal annealing is documented for metallised PECVD thin-film poly-Si cells and found to provide the largest improvement to both voltage and efficiency after annealing at 200 °C. This is contrast to

thin-film poly-Si cells deposited by e-beam evaporation, where 250 °C is widely regarded as the optimal post-metallisation anneal temperature.

The metallisation of PECVD diodes with an absorber deposited at high-rate are reported, where particularly high FFs of almost 73 % are attained. These are the first reported efficiency results for the metallisation of high-rate absorber thin-film poly-Si cells on textured glass superstrates. No major faults from series or shunt resistance is present, however the current of the high-rate devices is lower than expected. This is believed to be from phenomenon independent of cell metallisation; (i) The RTA process which introduced glass curvature, reducing the resolution of the photolithography process, and (ii) From high temperature RTAs (1000+ °C), which if not optimised with time, increase the peak EQE wavelength and shift the p-n junction towards the airside of the device.

Finally, a step by step outline to the design of an optimal photomask for interdigitated thin-film cells on glass is given. For a cell without a SiO_2 BSR, the total fractional power loss from metallisation can be reduced from ~20 %, for the 4.4 cm^2 cells investigated in this thesis, to ~ 10%, and for a cell with a SiO_2 BSR, from ~22 % to ~11 %. Optimisation of the photomask is thus a promising method to further enhance efficiencies and currents of interdigitated devices in the future.

Chapter 5

Wire-bond cell tabbing

"Let him look to his bond."

– Shylock to Salarino in Shakespeare's *The Merchant of Venice*.

5.1 Introduction

THIS chapter introduces wire-bonding as a proposed interconnection technique for or thin-film solar cells on glass. Firstly, an initial introduction is given outlining the difficulties of the interconnection of thin-film devices on glass (section 5.2). Prior to being used for attempts at series interconnection, cell tabbing - the wire-bonding of the busbars of individual cells to external contact leads (tabbing tape), is introduced in section 5.3, together with motivation for attempting the tabbing of individual cells before attempting to form interconnected mini-modules.

The remainder of the chapter focuses on determining the feasibility of wire-bond / cell tabbing on poly-Si on glass devices. The effect on cell shunt resistance, increasing amounts of wire-bond connections, a method for encapsulation, and the thermal stability of both wire-bonds and the tabbing is investigated. Finally in section 5.8, cell tabbing is applied to high efficiency individual cells as a means of attaining further efficiency boosts as a proof of concept for wire-bond tabbing.

5.2 The challenge of interconnection

5.2.1 Introduction and review

The superstrate and diode structure of the poly-Si devices studied here not only provide a challenge for cell metallisation, but also for interconnection to form mini-modules. Three key points for the motivation of the research and development of thin-film mini-modules on glass are; i) Interconnection to form modules allows for high-voltage, low-current devices which reduce resistive losses when compared to single cells of the same area; ii) (Mini-)modules can take advantage of light scattered within the glass superstrate that would otherwise be lost with small-area single cells; and iii) Is a natural progression of research efforts once a single-cell metallisation scheme capable of high fill factors has been developed.

Walsh [87] outlines the main considerations of interconnection schemes designed specifically for thin-film solar cells on glass as follows:

- Parallelism - the provision of more than one current path through the module to safeguard against shading or individual cell failure.
- Ease of manufacture - each processing step should be designed with a vision to be utilised on an industrial scale.
- Robustness - the scheme should allow for relatively large margins of error and allow for minor variations in processing.
- Thermal budget - thermal processes increase the final module price and additional processes should be avoided wherever possible.
- Light trapping - since thin-film solar cells rely on light trapping for reasonable current densities, any metallisation or interconnection scheme needs to allow for the possibility of incorporating light trapping capabilities.

Figure 5.1 shows the busbar interface that results from the interdigitated self-aligned metallisation discussed in the previous chapters. The **challenge of interconnection** requires electrically connecting the emitter busbar of cell A with the airside busbar of cell B without shunting the device, taking into account the considerations listed above.

The two most successful interconnection schemes for poly-Si on glass previously developed in the Thin-Film Group at the University of New South Wales are:

(I) The wrap-over interconnection scheme [87], which uses laser scribing to selectively form conductive and non-conductive sidewalls. It was noted

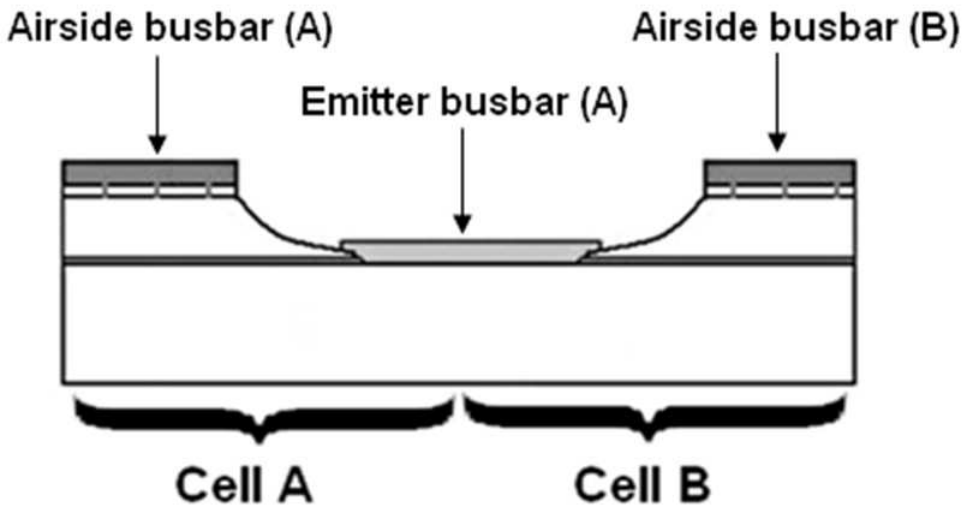


Figure 5.1: A schematic showing the busbars of two adjacent cells. The challenge is to connect the emitter busbar of cell A with the airside busbar of cell B without shunting the device.

that by using laser scribing along the sidewalls, an insulating thermal oxide layer forms on the sidewall of the scribe. The scheme involves a first laser scribe and oxide removal step (HF dip) to form one conductive sidewall, followed by a partially overlapping laser scribe with no oxide removal step, forming an insulating sidewall. Evaporated Al is then used to form the interconnection over the insulating sidewall as shown in figure 5.2.

As the interconnection only required laser scribes, this scheme allows for very small area devices. A mini-module containing 70 interconnected cells (individual cell area 0.24 cm^2) was fabricated, however the averaged open-circuit voltage per cell was low (346.6 mV). A high series resistance (9.2 $\Omega.cm^2$) and heavy shunting (57.5 Ω) resulted in a poor fill factor (< 40 %) and mini-module efficiency (2.6 %). The conclusion from this scheme was that the sidewall with the oxide layer of sidewall was not insulative

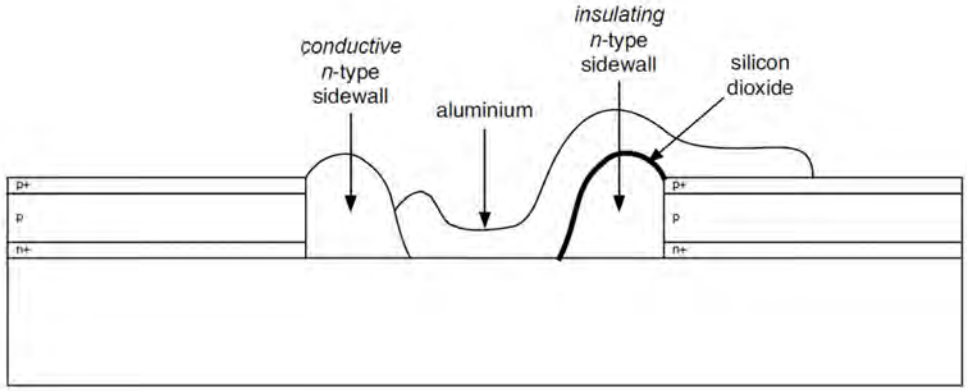


Figure 5.2: A cross-sectional image of the wrap-over interconnection scheme from [87], where laser scribing is used to form both conducting and insulating sidewalls and Al is used to form the interconnection.

enough to prevent shunting.

II) The screen-printed scheme shown in figure 5.3, whereby the emitter electrode (referred to as the *glass-side* electrode in the figure) is scribed through to the glass using a Nd:YAG laser (1064 nm, Q-switched). Using stencil printing, a dielectric polymer is printed over the scribe and partially covers a segment of each busbar. A silver paste is then printed, overlapping the polymer to connect the adjacent cells [87, 88].

Using this screen-printed scheme, cells were able to be successfully interconnected in the sense that the mini-module voltage is equal to the sum of the individual cell voltages, however a number of problems related to other device parameters were present; (i) The short circuit current density (per cell) of the mini-module (15.1 mA/cm^2) is significantly lower than the pre-interconnected current densities of the individual cells (18.2 mA/cm^2). This is due to the large shadow loss from the busbar region between the adjacent cells, required for the interconnection; (ii) The fill-

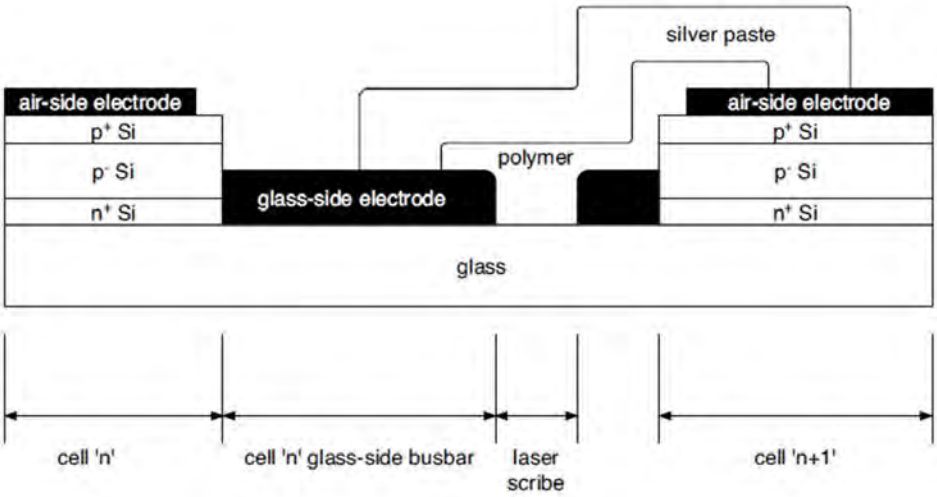


Figure 5.3: A schematic cross section of the monolithically integrated scheme from [87]. A laser scribe isolates the cells and an insulating polymer is used to prevent shunting. Silver paste is used to form the interconnection.

factor of the module was again poor (48.7 %), owing to both high series (27.6 Ωcm^2) and low shunt (129.4 Ω) resistances. This is likely due to the primitive metallisation scheme used [89] and the poor contact between the screen-printed silver paste and the busbars.

In this proceeding section, wire-bonding is presented as an alternative interconnection scheme to the above techniques. The concept is then investigated as a cell tabbing technique on individual cells as a proof of concept, prior to being utilised to form mini-modules in the proceeding chapter.

5.2.2 The wire-bonding solution

Wire-bonding, also referred to as fine wire microbonding early in its development, was advanced and popularised in the 1960s as a method for the interconnection of metal surfaces on a micron scale. Wire-bonding found use in almost all areas in microelectronic circuitry, including in integrated circuit (IC) - printed circuit board (PCB) interconnections, on transistor dies, and within packages such as flat packs [90, 91]. The technology has since advanced considerably, leading to smaller wire sizes, smaller contact pad areas, faster bond speeds and increased bond strengths.

Here, ultrasonic wedge-bonding of Al is chosen as it is deemed to be the best fit given the considerations for an interconnection technique in the previous section:

- Parallelism - since wire-bonds can be placed at a very high density on any metallised surface, the failure of one or more wire-bonds can have a negligible effect on the resulting mini-module, any parallel strings can be placed anywhere on the mini-module.
- Ease of manufacture - wire-bonding is a mature technology with wide-scale use in the microelectronics industry. It does not require the use of a cleanroom and has the capability to be scaled up to large area (>1 m^2) substrates.
- Robustness - automatic wire-bonds are commercially available where the bond force, distance, loop height, and other parameters can be regulated using software and sensors.

- Thermal budget - the wedge-bonding of Al wire can be conducted at room temperature and does not require any heating of the wire, unlike both ball-bonding (100 - 500°C) and the wedge-bonding of gold wire (~150 °C). This ensure the underlying Al electrode and poly-Si is not thermally affected by the wire-bond process.

- Light trapping - the diameter of the individual wires are the order of 25 μm and thus can be used at a high density without affecting the bifacial properties of cells. In addition, since the bond loops extend vertically, it is possible to use them in conjunction with a rear reflector, provided the material can be deposited under the bonds.

Ultrasonic wedge-bonding of Al wire therefore appears to be a suitable alternative interconnection technique for pre-metallised poly-Si films on glass. The interconnection scheme proposed in this thesis centres around using a laser scribe to electrically isolate the busbars via physical separation, followed by wire-bonding to interconnect the emitter and airside busbars of adjacent cells. Figure 5.4 shows this schematically, with a cross section of a wire-bond connecting the emitter and airside electrodes (busbars), and a laser-scribed etch physically separating the emitter busbar. The figure is heavily based on figure 5.3 (from [87]) to show the similarity of the schemes; wire-bonding replaces the silver paste for the electrical connection and air is used as the insulation instead of the polymer.

Since air is being used as the isolation layer there should be no shunting present - in contrast to the previously investigated thermal oxide-coated

Si sidewall (figure 5.2) and screen-printed polymer (figure 5.3).

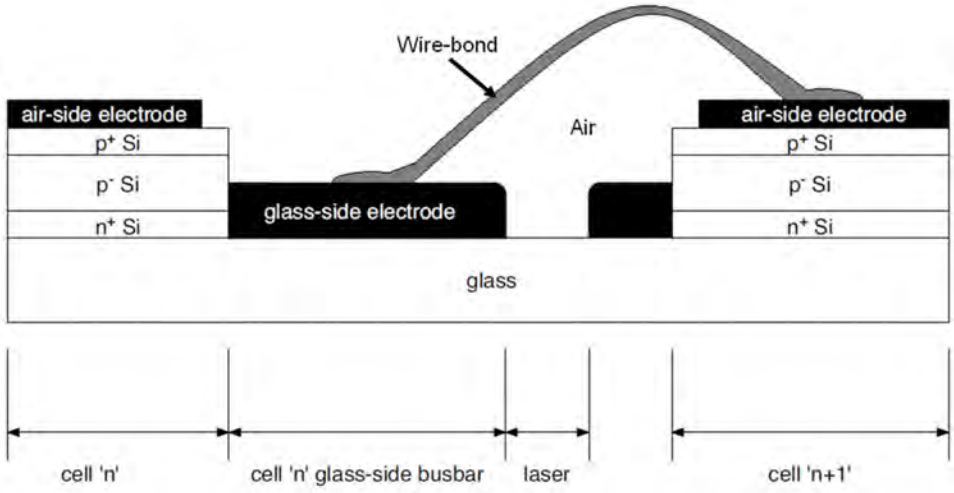


Figure 5.4: A schematic cross section of a wire-bond interconnection scheme. The image, modified to include the wire-bond and air gap, was originally produced by Walsh [87] and is included to show the similarities in the interconnection schemes.

5.3 Cell tabbing

5.3.1 Introduction and motivation

In investigating wire-bonding as a interconnection technique, it was chosen to first concentrate on using wire-bonding for the tabbing on single-cells, prior to expanding the technique into wire-bond cell interconnections if successful. The factors that influence this choice are; (i) Multiple cell tabbing experiments can be conducted on the one sample (four cells over a 5 x 5 cm^2 superstrate); (ii) If one cell is shunted, or otherwise damaged it cannot be used for series cell interconnection; (iii) Having adjacent cells with similar current densities was not always possible at the time

due to irregularities in the plasma etching process, and dopant diffusion into the absorber from the RTA process, as noted in section 4.5.4.

Therefore preliminary investigations into using wire-bonding as a cell tabbing technique is investigated as other researches focused on optimising the RTA process to fabricate diodes suitable for series interconnection.

In section 3.2.4 it was noted that the effective busbar length, A, could be halved by either placing a second external contact lead point at the other end of the device, or by placing the lead halfway along the busbars length. In the power loss analysis for the interdigitated metallisation approach in section 3.4.6, placing the positive and negative contact leads halfway along the busbar length is the standard configuration.

This section extends the reduction of effective busbar length further, by the application of wire-bonding to connect an individual cell's busbars to an Al tabbing tape material placed on top of the cell. A top-view of the proposed connection is shown in 5.5, where the conductive material (Al tape) is shown partially transparent for clarity. The use of wire-bonding to connect the busbars of a cell's busbars to Al tape is referred to as cell tabbing.

Tabbing has the following two main advantages; (i) Since the conductive tabbing material is considerably thicker (~ 30 μm) than the Al-evaporated busbars (< 2μm), the resistive loss along the busbar is reduced considerably; (ii) The wire-bond connections require only a very small contact area, approximately 40 x 80 μm.

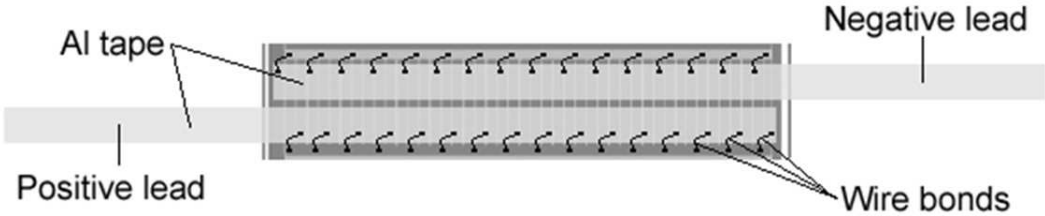


Figure 5.5: A top-view schematic of wire-bonding used to connect the busbars of a cell to Al tabbing tape. The Al tape has been shown partially transparent for clarity, however is 100% opaque in practice.

Figure 5.6 shows a focused-ion beam (FIB) image from the top-down of a wire-bond head, bonded to an Al busbar. The small contact area of the bond head, permits the use of significantly decreased busbar widths, lowering shadow losses from the emitter busbar.

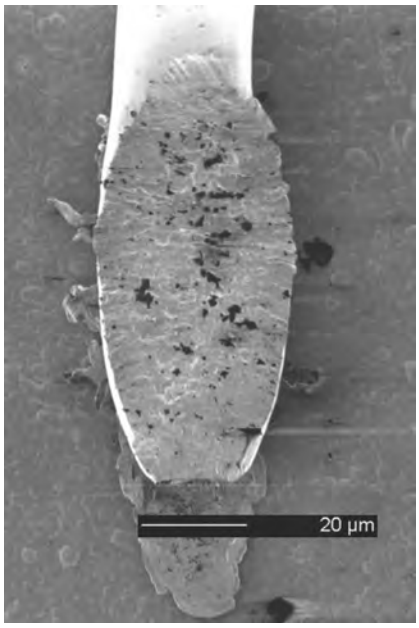


Figure 5.6: A focused-ion beam image (top view, 0° tilt angle) of a wire-bond head bonded to an Al busbar. The dimensions of the bonded area are approximately 40 x 80 μm.

5.3.2 Theory

To quantify the advantages of cell tabbing, the summary of power losses developed in chapter 3, table 3.2 will be revisited. The fractional resistive power loss for a busbar is given by:

$$P_{F,bb} = \frac{1}{3} A^2 \frac{J_{MP}}{V_{MP}} \frac{\rho_{s,bb}}{W_B},$$

where A is the distance from the end of the busbar to the current extraction point (generally equal to half the entire cell length), C is the cell width, J_{MP} is the maximum power point current , $\rho_{s,b}$ is the sheet resistivity of the busbar, and W_B is the busbar width.

The use of tabbing has the effect of reducing the distance A, in proportion to the number of wire-bond connections added. This reduced distance can be denoted as A_n, and is equal to $\frac{A}{n}$, where n is the number of wire-bonds connecting the busbar to the tabbing tape, assuming the wire-bonds are equally spaced along the cell busbar length.

The other consideration is that the tabbing tape is effectively acting as a second busbar, and thus has it's own resistive power losses along its length - the same as per the evaporated Al busbar that lies on the cell. The advantage of the tabbing tape, of course, is that it can be considerably thicker than the evaporated busbar, and since it can be placed directly over the cell area, can be considerably wider too.

The fractional resistive power loss along a piece of tabbing tape is therefore equal to the sum of these two losses:

$$\sum P_{L,bb} = \frac{1}{3} A_n^2 \frac{J_{MP}}{V_{MP}} \frac{\rho_{s,ab}}{W_A} + \frac{1}{3}(2A)^2 \frac{J_{MP}}{V_{MP}} \frac{\rho_{s,at}}{W_{AT}},$$

where $\rho_{s,t}$ is the sheet resistivity for the tabbing tape and W_T is the width of the tape. A distance of $2A$ has been used for the tabbing tape, since it is assumed current is extracted at the edge of the cell, rather than in the centre of the cell length.

To appreciate the reduction in power losses resulting from the use of tabbing tape, we may divide this summed resistive power loss of the tape by the resistive power loss of just the busbar when no tabbing is used, effectively giving us the normalised power loss. Doing this, we find the relative level of power losses with and without the tabbing tape simplifies to:

$$\frac{1}{n^2} + 4\left(\frac{\rho_{s,t} W_B}{\rho_{s,b} W_T}\right),$$

where n is the number of wire-bonds present.

The following example outlines the reduction in resistive power losses stemming from the use of cell tabbing. The following parameters have been used for the example, although these can be modified by the reader as needed: an Al tape sheet resistivity of ~ 9.3 x 10^{-4} $\Omega/\square$ (Al resistivity 2.8 x 10^{-8} Ωm and thickness 30 μm); an Al tape width of 4 mm. For the Al busbar, values from section 4.6.3 will be used: a sheet resistivity of 0.0187 $\Omega/\square$, and busbar width 500 μm.

Table 5.1 shows the relative resistive power loss levels when using tabbing tape, as compared to without tabbing tape (the 100 % baseline level),

for different amounts of wire-bond connections. The $\frac{1}{n^2}$ component represents the resistive power loss along the emitter/airside busbars towards a wire-bond connection, and the $4\left(\frac{\rho_{s,t}W_B}{\rho_{s,b}W_T}\right)$ component represents the resistive power loss along the tabbing tape. These values combine to give a relative power loss level compared to the baseline value. As the power loss along the tabbing tape is independent of the number of wire-bond connections used, this value is constant for all amounts of wire-bonds. Note that for case of n = 1 wire-bonds, one is better off characterising the cell directly without the use of tabbing tape, (i.e. directly measuring the 100% baseline) as the tabbing tape effectively acts as a resistor in series with the wire-bonded emitter/airside busbars.

Table 5.1: Relative resistive power loss of wire-bonded tabbing tape busbar compared to no tabbing tape using parameters found in the text. The case of no tabbing tape (i.e. a normal busbar) corresponds to the 100 % loss level.

Number of wire-bonds, n	$\frac{1}{n^2}$ component	$4\left(\frac{\rho_{s,t}W_B}{\rho_{s,b}W_T}\right)$ component	Sum of component losses
1	100.000 %	2.487 %	102.487 %
2	25.000 %	2.487 %	27.487 %
4	6.250 %	2.487 %	8.737 %
8	1.563 %	2.487 %	4.050 %
16	0.391 %	2.487 %	2.878 %

By using 4 or more wire-bonds connecting the busbar to the tabbing tape, the resistive power loss from the tabbing tape replacing the busbar is less than 8 % of that without using tabbing tape. At 16 wire-bonds, the majority of the power loss is due to resistance of the tabbing tape, and reduces, on an absolute scale, the resistive power loss component from busbar current transport by over 97 %.

This resistance can be further reduced by using tapes with thicker metallic films, which reduces the sheet resistivity, or by using wider tapes, which will also reduce electrical resistance.

5.4 Effect on cell shunting

5.4.1 Introduction

The proposed wire-bonding connection method involves ultrasonic wedge-bonding, which uses a high frequency (60 - 125 kHz) transducer. The ultrasonic energy softens the wire-bond material, in this case Al wire, and a clamp is used to press it against the target material which is also softened. This process also removes the oxides and contaminants from the surface of both the wire and the target area, allowing for a clean contact [92].

The main concern with wire-bonded connections on thin-film cells is the effect both the ultrasonic energy used to form the bond, and the clamp that presses the wire on to the target have on the thin (2 - 3 μm) poly-Si material, and the p-n junction that lies under the Al electrode.

As the thickness of the wire-bond is more than ten times that of both the poly-Si and the airside electrode, the danger of shunts forming through the junction from either the ultrasonic and clamp process is clear. To investigate the presence of any shunting, wire-bonds were progressively added to connect the airside busbar of a metallised cell to a strip of Al

tabbing tape, and the resistance of the cell's p-n junction continuously measured.

5.4.2 Method

Al tape (model AT502-50, from Advance Tapes), which consists of one side of non-conductive, pressure sensitive acrylic adhesive and another side of 30 μm Al foil is placed on top of a metallised thin-film poly-Si cell of area 4.0 x 1.1 cm^2. The airside and emitter busbars are left exposed to allow room for wire-bond connections to be formed and probes to be placed.

The wire-bond connections are formed by wedge-bonding 25 μm diameter Al wire (with 1 % Si) using a commercial ultrasonic wedge-bonder (Kulicke & Soffa, model 4523). Black felt is placed on the glass side of the sample to prevent stray light from entering the cell, and small probes are attached to the emitter and airside busbars.

A total of 16 wire-bonds are connected between the airside busbar and the tabbing tape, evenly distributed along the 4 cm long busbar. To detect any shunting of the cell's junction from the wire-bonding process, the resistance between the emitter and airside busbars is measured continuously using a digital multimeter as the wire-bond connections are added between the airside busbar and tabbing tape.

5.4.3 Results and discussion

The resistance across the busbars as a function of increasing wire-bonds is shown in figure 5.7. The large decrease in resistance from the first 1 - 4 bonds can mainly be attributed to calibration of the various wire-bonding parameters to ensure a satisfactory bond is formed.

The calibration involves adjusting the bond power, time, and force for the first and second bonds, as well as the loop height, tear strength and tail length. Reasonable wire-bond settings were found to produce high yield bonds which are displayed in table 5.2 and these were kept constant for the remainder of the bonds.

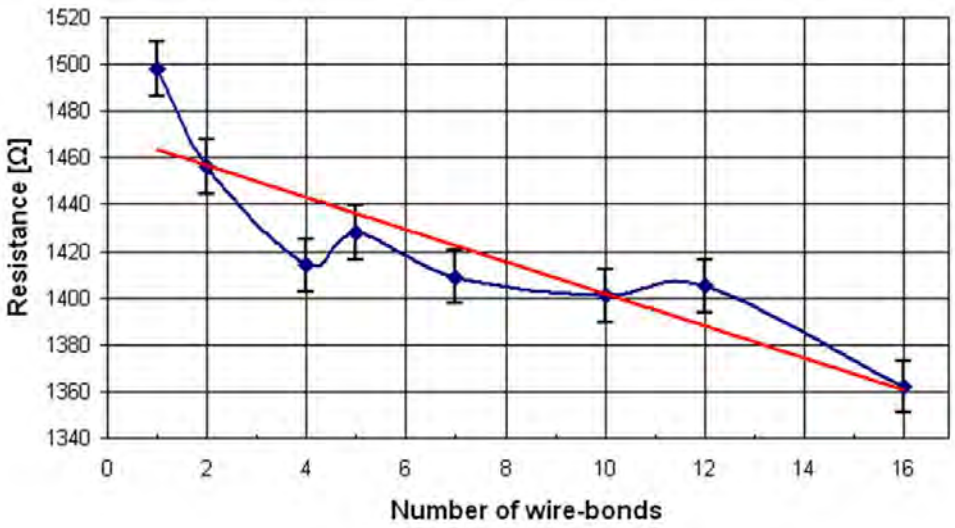


Figure 5.7: The effect of increasing wire-bond connections on emitter-airside busbar resistance. The Y-axis error bars correspond to the multimeter manufacturer's tolerance of 0.8% at a resistance range of 2000 Ω. The red line is the linear best line of fit for the measured data.

After 16 wire-bonds are placed, the resistance dropped from ~1500 to 1360 Ω, which suggests that either the ultrasonic power or the pressure

of the clamp can adversely effect the cell junction. The magnitude of this effect, however, is minimal when considering; (i) The deviation in fill factor from the theoretical maximum is primarily due to series resistance, for the self-aligned metallisation used here. Such a small reduction in shunt is unlikely to reduce the cell's fill factor by more than 0.15 % absolute; (ii) Here, a wire-bond density of 4/cm along the busbar is used. In practice, only 2 wire-bonds per cm busbar length, or less, may be required for cell interconnection; (iii) The wire-bond settings were not optimised to reduce shunting. A parameter-set that results in less shunting may exist.

If we disregard the first four wire-bonds placed, the remaining 12 bonds still produced a decrease in resistance, from ~1420 to 1360 Ω, corresponding to an average of ~5 Ω per wire-bond connected. This suggests that placing wire-bonds does impinge the cell junction and have a small adverse effect, however the net effect resulting from reducing series resistance and the possibility of smaller busbar widths greatly overcomes this effect. It is highly probable that alternate wire-bonder settings that have even less influence on the cell junction can be experimentally found.

Table 5.2: Wire-bond parameter settings that produced high-yield bonds without causing any major shunting of the cell junction. The wire-bonder used is a model 4523 from Kulicke & Soffa.

Parameter	First bond	Second bond
Tear	2.6	
Loop	6.5	
Tail	3.5	
Power	2.5	1.5
Time	2.9	2.9
Force	1.35	1.45

The above experiment was repeated on an emitter busbar, which lies di-

rectly on the glass superstrate. The Al tabbing tape was placed directly over the airside busbar and 16 wire-bonds were connected. No change in resistance was measured, indicating the tabbing tape has enough of a cushioning effect to not affect the airside busbar and underlying poly-Si material.

5.5 Sequential increase of wire-bonds

5.5.1 Introduction and method

In the previous section it was found that the addition of wire-bonds causes a small amount of shunting when connecting the airside busbar to the tabbing tape, and no shunting when wire-bonding the emitter busbar. In section 5.3.2 it was found that with at least 4 wire-bonds the resistive loss from the tabbing tape (busbar replacement) is over 90 % less than without tabbing tape. Here, these effects will be experimentally measured by wire-bonding the emitter and airside busbars of a metallised poly-Si cell to tabbing tape and measuring I-V data whilst sequentially increasing the amounts of wire-bond connections.

The Al tape used is the same as for the investigation into cell shunting, Advance Tapes model AT502-50 which consists of a 30 μm Al film on one side, and an insulating acrylic adhesive on the other side, which is used to stick the tape on the cell surface. The width of the tape is between 4 mm and 5 mm. Figure 5.8 is a digital photo showing the placement of the tabbing tapes and the two cells used in this investigation. Laser isolation

scribes have been used along the emitter busbar of each cell to ensure each cell is electrically isolated.

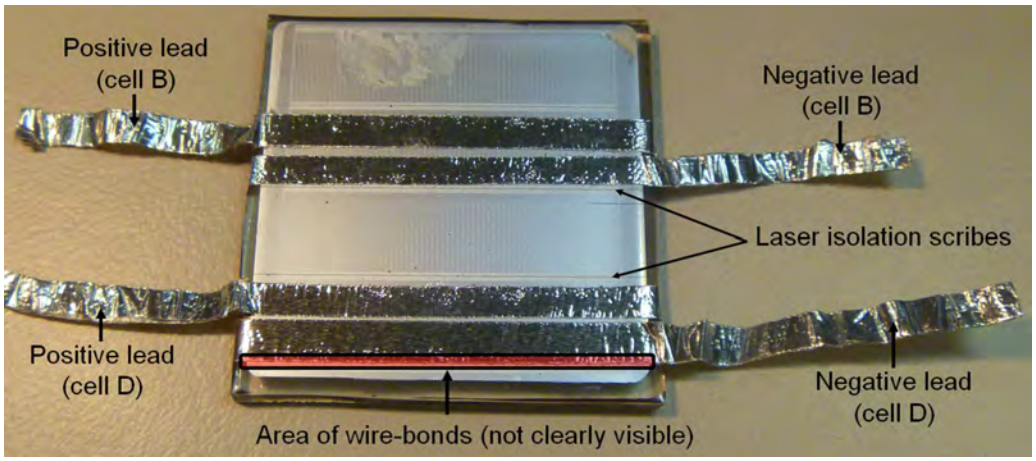


Figure 5.8: A digital photo of cells B and D, with the emitter and airside busbars of each cell connected to Al tabbing tape with wire-bonds. The are of each cell is 4.4 cm^2 and they have been electrically isolated using a laser scribe.

The wire-bond material and equipment used is the same as in the previous investigation into the shunting effect: 25 μm diameter Al wire with 1 % Si content, which is ultrasonically wedge-bonded using a Kulicke & Soffa model 4523 wedge-bonder. The amount of wire-bonds along each busbar are progressively doubled from 1 to 32, and I-V results are taken after each set of wire-bonds are connected. The length of each of the busbars is 4 cm. Figure 5.9 shows a side-view digital photo of the wire-bonds running along the tabbing tape after all 32 wire-bonds per busbar have been bonded. After the measurement with 1 wire-bond was taken, the wire-bond was removed so that the remaining wire-bonds (multiples of 2) were equally spaced. The wire-bonds are added along both the emitter and airside busbars of each cell.

I-V data is measured after each set of bonds are connected to the tape.

The glass superstrate temperature is ~25 °C during measurement, and each cell is apertured using black felt to 4.4 cm^2.

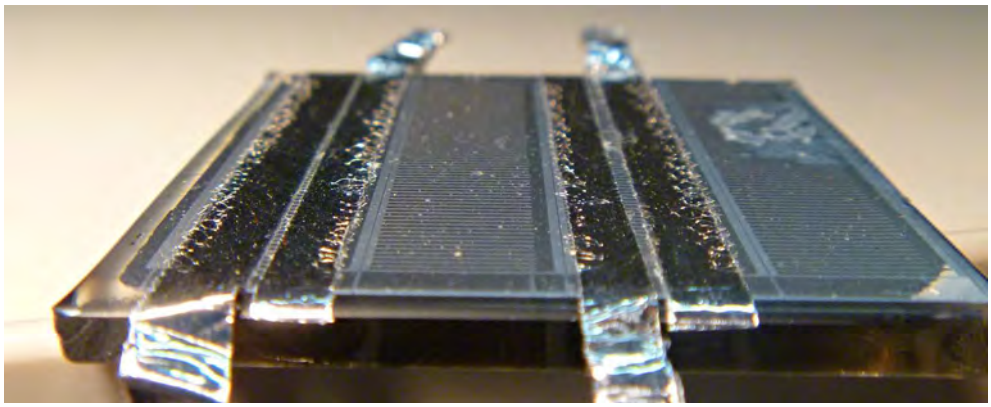


Figure 5.9: A digital photo (side-view) of the cells with Al tabbing tape after the completion of all 32 wire-bond connections from each busbar to the tape. The wire-bonds are the numerous string-like protrusions running along the top of the busbar-tape interfaces.

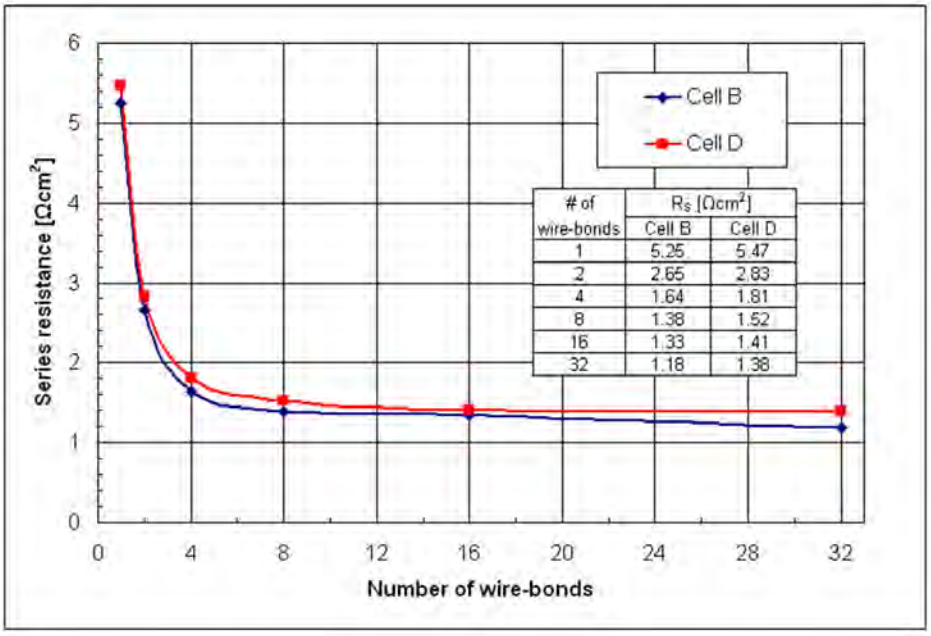
5.5.2 Results and discussion

Figure 5.10 shows the measured series resistance of cells B and D, after each series of wire-bond connections, with the raw data as an inset. The high cell series resistance value from the 1-wirebond datum is affected by the electrical resistance of the wire-bond itself, which is on the order of 0.05 Ω for a wire-bond connection of 1 mm in length.

With two or more wire-bonds, the series resistance from the tabbing scheme is dominated by the emitter/airside busbar resistive power loss towards the wire-bonds and the resistive loss along the tabbing tape effects, as discussed in the cell tabbing theory 5.3.2.

By increasing the amount of wire-bonds from 1 to 32, the bulk series

resistance of the cells decreased from 5.25 to 1.18 Ωcm^2 for cell B, and 5.47 to 1.38 Ωcm^2 for cell D. These final series resistances of the tabbed cells represent the series resistance of the devices with a negligible power loss contribution from the busbars: less than 2 % (table 5.1) than that of devices without tabbing tape.



# of wire-bonds	R_S [Ωcm^2] Cell B	Cell D
1	5.25	5.47
2	2.65	2.83
4	1.64	1.81
8	1.38	1.52
16	1.33	1.41
32	1.18	1.38

Figure 5.10: Measured series resistance for cells B and D after the respective amount of wire-bonds have been connected. Inset: The numerical series resistance data as a function of increased wire-bonds.

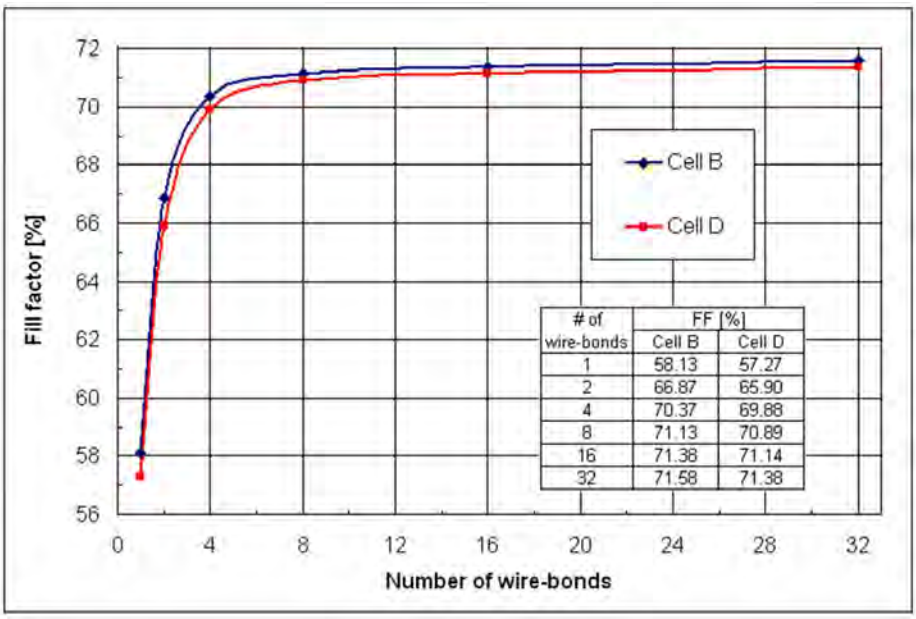
The 1.18 Ωcm^2 series resistance of cell B is the lowest series resistance measured for cells metallised using the self-aligned metallisation scheme in chapter 4, and the lowest series resistance of a thin-film poly-Si on glass fabricated at UNSW.

In section 5.4 the possibility of wire-bonds contributing to the cell shunting was raised. The key point is to confirm the reduction in series resistance outweighs any shunting from the placement of wire-bonds. Fill

factor, which is ideally a function of the series and shunt resistances, is an ideal measure to determine the net effect.

Figure 5.11 shows the I-V measured fill factors on cells B and D with increasing wire-bond connections to the tabbing tape. For doubling the amount of wire-bonds up to 32 (8 per cm of busbar length), the fill factor for both cells steadily increases, to 71.58 for cell B and 71.38 for cell D.

As the fill factor still increased when going from 16 to 32 wire-bonds per busbar on both cells, any wire-bond induced shunting present, if any, is not enough to decrease or balance out the fill factor gain from the reduced series resistance.



# of wire-bonds	FF [%] Cell B	FF [%] Cell D
1	58.13	57.27
2	66.87	65.90
4	70.37	69.88
8	71.13	70.89
16	71.38	71.14
32	71.58	71.38

Figure 5.11: Fill factors for cells B and D after the respective amount of wire-bonds have been connected. Inset: The numerical fill factor data as a function of increased wire-bonds.

One valid question to ask is that if the series resistance of these cells is particularly low and there is no major shunting present (after 32 wire-

bonds, cell B shunt 2111.32 Ω, cell D 2575.06 Ω), why isn't the FF closer to 73 %, as was the case with the high-rate absorber cells investigated in section 4.5? The answer lies in the strong effect V_{OC} has on capping the maximum fill factor of photovoltaic devices [35]. Here, the V_{OC} of cell B is 447 mV which corresponds to a theoretical maximum fill factor (with no series resistance and infinite shunt resistance) of ~75.9 %. For a device with a V_{OC} of 483 mV, as in section 4.5, this theoretical maximum FF is more than 1 % higher at ~77.1 %.

5.5.3 Summary

Wire-bonds, sequentially added to connect the cell's emitter and airside busbars with Al tabbing tape reduce the I-V measured series resistance of metallised cells considerably - to 1.18 Ωcm^2 and 1.38 Ωcm^2. The fill factor of the cells each increased to over 71 % after 32 connected wire-bonds. Since no decrease in fill factor occurred from 16 to 32 wire-bond connections, if there is any shunting of the device caused by forming the wire-bonds, it is not enough to manifest as a reduction in fill factor. The gain in fill factor from a reduction in series resistance far outweighs shunting, if any, from wire-bond formation.

5.6 White-paint encapsulation

5.6.1 Introduction and motivation

Encapsulation layers and films are commonly used in industry as a means of extending the module warranty and enhancing reliability. The most thoroughly investigated encapsulated is the organic-based ethylene vinyl acetate (EVA) [93] which is commercially available under many different product names. In recent years, other materials have been developed which claim increased UV stability, improved clarity and transmission, stiffer and faster curing times. Examples of more advanced encapsulation materials include Dow Corning Corporation's silicone-based PV-6100 [94], and the DuPont series of encapsulants including PV5200 (polyvinylbutryal, PVB) and the more stiffer and stronger ionomer-based PV5300 [95].

Here, a considerably cruder approach is used: commercially available white paint. The white paint encapsulation proposed here is devised to protect the protruding wire-bonds from breaking or becoming disconnected due to handling, and to protect the metallisation itself which is vulnerable to scratches and damage.

5.6.2 Method

Two poly-Si diodes on glass are metallised using the self-aligned scheme as described in section 4.2. One diode is fabricated on a planar glass

superstrate (sample 1), and the other is fabricated on a AI-textured superstrate (sample 2). Each glass sample contains four cells, however due to wrinkles in the glass from the RTA process, only two cells from sample 1, and three cells from sample 2 were flat enough for lithography, and thus successful metallisation, to be carried out on.

After metallisation, Al tabbing tape is applied to the airside surface of the cells and 8 wire-bonds, evenly distributed along the busbars, are connected from the busbars of each cell to the tabbing tape.

Commercially available white spray paint (White Knight quick dry enamel - Flat White) is used, since applying paint by a brush will physically break the 25 μm diameter wire-bonds. The tabbing that lies off the cell surface is covered with plastic to prevent the insulating white paint from affecting characterisation. The white paint is sprayed from all angles to ensure it is deposited both underneath and on top of the wire-bonds in an attempt to planarise the surface, maximising protection of the wire-bonds. As a result of the application of the paint from all angles, white paint coats the sides of the glass superstrate as well.

Cell I-V is measured before and after enough white paint encapsulant is applied to planarise the cells. The current of the cells is of particular interest since current gains of over 40 % (~1 μm thick) and 20 % (~1.6 μm thick) have previously been reported by applying white paint on the airside of bifacial planar thin-film poly-Si solar cells [96]. Whilst the cells used in this investigation are thicker, at ~2.2 μm and contain an blanket Al contact on the airside surface, these results show that there is still scope for current gains in thin-film devices by applying white paint on

completely metallised devices as a final light trapping component. This is particularly true for current that would otherwise leak from the sides of the glass, which now has the possibility to be scattered back into the cell.

5.6.3 Results and discussion

Figure 5.12 is a digital photo showing a single-cell tabbed sample during the white paint encapsulation process. As no wire-bond protrusions are visible, the cell has been successful planarised by the paint which has coated above and below the wire-bond connections.

After drying, the sample can be handled and placed airside-down (superstrate configuration) without the wire-bonds breaking or otherwise affecting the device performance.

Figure 5.12: A digital photo of a single-cell tabbed sample undergoing encapsulation by white paint. No wire-bond protrusions are present and the sampel is sufficiently planar to protect the wire-bonds are drying.

The measured I-V data for short-circuit current both before and after white paint encapsulation is shown in table 5.3. A planar glass superstrate is used for cells on sample 1, and a textured glass superstrate is used for sample 2. The change in current from the white paint application is most evident in the planar samples, where the short-circuit current density increased from between 0.12 and 0.28 mA/cm^2.

The change in current for the sample 2 cells, with a textured glass superstrate, was markedly lower than the planar cells, and negative for cell B. The negative change in current for sample 2, cell B can be attributed to a small amount of paint that reached the glass-side of the cell during application. This blocks some of the incoming light and reduces output cell current and is due to the cell wrinkles and glass curvature problems previously reported.

Table 5.3: The I-V measured short-circuit currents before and after white paint encapsulation. Sample 1 refers to a planar glass superstrate and sample 2 refers to a textured glass superstrate. The change in short-circuit current density, J_{SC}, is found by dividing the change in current by the cell area (4.4 cm^2).

Sample, Cell	I_{SC} [mA] before encaps.	I_{SC} [mA] after encaps.	ΔI_{SC} [mA]	ΔJ_{SC} [mA/cm^2]
1, A	62.69	63.92	1.23	0.28
1, B	67.45	68.08	0.63	0.14
1, C	68.80	69.33	0.53	0.12
2, A	78.09	78.33	0.24	0.05
2, B	79.67	79.19	-0.48	-0.11

The white paint application resulted in a considerable increase in current for the cells on planar glass superstrates, whilst only minimum current gain was noted in the glass-textured devices. The largest increases occurred on the cells at the edge of the glass area (cell A on both samples),

which have the additional benefit of a larger glass surface area for scattering light back into the cell. Figure 5.13 is a digital photo (side angle) of the white paint encapsulant showing it's application extending to the sides of the glass superstrate. Cell A is adjacent to a ~7.2 cm border of white paint-coated glass whilst cells B and C are adjacent to only ~2.2 cm of glass. This confirms that the white paint does scatter light back into the cell, however this effect is reduced with larger glass sample sizes.

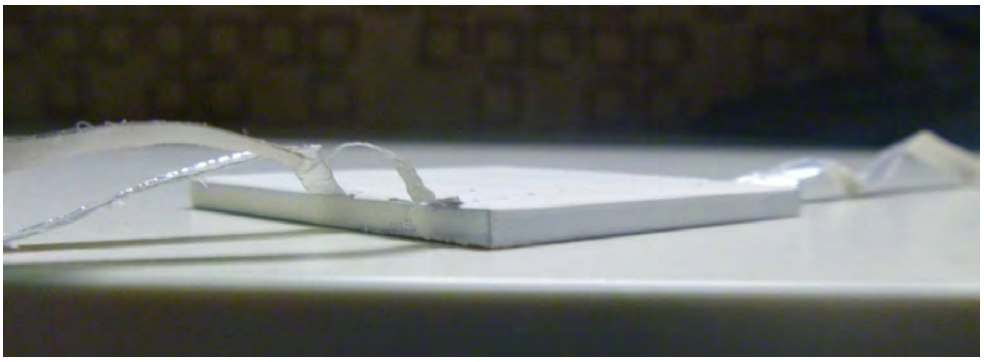


Figure 5.13: A digital photo (side angle) of a tabbed sample after the white paint encapsulant has dried.

The smaller increase noted in the textured cell (sample 2, A) suggests that the light trapping from the textured glass superstrate is already strong enough in the long-wavelength ranges. Any effect of either increasing the optical path length of long-wavelength light or back scattering from the paint coating the side surfaces of the glass superstrate is minimised due to the textured light trapping scheme already utilised.

Due to the planarisation and protection effect of the white paint, this encapsulation scheme is recommended practice for wire-bonded samples regardless of the nature of the glass superstrate.

5.7 Thermal stability of wire-bonds and tabbing

5.7.1 Introduction

The effect of thermal annealing processes on the device performance of metallised cells was investigated in section 4.4. This section aims to continue this investigation on wire-bonded/tabbed cells. The thermal stability and performance degradation, if any, of wire-bonds and the Al tabbing tape are important factors when determining the feasibility of this tabbing and interconnection technique, particularly on larger superstrate sizes and on an industrial scale.

Both the wire-bonds and the Al tabbing tape need to be able to sustain high temperatures found both in the field, and of any other thermal processes that are to be carried out on the tabbed/wire-bonded devices.

When investigating the thermal stability of the wire-bonds and tabbing, it is important to note that there are a myriad of effects present. In section 4.4.3 it was found that for metallised PECVD poly-Si cells, both voltage and efficiency peaked after annealing for 30 minutes at 200 °C. After 30 minutes at 250 °C, efficiency of the cells was lower than the initial value prior to any annealing. This was attributed to the Schottky barrier that forms at the metal-semiconductor interface and the different response of n and p-type material when in intimate contact with evaporated Al.

The additional of wire-bonds and tabbing tape are other sources of improvement or failure in the tabbed device performance stemming from thermal annealing. The wire-bonds act as numerous resistors in parallel with the cell busbar and tabbing tape, each with Al-Al contacts at each terminal, and the tabbing tapes act as resistors in series with the cell.

5.7.2 Method

PECVD material is metallised in accordance with the self-aligned scheme in section 4.2. Tabbing tape is added to the surface of the cell and 16 wire-bonds are connected between each of the airside and emitter busbars to the tabbing tape.

The tabbed sample is then sequentially annealed in a N_2-purged oven at 150 °C, 200 °C and 250 °C for 30 minutes at each temperature. Before the first anneal, and at the conclusion of each anneal, the wire-bonds and tabbing tape is inspected for any signs of breakage or thermally induced damage. I-V data is also taken before the first anneal, and after each subsequent anneal after the sample has cooled to ambient temperature, in the same manner as in section 4.4.2.

A particular parameter of interest is the open-circuit voltage of the device, since thermal annealing was found to have a strong influence on the voltage in poly-Si cells arising from the metal-semiconductor contact. Additionally, as the figure of merit for solar cells, efficiency is of interest since compromises in certain cell parameters (e.g. voltage degradation)

are acceptable provided it results in a net efficiency increase, for example, by a corresponding decrease in series resistance.

Finally, as the wire-bonds themselves and tabbing tape act as extra resistive elements to the device, the bulk series resistance will be investigated, as failures in wire-bond/tabbing tape connections, contacts and surfaces will manifest as an increase in measured series resistance of the device. This series resistance is again determined by measuring and comparing the I-V curves of the cells at two different light intensities, as in [81].

Note that during I-V measurement, the glass superstrate temperature was between 24.3 and 24.5 °C. Due to the high thermal coefficient of PECV-deposited poly-Si material [97], the voltages presented in this section are therefore not representative of those found at standard temperature and conditions (STC).

5.7.3 Results: Physical

Upon visual inspection of the wire-bonds after each annealing step, no wire-bonds were found to be disconnected, or otherwise removed from the busbars or Al tabbing tape.

After the 30 minute, 250 °C anneal however, the Al tabbing tape began to delaminate from the cell surface at the edge of the cell. The delamination of the tape is shown in figure 5.14 (a), where charring/discolouration is also present.

The under-side of the tape contains a pressure sensitive adhesive (acrylate polymers) which is transparent (i.e. both sides of the Al tape appear silver-coloured) when initially applied to the cell. Figure 5.14 (b) is a digital photo from the under-side of the tabbed cell, showing the charred tapes as a golden colour which occurred after the 250 °C anneal.

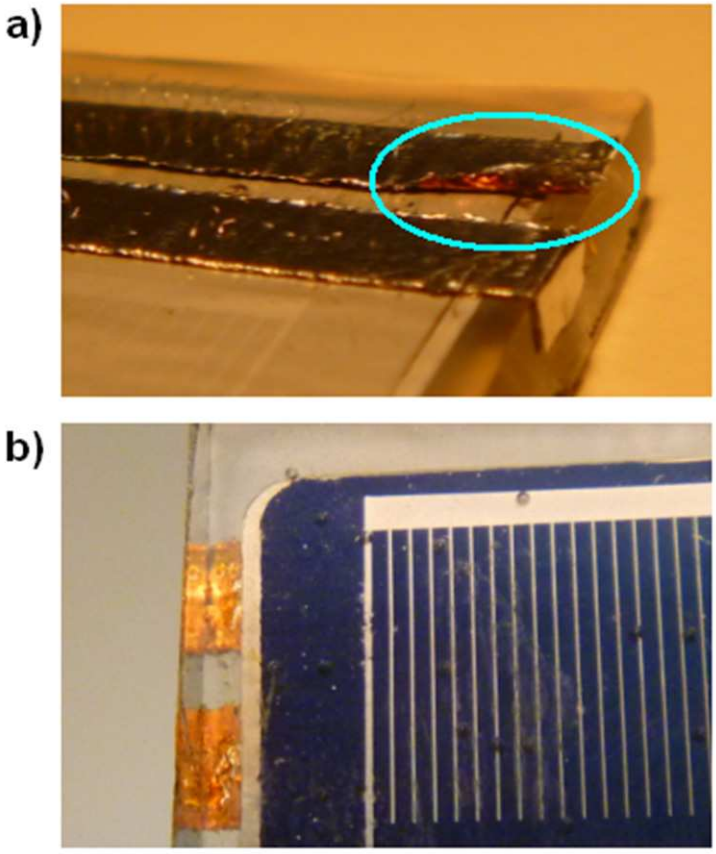


Figure 5.14: Digital photos of the delamination and charring found after the 30 minute, 250 °C thermal anneal. a) Delamination of the tabbing tape at the edge of the cell (circled in cyan). Charring is also visible on the under-side of the tape. b) The discoloured/charred ends of the tabbing tape from the glass-side, where light enters the cell.

Although the documentation for the Al tape used states the tape is flame retardant and has good high temperature resistance [98], it also states a

service temperature of -20 to 110 °C. Thus it was decided not to pursue any additional thermal anneals at 300+ °C.

5.7.4 Results: Electrical

The I-V measured open-circuit voltage before any annealing, and after each subsequent thermal anneal are displayed in figure 5.15. The open-circuit voltage increases only slightly (~2 mV) after the initial 30 minute, 150 °C anneal, then increases a further 5.5 mV after the 200 °C anneal. The open-circuit voltage drops considerably from the 250 °C anneal, well below the initial voltage prior to any annealing.

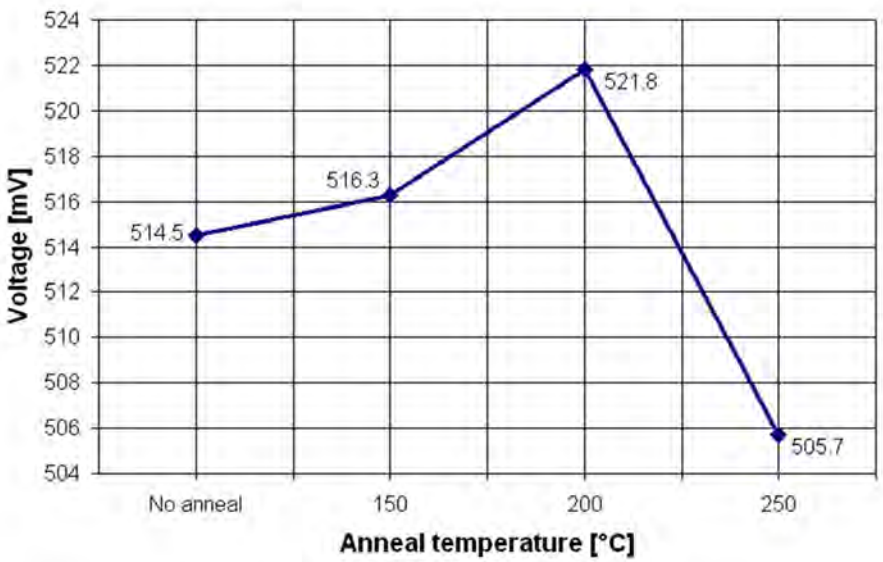


Figure 5.15: The I-V measured open-circuit voltage of a wire-bond tabbed poly-Si sample with no anneal, and after each thermal anneal. The anneals were for 30 minutes at the respective temperature. Note that the temperature of the glass superstrate was between 24.3 and 24.5 °C.

Figure 5.16 displays the one-sun efficiency and series resistance of the

sample without any thermal anneal, and after each 30 minute anneal. The efficiency of the device peaks after the 150 °C anneal, but is only marginally better than the initial efficiency with no anneal. The efficiency drops by 0.14 % absolute after the 200 °C anneal before a significant reduction is measured after the 250 °C anneal, dropping by a further 0.71 % absolute.

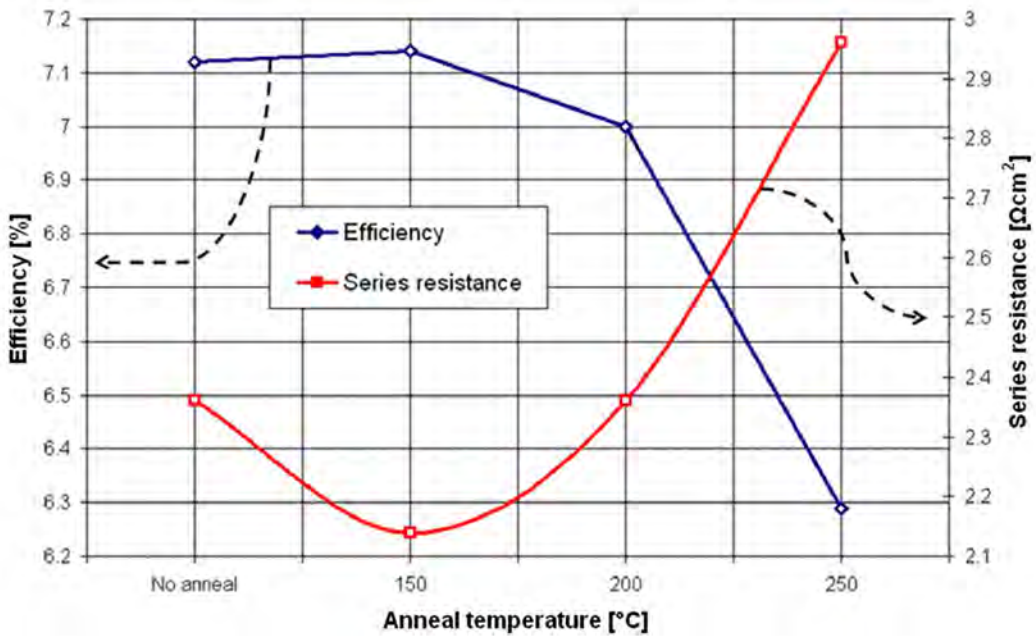


Figure 5.16: The I-V measured efficiency and series resistance of a wire-bond tabbed poly-Si sample with no anneal, and after 30 minute anneals at the respective temperatures.

The series resistance is 2.36 Ωcm^2 after tabbing and wire-bonding, prior to the first anneal. The series resistance decreases to 2.14 Ωcm^2 after the 150 °C anneal, is restored to the 'no anneal' value after the 200 °C anneal, and increases dramatically after the 250 °C anneal to 2.96 Ωcm^2.

5.7.5 Discussion

On a macroscopic level, no damage or physical disconnection of wire-bonds was visible upon thermal annealing to 250 °C. At 250 °C the Al tabbing tape began to delaminate towards the edge of the cell, and charring/discolouration was noted on the under-side of the tape. It was for this reason that further anneals at higher temperatures were not performed. The effect of the charring on the tape and any microscopic electrical changes in the wire-bonds is discussed with the series resistance results later in this section.

The voltage of the device as a function of thermal anneal temperature follows a similar trend to that of the untabbed cells investigated in section 4.4.

Here, only a slight increase (1.8 mV) is measured after the 150 °C anneal, followed by a strong (5.5 mV) increase from the 200 °C anneal. For the untabbed cells in section 4.4, the 150 °C anneal provided a significant boost in voltage, with the 200 °C only adding a minimal improvement. For both the wire-bond tabbed samples investigated here and the untabbed samples, the peak voltage occurred after the 200 °C anneal.

It is proposed that there are no additional effects at play with the addition of the wire-bonds and tabbing tape, as results are consistent with non-tabbed samples discussed in section 4.4. The voltage increase up to 200 °C and decrease after 250 °C can be explained by; (i) the increasing penetration depth of the airside Al film into the (hydrogenation-damaged) p^+ BSF with increased temperature; (ii) The Schottky barrier present at the

Al/n^+ poly-Si interface, where Al, a p-type dopant, diffuses into the poly-Si and reduces the effective doping concentration; (iii) De-hydrogenation, although this is believed to prevail mainly at anneals of 300 °C or more.

The series resistance is at a minimum after the 150 °C anneal and increases at higher anneal temperatures. This is directly seen in the device efficiency, peaking slightly after the no anneal efficiency, then decreasing slightly after the 200 °C anneal and dramatically after the 250 °C anneal. For the un-tabbed samples previously investigated, efficiency was found to peak after the 200 °C anneal, together with the voltage. This suggests that the wire-bonds and/or tabbing tape is affecting the electrical performance of the device on a microscopic scale.

Wire-bonding of Al wires on Al films is generally seen as a very reliable system, as mono-metallic systems such as Al-Al are not subject to corrosion or the formation of intermetallics at the interface. For example, ceramic dual in-line packages (CERDIPs), containing large numbers of Al-Al bonds are sealed at temperatures of 400+ °C for 30 minutes and do not suffer from weakening or reliability issues [99]. It follows that the wire-bond to busbar bonds are likely to be thermally stable.

The increase in series resistance is thought to be a combination of an increase in contact resistance between the evaporated busbars and the poly-Si material, and electrical resistance of the tabbing tape.

The delamination and discolouration of the tabbing tape confirms changes in the tape structure, at least on the bottom (adhesive) surface, have taken place. The charring of the tape and high-temperature annealing

may increase the sheet resistivity of the Al tape, for example by diffusion of contaminants into voids and microcracks in the Al film of the tape, reducing the *effective* conductive width and height of the tape.

Both the increasing series resistance and reduced cell voltage combine to explain the dramatic drop in device efficiency, particularly found after annealing at 250 °C.

5.7.6 Summary

The highest cell voltage occurs after the 30 minute, 200 °C anneal, which concurs with the result found for the non-tabbed cells investigated in section 4.4. After the 150 °C anneal, the efficiency and series resistance improved slightly, but degraded rapidly after annealing at higher temperatures. This is in contrast to the efficiency of non-tabbed cells, where the highest efficiencies were found after annealing at 200 °C.

The optimal process is thus to anneal the device for 30 minutes at 200 °C prior to wire-bonding and cell tabbing, securing the voltage increase of the cell without compromising the integrity of the tape. Once the cell has been wire-bonded to tabbing tape, annealing 30 minutes at 150 °C is recommended, to improve the contacts of the wire-bonds to both the Al busbars and tabbing tape.

5.8 Cell tabbing for high efficiency

5.8.1 Introduction and method

This section presents some notable results from cell tabbing that demonstrate the feasibility and effectiveness of the technique. Devices with either large increases in FF and efficiency as a result of cell tabbing, or results of cell tabbing on high efficiency devices are of interest here.

After standard self-aligned metallisation, the Al tabbing tapes are attached to the airside of the cells and between 8 and 12 wire-bonds per busbar are bonded to the tape. Cell I-V data are measured before and after the tabbing tape has been applied.

5.8.2 Fill factor increases from tabbing

Figure 5.17 shows the measured 1-sun I-V curve of the cell with the highest fill factor before, and after cell tabbing. The cell has been deposited on planar glass and does not contain a SiO_2 BSR. The low current (~15.99 mA/cm^2) and high voltage (497 mV) are both conducive to the high fill factor.

The placement of wire-bonds on this sample resulted in a decrease in series resistance of 0.46 Ωcm^2 to 1.27 Ωcm^2. Even though it is low for these PECV-deposited devices, the series resistance is still the dominant parasitic loss mechanism when compared to the shunt resistance of the

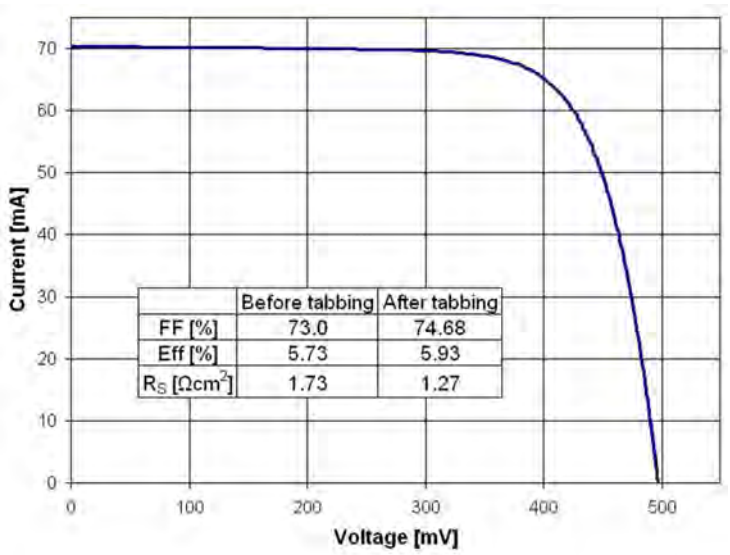


Figure 5.17: 1-sun I-V curve of the high fill factor cell after tabbing. The glass superstrate is planar and no SiO_2 BSR is present. The glass superstrate temperature was 24.89 °C and the cell was apertured to 4.4 cm^2 during measurement. Inset: The fill factor, efficiency and series resistance before and after cell tabbing.

final device (2780.03 Ω). The FF of this device (74.68 %) is among the highest fabricated for thin-film poly-Si on glass devices.

5.8.3 High efficiency tabbed devices

I-V data for high efficient (7 % or more) devices are reported in this section. Both cells reported have a point-contacted SiO_2 BSR, outlined in section 4.2.4 and have been fabricated on textured glass superstrates. Figure 5.18 shows the measured I-V curve of a 7.24 % efficient cell after tabbing, together with the FF, efficiency and series resistance before and after cell tabbing.

The reduction in series resistance to 1.85 Ωcm^2, together with the reason-

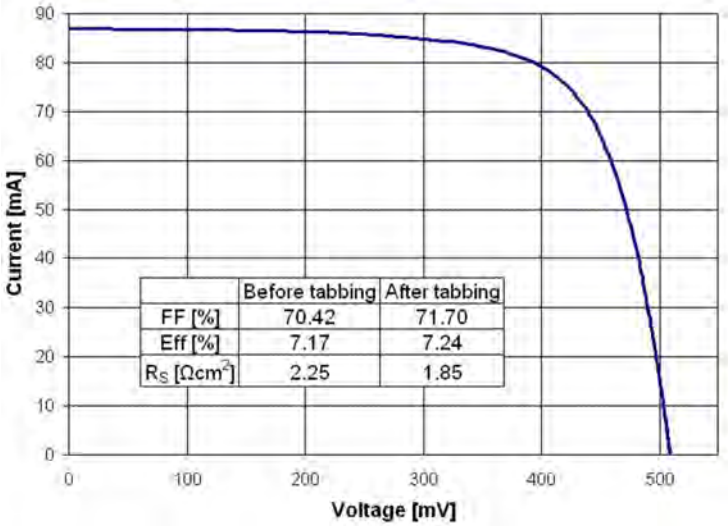


Figure 5.18: 1-sun I-V curve of the cell after tabbing. The glass superstrate is textured and a SiO_2 BSR is present. The glass superstrate temperature was 24.55 °C and the cell was apertured to 4.4 cm^2 during measurement. Inset: The fill factor, efficiency and series resistance before and after cell tabbing.

able shunt resistance of the final device (1866.58 Ω) from the application of wire-bonds results in a FF increase of 1.28 % to 7.24 %.

Finally, figure 5.19 shows the I-V curve of another high efficiency, tabbed device, also fabricated on textured glass with a SiO_2 BSR. The FF, efficiency and series resistance before and after tabbing are also included.

This device is one of the highest efficiency thin-film poly-Si solar cells fabricated at UNSW. Again, low series resistance, of 1.80 Ωcm^2 after wire-bonding, together with a high V_{OC} (508.15 mV) and high shunt resistance (2416.06 Ω) allow for a particularly high FF and final cell efficiency.

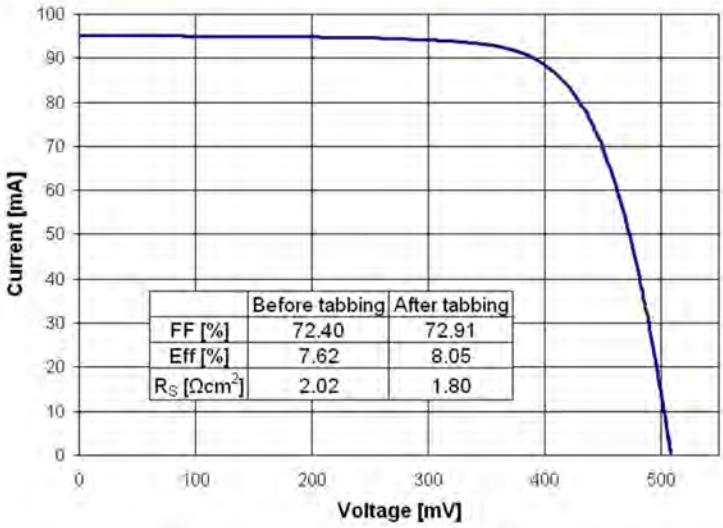


Figure 5.19: 1-sun I-V curve of the cell after tabbing. The glass superstrate is textured and a SiO_2 BSR is present. The glass superstrate temperature was 25.71 °C and the cell was apertured to 4.4 cm^2 during measurement. Inset: The fill factor, efficiency and series resistance before and after cell tabbing.

5.8.4 Summary

I-V data of the highest FF and efficiency cells that underwent cell tabbing are reported. By the use of cell tabbing, a cell with a FF of over 74.6 % was formed as well as a separate device with an efficiency of over 8 %. This confirms the potential of wire-bond connected cell tabbing as a means of decreasing series resistance.

The wire-bond cell tabbing processes increased the FF of the devices presented from between 0.51 % to 1.68 % absolute, and reduced series resistance from between 0.22 to 0.46 Ωcm^2.

Even with the large reductions in series resistance that arise from the cell tabbing process, series resistance is still the dominant parasitic ab-

sorption that reduces FF of cells metallised using the self-aligned process.

5.9 Chapter summary

The challenge of interconnection is presented and wire-bonded is introduced as a possible interconnection technique. In this chapter, a preliminary investigation into wire-bonding has been carried out on individual cells by connecting wire-bonds from the cell busbars to Al tabbing tape.

Theory of increasing wire-bonds is introduced, suggesting that the resistive power loss from the busbars can be reduced by over 90 % with 4 wire-bonds evenly spaced along the busbar, and over 97 % with 16 wire-bonds along the busbar.

A small contribution of shunting is found with the addition of wire-bonds on the airside busbar of metallised devices, however the magnitude of the effect does not manifest as a reduction in FF, which takes into account both series and shunt resistances. The decrease in series resistance from increasing the number of wire-bond connections far outweighs any increase in shunt resistance, up to 32 wire-bonds across a 4 cm long busbar, and therefore shunting is not seen as a detrimental factor for wire-bond tabbing or interconnection. The same investigation confirms strong reductions in series resistance from increasing wire-bond connections, with a 1.18 Ωcm^2 series resistance device fabricated from cell tabbing.

White paint, chiefly used as a method for encapsulting/protecting the wire-bonds during handling both fulfills this goal by planarising the air-

side of the device without affecting device performance, as well as provides a small increase in cell current for planar cells. The application of white paint on the airside of the device and on the glass sides allows for some long-wavelength light that would otherwise be lost, to be scattered back into the device.

The voltage of thermally annealed, tabbed samples is comparable with that found previously in chapter 4, peaking after the 30 minute, 200 °C anneal. The effect of annealing on series resistance and efficiency were optimal after the 150 °C anneal, but began to impair series resistance and efficiency performance after the 200 °C anneal. This is believed to be caused by a combination of series resistance of annealed tabbing tape and the busbar-poly-Si interface.

Annealing the sample for 30 minutes at 200 °C prior to tabbing and wire-bonding to increase the cell voltage, followed by an anneal at 150 °C after tabbing and wire-bonding is found to be the logical optimal anneal method for tabbed samples.

Finally, cell tabbing has been applied to high FF and high efficiency devices and delivers a notable increase in cell performance, leading to a tabbed device with a FF of over 74.6 % and a device with an efficiency of over 8 %. Even with the large reductions in series resistances found by wire-bond tabbing, series resistance is still the dominant loss mechanism that reduces the FF of metallised devices, accounting for between 75 and 97 % of the reduction in FF from the ideal.

Wire-bonding has been successful proven as a cell tabbing technique and

the preliminary investigation undertaken in this confirms its suitability as a series-cell interconnection technique.

Chapter 6

Wire-bond interconnection

"Eventually everything connects - people, ideas, objects. The quality of the connections is the key to quality per se."

– *Charles Eames*, American architect and industrial designer.

6.1 Introduction

THE previous chapter focused on using wire-bonding as a cell tabbing technique and resulted in reduced series resistances, with negligible increases in shunt resistance with up to 32 wire-bonds connected across a 4 cm long busbars. The remainder of this chapter focuses on using wire-bonding to form series-interconnected mini-modules.

Having a technique that can be used to produce interconnected mini-modules from metallised cells is a vital process for the Thin-Film Group

at UNSW, for both the characterisation of larger area devices, and as a proof of concept of the technology researched by the group. The importance is particularly strong in light of the previous attempts by the group at cell interconnection which was discussed at the start of chapter 5.

In this chapter, the wire-bonding technique used for the cell tabbing of individual cells is combined with laser scribe isolations and wire-bonding over the isolation groove to form series interconnected mini-modules. Results are reported for both a two-cell mini-module (section 6.2.3) and a four-cell mini-module (section 6.2.4) are reported.

An introduction to the design and optimisation of cells specially designed for both individual cell tabbing (section 6.3.2) and series interconnection (section 6.3.4) is given. Two innovative examples that incorporate wire-bonding in the metallisation layout are presented and discussed.

6.2 Efficiency results: Interconnected mini-modules

6.2.1 Introduction

Additional motivation for the fabrication of large area devices is provided by the recent work of Ouyang [73], which suggests that over 6 % (rel.) of current is lost due to light leakage - light scattered at the glass/Si interface (i.e. prior to light entering the Si material). This result was found for

PECVD poly-Si material on planar glass with a BSR, and textured glass both with and without a BSR.

The devices used in this section have been metallised by a former researcher in the Thin-Film Group, Dr. Per Widenborg. The cells used to produce the four cell mini-module, in particular, are ideal for this investigation as all four cells have similar fill factors and current across the 5 cm x 5 cm sample area.

The effect of wire-bonding on the voltage, current, FF, and efficiency before and after interconnection is of particular interest. A successful interconnections implies the sum of the V_{OC} of the individual cells is close to the final V_{OC} of the mini-module. The current is of interest since the light leakage effect discussed above should result in increased cell currents - particularly for the larger-sized mini-module.

The maintenance of FF, ideally a measure of series and shunt resistance, is another confirmation of a proper interconnection being formed between adjacent cells. Cell tabbing of individual cells reported minor contributions to shunting from increasing wire-bonds along the airside busbar, but at the same time considerable reductions in series resistance from reductions in *effective* busbar length strongly benefit the FF. A similar effect is expected for interconnected devices here.

For the device voltage and currents investigated here, the efficiency is expected to scale directly in proportion to the increase or decrease in FF resulting from interconnection.

6.2.2 Method

In this section, results from two mini-modules are reported, one two-cell mini-module and one four-cell mini-module. Both samples are deposited on textured glass superstrates, with the two-cell sample containing a point-contacted SiO_2 BSR. The four-cell sample does not contain a SiO_2 BSR. Once cells have been metallised using the self-aligned scheme, a Nd:YAG laser (wavelength 1064 nm, Q-switched) is used to scribe separation grooves in the emitter busbars to electrically isolate the cells.

Figure 6.1 is an isometric cross-section drawing of an emitter busbar between two adjacent cells. The figure shows an emitter busbar laser scribed, with the right side of the emitter busbar acting as an 'inactive' area - contributing to the shadow loss. Due to it's isolation, it is also unable to contribute to the emitter busbar resistance. A wire-bond is shown above the isolation groove, connecting the emitter busbar from the cell on the left to the airside busbar of the cell on the right.

Al tabbing tape, this time ~1cm wide, but otherwise the same as that used in chapter 5 is then applied to the first and last cells of the module to act as external contact leads. For the two-cell mini-module, 20 wire-bonds per connection are used - over the isolation groove to form the interconnection, as well as from each of the terminal airside and emitter busbars to the tabbing tape. For the four-cell mini-module 12 wire-bonds are added across each of the three isolation grooves, and from the terminal busbars to the tabbing tape.

Additionally, the white paint encapsulation step outlined in 5.6 is applied

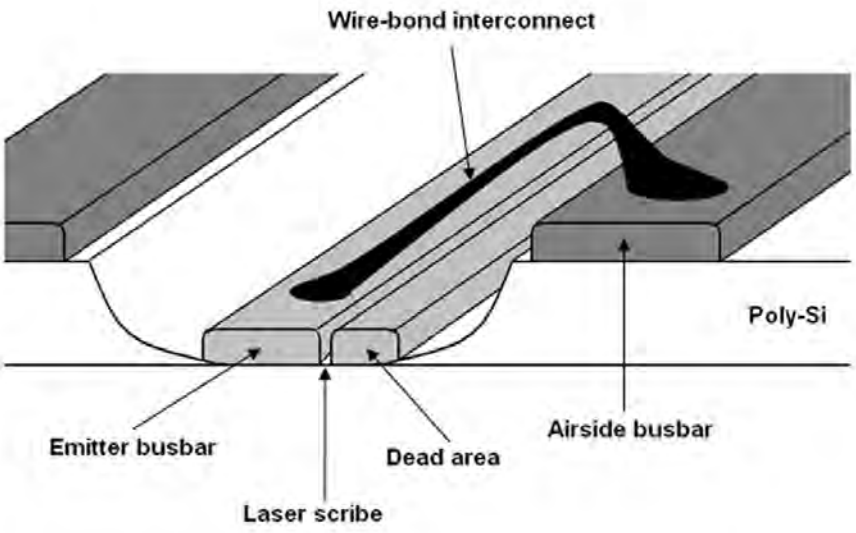


Figure 6.1: An isometric cross-sectional drawing of a wire-bond interconnection. A laser scribe electrically isolates the cells via the emitter busbar and a wire-bond is formed over the scribe to connect the emitter and airside busbars. For simplicity the glass superstrate is not shown. The image is not to scale.

to the four-cell mini-module to protect the wire-bonds from damage from handling and transport.

The I-V data of the individual cells before interconnection, and after the interconnection and tabbing process (in the case of the four-cell mini-module, after encapsulation) are measured and compared, to investigate the effect of wire-bond tabbing and interconnection to form mini-modules.

6.2.3 Results and discussion: Two-cell mini-module

Table 6.1 shows the I-V data individually for cells A and B, as well as for the interconnected mini-module. The V_{OC} of the mini-module is 99.7% of the sum of the two individual cells (1016.71 mV), indicating that the cells have been successfully interconnected using the wire-bonding technique.

The normalised ('per cell') short-circuit current density is 22.88 mA/cm^2, an increase of ~4 % over the lowest cell current of the module, 21.97 mA/cm^2 of cell A. It is proposed that increase in current is caused by the capture of light that would otherwise exit the device if a single cell was being characterised - the light leakage effect discussed at the start of the previous section.

Table 6.1: I-V results for the two-cell mini-module, using a SiO_2 BSR and a textured glass superstrate. Cells A and B are results before interconnection and cell tabbing. Each cell is apertured to 4.4cm^2. The mini-module is apertured to 8.8cm^2. Note that the mini-module short-circuit current density of 22.88 mA/cm^2 is normalised to 'per cell' rather than across the entire mini-module.

Parameter	Cell A	Cell B	Interconnected mini-module
V_{OC} [mV]	508.72	507.99	1013.51
J_{SC} [mA/cm^2]	21.97	22.26	22.88
FF [%]	69.78	68.45	71.41
Efficiency [%]	7.80	7.74	8.28
R_S [Ωcm^2]	2.15	2.30	4.95* / 1.24
R_{SH} [Ω]	1991.56	1163.06	1611.82
Glass temp. [°C]	25.11	25.66	25.22

*This R_S value has been incorrectly calculated by the I-V system software. The true R_S value is on the order of 1.24 Ωcm^2 - see text.

Notable increases are found in the mini-module's FF and efficiency, but this is contradicted by the large increase in measured series resistance given by the I-V tester. After investigating the LabView software used to parse the collected I-V data, it was found that indeed the algorithm incorrectly factored for interconnected cells; both voltage and current are not normalised to a 'per cell' level. For the 8.8 cm^2 interconnected mini-module here, the original algorithm performs the calculations as if it were a single 8.8 cm^2 cell rather than two individual 4.4 cm^2 cells. The outcome of this is that the 'cell' voltages used in the series resistance calculation are twice as much as they should be, and the current density is half of what it should be (i.e. it is divided by 8.8 rather than 4.4). For a 2-cell mini-module, this results in an outputted series resistance being 4x greater than intended and it follows that the true R_S is on the order of 1.24 Ωcm^2.

The increase in FF and efficiency of the mini-module resulting from the improved series resistance, together with the V_{OC} of the mini-module being ~double that of the individaul cells confirms that wire-bonding can successfully interconnect cells to form mini-modules, whilst not incorporating any additional parasitic resistances.

Figure 6.2 shows the 1-sun I-V curves from the two individual cells A and B, together with that of the series-interconnected mini-module. The voltage addition from the two cells, together with the increased current of the mini-module over that of the two cells confirm the successful interconnection to form an interconnected mini-module.

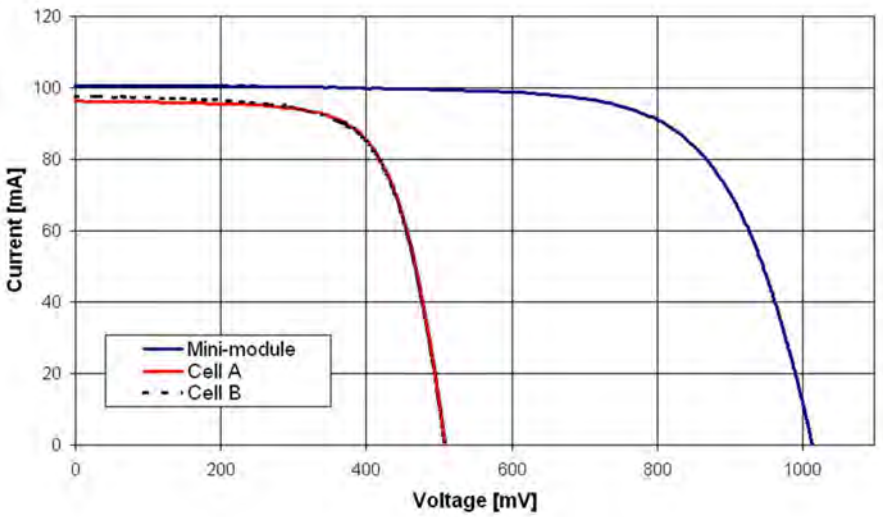


Figure 6.2: 1-sun I-V curves of the individual cells A and B (red and dashed black lines, respectively) before tabbing and interconnection, together with the I-V curve of the mini-module (dark blue line) after tabbing and interconnection. The glass superstrate is textured (AIT) and a SiO_2 BSR is incorporated into the cells.

6.2.4 Results and discussion: Four-cell mini-module

The I-V data of the four individual cells before interconnection, and those of the interconnected mini-module (after white-paint encapsulation) are shown in table 6.2.

The voltage of the four-cell mini-module is over 98.5 % of the sum of the four individual cells, again confirming the successful interconnection of the devices.

The normalised short-circuit current density for the interconnected mini-module is 19.12 mA/cm^2. This corresponds to an increase of over 8 % from the lowest individual cell current. This large increase is due to both the reduction of light leakage in the glass, and the white-paint encapsulation

application which covers the airside surface, as well as encompasses all sides of the glass superstrate.

Table 6.2: I-V results for the four-cell mini-module. Here, a textured glass superstrate is used but with a SiO_2 BSR. Cells A, B, C and D are results before interconnection and cell tabbing. Each cell is apertured to 4.4 cm^2. The I-V result for the interconnected mini-module is after white paint encapsulation has been applied, and is apertured to 17.6 cm^2. Note that the mini-module short-circuit current density of 19.12 mA/cm^2 is normalised to 'per cell' rather than across the entire mini-module.

Parameter	Cell A	Cell B	Cell C	Cell D	Interconnected mini-module
V_{OC} [mV]	430.82	433.30	433.67	431.73	1704.41
J_{SC} [mA/cm^2]	18.04	17.85	17.61	17.70	19.12
FF [%]	63.42	63.97	64.06	62.68	69.16
Efficiency [%]	4.93	4.95	4.89	4.79	5.63
R_S [Ωcm^2]	3.21	3.12	3.14	3.49	29.50† / 1.84
R_{SH} [Ω]	1129.81	1246.88	1166.27	745.38	2406.05
Glass temp. [°C]	25.45	25.23	25.00	25.11	25.18

Once again, the initial R_S value has been incorrectly calculated. Similarly to the 2-cell mini-module in section 6.2.3, in the calculation here (4-cell mini-module) the voltage values are 4x greater than they should be, and in addition the current density values used have been divided by 17.6 rather than 4.4. The end result being the otuputted series resistance is 16x larger than that intended. This new value, 1.84 Ωcm^2 has been included in the I-V table.

An additional reason for the reduction in R_S in this particular large area mini-module comes from the wider tabbing tape used, ~1 cm width as opposed to the ~0.4 cm width used for the cell tabbing of individual cells.

†This R_S value has been incorrectly calculated by the I-V system software. The true R_S value is on the order of 1.84 Ωcm^2 - see text and section 6.2.3.

The wider tapes can be seen in figure 6.3, a digital photo of the four-cell mini-module after tabbing, wire-bonding and white-paint encapsulation.

Figure 6.3: A digital photo of the four-cell mini-module after encapsulation with white paint. The wider (~1 cm) tabbing tapes are also visible.

The roughly doubled tape width results in more than half the resistive losses across along the tabbing tape, in according with the theory outlined in section 5.3.2. Since this resistive loss of a tabbed device, regardless of tabbing width, is already small compared to a non-tabbed busbar, the wider tabbing tape used here does not significantly further reduce R_S.

The combination of the increased (cell-normalised) J_{SC}, together with the significant reduction in R_S combine to produce a significant boost in efficiency from the individual cells to the mini-module: the increase from the average individual cell efficiency (4.89 %) to the mini-module efficiency of 5.63 % represents a relative gain in efficiency of over 15 %.

6.2.5 Summary

The concept of cell tabbing discussed in chapter 5 is combined with laser isolation of cells and the connection of wire-bonds across the isolation groove. Both a two-cell mini-module and a four-cell mini-module have successfully been tabbed and interconnected.

The voltage of the mini-modules is >98 % of the sum of the individual cells used to form the mini-modules, indicated the cells are successfully interconnected. For the two-cell mini-module, the efficiency increased from a cell-average of 7.77 % to 8.28 % for the interconnection mini-module. For the four-cell mini-module, the efficiency increased by over 15 % (relative), from the average of the individual cells to the interconnection mini-module.

The large increase in current within both mini-modules comes from the reduced loss of light leakage due to a higher capture area, and the series resistance reduction resulting from the cell tabbing and interconnection process. Additionally, for the four-cell mini-module the application of white paint on the airside, as well as on the sides of the glass superstrate provide an extra boost in cell current: an ~8 % increase in total, from the average current of the individual cells to that of the mini-module.

The results outlined in this section, together with those of chapter 5 have been published by the author in [50], and are the subject of a number of provisional and full patent applications.

6.3 Tabbing and mini-modules: Design and optimisation

6.3.1 Introduction

In this section, considerations for cells designed to be tabbed individually, and as part of interconnected mini-modules are presented.

Apart from factoring in these considerations, the optimisation for cells specifically designed for either tabbing, or incorporation into a mini-modules is done in the same manner as in chapter 4. The concept of the numerical optimisation, the most convenient and effect optimisation method is discussed in section 3.5.3. This has previously been applied to individual cells (which are not intended for cell tabbing), in section 4.6.

The optimisation process involves looking at the material constraints, technical limitations, and geometric factors. Material constraints - those related to the cell and metal contact material, are relatively unchanged, since the same poly-Si material is being used. The technical limitations based on the technology used is also the same: for example, the concerns over finger widths under ~10 μm still exist.

The main allowance for innovative designs involving wire-tabbing is in the metallisation geometry where notable differences exist. The use of wire-bonding for tabbing and interconnections allows for a large range of innovating metallisation patterns aimed to reduce both shadow and resistive losses. Two particular examples are discussed here which the

author has previously proposed in [100], although there is considerable scope for alternatives not yet conceived by the author.

The actual optimisation of these devices is done in the same manner as 4.6. Only changes in the values of parameters are required to perform the optimisation of the proposed new designs. The optimisation steps are therefore not repeated here.

6.3.2 Cell tabbing: Design

The cell tabbing approach outlined previously has been used to increase cell efficiency and FF of devices whose metallisation pattern was not originally intended for tabbing. This section focuses on a metallisation layout specifically to be compatible with cell tabbing.

In the previous optimisation in chapter 4, the emitter busbar has had to remain relatively large (i.e. consist of a 1 mm x 2 mm pad for probing). The airside busbar width, which contributes a resistive, but not a shadow loss, is also large at 660 μm and 609 μm for the no-BSR and BSR cases, respectively. These optimal widths were determined by the optimisation. The incorporation of wire-bonding and tabbing tape allows for the geometry of the devices to be re-arranged completely.

The area of a single Al wire-bond (25 μm, 1 % Si content) is ~40 x ~80 μm, although the author notes that an area requirement of 150 x 200 μm per wire-bond should be assumed, to allow for a margin of error in placement.

Some notes that inspire the new cell geometries are:

- Probing and characterisation of the tabbed devices can take place on top of, or beyond the cell area, reducing the need for large (1 mm x 2 mm) contact pad areas.
- The required busbar area is now only required to have a minimum area dictated by the wire-bond connection area.
- Since tabbing tape can be placed anywhere over the airside of the metallised cells without ill effect, it makes sense to use up as much of the area as possible with tabbing to reduce the resistance component.
- The wire-bonds can be placed and targeted anywhere on the device, so the emitter and airside busbar locations are not restricted to the far edges of the cell.

Figure 6.4 shows an example of the proposed 'fork' individual cell tabbing technique, after consideration of the above notes. The tabbing tape is shown transparent for clarity, however in practice it is opaque to light. The next section discusses the outcomes with regards to optimising individual cells with such a metallisation layout.

6.3.3 Cell tabbing: Optimisation

The basic layout developed above still follows the interdigitated scheme, and therefore the power loss analysis from chapter 3 can still be used for the analysis.

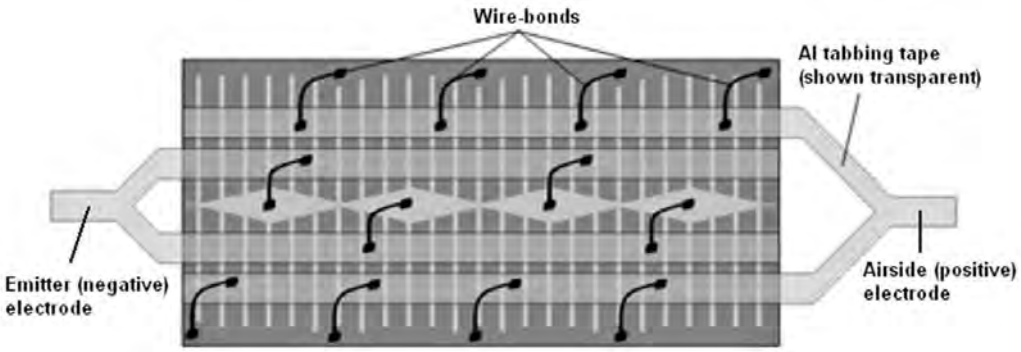


Figure 6.4: A schematic of the 'fork' style individual cell tabbing technique. Contact pads for the wire-bonds are located in the centre of the cell, effectively splitting the cell area up into two mirrored cells. The image is not to scale, with contact areas and wire-bonds shown larger for clarity.

Although the fork style layout appears trivial and similar to that of the regular, interdigitated layout, the advantages are realised when determining the new cell parameters needed for performing the optimisation. These advantages and resulting effect of the relevant cell parameters, as compared to a standard interdigitated devices of the same total cell area, are listed here:

- The uniform emitter busbar is replaced by multiple smaller, tapered 'mini'-busbars. The amount of these mini-busbars is regulated by the number of wire-bonds the operator wishes to place across the cell length. For every doubling of the amount of mini-busbars (i.e. a 2x reduction in length A), the resistive loss from the emitter busbar is reduced by a further 4x. This is due to the squared dependence of busbar length on fractional resistive loss.

- The emitter mini-busbars are located in the centre of the cell, which effectively split the full cell area up into two smaller cells. The out-

come is that the finger length, B is halved and thus the resistive loss along each finger is also reduced by 4x.

- The airside busbars at the top and bottom, which can also be thought of as mini-busbars are another source of a strong reduction in series resistance. The same squared-dependency of the number of mini-busbars on the fractional resistive loss exists here.

In figure 6.4, the area of the tabbing tape over the cell surface is ~50 %, however to make the full use of the tabbing tape, it should be applied to almost 100 % of the cell surface - leaving gaps where wire-bond connections need to be made.

This example shows one example of the tremendous potential the application of wire-bonding and tabbing tape has on the prospects of increases cell efficiency resulting from cell metallisation. Many more metallisation patterns, with various combinations of wire-bond and tabbing tape placement areas are feasible, and the author believes this to be an interesting path for attaining increases in the performance of individual cells.

6.3.4 Interconnection: Design

The design and optimisation of cells designed for us in interconnected mini-modules is perhaps one of the most critical further research areas identified, after the demonstration of the proof of concept of cell tabbing and interconnected mini-modules.

For cells metallised using the standard, interdigitated scheme, interconnection involves using a laser scribe across the emitter busbar (see for example figure 6.1). This incorporates an inactive area where neither light absorption or current transport can take place. This inactive area can be though of as comprising both the groove formed by the laser scribe, and the remainder of the emitter busbar itself.

The best previous attempts at interconnected devices (section 5.2.1) also contained a non-functional inactive area adjacent to the laser isolations scribe of either an n-type sidewall or remnants of the glass-side (emitter) electrode.

Unfortunately, there appears to be no trivial way to remove the requirement for this inactive area, but the author does propose a way to minimise its contribution to shadow losses. Figure 6.5 shows a schematic of the proposed method to reduce the influence of the inactive area of the emitter busbar.

For the Nd:YAG laser used in this thesis, the width of the laser scribe used to remove the emitter Al film is ~70 μm (at 1064 nm, Q-switched). The goal is to have the width of the emitter busbar just larger than this value, such that the laser isolation scribe can be performed routinely without straying onto the airside features, which results in shunting.

Contact pads specially designed and shaped for wire-bond interconnections are found at the terminals of multiple emitter fingers, regulated by how many wire-bond connections are desired. What remains of the 'active' emitter busbar is used to facilitate current transport towards the

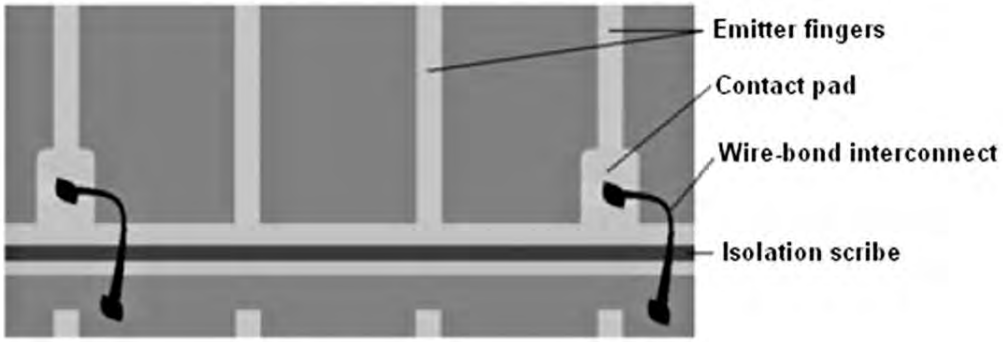


Figure 6.5: A schematic of the 'busbarless' interconnection scheme. The width of the emitter busbar is chosen to as to be only slightly larger than the width of the isolation scribe. Wire-bond connections are added from the terminals of the emitter fingers, rather than from the emitter busbar itself.

contact pads/wire-bond interconnections.

For realistic laser scribes, this active emitter busbar width will vary depending on the exact location and width of the laser isolation scribe. For certainty in device characterisation, the author proposes that every emitter finger could have a contact pad at it's terminal, and the amount of wire-bonds are selected based on the final width of the 'active' emitter busbar after laser scribing. For example, only wire-bonding one in every 16 fingers if the active busbar width is large, and one in every 8 fingers if the active busbar width is small.

6.3.5 Interconnection: Optimisation

With regards to the effect of metallisation structures such as this on optimisation, the only consideration to be noted is that the effective emitter busbar length, A is reduced depending on the number of wire-bonds.

However, the active emitter busbar width, W_E is also decreased - which has positive (shadow loss) and negative (resistance) effects on the device performance. Therefore a balance needs to be between these two parameters when attempting to optimise metallisation designs based on this approach.

The additional shadow loss from the incorporation of contact pads at the finger terminals is miniscule and can be neglected for optimisation calculations: 8 contact pads, each 150 x 200 μm in area along a 1cm^2 area cell incorporates a total fractional shadow loss of 0.0024 %.

This 'busbarless' approach can be taken to the extreme length: that of having no emitter busbar at all. Figure 6.6 shows a digital photograph of a 25 μm diameter Al wire-bond connected to a ~60 μm wide emitter finger. The head of the wire-bond is squashed due to the clamping action of the (wedge) wire-bonder, with an actual bonded area of ~40 x 80 μm.

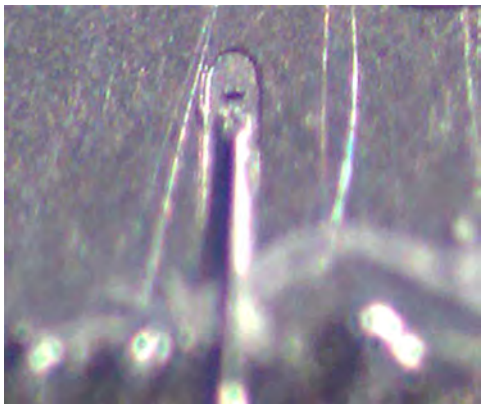


Figure 6.6: A 25 μm diameter Al wire-bond connected to a ~60 μm wide emitter finger. Individually bonding each finger of the device over an isolation groove completely removes the need for an emitter busbuar.

By connecting the terminal of every emitter finger over an isolation groove to an adjacent cell, the need for an emitter busbar is completely removed

- a true 'busbarless' cell. Note however, that for typical interdigitated devices the emitter finger spacing is on the order of 300 μm (see table 4.8 from the optimisation in chapter 4). Wire-bonding each of the emitter fingers will result in over 30 wire-bond connections per cm length of the device - likely beyond the feasibility of an industrially relevant metallisation scheme. However, it is clear that enormous reductions in shadow and resistive power loss by implementing such a scheme.

6.3.6 Wire-bonding: Applications

The previous sections outline the gains in FF and efficiencies from applying wire-bonds to pre-metallised devices, whilst design and optimisation of wire-bonded cells have been discussed in this section. It is worth mentioning the application of wire-bonding to larger area modules. Typical wire-bonding speeds of commercially available wire-bonders are on the order of 12 wire-bonds per second [101] with research efforts concentrating on surpassing 25 bonds per second [102].

In the future it would be desirable for glass superstrate sizes to be on the order of ~1m^2 or larger. For a 1m^2 module and a wire-bond spacing of 1 wire-bond per cm, it would take around 12 minutes to connect the ~7500 wire-bonds to interconnect the entire module. The cost of incorporating wire-bonders to interconnect metallised devices is not expected to be prohibitive compared to other equipment required for the deposition/processing of the cells, however the module-by-module processing may be restrictive in a production environment.

The author notes that the most preferred method for the interconnection of the thin-film PECVD silicon on glass devices discussed in this thesis would be to somehow incorporate the metallisation and interconnection within the one sequence. For example, via a common metal evaporation step as was attempted by Walsh [87].

6.3.7 Summary

Two potential metallisation layouts, one designed specifically for individual cell tabbing, and one for cell series-interconnection are presented. As the interdigitated structure of the devices is maintained, the power loss analysis developed in chapter 3, and applied for the optimisation of cells in chapter 4 is still relevant.

Only parameters need adjusting, otherwise the optimisation process previously shown can be used to analyse the power losses of these specially designed layouts.

Large reductions in both shadow and resistive power losses are possible with the proposed layouts, which serve only as an introduction to the wide variety of innovative and novel schemes possible when utilising tabbing and wire-bonding into the metallisation of devices. It is found using commercially available wire-bonders, it would take ~12 minutes to fully interconnect a $1m^2$ module, however the preferred interconnection scheme would be one that incorporates both metallisation and interconnection in the one step.

6.4 Chapter summary

Wire-bonding as an interconnection technique for poly-Si devices on glass is introduced, consisting of a laser scribe being used to electrically isolate the cells, followed by wire-bonding the busbars of adjacent cells across the isolation. Wire-bonded tabbing is also used at the terminal busbars to act as external contact leads for characterisation, as well as for the improved series resistance investigated in chapter 5.

The wire-bonding technique has been demonstrated to successfully interconnect both a two-cell and a four-cell thin-film poly-Si on glass mini-modules. The voltage of both mini-modules is greater than 98 % of the sum of the individual cells used. Current increases from a reduction in light leakage in the glass, in agreement with literature, is found for both mini-modules. In addition, the application of the white-paint encapsulation step is applied to the four-cell mini-module, and the combination of this step, together with the reduction of light leakage, results in an increase of over 8 % in short-circuit current for this device.

Increases of fill factors and efficiencies, in line with those found for tabbed individual cells are demonstrated, with the efficiency of the two-cell mini-module increasing from 7.77 % (average of the two cells) to 8.28 % for the mini-module. Similarly for the four-cell mini-module, efficiency increased from a cell average of 4.89 % to 5.63 %.

The consideration of wire-bond cell tabbing and interconnection into the cell design is presented. Cell metallisation layouts specially designed for individually tabbed cells, and series-interconnected cells are proposed.

These layouts result in considerable reductions in shadow and resistive power losses, and follow the interdigitated approach analysed in previous chapters. The optimisation and power loss analysis can still be used for characterising the new layouts. There is considerable scope for further innovating cell designs utilising wire-bonding for both cell tabbing and cell interconnection.

Chapter 7

Summary and conclusions

7.1 Summary

THIN -film poly-Si solar cells on glass, deposited by PECVD are a technology that combines the electronic stability of crystalline wafers, with the reduced cost and material requirement of thin-films. This thesis investigated the metallisation and post-metallisation processes carried out on thin-film poly-Si material. A summary of the key findings from each chapter is as follows:

In chapter 3, utilising the unit-cell approach and the introduced concept of flow current - the actual correct flowing through the poly-Si material, power losses for the interdigitated metallisation scheme are derived. The power losses differ substantially from those found in the literature for other metallisation layouts, in particular for the lateral resistance in the n^+ emitter layer, and the resistive loss of the emitter and airside fingers.

The absolute power losses are normalised to per-unit-area, which allows for a comparison of the relative contribution to the total power losses of the device. This allows for the optimisation of metallisation layouts, by minimising the sum of total power losses of the device.

Chapter 4 begins with a procedure for the self-aligned metallisation used to form interdigitated cells. The plasma-etched sidewall is identified as the vital processing step which causes large variations between the final FF of metallised cells. Using optical microscopy and FIB imaging, the sidewall profile as a function of plasma etching time is analysed. It is found that to maximise the FF of the device, a 'patchy' mixture of both glass and n^+ emitter material should be present in the emitter groove when viewed under an optical microscope. If the emitter has already been completely removed from the etch, the area should still be masked to protect it from further etching - there is a large etching-time gap of 3 - 4 minutes after the emitter has been removed, where reasonable devices can still be fabricated. Post-metallisation thermal annealing up to 200 °C is found to increase both the voltage and efficiency of thin-film PECVD cells. Annealing at higher temperatures (250+ °C) degrades the device.

The first metallised results of PECVD poly-Si cells on glass with an absorber deposited at a high-rate (~220 nm/min) are presented. The voltage and current across the four cells on the sample are stay relatively constant, indicating the film quality and uniformity is sufficiently high. Efficiencies of 4.8 % for cells without a BSR, and 5.9 % for cells with a BSR are reported. This investigation shows that one of the main disadvantages of PECVD - the slow deposition rate, can be overcome by

regulating the deposition pressure and/or RF power. Finally, a worked example for the optimisation of an interdigitated metallisation layout is given, showing the steps and justifications for approximations. It is found that optimal metallisation layouts exist that have about half of the power losses than for the 4.4 cm^2 devices investigated in this thesis.

In chapter 5, the challenge of interconnecting poly-Si devices on glass is presented. Wire-bonding/cell tabbing is proposed as a potential method and a variety of experiments are carried out on individual cells as a proof of concept. It is found that having 4 evenly distributed wire-bonds, connected the busbar to a strip of tabbing tape reduces the resistive loss of the busbar by over 90 %. With 16 wire-bonds, the resistive loss is further reduced to under 93 %.

Wire-bonds are found to cause a small amount of shunting along the air-side busbar of poly-Si cells, although the magnitude of the shunt (~5 Ω/wire-bond) has very little effect on device performance. It is entirely plausible that by optimising the wire-bonder settings (bond force, power, time, etc.) the effect on shunt can be reduced or even eliminated.

By sequentially increasing the number of wire-bonds connections from cell busbars to tabbing tape, the FF of the device continues to rise with up to 32 wire-bonds connected (8/cm). This confirms that any increase in shunt resistance from the addition of wire-bonds has a negligible effect on FF, compared to the reduction in series resistance. The application of white paint as an encapsulation results in planarising of the airside cell surface, to protect the wire-bonds from handling and the environment.

Additionally, a small current gain was noted, due to the white paint coating the sides of the glass superstrate, scattering some light back into the cells. The thermal stability of wire-bonds on tabbing tape is investigated and the optimal anneal temperature is found to be 150 °C. This does not conflict with the optimal anneal temperature found for non-tabbed cells (200 °C), as recommended practice is to anneal cells at 200 °C before wire-bond tabbing, then anneal at 150°C after tabbing.

Lastly, the wire-bond/tabbing technique is applied to high FF and high efficiency metallised cells. This resulted in the formation of a tabbed cell with a FF of 74.68 %, the highest-yet FF reported for poly-Si on glass cells at UNSW and possibly the highest ever reported for thin-film poly-Si cells. In addition, a tabbed cell with an efficiency of 8.05 % is fabricated.

In chapter 6, the wire-bond tabbing process is expanded to produce series-interconnected mini-modules. The interconnection and tabbing results in large gains in device current and FFs, due to both a reduction of leakage light lost and reduced series resistance from the interconnection and tabbing. An 8.28 % two-cell mini-module is obtained, where the average efficiency of individual cells prior to interconnection was 7.77 %. Finally, both wire-bond interconnection and white paint encapsulation is combined onto produce a four-cell mini-module, where again large increases in FF (from a cell average of 63.53 % to 69.16 % for the mini-module) and efficiency (4.89 % to 5.63 %). The wire-bonding technique, both for the tabbing of individual cells, and for cell interconnection is found to be a promising technique for thin-film poly-Si solar cells on glass.

7.2 Original contributions

The author's main contributions to the advancement of the metallisation and interconnection of thin-film poly-Si material on glass superstrates are as follows:

- Introduction of the flow current concept applied to the power loss analysis of interdigitated thin-film solar cells.
- Application of the unit cell approach to derive power loss formulas for the unique interdigitated cell on glass metallisation scheme.
- A more detailed demonstration than that previously published of the self-aligned metallisation process used to form interdigitated poly-Si devices.
- Investigation of the plasma-etching step and its influence on both sidewall formation and series/shunt resistances in metallised devices.
- Demonstration of increase voltage (>10 mV) and efficiency (up to 0.15% abs.) of metallised PECVD cells resulting from a post-metallisation thermal anneal step for 30 minutes at 200 °C.
- Successful metallisation of diodes deposited using high-rate PECVD - the first ever reported for thin-film poly-Si high-rate absorber cells on textured glass.
- Demonstration of high FF (72.96 %) and high efficiency (5.9 %) on from the metallisation of devices with a high-rate absorber.

- Introduction of the concept of wire-bonding metallised individual thin-film on glass cell busbars to external tabbing tape.
- It is found that the application of wire-bonds to the airside busbars of metallised PECVD devices induces a small (~5 Ω per wire-bond) decrease in cell shunt resistance. No such decrease is found when wire-bonding to the emitter busbars.
- Introduction of theory suggesting >90 % of resistive power losses in busbars can be eliminated by the application of 4 wire-bonds evenly spaced along the busbar, increasing to >97 % for 16 wire-bonds.
- Confirmation of this effect is found by the fabrication of a tabbed cell (32 wire-bonds) with a series resistance of 1.18 Ωcm^2, the lowest to date for a thin-film poly-Si glass fabricated at UNSW.
- Demonstration of white-paint encapsulation to both planarise the airside of wire-bond tabbed cells, as well as provide a small boost in cell current of planar cells, on the order of ~0.1 to ~0.3 mA/cm^2, depending on the cell's location on the superstrate.
- Demonstration of the thermal stability of both the wire-bonds and tabbing tape up to an anneal temperature of 150 °C, where both increased voltage (~8 mV) and device efficiency are found to result from the anneal. The tabbing process is detrimental at higher anneal temperatures.
- Proof of concept for wire-bond tabbing on single cells, together with notable improvements in FF and efficiency resulting from the tabbing process:

- Cell tabbing of a 74.7 % FF device (73.0 % prior to tabbing), is presented - the highest reported for a thin-film poly-Si cell fabricated at UNSW and possibly ever reported for thin-film poly-Si on glass.
- Cell tabbing of a 8.05 % efficient device (7.62 % prior to tabbing), among the highest for thin-film poly-Si cells on glass fabricated at UNSW.
- Successful demonstration of the wire-bonding interconnection technique. The technique has been used to fabricate an 8.28 % efficient two-cell mini-module, and a 5.63 % efficient four-cell mini-module.

7.3 Outlook

The work presented in this thesis is only a small part of the possible improvements, modifications and simplifications possible for the metallisation and interconnection of thin-film poly-Si solar cells on glass. Presented below are some areas where the author believes further research efforts are warranted:

- For the standard self-aligned metallisation, the airside Al electrode is traditionally over-etched for 40 seconds during the phosphoric etch step. For a more complete understanding of the sidewall formation, the author believes it is worthwhile to investigate the effect of both no over-etching, and heavily over-etched Al electrodes. It is suspected the airside Al electrode acts as a secondary mask beneath the primary photoresist etching mask.

- Reasonable voltages of up to 487 mV, and FFs of almost 73 % were obtained on material with an absorber deposited by high-rate (~220 nm/min) PECVD. As the slow deposition rate of PECVD is seen as a major drawback of the technology, the author believes the potential of this deposition method is immense and should be the subject of further research efforts.

- From the optimisation carried out in chapter 4, it is found that metallisation layout used to produce the (4.4 cm^2 cell area) cells in this thesis have slightly more than double the fractional power loss for optimised, 1 cm^2 area cells. There is considerable scope for improved device efficiencies by the utilisation of optimised metallisation layouts.

- Throughout chapter 4 and 5, a various of post-metallisation treatments were investigation, including thermal annealing (once before and once after wire-bonding), the application of tabbing tape/cell interconnection, and white-paint encapsulation. The author notes that on no device were all four post-metallisation treatments carried out - the relative and cumulative effect on each would certainly be of interest.

- At the end of chapter 6, two metallisation layouts are proposed that make use of the wire-bonding tabbing and interconnection technique. These devices have significantly reduced power losses from the reduction or even complete elimination of busbar area. A large range of alternative schemes are possible with even lower power losses. This is limited only by the imagination of the reader.

- The self-aligned metallisation scheme outlined in 4 contains a least one lithography step, and two Al deposition steps. It is a worthwhile research goal to simplify this metallisation scheme, both for faster metallisation of laboratory cells, and for the push towards industry-relevant metallisation schemes.

Nomenclature

Abbreviations and terminology

AIT Aluminium induced texture

BFG Borofloat glass

BSF Back surface field

BSR Back surface reflector

CSG Crystalline silicon on glass

DI De-ionised

FF Fill factor

FIB Focused-ion beam

IBC Interdigitated back contact

ITO Indium-tin oxide

PECVD Plasma-enhanced chemical vapour deposition

RTA Rapid thermal anneal

SPC Solid-phase crystallisation

SWE Staebler-Wronski effect

TCO Transparent conductive oxide

TLM Transmission line measurement

Symbols (section 3.2)

$\rho_{s,b}$ Busbar sheet resistivity

$\rho_{s,em}$ Emitter layer sheet resistivity

$\rho_{s,f}$ Finger sheet resistivity

A Busbar length

B Cell width

J_{MP} Current density at maximum power point

S Finger to finger distance

V_{MP} Voltage at maximum power point

W_b Busbar width

W_f Finger width

Symbols (remainder of thesis, if different from above)

ρ_c Specific contact resistance

A Distance from the edge of the cell to the current extraction point (i.e. half the cell length)

A_n Half the distance between wire-bond connections, equal to A/n where n is the number of wire-bonds used.

B Emitter finger length

I_{SC} Short-circuit current

J_F Flow current

J_{SC} Short-circuit current density

n^+ Highly doped n-type silicon

p^+ Highly doped p-type silicon

p^- Lightly doped p-type silicon

R_{SH} Shunt resistance

R_S Series resistance

V_{OC} Open-circuit voltage

W_A Airside busbar width

W_E Emitter busbar width

W_F Emitter finger width

Publications

Conference papers

- A.G. Aberle, P.I. Widenborg, P. Campbell, A. Sproul, M. Griffin, O. Kunz, J.W. Weber, B. Beilby, D. Inns, M. Terry, T. Walsh, S. He, C.Y. Tsao, Z. Ouyang, J. Wong, B. Hoex, L. Shi, T. Sakano, M. Wolf, J. Huang, G. Jin, L. Huang, S. Peng, M. Lang, D. Schmunk, F. Bamberg, S.V Chan, J. Han, T. Rouf, O. Berger, D. Di, A. Fattal, **P. Gress**, M. Pelletier, E. Mitchell, Y. Zhou, F. Fecker and S. Pohlner. Poly-Si on Glass Thin-Film PV Research at UNSW. In *22nd European Photovoltaic Solar Energy Conference*, pages 1884-1889, Milan, Italy, 2007.

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Patents and patent applications

Numerous full and provisional patent applications in various jurisdictions under the general title of:

A.G. Aberle, P.W. Widenborg, **P.J. Gress**, *Thin-film solar cell interconnection*.

- Australia Provisional Patent Application No. 2008903093 (filed 17/6/08).

- Patent Cooperation Treaty (PCT) Application No. PCT/SG2009/000213, Publication No. WO/2009/154575 (filed 19/6/09, published 23/12/09).

- Taiwan Patent Application No. 098120070, Publication No. 201010112 (filed 16/6/09, published 1/3/10).

- China Patent Application No. 200980122980.X, Publication No. CN 102150284 A (filed 17/12/10, published 10/8/11).

- European Patent Application No. 2009766958.4, Publication No. EP 2 291864 A0 (filed 16/6/09, published 3/9/11).
- US Patent Application No. 12/999160, Publication No. US 2011/0214714 A1 (filed 15/12/10, published 8/9/11).

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