AN INTEGRATED SWITCHED-CAPACITOR N-PATH FILTER WITH DECIMATION AND INTERPOLATION FILTERS

by

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CERTIFICATION

This thesis has not been submitted by the undersigned for a higher degree to any other universities or institutions.

Signed

Arpakorn Kasemsuwan

To my beloved parents
and the memory of my grandfather

ABSTRACT

Consider the design of bandpass switched-capacitor (SC) filter for a very high Q. None of the conventional SC filters, including SC ladder filters are suitable for this purpose, due to their high sensitivities to the element value variations and the practical op-amp gain specifications.

The switched-capacitor N-path filter is a better solution, since the overall sensitivities are identical to the individual lowpass cell of each path.

The design of SC bandpass N-path filter is presented. As the N-path filter produces the undesirable additional passbands, the design also includes corresponding band-stop filters.

In a switched-capacitor system, an antialiasing filter (AAF) is required to confine the input frequency. The specifications of AAF are related to the sampling frequency of the SC system. In order to have a low order AAF, the sampling frequency of the SC system should be relatively high. The gain bandwidth product of the op-amps put a limit on the sampling frequency as the op-amp's unity gain frequency needs to be five times higher than the clock frequency (f_c), otherwise distortions occur in the frequency response.

A solution is to add a "cosine decimator" between the AAF and the SC system. Such a cosine decimator has been developed and tested. The theory and implementation of a cosine decimator with the SC bandpass N-path filter is also discussed.

The smoothing filter (SMF) at the output of the SC filter also imposes a lower limit on the sampling frequency similar to AAF. A solution is to add an "interpolator" between the SC system and the SMF.

An interpolation circuit is presented. The theory and implementation the interpolator with the SC bandpass N-path filter is discussed.

A passive bandpass SC 4-path filter, including the bandstop filters has been developed. The measured Q is about 320. In order to simplify the requirements of the smoothing filter, a CMOS SC bandpass 6-path filter, including the band-stop filters is built on the chip.

The system comprising of cosine decimator, 4-path filter and interpolator has been tested. The measurement results are in good agreement with the theory.

ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to my supervisor, Professor G. A. Rigby for his encouragement and instructions.

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Lastly, I would like to express my gratitude to my uncle for his support and my parents for their sacrifices.

CONTENTS

CHAPTER 1

INTRODUCTION

In this chapter, the basic concept of a switched capacitor which performs as a simulated resistor is introduced. Then, the comparison between an analog RC-active filter and a switched capacitor filter will be briefly discussed.

The problem of sensitivity to the parameter variations of a switched capacitor filter at high Q-poles and the solution to overcome this problem will also be briefly discussed.

At the end of this chapter, some switched capacitor systems that can be added to simplify the requirements of some RC active lowpass filters, which are needed for antialiasing and band-stop functions in sampled data systems, will also be briefly presented.

1.1 THE LIMITATIONS OF USING AN RC ACTIVE FILTER.

It is desirable when realising filters in microelectronics form to place all components on a chip. This reduces cost, pin-count and board area. But, there are some major problems that arise when RC active filters are used, namely,

(a) Very large chip area is needed by the RC components.

(b) The accuracy and stability requirements for these components can not be satisfied by integrated components. Consequently pole/zero variations are too large for most applications.

An effective method which can solve both problems is to replace each resistor in the circuit by a combination of capacitor and MOS switches. Consider a branch shown in Fig. 1.1.

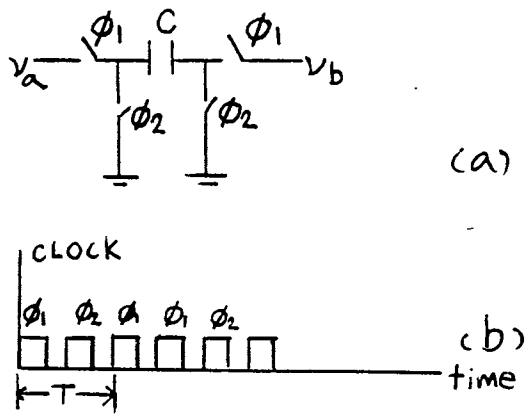


Fig. 1.1. a) Switched capacitor realization of a resistor branch.
b) Non-overlapped clock signals.

When switch ϕ_2 closes, capacitor discharges. By closing switch ϕ_1 and opening switch ϕ_2 , a charge (ΔQ) is caused to flow from v_a to v_b for every clock period T. Thus the average branch current is

$$i_{av} = \frac{q}{T} = \frac{C}{T}(v_a - v_b) \qquad (1.1)$$

i_{av} in (1.1) is proportional to the branch voltage $v_a - v_b$. Similarly for a branch containing a resistor R, the branch current (i) equals to $\frac{1}{R}(v_a - v_b)$. Thus , the average current flows are the same if the condition $R = \frac{T}{C}$ holds.

In an active RC filter, all resistors can potentially be replaced by this branch. Consequently, some major advantages arise as follows:

(a) All time constants, previously determined by the poorly controlled RC product, will be the expression of the form $(\frac{T}{C_1})C_2 = T(\frac{C_2}{C_1})$, where T is the clock period and $\frac{T}{C_1}$ represents a simulated resistor.

(b) The clock signal can be controlled very accurately, eg. by a quartz-crystal oscilator.

With these two major advantages, the overall accuracy and stability can be improved by hundred times compared to that of an on chip resistor and capacitor implementation.

(c) Coefficients in the transfer-function polynomial depend on capacitor ratios - not

absolute value - and these ratios can be controlled to 1% or better in IC technology.

1.2 CONSIDERATION OF BANDPASS FILTER WITH HIGH-Q POLE

Several techniques that have been developed to design switched-capacitor filters, such as cascading the first- and second-order sections of a switched capacitor filter and a well known technique called "switched capacitor ladder filters" which has the low-sensitivity properties of a doubly terminated reactance two-port network.

These techniques cannot be applied to a high Q bandpass filters because they are still too sensitive to the op-amp gain effects, stray and element-value variations. The reason is that in such filters, the transfer function H(z) usually contains poles very close to the unit circle in the z-domain, then the response that is considered at high Q poles is very sensitive to the element-value variations.

From the above problem, it apparently shows that at high Q, conventional switched capacitor bandpass filters cannot achieve the goal of having low sensitivity to the element value variations.

A possible solution seems to lie in the use of N-path switched capacitor bandpass filter concept. The properties of this solution that are attractive are given as follows:

First of all, let us consider the comparison between bandpass filter and lowpass filter with identical bandwidths as well as passband and stopband specifications. The relationship between pole-Q of the dominant poles of bandpass filter and lowpass filter is:

$$Q_{bp} \sim (2\frac{\omega_o}{B})Q_{lp} \qquad (1.2)$$

where ω_o = the center frequency of bandpass filter

B = bandwidth of bandpass filter.

At high Q_{bp} , bandpass (high ω_o,low B), Q_{bp} will be much higher than Q_{lp}. Consequently, the overall response of high pole Q_{bp} bandpass filter will become too sensitive to the element value variations when compared to a lowpass one.

The most important reason of using N-path filter is that the sensitivities to the element-value variations of the overall N-path filter is the same as each path filter acting alone. Since the latter is a lowpass filter, its pole-Q's Q_{lp} are low, and hence, its sensitivities can also be made

low. Thus, the sensitivities of the overall N-path filter are lowered by a factor $\frac{Q_{bp}}{Q_{lp}} \sim \frac{2\omega_o}{B}$, as shown in Equ (1.2).

From the above explained advantage, if a bandpass filter that has pole-Q at 100 is considered, by using N-path filter the sensitivities of the overall N-path filter will be equal to the sensitivities of a lowpass filter of each path, which is proportional to $Q_{lp} = \frac{BQ_{bp}}{2\omega_o} = \frac{B}{2\omega_o}100$. (If $\frac{B}{2\omega_o} = \frac{1}{100}$, then Q_{lp} at each path will be 1, so the sensitivities of the overall N-path filter will be lowered by a factor of 100.)

The other major advantage of the N-path SC bandpass filter is that the centre frequency can be controlled very accurately by a quartz-crystal oscillator.

The frequency response of the SC N-path filter is periodic. To convert the SC N-path filter to a bandpass filter, the additional bandstop filters, which suppress undesirable passbands, are required.

A passive SC 4-path filter and bandstop filters will be designed in Chapter 4. In Chapter 6, their operation together will be tested.

The main problem of the SC bandpass filter is the path mismatch. If all the paths are symmetrical, the clock feedthrough noise, which is introduced from each switch, will form a polygon with zero resultant at the output. In Chapter 4, some techniques are introduced to reduce the effects of the path mismatch.

1.3 PREFILTERING REQUIREMENTS FOR A SWITCHED-CAPACITOR FILTER.

A switched capacitor filter is a sampled data system. For the sampled data system, unless the Nyquist's criterion is satisfied , the aliasing effect causes out-of-band signals to appear in the passband, thus antialiasing filter is required to confine the input frequency range.

The complexity of antialiasing filter depends on the sampling frequency. If the sampling frequency is high, the requirements for the antialiasing filter become less complex.

In practice, the sampling frequency cannot be too high because of the limitations of some components such as op-amps [Ref. 4]. A requirement of the op-amps is that the sampling frequency has to be low enough so that op-amp has enough time to settle, or it will cause non-linear distortion at the output signal. We then have to compromise the requirements of the op-amp and the antialiasing filter.

Due to the above mentioned problem, an additional sampled data system can be used to simplify the complexity of both the op-amp and the antialiasing filter. This addtional sampled data system is called "decimator" [Ref. 18].

The basic concept of a decimation filter is that it is designed to have its stopband frequency the same as the frequency band of the input signal, where aliasing occurs, to suppress this effect.

The design of a decimator will be described in Chapter5. In Chapter6, the decimator will be presented for operation with a passive SC 4-path filter. Test results will also be given in this chapter.

Consider the output of a sampled data system, the frequency spectrum is periodic at nf_s where n = 0, 1, 2, 3,...and f_s = the sampling frequency. In order to obtain a continuous-time signal, a lowpass filter is needed to eliminate the unwanted frequency bands. This lowpass filter is often called a smoothing filter.

The complexity of a smoothing filter also depends on the sampling frequency. The higher the sampling frequency is, the requirements of smoothing filter will become less complex. In practice, the sampling frequency of the sampled data system cannot be too high as we have already discussed at the beginning of this section.

From the above mentioned problem, an additional sampled data system is needed to simplify the requirements of the smoothing filter. This sampled data system is called an "interpolator" [Ref. 11, 19]. The basic concept of an interpolator is that it will interpolate the sampling frequency to the output sampled signal in such a way that the sampling frequency of the output sampled signal is increased.

In Chapter 5, the interpolation filter will be designed to co-operate with the passive SC 4-path filter and the cosine decimation filter. The measurements and results will be shown in Chapter 6.

By using the above additional sampled data system, we can save a large chip area that is required to construct high order of an antialiasing filter and a smoothing filter.

The outlines of each chapters are given as follow:

In Chapter 2, the switched-capacitor filter is analysed as a sampled-data system, but the process of understanding how it performs can be simplified by the transformation from a sampled-data system to a digital system. A brief fundamental background of the digital simulation of the analog systems will be given in this chapter. Some transformations in both

the time and frequency domains will be compared. The output waveform of switched-capacitor filter is a sampled and held signal, so the distinction between sampled signal and sampled and held signal will also be presented in this chapter.

In Chapter 3, some switched capacitor configurations that can overcome the problem of sensitivities to the parameter variations are presented. At the end of this chapter, a technique called "switched-capacitor N-path filter" will be presented.

In Chapter 4, the concepts and the design of a passive switched capacitor 4-path filter and bandstop filters will be detailed. At the end of this chapter, some techniques that are used to overcome the path mismatch will be briefly presented.

In Chapter 5, the concept and the design of decimation and interpolation filters are detailed. The co-operation between the 4-path filter, a cosine decimator and an interpolator will be detailed. The testing result will be shown in Chapter 6.

In Chapter 6, all of switched-capacitor N-path filter, decimation and interpolation filters are combined, tested and compared with the theoretical prediction. The layout of a switched-capacitor bandpass 6-path filter will be shown and the test results of the chip will be given.

In Chapter 7, the conclusion of the fundamental principle of SC N-path filter will be summarized. The test results of SC 6-path filter on the chip and the co-operation between the 4-path filter, a cosine decimator and an interpolator will be concluded.

CHAPTER 2

DIGITAL, ANALOG AND SAMPLED DATA SYSTEMS

INTRODUCTION

The switched-capacitor filter is classified as a sampled-data system, which is closely related to digital systems, hence, the fundamental understanding of the digital simulation of the analog system is essential.

In section 2.1, a type of transformation in the time domain, which is known as matched s to z transform [Ref. 13,15], from an analog to a digital system is described. This transformation can efficiently preserve both loss and phase response at the passband and stopband. At the end, the disadvantages of the matched s to z transformation will be given.

In section 2.2, in practice, the output waveform of the switched-capacitor filter is a sampled and held signal, and the distinction between sampled signal and sampled and held signal will be studied in this section.

In section 2.3, the effect of aliasing, which has an important role for sampled-data and digital systems, will be described. This section is needed as a fundamental background to understand the design of decimation and interpolation filters, which is described in Chapter 5 and Chapter 6.

In section 2.4, the relation between a sampled-data system and a digital system will be discussed [Ref. 15]. A method of simulating a switched-capacitor circuit, which is a sampled-data system, by a digital system is given. The concepts of this section will be used throughout the thesis.

In section 2.5, the transformation in the frequency domain from an analog to a digital system will be discussed. Some well-known transformations such as the bilinear and LDI transformations [Ref. 22], which can preserve loss response at the passband and stopband, will be compared to each other.

2.1 DIGITAL SIMULATION OF ANALOG SYSTEM IN THE TIME DOMAIN.

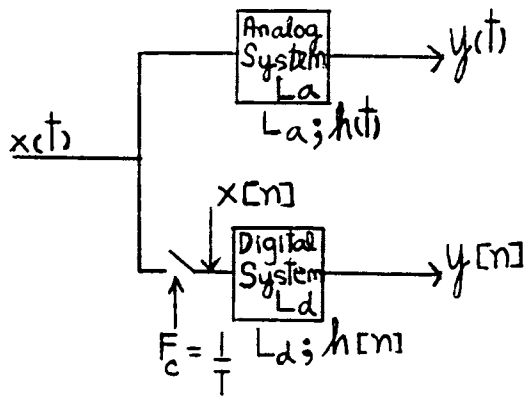


Fig. 2.1. Representation of a mixed analog (L_a)/simulated analog (L_d) system.

In Fig. 2.1. we show an analog system (L_a) and a digital system (L_d). The input to the analog system is a continuous-time signal x(t), and the input to the digital system is a discrete-time signal x[n] such that:

$$x[n] = x(nT) \qquad (2.1)$$

where x(nT) is the samples of x(t) with the sampling frequency equal to 1/T.

We shall say that the system L_d is a digital simulator L_d if its output y[n] equals the samples of the output y(t) of L_a at time nT:

$$y[n] = y(nT) \qquad (2.2)$$

There are two types of simulators (using a digital system L_d to simulate an analog system L_a)

1 Simulation in the frequency domain. This type of simulation will be mentioned in the following section, and it also will lead to some well-known s to z transformations.

2 The time sampling method of simulation (simulation in the time domain).

Consider briefly how to simulate L_a by L_d in the time domain. (matched s to z transformation)

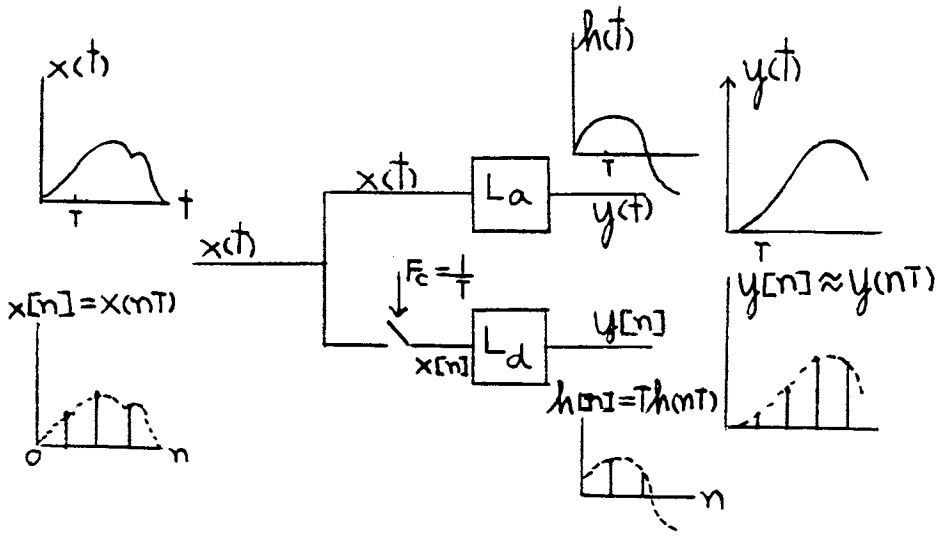


Fig. 2.2. Representation of a time sampling method of simulation.

As we know the output y(t) of any analog system can be represented by the integral:

$$y(t) = \int_0^\infty x(t-m)h(m)dm \qquad (2.3)$$

where x(t) is the continuous-time input signal.

h(t) is the impulse response of the system.

For a given t the integral in(2.3) is the area under the curve:

$$w(m) = x(t-m)h(m) \qquad (2.4)$$

where the variable of integration is m . It is well known from the theory of integration that this area can be approximated by a sum:

$$\int_0^\infty w(m)d(m) = T(w(0)+w(T)+.....+w(kT)+....) \qquad (2.5)$$

inserting(2.5)into(2.3), we obtain

$$y(t) = y_t(t)$$

where $y_t(t)$ = T[x(t)h(0)+x(t-m)h(m)+.....+x(t-kT)h(kT)+.....] (2.6)

(where $y_t(t)$ represents the output of the analog sampled data system)

We have approximated the integral in(2.3) by the sum $y_t(t)$ in(2.6). We shall show in this section that $y_t(t)$ is the output of an analog system consisting only of delay elements and multipliers. This system will be called a sampled data system.

By setting t = nT in(2.6) we obtain (T = the sampling period)

$$y_t(nT) = \sum_{k=0}^{k=\infty} \text{Th(kT)x(nT-kT)} \qquad (2.7)$$

The above sum is equal to the output y[n] of a digital system with input x[n], and the impulse response is equal to the samples

$$h[n] = Th(nT) \qquad (2.8)$$

of Th(t) of analog system. This system is the digital simulator L_d of the analog system L_a, and its system function is the sum.

$$H(z) = T \sum_{n=0}^{n=\infty} h(nT)\, z^{-n} \qquad (2.9)$$

The approximation of the convolution integral in (2.3) by the sum in (2.6) leads to the approximation:

$$y_t(nT) = y[n] \qquad (2.10)$$

A digital simulator can be constructed from a given analog system by simulation in the time domain, firstly the analog system is transformed to a sampled-data system. Then, this sampled-data system is transformed to the desired digital simulator.

The above process is called the time-sampling method of simulation. The conclusion is explained pictorially in Fig. 2.2. This type of transformation from an analog to a digital system in the time domain can be called the " impulse-invariant design method " or " matched s to z transform ". As the name implies, the impulse response of the digital simulator, which is used to simulate the continuous-time filter, is the same as the impulse response of the continuous-time filter at each sampling instant.

In this technique, the zeros and poles of $H_a(s_a)$ of the analog system L_a are duplicated at the same location in the s-plane, which is the Laplace variable domain of the sampled-data system.

The mathmatical expression is illustrated below:

Consider Fig. 2.2.

The impulse response of the continuous-time filter is h(t).

The impulse response of the digital filter which is used to simulate continuous-time filter is h[n] = Th(nT), where h(nT) is the samples of the continuous-time impulse response of analog system L_a so,

$$h(nT)=h(t)*\sigma_T(t) \qquad (2.11)$$

where $\sigma_T(t) = \sum_{n=-\infty}^{n=\infty} \sigma(t-nT)$ $\sigma(t)$ = impulse function (2.12)

We can expand $\sigma_T(t)$ as a Fourier series, that is

$$\sigma_T(t)= \sum_{n=-\infty}^{n=\infty} Cne^{jn\omega_s t} \qquad (2.13)$$

where $Cn = 1/T \int_{-T/2}^{T/2} \sigma(t)e^{-j\omega_s t}dt$ (2.14)

and ω_s is the angular sampling frequency equal to $2\frac{\pi}{T}$ rad/s. Since the area of the impulse function is unity, then

$$\int_{-T/2}^{T/2} \sigma(t)e^{-jn\omega_s t}dt = 1$$

and therefore Cn = 1/T,hence (2.13) can be rewritten as illustrated below:

$$\sigma_T(t)=1/T\sum_{n=-\infty}^{n=\infty} e^{jn\omega_s t} \qquad (2.15)$$

We substitute (2.15)into(2.11)

$$\text{so } h(nT) = 1/T \sum_{n=-\infty}^{n=\infty} h(t)e^{jn\omega_s t} \qquad (2.16)$$

Now taking the Laplace-transforms and using the associated shifting theorem we obtain:

$$\pounds[h(nT)]=1/T\sum_{n=-\infty}^{n=\infty} H(s-jn\omega_s)$$

$$\pounds(h[n])=\pounds[Th(nT)]=\sum_{n=-\infty}^{n=\infty} H(s-jn\omega_s) \qquad (2.17)$$

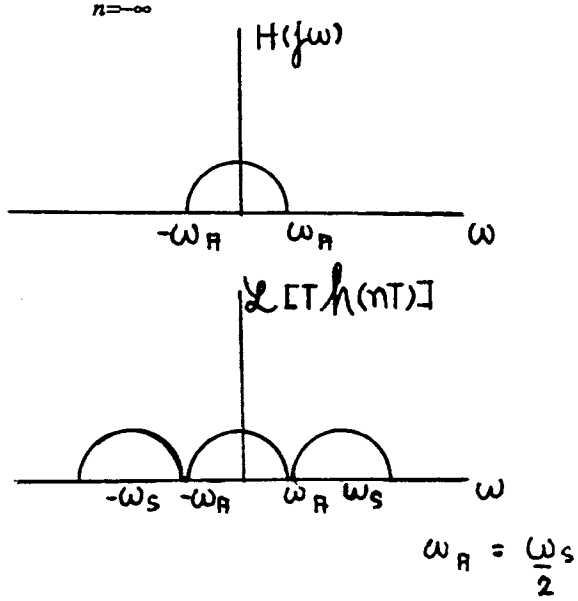


Fig. 2.3. (a) Frequency response of the transfer function of an analog system L_a .

(b) Frequency response of the transfer function of a sampled data system which is used to simulate L_a by using matched s to z transformation.

From (2.17) indicates that the impulse response of a sampled data system that is

transformed from L_a to L_d by "impulse invariant design method", has an infinite number of complementary frequency spectra, which means that there must be an infinite number of associated pole-zero patterns in its s-plane representation.

This can be explained pictorially as illustrated below:

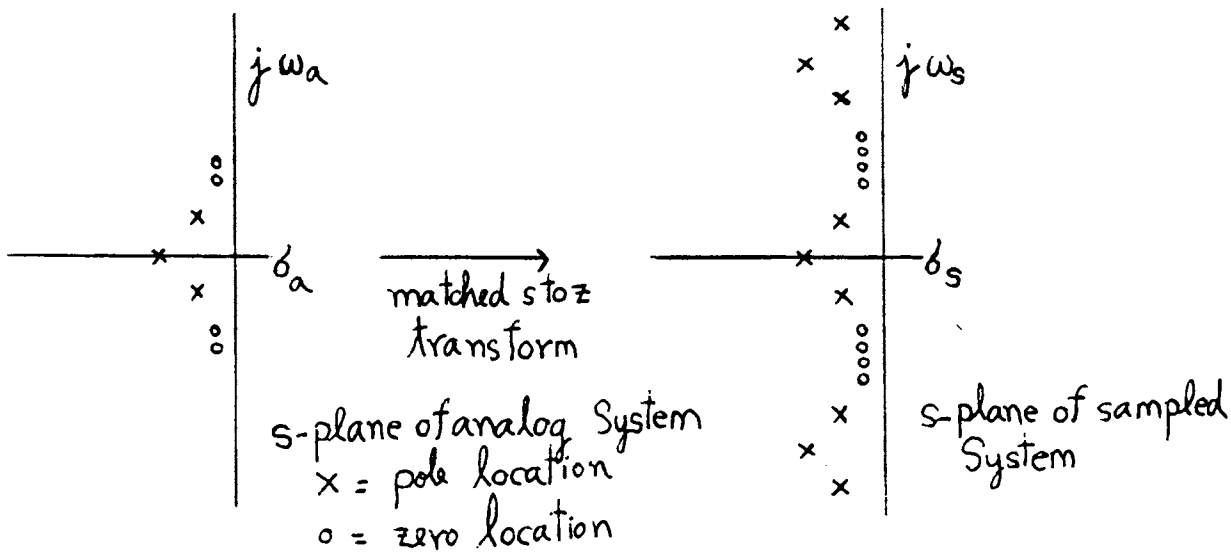


Fig. 2.4. (a) Locations of poles and zero of an analog system L_a.

(b) Locations of poles and zero of a sampled data system which is used to simulate the operation of the above analog system by matched s to z transformation.

The advantage of this method is that for narrow-band filters (lowpass or bandpass), it preserves both the loss and phase response in and near the passband.

In designing and implementing impulse-invariant digital filters, care must be taken to ensure that the value of the sampling frequency does not produce unacceptable aliasing errors. In order to avoid unacceptable errors, the frequency response of the filter has to be insignificant above $\frac{f_s}{2}$ where f_s = sampling frequency. This is a disadvantage of this method. Consequently the impulse-invariant design method can be used to design non-bandlimited filter such as high-pass and bandstop. An alternative method is by using simulation in the frequency-domain such as a well known bilinear s to z transformation and lossless discrete integration (LDI) , which will be discussed in the section 2.5.

2.2 SAMPLED SIGNAL AND SAMPLED AND HELD SIGNAL

We will consider the relationships between a continuous-time signal f(t), a sampled signal $f_s(t)$ and a digital signal f[n].

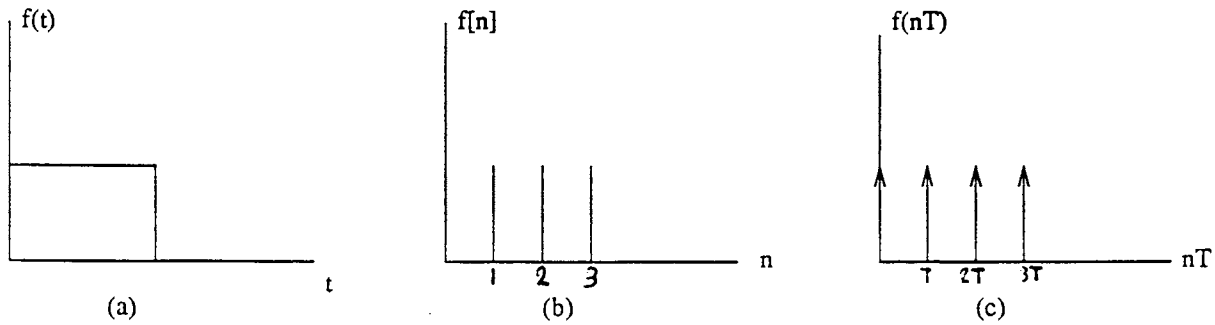


Fig. 2.5. (a) continuous-time signal
(b) digital signal
(c) sampled signal

Given a function f(t), we form a sequence.

$$f[n] = f(nT) \qquad (2.18)$$

obtained by sampling f(t), as in Fig. 2.5. We shall express the z-transform of the digital signal f[n] of Fig. 2.5(b):

$$F(z)=\sum_{n=0}^{n=\infty} f(nT)z^{-n} \qquad (2.19)$$

Consider Fig 2.5(c). This is a sampled signal of the continuous-time signal in Fig 2.5(a).

The mathmatical expression of the sampled signal Fig. 2.5(c) is shown below:

$$f_s(t)=\sum_{n=0}^{n=\infty} f(nT)\sigma(t-nT) \qquad (2.20)$$

A sampled data signal is a type of analog signal, so we can apply the Laplace transform to the sampled signal as illustrated below:

$$F_s(s)=\sum_{n=0}^{n=\infty} f(nT)e^{-nTs} \qquad (2.21)$$

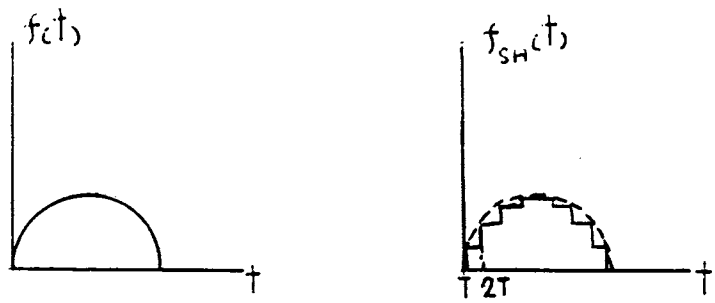
If in the above sum we replace the exponential e^{sT} by z, we obtain the z-transform F(z) of the samples f(nT) of sampled signal. This leads to the conclusion that:

$$F_s(s) = F(z) \qquad (2.22)$$

where $z = e^{sT}$

From (2.22), the Laplace-transform of a sampled data signal is equal to the z-transform of that signal in which the variable z is replaced by e^{sT}.

Consider a sampled and held signal



(a) (b)

Fig. 2.6 (a) A continuous-time signal

(b) A sampled and held signal of Fig. 2.6(a)

From Fig. 2.6(b), $f_{sh}(t)$ is the sampled and held signal of a continuous-time signal f(t) which is shown in Fig. 2.6(a).

The mathmatical description of sampled and held signal Fig. 2.6(b) is given below:

$$f_{sh}(t) = \sum_{n=0}^{n=\infty} f(nT)[u(t-nT)-u(t-nT-T)] \qquad (2.23)$$

The Laplace transform $f_{sh}(s)$ of $f_{sh}(t)$ is given below:

$$f_{sh}(s) = (1-e^{-sT})/s \sum_{n=0}^{n=\infty} f(nT)e^{-snT} \qquad (2.24)$$

Comparing (2.21) and (2.24), it is clear that the difference between the Laplace-transform of the sampled and the sampled and held signals is the factor:

$$H_{sh}(s) = (1-e^{-sT})/s \qquad (2.25)$$

2.3 THE SPECTRUM OF A SAMPLED - DATA SIGNAL

Consider the comparison between the frequency spectrum of continuous and sampled data signals. The Laplace transform of the continuous-time signal x(t) and the sampled data signal of x(t) are shown respectively again from (2.21).

$$F_a(s)=\int_0^{\infty} f(t)e^{-st}d(t) = F_a(j\omega) \qquad (2.26)$$

$$F_s(s)= \sum_{n=0}^{n=\infty} f(nT)e^{-snT}=F(e^{j\omega T}) \qquad (2.27)$$

To complete our objective, we shall use the following important identity known as the Poisson sum formula.

$$\sum_{n=0}^{n=\infty} Tf(nT)e^{-jn\omega T}= \sum_{n=0}^{n=\infty} F_a(j\omega+j2n\frac{\pi}{T}) \qquad (2.28)$$

Comparing with (2.27), we conclude that:

$$F_s(s)=F(e^{j\omega T})=\sum_{n=0}^{n=\infty} f(nT)e^{-snT}=1/T\sum_{n=-\infty}^{n=\infty} Fa(j\omega+j2n\frac{\pi}{T}) \qquad (2.29)$$

or

$$F_s(j\omega)=1/T\sum_{n=-\infty}^{n=\infty} F_a(j\omega+j2n\frac{\pi}{T}) \qquad (2.30)$$

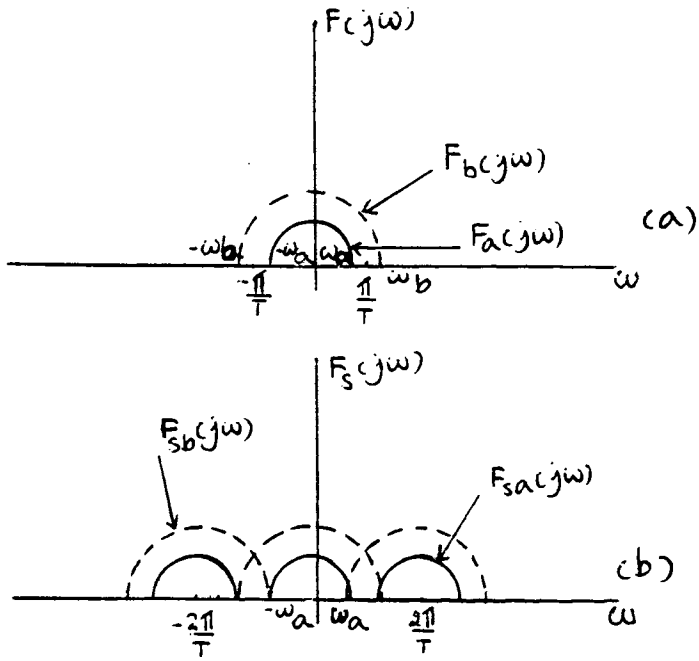


Fig. 2.7. (a) Frequency spectrum of continuous-time signals $F_a(j\omega)$ and $F_b(j\omega)$
(b) Frequency spectrum of sampled-data signals $F_{sa}(j\omega)$ and $F_{sb}(j\omega)$

Equation (2.30) has some very important implications. Consider the continuous-time spectrum $F_a(j\omega)$ in Fig 2.7. It is full band limited, that is, it vanishes outside the bound $-\omega_a$ and ω_a where $\omega_a < \frac{\pi}{T}$. Hence, when $F_{sa}(j\omega)$ is replicated with a repetition period $2\frac{\pi}{T}$ as dictated by (2.30), the replicas forming $F_{sa}(j\omega)$ do not overlap Fig. 2.7(b) Thus, there is one to one relation between the value of $F_a(j\omega)$ and $F_{sa}(j\omega)$.

By contrast, the tails of the broader spectrum $F_b(j\omega)$ extend beyonds the bounds $\frac{\pi}{T}$ Fig.

2.7(a) to ω_b . Thus when it is replicated (Fig. 2.7(b)), these tails overlap, and the value of $F_{sb}(j\omega)$ at any frequency is influenced by the value of $F_b(j\omega)$ at several different frequencies. This phenomenon is called aliasing or folding. It is a nonlinear distortion.

We conclude that if the sampling frequency $2\frac{\pi}{T}$ is larger than the twice the maximum frequency in the spectrum of the continuous-time signal, then no aliasing distortion will take place. The original spectrum can then be recovered undistorted from the sampled-signal spectrum by using a lowpass filter with a cut-off frequency $\frac{\pi}{T}$. If on the other hand, $2\frac{\pi}{T}$ is less than twice the band limit of the original signal, then aliaing occurs, and the continuous-time signal is irretrievably lost.

To avoid the aliasing, the condition of the sampling frequency (1/T) has to satisfy the following equation.

$$2\frac{\pi}{T} > 2\omega_a \qquad (2.31)$$

where T = The sampling period.

ω_a = The band limit of the frequency of the continuous-time signal. Equ (2.31) expresses the " Nyquist's criterion", while the lower bound $2\omega_a$ on the sampling frequency is called the Nyquist rate.

We now consider the comparison between the frequency spectrum of the continuous-time and the sampled and held signals,

Again from (2.24), the Laplace transform of sampled and held signal:

$$F_{sh}(j\omega) = \frac{(1-e^{-j\omega T})}{j\omega}\sum_{n=0}^{n=\infty} f(nT)e^{-jn\omega T} \qquad (2.32)$$

The Poisson sum formula (2.32) can be changed to:

$$F_{sh}(j\omega) = F_{sh}(s) = e^{-\frac{j\omega T}{2}}\frac{\sin(\frac{\omega T}{2})}{\frac{\omega T}{2}}\sum_{n=-\infty}^{n=\infty} F_a(j\omega+2n\frac{\pi}{T}) \qquad (2.33)$$

where

$$H_{sh}(j\omega) = \frac{(1-e^{-j\omega t})}{j\omega} = Te^{\frac{-j\omega T}{2}}\frac{(\sin(\frac{\omega T}{2}))}{(\frac{\omega T}{2})} \qquad (2.34)$$

$H_{sh}(j\omega)$ is often called " (sin x)/x response" and is the characteristic of sampled and held signal spectrum.

Next, the spectrum of the continuous-time signal will be compared with that of S/H signal obtained from it. Assuming that the Nyquist criterion (2.31) holds, the situation is as shown in Fig. 2.8.

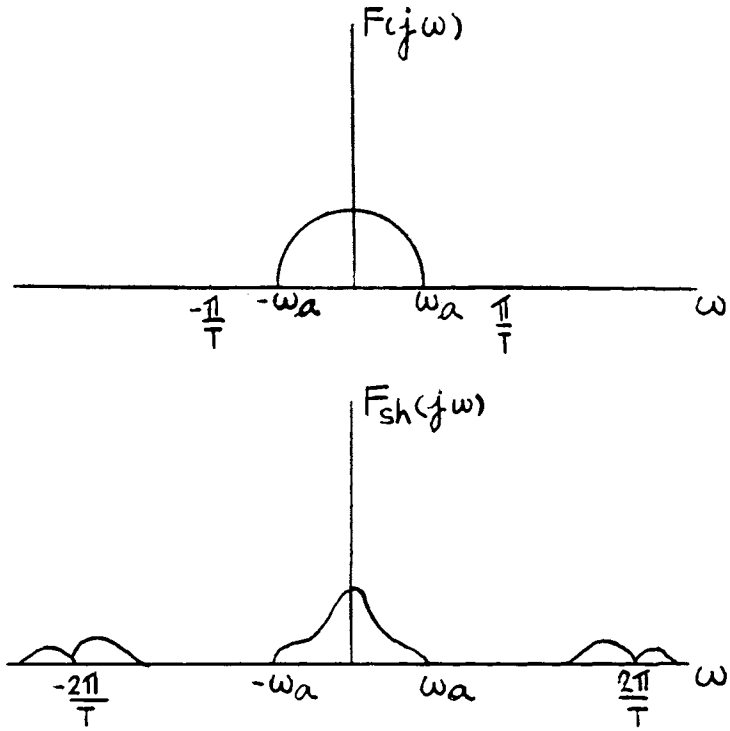


Fig. 2.8. (a) Frequency spectrum of the analog signal.
(b) Frequency spectrum of the sampled and held signal.

Comparing (2.33) and (2.29), $F_{sh}(j\omega)$ is replicated and multiplied by the "(sin x)/x response". As a result, the main lobe in $-\frac{\pi}{T} < \omega < \frac{\pi}{T}$ is no longer the same as (2.30), and the side lobes centered around $2\frac{\pi}{T}$, $4\frac{\pi}{T}$ are greatly reduced.

The distortion of the main lobe is simply due to the factor $H_{sh}(j\omega)$. It is linearly distorted as opposed to the nonlinear distortion which aliasing introduces.

In practice, the Nyquist criterion is often satisfied not simply by choosing the sampling rate $2\frac{\pi}{T}$ higher than ω_a, but rather by reducing ω_a. Thus, before sampling the continuous-time

signal, f(t) is passed through a lowpass filter (called an antialiasing filter) which reduces its bandwidth to the $-\frac{\pi}{T} < \omega < \frac{\pi}{T}$ range. In practice, the antialiasing filter is usually a continuous-time filter.

A schematic representation of a sampled-data system with continuous-time input and output signals is of the form shown in Fig. 2.9.

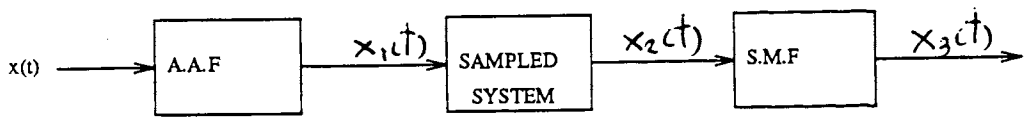
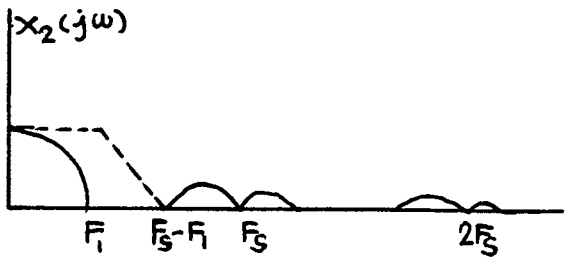


Fig. 2.9. Representation of a sampled – Data system.

x(t) represents the continuous-time input signal. The frequency spectrum of x(t) will become band-limited to be less than the Nyquist rate after it passes AAF in order to avoid aliasing.

$x_1(t)$ will be the band-limited output signal from the AAF then it will be processed by a sampled data system.

$x_2(t)$ will be the output of the sampled data system, so its frequency spectrum will be periodic as illustrated below:



F_s = sampling frequency.

Fig. 2.10. (a) The solid line represents the frequency spectrum of $x_2(t)$. (F_1 is the stopband frequency of $x_2(t)$.)

(b) The dashed line represents the frequency response of a smoothing filter (SMF). (F_s–F_1 is the stopband frequency of SMF.)

The centre of each lobe is at n F_s n = 0, 1, 2, 3...., where F_s is the sampling frequency of sampled data system. To convert $x_2(t)$ back to the continuous-time signal, a lowpass filter is needed to suppress the side lobes as illustrated by the dashed line in Fig. 2.10.

$x_3(t)$ will be the continuous-time signal with a little bit of irretrievable distortion at the passband due to the (sin x)/x response, which is a property of the sampled and held signal.

2.4 THE RELATION OF SWITCHED-CAPACITOR FILTERS, SAMPLED DATA AND DIGITAL SYSTEMS

Consider the relationship between a switched capacitor filter system, a sampled data system and a digital system. At the end of this section, an example of a switched capacitor circuit is given. We will analyze it as a sampled data system by using a digital system as a simulator.

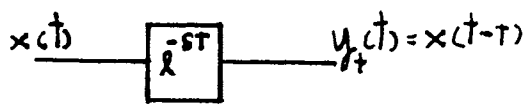
Switched-capacitor filters are sampled data systems, with analog signal representation. Hence their analysis requires, in general, the mathmatical tools of both analog signals (Laplace and Fourier transformations)and those of sampled signals, which are simulated by a digital signal(z-transform).

First, consider the characteristics of a sampled data system. (Note once again that the characteristics of the switched capacitor filter are the same as the sampled data system).

A sampled data system consists of multipliers and analog delay elements.

Delay element

$y_t(t) = x(t-T)$ $\quad y_t(s) = x(s)\, e^{-sT}$ $\quad H_t(s) = e^{-sT}$



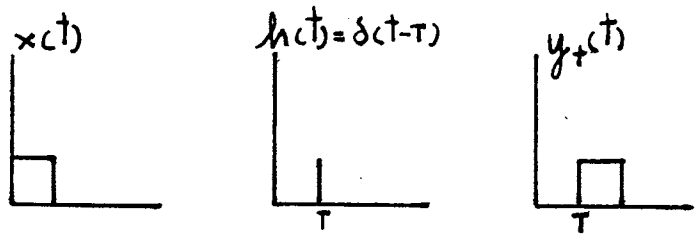


Fig. 2.11. A delay element of a sampled-data system.

The above figure shows that the system function of the delay element is an exponential.

$$H_t(s) = e^{-sT} \qquad (2.35)$$

and its impulse response a delayed impulse.

$$h(t) = \sigma(t-T) \qquad (2.36)$$

Now, we will consider an example of a switched capacitor filter, which is realized as a sampled data system, then we will use a digital system to simulate its operation.

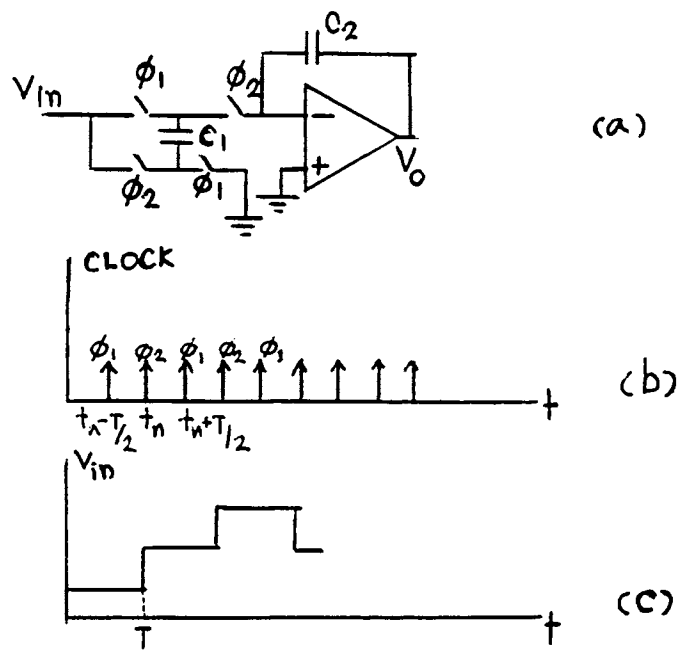


Fig. 2.12. (a) The switched capacitor integrator which simulates the operation of RC integrator by using bilinear transformation.

(b) the clock signals

(c) the input signal (We assume that the input is a sampled and held signal. It changes state when ϕ_2 goes high, then holds for one period of clock signal.)

Consider at $t = t_n$ when ϕ_2 is "on".

First consider at C_1

$$\Delta Q(t_n) = C_1 \Delta V(t_n)$$
$$= C_1 (V_{in}(t_n) + V_{in}(t_n - \frac{T}{2})) \quad (2.37)$$

From Fig. 2.12(c), $V_{in}(t_n - T) = V_{in}(t_n - \frac{T}{2})$, therefore Equ(2.37) can be rewritten as shown below:

$$\Delta Q(t_n) = C_1 (V_{in}(t_n) + V_{in}(t_n - T)$$

We now consider at C_2.

The charge $\Delta Q(t_n)$ at $t=t_n$ flows in to C_2, then:

$$\Delta V_{c2}(t_n) = \frac{\Delta Q(t_n)}{C_2}$$
$$= \frac{C_1}{C_2}(V_{in}(t_n) + V_{in}(t_n - T))$$

but $$\Delta V_{c2} = -\Delta V_0 = -(V_o(t_n) - V_o(t_n - T))$$

so $$V_o(t_n) = V_o(t_n - T) - (\frac{C_1}{C_2} V_{in}(t_n) + \frac{C_1}{C_2} V_{in}(t_n - T)) \quad (2.38)$$

From the above equation, we can draw a sampled data system diagram:

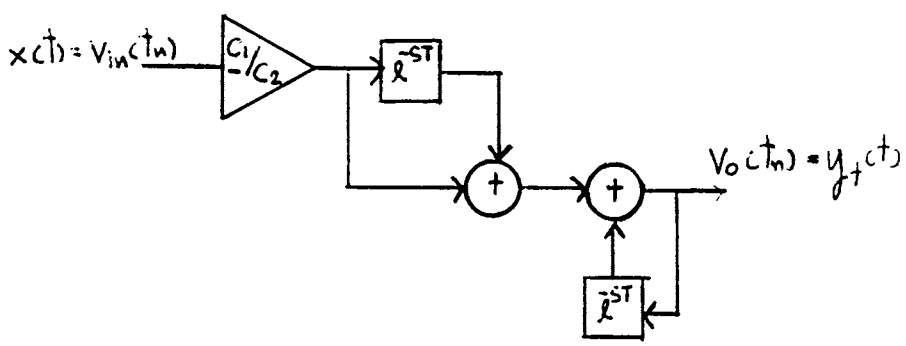


Fig. 2.13. A diagram of a sampled data system of Eq (2.38).

Now, the operation of this system is simulated by a digital system. Replacing all of the sampled data system delay elements(e^{-sT}) and the input x(t) by z^{-1} and x[n] respectively , and leaving the rest unchanged.

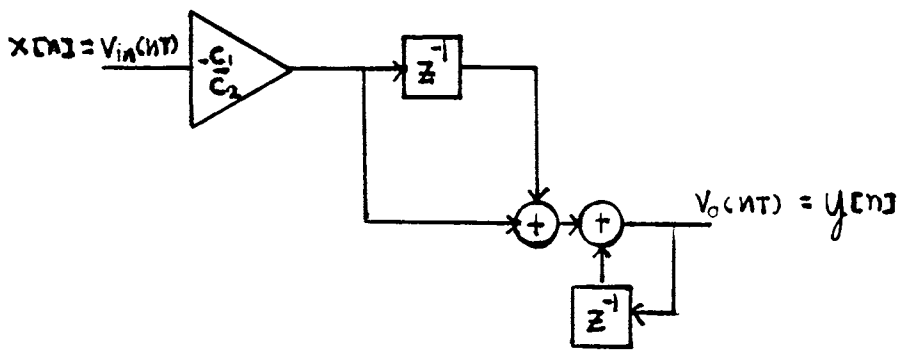


Fig. 2.14. A digital simulator of Fig. 2.13.

Then the output of this digital system y[n] will be equal to $y_t(nT)$, which is the samples of the output of the sampled data system.

$$\frac{y[n]}{x[n]} = \frac{y_t(nT)}{x(nT)} = -\frac{C_1}{C_2}\frac{(1+z^{-1})}{(1-z^{-1})} = H(z) \qquad (2.39)$$

Hence, the system function of this switched capacitor filter is $H(e^{j\omega T})$.

$$H(e^{j\omega T}) = -\frac{C_1}{C_2}\frac{(1+e^{-j\omega T})}{(1-e^{-j\omega T})} \qquad (2.40)$$

Where 1/T is the sampling frequency.

We can summarize that if a sampled data system $L_t(t)$ with system transfer function $H_t(s)$ is given, we replace all its delay elements e^{-sT} with digital delay elements z^{-1}, then the new system will be the digital simulator of the sampled data system L_t.

2.5 THE DESIGN OF THE SAMPLED-DATA SYSTEM FROM A CONTINUOUS-TIME SYSTEM.

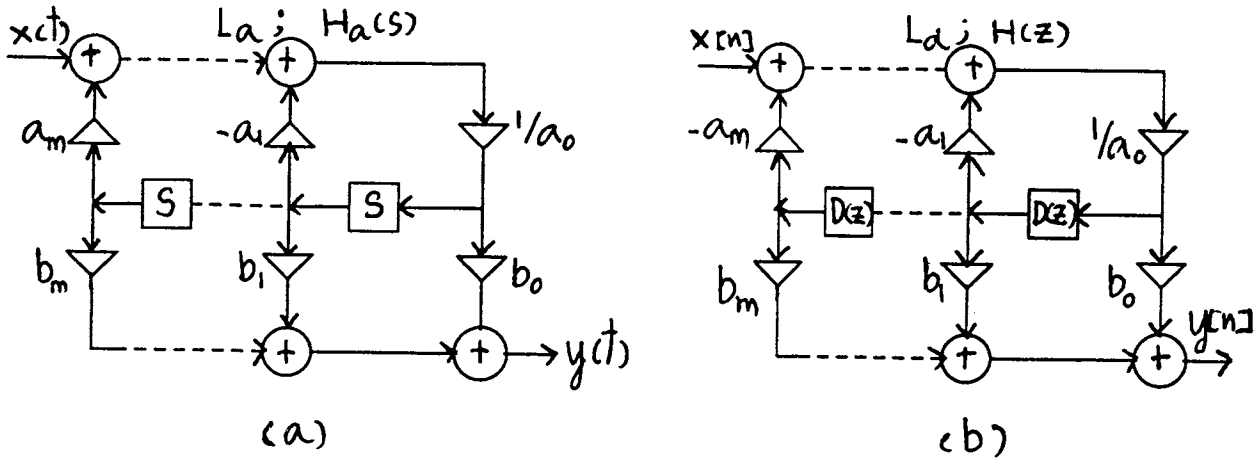
The simulation of an analog system by a digital system is considered. If a digital simulator of an analog system is known, then it will be easy to construct a sampled data system from this digital simulator.

THE FREQUENCY TRANSFORMATION METHOD OF SIMULATION

We are given an analog system L_a with a system function:

$$H_a(s) = \frac{b_m s^m + ...+b_1 s + b_o}{a_m s^m + ...+a_1 s + a_o} \qquad (2.41)$$

and we wish to find its digital simulator. The above function can be realized the system of Fig. 2.15(a) consisting of differentiators and multipliers. We shall design a digital simulator of the system of Fig. 2.15(b) by using the following method.



$$H_a(s) = \frac{b_m s^m + ...b_1 s + b_o}{a_m s^m + ...a_1 s + a_o} \qquad H(z) = \frac{b_m D^m(z) + ...+ b_1 D(z) + b_o}{a_m D^m(z) + ...+ a_1 D(z) + b_o}$$

Fig. 2.15. (a) An analog system (L_a)

(b) A digital simulator (L_d) of the analog system (L_a).

Suppose that we can find a digital simulator D(z) of a differentiator. If we replace each differentiator of the system of Fig. 2.15(a) with D(z), we will obtain the digital system Fig. 2.15(b). This system is the desired simulator of the system L_a. Comparing the transfer domain equations of the two system of Fig. 2.15., we conclude that to find the system function H(z) of the digital simulator L_d, we must replace the variable s in $H_a(s)$ with the system function D(z) of L_d. This yields:

$$H(z) = H_a(D(z)) \quad (2.42)$$

To complete the determination of the system L_d, we have to find the simulator D(z) of a differentiator. As we shall see, this leads to the frequency transformation method of simulation.

The frequency transformation has to yield 3 conditions which are determined below:

1 D(z) must be a rational function of z.

2 For $|z|=1$, D(z) must be purely imaginary; $D(e^{j\omega T}) = j\omega_a$. Vice versa, if s = D(z) is imaginary, then $|z| = 1$ must hold. (Any s to z transformations which follow the

second rule will ensure that the transformation will maintain the characteristic of the passband and stopband.)

3 For $|z|<1$, the real part of s = D(z) must be negative. Vice versa if Re s < 0 then the corresponding z must have an absolute value less than 1. (Any s to z transformations which follow this third rule will ensure that the transformation will maintain the stability.)

There are several types of s to z transformations. Only well known bilinear and LDI (lossless discrete integration) transformations will be considered and compared in this section.

1 Bilinear s to z transformation

$$s = D(z) = (\frac{2}{T})[\frac{(z-1)}{(z+1)}] \qquad (2.43)$$

(2.43) is usually called the bilinear s to z transformation.

Testing for condition 1, we find that it is a rational function of z

Testing for condition 2 set $s = j\,\omega_a$

$$z = |\ \frac{(1+j\omega_a T/2)}{(1-j\omega_a T/2)}\ | = 1$$

So the bilinear mapping satisfies the condition 2

Testing for condition 3, let $s = \sigma_a + j\omega_a$ with $\sigma_a<0$ then:

$$|\ z\ | = |\ \frac{(1+\sigma_a\frac{T}{2})+j\omega_a\frac{T}{2}}{(1-\sigma_a\frac{T}{2})-j\omega_a\frac{T}{2}}\ | < 1$$

So the condition 3 is also satisfied.

Since condition 2 is satisfied, the flat passband and stopband of the continuous-time filter will be preserved in the frequency response of the sampled data filter. In addition, the stability of the continuous-time filter will also be preserved because condition 3 is satisfied.

This method has three main disadvantages namely that a warping of the frequency scale exists due to its bandlimiting characteristic, the phase/frequency characteristic of the filter is not preserved and the frequency and time response of digital filter may differ significantly from the desired simulation of continuous-time filter $H_a(s)$.

The effect of warping may be seen by letting s = $j\omega_a$ and $z=e^{j\omega_s T}$, where ω_a and ω_s refer respectively to the continuous-time filter and the derived digital filter. The relation between ω_a and ω_s is shown in Fig. 2.16.

$$\omega_a = 2/T \tan \omega_s T/2 \qquad (2.44)$$

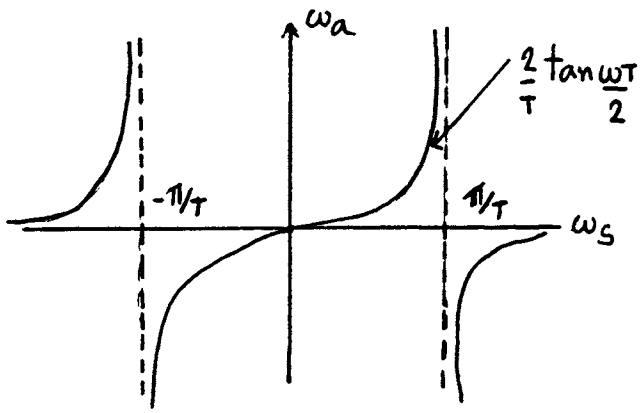


Fig. 2.16. The relation between the continuous-time and sampled-data frequencies for the bilinear s to z mapping.

From Fig. 2.16., we see that the frequency scale of the digital filter is not linearly related to that of the continuous-time filter. It will be linear at low frequency.

2 LDI transformation (LDI = lossless discrete integrator)

$$s = \frac{1 - z^{-1}}{T_s z^{-1/2}} \qquad (2.45)$$

(2.45) is usually called s to z LDI transformation.

Testing for the first condition, it is also a rational function, so the first condition is satisfied.

Testing for the second condition, from (2.45)

$$s = \frac{z^{1/2} - z^{-1/2}}{T_s}$$

$$z^2 - (2 + s^2T^2)z + 1 = 0$$

$$|z| = \left| \frac{(2 + s^2T^2) \pm sT(4 + s^2T^2)^{\frac{1}{2}}}{2} \right| \quad (2.46)$$

If the Laplacian variable s in (2.46) is replaced by $j\omega$, then $|z|$ will be equal to one, so it satisfies the second condition.

Testing for the third condition, if the Laplacian variable s in (2.45) is replaced by $-\sigma_a + j\omega$, then $|z|$ will be less than one. ($\sigma_a > 0$)

The LDI transformation also satisfies the third condition.

We eventually find that both the bilinear and LDI transformations have a property that the imaginary part of the s-plane is mapped on to the unit circle of the z-plane. This property is essential because the loss response of the discrete-time transfer function would be the same as the continuous-time one except for the frequency warping effect.

A difference between them is that the bilinear transformation maps the entire imaginary axis of the s-plane on to the unit circle of the z-plane, but for the LDI transformation, only part of the $j\omega$ axis of analog system ($-2/T < \omega < 2/T$) is mapped onto the unit circle whereas the LDI transformation expands it. This is shown by the following inequalities:

$$| \sin(x) | < x < | \tan(x) | \text{ for } -\frac{\pi}{2} < x < \frac{\pi}{2}$$

This makes the bilinear transformation preferable in filter design because after the transformation, the transition band becomes narrower.

On the basis of the above discussion, the design procedure can be found when a sampled-data filter transfer function H(z) is to be found by the bilinear mapping from a continuous-time model transfer function $H_a(s)$.

(1) From the specified passband of the required digital filter and the sampling frequency, ω_a is calculated by using (2.44).

(2) The transfer function of the continuous-time filter $H_a(s)$ is chosen or derived having

a response of correct shape to satisfy the specifications defined by the frequencies calculated in step 1.

(3) s = (2/T)[(z-1)/(z+1)] is substituted in $H_a(s)$, so the transfer function of sampled-data filter H(z) will be produced.

CHAPTER 3

SWITCHED-CAPACITOR FILTERS

INTRODUCTION

This chapter will discuss about the basic operation of switched-capacitor circuits. In addition, some solutions to overcome the problem of sensitivities at high Q-pole will also be given. At the end of this chapter, the design which is called "switched-capacitor N-path filter" will be briefly presented.

3.1 THE USE OF SWITCHED-CAPACITOR FOR SIGNAL PROCESSING

Since classical RC-active filters have proven difficult to meet the requirements of accuracy and low sensitivities on a silicon chip. As a result a lot of techniques that seem to solve these problems efficiently are developed. One of these techniques, switched-capacitor filter is the subject of this thesis.

The switched-capacitor circuits make use of the unique properties of metal-oxide-semiconductor (MOS) integrated circuit technology.

Some of the advantages of MOS technology are explained as follows:

(a) The MOS transistor is self-isolating, so it has superior logic density.

(b) MOS integrated circuit offer the ability to store charge on a node over a period of milliseconds because it has the high impedance in the off state.

(c) It can sense the value of charge continuously and nondestructively because it has infinite input impedance in the active mode of operation.

The above advantages of MOS encourage the use of switched-capacitor circuits because they utilize MOS switches and a capacitor to simulate the circuit behavior of a resistor.

In Fig. 3.1(a) shows a switched-capacitor circuit. Fig. 3.1(b) illustrates the clock signal v_{g1} and v_{g2}.

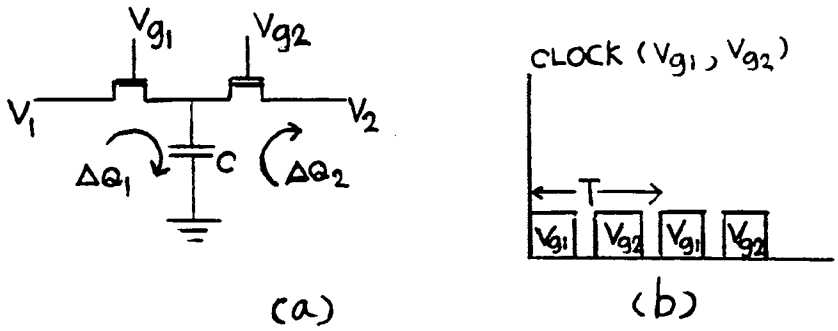


Fig. 3.1. (a) Representation of a switched-capacitor simulator of a resistor.
(b) Clock signals

Consider in Fig. 3.1(a) the charge ΔQ_1 entering C from input as v_{g1} goes high. Because the previous voltage of C was v_2 and is now recharged to v_1, so $\Delta Q_1 = C(v_1 - v_2)$. Next v_{g1} goes low, so Q1 acts as an open circuit and C still maintain the voltage at v_1. When v_{g2} goes high, C is recharged to v_2, so $|\Delta Q_2| = |C(v_2 - v_1)| = |\Delta Q_1|$.

Since a charge $C(v_1 - v_2)$ flows at node 1 and leaves at node 2 during the clock interval T. The average current I which flows from node 1 to 2 is determined below:

$$I = \left|\frac{\Delta Q_1}{T}\right| = \frac{C}{T} = \frac{C}{T}(v_1 - v_2)$$

but

$$I = \frac{(v_1 - v_2)}{R}$$

so

$$R = T/C \qquad (3.1)$$

From 3.1 shows that the circuit of Fig. 3.1(a) behaves as a resistor of value T/C ohm.

Some of the advantages of using the switched-capacitors are determined below:

(a) A time constant of the form R_1C_2 will be replaced by $(\frac{T}{C_1})C_2=(\frac{C_2}{C_1})f_c$

Where C_1 is the value of the switched-capacitors used to replace R_1, f_c is the clock frequency.

(b) The clock frequency can be controlled very accurately by using the crystal oscilator.

(c) The area needed by the simulated resistor is usually much smaller than that needed for a direct relization.

(d) The overall response of the SC filter will be a lot more accurate than a continuous-time filter because it depends on the ratio of the capacitors in stead of the absolute value of capacitors.

3.2 SWITCHED-CAPACITOR LADDER FILTERS.

From section 3.1, we find that by using the switched-capacitors to replace resistors, systems will become more accurate. Yet when high-Q pole are realized, switched-capacitor systems may still be too sensitive to parameter variations.

For the filters which have to realize high-Q poles, the most widely used are based on the simulation of the low sensitivity response of a doubly terminated reactance two port network [Ref. 10]. The system is shown below:

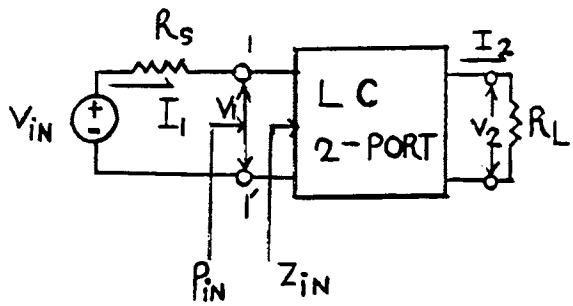


Fig. 3.2. Representation of a doubly terminated reactance two port with generator impedance R_s and load R_l .

The input impedance of this circuit seen from input terminal $1-1'$ is expressed as follow:

$$Z_{in}=R_1(\omega)+jX_1(\omega_1) \qquad (3.2)$$

The input power can be determined to be:

$$P_{in} = |I_1|^2 \mathrm{Re}(Z_{in}) = \frac{V_{iN}^2 R_1}{(R_s+R_1)^2+X_1^2} = P_{out} \qquad (3.3)$$

The reason why $P_{in} = P_{out}$ because we assume that the LC twoport is lossless. Our aims is to find the sensitivity of the output to the element variation of the LC twoport network at the maximum power transfer condition.

For the differential equation; the differentiating P_o with respect to X yields:

$$\frac{\partial P_o}{\partial X} = \frac{\partial P_o}{\partial R_1}\frac{\partial R_1}{\partial X} + \frac{\partial P_o}{\partial X_1}\frac{\partial X_1}{\partial X}$$

so $$\frac{\partial P_o}{\partial R_1}=\frac{(R_s^2-R_1^2+X_1^2)V_{in}^2}{\left((R_1+R_s)^2+X_1^2\right)^2}$$

$$\frac{\partial P_o}{\partial X_1}=\frac{-2R_1X_1V_{in}^2}{\left((R_1+R_s)^2+X_1^2\right)^2} \qquad (3.4)$$

The maximum power transfer condition can be obtained when the source impedance Z_s and Z_l are conjugate-matched to the input and output impedance.

$$Z_{in}=Z_s^* \quad R_1=R_s \text{ and } X_1=0 \qquad (3.5)$$

These conditions satisfy the frequencies at which the filter transmission is maximum.
By substitution (3.5) into (3.4)

$$\frac{\partial P_o}{\partial R_1}=0 \text{ and } \frac{\partial P_o}{\partial X_1}=0 \qquad (3.6)$$

(3.6) implies that the differential sensitivity in the (3.3) is zero:

$$S_X^{P_o}=\frac{X}{P_o}\frac{\partial P_o}{\partial X}=0 \qquad (3.7)$$

∂X = element variation

X = element value

We conclude that at the frequencies, at which the maximum power transfer occurs, the sensitivity of the response to the element variations will be zero.

The above descriptions explain why switched-capacitor ladder filters are used to realize high Q filters. The designers try to simulate the LC two-port filters by using the active elements on conditions that:

(a) The transfer function of the active LC two port which is the simulator of the passive LC filter and passive LC filter are the same.

(b) The parameters of active filter (simulated passive filter) and passive filters enter their

respective transfer functions the same way.

The most widely used strategy is developed in terms of the signal flow graph [Ref. 22] of LCR filters, then they are converted to active RC circuits which will eventually be turned into the switched-capacitor circuits. Filter derived this way are called "switched-capacitor ladder filters" [Ref. 2, 3].

3.3 SWITCHED-CAPACITOR N-PATH FILTERS

Even when the above method is used, the design for the high-Q narrow-band bandpass filters still can not be achieved because the response will still be too sensitive to parameter variations. In such cases a design based on the N-path filter concept comes in to use.

Let us consider the requirements on the bandpass filter.

A bandpass filter with a centre frequency ω_o, lower 3-db frequency ω_1 and upper 3-db frequency ω_2 is obtained from the normalized lowpass prototype filter by the transformation shown below:

$$S = \frac{1}{\gamma}\left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right) \quad (3.8)$$

where $\gamma = \dfrac{\omega_2 - \omega_1}{\omega_o}$ is the relative bandwidth.

S = normalized parameter of the lowpass filter, s= denormalized parameter of the band pass filter. The pole and zero locations of the ordinary bandpass filter relative to the pole and zero locations of a lowpass filter are given by:

$$(s = \sigma + j\omega)$$

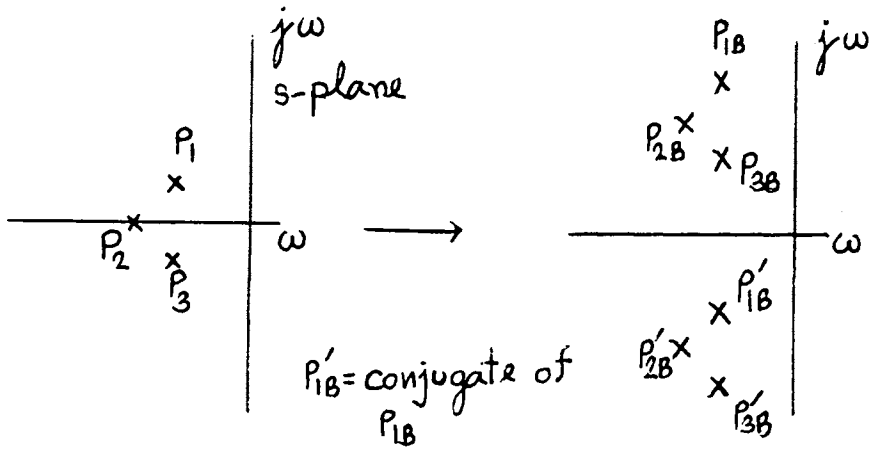
$$s_{1,2} = \omega_o\left(\frac{\gamma}{2}S_i \pm j\left(1 - \left(\frac{\gamma S_i}{2}\right)^2\right)^{\frac{1}{2}}\right) \quad (3.9)$$

Here we will concentrate on the "high-Q bandpass filter", so the bandwidth will be very

small, $\gamma=\frac{\omega_2-\omega_1}{\omega_0}$ will be << 1. We may assume that $|\frac{\gamma}{2}Si|\ll 1$ for the high Q bandpass filter. Equ (3.9)as shown above can be changed to the equation shown below:

$$s_i = \frac{\omega_2-\omega_1}{2}Si \pm j\omega_o \quad (3.10)$$

The relationships of the pole and zero locations between the lowpass and narrow-band bandpass filter are illustrated in Fig 3.3.



(a) (b)

Fig. 3.3. (a) Pole locations of the lowpass filter.

(b) Pole locations of the high-Q bandpass filter transformed from the lowpass filter.

From the foregoing description, we know that as the relative bandwidth of the bandpass filter becomes smaller (higher Q), the poles locations will become closer to the jw-axis, therefore become more sensitive to parameter variations.

Let us find the relationship between Q pole of the lowpass and bandpass filters.

Consider the biquadratic form of the lowpass filter

$$H_{lp}(s) = \frac{k\omega_p^2}{s^2 + \frac{\omega_p}{Q_{lp}} s + \omega_p^2}$$

$$Q_{lp} = \frac{|\omega_p|}{2|\sigma_1|}$$

ω_p = cutt off frequency

σ_1 = real part of the poles

Then make a transformation from a lowpass to a narrow-band bandpass filter from (3.10)

$$s_i = \frac{(\omega_2 - \omega_1)}{2} Si \pm j\omega_o$$

ω_o = Center frequency of bandpass filter.

Si = Normallized parameters of lowpass filter

s_i = Denormalized parameters of bandpass filter.

$\omega_2 - \omega_1$ = Bandwidth of the bandpass filter.

After the transformation $\omega_2 - \omega_1 = 2\omega_p$

Rewrite Fig. 3.3. again (consider P_1 only)

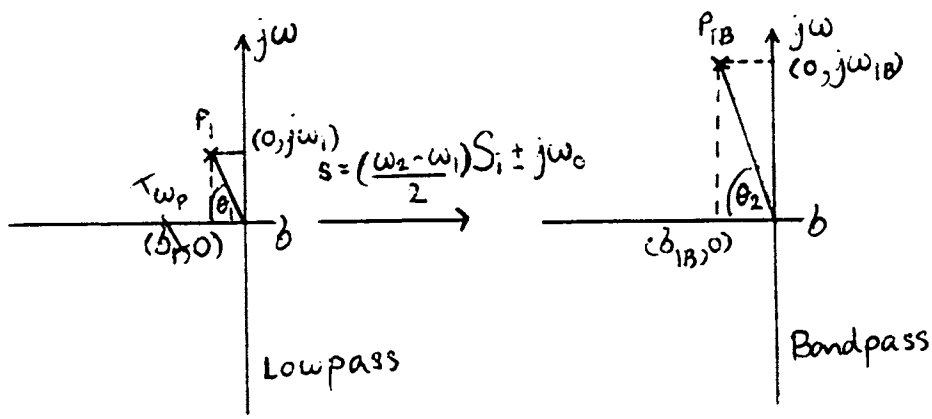


Fig. 3.4. Transformation from the lowpass filter to the bandpass filter (consider a pole only)

$$\text{pole of lowpass} = \sigma_1 + j\omega_1$$

$$\text{pole of bandpass} = s_{1,2} = \frac{(\omega_2-\omega_1)}{2}\frac{(\sigma_1+j\omega_1)}{\omega_p} \pm j\omega_o$$

$$s_{1,2} = \left(\frac{\omega_2-\omega_1}{2}\right)\left(\frac{\sigma_1}{\omega_p}\right) \pm j\left(\omega_o + \frac{\omega_1}{\omega_p}\left(\frac{\omega_2-\omega_1}{2}\right)\right) \quad (3.11)$$

Consider very high Q pole, the angle θ_1 and θ_2 will almost approach 90° . Hence, the length from (0,0) to (σ_1 , $j\omega_1$) and (0,0) to (σ_{1b} , $j\omega_{1b}$) are approximately equal to the length from (0,0) to (0,j ω_1) and (0,0) to (0, $j\omega_{1b}$) respectively, so $\omega_1 \approx \omega_p$.

From the above explaination, ω_1 will be approximately equal to ω_p, therefore Equ (3.11) can be changed to a form as shown below:

($\omega_2 - \omega_1 = 2\omega_p$ and $\omega_1 \approx \omega_p$ are replaced into Equ (3.11))

$$s_{1,2} = \sigma_1 + j\left(\omega_o + \frac{B}{2}\right) \quad (3.12)$$

At high Q, the angle θ_2 in the s-plane of the bandpass filter approaches 90°, therefore ($\omega_o + \frac{B}{2}$) in Equ (3.12) will be approximately equal to the length from (0,0) to (σ_{1b} , $j\omega_{1b}$). Hence, the mathmatical expression of Q_{bp} can be expressed as shown below:

$$Q_{bp} = \frac{\omega_o + B/2}{2|\sigma_1|} \quad (3.13)$$

We can say that

$$\frac{Q_{bp}}{Q_{lp}} \approx \frac{\omega_o + B/2}{\omega_p}$$

but $\omega_p \approx B/2$ so $\frac{Q_{bp}}{Q_{lp}} \approx \frac{2(\omega_o + B/2)}{B}$

but $\omega_o \gg B/2$ then $\frac{Q_{bp}}{Q_{lp}} = 2\frac{\omega_o}{B}$ (3.14)

We can conclude that $Q_{bp} \gg Q_{lp}$

If say $\frac{\omega_o}{B}=50$,then $Q_{bp}=100Q_{lp}$. The sensitivity to the parameter variation is proportional to the high-Q pole, as a result the sensitivity will become 100 times or more in the narrow-band bandpass filters. This certainly cannot be achieved by the conventional ladder filter design outlined in the begining of this chapter.

An effective way to solve this problem is by using the N-path filter.

Principles of the N-path filter.

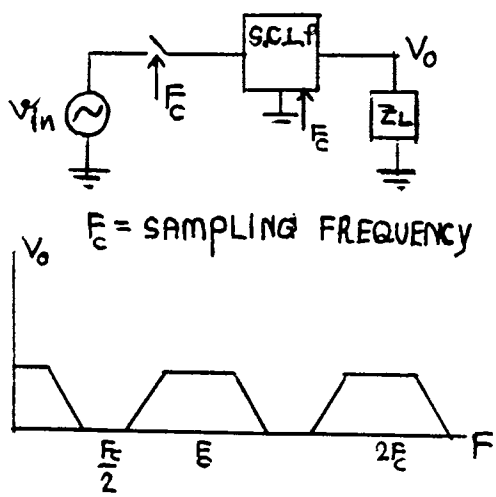


Fig. 3.5. Amplitude response of the SC lowpass filter (Asclp).

First, let us consider the amplitude response of an ideal SC lowpass filter in Fig. 3.5. This SC lowpass filter is a sampled-data network and is sampled with the clock frequency Fc. The resulting periodical frequency response of the SC lowpass has a bandpass characteristic related to the LP response at the multiples of the clock frequency.

This characteristic apparently shows the use of the lowpass filters as bandpass filters under the condition that the sampling frequency has to be 2 times higher than the input frequency. The range of the input frequency from 0 to $\frac{F_c}{2}$ is called the " Nyquist range".

To be able to increase the Nyquist range, there are two options:

(a) Simply by increase the clock frequency.

(b) Putting more additional paths in parallel. Such this process is called the N-PATH filter.

Some of the qualifications of this N-path filter are explained below;

(a) The transfer function characteristics are the same for every paths and the overall transfer function is the same to each path.

(b) The output signal is composed of N-sample per period T_c, so that the Nyquist range for the N-path filter is expanded N times as follow:

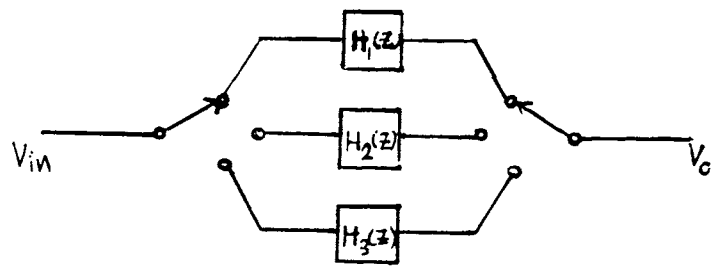


Fig. 3.6. Representation of 3-path filter.

Such the expanded SC Lowpass filters can be used as the bandpass filters with the center frequency $F_m = F_c$.

The most important properties of the SC N-path filter.

(a) Due to the structure of N-path filter (lowpass filter in parallel), we can arrange the sampling frequency at each path in such a way that the overall sampling frequency (looked from coming input signal to N-path filter) is increased n times where n is the number of paths. (By using nonoverlapped clock at each path.)

(b) The overall transfer function of the N-path filter in the z-domain is the same as the transfer function Hcell(z) of one path [Ref. 9, 14]:

$$H_{npath}(z) = H_{cell}(z)\big|_{z=e^{j2\pi\frac{f}{f_c}}} \quad (3.15)$$

The overall transfer function of the N-path filter has the identical sensitivity to the parameter variation as an individual path cell(This is a reason why N-path filter comes in to use). To understand more clearly, let us consider the mathmatical expression shown below.

From Fig. 3.6, This can be expressed as follow:

$$V_o(z) = H_p^1(z)V_{in}^1(z) + H_p^2(z)V_{in}^2(z) + ... + H_p^n(z)V_{in}^n(z) \quad (3.16)$$

Here, $H_p(z)$ is the transfer function of the Kth path in the filter. We have already known that the transfer function of the overall filter is the same as the transfer function of the individual cell ($H_p^1 = H_p^2 = H_p^k(z)$). If a parameter P (element value , Op-amp gain, etc.) in the Kth path filter changes from its norminal value by a small amount, then the output voltage changes by

$$\Delta V_o(z) = \Delta H_p^k(z)V_{in}^k(z) \sim \frac{\partial H_p^k}{\partial p}(z)\Delta p V_{in}^k(z) \quad (3.17)$$

Hence, for $z = e^{j\omega T}$, the change in frequency response of the overall filter is the same as for the Kth path acting alone. Since the latter is a low-pass filter, its pole-Q's(Qlp) will be low when it is compared with the pole-Q of the narrow-band bandpass filter.(We have already compared between the pole-Q of the lowpass and bandpass at the beginning of this chapter). From (3.13) and (3.14) the sensitivities are lowered by about a factor $\frac{Q_{bp}}{Q_{lp}} \sim \frac{2\omega_o}{B}$.

CHAPTER 4

SWITCHED-CAPACITOR N-PATH FILTER

INTRODUCTION

Switched-capacitor N-path filters will be discussed in this chapter and they are shown to have properties such as stable passband response and low sensitivities to element-value variations even for extremely narrow bandwidth, in contrast to other design approachs.

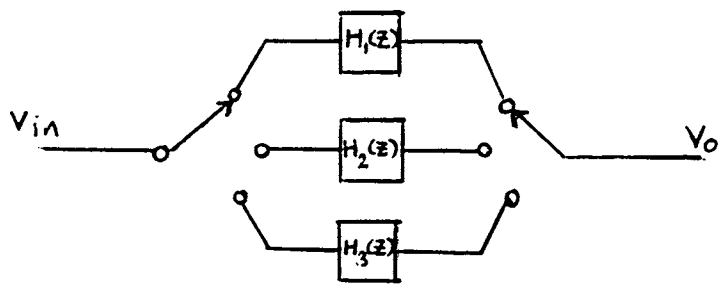


Fig. 4.1. N-path filter(N=3)

The above figure illustrates generally the structure of an N-path filter which consists of N identical paths. Due to mismatch in the filter paths, unwanted mirror frequencies appear at the output. For the case where the N-path filter is driven by a sine generator $v_{in}\sin(\omega_o t)$. The clock frequency is f_c. Fig. 4.2. is the frequency spectrum of the output of the 4-path filter. The small arrows T in Fig. 4.2. represent the spectral fractions of the mirror frequencies and are induced by the path mismatch. The spectral components of the mirror frequencies at $2\omega_c-\omega_o$ and $-2\omega_c+\omega_o$ lie in the passband of the N-path filter.

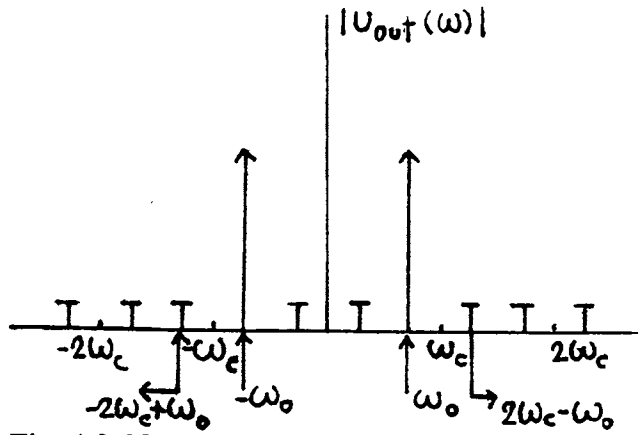


Fig. 4.2. N-path filter output spectrum containing spectral fractions of mirror frequencies.

An important property of N-path filters is that if the responses of all the paths are identical to each other, the phasors of the mirror frequency will form a polygon with zero resultant at the output. Unfortunately, it is not possible in practice to make each channel identical to each other by such a connection that is illustrated in Fig. 4.1.

To overcome the effect of path mismatch, the concept of a pseudo-n-path filter [Ref. 6] has been proposed. The idea is that it consists of having the signal of each path cyclically processed by all paths in such a way that, at regular spaced intervals, the current state is moved from one path to the next. Thus, the precise balance in one path is potentially obtained. However, some disadvantages such as the limitations of op-amp performance in the above concept may cause imperfections at the passband. In such cases, another technique known as a memory type N-path filter [Ref. 6] can be used since it is less sensitive to the low gain of op-amps.

In the first part of this chapter, a passive SC N-path filter circuit will be discussed and designed. One of its advantages over an active switched capacitor N-path filter is that we do not need to be concerned about the limitations of op-amps.

4.1 SWITCHED CAPACITOR N-PATH FILTERS BASED ON RC FILTER SIMULATION.

To construct a passive switched capacitor N-path filter, we first consider a simple first order SC lowpass filter as illustrated below:

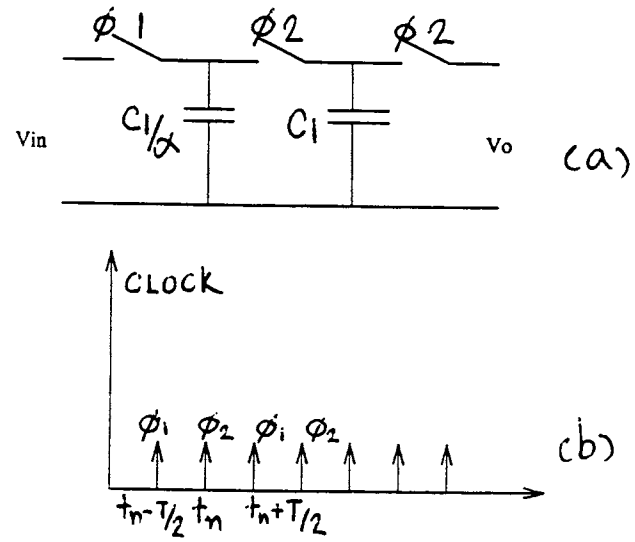


Fig. 4.3. a simple passive filter (a) circuit diagram (b) clock signals

When switch ϕ_2 closes, ΔQ flows from $\frac{C_1}{\alpha}$ to C_1. Now, consider at t_n when ϕ_2 turns on.

$$\Delta Q(t_n) = \frac{C_1}{\alpha}\Delta v(t_n) = \frac{C_1}{\alpha}(v_{in}(t_n - \frac{T}{2}) - v_o(t_n)) \quad (4.1)$$

Consider at " C_1 " output.

The number of charge flowing in to " C_1 " at the output will be expressed below; (consider at the time equal to t_n)

$$\Delta Q(t_n) = C_1 \Delta V = C_1(V_o(t_n) - V_o(t_n - 1)) \quad (4.2)$$

The amount of charge flowing out from $\frac{C_1}{\alpha}$ is equal to the amount of charge flowing in to C_1.

$$\frac{C_1}{\alpha}(V_{in}(t_n - \frac{T}{2}) - V_o(t_n)) = C_1(V_o(t_n) - V_o(t_n - 1))$$

$$V_o(z)(1 + \alpha - z^{-1}\alpha) = z^{-1/2} V_{in}(z)$$

$$\frac{V_o(z)}{V_{in}(z)} = \frac{z^{1/2}}{1 + (\alpha + 1)(z - 1)} \quad (4.3)$$

The frequency response of the (4.3) can be shown below:

$$\frac{V_o}{V_{in}} = \frac{(e^{j\omega T})^{1/2}}{1+(\alpha+1)(e^{j\omega T}-1)}$$

but if $\omega T \ll 1$ then $e^{j\omega T} \approx 1+j\omega T$, and

$$\frac{V_o}{V_{in}} \approx \frac{(1+j\omega T)^{1/2}}{1+(\alpha+1)(j\omega T)}$$

$$\approx \frac{1}{1+(\alpha+1)(j\omega T)} \qquad (4.4)$$

So the frequency response will be the same as the frequency response of a lowpass filter with R = $\frac{(\alpha+1)}{C}T$. To obtain a better roll off, additional circuits may be cascaded with buffers between each stage.

A third order switched capacitor lowpass filter (SCFLP) is considered, whose configuration is shown in Fig. 4.4.

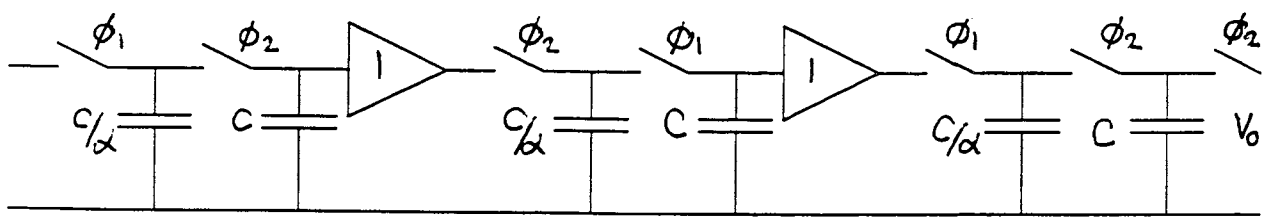


Fig 4.4. A third order SC lowpass filter.

From Fig. 4.4., it is shown that if $\frac{C}{\alpha}$ and C share the charge, then the voltage from buffer 1 will be transferred to the next stage at $\frac{C}{\alpha}$. The voltage of $\frac{C}{\alpha}$ of the second stage is equal to the voltage of the $\frac{C}{\alpha}$ of the first stage, so $\frac{C}{\alpha}$ of the first state can be used as $\frac{C}{\alpha}$ of the second

stage without any buffering. This idea can be used to construct a new circuit as shown in Fig. 4.5.

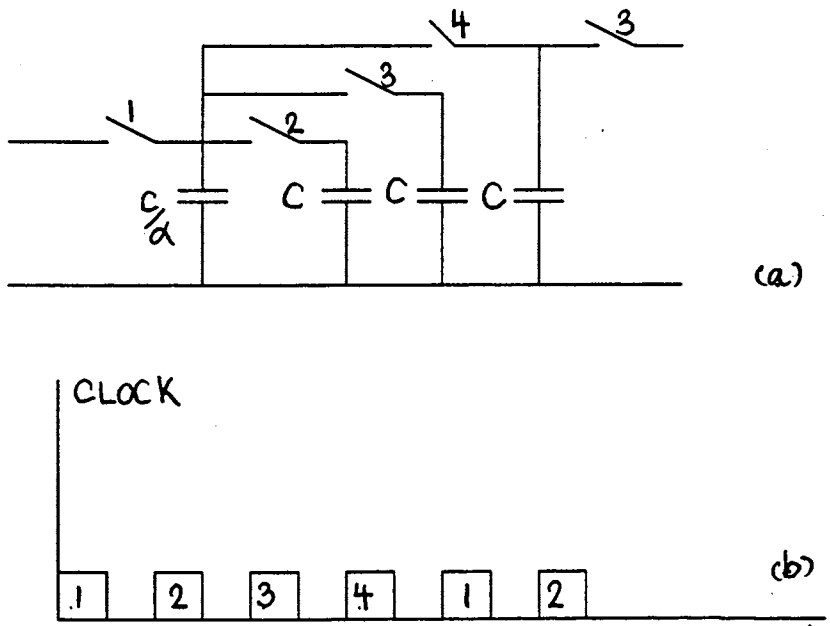


Fig. 4.5. Third order filter (a) new configuration (b) the clock frequency

The purpose is to make a bandpass filter. Let us consider the frequency response in Fig. 4.6.

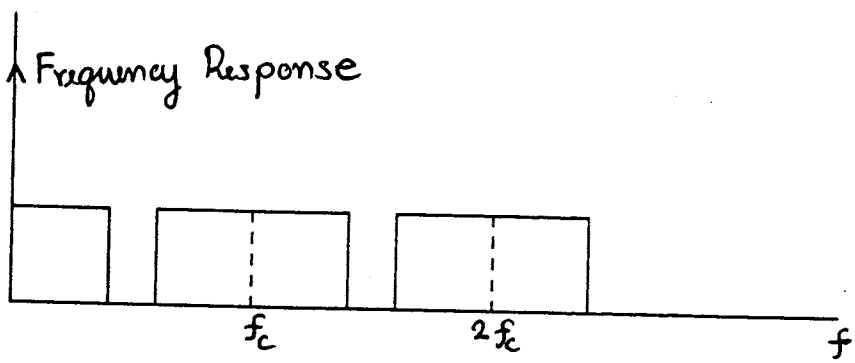


Fig. 4.6. The frequency response of the circuit in Fig 4.5.

From Equ (4.3), F(z) is the first order, so the third order form of F(z) of Fig 4.5 is:

$$F^3(z)=\frac{z^{3/2}}{(1+(1+\alpha)(z-1))^3} \qquad (4.5)$$

The frequency response which is expressed by (4.5) is periodic because (4.5) consists of the z variables which are equal to $e^{j\omega T}$.

In order to have the circuit in Fig. 4.5 operated as a bandpass filter, which has a centre frequency at f_c, a problem lies in the fact that the sampling frequency of the circuit in Fig. 4.5 is only at f_c . A solution is to add additional paths in parallel, then every clock each path has to be arranged in such a way that the sampling frequency of the overall system is increased to nf_c, where n = the number of path.

The new configuration is shown in Fig. 4.7.

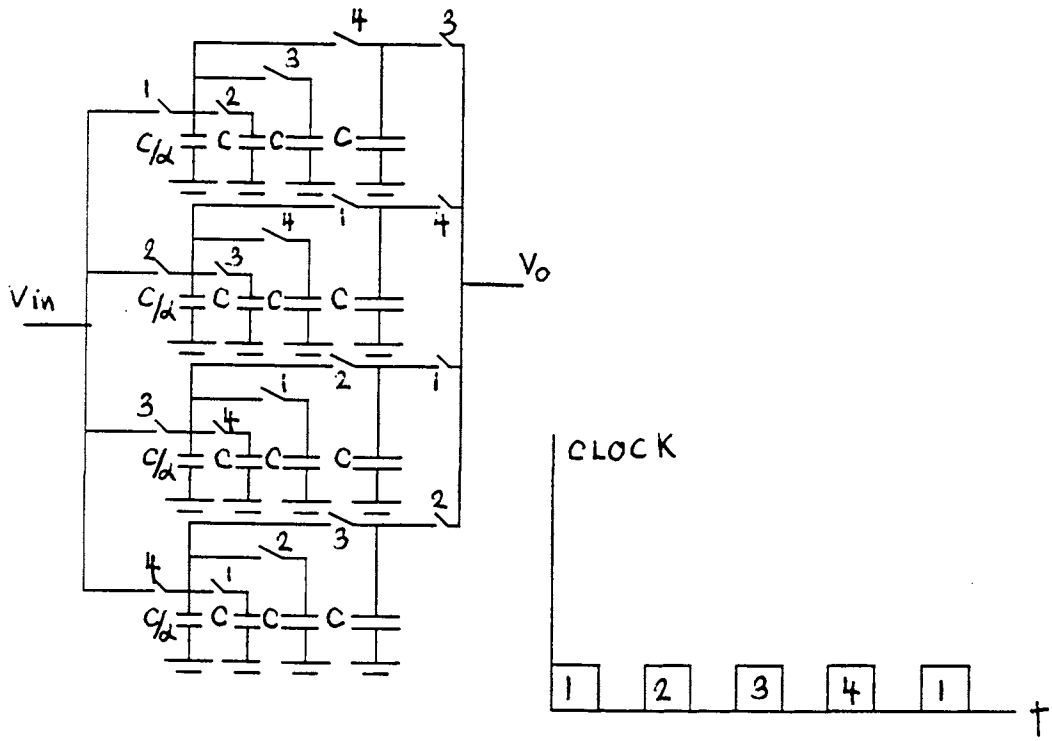


Fig. 4.7. Passive 4-path filter.

So the Nyquist limit will be extended to $2f_c$, where f_c is the clock frequency of each path.

If the Nyquist limit is extended this way, bandpass filters which have a centre frequency at f_c can be realized.

4.2 PREFILTER

In order to obtain a bandpass filter which has the centre frequency equal to the clock

frequency from the switched capacitor N-path filter, discussed at the beginning of this chapter, a prefilter that has a stopband at twice the clock frequency is required.

A solution is to use an additional bandstop filter [Ref. 7, 8, 23] to suppress the side bands. Consider the transfer function of a bandstop filter and its diagram as illustrated below.

$$F_{bandstop}(z) = \frac{1}{2}(1-z^{-1/2}) \qquad (4.6)$$

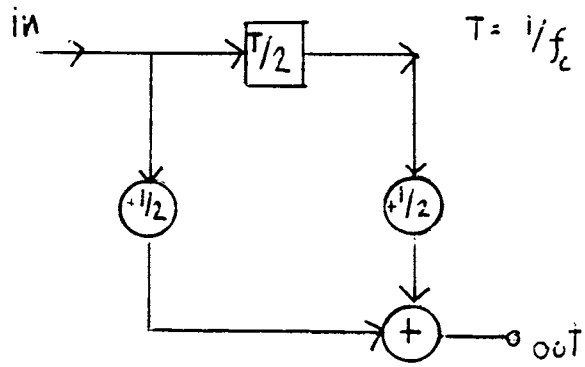


Fig. 4.8. Flowchart representation of the bandstop filter obtained from (4.6)

A switched capacitor circuit that realises (4.6) is illustrated in Fig. 4.9

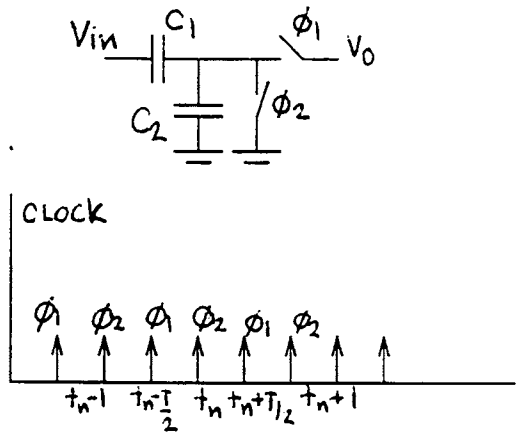


Fig. 4.9. A bandstop prefilter that realises (4.6)

consider at $t = t_n$

First consider at C_2

when ϕ_1 " on "

$$C_2 = \frac{\Delta Q_{(t_n)}}{\Delta V(t_n)}$$

so $$\Delta Q(t_n) = C_2 \Delta V(t_n) = C_2 V_o(t_n)$$

We now consider at C_1.

$$\Delta Q(t_n) = C_1 \Delta V(t_n) = C_1 (V_{in}(t_n) - V_o(t_n) - V_{in}(t_n - T/2))$$

$$C_2 V_o(t_n) = C_1 (V_{in}(t_n) - V_o(t_n) - V_{in}(t_n - T/2))$$

so $$\frac{V_o}{V_{in}} = \frac{1 - z^{-1/2}}{\left(\frac{C_2}{C_1} + 1\right)}$$

If $$C_2 = C_1, \text{ then } H(z) = \frac{1}{2}(1 - z^{-1/2}) \qquad (4.7)$$

Consider the frequency response of 4.7. It is shown in Fig. 4.10.

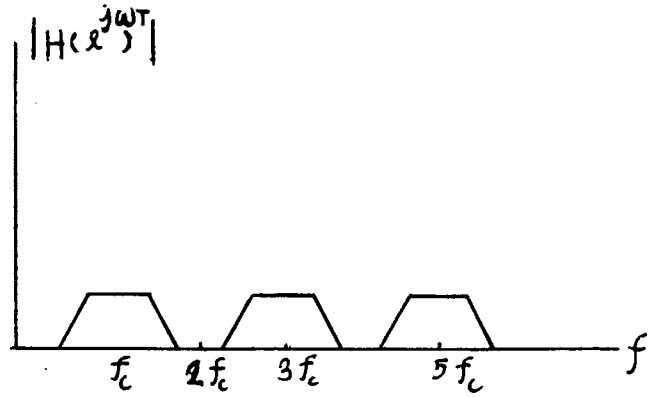


Fig. 4.10. The frequency response of prefilter.

From (4.7), the frequencies at which there is null response, can be found by:

$$\frac{1}{2}(1-z^{-1/2})=0$$

so $f=2nf_c$ where n = 0,1,2,3,.... (integer) (4.8)

From Fig. 4.10, there are still the bands around f_c such as $3f_c$,$5f_c$. They can not be eliminated by the prefilter but these unwanted bands do not have much affect, because their frequencies are high enough and they will be suppressed later by a smoothing filter (SMF).

The design now adds a prefilter ahead of the SCFLP, resulting in the new configuration shown in Fig. 4.11.

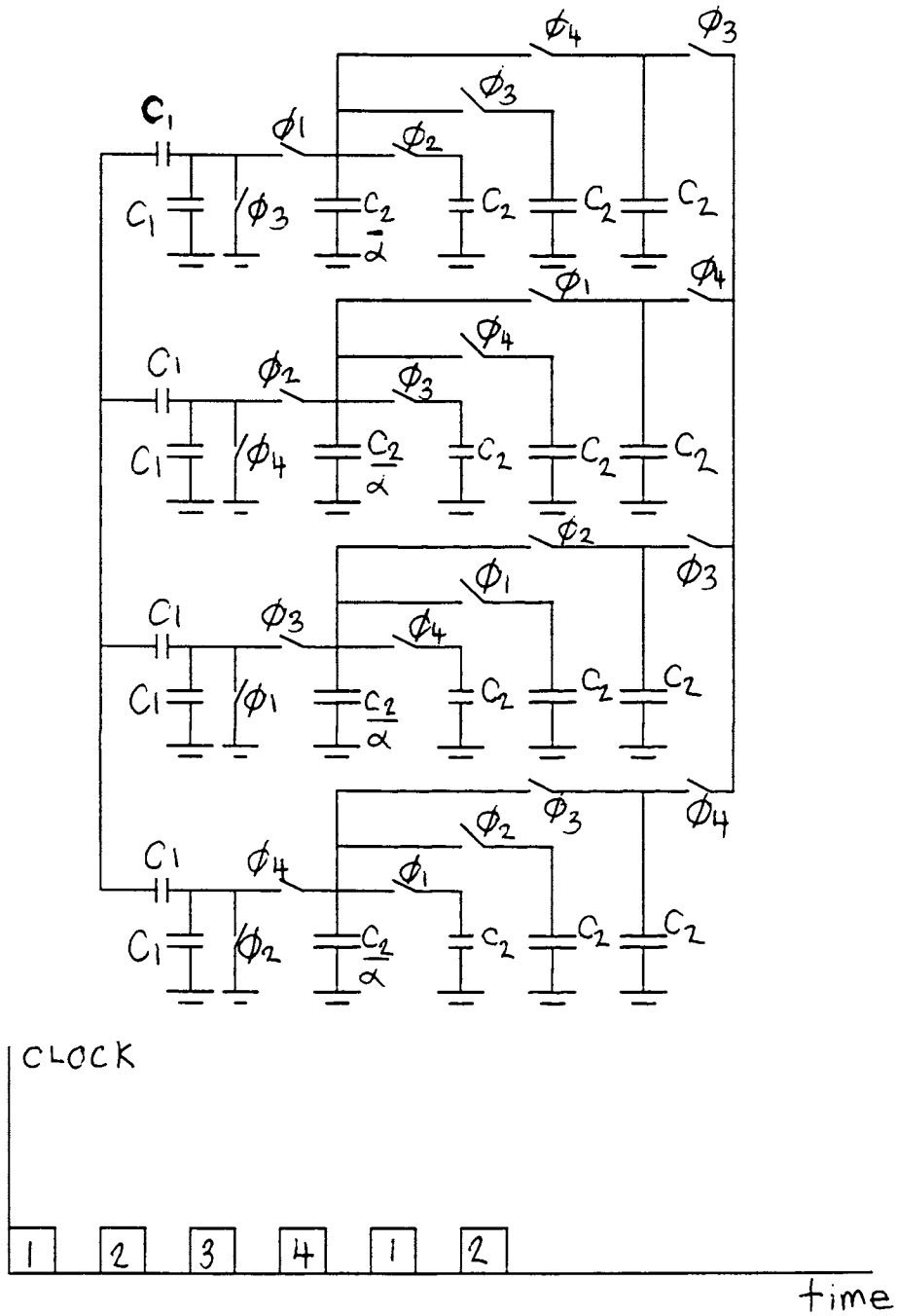


Fig. 4.11. A bandpass SC 4-path filter

Note that the bandwidth of the SCLP N-path filters has to be smaller than the rejection bandwidth of the prefilters.

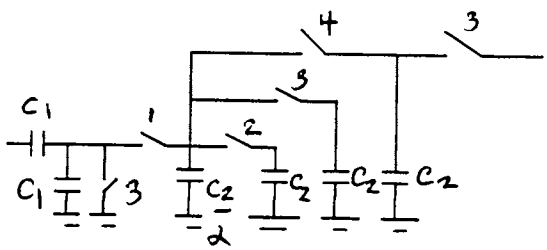
The calculation of the bandwidth of SCLP N-path filters and prefilters is shown below:

From Equ (4.3), the bandwidth of prefilter = $\frac{2f_c}{\pi}$ (4.9)

From Equ (4.8), the bandwidth of SCLP N-path filter = $\frac{f_c}{\pi(\alpha+1)}$ (4.10)

We now find the transfer function of the overall N-path filter of Fig. 4.11. The overall transfer function of the N-path filter is the same as the transfer function of each path. The transfer function of each path will be analyzed as illustrated below:

Consider a single path of Fig. 4.11. (the top path):



The above configuration is equivalent to a circuit, which is illustrated below:

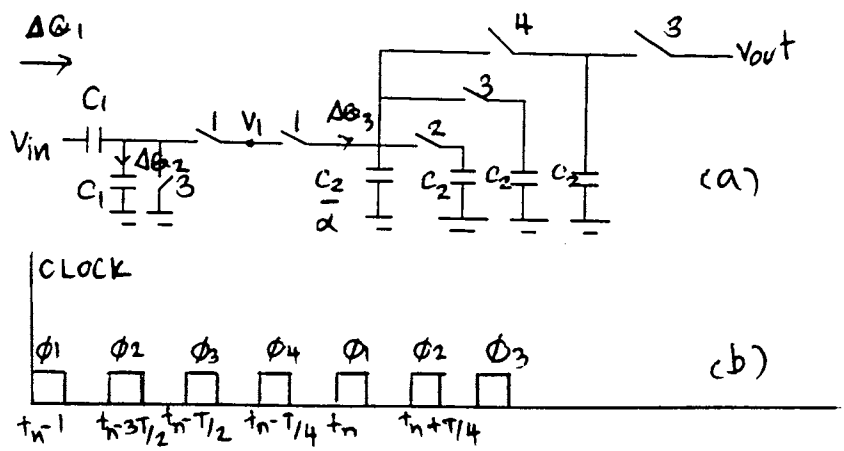


Fig. 4.12. (a) The combination of a bandstop and a 3-order lowpass filter.

(b) The clock signals

consider at t = t_n, clock ϕ_1 *closes*.

$$\Delta Q_3(t_n) = \frac{C_2}{\alpha}(v_1(t_n) - v_1(t_n - \frac{T}{4}))$$

$$\Delta Q_2(t_n) = C_1 \Delta v(t_n) = C_1 v_1(t_n)$$

$$\Delta Q_1(t_n) = C_1 \Delta v(t_n) = C_1(v_{in}(t_n) - v_1(t_n) - v_{in}(t_n - \frac{T}{2}))$$

$\Delta Q_1 = \Delta Q_2 + \Delta Q_3$, therefore:

$$C_1(v_{in}(t_n) - v_1(t_n) - v_{in}(t_n - \frac{T}{2})) = C_1 v_1(t_n) + \frac{C_2}{\alpha}(v_1(t_n) - v_1(t_n - \frac{T}{4}))$$

$$C_1 v_{in}(z)(1 - z^{\frac{-1}{2}}) = 2C_1 v_1(z) + \frac{C_2}{\alpha} v_1(z) - \frac{C_2}{\alpha} z^{\frac{-1}{4}} v_1(z)$$

$$\frac{v_1}{v_{in}} = \frac{C_1(1 - z^{\frac{-1}{2}})}{(2C_1 + \frac{C_2}{\alpha} - \frac{C_2}{\alpha} z^{\frac{-1}{4}})}$$

From Equ (4.5), $\frac{v_o}{v_1} = \frac{z^{\frac{3}{2}}}{(1 + (1+\alpha)(z-1))^3}$, therefore the transfer function of the overall bandpass 4-path filter is:

$$\frac{v_o}{v_{in}} = \frac{C_1(1 - z^{\frac{-1}{2}}) z^{\frac{3}{2}}}{(2C_1 + \frac{C_2}{\alpha} - \frac{C_2}{\alpha} z^{\frac{-1}{4}})(1 + (1+\alpha)(z-1))^3} \quad (4.11)$$

From Equ(4.11), a factor ($1 - z^{\frac{-1}{2}}$) suppresses the undesirable passbands at nf_c for even values of n.

In order to simplify the requirements of the smoothing filter, additional paths can be used so that there are more samples per cycle of the input waveform. The switched-capacitor bandpass 6-path filter will be constructed on a chip as described later. The design rule is still the same as the design of the SC bandpass 4-path filter. The order of the SC bandpass 6-path filter is five, therefore it gives better roll off than the SC bandpass 4-path filter.

The measurement of the SC bandpass 6-path filter on the chip is reported in Chapter 6. The circuit diagram of the SC bandpass 6-path with bandstop filters is shown in Fig. 4.13.

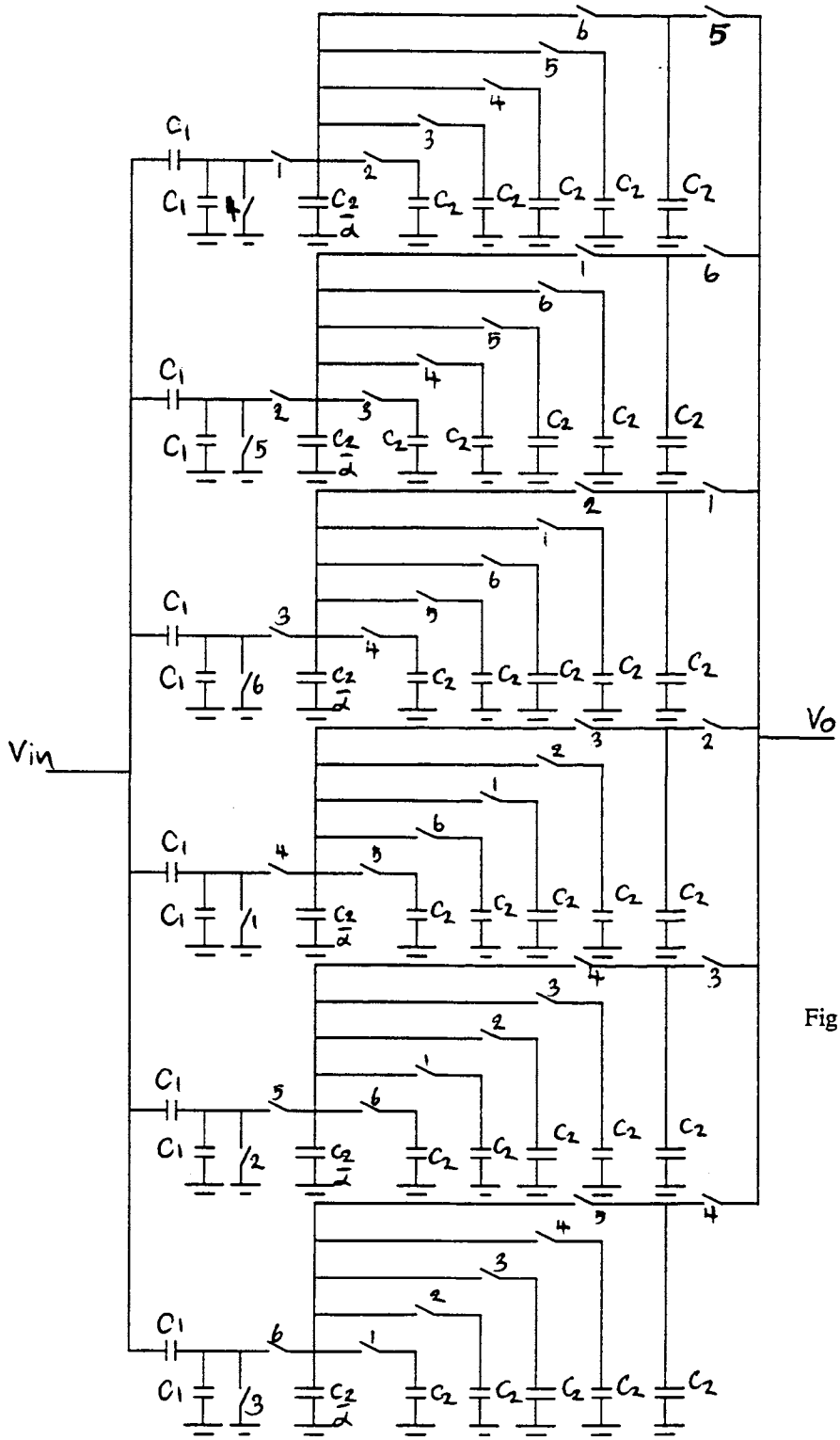
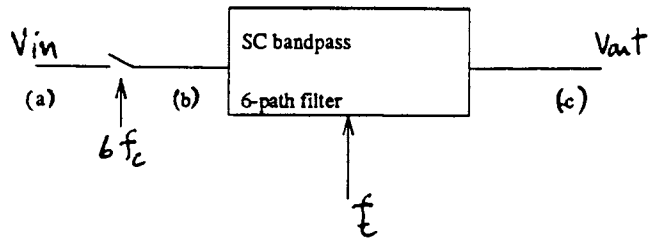


Fig. 4.13. The SC bandpass 6-path filter

We now consider the appearance of the frequency spectrum of the output of the SC bandpass 6-path filter.

f_c = the clock frequency of the SC bandpass 6-path filter

$6f_c$ = the overall sampling frequency of the SC bandpass 6-path filter which is seen by the input signal.



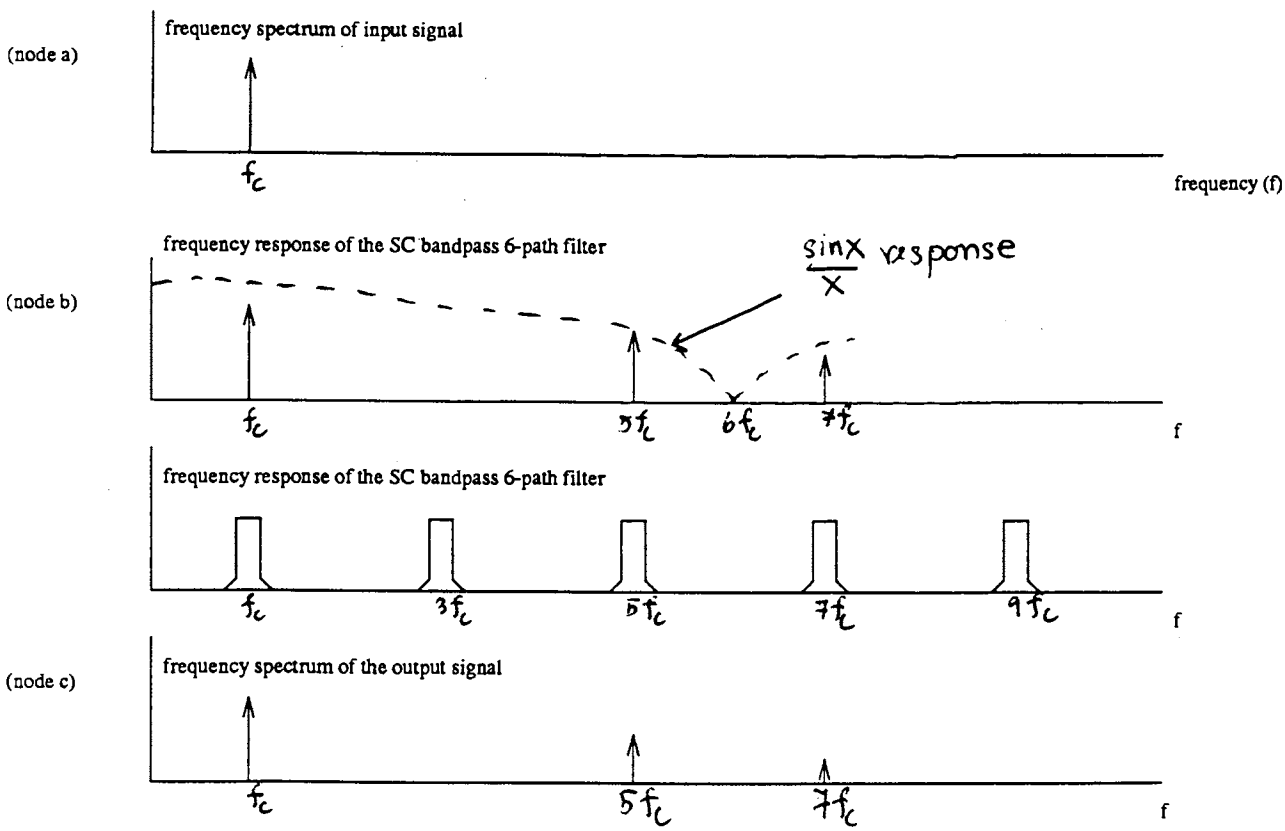


Fig. 4.14(a), shows the frequency spectrum of a single sinusoidal input signal.

Fig. 4.14(b), shows the frequency spectra of the sampled and held input signal after it was sampled by the sampling frequency ($6f_c$). From Fig 4.14 b, the magnitude of the frequency spectra decreases as the harmonic is higher due to $\frac{\sin x}{x}$ response.

Fig. 4.14(c), shows the overall frequency response of the SC 6-path bandpass filter.

Fig. 4.14(d), shows the frequency spectra of the output of the SC bandpas 6-path filter.

The transfer function of the overall bandpass 6-path filter of Fig 4.13.is shown below: (The calculation is similar to the calculation of the transfer function of the overall bandpass 4-path filter.)

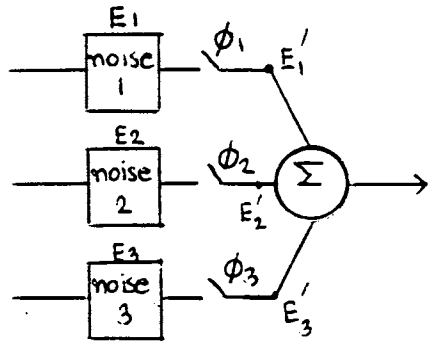
$$F(z) = \frac{C_1(1 - z^{\frac{-1}{2}})z^{\frac{5}{2}}}{(2C_1 + \frac{C_2}{\alpha} - \frac{C_2}{\alpha}z^{\frac{-1}{6}})(1 + (1+\alpha)(z-1))^5} \quad (4.13)$$

In Chapter 6, the frequency spectra of the output of the SC bandpass 6-path filter on the chip will be measured and compared to Fig. 4.14(d).

The main disadvantages of the N-path filter are as follows:

1 Due to the parasitic capacitances between gate-drain and gate-source of MOS switches in the SC circuit, the clock signal from the gates can feedthrough the parasitic capacitances and appear at the output.

If all paths are symmetrical, the mirror frequency generated from each path will cancel out at the output. We can express this phenomenon below.



E_1 , E_2 and E_3 are the mirror frequencies produced by each path. All E_1 , E_2 and E_3 are sampled at different time due to the non-overlapped clock signals , therefore their phases differ by $\frac{2\pi}{N} = \frac{2\pi}{3}$. If all the paths are symmetrical, $E_1' + E_2' + E_3'$ will cancel out at the output. Hence the mirror frequency will no longer appear.

Comparison between N-path filter and the conventional SC-bandpass filters.

(a) The centre frequency (f_{centre}) of the conventional SC bandpass filter is proportional to the clock frequency (f_{clock}).

$f_{centre} = kf_{clock}$;where k is a function of capacitor ratios.

The centre frequency of the N-path filter is equal to a multiple of the clock frequency of the lowpass cell of each path.

$f_{centre\ of\ N-path} = nf_{clock\ of\ lowpass\ cell}$;where n = 0, 1, 2, 3,...

For most applications, only the passband at f_{clock} is desired (n = 1).

(b) The conventional SC bandpass filters with high Q have high sensitivities to the element-value variations. For SC N-path filter, the lowpass cells have low Q, thus the overall sensitivities are lower.

(c) Noise in the conventional bandpass filter are produced by the switches and by op-amps. There are additional noises source in the N-path filter which are introduced by the switches, op-amp , path mismatch and the clock feedthrough.

4.3 PSEUDO-N-PATH FILTER

The circuit that is discussed in section 4.1 is not suitable for critical applications , where the clock feedthrough noise and mirror frequencies are introduced into the passband by the path mismatch. In such a this problem, the pseudo-N-path principle can be used.

The concept of the pseudo-N-path filter is that in these filters only one physical path exists;however all of the memoried elements in the paths are connected to a circulating delay line , which consists of some memoried elements, and they work in such a way that there are N-path working altogether with different clock phases, hence the same amount of unwanted frequencies is introduced from each path, so the phases of these unwanted signals will form a polygon with zero resultant at the output. (To simplify the above concept, we will compare it with a property of the op-amp which the non-inverting input is connected to the ground. Hence, the inverting input will behave as a virtual ground. This inverting input can be compared with the circulating-delay line , which is not N-path filter, but it behaves in such a way that it represents a N-path filter)

The process to construct a pseudo-N-path filter is often applied to a SC ladder filter which is based on signal flow graph representation(SFG).

As we know that a LDI SC ladder filter based on SFG consists of non-inverting and inverting integrators, which are put alternately in the circuit. At the feedback of these integrators are memoried elements. We then can apply a circulating delay line into these memoried elements to convert to the pseudo-N-path filter. Some of elements in the circuit are memoryless , so we do not need to change anything.

We now consider the structure of both inverting and non-inverting integrators that are used in the LDI ladder SC filter and consider how to combine the circulating-delay line with the memoried elements of these integrators.

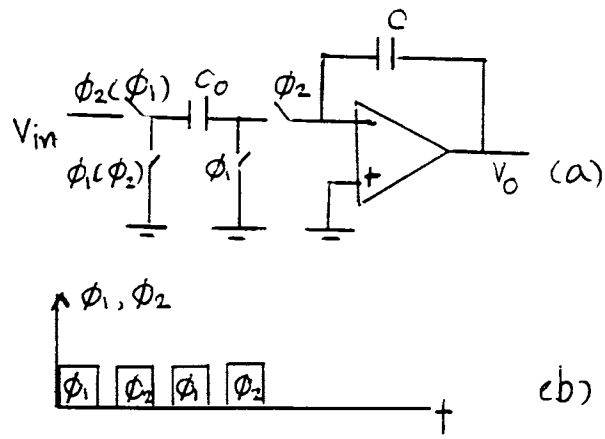


Fig. 4.15. SC integrator stage

(a) Circuit

(b) Timing diagram

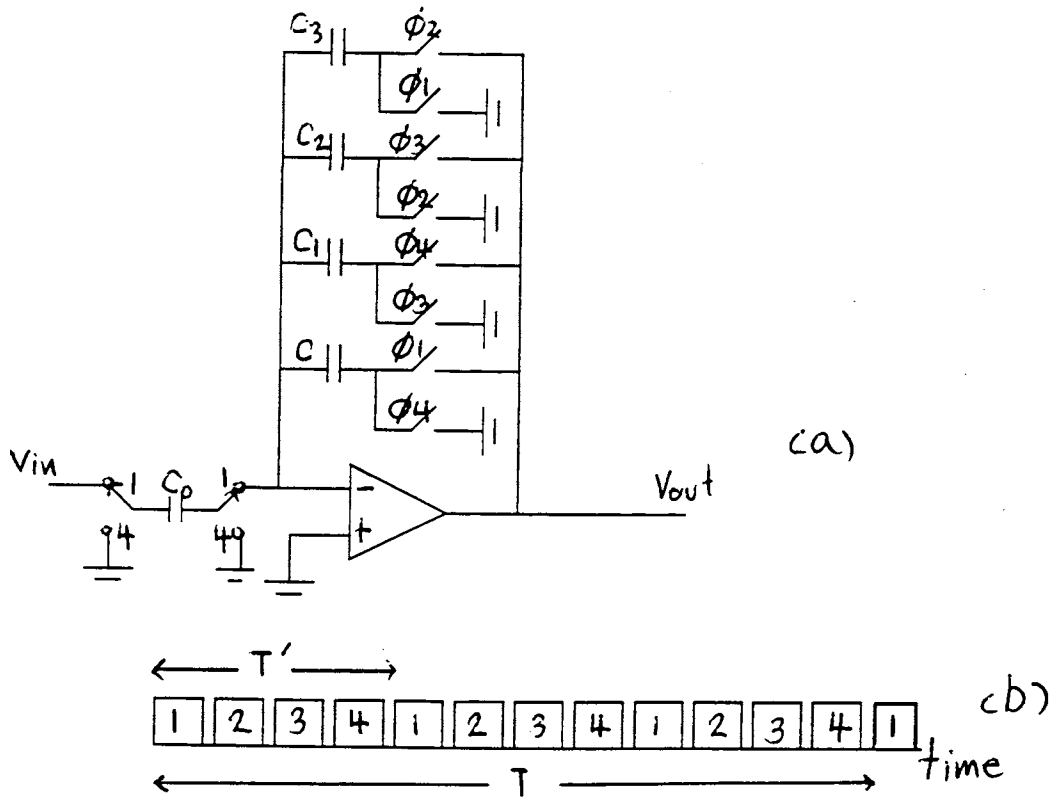


Fig. 4.16. Circulating-delay type pseudo-N-path filter stage

(a) circuit

(b) Timing diagram. T' is the clock period for the N-path filter. T is the interval for a full cycle of each path.

In Fig. 4.15. demonstrates the inverting SC integrator (the clock phases without parenthesises) and non-inverting SC integrator(the clock phases inside parenthesises). In this case, we will consider the inverting SC integrator only. The clock phase of this SC integrator equals to T, then the overall transfer function will be:

$$H(z)=\frac{(-C_o/C)}{(1-z^{-1})} \qquad (4.14)$$

where $z = e^{sT}$; T = the period of clock frequency.

We now consider Fig. 4.16. that illustrates how to put the circulating delay line at the memory element, which is the feedback capacitor of the op-amp.

At the C_o which is memoryless element, we do not need to put circulating delay elements because it charges and discharges periodically.

We now consider the performance of the circuit in Fig. 4.16.

During clock phase 1, the feedback capacitor C receives a signal charge from the storage capacitor C_3. This charge is also increased by the input charge that enters from the coupling capacitor C_o.

During clock phase 2, the charge from C_2 is transferred to C_3.

During clock phase 3, the charge from C_1 is transferred to C_2.

During clock phase 4, the charge from C is transferred to C_1 as C_o is discharged.

Then the above cycle is repeated again. We clearly see that if the clock feedthrough noise is introduced from each switch, then the same amount of noise will be introduced from each path. Hence, their phases will form a polygon with zero resultant at the output. (Because all of the unwanted signal goes through the same circulating delay line.)

From the above discussion, the first passband will be located at around f = 1/NT, where the path period T contains 12 clock signals.

From Fig. 4.16., its overall transfer function will be changed to:

$$H(z)=\frac{(-C_o/C)}{(1-z^{-3})} \qquad (4.15)$$

where $z = e^{sT'}$

Again the sensitivity of a narrowband SC bandpass N-path filter depends on each path, which is a lowpass filter representation. We also may consider that the properies of the overall N-path filter are similar to the properties of the lowpass filter at each path. Hence, we will concentrate on the improvement of the properties of each path.

If each path is designed by LDI ladder SC filter based on SFG, the Q of the overall N-path filter can be increased further, since LDI ladder SC filter uses parasitic-free structure of SC circuit to replace each resistors. (The less capacitance the circuit has, the higher the speed of the circuit can be obtained.)

The main problem of LDI ladder SC filter is that the load termination of a doubly terminated LC ladder is a resistive termination, so the LDI s to z transformation can not be realized at the resistive terminations. Hence, an approximation is needed at the resistive load terminations. However, this approximation causes some losses at the passband. Fortunately, we now are considering only very narrow-band bandpass filter, this effect from the approximation error at the resistive load of doubly terminated LC ladder can be ignored.

We now come back to consider low-pass LDI ladder SC filter. After we complete designing lowpass LDI ladder SC filter, we then just find where the locations of memoried elements are, then have them supplemented by circulating delay lines, in order to transform the lowpass to a bandpass filter. (We suggest that most of the memoried elements are regularly at the feedback capacitors of the integrators.) For the memoryless elements will be unchanged.

(Some memoried elements which are not at the feedback capacitors of integrators will be very hard to be supplemented by the circulating delay lines. Hence, we need some modifications to turn them to memoryless elements but of course, the overall operation of the circuit has to be maintained [Ref. 9, 12].)

There are however some disadvantages of the SC pseudo N-path filter, namely:

1. It needs a lot of clock phases intervals to complete one period, so the op-amp must operate fast. It results in the complex requirements of the op-amp.

2. Each charge package must complete four transfer in each period T, incomplete charge transfer effects due to imperfect virtual ground will appear even at high op-amp gain.

Both of these disadvantages can be partially corrected by a circuit illustrated below.

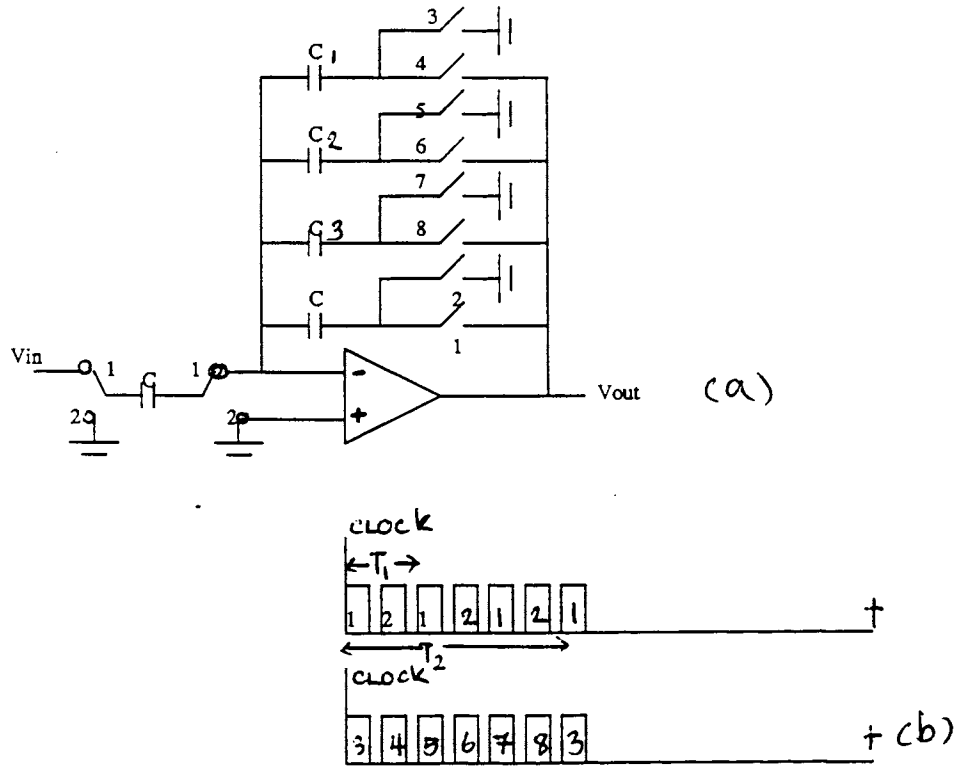


Fig. 4.17. Memory-type SC filter stage

(a) circuit

(b) Timing diagram. T_1 is the sampling period of the N-path filter. T_2 is the period of the first center frequency.

This circuit operates on the principle of supplementing the feedback capacitor by using memory elements in stead of using a circulating delay line as illustrated in Fig. 4.16. and its operation is as follows:

When phase 3 and 1 are on, the charge from C_1 is transferred into C, where it is also increased by the input charge entered from the coupling capacitor C_o. (We assume that this operation represents the operation of path 1.)

During phase 4 and 2, the updated charge is transferred back into C_1. (Now C_1 memorizes the operation of path 1 and waits for one clock period to reoperate again.)

During phase1 and 5, the charge from C_2 is transferred into C where it is increased by the input charge entered from C_o. (Then, this operation represents the operation of path 2.)

During phase 2 and 6, the updated charge is transferred back into C_2. (Now C_2 memorizes the operation of path 2 and waits for T second to reoperate again.)

The same operation cycle will be performed on the charge of C_3 during phase 7 and 8.

From the above discussion of memory type filter, we clearly see that each channel operates separately, then the path mismatch can occur.

CHAPTER 5

DECIMATION AND INTERPOLATION FILTERS

INTRODUCTION

In this chapter, some of the techniques that can be used to simplify the requirements of antialiasing and smoothing filters will be described in more detail.

5.1 PREFILTERING REQUIREMENTS FOR SWITCHED-CAPACITOR FILTERS.

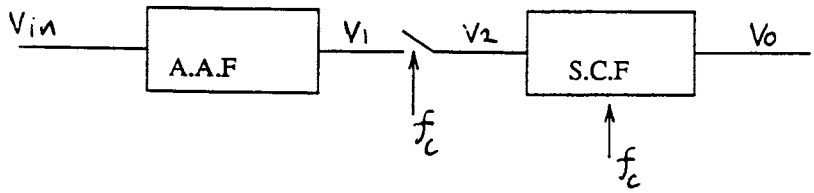
All sampled data systems require band-limiting of their input signal to prevent aliasing. We normally use a continuous-time filter to limit the frequency spectrum of the input signal. This filter is often called antialiasing filter (AAF). It is more convenient to design an AAF if the sampling frequency of the sampled data system is high, but difficulties arise if the sampling frequency is too large. These problems are:

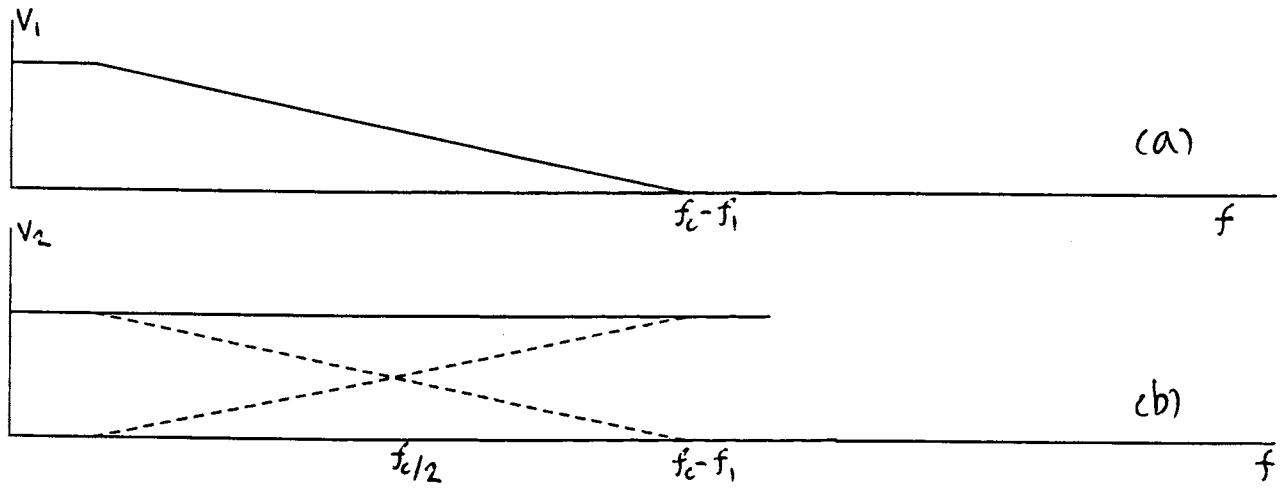
(a) The spread of the capacitance values becomes large [Ref. 9]

(b) The sensitivities of the response to parasitics and tolerances may increase [Ref. 9].

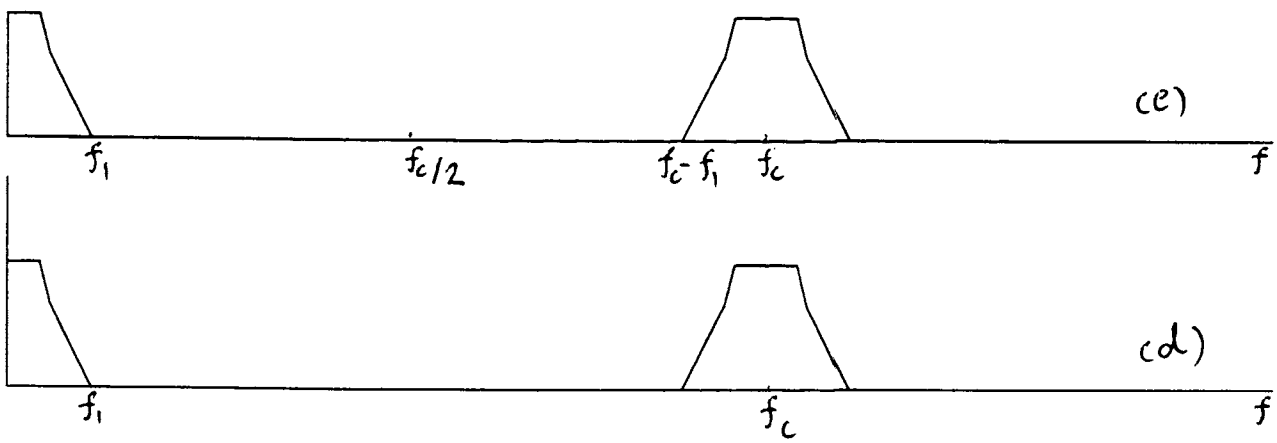
(c) The op-amp unity gain frequency needs to be five times higher than the clock frequency, otherwise distortion will occur at the output. Consequently, for large clock frequencies high speed op-amps are difficult to realise [Ref. 4].

A solution is to use the technique that is illustrated in Fig 5.1. According to the following technique, the stopband of AAF will be extended from $\frac{f_c}{2}$, which is the Nyquist limit of the SCF, to $f_c - f_1$, where f_c and f_1 are the sampling frequency and stopband frequency of the SCF respectively. As a result the structure of AAF will be less complex.





frequency response of SCF



f_c = the clock frequency of SCF

f_c =the sampling frequency of SCF

f_1 = the stopband frequency of SCF

$f_c - f_1$ = the stopband frequency of A.A.F

FIG 5.1

Fig. 5.1(a) represents the frequency spectrum of signal at v_1 which is similar to the frequency response of AAF, which is assumed to have a stopband at $f_c - f_1$, where f_c and f_1 are the sampling frequency and stopband frequency respectively.

In Fig. 5.1(b), the dashed line represents the aliasing that occurs at v_2. If the stopband frequency of v_1 goes beyond the Nyquist limit ($\frac{f_c}{2}$), that part of the spectrum of v_1, that contains energy in the $\frac{f_c}{2} < f_c < f_c - f_1$ range, will be aliased into the $f_1 < f < \frac{f_c}{2}$ range as was illustrated in Fig 4.2(b). The solid line represents the actual frequency spectrum of v_2, which comes from the arithmetic sum of the dashed line.

Fig: 5.1(c) represents the frequency response of SCF, which has the stopband and clock frequency equal to f_1 and f_c respectively.

In Fig. 5.1(d), the frequency range $f_1 < f < f_c - f_1$ from Fig5.1b which is the frequency range, where aliasing occurs, will fall into the stopband of the SCF, so that the resulting aliasing distortion will be suppressed by SCF and will not appear at the output of the overall system. Then the output will appear without distortion, as illustrated in Fig. 5.1(d).

The above technique can therefore simplify the requirements of an AAF.

Another technique involves adding a further SCF, which uses a multiple clock frequency, between the AAF and main SCF. This additional SCF is called a decimation filter.

This decimation filter is actually a lowpass filter which has a clock frequency n times that of the SCF.

Now, we will consider its performance when combined with the whole system as illustrated in Fig. 5.2. For this illustration, we assume that n = 4

$4f_c$ = the sampling frequency of the decimator.

f_c = the sampling frequency of the SCF

f_1 = the stopband frequency of the decimator.

$4f_c - f_1$ = the stopbad frequency of AAF

f_s = the stopband frequency of SCF

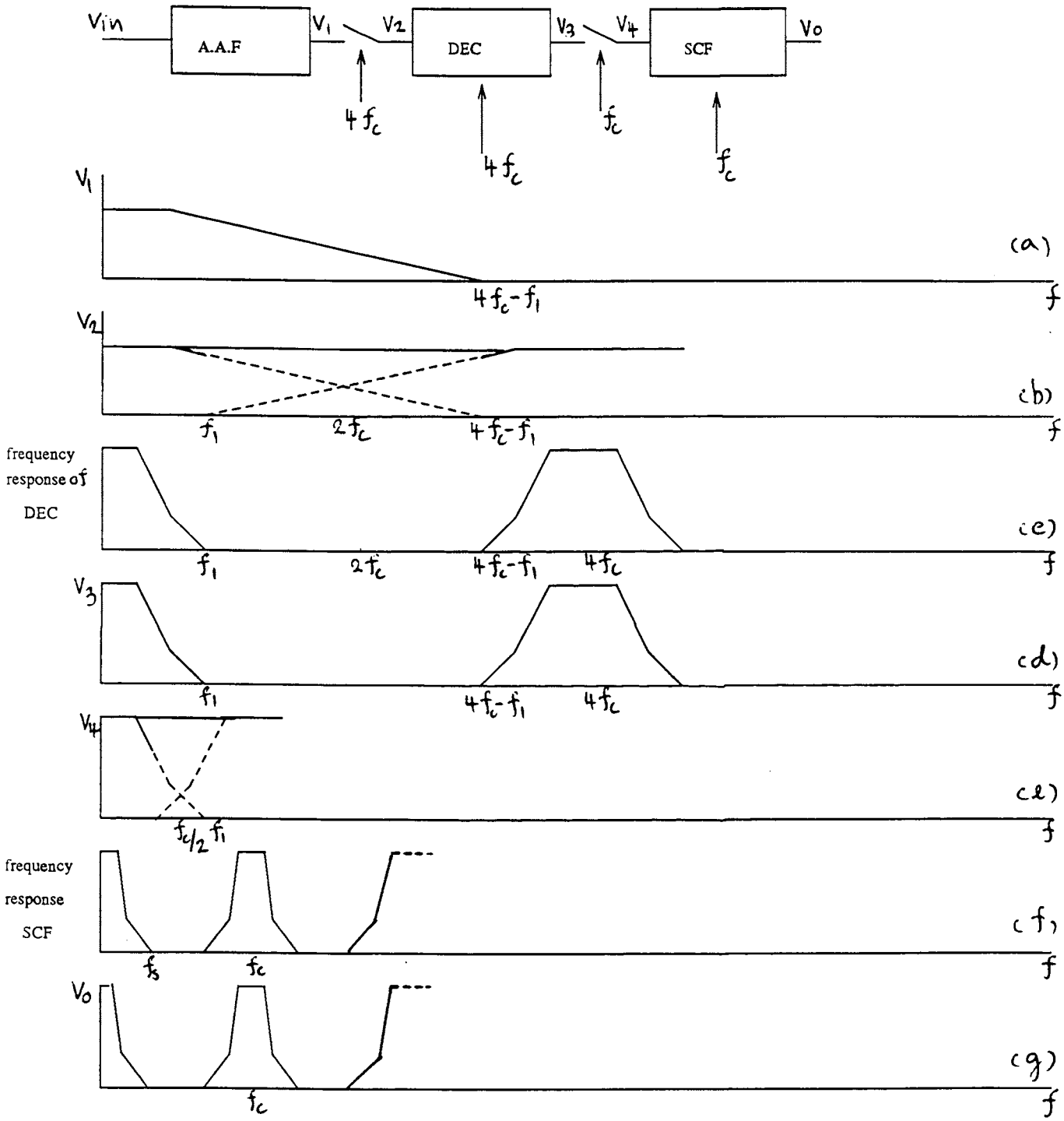

Vin
A.A.F
V1
V2
DEC
V3
V4
SCF
Vo
4fc
4fc
fc
fc
V1
(a)
4fc-f1
f
V2
(b)
f1
2fc
4fc-f1
f
frequency response of DEC
(e)
f1
2fc
4fc-f1
4fc
f
V3
(d)
f1
4fc-f1
4fc
f
V4
(c)
fc/2
f1
f
frequency response SCF
(f)
fs
fc
f
Vo
(g)
fc
f

Fig 5.2.(a) represents the frequency spectrum of v_1 which is similar to the frequency response of AAF, which has the stopband frequency at $4f_c - f_1$.

In Fig 5.2.(b), the dashed line represents how aliasing occurs and the solid line represents the actual frequency spectrum of v_2 that occurs from the arithmetic sum of the dashed line.

Fig 5.2.(c) shows the frequency response of the decimator.

Fig. 5.2(d) shows the frequency spectrum of the input signal to the decimator in Fig. 5.2(b), that has a region of frequency which aliasing occurs, will be suppressed by the stopband of the decimator, so that the frequency spectrum of the signal at the output of the decimator will be free from distortion as illustrated in Fig. 5.2(d)

Fig. 5.2(e), the dashed line shows how aliasing occurs and the solid line represents the actual frequency spectrum of v_4 .

Fig. 5.2(f) represents the frequency response of SCF.

In Fig. 5.2(g), let us go back to Fig. 5.2(e), at the region of frequency spectrum of v_4, which aliasing occurs, will be suppressed by the stopband of SCF, so the frequency spectrum of the output signal will be free from distortion as illustrated in Fig. 5.2(g).

From the above discussion, we find that the decimator can help to simplify the requirements of the anti-aliasing filter.

Comparing the first technique and the second technique, we find that by using the decimator, the requirements of AAF can be simplified by a factor close to n, where n is the ratio between clock frequency of the decimator and the SCF.

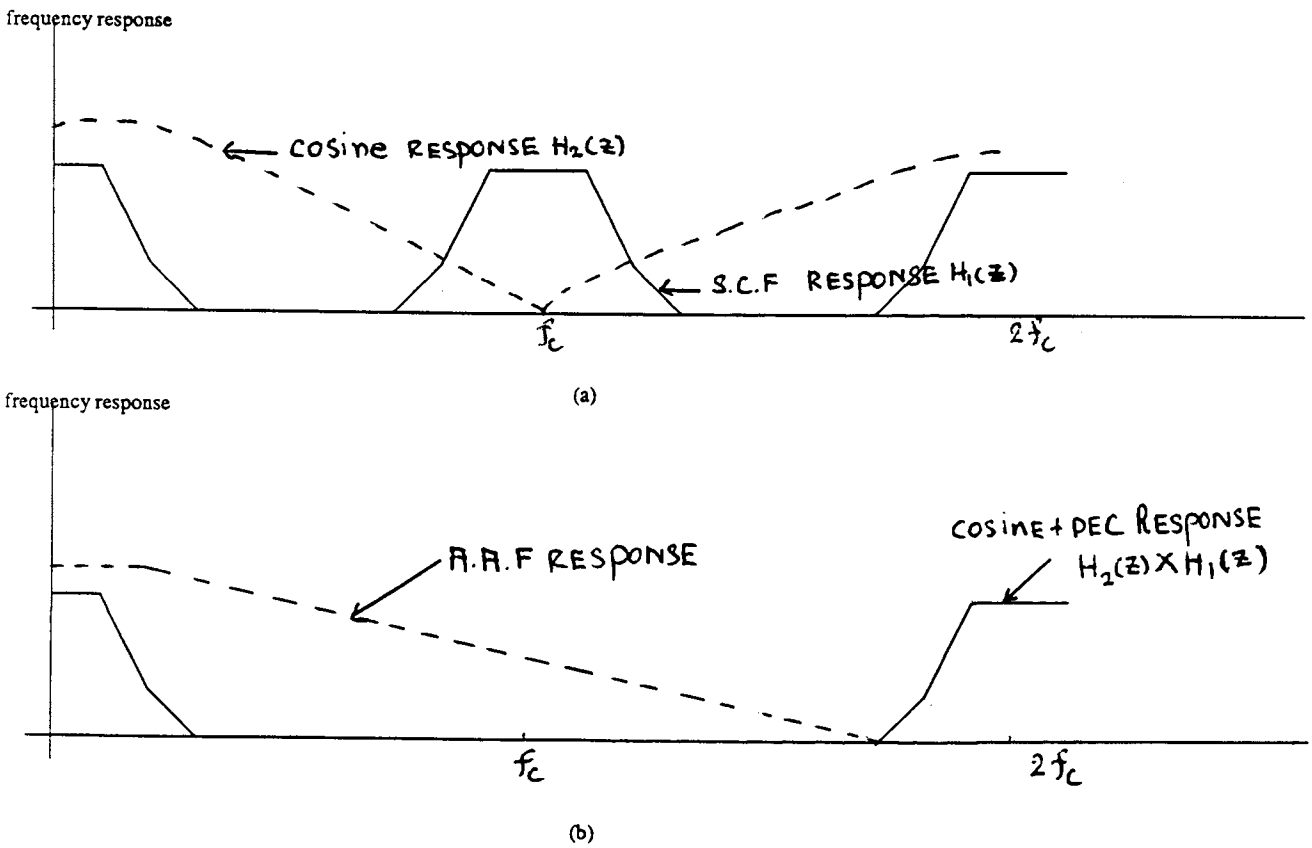
Next, we will consider a switched-capacitor circuit which is used to improve the performance of decimator, so the order of AAF will be reduced more.

This new additional SC circuit is incorporated in the decimator by modification of its input. Consequently the additional SC circuit at the input will introduce a new factor $H_2(z)$ in to the transfer function of the decimator. To obtain the desired result, we require the transfer function to contain a new factor $H_2(e^{j\omega T}) = 2\left|\cos\pi\frac{f}{2f_c}\right|$

$H_2(z)$ has a high attenuation at signal frequencies of f_c , $3f_c$.

Let us assume that the transfer function of the decimator before modification is $H_1(z)$. After the input is modified, the overall transfer function will be $H_2(z) \times H_1(z)$

Consider the frequency response of the additional function $H_2(z)$.



In Fig. 5.3(a), the solid line represents the frequency response of decimator ($H_1(z)$) before the input is modified and the dashed line represents the frequency response of the new factor [$H_2(z)$]. After combine them together, the combined filter's frequency response is illustrated in Fig. 5.3(b) in which the dashed line represents the frequency response of the AAF. From Fig. 5.3(b), we see that the stopband of the decimator is extended by a factor close to 2.

After the new factor ($H_2(z)$) is introduced into the decimator transfer function, we will call this a cosine decimator.

5.2 THE DESIGN OF THE DECIMATOR

The design of a decimator and a cosine function will be demonstrated respectively. From the above discussion of the performance of a decimator, it is actually a lowpass filter. Hence, we can construct a lowpass filter from the biquadratic transfer function as illustrated below.

Consider the general form of a second order biquadratic transfer function

$$H(s) = \frac{v_o(s)}{v_{in}(s)} = -\frac{k_2 s^2 + k_1 s + k_o}{s^2 + (\frac{\omega_o}{Q})s + \omega_o^2} \qquad (5.1)$$

where ω_o = the pole frequency

Q = the pole Q

If the pole is $s_p = \rho_p \pm j\omega_p$ then

$$\omega_o = (\rho_p^2 + \omega_p^2)^{\frac{1}{2}} = |s_p| \qquad (5.2)$$

$$Q = \frac{\omega_o}{2\rho_p} = \frac{|s_p|}{2\rho_p}$$

To construct a lowpass filter, the numerator of (5.1) needs to be only a constant, so we set k_2 and $k_1 = 0$ to produce:

$$H(s) = \frac{v_o(s)}{v_{in}(s)} = -\frac{k_o}{s^2 + (\frac{\omega_o}{Q})s + \omega_o^2} \qquad (5.3)$$

From (5.3), we will use integrators to simulate the transfer function by arranging integrators in such a way that the input and output realize current and voltage respectively. Hence, Equ (5.3) will be rewritten in such a way that the above discussion can be applied as illustrated below:

$$s^2 v_o = -k_o v_{in} - (\frac{\omega_o}{Q}s + \omega_o^2)v_o$$

$$v_{out} = -\frac{1}{s}(\frac{\omega_o}{Q}v_{out} - \omega_o v_1) \qquad (5.4)$$

$$v_1 = \frac{-1}{s}\left(\frac{k_o}{\omega_o} v_{in} + \omega_o v_{out}\right) \qquad (5.5)$$

The transfer function of (5.4) can be represented as an integrator where the feedback capacitor from output voltage to inverting node = 1. At the inverting node, the currents that are equal to $\frac{v_o}{\frac{Q}{\omega_o}}$ and $-\frac{v_1}{\frac{1}{\omega_o}}$ will flow through the feedback capacitor as illustrated in the below figure:

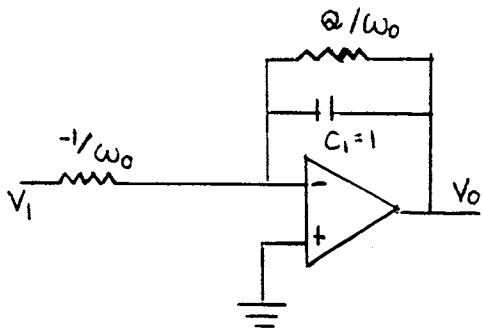


Fig. 5.4. A lossy integrator.

For (5.5), we still use the same method as explained above and end up with a circuit shown below.

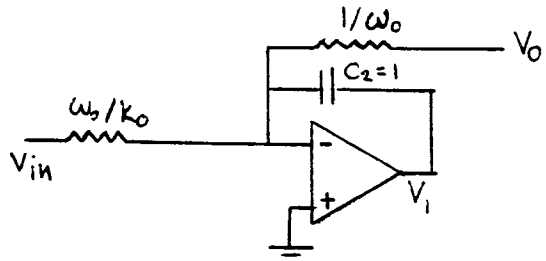


Fig. 5.5. A circuit diagram of Eq.(5.5)

So the whole circuit can be realised by a combination of Fig. 5.4. and Fig. 5.5.

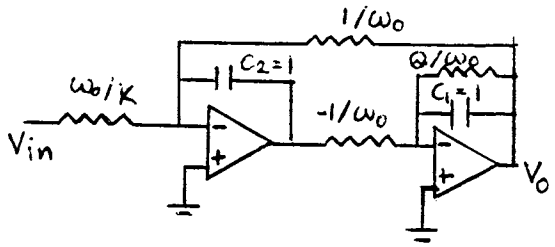


Fig. 5.6. Circuit diagram of a biquadratic transferfunction

Then the transfer function of the circuit in Fig. 5.6. will be as given by (5.3). We can replace positive and negative resistors by stray insensitive switched capacitor models.

We first consider the performance of a stray insensitive integrator that is illustrated below.

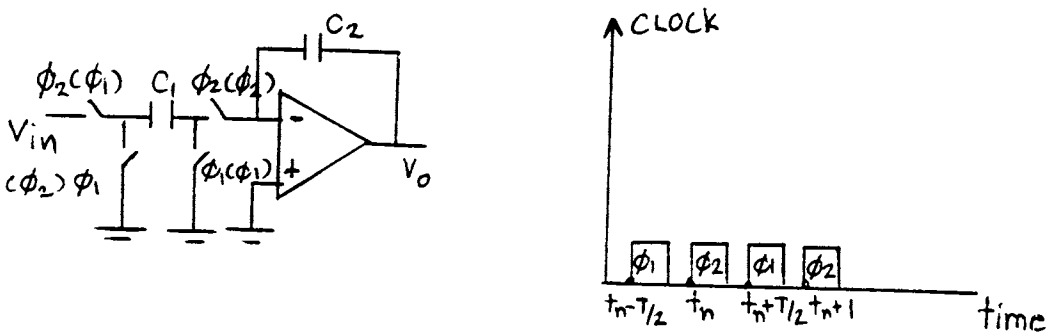


Fig. 5.7. A stray insensitive SC integrator.

Fig. 5.7. represents a stray insensitive SC integrator. We will first consider the transfer

function of this circuit for the clock phase outside the parenthesises.

We assume that input voltage is a sampled signal. It changes the state when clock Φ_2 goes high.

at C_1 when $\Phi_2 = on$ at $t = t_n$

$$\Delta Q(t_n) = C_1 \Delta v(t_n) = C_1 (v_{in}(t_n))$$

at C_2 when $\Phi_2 = on$ at $t = t_n$; $\Delta Q(t_n) = -C_2 \Delta v_o(t_n)$

$$C_1 v_{in}(t_n) = -C_2 (v_o(t_n) - v_o(t_n - T))$$

$$\text{so } \frac{v_o}{v_{in}}(z) = -\frac{C_1}{C_2}(1 - z^{-1}) \qquad (5.6)$$

From (5.6), it is found that when input voltage is increased, output voltage will decrease the same as usual RC integrator. Hence, we can summarize that for the clock phase outside parenthesises, the SC model represents a positive resistor.

For the clock phase inside parenthesises, the SC model represents a negative resistor.

Now, we go back to Fig. 5.6. and replace all positive and negative resistors by SC models, that were described above.

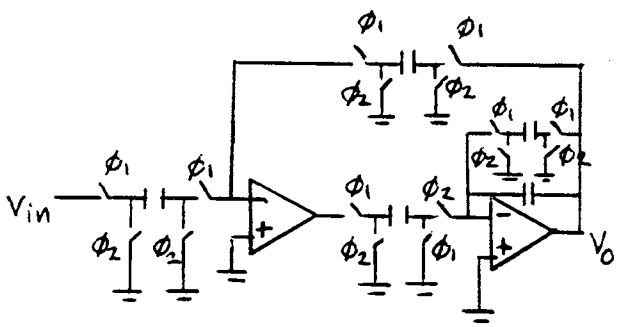


Fig. 5.8. A full switch model of a SC circuit which realises the biquadratic transferfunction.

Althrough Fig. 5.8. realises the desired transfer function, it consumes too many switches. We can save the switches by the following:

Consider a lossy integrator

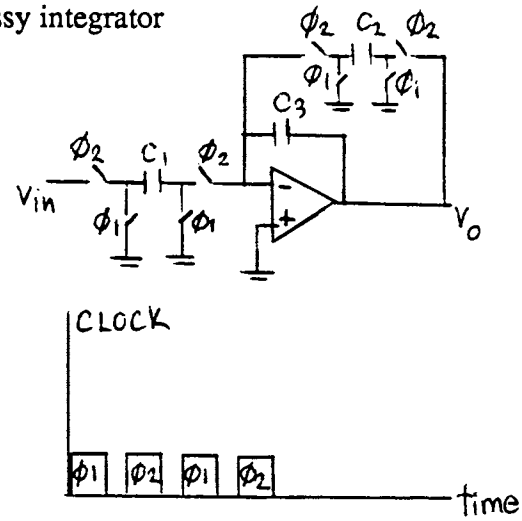


Fig. 5.9. A full switch model of a RC integrator

Consider node 1 and two arguments that are explained below.

1 When clock phase Φ_2 goes high, the charge flows into C_3 and C_2 .

2 When clock phase Φ_1 goes high, C_1 and C_2 discharges.

From the above 2 arguments, we can save the switches as illustrared in the below figure:

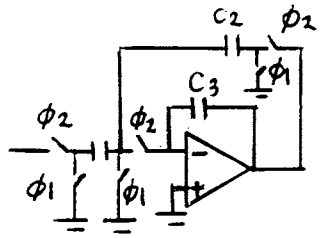


Fig. 5.10. A SC model which the switches are already reduced.

From, Fig. 5.10., the above two arguments are still maintained, so this method can be applied for Fig. 5.8. The final circuit will be as shown below:

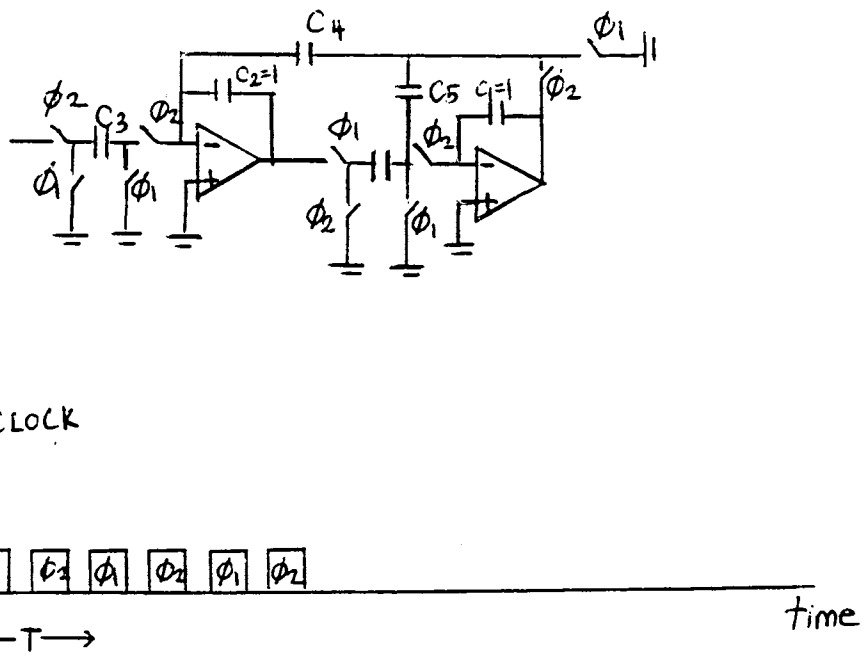


Fig. 5.11. Representation of a SC filter that realises the biquadratic transfer function and the number of switches are already reduced.

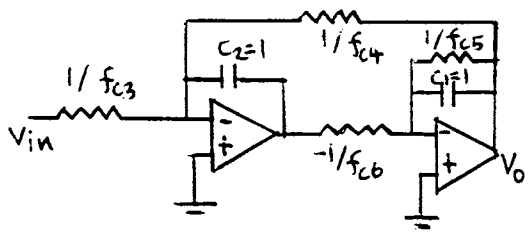
Compare the SC circuits of Fig. 5.11. and the RC circuit of Fig. 5.6. The relationship between each capacitor, clock period and resistor are demonstrated below:

$$\frac{T}{c_3} = \frac{\omega_o}{K}$$

$$\frac{T}{c_4} = \frac{1}{\omega_o} \qquad (5.7)$$
$$\frac{-T}{c_o} = \frac{-1}{\omega_o}$$
$$\frac{T}{c_5} = \frac{Q}{\omega_o}$$

We now find the bandwidth of SC circuit of Fig. 5.11. as illustrated below.

We redraw Fig. 5.11. again and replace each switch by a simulated resistor as illustrated below:



By assuming that $C_1 = C_2 = C_6 = C_5 = C_3 = 1nf$ to simplify the calculation. We eventually get the bandwidth as demonstrated in (5.8)

$$\text{bandwidth} = f_{cut\ off} = \frac{f_{clock}}{2\pi} \left[\frac{(2C_4 - 1) + ((1-2C_4)^2 + 4C_4^2)^{\frac{1}{2}}}{2} \right]^{\frac{1}{2}} \qquad (5.8)$$

We now consider a cosine function which is used to improve the performance of the decimator.

A SC circuit that produces the cosine function is illustrated below.

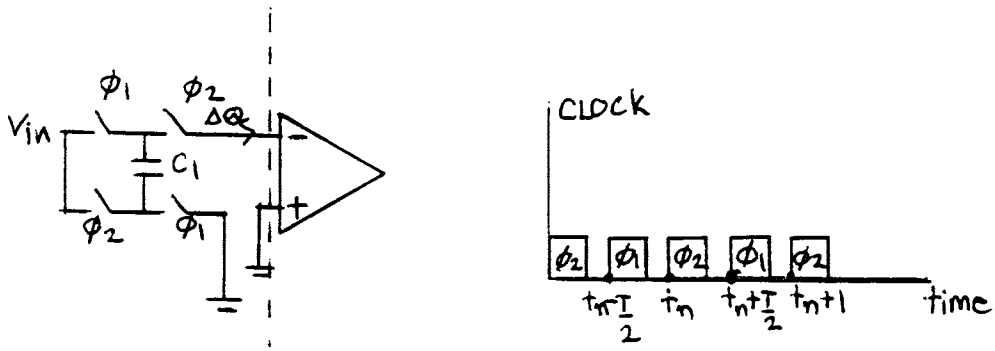


Fig. 5.12. A cosine filter.

$$at\ \ t=t_n \quad \Delta Q(t_n)=C_1\Delta v(t_n) = C_1(v_{in}(t_n)+v_{in}(t_n-\frac{T}{2}))$$

so:

$$\frac{\Delta Q}{v_{in}}(z) = C_1(1+z^{\frac{-1}{2}}) \qquad (5.9)$$

$$\frac{\Delta Q(e^{j\omega T})}{v_{in}} = 2C_1\cos\frac{\pi f}{2f_c} \qquad (5.10)$$

Consider the amplitude response of (5.10) which has a cosine function.

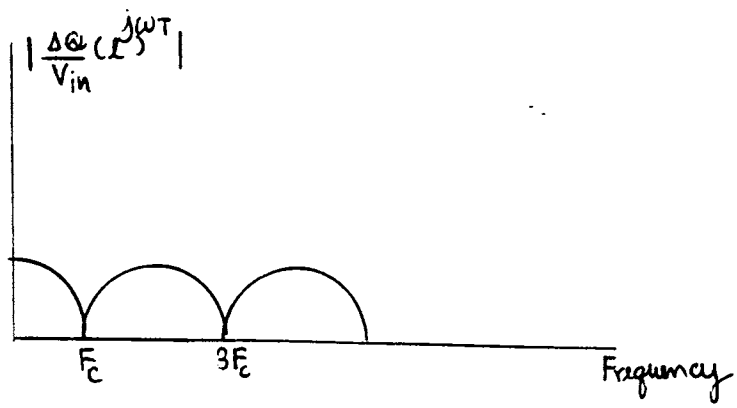


Fig. 5.13. The amplitude response of a cosine function.

From Fig. 5.13., it apparently determines that this cosine function has nulls in its response at nf_c, where n = 1,3,5,...(odd).

This cosine function can be applied to the decimator by modification at the input of the decimator as stated previously.

(Note that if we would like to introduce a cosine function into a decimator , we can not cascade them because the transfer function of (5.10), which is the cosine function, is not the ratio between output voltage and input voltage, but it is the ratio between output charge Q(z) and input voltage $v_{in}(z)$.)

We will now consider how to modify the input of decimator Fig. 5.11 and introduce the cosine function.

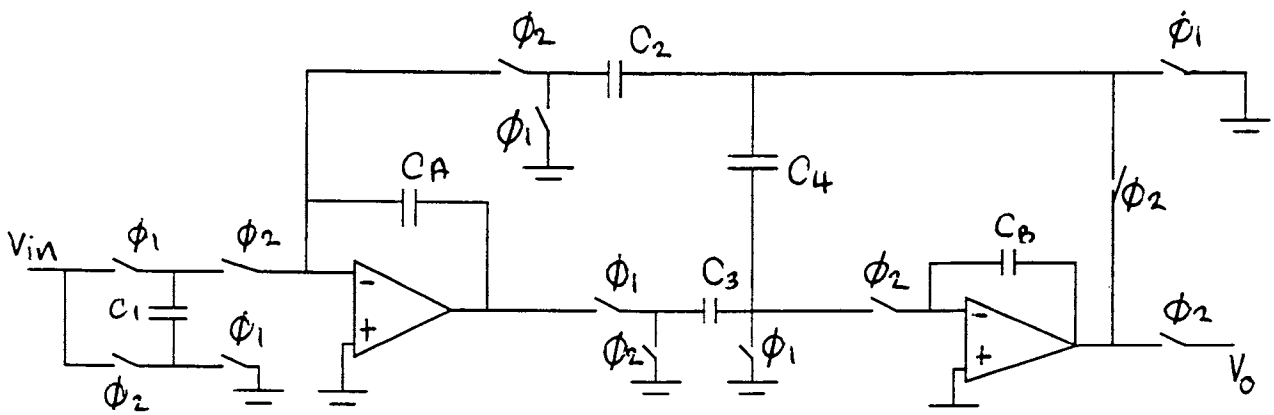


Fig. 5.14. A cosine decimator filter.

The circuit that is illustrated in Fig. 5.14. is a decimator, which the input is already

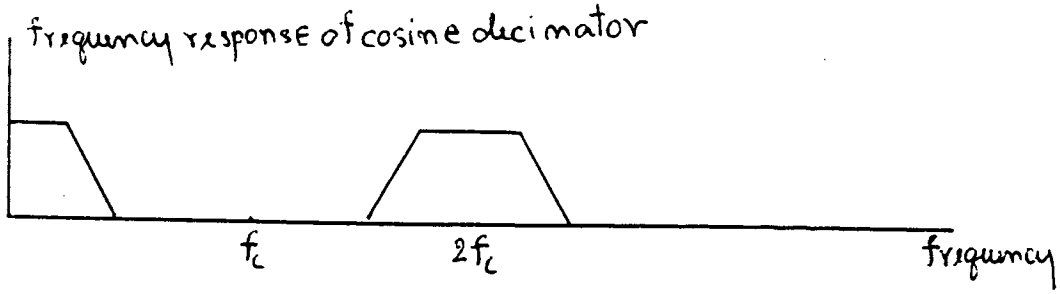
modified by introducing a cosine function, so the new transfer function will be

$$|H(z)| \text{ the overall transformation} = |H_1(z) \times H_2(z)| \qquad (5.11)$$

$H_1(z)$ = the transfer function of decimator.

$H_2(z)$ = the cosine function = $k\cos\frac{\pi f}{2f_c}$

We then demonstrates the amplitude response of (5.11) in the below figure.



f_c = clock frequency of cosine decimator filter.

$2f_c$ = sampling frequency of a cosine decimator filter.

f_c = Nyquist limit of a cosine decimator.

Fig. 5.15. Frequency response of a cosine decimator filter.

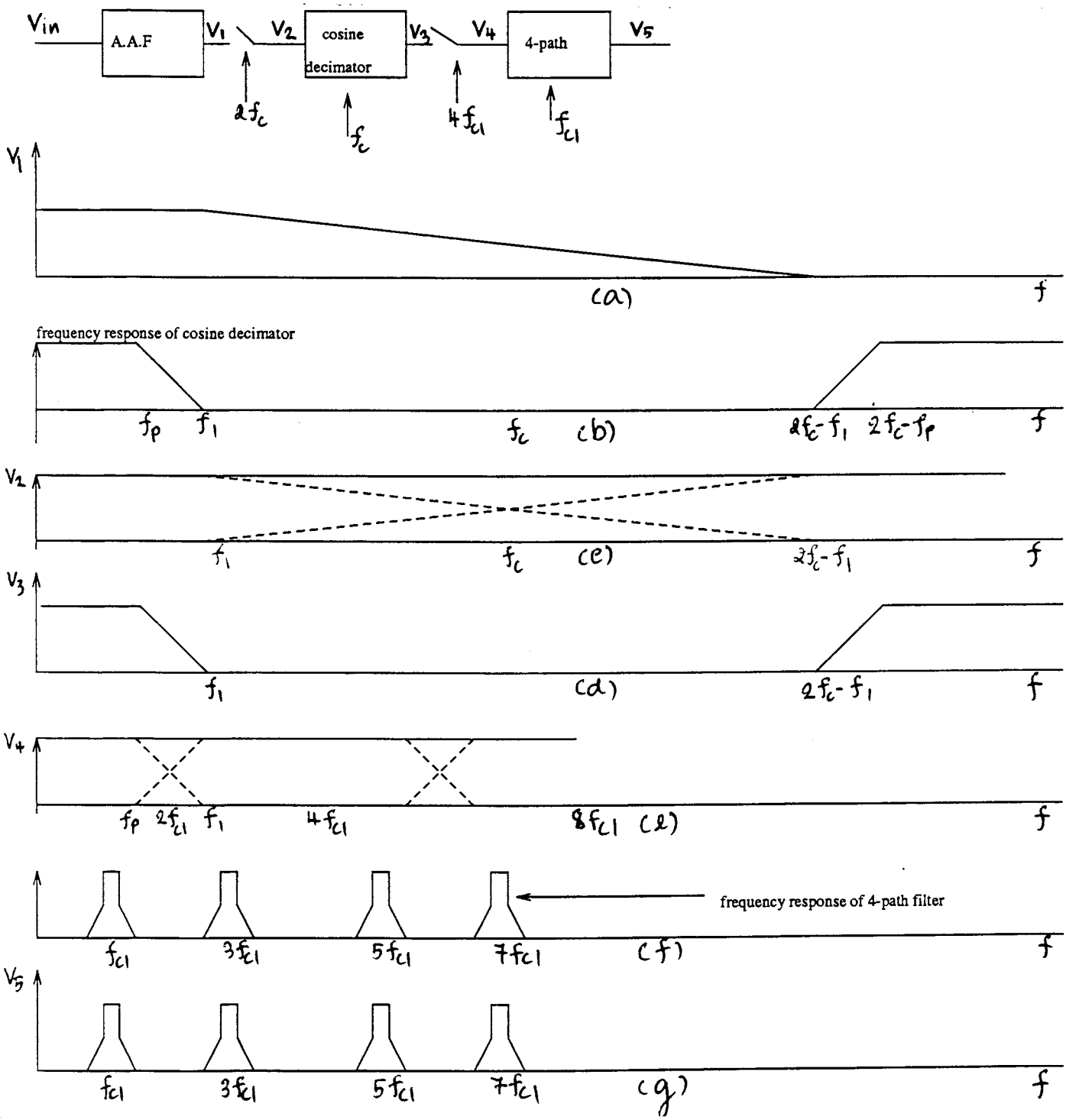
This transfer function which comes from the modification at the input of the original decimator is called cosine decimator. This cosine decimator runs at the clock frequency equal to f_c, but the effective sampling frequency is $2f_c$. As a result, the Nyquist limit of this cosine decimator will be f_c instead of $\frac{f_c}{2}$ for a normal decimator.

From the frequency response of the cosine decimator, it is found that this cosine decimator will simplify the requirements of AAF a lot more than conventional decimation filters normally do.

5.3 THE DESIGN OF THE CO-OPERATION BETWEEN THE ANTIALIASING FILTER, COSINE DECIMATOR AND SC BANDPASS 4-PATH FILTER.

We now consider the operation of the co-operation between an AAF, a cosine decimator and a 4-path filter in Fig. 5.16. The result of the testing of this operation will be shown in Chapter 6.

f_c = the clock frequency of the cosine decimator. f_{c1} = theclock frequency of the bandpath 4-path filter. f_1 = the stopband of the cosine decimator.



Assume that input frequency is a band of frequency.

Fig. 5.16(a) shows the frequency spectrum of v_1.

In Fig. 5.16(b), the solid line represents the frequency response of the cosine decimator.

In Fig. 5.16(c), the dashed line represents how aliasing occurs. When the input frequencies go beyond the Nyquist limit of the cosine decimator, which is f_c, it will fold ((aliased) back. From Fig. 5.16(c), the input frequencies between $2f_c - f_1$ and f_c, which are greater than f_c, will fold back to the frequencies between f_1 and f_c as illustrated by the dashed line. The arithmetic sum of the magnitude of the dashed line will be the solid line, which is actually the frequency spectrum of v_2.

(Note that it is very important to keep the area that aliasing occurs out of the passband, or the information in the passband will become non-linear distortion.)

Fig. 5.16(d) shows the frequency spectrum of v_3. We apparently see that the area of the frequency spectrum of v_2 (solid line), where aliasing occurs , will be suppressed by the stopband of the cosine decimator in Fig. 5.16(b).

Fig. 5.16(e), the solid line and the dashed line show the frequency spectra of v_4 and aliasing respectively. From Fig. 5.16(e), we see that the frequencies of v_3, that go beyond the Nyquist limit $2f_{c1}$ of a 4-path filter, will be fold (aliased) back as illustrated by the dashed line. The arithmetic sum of the magnitude of the dashed line will actually be the frequency spectrum of v_4 (solid line).

In Fig. 5.16(f), the solid line represents the frequency response of a 4-path filter which has the centre frequency at f_{c1} , $3f_{c1}$,...

Fig. 5.16(g) represents the frequency spectrum of v_5 . The stopband of the 4-path filter will suppress the area, where the aliasing occurs in the frequency spectrum of v_4 .

From the above argument, it apparently shows that the stopband frequency of the anti-aliasing filter can be $2f_c - f_1$ instead of $2f_{c1}$, where $2f_{c1}$ is the Nyquist limit of the 4-path filter. Hence, the high order of the anti-aliasing filter is no longer required due to the effective performance of the decimator.

In Chapter 6, the testing of this operation will be done. The input frequency will be a single sinusoidal frequency in stead of a full-band of the frequency.

We now consider the design rule, which is going to be tested in section 6.8 of Chapter 6. (By using the principle which is illustrated in Fig. 5.16.)

1. The stopband frequency of the anti-aliasing filter has to be less than $2f_c - f_1$.

2. The stopband of the cosine decimator (f_1) has to be less than $3f_{c1}$.

(Note again that the input signal is a single sinusoidal waveform)

3. The clock frequency of the cosine decimator has to be high enough to get wide stopband , but it may cause the cut off frequency of the cosine decimator wider. Hence, the clock frequency and the stopband of the cosine decimator have to be compromised.

5.4 INTERPOLATOR FILTER

Consider the frequency spectrum of a sampled and held signal at the output of a switched-capacitor filter circuit which is illustrated below.

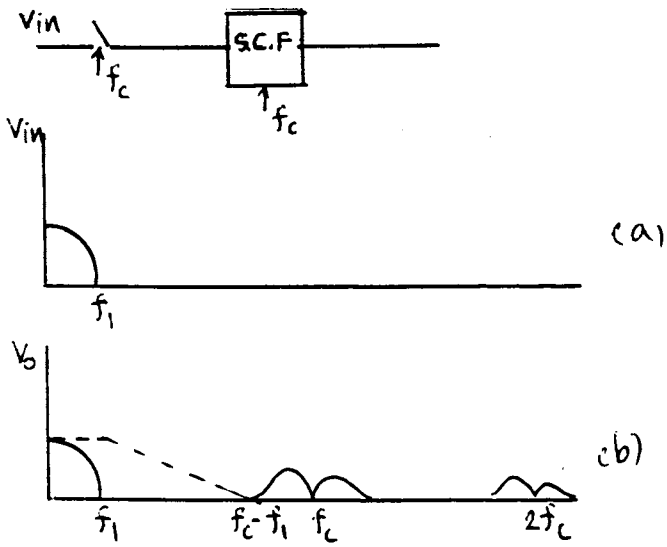


Fig. 5.17(a) The frequency spectrum of the input

(b) The frequency spectrum of the output is represented by the solid line. The dashed line represents the frequency response of a smoothing filter.

The frequency spectrum of the sampled and held output signal is attenuated by the characteristic S/H function, which is often called $\frac{\sin x}{x}$ response. (The detail of $\frac{\sin x}{x}$ response has already been mentioned in the previous chapter.) To convert the sampled and held signal to a continuous-time signal, a lowpass filter is needed to eliminate the unwanted frequency components. From Fig. 5.17., the lowpass filter which has a stop band at $f_c - f_1$ will eliminate the harmonics of the sampled and held output signal at nf_c where n = 1, 2, 3,.... This lowpass filter is often called a smoothing filter (SMF). If the sampling frequency of the switched capacitor filter is low, a high order of SMF will be required. Then the structure of SMF will be more complex and a large chip area will be consumed.

In order to relax the specification of SMF, the sampling frequency of SCF could be increased, but the drawback is that again for a two phase clock, the unity-gain bandwidth of the op-amp should be at least five times as large as the clock frequency, or the distortion may occur at the output.

A solution to simplify the requirements of the SMF is by using a well known interpolator and add it between a sample data system and a SMF.

5.5 THE PRINCIPLE OF THE INTERPOLATOR

The operation of the interpolator is that it increases the sampling rate of the signal by some integer factor r. The values of the increased samples can be obtained by linear interpolation. This method is illustrated for impulse sampling in the below figure Fig. 5.18. and for the sampled and held signal in Fig. 5.18(b)

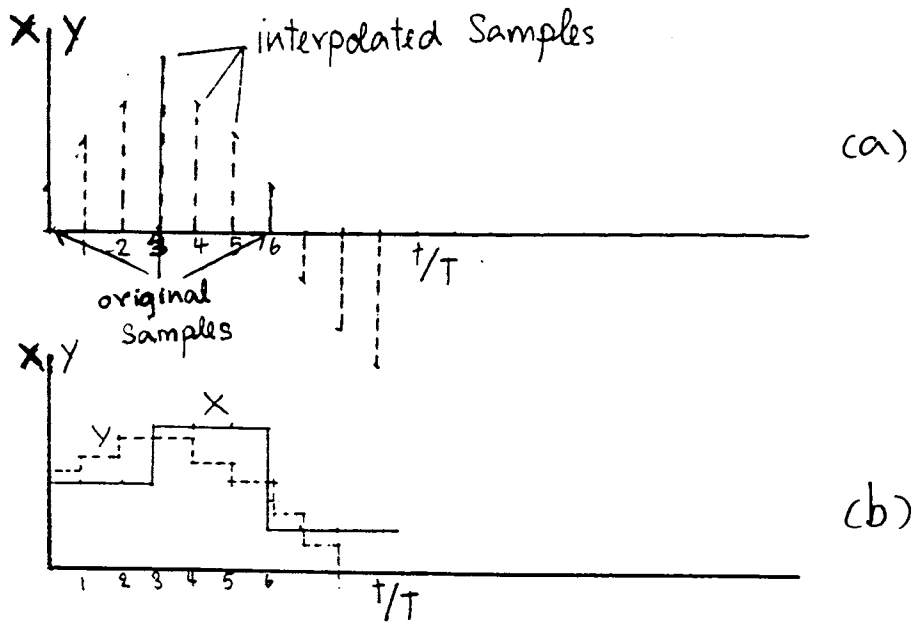


Fig. 5.18. (a) impulse-sampled signal
(b) sampled and held signal

In Fig. 5.18(b), the input signal x(t) is shown as a continuous-line, the interpolated signal y(t) as a broken line. The ratio r of the sampling period is three in this example.

We next will consider how to obtain the transfer function of the circuit used to produce y(t) from x(t).

We shall define the sequence x_n such that x_n = x(nT) for $n = 0, \pm r, \pm 2r, \ldots,$ and $x_n = 0$ for other values of n. We shall also define a sequence $U_n = \sum_{k=0}^{r-1} x_{n-k}$. Thus, U_n is obtained by holding the value of x_n constant between nonzero samples. From Fig. 5.18(a), therefore, $y_n = y(nT)$ satisfies;

$$y_n - y_{n-1} = \frac{(U_n - U_{n-r})}{r}$$

$$= \frac{1}{r}\sum_{k=0}^{r-1} (x_{n-k} - x_{n-k-r})$$ Then, apply z-transform in to both sides:

$$(1-z^{-1})Y(z) = \frac{1-z^{-r}}{r}\sum_{k=0}^{r-1} z^{-k}X(z)$$

$$\frac{Y(z)}{X(z)} = \frac{1}{r}\left[\frac{1-z^{-r}}{1-z^{-1}}\right]^2 = \frac{1}{r}[\sum_{k=0}^{r-1} z^{-k}]^2$$

$$= \frac{1}{r}[H_1(z)]^2$$

$$\frac{Y}{X}(z) = \frac{1}{r}\left[\frac{1-z^{-r}}{1-z^{-1}}\right]^2 \qquad (5.12)$$

The frequency response is obtained by replacing z by $e^{j\omega T}$

$$H(e^{j\omega T}) = \frac{1}{r}\left[\frac{\sin(\frac{r\omega T}{2})}{\sin(\frac{\omega T}{2})}\right]^2 \qquad (5.13)$$

If the sampling frequency is a lot higher than the input frequency ($\frac{\omega T}{2} \ll 1$), then the above equation can be expressed as shown in the following equation:

$$H(e^{j\omega T}) = r\left[\frac{\sin(\frac{r\omega T}{2})}{(\frac{r\omega T}{2})}\right]^2 \qquad (5.14)$$

We can plot this easily because it is similar to the $\frac{\sin x}{x}$ function. We now consider at which frequencies, the (5.14) has high attenuation.

$$\frac{r\omega T}{2} = n\pi \quad n = 0,1,2,3,.....$$

At $f = n\frac{f_c}{r}$, then the frequency response of (5.14) has high attenuation as illustrated below:

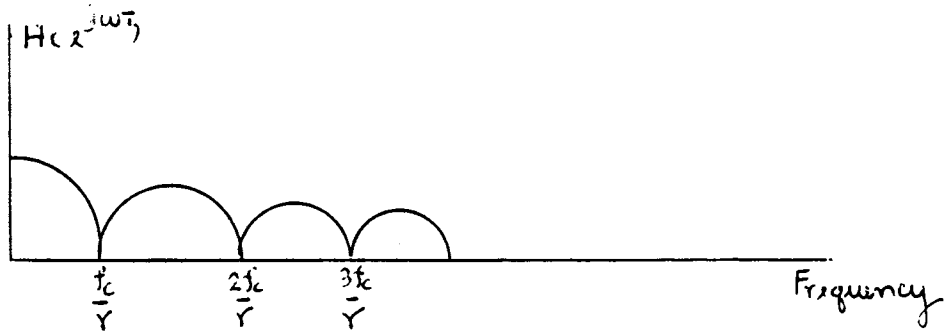
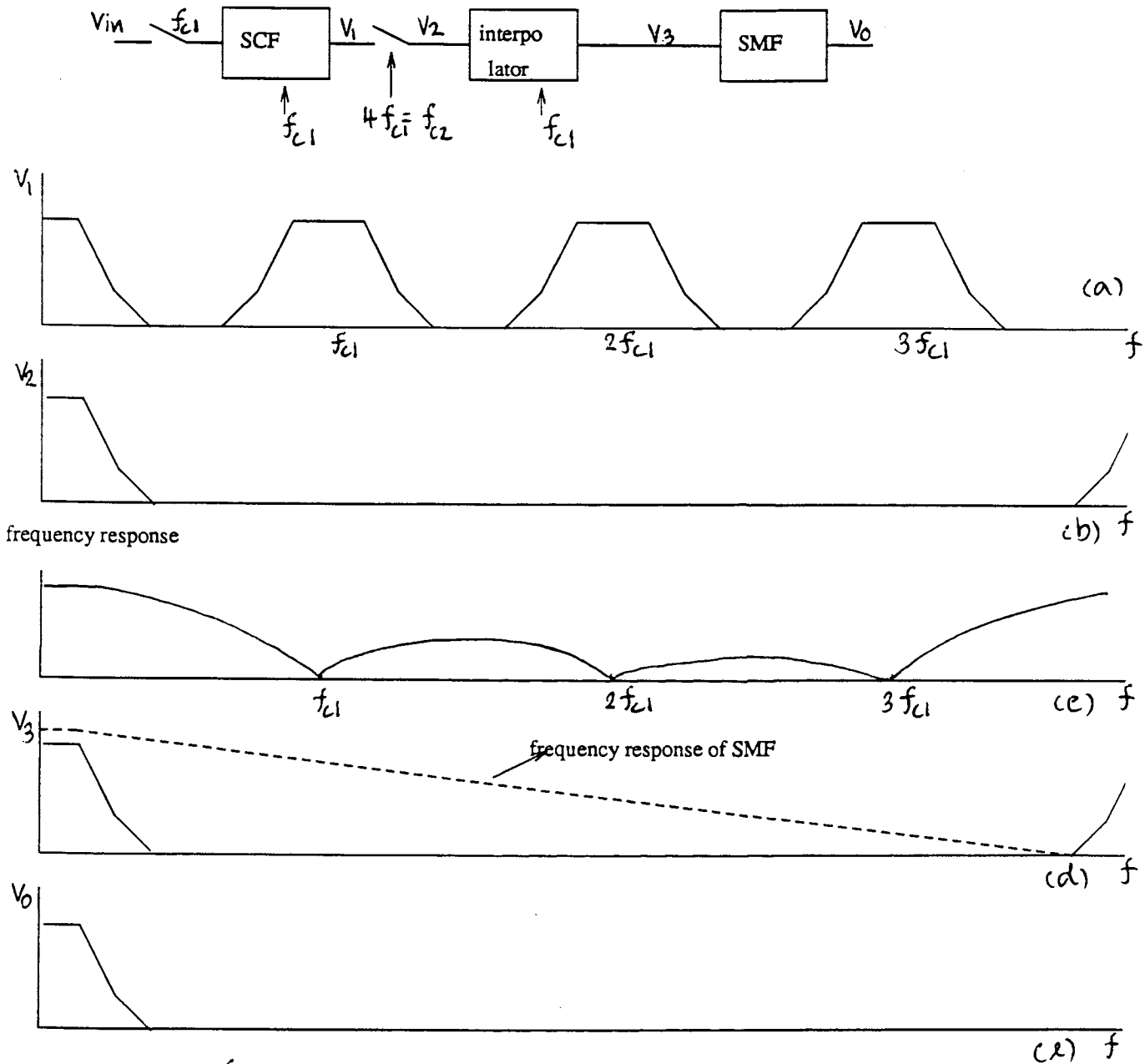


Fig. 5.18. The frequency response of Eq.(5.14)

Now we consider the performance of the whole system after the interpolator is inserted between a sampled data system and a SMF.



f_{c1} = the clock frequency of SCF

r = linear interpolation = 4

$4f_{c1}$ = the sampling frequency of interpolator filter = f_{c2}

Fig. 5.20 The performance of an interpolator when it is combined with a sampled data system and a smoothing filter.

Fig. 5.20(a) shows the frequency spectrum of signal at v_1.

Fig. 5.20(b) shows the frequency spectrum at v_2 after it is sampled by sampling frequency(f_{c2}) , which is equal to r times f_{c1}, where f_{c1} is the clock frequency of SCF and r is the interpolation ratio.

Fig. 5.20(c), again illustrates the frequency response of an interpolator filter.

In Fig. 5.20(d), the solid line demonstrates the frequency spectrum of signal at v_3. Compare with (a) we clearly see that the first harmonic is moved further away from f_{c1} to f_{c2}, so the requirements of the smoothing filter can be simplified. The dashed line represents the frequency response of the smoothing filter.

In Fig. 5.20(e), the resulting output signal from SMF will eventually become a continuous-time signal.

Now, we consider an interpolator filter circuit that realizes the (5.12).

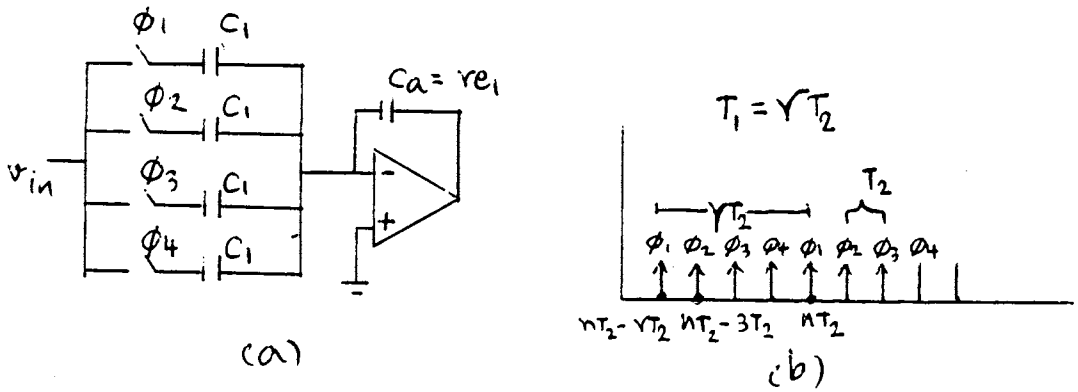


Fig. 5.21. An interpolation filter.
(a) interpolation filter
(b) clock signals

r = linear interpolation ratio

at $t = nT_2$, consider C_1 ($T_1 = rT_2$)

$$\Delta Q(nT_2) = C_1 \Delta v(nT_2) = C_1(v_{in}(nT_2) - v_{in}(nT_2 - T_1)) \qquad (5.15)$$

consider at C_a

$$\Delta Q(nT_2) = C_a(-v_o(nT_2) - (-v_o(nT_2-T_2)) = C_a(v_o(nT_2-T_2)-v_o(nT_2)) \qquad (5.16)$$

(5.16) = (5.15) so $C_1(v_{in}(nT_2) - v_{in}(nT_2-T_1)) = C_a(v_o(nT_2-T_2) - v_o(nT_2))$

but $C_1 = \frac{C_a}{r}$, $T_1 = rT_2$

$$\frac{1}{r}(v_{in}(nT_2) - v_{in}(nT_2-rT_2)) = (v_o(nT_2-T_2) - v_o(nT_2))$$

$$H(z) = \frac{v_o}{v_{in}}(z) = -\left[\frac{1}{r}\right]\left[\frac{1-z^{-r}}{1-z^{-1}}\right] \qquad (5.17)$$

$$H(e^{j\omega T}) = \frac{1}{r}\left|\frac{\sin(\frac{r\omega T_2}{2})}{\sin(\frac{\omega T_2}{2})}\right| \qquad (5.18)$$

From (5.18), it is not exactly the same as (5.13), which we want, since in the analysis, we do not include the sampled and held system into our consideration. (Note that this is always the problem when we use z-transformation to analyze SC-circuit.)

If $\frac{\sin x}{x}$ response which is a characteristic of the sampled and held signal, is included into (5.18), Equ (5.13) can be obtained from SC-circuit of Fig. 5.20. (Note that, in Fig. 5.19. the frequency response of the interpolator can not eliminate the harmonic $4f_{c1}$ of the spectrum of v_2. The reason is explained below.)

The transfer function of interpolator is $= \frac{1}{r}\left|\frac{1-z^{-r}}{1-z^{-1}}\right|^2 = H(z)$

$$\text{so } H(e^{j\omega T}) = \frac{1}{r}\left[\frac{\sin(\frac{r\omega T}{2})}{\sin(\frac{\omega T}{2})}\right]^2$$

where $T = \frac{1}{4f_{c1}}$; f_{c1}= *clock frequency of the interpolator*

$4f_{c1}$ = the sampling frequency of the interpolator filter.

From Fig. 5.19., r = linear interpolation ratio = 4,.so:

$$H(e^{j\omega T}) = \frac{1}{4}\left[\frac{\sin(\frac{4\omega T}{2})}{\sin(\frac{\omega T}{2})}\right]^2 \qquad (5.19)$$

At the input frequencies, where Equ (5.19) has high attenuation, are nf_c , where n = 1,2,3 only. At n = 4, the denominator of Equ (5.19) will be zero. Hence, the frequency response of the interpolator, which has the linear interpolation ratio at four, does not have high attenuation at $4f_c$, where f_c is the clock frequency of the interpolator.

5.6 THE DESIGN OF THE CO-OPERATION BETWEEN THE 4-PATH FILTER, INTERPOLATOR AND SMOOTHING FILTER.

We now connect an interpolator and a smoothing filter at the output of a 4-path filter. We will redraw and extend the block diagram of Fig. 5.16. by putting an interpolator and a smoothing filter as illustrated below. We will also continue to demonstrate the appearance of the frequency spectrum at each node since v_5 to v_{out} .

f_{c1} = clock frequency of 4-path filter.

$4f_{c1}$ = clock frequency of the interpolator.

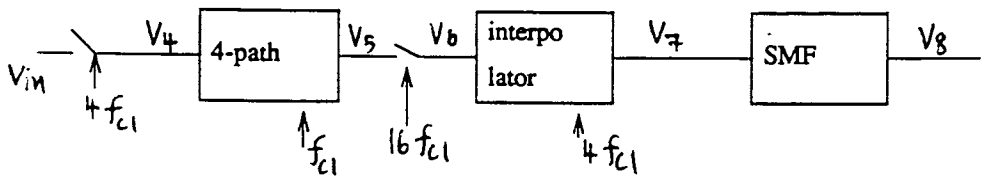
$4f_{c1}$ = sampling frequency of 4-path filter.

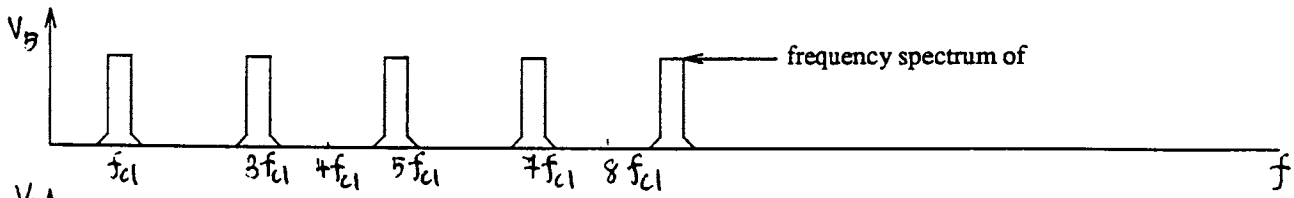
$16f_{c1}$ = sampling frequency of the interpolator.

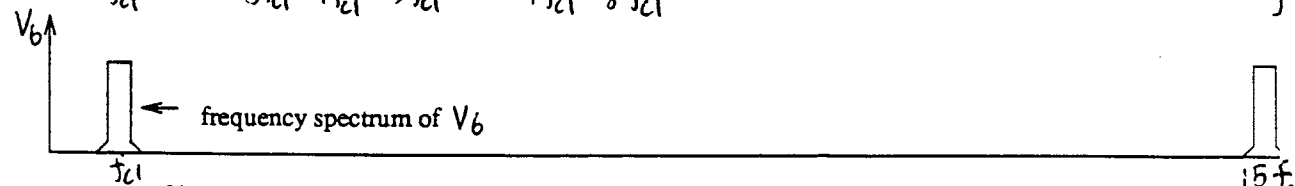
The above symbols will still be used in the section 6.9 in Chapter 6 to prevent confusion.

continue from Fig. 5.16.

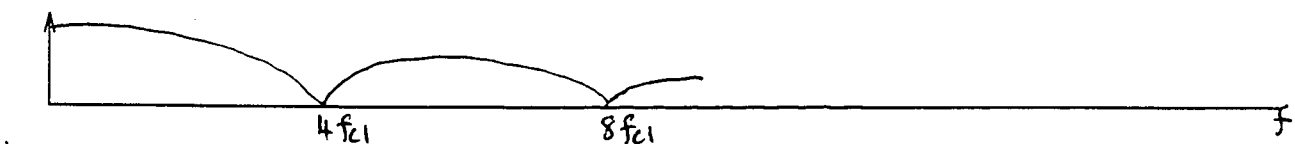
(continue from Fig. 5.16.)







frequency response of interpolator filter



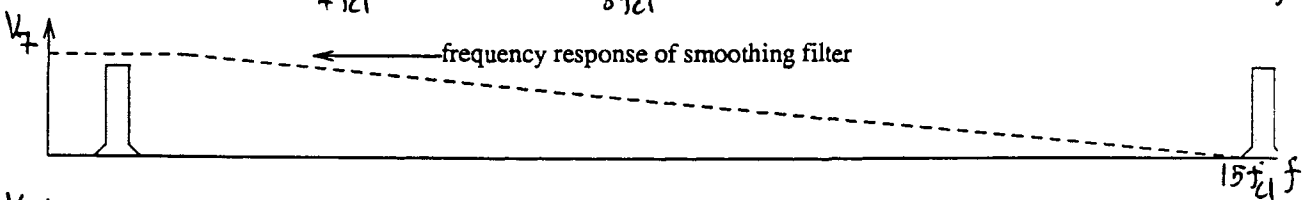


Fig. 5.22. (h) the frequency spectrum of v_5.

(i) the frequency spectrum of v_6.

(j) the frequency response of the interpolator filter.

(k) The solid line represents the frequency spectrum of v_7 . The dashed line represents the frequency response of a smoothing filter.

(l) the frequency spectrum of the output signal.

Form the above Fig. 5.22., it apparently shows that the stopband of the smoothing filter can approximately be $15f_{c1}$ in stead of $3f_{c1}$. Hence, the high order of the smoothing filter is no longer required due to the effective performance of the interpolator.

In Chapter 6, the testing of this operation will be done in section 6.5. For the testing, the input frequency is a single sinusoidal signal.

We now consider the design which is going to be used in section 6.5 in Chapter 6.

(By using the principle that is given in Fig. 5.22.)

1. The clock frequency of the interpolator has to be the same as the overall sampling frequency of the N-path filter. In section 6.5 of Chapter 6, we use 4-path filter, therefore the clock frequency of the interpolator will be $4f_{c1}$, where f_{c1} is the clock frequency of the 4-path filter.

2. The stopband of the smoothing filter has to be less than $15f_{c1}$, where f_{c1} is the clock frequency of the 4-path filter. (Note again that the input signal is a single sinusoidal waveform.)

CHAPTER 6

TESTING AND IMPLEMENTATION

INTRODUCTION

The decimator, interpolator and N-path filter which were described in the previous chapters have all been constructed and tested. The results are presented in this chapter. The decimator can function as an input stage and the interpolator as an output stage in a filter system. This allows the use of differing clock rates in the various stages of the system, which can result in simpler antialiasing requirements.

In these experiments, the frequency response of cosine decimator, 4-path filter and interpolator circuit will be shown.

At the end of this chapter, all of decimator, 4-path filter and interpolator will be combined in order to show how cosine decimator and interpolator simplify the requirements of antialiasing and smoothing filter respectively.

6.1 DECIMATOR

The cosine decimator circuit which is tested in this experiment is illustrated below. (The detail and design of this circuit were already described in Chapter 5.)

It was constructed as a discrete component prototype and capacitance values are scaled up by approximately 200 the values that would be used on chip. The comercial standard components used are:

IC type MC 14016 BCP is used as a switch. LF 347 N is used as an op-amp. For the two non-overlapping clock phases, an 4013 dual D-type is used as a divide-by-4 counter and a 4011 dual package is used to produce two non-overlapping clock phases which run at one-quarter the input clock rate.

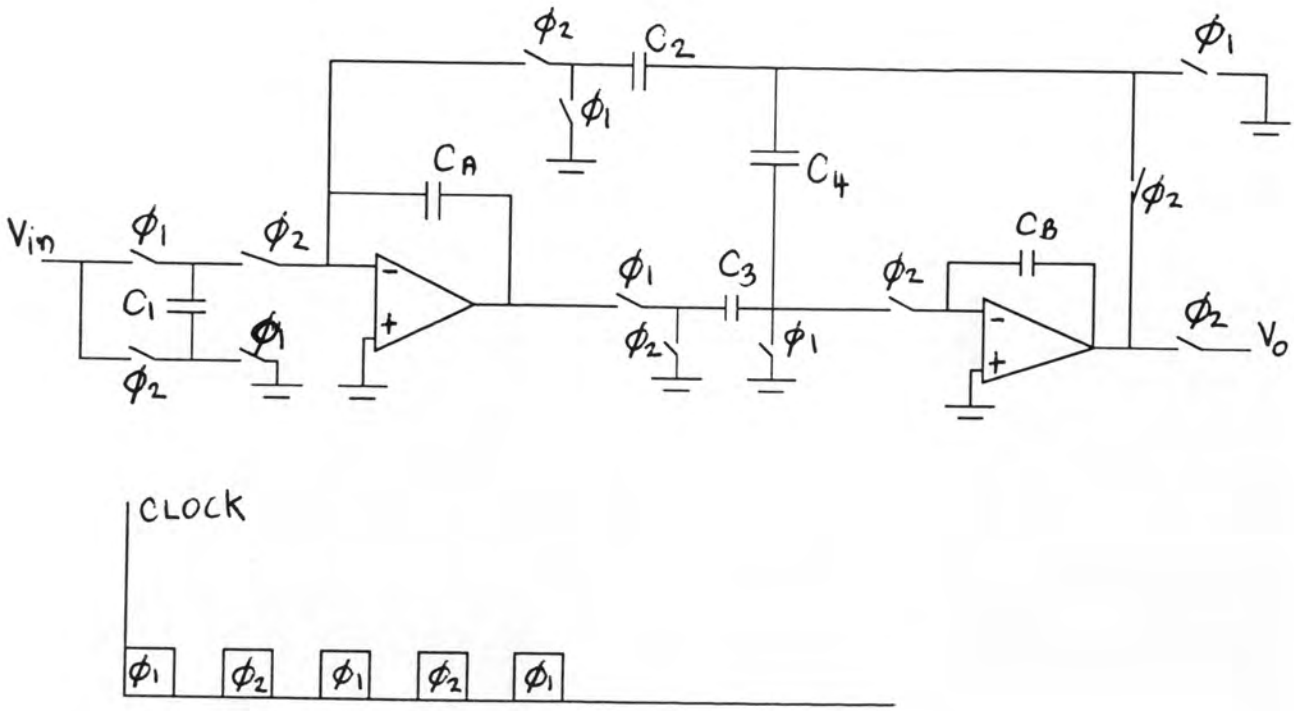


Fig. 6.1. A cosine decimation filter circuit.

After it is supplied by an input sinusoidal signal which runs at 27 kHz, the output waveform is illustrated below.

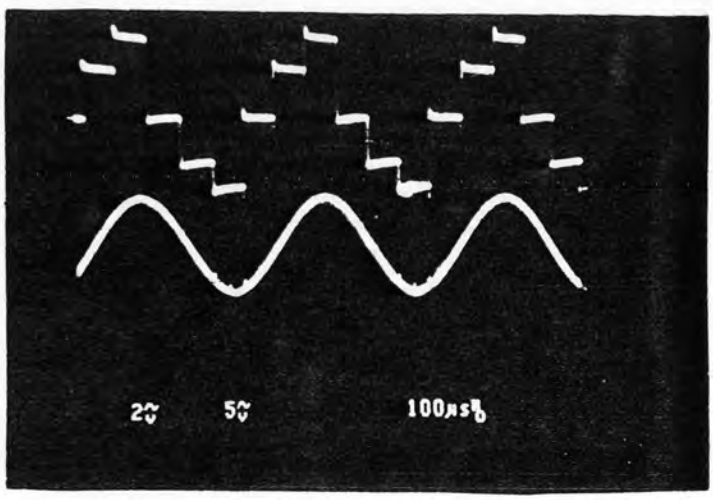


Fig. 6.2. The input and output signal are a sinewave and a sampled and held signal respectively.

The frequency response of the cosine decimator is demonstrated in Fig. 6.3. The element values that are used to get the frequency response in Fig. 6.3. are given below.

($C_a = C_b = C_1 = C_3 = C_4 = 1nf$, $C_2 = .267nf$, clock frequency = 187 kHz, the constant amplitude of the input voltage = .125 volt)

From the measurement, it has the first stopband at 187 kHz which is the clock frequency of the cosine decimator. The bandwidth is about 10.2 kHz. This value is very close to the value which is calculated from Equ (5.8). At the stopband and passband, the voltage gains are about -9.89 db and 24.08 db respectively. From this measurement, it apparently shows that the voltage gain of the stopband is very low due to the effective operation of the cosine filter.

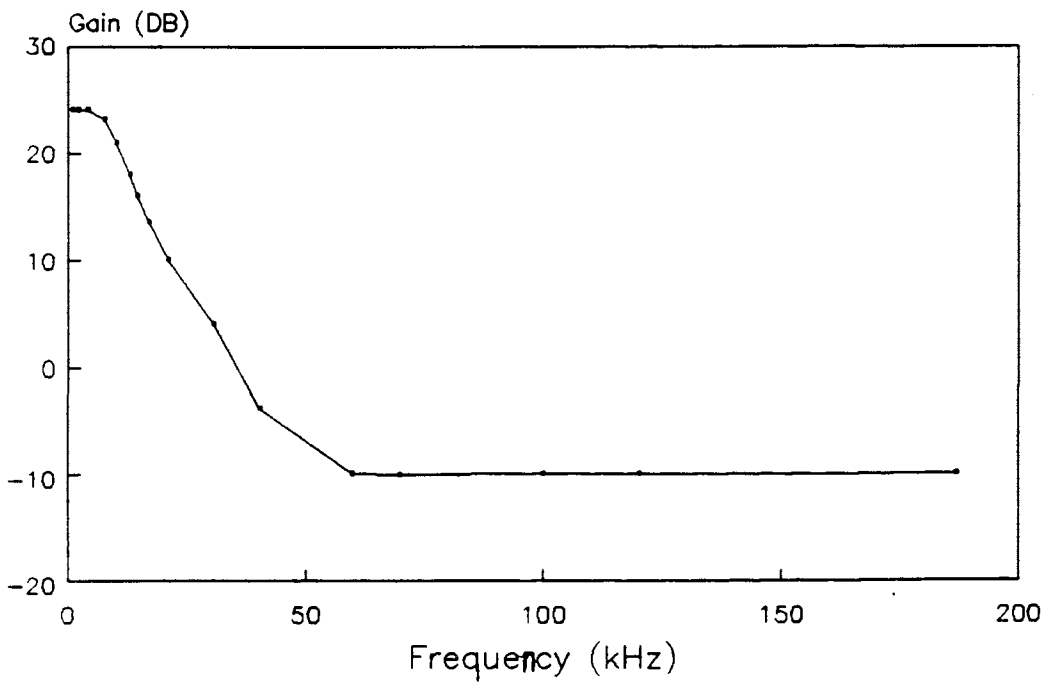


Fig. 6.3. The frequency response of the cosine decimator

6.2 SWITCHED-CAPACITOR BANDPASS 4-PATH FILTER.

A 4-path passive bandpass filter and prefilters are combined and tested. The prefilters and a 4-path filter circuit are redrawn again as illustrated below: (The purpose of prefilter is to provide a bandstop at $2f_{c1}$, $4f_{c1}$, $\cdots$, where f_{c1} is the clock frequency. These use the capacitors marked C_1.)

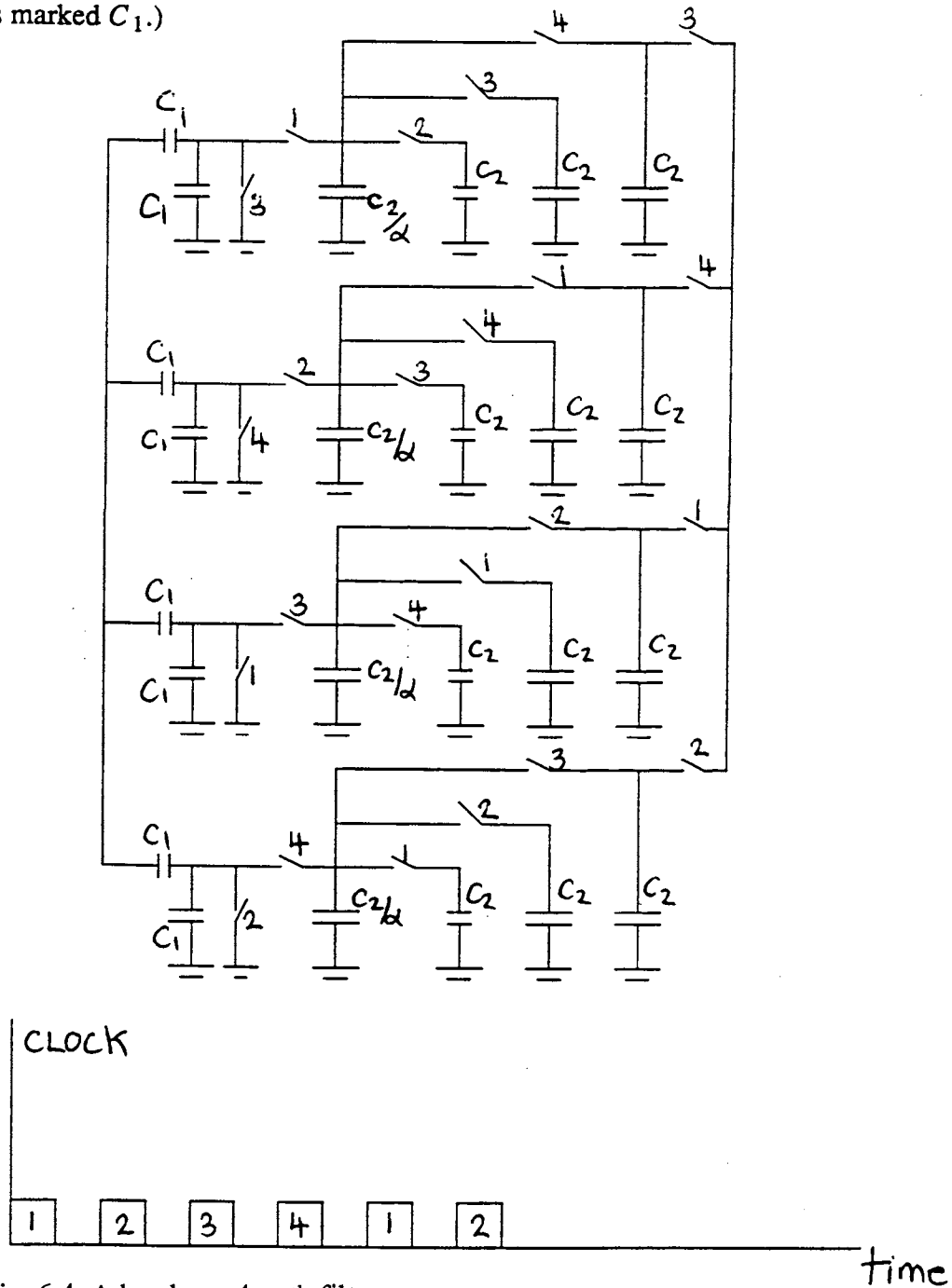


Fig. 6.4. A bandpass 4-path filter.

(a) A bandpass filter

(b) Clock signals

When the circuit is supplied by an input signal at the same frequency as the clock (f_{c1}), the output waveform is obtained in Fig. 6.5.

IC number MC 14016 BCP is used as a switch. $C_1 = .7\ nf\ C_2 = 10.487\ nf\ \frac{C_2}{\alpha} = .103\ nf.$ For the four non-overlapping clock phases, DM 74LS193 N is used as a binary counter. DM 74LS138 and 74LS04N are used as a decoder and an inverter respectively.

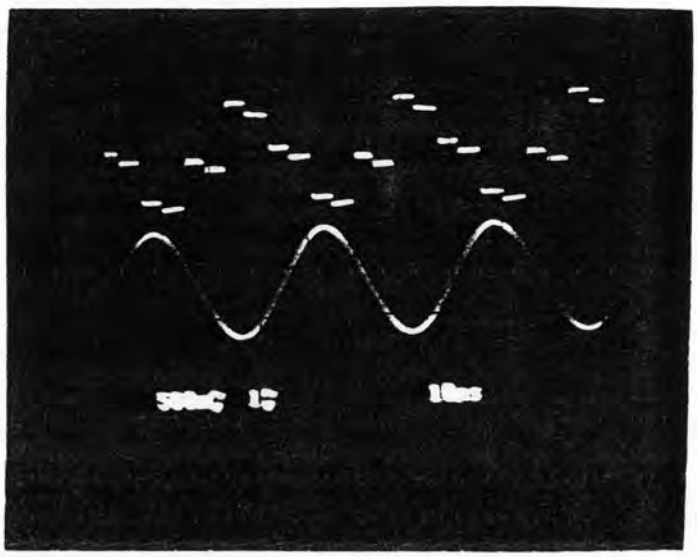


Fig. 6.5. A sampled and held output waveform (upper trace)and a sine wave input signal (lower)

From Fig. 6.5., demonstrates that the output waveform is equivalent to the input waveform and is sampled and held about 4 times due to non-overlapped 4-phase shift of the clock signals. The frequency response of 4-path filter is demonstrated in Fig. 6.6.

From Fig. 6.6., the input frequency will be limited at 8.4 kHz ($2f_{c1}$) due to the Nyquist range. It shows that the prefilters can suppress unwanted bands at 0, $2f_{c1}$, ... , nf_{c1} , where n equals to even integer number.

From the measurement, at a centre frequency equals of 4.18kHz, the bandwidth is about 13.5 Hz. This value is very close to the value that is calculated from Equ (4.9).

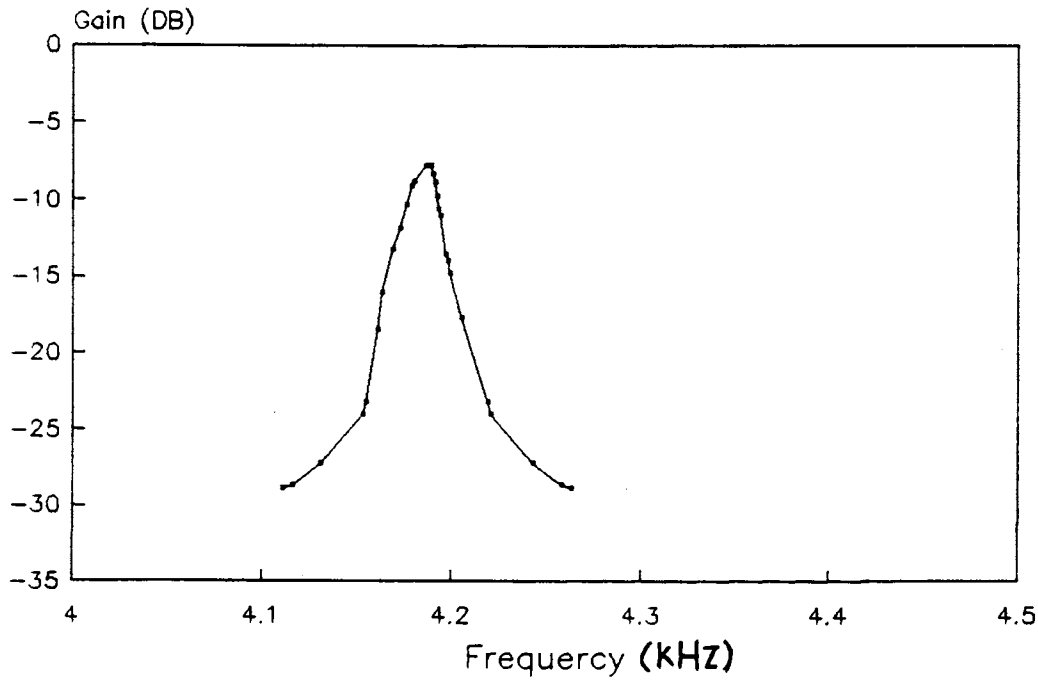


Fig. 6.6. Frequency response of the SC bandpass 4-path filter

The Q which is measured from the measurement is 320. The dynamic range, where the supply voltage and the centre frequency are 5 volt and 4.187 kHz, is 57 db.

6.3 TESTING THE SWITCHED-CAPACITOR BANDPASS 6-PATH FILTER ON THE CHIP

Consider a configuration of a bandpass switched-capacitor 6-path filter as illustrated in Fig. 6.7.

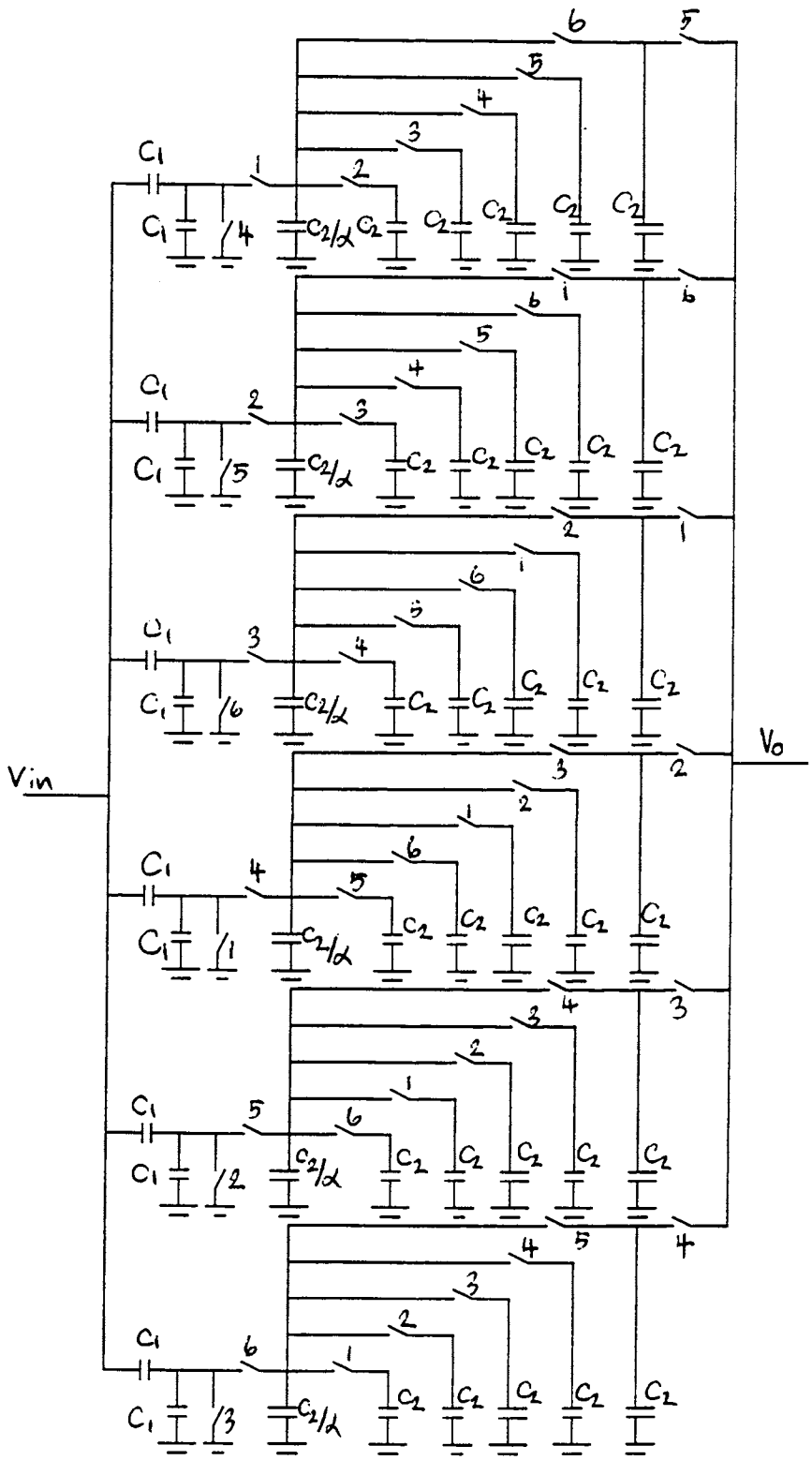


Fig. 6.7. bandpass switched-capacitor 6-path filter

A layout of SC bandpass 6-path filter which was designed by author is demonstrated in Fig. 6.8.

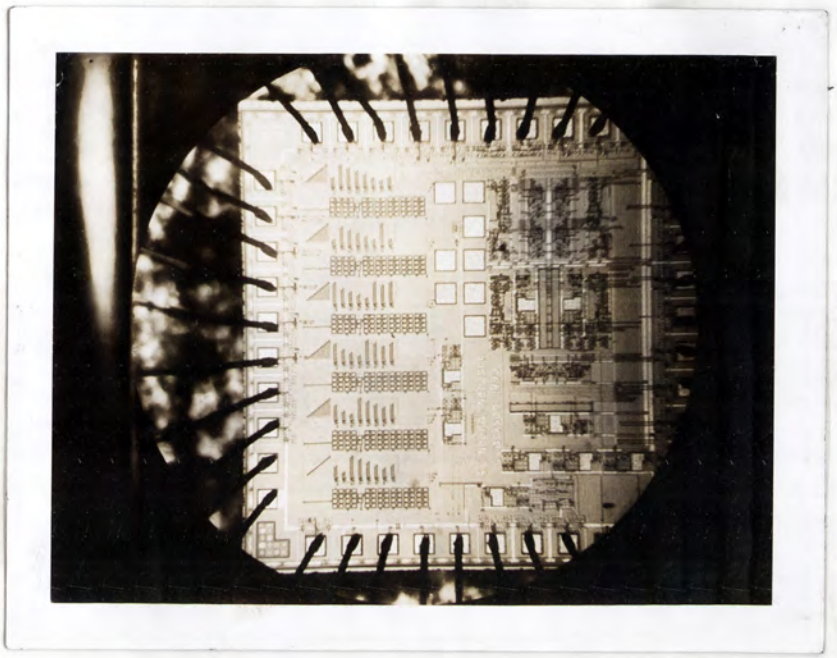


Fig. 6.8. The layout diagram of a switched capacitor bandpass 6-path filter

The element values are shown below:

$C_1 = C_2 = 1.224\ PF$

$\frac{C_2}{\alpha} = .306\ PF$

the aspect ratio of CMOS = 3 = $\frac{width\ of\ the\ gate}{length\ of\ the\ gate}$

$C_{ox} = \frac{3.5 \times 10^{-13}}{t_{ox}}\ cm$ $t_{ox} = thickness\ of\ the\ gate\ oxide$

the thickness of the gate oxide = .04 μm

The layout diagram is shown in Fig. 6.9.

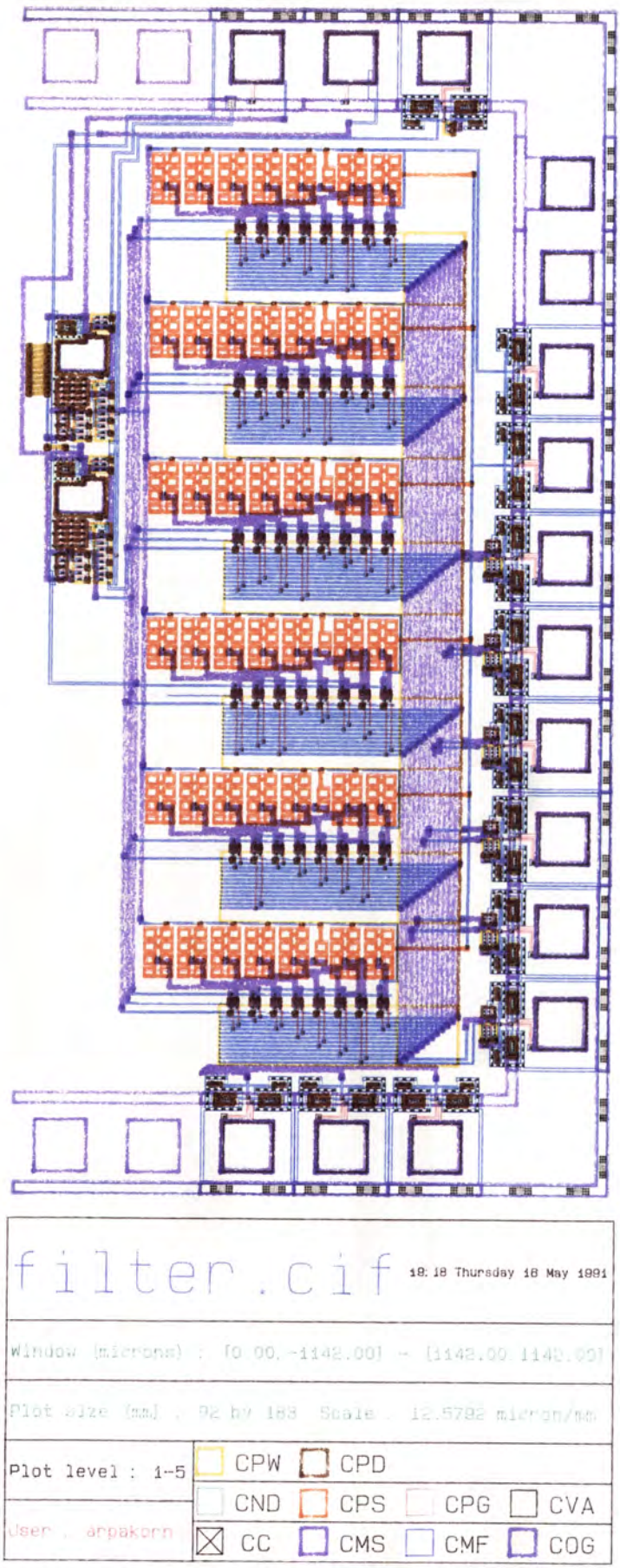


Fig. 6.9. The layout diagram of the SC bandpass 6-path filter

The circuit layout was designed for a double metal ISO-CMOS (P^- well) process design rule with 2μ double poly technology.

The buried channel potential was adjust by the ion implantation. The SOG planarization technology was utilized to smooth the top surface and define the 2nd metal.

In order to minimize the noise coupling from the noisy digital clock lines into the substrate, the *P^-well* is placed under the metal.

The configuration of the input protection circuitry is shown in Fig. 6.10.

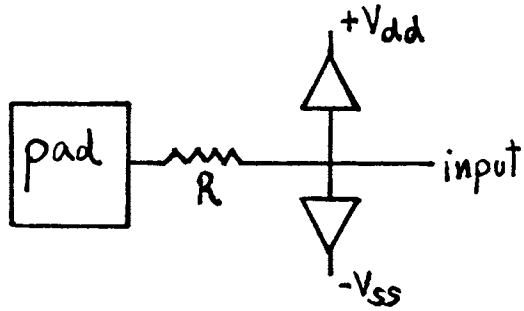


Fig. 6.10 The input protection circuit.

A resistor R, associated with the capacitance of the reverse-biased clamp diodes can prevent sudden spikes in the input signal from reaching the internal logic. The two diodes can protect over voltages.

The chip was fabricated by ORBIT Semicoductor Corperation at 1230 Bordeaux Drive Sunnyvale California 94089.

For the six non-overlapping clock phases, DM 74LS193 is used as a binary counter. DM 74LS154N and DM 74LS04N are used as a decoder and an inverter respectively.

When the input voltage is over .6 volt, the chip functions correctly (DC supply = 5 volt), though some mailfunctions were observed for low input voltage.

The maximum centre frequency where the author can obtain is 1.015 MHz. The bandwidth is about 63.9 kHz. Above this frequency, the output waveform is dominated severely by the noises.

The table below shows the comparison between the result from the calculation and the measurement.

6-Path Filter Parameters at centre frequency = 835 kHz

	theoritical prediction	measured
bandwidth	53.15 kHZ	52.8 kHz
Quality factor (Q)	15.8	15.71

The frequency response which is measured at the centre frequency about 835 kHz is shown below:

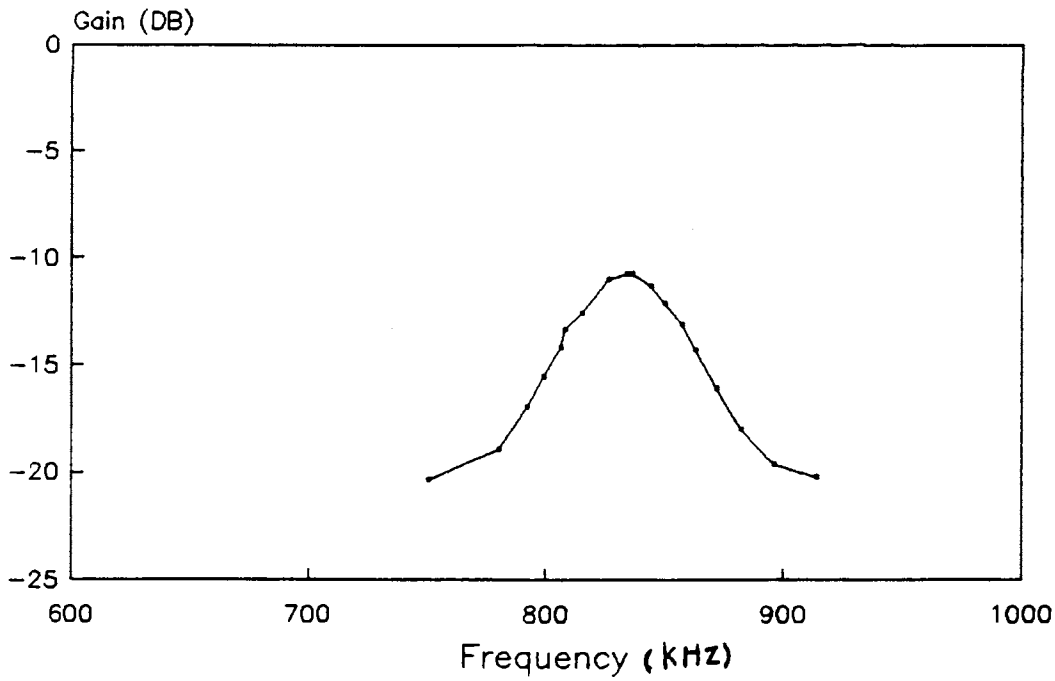


Fig. 6.11 The frequency response of switched-capacitor bandpass 6-path filter.

The dynamic range, where the supply voltage and the centre frequency are 5 volt and 835 kHz respectively, is 41 db.

6.4 INTERPOLATION FILTER

The interpolation filter circuit, that is tested, is illustrated below.

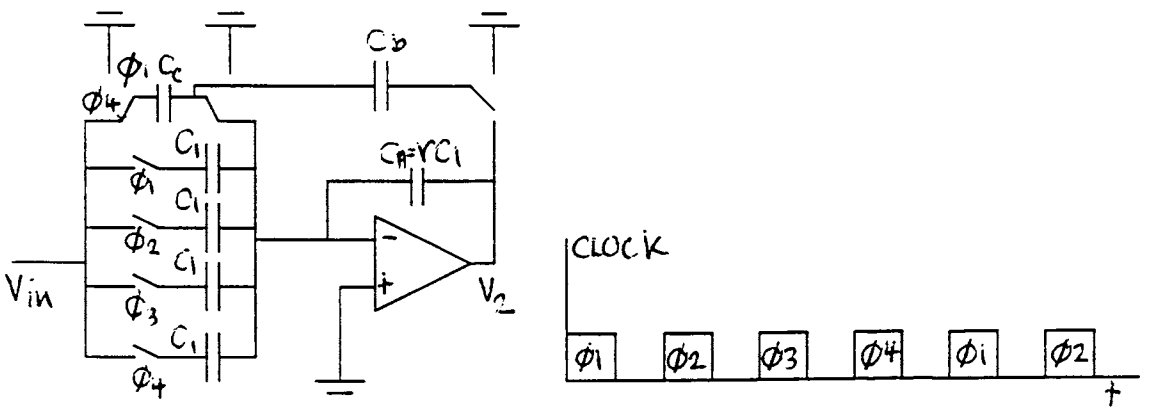


Fig. 6.12. An interpolation filter circuit

The frequency response of this circuit is plotted in Fig. 6.13.

(The clock frequency of each path that is used in this measurement is 5.38 kHz (f_{c2}).

IC number 14016 BCP is used as a switch. For the four non-overlapping clock phases, CD 4040 BCN is used as a binary counter. DM 74LS138 and 74LS04N are used as a decoder and an inverter respectively. ($C_1 = C_2 = C_3 = C_4 = C_b = C_C = 1.8nf$ $C_a = 7.35nf$)

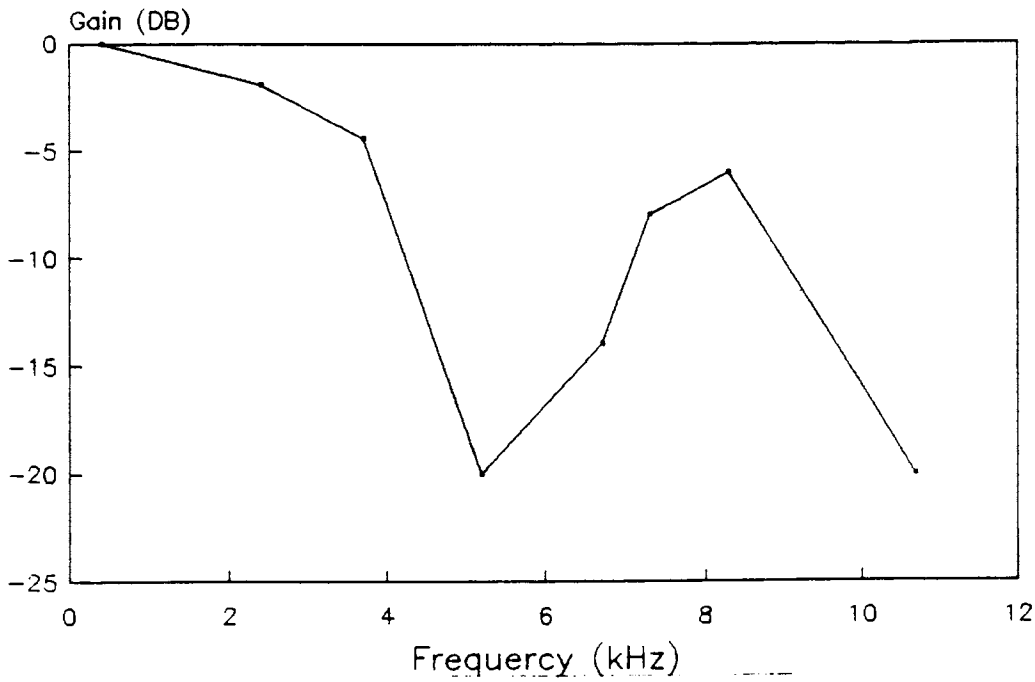


Fig. 6.13. The frequency response of the interpolator.

From the frequency response that is shown in Fig. 6.13. indicates that it has high

attenuation at f_{c2} and $2f_{c2}$, where f_{c2} is the clock frequency. The frequency response over $2f_{c2}$ can not be measured due to the Nyquist limit at $2f_{c2}$, where f_{c2} is the clock frequency.

This result insists the theory that this circuit has high attenuation at f_{c2} , $2f_{c2}$, $3f_{c2}$, $\cdots$

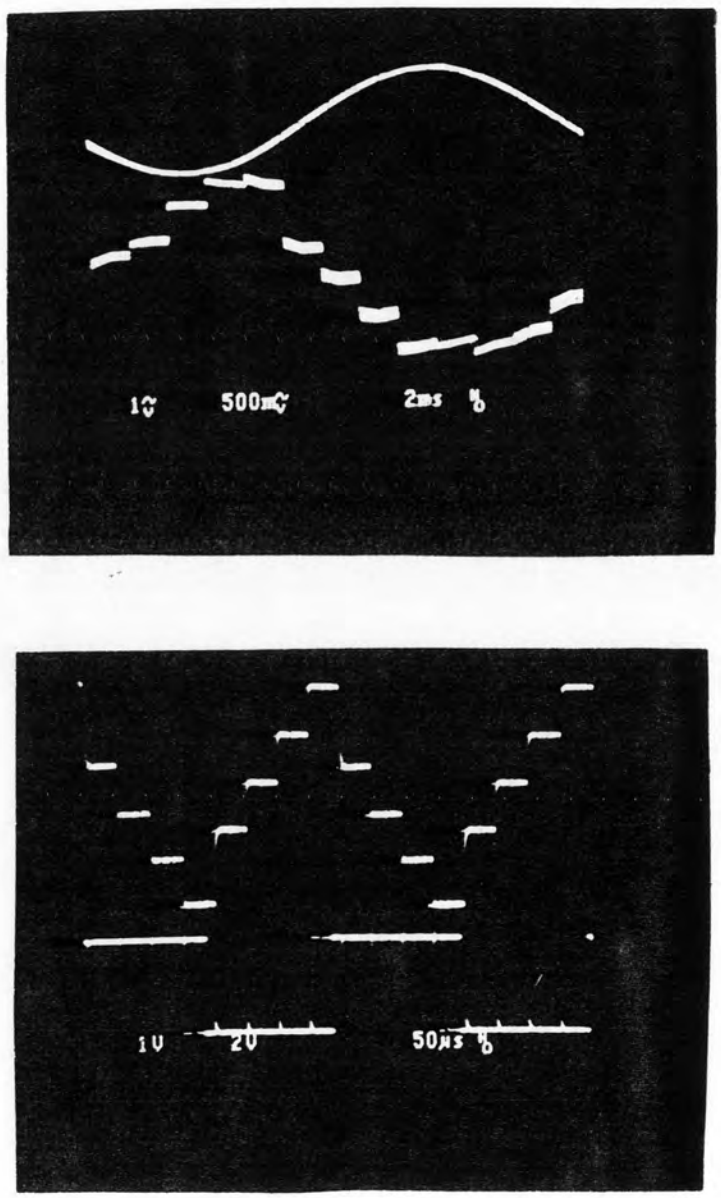


Fig. 6.14. (a) The output waveform after the input is supplied by a sinusoidal input signal.

(b) The output waveform after the input signal is supplied by a square wave signal.

6.5 THE SWITCHED-CAPACITOR BANDPASS 4-PATH FILTER AND INTERPOLATOR

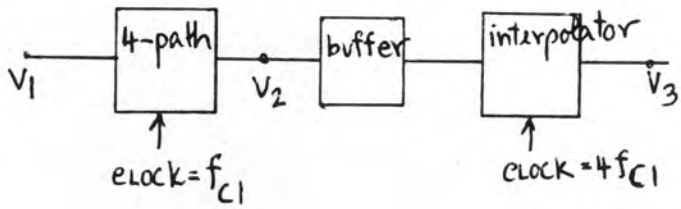


Fig. 6.15. The block diagram demonstrates the connection between the SC bandpass 4-path filter and the interpolator.

v_1 = input signal = clock frequency = 4200 Hz (f_{c1})

The clock frequency of the interpolator is $4\times f_{c1} = 4\times 4200 = 16800Hz$. The design parameters of the 4-path filter are shown below:

$$C_1 = .7nf \; C_2 = .547nf \; \frac{C_2}{\alpha} = .103nf$$

The frequency spectrum of v_2 is measured as illustrated in Fig 6.16.

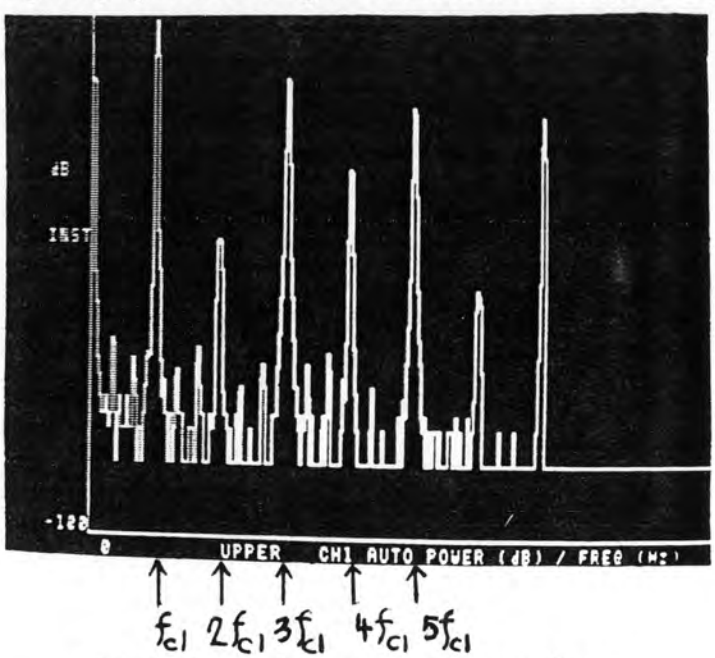


Fig. 6.16. The frequency spectrum of v_2

From Fig 6.15., f_{c1} $3f_{c1}$ $5f_{c1}$ are the frequency spectrum of the output signal. $2f_{c1}$, $4f_{c1}$, $6f_{c1}$ are the parasitic spectra, which are caused by the clock feedthrough noise from the CMOS switches.

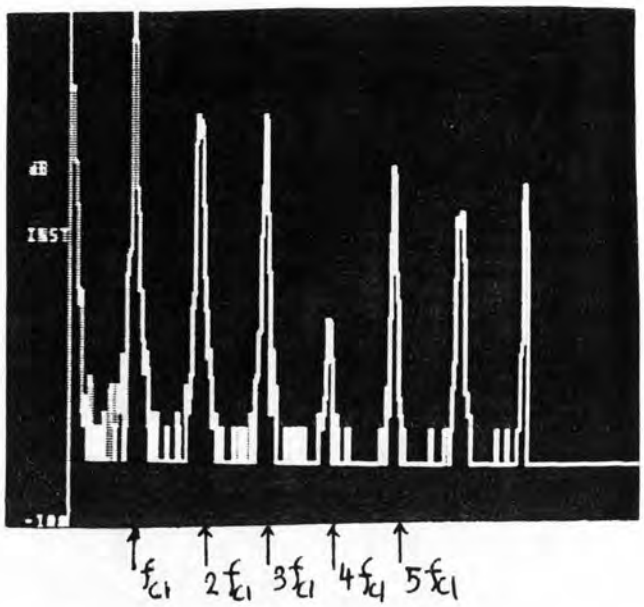


Fig. 6.17. The frequency spectrum of v_3

Comparison of v_2 and v_3 spectra, showing attenuation of odd harmonics.			
Frequency spectra of the output of the 4-path filter (v_2)	Amplitude (DB)	Frequency spectra of v_3	Amplitude (DB)
f_{c1} 4200 Hz	-6.8	f_{c1} 4200 Hz	-3.8
$3f_{c1}$ 12600 Hz	-16.8	$3f_{c1}$ 12600 Hz	-24
$5f_{c1}$ 21000 Hz	-22.2	$5f_{c1}$ 21000 Hz	-37.7

The comparison of the Table of Fig. 6.16. and Table of Fig. 6.17. shows the effective performance of the interpolator. The frequency spectrum at $3f_{c1}$ $5f_{c1}$ are attenuated in order to simplify the requirements of the smoothing filter.

6.6 THE SWITCHED-CAPACITOR BANDPASS 6-PATH FILTER AND INTERPOLATOR

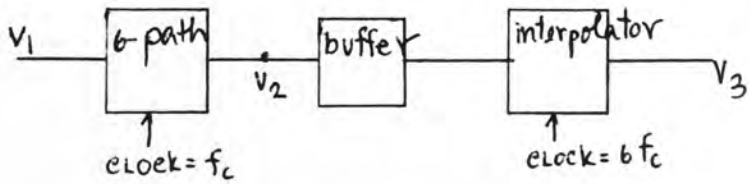


Fig. 6.18. The block diagram demonstrates the connection between the SC bandpass 6-path filter and the interpolator.

The configuration of the interpolation circuit and the values of the parameters are given in the experiment 3. LF 347 N is used as a buffer.

input frequency of v_1 = clock frequency of the SC 6-path filter f_c = 3600 Hz

clock frequency of the interpolator = $6 \times f_c = 6 \times 3600 = 21600\ Hz$

(Note that the design rule of the interpolator was discussed in section 5.4)

The waveforms of v_2 and v_3 are given in Fig. 6.19.

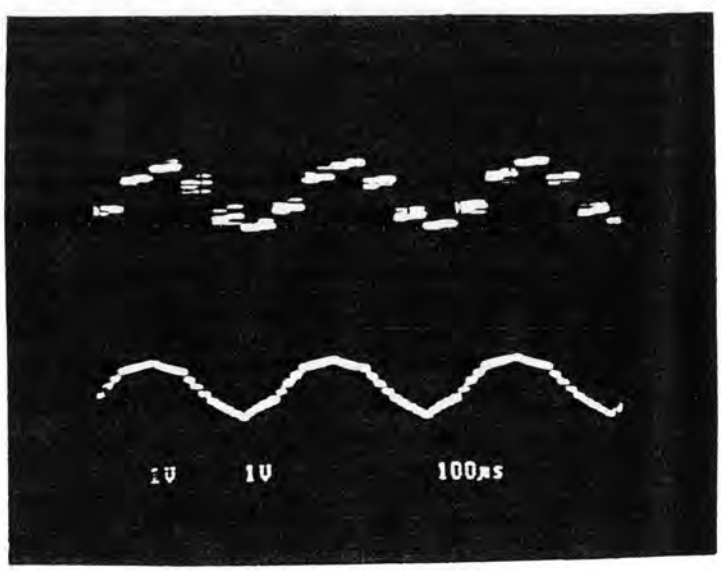


Fig. 6.19. The top waveform represents the output waveform of the SC bandpass 6-path filter

The below waveform represents the sampled and held output waveform of the interpolator

The frequency spectra of v_2 is measured as illustrated in Fig. 6.20.

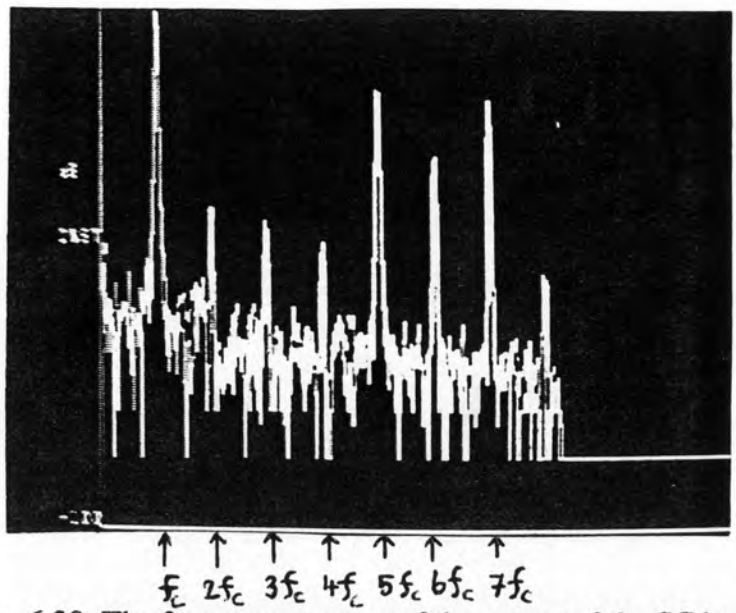


Fig. 6.20. The frequency spectra of the output of the SC bandpass 6-path filter.

From Fig. 6.20., f_c , $5f_c$, $7f_c$ are the frequency spectra of the output of the SC bandpass 6-path filter. $2f_c$, $3f_c$, $4f_c$, $6f_c$ are the parasitic spectra of the SC bandpass 6-path filter. These parasitic spectra are caused by the clock feedthrough of the CMOS switches.

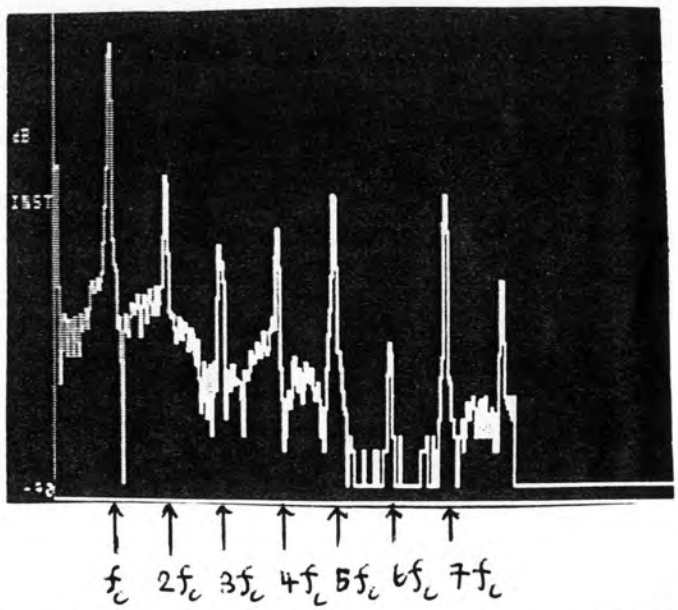


Fig. 6.21. The frequency spectra of the output of the interpolator (v_3)

Comparison of v_2 and v_3 spectra, showing attenuation of odd harmonics.			
Frequency spectra of v_2	Amplitude (DB)	Frequency spectra of v_3	Amplitude (DB)
f_c 3600 Hz	-6.1	f_c 3600 Hz	-7.9
$5f_c$ 18000 Hz	-29.0	$5f_c$ 18000 Hz	-52
$7f_c$ 25200 Hz	-30.4	$7f_c$ 25200 Hz	-67

The comparison of Table of Fig. 6.20. and Table of Fig. 6.21. shows the effective performance of the interpolator. The frequency spectra at $5f_c$ and $7f_c$ are attenuated in order to simplify the requirements of the smoothing filter.

In the following experiment, all antialiasing filter, cosine decimator, 4-path filter and interpolator will be combined in order to see how efficiently cosine decimator and interpolator filter can simplify the requirements of the antialiasing and smoothing filters respectively.

Some symbols which are shown below will be used from section 6.7 to 6.9. (The designs of the clock frequency of the interpolator and decimator were already discussed in Chapter 5.)

The parameters of the 4-path filter are $C_1 = .7\ nf$ $C_2 = .547\ nf$ $\frac{C_2}{\alpha} = .103\ nf$ (see Fig 6.4)

f_{c1} = the clock frequency of the SC 4-path filter.

$4f_{c1}$ = the overall sampling frequency of the 4-path filter.

$f_{c2} = 4f_{c1}$ = the clock frequency of the interpolator.

$4f_{c2} = 16f_{c1}$ = the sampling frequency of the interpolator.

6.7 ANTIALIASING AND 4-PATH FILTER

A first order RC passive antialiasing filter (AAF) is designed to have a cut off frequency at which corresponds to $3f_{c1}$, where f_{c1} = the centre frequency of the 4-path filter. The purpose to design the cut off frequency at $3f_{c1}$ in stead of $2f_{c1}$, which is the Nyquist limit of 4-path filter, and use only the first order passive AAF is that we want to see whether the decimator really help to relax the specifications of AAF or not.

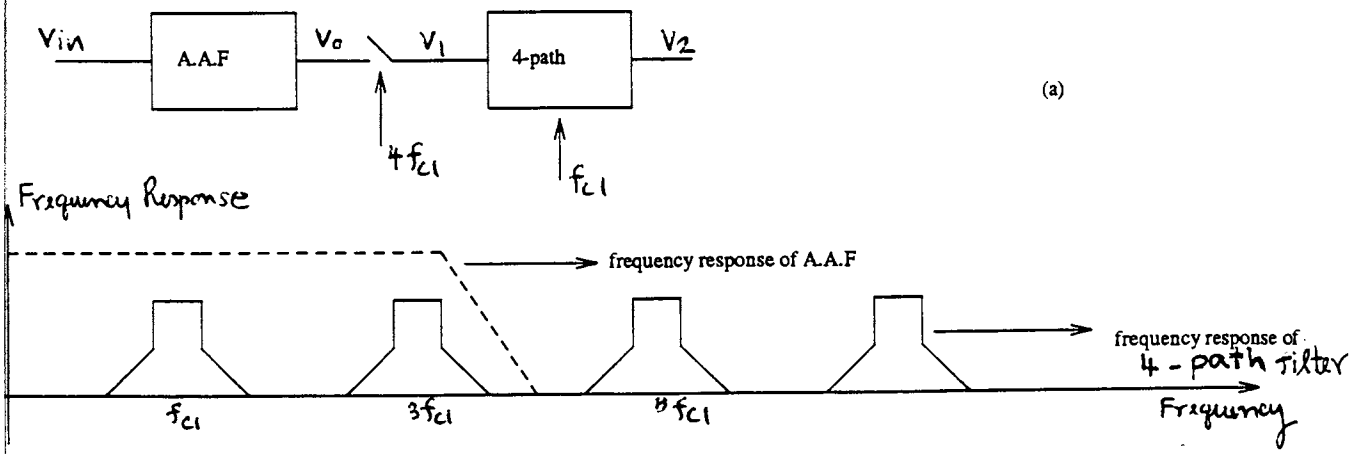


Fig. 6.22. (a) The block diagram demonstrates the connection.

(b) The dashed line and solid line represent the frequency response of AAF and 4-path filter respectively.

Testing result

Clock frequency of 4-path filter = 9.6 kHz (f_{c1})

AAF is a first order RC lowpas filter and it has a cut off frequency at $3f_{c1}$ = 28.8 kHz

Aliasing measurements

input frequency (kHz)	output (v_2) (volt)
$3f_{c1}$ 28.9	.5
$5f_{c1}$ 48.2	.4
$7f_{c1}$ 67.8	.3
$9f_{c1}$ 87.1	.4

The frequency response of $\frac{v_2}{v_{in}}$ is shown below:

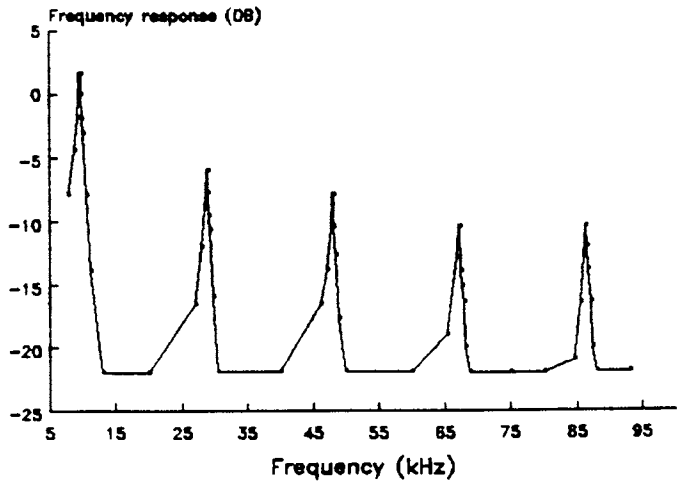


Fig. 6.23 Frequency response of $\frac{v_2}{v_{in}}$

6.8 AAF, COSINE DECIMATOR AND 4-PATH FILTER

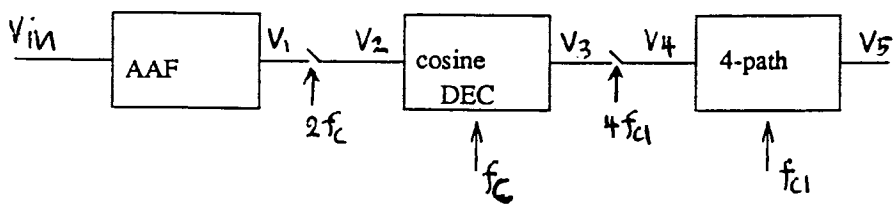


Fig. 6.24. The block diagram demonstrates the connection.

The designs of the following parameters were already discussed in Chapter 5.

cut off frequency of AAF = $3f_{c1}$ = 28.8 kHz (the same as section 6.7)

cut off frequency of the cosine decimator = f_{c1} = 9.6 kHz

stopband frequency of AAF (f_s) = $2f_c - f_1$ = 345.2 kHz

stopband frequency of the cosine decimator (f_1) = $3f_{c1}$ = 28.8 kHz

v_{in} = 2×5 v_{p-p}

clock frequency of the 4-path filter (f_{c1}) = 9.6 kHz

clock frequency of the cosine decimator (f_c) = 187 kHz

input frequency	output (v_5)
9.6 kHz	2×1.4 v_{p-p}

Only aliasing occurs at the input frequency equals to 28.9 kHz and the output comes out only 2×.3 v_{p-p}. (Note that 28.9 kHz = 3 f_{c1} = 3 × 9.6 kHz)

The frequency response of $\frac{v_5}{v_{in}}$ is shown below:

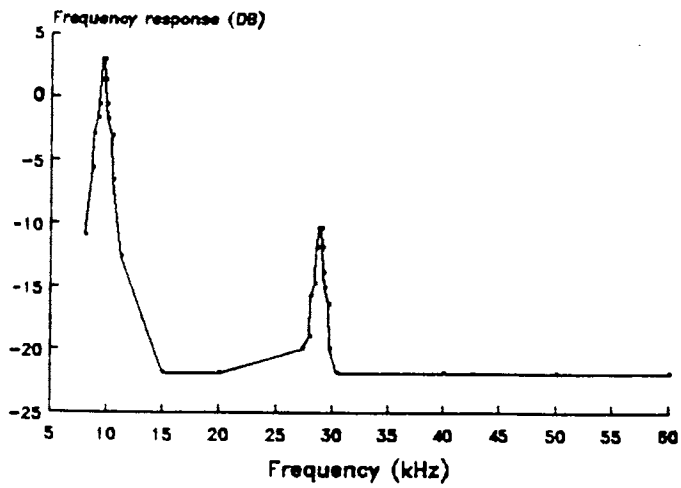


Fig 6.25 Frequency response of $\frac{v_5}{v_{in}}$.

Compare with the result from section 6.7, we apparently see that the input frequencies which are higher than f_{c1}, where f_{c1} is the clock frequency and the centre frequency of 4-path filter, only a small amplitude of aliasing of the output occurs when the input frequency is $3f_{c1}$ due to too high cut off frequency of cosine decimator. However, we can summarize that this cosine decimator can efficiently simplify the requirements of AAF.

6.9 4-PATH FILTER, INTERPOLATOR AND SMOOTHING FILTER.

The centre frequency of 4-path filter is still at 9.6 kHz.(f_{c1}) The clock frequency of the interpolator filter is at 4×9.6 kHz = 38.4 kHz.(f_{c2}) From the experiment, the waveform at the output of the interpolator is shown below:

The designs of the following parameters were already discussed in Chapter 5

f_{c1} = clock frequency of 4-path filter = 9.6 kHz

$f_{c2} = 4 \times f_{c1}$ = 38.4 kHz = clock frequency of the interpolator.

sampling frequency of the interpolator = 4×38.4 *kHz* = 153.6 kHz

sampling frequency of the 4-path filter = 4×9.6 *kHz* = 38.4 kHz

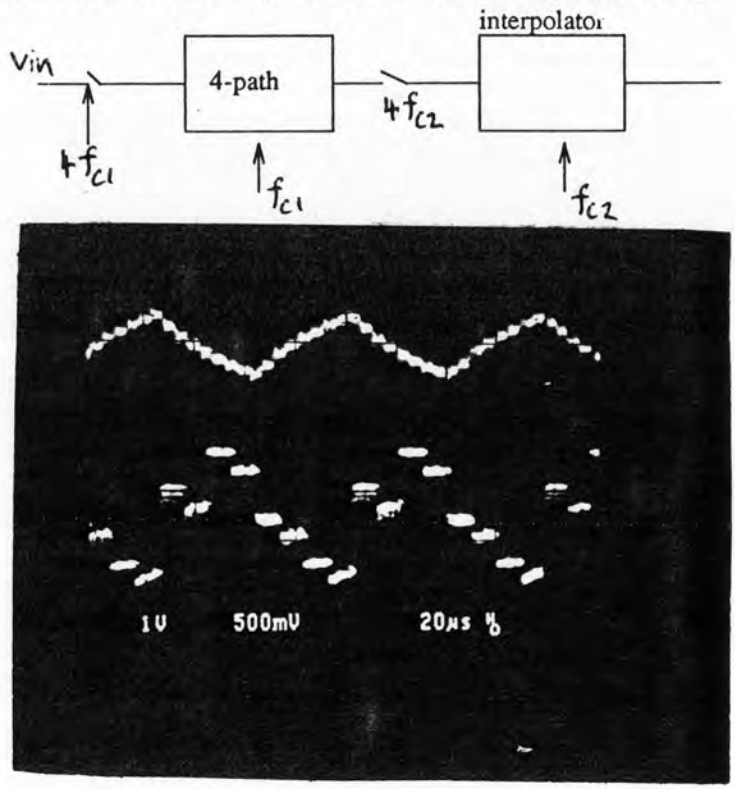


Fig. 6.26. (a) The block diagram demonstrates the connection.

(b) The sampled and held signal demonstrates the input frequency of the interpolator. The continuous-time signal represents the output signal from the smoothing-filter.

To recover the sampled and held signal from the output of the interpolator filter to a continuous-time signal, a smoothing filter which has the stopband lower than $15f_{c1}$ (15×9.6kHz = 144kHz) is required.

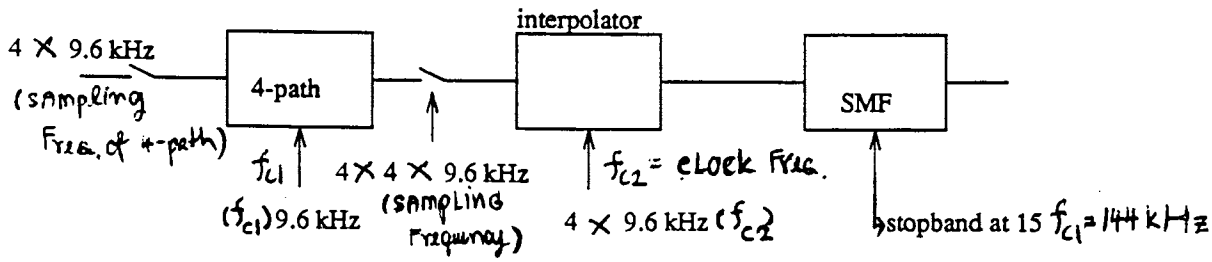


Fig. 6.27 Block diagram demonstrates the effective performance of interpolator to relax the specifications of smoothing filter

Above block diagram apparently demonstrates that the stopband of the smoothing filter can be $15f_{c1}$ in stead of $3f_{c1}$, so the interpolator can really help to simplify the requirements of the smoothing filter.

From the experiment, the output waveform from the output of the smoothing filter is not a perfect sinewave , due to the fact that it is distorted by the $\frac{\sin x}{x}$ response.

CHAPTER 7

CONCLUSION

Switched capacitor N-path filters are attractive for realising bandpass filters at high Q because of two properties.

(a) The overall transfer function of the N-path filter has the same order, same filter coefficients and accordingly, identical sensitivities to element-value variations as an individual lowpass filter of each path. The sensitivities of the lowpass cell are proportional to the Q_{lp}, which is lower than the overall Q_{bp} of the bandpass filter by a factor $\frac{Q_{bp}}{Q_{lp}} \sim \frac{2\omega_o}{B}$. ($Q_{bp}$ and Q_{lp} are the pole-Q of the dominant poles of the lowpass and bandpass filters respectively.) Hence the overall sensitivities of the N-path filter are lower.

(b) The centre frequency can be controlled accurately by using a quartz stabilized clock oscillator. Hence a very stable and exact centre frequency can be obtained.

The use of conventional switched capacitor filter as a narrow band bandpass filter, results in poles with a much higher Q. This results in high sensitivity to parameter variations.

The results of testing demonstrates that a passive SC bandpass N-path filter, which is combined with band stop filters, can suppress the undesirable passbands occuring at even multiples of the clock frequencies efficiently. From the measurement of the SC bandpass 6-path filter on the chip in Chapter 6, the maximum centre frequency and the Q are 1.005 megahertz and 15 respectively. The dynamic range, where the supply voltage and the centre frequency are 5 volt and 835 kHz, is 41 db. Path mismatch, clock feedthrough, and mirror frequencies produce spurious responses in the passband which reduce the dynamic range to this relatively low level.

For the SC bandpass 4-path filter which was built on the bread board, the Q, which is measured from the experiment, is about 320. The dynamic range, where the supply voltage and the centre frequency are 5 volt and 4.187 kHz respectively, is 57 db. The value of Q, which is calculated from the theory in Chapter 4, is about 323, which is close to the testing result. At the frequency spectra of the output signal, there are some parasitic spectra, which

occur at nf_c (n = 1,2,3,..). These parasitic spectra are caused by the clock feedthrough of the CMOS switches.

If all paths are symmetrical, unwanted parasitic spectra will cancel out at the output.

In practice, because of path mismatch, the unwanted frequencies from each path will not completely cancel and cause interference of the output signal, more so than does a conventional single path switched capacitor.

A design, which is called a pseudo-N-path filter seems to be superior, however it results in a very complex op-amp. The requirements of the op-amp that is used for the pseudo-N-path filter are given as follows: (see Fig. 4.16.)

1. It requires N(N+1) clock phases, where N is the number of path of the pseudo-N-path filter, to perform the full cycle of operation. Thus the op-amp must be fast even for a relatively low centre frequency.

2. Each charge packet must complete transfers in each period, incomplete charge transfer effects due to imperfect virtual ground will appear even for fairly high op-amp gains.

For a digital system and a sampled data system, an antialiasing filter and a smoothing filter are needed in order to confine the input frequency band and recover the discrete output signal to a continuous-time output signal respectively.

In practice, due to the low sampling frequency, the requirements of AAF and SMF become very complex and this results in large chip area. The additional sampled data systems which are known as decimation and interpolation filters are needed to simplify the requirements of AAF and SMF. In Chapter 5, a cosine decimator was designed to achieve further relaxation of the AAF specifications.

From the testing in Chapter 6, AAF was designed to have a cut off frequency at $3f_c$, where f_c is the clock frequency of the 4-path filter. The Nyquist limit of the 4-path filter is at $2f_c$. The additional cosine decimator filter effectively simplifies the requirements of the AAF and this results in no aliasing effect at the output. The designs of the clock frequency and bandwidth of the cosine decimator to operate with the 4-path filter were described in Chapter 5.

For an interpolation filter that is required to simplify the requirements of the SMF, the testing results in Chapter 6 have demonstrated its effective performance. The designs of the clock frequency of the interpolator and the cut off frequency of the SMF were already given in section 5.6.

In the future, both cosine decimation and interpolation filters will have important roles for sampled data systems because they can effectively relax the specifications of AAF and SMF respectively, therefore the chip area can be reduced.

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