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Author:
Mumford, Peter; Balaei, Asghar; Dempster, Andrew

Publication details:
Proceedings of IGNSS2007

Event details:
IGNSS2007
Sydney, Australia

Publication Date:
2007

DOI:
https://doi.org/10.26190/unsworks/690

GNSS Interference Detection Device

Peter J Mumford
CRC for Spatial Information, Surveying & SIS, University of New South Wales
+612 9385 4189 p.mumford@unsw.edu.au
Asghar Tabatabaei Balaei
CRC for Spatial Information, Surveying & SIS, University of New South Wales
+612 93854206 asghart@student.unsw.edu.au
Andrew G Dempster
CRC for Spatial Information, Surveying & SIS, University of New South Wales
+612 93856890 a.dempster@unsw.edu.au

ABSTRACT

The radio frequency signals transmitted by Global Navigation Satellite Systems (GNSS) have very low power and are susceptible to radio frequency interference. Most GNSS receivers do not measure and quantify any interference they may be suffering; they just do what they can with the signals they receive. Interference can lead to poor receiver positioning performance and, if severe, such as in a jamming environment, complete positioning failure. Interference monitoring could be beneficial in areas such as airports where GNSS positioning will soon be more critical and interference could be present.

This paper outlines the work to date on developing an interference detection device based around the Namuru GNSS receiver platform developed at the University of New South Wales (UNSW). The detection device is a hardware and embedded software realization of detection schemes and algorithms developed at UNSW. The detection technique is briefly explained followed by a discussion of the hardware design, software implementation, testing and results, some conclusions and finally, a discussion of possible future activities.

KEYWORDS: radio frequency interference, GNSS, RFI detection

1. INTRODUCTION

Society is witnessing an ever-increasing reliance on the Global Positioning Systems (GPS). This system relies on extremely low power radio frequency (RF) signals transmitted by the satellites, Kaplan (1996). This signal can be interfered with by unwanted RF signal generated intentionally or unintentionally by terrestrial or celestial RF transmitters. Detection of interference is the first step towards dealing with it and subsequently improving system integrity. Detection aids in mitigating or localizing the interference, see Tabatabaei *et al*. (2007) and Brown *et al*. (1999). Navsys Corporation in 1999 introduced its High Gain Antenna Receiver (HAGR) technology to detect and locate the direction of arrival of an RFI signal, see Brown *et al*. (1999). In 2000, the Stanford GPS laboratory introduced an interference detection board which, using antenna array processing, was capable of detecting and localizing the interference using time difference of arrival (TDOA) of the signal, see Gromov (2000). Statistical inference has been widely used to detect a signal in noise, see Shnidman (1995, 2005). In Marti *et al*. (2004) and Tabatabaei *et al*. (2006) this technique is

used to detect continuous wave (CW) interference which has a very strong effect on the acquisition and tracking of the receiver, see Kaplan (1996). In Tabatabaei *et al*. (2006) a method is introduced to improve the sensitivity of detection which allows the detection of interference with power levels below the background noise level. This sensitivity can help in localizing the source of interference using received signal power in the following stages. The class of CW interferences includes narrowband signals that can be reasonably represented as pure sinusoids appearing in the GNSS bands. These kinds of interfering signals can be generated by UHF and VHF TV, VHF Omni-directional Radio-range (VOR) and Instrument Landing System (ILS) harmonics, by spurious signals caused by power amplifiers working in non-linearity region or by oscillators present in many electronic devices, see Landry *et al*. (1997).

The paper is organized as follows: section 2 describes the detection technique and how to improve the sensitivity of detection both in terms of frequency and power. In section 3, the hardware implementation is provided, in section 4 software is briefly discussed followed by some results of testing in section 5. Finally, in section 6, a summary, conclusions and future work complete the paper.

2. THE DETECTION TECHNIQUE

In this section the algorithms to improve the sensitivity and resolution of interference detection in terms of power and frequency are presented. The high sensitivity to low level power interference can be useful in locating the interference source using the received signal power. In addition, resolution in frequency is needed for prediction or estimation of the adverse effects of the interference on the received GNSS signal see Tabatabaei *et al*. (2007). The theoretical background for Hypothesis testing can be found in Kay (1998). The idea is to choose a window of IF data samples which is known to be free from interference. Then, to check the existence of interference at any time, another window of data is taken. Then the statistical parameters of the two windows are compared. The null hypothesis is that interference does not exist. The alternative hypothesis is that interference does exist. The truth of each hypothesis is tested by conducting a t-test. It is shown in Figure 1 how to break each window down into blocks of data. The Fast Fourier Transform (FFT) of each block of data gives us a value for the frequency component of the signal at that specific block in each frequency bin across the whole bandwidth, see Tabatabaei *et al*. (2006). The number of blocks is chosen to be high enough for the Central Limit Theorem (CLT) to be applicable as the distribution of the power of signal in each bin is not necessarily normal.

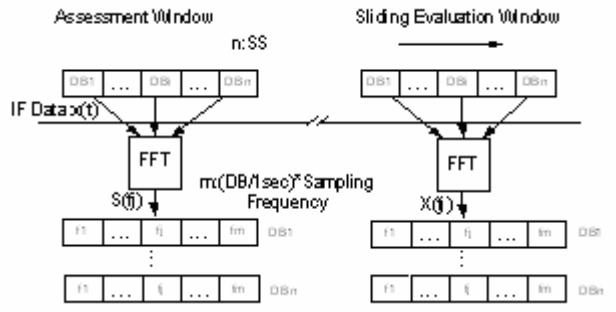

Figure 1. Process of generating the samples for each frequency bin of the two populations

In Tabatabaei *et al*. (2006) it is shown how to break the data window into data blocks in order to achieve maximum sensitivity in terms of the power of interference.

In the technique discussed above, the frequency of interference can best be determined by the resolution of the frequency bins. In Tabatabaei *et al*. (2006) the authors have introduced techniques to predict the effect of interference on the quality of the received signal in the presence of CW interference. In that work, it was shown that the frequency resolution needed to predict the C/No as an indication of signal quality is comparable to the tracking loop bandwidth which is usually a few hertz. To improve the resolution, a two stage detection method is used. In the first stage, the interference is found using the above explained algorithm with a rough estimation of the frequency. In the second stage, interference is down-converted in frequency to the base band and after down-sampling the data, the frequency is found with a few hertz resolution. In section 3 we will introduce a prototype hardware implementation of these techniques.

3. HARDWARE

The hardware is implemented on the Namuru field programmable gate array (FPGA) GNSS receiver board. The Namuru board includes an L1 band RF front-end, Altera 'Cyclone' FPGA chip, memory, various I/O options including serial ports and Ethernet socket, and other support devices. Details about the board can be found in Mumford *et al*. (2006).

The RF front-end amplifies, filters, down-converts and band-pass samples the incoming signal. It passes the sampled intermediate frequency (IF) to the FPGA for digital processing as two-bit, sign and magnitude values. This process is shown in the frequency domain in Figure 2.

At the heart of the design is an Altera FFT block, providing a 2048 bin, complex FFT with 8 bits of input precision. Input to this FFT block can come from two sources; direct from the incoming raw GPS IF data stream, or from a local oscillator mixed and accumulated version of the raw data. The second source provides the 'zoom' functionality for determining the interference frequency to greater resolution. Figure 3 shows a simplified block diagram of the system.

The complex output of the FFT is scaled and processed into a magnitude value, and then transferred to on-chip memory using an Altera direct memory access (DMA) block function. The data is then available for the Nios processor to access. This is where the software algorithms take over, an overview of the software is provided in section 4.

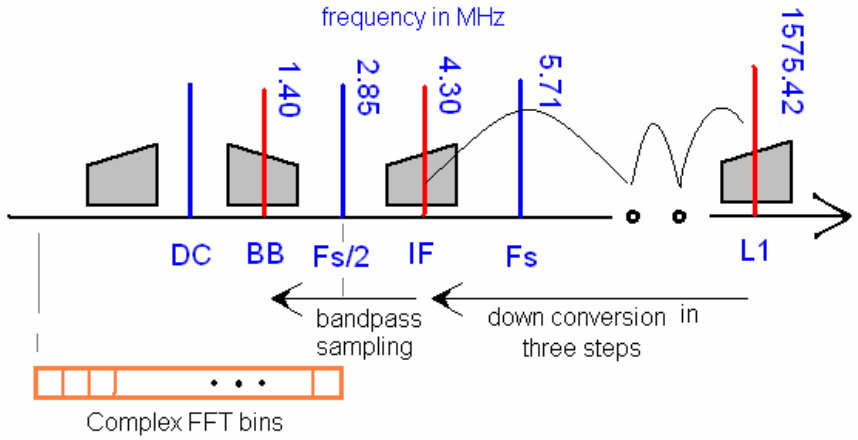

Figure 2. RF down-conversion and band-pass sampling diagram

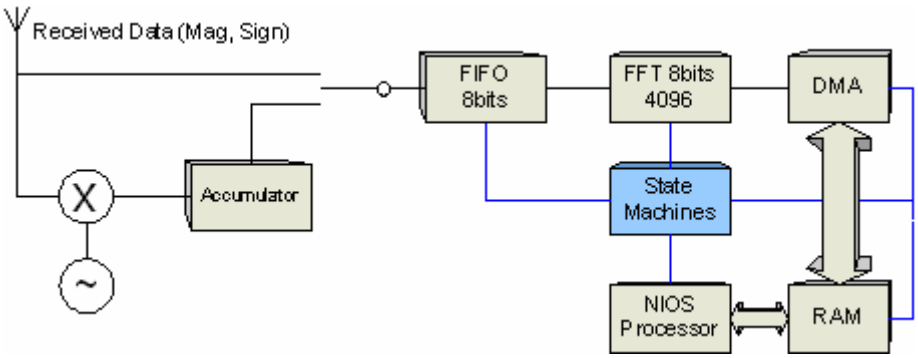

Figure 3. Simplified hardware block diagram

Coordinating all this activity is a number of finite state machines, these in turn are controlled by the state of registers that can be set by software and appear as a memory-mapped peripheral to the Nios processor. The DMA is responsible for making the data available to be processed in software, and provides a set of memory-mapped registers for status and control, see Altera (2006). Figure 4 provides a detailed block diagram of the system.

The FFT block receives data in a 2048 sample (real only) sequence, then takes some cycles to process, and finally outputs 2048 bin (real and imaginary) values in sequence, along with a scale factor. The Altera Avalon Streaming Interface protocol defines how to control data flow in and out of the FFT block. More information on this protocol can be found at Altera (2006).

The FFT scale factor presents a problem, as while it varies only a little between FFT processes in the normal mode, it varies a lot in the change to zoom mode and this needs to be taken into account. A trade-off between dealing with scaling in hardware, and adjusting scaling from software has been found to keep the bit width of the resulting data to a suitable size. In the present design, the values coming out of the final math block (the square-root) and going into the DMA is 8 bits. This is a very convenient size, and makes for an easy and efficient implementation of the DMA data transfer.

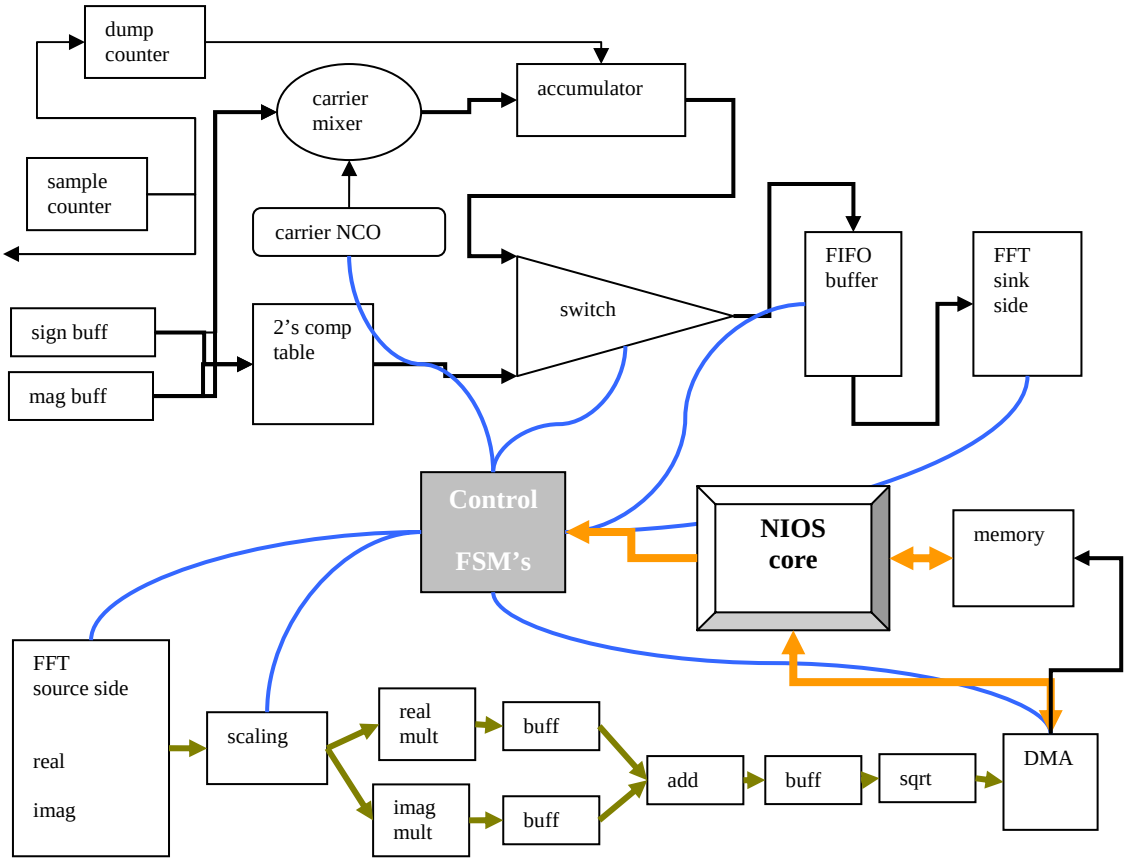

Figure 4. Detailed hardware block diagram

An example of output from a 512 bin Altera FFT block is provided in Figure 5. Here a 1575.42MHz sine-wave signal at -80dBm is injected into the RF front-end, sampled and fed into the FFT block as a 2's compliment real value. The output is a positive and negative frequency sweep from DC to half the sample rate. In the prototype hardware implementation, a 2048 point FFT block is used, but only the first half of the output data is used, providing magnitude values over 1024 frequency bins. The second half of the output is close to a mirror image and for these purposes, redundant.

All RF down conversion steps, sampling and FPGA digital processes are driven by one TCXO crystal oscillator running at 10MHz. Ultimately, all frequency determinations are based on this reference clock, and the accuracy, stability and possible calibration of this clock determine the absolute accuracy of the measurements made by the system. Having said this, it must be noted that the oscillator used on the Namuru board is a quality Rakon TX0215BR TCXO with an overall accuracy estimated at 2ppm or better.

So why do so much processing in hardware? The first reason is that the Altera function blocks are tested and easily available, and can fit within the available FPGA chip space. The second reason is to allow the Nios processor to operate on the higher levels of the system, without being burdened with time-consuming DSP functions such as the FFT. This also makes software development much quicker and easier. Finally, the Nios processor potentially has enough spare capacity for communication to users, through serial ports, some visual unit such

as an LCD screen, or via the internet through a TCP/IP software stack and the on-board Ethernet connector.

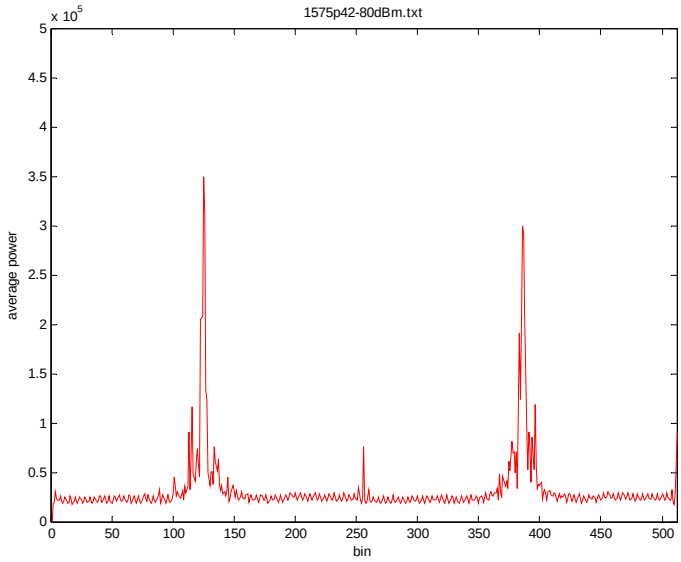

Figure 5. Output of 512 bin FFT engine with L1 center frequency input

4. SOFTWARE

Software for the prototype system was written in 'C' using the Altera NiosII IDE. The functions the software performs are; initialise hardware, control DMA transfers, collect and analyse data, control zoom processing and report on results. A brief overview of these activities is provided in this section.

The hardware is attached to the Nios core as a memory-mapped peripheral, status is observed by reading registers and hardware controlled by writing to registers. The DMA, control state machines and serial ports all require initialisation. After this, the software goes into a looping sequence of data collection, statistical testing and deciding if a switch to zoom processing is required. Zoom processing follows a similar sequence, and can fall back into normal processing if statistical tests fail over a number of trials. Various data from each processing sequence can optionally be logged to an external computer via an RS232 serial link for further off-line processing or viewing.

Because most of the hard work is performed in hardware, the software is relatively straight-forward and small. The most critical part was found to be seting up and controlling DMA functions. The software is still in the development stage and requires plenty of refinment and expansion before evolving towards release status. Items on the list for inclusion are; on-board display and user interface, watchdog timer and reset system to reboot if crashes occur, ethernet TCP/IP stack for on-line status reporting and frequency calibration capability.

5. EXPERIMENTS

The system was tested to determine performance in three areas. The first was the detection of a continuous sine-wave in the L1 band to confirm correct overall system functioning and an initial indication of the performance of the statistical method used. The metrics of this test include an estimate of the sine-wave frequency and the t-value used in the hypothesis testing.

The second test was to confirm the resolution of the zoom frequency determination system. The third test was to assess the operation of the device in the field, in an area suspected of having occasional interference.

The first two tests had the following setup; a Hewlett Packard 8648B RF signal generator was used to provide a sine-wave at a known frequency and level. The specifications for this generator for the L1 band are; frequency accuracy +/- 4.7kHz, frequency resolution to 0.001Hz, power level accuracy +/- 1dB, within one year of calibration, see Hewlett Packard (1996). The internal oscillator is rated as +/- 2ppm/year. Unfortunately, the calibration status of this unit is unknown, and it cannot be assumed to be within specification. This signal is injected into the antenna connection of the Namuru's RF front-end. The signal is down-converted and sampled into the FPGA chip where processing is performed. Software running on a Nios core on the FPGA communicates via a JTAG serial interface to a console window providing status information, and also data can be logged to file via an RS232 serial link for further analysis.

With the HP signal generator set to RF OFF (no signal) maximum t-values where observed. Over a sample of 50 trials, the average t-value was 0.39 with a standard deviation of 0.07 and maximum off 0.46. These values represent the lowest range of t-values that the system will produce.

Some results from testing for the detection of a sine-wave in the L1 band and frequency determination using the zoom technique at zoom 10 is provided in Tables 1 and 2. The threshold for detection was set at 95% confidence level, providing a t-value threshold of 1.64. In Table 1, the RF input level from the HP signal generator was set at -100dBm, and Table 2 the input was set at -110 dBm. It can be seen that -110dBm is close to the limit of detection at 95% confidence for this system. It can also be seen from the tables that there is a near constant frequency offset between the frequency set on the HP signal generator and the reported frequency determination from the zoom process. This offset is most likely due to the differences in reference clock frequencies in the two devices, but also may include other factors.

Input frequency -100dBm (MHz)	Detection t-value	Zoom 10 frequency determination (MHz)	Delta (Hz)
1574.40	13.5	1574.403689	3689
1574.91	8.9	1574.913734	3734
1575.03	9.8	1575.033991	3991
1575.42	7.2	1575.423779	3779
1575.81	11.0	1575.813845	3845
1575.23	13.0	1576.233767	3767
1576.54	9.1	1576.543756	3756

Table 1. Detection of -100dBm sine-wave @ zoom 10

Table 1 reveals a good correlation between the frequency set on the HP RF generator and the determined frequency, with an average delta of 3794Hz with standard deviation 98Hz. The t-values are all well above the 95% confidence threshold.

Table 2 also reveals good correlation, with average delta of 3754Hz and standard deviation 50Hz. Most of the t-values clear the 95% confidence threshold convincingly, except for the L1 center frequency that clears the threshold by just 0.26. It is clear from this that detection would begin to fail at signal power levels lower than this at the 95% confidence level.

Sensitivity could be improved by using a larger FFT block with more bins, FPGA space permitting.

Input frequency -110dBm (MHz)	Detection t-value	Zoom 10 frequency determination (MHz)	Delta (Hz)
1574.40	3.7	1574.403689	3689
1574.91	2.4	1574.913734	3734
1575.03	2.5	1575.033712	3712
1575.42	1.9	1575.423779	3779
1575.81	3.0	1575.813843	3843
1575.23	3.6	1576.233767	3767
1576.54	2.2	1576.543756	3756

Table 2. Detection of -110dBm sine-wave @ zoom 10

Input frequency -110dBm (MHz)	Detection t-value	Zoom 100 frequency determination (MHz)	Delta (Hz)
1574.40	3.6	1574.403298	3298
1574.91	2.5	1574.913287	3287
1575.03	2.6	1575.033293	3293
1575.42	1.8	1575.423304	3304
1575.81	2.9	1575.813315	3315
1575.23	3.8	1576.233293	3293
1576.54	1.9	1576.543309	3309

Table 3. Detection of -110dBm sine-wave @ zoom 100

Table 3 shows improved frequency correlation with an average delta of 3299Hz and standard deviation of 9.9Hz. The t-values are similar in Tables 2 and 3 showing a marked dip in the center.

Input frequency -110dBm (Hz)	Zoom 100 frequency (f1) determination (Hz)	diff	Adjusted frequency (Hz) (f1 – 3299)
1575422200	1575425509		1575422210
1575422210	1575425509	0	1575422210
1575422220	1575425536	27	1575422237
1575422230	1575425536	0	1575422237
1575422240	1575425536	0	1575422237
1575422250	1575425564	28	1575422265
1575422260	1575425564	0	1575422265
1575422270	1575425564	0	1575422265
1575422280	1575425592	28	1575422293

Table 4. Frequency resolution at zoom 100

During normal operation, the FFT covers the digitized IF range from DC to 2.8MHz. Each of the 1024 bins have a frequency range of about 2790Hz. To zoom in on an interfering signal found in a particular bin, the zoom level should cover the range of the bin to avoid ambiguities. At a zoom level of 10, the FFT covers a range of about 285kHz, with each bin being 279Hz wide, providing a potential frequency resolution to 279Hz. The overall requirement for proactive GPS interference mitigation as proposed in section 2 is for frequency resolution down to around 10Hz, a zoom level of 300 is the minimum to achieve this with a 1024 bin FFT, giving a range of 9523Hz and 9.3Hz per bin. Unfortunately, with 300 accumulations a problem can occur where the input to the FFT overflows producing

errors in the system. The alternate method of decimation solves this problem and in addition reduces the scaling range significantly, removing the need to monitor and adjust the scaling range settings. A zoom of around 100 appears to be the upper limit to avoid overflow with this method and an 8-bit FFT. At a zoom level of 100 the FFT range is 28.5kHz with bin width of 27.9Hz. Results from the second test are given in Table 4. This table reveals the frequency resolution with zoom level 100, showing frequency jumps of 27 and 28Hz for actual frequency changes of 30Hz in 10Hz steps. Table 4 also shows the frequency adjusted to account for the offset calculated from Table 3. It is evident that the system can work quite well and could provide accurate frequency determination once the internal frequency reference is calibrated.

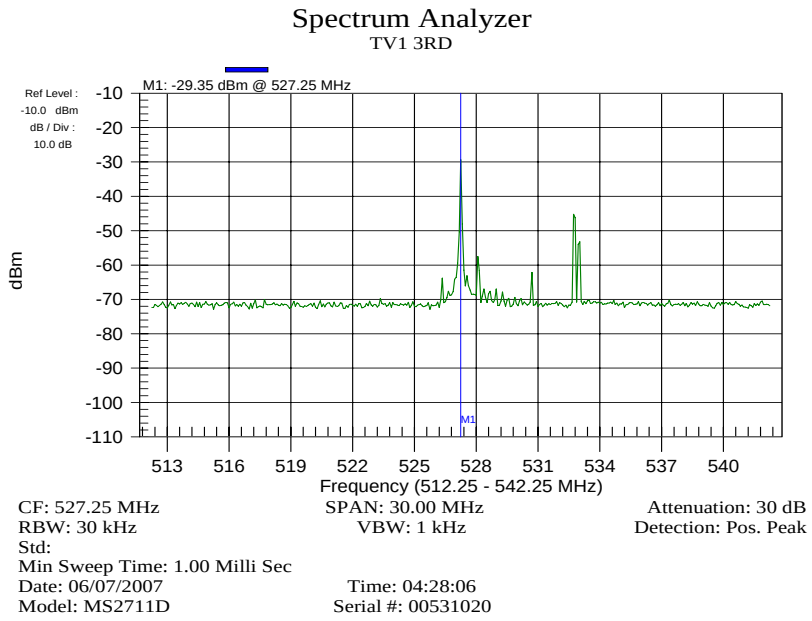

Figure 6. Frequency sweep around 527.25MHz near the Artarmon transmitter tower

The third test was a trial to evaluate the prototype system in the field. The area around the television and radio broadcast tower at Artarmon in the north of Sydney was chosen. Previous work by Tabatabaei *et al*. (2006) identified this site as a potential source of interference due to the third harmonic of a broadcast signal falling near the L1 band. There is a signal broadcast from the tower centred around 527.25MHz. Figure 6 shows a spectrum analyser sweep around this frequency. The third harmonic of this broadcast frequency would lie around 1581.75MHz, just outside the GPS L1 signal bandwidth of 2MHz centred at 1575.42MHz.

The prototype system was setup and run at a number of sites near the tower. A console window (see Figure 7) provided status information from the system, updated every few seconds. In Figure 7, the results of statistical processing including the maximum t-value and the frequency of the associated FFT bin can be seen over three cycles. Bin 533 keeps coming up as having the maximum t-value of around 0.57, with a frequency range of 1575.33812 to 1575.34091MHz.

The t-value threshold is set according to the level of confidence required in declaring the existence of interference. For a confidence level of 95% the t-value threshold is 1.64, clearly the obtained t-values are well under this level. The t test is used to trigger the switching to zoom processing to determine the frequency of the suspected interference signal to a higher resolution. The screen shot in Figure 8 reveals processing when the confidence level is

relaxed to investigate bin 533 in more detail. Figure 8 shows the transition to zoom processing, with the maximum power level found in bin 55 or 56 repeatedly over a trial of several minutes. This relates to a frequency of 1575.339682MHz, and removing the constant offset calculated previously of 3299Hz gives 1575.336383MHz.

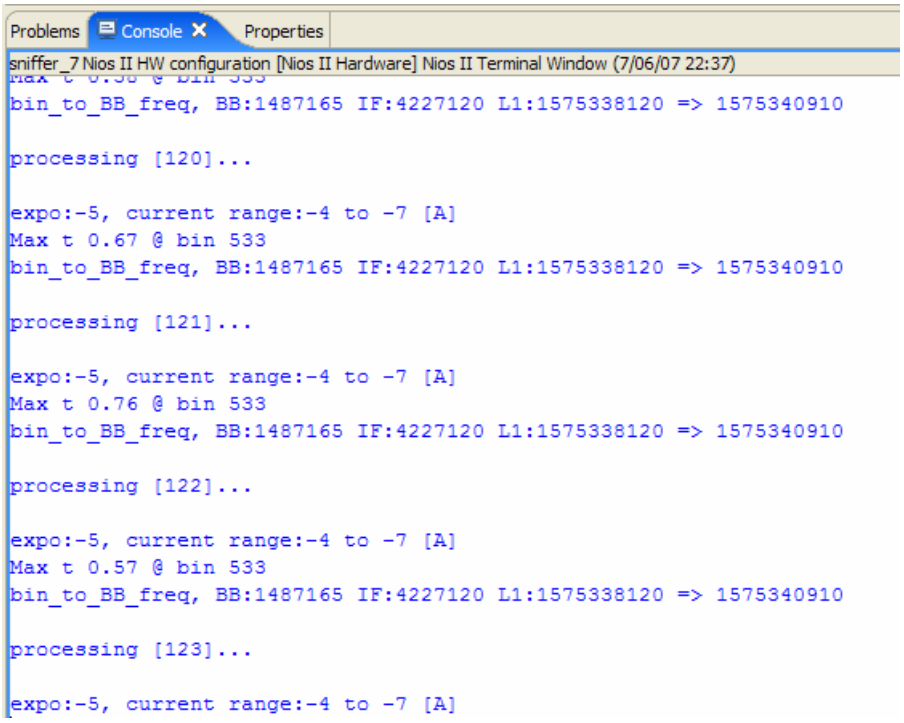

Figure 7. Example of statistical result output to a console window

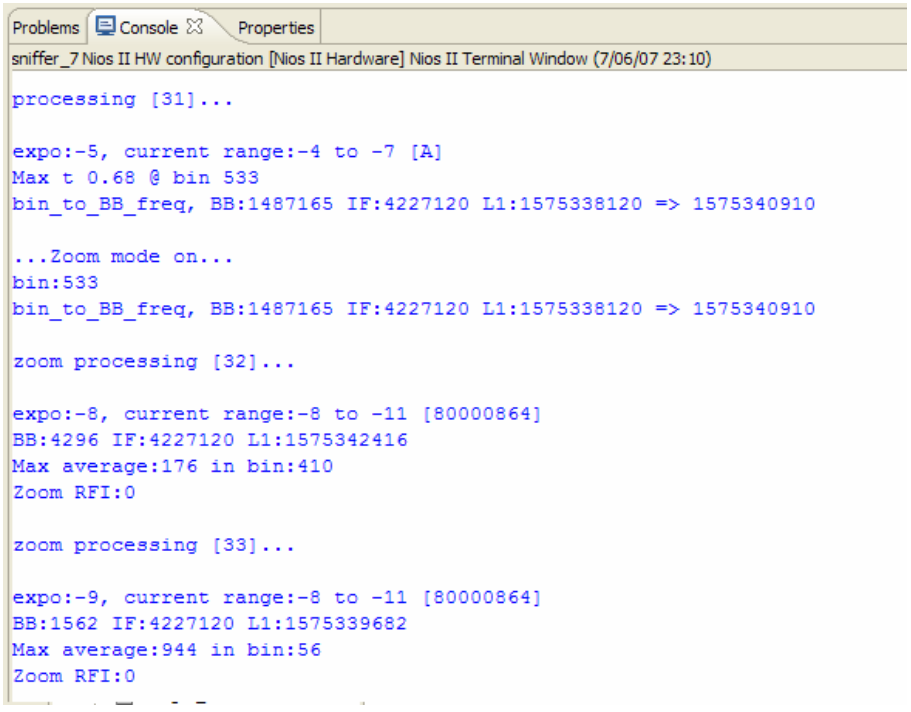

Figure 8. Example of zoom processing to console window

While this test is inconclusive, and certainly does not declare the existence of interference at a high level of confidence it does provide an example of the processing flow employed by the prototype system. The test was also performed in an area removed from known transmitters and maximum t-values (and associated bin number) over many trials where observed. There appeared to be no trend. Over a 50 trial sample the average t-value was found to be 0.39 with a standard deviation of 0.043.

6. SUMMARY AND FUTURE WORK

A prototype device for the detection of CW interference has been presented in this paper. Preliminary testing indicates that the fundamental design operates correctly. Testing has also helped in identifying areas where refinement, enhancements and further testing is required including; 1) improving sensitivity in the 'normal' mode, 2) changing from an accumulation to decimation technique in the zoom hardware to avoid FFT input overflow and alleviate the scaling problem, 3) frequency and power calibration of the reference RF signal generator, 4) create a frequency calibration technique for the detection device, 5) develop a user interface and 6) an interference reporting strategy.

The Namuru version 1 board has been used for development to this point, however, a new board (Namuru V2) will be available by the end of 2007. This board will have better specifications in a number of key areas, facilitating an improved and expanded detection hardware design with more FPGA space, two RF front-ends, more RAM and USB 2.0. A larger FPGA chip means a bigger FFT block can be used, potentially improving sensitivity and frequency resolution. In addition, a complete GPS receiver could sit alongside the detection unit, providing frequency calibration services. More RAM means bigger software programs; more sophisticated statistical algorithms and bigger data sets can be realised. Finally, the USB provides faster data transfer.

ACKNOWLEDGEMENTS

The authors acknowledge the support of the CRC for Spatial Information in funding this project (CRC-SI Project 1.1).

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