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Author:

Willems van Beveren, Laurens Henry; Tan, Kuan; Lai, Nai Shyan; Dzurak, Andrew; Hamilton, Alex

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Overlapping-gate architecture for silicon Hall bar field-effect transistors in the low electron density regime

L. H. Willems van Beveren,^{1,a)} K. Y. Tan,² N. S. Lai,² A. S. Dzurak,² and A. R. Hamilton³

¹Australian Research Council Centre of Excellence for Quantum Computer Technology, School of Physics, The University of New South Wales, Sydney 2052, Australia

²Australian Research Council Centre of Excellence for Quantum Computer Technology, School of Electrical Engineering and Telecommunications, The University of New South Wales, Sydney 2052, Australia ³School of Physics, The University of New South Wales, Sydney 2052, Australia

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We report the fabrication and study of Hall bar field-effect transistors in which an overlapping-gate architecture allows four-terminal measurements of low-density two-dimensional electron systems while maintaining a high density at the Ohmic contacts. Comparison with devices made using a standard single gate show that measurements can be performed at much lower densities and higher channel resistances, despite a reduced peak mobility. We also observe a voltage threshold shift which we attribute to negative oxide charge, injected during electron-beam lithography processing. © 2010 American Institute of Physics. [doi:10.1063/1.3501136]

A common issue in low temperature measurements of enhancement-mode metal-oxide-semiconductor field-effect transistors (MOSFETs) in the low electron density regime is the high contact resistance dominating the device impedance. In that case, a voltage bias applied across the source and drain contact of a Hall bar MOSFET will mostly fall across the contacts (and not across the channel) and therefore magnetotransport measurements become challenging. However, from a physical point of view, the study of MOSFET nanostructures in the low-electron density regime involves a number of interesting phenomena (impurity limited mobility,¹ carrier interactions,^{2,3} and spin-dependent transport⁴) and it is therefore important to come up with solutions that work around the problem of a high contact resistance.

Previously, a split-gate MOSFET technique^{5,6} was developed with submicron gaps (50-70 nm) in the gate electrode which allowed one to maintain a high electron density in the vicinity of the contacts regardless of its value in the main part of the sample. This technique has permitted reliable measurements of two-dimensional (2D) transport at low densities in the quantum Hall regime.' However, a prerequisite for this technique is that the gate oxide thickness must be larger than the gap size to ensure that the channel is continuous under the gap. Since it is challenging to fabricate in a reproducible manner narrow gaps on the nanometer scale over the full width of a MOSFET, this technique is not suitable for the study of MOSFET structures with very thin $(\sim 5 \text{ nm})$ gate dielectric. Moreover, the reactive ion etching process used to create the submicron gaps in the gate metallization could in principle reduce the device mobility.

In this letter, we present a simple device architecture that allows measurement of a thin-oxide Hall-bar MOSFET for very low electron densities in the channel, where the resistance of the contacts can be controlled electrically by separate electrodes (referred to as lead gates). The fabrication process involved, based on overlapping-gates, has been demonstrated for the fabrication of tunable few-electron silicon quantum dots^{8,9} and does not require additional processing steps like atomic layer deposition or polycrystalline silicon

etch steps that are known to reduce the device mobility.¹⁰ Figure 1 shows the scanning-electron microscope images of the two enhancement-mode Hall bar MOSFET device architectures studied in this work. The first device in panel (a) is fabricated by optical photolithography (PHOTO) and has a channel dimension of 19.9 by 4.9 μ m with L/W=4.06. Here a single aluminum gate (100 nm thickness) is patterned on top of a 5 nm SiO₂ gate dielectric which was grown by ultradry oxidation (UDOX) using dichloroethylene. The second device has a channel dimension of 19.0 μ m × 2.87 μ m, with L/W=6.62, and is fabricated by a two-step electron-beam lithography (EBL) process. The electron energy in the EBL process was 30 keV and a typical dose of 500–600 μ C/cm² was used to expose the e-beam resist.



FIG. 1. (Color online) Scanning electron micrographs of the MOSFET device architectures studied. (a) Photolithography defined Hall bar with a single gate. (b) EBL defined Hall bar with overlapping-gate architecture. (c) Zoom-in of panel (b) showing the area where the channel gate is electrically insulated from the lead gates by a thin layer of aluminum oxide Al_xO_y .

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^{a)}Electronic mail: l.h.willemsvanbeveren@unsw.edu.au.



FIG. 2. (Color online) (a) Control of the contact resistance R_c in the overlapping-gate Hall bar MOSFET (EBL fabricated device). Here only the channel gate voltage is swept as the voltage of the lead gates is increased stepwise from V_{lg} =0.6 to 1.0 V. (b) Four-terminal device resistance R_{4T} as a function of the lead gate voltage.

The channel gate is defined by thermal aluminum evaporation (50 nm) and lift-off, followed by oxidation on a hotplate 150 °C to form a layer of aluminum oxide, with a thickness of a few nanometers.¹¹ This dielectric film is used to electrically insulate the channel gate from a second layer of aluminum (100 nm), which defines "lead gates" to independently induce high-density electron layers connecting to the Ohmic contacts. To avoid leakage (pinholes) between the two layers of aluminum the overlap at the contacts is kept to a minimum (about 80 nm by 2 μ m). Both devices were subject to a final forming gas anneal (FGA) to reduce the interface trap density. The EBL device was also subject to a rapid thermal anneal at 1000 °C for 5 s directly after the UDOX process. The oxide thickness t_{ox} and interface trap density D_{it} for both devices were independently measured on *in situ* grown MOS capacitors by ellipsometry and capacitance-voltage deep level transient spectroscopy (CV-DLTS) analysis^{12,13} to be $t_{ox} = 5.4 \pm 0.2$ nm and $D_{it} \le 1 \times 10^{11} / \text{eV} / \text{cm}^2$ (near the conduction band edge), respectively.

We now discuss the electrical transport characteristics of the two device architectures in detail. Magnetotransport measurements up to 8 T were performed in a dilution refrigerator containing a superconducting magnet with a base temperature of 20 mK, using standard four-terminal ac lock-in techniques with an excitation voltage of 100–200 μ V at 87 Hz. Figure 2(a) shows that the contact resistance R_c of the Hall bar MOSFET with overlapping-gate geometry (EBL device) can be controlled, by adjusting the voltage of the lead gates V_{lg} , and is approximately independent from the channel gate voltage V_{cg} . The contact resistance was calculated by R_c $=1/2(R_{2T}-(L_{2T}/L_{4T})R_{4T})$, where R_{2T} and R_{4T} are the 2 and four-terminal device resistances and $L_{2T}=19.9 \ \mu m \ (L_{4T})$ =19.0 μ m) is the length of the current trajectory from source to drain (channel), respectively. In the EBL device the source and drain contacts are much closer to the voltage probes than for the PHOTO device, $(L_{2T}/L_{4T}) \sim 1$. Figure 2(b) shows the four-terminal device resistance corresponding to each trace in Fig. 2(a), demonstrating that R_{4T} is indepen-



FIG. 3. (Color online) Device resistance (a) and electron density (b) as function of (channel) gate voltage for the two device architectures studied.

dent of lead gate voltage. Even though the channel resistance R_{4T} varies by three orders of magnitude, the contact resistance is essentially independent of the channel gate bias. For $V_{lg}=1$ V the contact resistance is always much less than the channel resistance. This is especially important for measurements at low carrier densities, where interaction effects are significant¹⁴ but large R_c makes it hard to cool the electrons.¹⁵

The device resistance of the two device architectures as a function of applied channel gate voltage is compared in Fig. 3(a). For the PHOTO device the contact resistance is always dominating the channel resistance $(R_c \gg R_{4T})$. This is particularly evident close to threshold, where R_{2T} is starting to get very large (>10 M Ω), even though R_{4T} is only 1 M Ω . In contrast, in the EBL device, with lead-gates set to $V_{lo}=1$ V, we are able to keep the carrier density near the Ohmic contacts high, so that R_c is always less than R_{2T} . This enables us to measure reliably to much larger channel resistances $R_{4T} > 100 \text{ M}\Omega$, limited only by the input impedance of the voltage preamplifier (lock-in) used. Measurements with high impedance voltage preamplifiers will be carried out in the future to probe this regime in more detail. For the calculation of the contact resistance of the PHOTO device we used $L_{2T}=45.3 \ \mu m$ and $L_{4T}=19.9 \ \mu m$, so that $(L_{2T}/L_{4T}) = 2.27.$

Additionally, from the Hall effect measurements it is possible to obtain the 2D electron gas (2DEG) density *n* as a function of (channel) gate voltage $V_{(cg)}$. From Fig. 3(b) we can extract the gate capacitance per area of the two Hall bar devices $(C_{ox}/A) = (\epsilon_0 \epsilon_{r,eff}/t_{ox,eff}) = (Q/V) = e(dn/dV)$, where *A* is the channel area, $t_{ox,eff}$ is the effective SiO₂ thickness and ϵ_0 ($\epsilon_{r,eff}$) is the (effective relative) dielectric constant, respectively. Since the 2DEG is formed within 10 nm of the silicon crystal and the oxide film is only 5.4 nm thick, we use an effective dielectric constant defined by $1/\epsilon_{r,eff} = 1/\epsilon_r(Si)$ $+ 1/\epsilon_r(SiO_2)$ resulting in $\epsilon_{r,eff} = 2.82$ using $\epsilon_r(Si) = 11.9$ and $\epsilon_r(SiO_2) = 3.7$. For the PHOTO device, using C_{ox}/A $= 46 \ \mu F/cm^2$ as obtained from Fig. 3(b), we extract $t_{ox,eff}$ = 5.4 nm, in excellent agreement with CV-DLTS measurements.^{12,13} However, the slope of n(V) is noticeably



FIG. 4. (Color online) Mobility vs electron density. Note that with the EBL device one can measure at much lower densities as compared to the PHOTO device.

different for the EBL device, despite both devices having identical SiO₂ thicknesses. The difference in slopes (gate capacitance) indicates a difference in gate dielectric between the devices. Cross-sectional transmission electron microscopy (X-TEM) studies on similar devices has shown that the Al oxidation process, used to form the overlapping gates, leads to an extra insulating layer of Al_xO_y at the SiO₂/Al interface.¹⁶ This film has a dielectric constant $\epsilon_r(Al_2O_3)$ =11.5 (sapphire), that is, more than twice the value for SiO_2 . This results in a lower C_{ox} and an apparent thicker t_{ox} if we assume only SiO₂ is present between the gate and the channel. From this data we extract a sapphire thickness of $t_{\rm ar}(Al_rO_v) \sim 2$ nm, in reasonable agreement with the previous X-TEM study. The second key difference between the two device architectures is the large shift in threshold voltage ΔV_T , as seen in Fig. 3(a), which we will return to shortly. By plotting *n* versus V/t_{ox} we estimate that a total negative charge of $\sim 10^{12}$ cm⁻² is responsible for the ~ 400 mV shift in threshold voltage.

The channel mobility μ was measured as function of electron density n and is compared between the two types of devices in Fig. 4. The data demonstrate that the EBL device allows precise mobility measurements at lower 2DEG densities than possible with the PHOTO device. In the low electron density regime the critical density n_c (where $\mu=0$) measured on the PHOTO device extrapolates (blue dashed line) to the same value as measured with the EBL device, $n_c \sim 4$ $\times 10^{11}$ /cm². Equating the critical density with the interface trap density,² this suggests that the interface trap density D_{it} is the same for both device architectures, corresponding to an average area of $\sim 250 \text{ nm}^2$ per trap. In the high electron density regime, interface roughness limits the mobility. The larger gate voltages applied in this regime pull the electron wave function closer to the Si/SiO2 interface. In the intermediate electron density regime the peak mobility is determined by the interplay of impurity scattering and interface roughness. In this regime we observe a peak mobility for the PHOTO device of $\mu \sim 3800 \text{ cm}^2/\text{Vs}$ at a density of n=2 $\times 10^{12}$ /cm² which is consistent with previous calculations¹⁷ and experiments.¹⁸ In comparison, for the EBL device the peak mobility is substantially reduced to $\mu \sim 2700 \text{ cm}^2/\text{Vs}$. If we assume D_{it} is the same for both device types, we can only conclude that the large shift in threshold voltage V_T observed is related to negative fixed oxide charge, arising from the EBL device processing. This additional charge is a possible explanation for the reduction in peak mobility for the EBL device. Previous studies have showed that EBL processing (even after a postprocessing FGA) can cause threshold shifts of up to ~400 mV due to negative oxide charge, screening the gate electrode.¹⁹ We estimated from Fig. 3(b) the induced charge to be ~ $10^{12}/\text{cm}^2$. The trapped charge density and threshold shift are consistent with results of Aitken.²⁰

In summary, we have shown that the overlapping-gate device architecture allows accurate mobility measurements in the low electron density regime, not limited by contact resistance. The (extrapolated) critical density, or interface trap density, is the same for the two device architectures. We observe a large threshold voltage shift for the EBL device as compared to the PHOTO device. The EBL processing reduces the peak mobility in the intermediate electron density regime in comparison to the PHOTO device. The fact that the mobility for both device architectures in the low electron density regime is similar provides further evidence that the threshold shift is caused by fixed oxide charge and not by interface traps.

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