Atomically Controlled Device Fabrication Using STM

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Certificate of originality

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Abstract

We present the development of a novel, UHV-compatible device fabrication strategy for the realisation of nano- and atomic-scale devices in silicon by harnessing the atomic-resolution capability of a scanning tunnelling microscope (STM). We develop etched registration markers in the silicon substrate in combination with a custom-designed STM/ molecular beam epitaxy system (MBE) to solve one of the key problems in STM device fabrication - connecting devices, fabricated in UHV, to the outside world. Using hydrogen-based STM lithography in combination with phosphine, as a dopant source, and silicon MBE, we then go on to fabricate several planar Si:P devices on one chip, including control devices that demonstrate the efficiency of each stage of the fabrication process.

We demonstrate that we can perform four terminal magnetoconductance measurements at cryogenic temperatures after ex-situ alignment of metal contacts to the buried device. Using this process, we demonstrate the lateral confinement of P dopants in a d-doped plane to a line of width 90 nm; and observe the cross-over from 2D to 1D magnetotransport. These measurements enable us to extract the wire width which is in excellent agreement with STM images of the patterned wire.

We then create STM-patterned Si:P wires with widths from 90 nm to 8 nm that show ohmic conduction and low resistivities of $1 - 20 \times 10^{-6}$ Ωcm respectively – some of the highest conductivity wires reported in silicon. We study the dominant scattering mechanisms in the wires and find that temperature-dependent magnetoconductance can be described by a combination of both 1D weak localisation and 1D electron-electron interaction theories with a potential crossover to strong localisation at lower temperatures.

We present results from STM-patterned tunnel junctions with gap sizes of 50 nm and 17 nm exhibiting clean, non-linear characteristics. We also present preliminary conductance results from a 70×90 nm^2 dot between source-drain leads which show evidence of Coulomb blockade behaviour.

The thesis demonstrates the viability of using STM lithography to make devices in silicon down to atomic-scale dimensions. In particular, we show the enormous potential of this technology to directly correlate images of the doped regions with ex-situ electrical device characteristics.

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Change is created by those whose imaginations are bigger than their circumstances

-a dear friend

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List of Abbreviations

The following list includes both widely used abbreviations and abbreviations defined in the context of this work. Lists of symbols for selected SI units, non-SI units and SI prefixes are included in App. A. Symbols for some relevant fundamental constants are listed in App. B.1, and a list of relevant properties of Al is included in App. B.2.

1D	One dimensional
2D	Two dimensional
3D	Three dimensional
AB	Aharonov-Bohm
AC	Alternate current
AFF	Atomic Fabrication Facility
CB	Coulomb blockade
CQCT	Centre for Quantum Computer Technology
DC	Direct current
EBL	Electron-beam lithography
FIB	Focused ion beam
HMDS	Hexamethyl disilizane: $(CH_3)_3SiNHSi(CH_3)_3$
IPA	Isopropyl alcohol: $(CH_3)_2CHOH$
IVC	Inner vacuum chamber
MBE	Molecular beam epitaxy
MOSFET	Metal-oxide-semiconductor field-effect transistor
NML	National Magnet Laboratory
NW	Nano wire
OVC	Outer vacuum chamber
PMMA	Poly(methyl-methacrylate): $H[CH_2C(CH_3)(COOCH_3)]_nH$
QC	Quantum computer/computing
QCA	Quantum-dot cellular automata
QM	Quantum mechanics/mechanical
qubit	Quantum bit
QW	Quantum wire
RIE	Reactive ion etching

RT	Room temperature ($T = 20\ ^{o}\mathrm{C} = 293.15$ K)
RTS	Random telegraph signal
SEM	Scanning electron microscope/microscopy
SET	Single-electron (tunnelling) transistor
SI	Système International d'Unités
Si:P	Silicon doped with phosphorous
SIMS	Secondary ion mass spectroscopy
SL	Strong localisation
SNF	Semiconductor Nanofabrication Facility
SSQC	Solid-state quantum computer/computing
STM	Scanning tunnelling microscope/microscopy
STS	Scanning tunnelling spectroscopy
UHV	ultra high vacuum typically below $10^{-10} mbar$
UV	Ultraviolet
WKB	Wentzel-Kramers-Brillouin
WL	Weak localisation
XPS	X-ray photoemission spectroscopy

Publications arising from this work

Peer reviewed journals

[1] Rueß, F. J., T. C. G. Reusch, Pok, W., Scappucci, G., Hamilton, A. R., Simmons, M. Y., Formation and electrical characterisation of STM-defined, metallic Si:P islands. *In preparation* (2006)

[2] Rueß, F. J., B. Weber, Goh, K. E. J., Hamilton, A. R., Simmons, M. Y., Detailed study on the dephasing mechanisms in a narrow, STM-fabricated Si:P nanowire in the vicinity of the Thouless crossover. *In preparation* (2006)

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[1] Rueß, F. J., Oberbeck, L., Simmons, M. Y., Goh, K. E. J., Hamilton, A. R., Hallam, T., Schofield, S. R., Curson, N. J., Clark R. G., The fabrication of devices in silicon using scanning probe microscopy. *Proc. SPIE Int. Soc. Opt. Eng.* **5649**, 306 (2005)

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Conference presentations

[1] **Oral presentation**, Electrical properties of atomically controlled Si:P devices created by scanning probe microscopy. *28^{th} International Conference on the Physics of Semiconductors*, 24-28/07/2006, Vienna, Austria

[2] **Contributed talk**, Fabrication of silicon devices with atomically precise dop-. ing using scanning tunnelling microscopy
23^{rd} European Conference on Surface Science, 4-9/9/2005, Berlin, Germany

[3] **Scheduled talk**, STM-based Si:P devices. *US National Security Agency visit to Centre for Quantum Computer Technology*, 6/6/2005, Sydney, Australia

[4] **Contributed talk**, Scanning Probe Microscopy for Silicon Device Fabrication. *SPIE International Symposium on Smart Materials, Nano and Micro-Smart Systems*, 12-15/12/2004, Sydney, Australia

[5] **Poster**, The Fabrication of Nano-scale Devices in Silicon using Scanning Probe Microscopy. *2nd NTT- BRL School on Transport Properties in Quantum Nanostructures*, 08-14/10/2004, Fuji-yoshida, Japan

[6] **Invited talk**, Fabrication of nano-scale devices in silicon using scanning probe microscopy. *28th Annual Condensed Matter and Materials Meeting, Charles Sturt University*, 03-06/02/2004, Wagga Wagga, Australia

[7] **Contributed talk**, Fabrication of nano-scale devices in silicon using scanning probe microscopy. *International Conference on Nanometre-Scale Science and Technology (NANO-8)*, 28/06-02/07 2004, Venice, Italy

[8] **Highlight talk**, Fabrication of nano-scale devices in silicon using STM. *Centre for Quantum Computer Technology, Annual Workshop*, 09-13/02/2004, Avoca Beach, Australia

[9] **Contributed talk**, Scanning Probe Microscopy for Silicon Device Fabrication. *4^{th} Annual Coogee Bay Meeting*, 09/12/2004, Coogee, Australia

[10] **Contributed talk**, Fabrication of nano-scale devices in silicon using STM. *Atomically Controlled Surfaces, Interfaces and Nanostructures-7 Conference*, 16-20/11/2003, Nara, Japan

[11] **Poster**, Registration for Nano-Scale Devices. *US/Australia Workshop on Solid-State and Optical Approaches to Quantum Information Science*, 07-10/01/2003, Newport, Australia

[12] **Poster**, Registration for Nano-Scale Devices. *27th Annual Condensed Matter and Materials Meeting, Charles Sturt University*, 04-07/02/2003, Wagga Wagga, Australia

[13] **Contributed talk**, Registration for the fabrication of nano-scale devices using scanning probe microscopy. *3^{rd} Annual Coogee Bay Meeting*, 20/12/2002, Coogee, Australia

Patents

[1] **PCT/Au2004/001118 :** Fabricating nano- and atomic scale devices

[2] **PCT/Au2004/001119 :** Buried quantum device

Chapter 1

Introduction

The annual turnover of the electronics/semiconductor industries is over 1 trillion dollars constituting 10 % of the gross domestic product of the planet. The driving force for the continued expansion of the microelectronics industry is the ability to pack even more features onto a silicon chip, achieved by continual miniaturisation of the size of the individual components. Over the past three decades, this trend, known as *Moore's Law* has continued with the number of components on a chip doubling roughly every 18 months as shown in Fig. 1.1. Current state-of-the-art optical lithography used in commercial semiconductor manufacturing produces feature sizes down to $\sim$90 nm [1]. Most recently, researchers at IBM's Almaden Research Center have developed interference immersion lithography which uses two intersecting laser beams to create interference patterns with spacings as narrow as $\sim$30 nm [2]. If device miniaturisation continues at the same rate then by $\sim$2017 commercial device sizes will reach the sub-nanometre scale. To date, the only tools that have allowed the manipulation of matter at the atomic level are scanning probe microscopes.

Since the invention of the scanning tunnelling microscope (STM) in 1982 by Binnig and Rohrer [3], STMs have been used to create real space images of conducting surfaces with sub-atomic resolution. The seminal work by Eigler *et al.* [4] demonstrated that STMs can also be used to manipulate matter at the atomic level. A beautiful example is the STM-manipulated formation of a *quantum corral* [5] consisting of a circular arrangement of Fe atoms on a Cu surface, where STM imaging allowed the investigation of the wave nature of electrons on the surface of a metal. Atomic manipulation in semiconductors however has not been so easy due to the strong covalent bonds, requiring large voltages that damage the crystalline structure [6]. STM studies of the silicon surface date back to 1986 when Hamers *et al.* published the first real

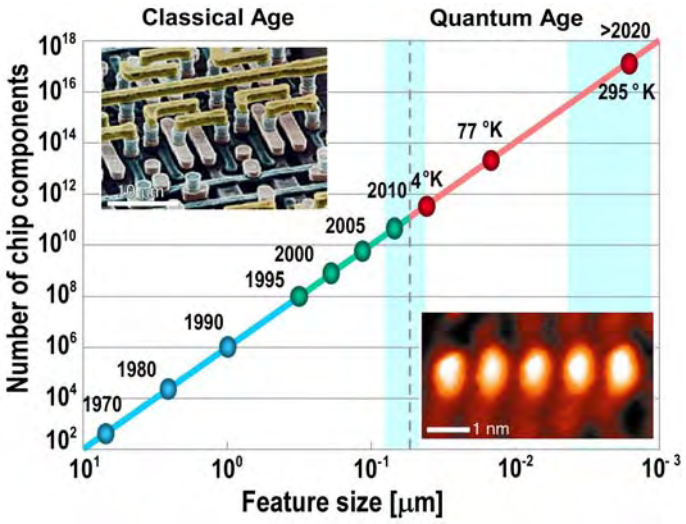

Figure 1.1: The number of components on a chip double roughly every 18 months as empirically found by G. Moore. As a consequence, device sizes will reach the sub-nanometre scale by ∼2017. *left inset:* Scanning electron microscope image of a transistor circuit. *right inset:* STM image of a hydrogen-terminated Si(100):H surface created in this thesis. 5 individual hydrogen atoms (bright features) were desorbed from the surface using STM lithography demonstrating atomic-scale pattern control.

space images of the electronic properties of Si(111) [7] and Si(100) [8]. Since then, the properties of the Si(100) surface have been widely studied due to its extensive use in the semiconductor industry. However, to achieve atomic manipulation in this system without damaging the surface, a resist strategy was developed similar to that found in the semiconductor industry, where optical lithography is used [9], [10], [11], [12]. The basic concept involves passivating the silicon surface with hydrogen atoms thus forming an atomic monolayer of hydrogen resist. The extremely confined electron beam from an STM tip can then be used to remove multiple and even individual hydrogen atoms from this resist under certain voltage and current conditions thereby exposing the silicon surface underneath. These highly reactive dangling bonds can then be used for the adsorption of atomic and molecular species. Initial studies on the hydrogen-passivated Si(111) surface by Becker *et al.* [9] proved the concept, before the process was demonstrated on the technologically more prevalent Si(100) surface by various other groups [10], [11], [12].

This approach has since been adopted to form nano-scale features on the silicon surface for the subsequent adsorption of numerous materials including oxygen [11], ammonia [13], aluminium [14], gallium [15], silver [16], cobalt [17], [18] and

phosphine [19]. More recently, the adsorption of organic molecules such as Styrene [20], TEMPO [21], Vinylferrocene [22] and carbon nanotubes (CNT) [23] on an STM-patterned, hydrogen-terminated Si surface has been reported in the emerging field of molecular electronics. However, since 1997, there has been a growing interest to incorporate STM-based lithography into proposals for atomic-scale semiconductor device fabrication [19], [24], [25], [26]. To date, few device structures have been realised [27], [28], [29], [30], [31] due to the technological difficulty of making electrical contact to the STM-patterned region. However, one of the key advantages of using an STM for device patterning is, that it allows us to observe each stage of the fabrication process and see exactly where the adsorbates are, so that we can relate the structural distribution at the atomic-scale directly to its electrical device characteristics.

As mentioned, one of the major hurdles for making functional semiconductor devices with the STM is connecting leads to the device once it is removed from the UHV environment. In this thesis, we concentrate on the use of the STM to pattern a hydrogen resist layer for the subsequent adsorption of phosphorus dopants in silicon via a phosphine source. Since the STM can essentially create an atomically perfect device, there is little contrast between the STM-patterned dopants and their surrounding silicon environment, making the device invisible to optical and electron beam microscopes. As a consequence, it is necessary to register the STM-patterned structure to some sort of feature or marker on the silicon surface before it is removed from the vacuum. These markers can then be used to align macroscopic contacts to the buried dopant structure to form a device, so that we can perform electrical measurements. One way to overcome this challenge is to develop registration markers that survive all the high temperature and UHV-STM fabrication steps, without contaminating the atomically flat surface required for atomic-scale STM imaging and lithography.

This thesis contains the development of such an ultra-high vacuum compatible (UHV) strategy for atomically controlled STM device fabrication. The fabrication process is based on the development of (1) registration markers etched into the silicon, (2) hydrogen based STM lithography for device patterning, (3) harnessing the self-terminating adsorption properties of phosphine gas as a dopant source, (4) thermal P incorporation from the phosphine molecule into the top Si layer and hydrogen resist removal, (5) low temperature silicon molecular beam epitaxy for device encapsulation and (6) ex-situ alignment of metal contacts to the buried devices using the registration markers to allow four terminal, temperature-dependent conductance measurements.

In particular, we demonstrate (Chapter 4) a novel UHV compatible device fabrication strategy for the realisation of nano- and atomic-scale devices in silicon which uses a combination of etched registration markers and a custom designed STM-SEM/molecular beam epitaxy system. We demonstrate various intermediate steps of the fabrication process to show that hydrogen acts as a perfect resist layer and that the STM desorption process leads to complete resist removal. We also demonstrate the registration marker concept by contacting a 4×4 μm^2 sized P-doped device. Comparison between an unpatterned control device and the P-doped device confirm that the alignment of surface contacts to the buried STM pattern truly leads to conduction through buried P dopants.

In Chapter 5, we present Hall measurements on this square device clearly demonstrating that electrical dopant activation of the P dopants is not affected by the lithographic process. We then go on to compare this with a device, where we further confine the P dopants by STM patterning into a 90 nm wide wire. We observe a crossover from 1D to 2D magnetotransport behaviour of this device at low temperatures, where the electron phase coherence length exceeds the width of the wire. The magnetic length at the crossover point is used to extract the electrical width of the wire which shows excellent agreement with the 90 nm wire width patterned by STM.

In Chapter 6, we investigate the electrical transport characteristics of a series of STM-patterned wires from widths of 50 nm to 8 nm. We show that the wires remain structurally intact and observe ohmic conduction down to widths of 8 nm with very low resistivities (1 – 20×10^{-6} Ωcm) compared to the literature. Particular focus is given to a detailed temperature-dependent, electrical characterisation of a 27 nm wide wire, in order to study what scattering mechanisms limit device conductance at millikelvin temperatures. We show that the conductance is affected by electron-phonon dephasing at higher temperatures. At intermediate temperatures the conductance correction is dominated by 1D weak localisation and electron-electron interaction effects. Finally at low temperature, we observe the onset of strong localisation in this highly doped, planar nanowire which is likely to limit the wire conductance for thinner wires towards the atomic-scale.

In Chapter 7, we explore the electrical characteristics of tunnel junctions with gap sizes down to 17 nm formed between two buried P-doped leads patterned by the STM. The corresponding I-V characteristics are highly non-linear exhibiting smooth, low noise differential conductances with no sign of resonant tunnelling or Coulomb

blockade behaviour. The clean results obtained from these tunnelling junctions bode well for the fabrication of more sophisticated devices such as single electron transistors (SETs).

We pursue the formation of one such Coulomb blockade type device structure, where transport is governed by single electron charging effects, in Chapter 8. In particular, we report on the formation of Si:P dots with island sizes down to 10×10 nm^2 corresponding to $\sim$100 P dopants. Electrical measurement results of a 70×90 nm^2 source-island-drain device suggest that device characteristics at 4 K are governed by Coulomb blockade behaviour.

Overall, the thesis demonstrates the ability of the STM to pattern devices with dimensions to below $<$10 nm. By using a novel registration technique, it is now possible to align *ex-situ* macroscopic contacts to buried STM-fabricated Si:P devices using conventional optical lithography. The electrical characterisation of devices such as narrow Si:P wires, tunnel junctions and Coulomb blockade devices enable the study of their characteristic transport properties at low temperatures and provides vital information for the fabrication of devices with feature sizes approaching the quantum limit. The achievement of electrical device characterisation together with the recent demonstration of single P atom placement with atomic precision [32] make STM-based fabrication strategies a suitable candidate technology for the fabrication of more advanced semiconductor devices down to the atomic-scale such as a solid state quantum computer [33]. Here, either the electron or nuclear spin of single phosphorus acts as quantum bit (qubit). A considerable challenge for the future realisation of such atomic-scale devices is the incorporation and alignment of surface gates to control the charge transfer between the phosphorus atoms. For this purpose, several pathways to implement an insulating barrier, separating the device from the gate, are currently under way in our group.

However, a key advantage of this fabrication technique is that devices can be monitored with atomic precision as they are made, allowing, for the first time, to correlate device specific dopant distribution with the results from electrical device characterisation. Finally, using this strategy, it will be possible to perform multilevel STM-patterning. In combination with atomic precision MBE growth, this will allow the formation of truly 3D atomic-scale devices, giving atomic-scale patterning resolution in all three spatial dimensions.

Chapter 2

Background

2.1 Scanning Probe Microscopy

Ever since the invention of the scanning tunnelling microscope by Binnig and Rohrer [3] at IBM Rüschlikon, Switzerland 25 years ago, the STM has found its way as a standard research tool for the study of conducting surfaces at the atomic level. The minimal lateral extension of the wavefunction of a sharp metal tip in combination with the exponentially sensitive tunnelling current are the key reasons which provide scanning probe techniques with the unique capability to image and manipulate individual atoms.

Atomic level control implies a high level of mechanical stability, positioning at the atomic-scale and stable feedback operation between the acquired measurement current and the positioning unit. This is generally achieved by means of different vibrational damping mechanisms such as eddy-current damping or airleg damping in order to decouple the STM from its environment. Accurate positioning is achieved using piezo-ceramic actuators.

By approaching the tip of an STM close to a metallic or semiconducting surface, electrons can tunnel from the tip to the sample or, vice versa depending on the polarity of the bias voltage. By scanning the STM tip over the sample surface, a topological map z(x,y) is obtained which comprises a convolution between the topographic and electronic properties of the sample. STM imaging performed by tunnelling from the tip into unoccupied sample states is referred to as *empty state* imaging whereas tunnelling from occupied sample states to the tip is known as *filled state* imaging.

In this section, the underlying theoretical foundation of the principal mode of operation of the STM is presented. Whereas the basic operation mode can be explained

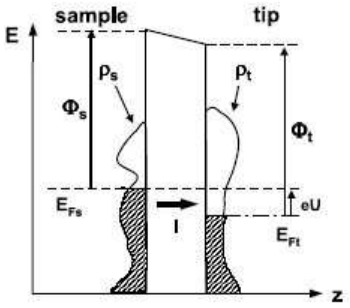

Figure 2.1: Tunnel junction with sample, vacuum barrier and STM tip. States with energies between the Fermi levels of the tip and the sample over the energy range eU contribute to the tunnel current. $\Phi_{s,t}$ denotes the work function of the sample and tip respectively.

using relatively simple quantum tunnelling pictures, the quantitative interpretation of STM images is a somewhat more complicated topic and the subject of active research. Excellent reviews on the theoretical description of STM [34], [35], [36] have been written to which the interested reader may refer to for a more detailed treatment.

2.1.1 Bardeen's approach and the Tersoff-Hamann expression

Bardeen's early work on macroscopic tunnel junctions [37] is historically the starting point for a qualitative description of the tunnelling process. The tunnelling current strongly depends on the overlap between the tip and the sample state and can be obtained by summing over all relevant sample and tip states. The resulting current after the application of a small bias voltage is given by:

$$I \propto \int \left(f(E_F+\varepsilon) - f(E_F - eU + \varepsilon)\right) \rho_s(E_F+\varepsilon)\rho_t(E_F - eU + \varepsilon) \mid M \mid^2 d\varepsilon \qquad (2.1)$$

where $f(E) = \frac{1}{1+exp(E/kT)}$ is the Fermi-Dirac distribution function and $\rho_{s,t}(E)$ are the density of states (DOS) for the sample and the tip respectively. The gap voltage between STM and sample is labelled U, ε denotes the energy difference with respect to the Fermi energy E_F. In Bardeen's approximation, the matrix M contains the tunnelling elements which are approximated by the exchange integral that describes quantum tunnelling from sample to tip states (or vice versa):

$$< \varphi \mid M \mid \psi > \approx -\frac{\hbar^2}{2m} \int \psi(\mathbf{r})\Delta\varphi(\mathbf{r}) - \varphi(\mathbf{r})\Delta\psi(\mathbf{r}) d\mathbf{n} \qquad (2.2)$$

where $\varphi(\mathbf{r})$, $\psi(\mathbf{r})$ are the electron wavefunctions emerging from the Hamiltonian in the sample and the tip respectively and $d\mathbf{n}$ is a vector normal to a surface of constant energy.

For low temperatures ($T \rightarrow 0$), small bias voltages or where the experimental energy resolution is smaller than kT, the Fermi-Dirac distribution in Eq. 2.1 can be replaced by Heavyside (step-) functions. Thus Eq. 2.1 reduces to

$$I \propto \int \rho_s(z, E_F + \varepsilon)\rho_t(E_F - eU + \varepsilon) \mid M \mid^2 d\varepsilon \tag{2.3}$$

where $\rho_s(z, E)$ is the local density of states (LDOS) at a location z and energy E, defined as:

$$\rho(z, E) \doteq \frac{1}{\epsilon} \sum_{E_n = E - \epsilon}^{E} |\Psi_n(z)|^2 \tag{2.4}$$

where $|\Psi_n(z)|^2$ is the probability density of a sample state. From Eq. 2.3, we can see that the tunnelling current I depends on the *integral* over the LDOS of the sample.

For metal surfaces, we can assume that the density of states in the tip and the sample and the elements of $\mid M \mid$ are nearly constant over the probed energy range E from E_F to $E_F - eU$ and E $\sim E_F$ due to the small applied voltages needed for imaging. A simple expression for the tunnelling current is then obtained:

$$I \propto U\rho_s(E_F)\rho_t(E_F) \tag{2.5}$$

Derivation of Eq. 2.5 yields the differential conductance:

$$\frac{dI}{dU} \propto \rho_s(E_F)\rho_t(E_F) \tag{2.6}$$

Therefore the differential conductance is a measure of the local density of states since $\rho_t(E_F)$ was assumed constant in first order approximation, which is a valid assumption for metals. Tersoff and Hamann [38], [39] derived a similar expression for the tunnelling current by modelling the electron wavefunction of the tip by radially symmetric wavefunctions, namely

$$I \propto U \cdot \rho_s(E_F, r_0)\rho_t(E_F) \tag{2.7}$$

where r_0 is the centre of curvature of the STM tip.

As a consequence of the surface band gap in most semiconductors[1], the applied STM voltage is of order $\pm$ 1 – 10 V. Therefore, the *low voltage* approximation does

[1]The indirect band gap of Si is 1.4 eV.

not hold anymore. To accommodate for the higher applied bias, Hamers *et al.* [36] modified Eq. 2.3 by replacing the tunnelling matrix M with an energy-dependent tunnelling coefficient $T(E, eU)$:

$$I \propto \int \rho_s(E_F + \varepsilon)\rho_t(E_F - eU + \varepsilon) \mid T(\varepsilon, eU) \mid^2 d\varepsilon \tag{2.8}$$

The transmission coefficient contains information about the energy-dependent decay of the electron wavefunction and the voltage dependence of the vacuum barrier formed between the tip and the sample. A simple model [36] of the vacuum barrier is a linear potential drop of the applied voltage on the barrier resulting into a trapezoidal shape. Using the Wentzel-Kramer-Brillouin (WKB) method to obtain the respective wavefunction for such a potential, $T(E, eU)$ can be approximated by

$$T(E, eU) = e^{-\frac{2z\sqrt{2m}}{\hbar}\sqrt{\frac{\Phi_s+\Phi_t}{2}+\frac{eU}{2}-E}} \tag{2.9}$$

where z is the sample tip distance, $\Phi_{s,t}$ are the work functions of sample and tip respectively. At higher bias voltages, the tunnelling current is not directly related to the LDOS anymore. Instead states with higher energies above the Fermi level govern the tunnelling current due to their lower tunnelling barrier. Therefore the interpretation of STM images of semiconductor surfaces in the higher bias regime is more complicated.

2.1.2 Vertical resolution

The vertical resolution of STM [34] may be estimated from the textbook solution of 1D quantum tunnelling, where the barrier height is given by:

$$\Phi = \frac{\hbar^2}{8m}\left(\frac{d\ lnI}{dz}\right)^2 \tag{2.10}$$

Using the work function of Si and that of W, the most commonly used STM tip material, $\Phi \sim 4.8$ eV, the tunnelling current changes by one order of magnitude for a height displacement of 1 Å. For comparison, an atomic step on the Si(100) surface corresponds to a geometric height change of 1.4 Å. High resolution images with vertical resolutions $<$0.5 Å are regularly observed in STM experiments from our group and others.

2.1.3 Lateral resolution

For obtaining high quality topographic images of the sample surface, it is not only important to have a high vertical resolution but also a high lateral resolution, i.e. in

the (x, y) sample plane. Tersoff and Hamann [38] derived an expression to estimate lateral resolution:

$$\Delta x = \left(\frac{\hbar \cdot (r_0 + l)}{\sqrt{4m(\Phi - E)}} \right)^{\frac{1}{2}} \tag{2.11}$$

where, r_0 refers to the curvature of the tip apex and l stands for the tip sample separation. In the limit of low bias voltages, using the work functions for Si and W, the typical sample tip distance of a few Å and a tip apex curvature of a few nanometres, the estimated lateral resolution is only of order 1 – 2 nm insufficient to explain the sub-atomic resolution observed experimentally [40]. This estimation led researchers to believe, that the tunnelling current is mainly carried by a single atom sitting at the end of the STM tip. Indeed, it was widely accepted that atomic resolution images are obtained by tunnelling from a single atom as first proposed by Lang et al. [41]. However Yang *et al.* [42] performed atomic charge superposition calculations of STM images of glycine and alanine on a graphite surface and found that for interpretation of the images, STM tip states have to be taken into account. They concluded that the high resolution stems from tunnelling into a d-type localised state of the W tip. This shows, that for a precise analysis of the atomic resolution capability, the (material-specific) tip and sample states have to be taken into consideration.

2.2 Operating modes

2.2.1 Constant current measurements

The most commonly used mode of operation of an STM (also used in this thesis) is the constant current mode, where the height change z across the surface is measured at a constant tunnelling current. This necessitates a feedback loop between the positioning instruments and the tunnelling current such that the sample tip distance is adjusted to keep the average tunnelling current constant. The height changes z are measured as a function of the lateral piezo displacement (x, y). The resulting matrix is a convoluted representation of the sample's electronic and geometric topography.

2.2.2 Constant height measurements

In constant height mode, the sample tip distance is held constant and the variation of the tunnelling current is measured across the (x, y) plane. This mode of operation is

convenient since it does not require a feedback loop. However, it is only suitable for small scan areas, since the STM tip is likely to collide with the sample surface due to sample tilt, corrugation and thermal drift.

2.2.3 Scanning tunnelling spectroscopy

From Eq. 2.3, we can see that the voltage-dependent tunnelling current measurements provides information of the integral LDOS governed by those energy states with the highest energies due to a lower tunnelling barrier. Therefore, by imaging the sample surface using different bias voltages, information about the LDOS may be obtained.

Such a measurement can be performed in two different ways. One way is to sequentially image the sample surface under different bias conditions thus obtaining a topological map z(x,y) at various constant biases. In order to obtain information about the LDOS close to the surface band gap, where the tunnelling current is low, a better way is to fix the tip height at a fixed point of the surface area (x, y) with a higher, constant tunnelling current I_0 and then, by varying the STM tip bias, measure the superimposed $\frac{dI}{dV}$ characteristics. This technique is known as Constant Imaging Tunnelling Spectroscopy (CITS). A complete topographic image consisting of a three-dimensional tunnelling current matrix $\frac{dI}{dV}(x, y, V)$ is obtained by a step and repeat procedure across the *(x,y)* plane. We have applied this technique in Chapter 6 to investigate the integrity of Si:P wires buried under a few monolayers of epitaxial silicon.

In order to interpret STM tunnelling spectroscopy measurements in terms of the surface LDOS, it is common practice to normalise $\frac{dI}{dV}$ by dividing by $\frac{I}{V}$, as proposed by Stroscio and co-workers [43]. This normalisation eliminates the exponential dependance of the transmission probability on the STM bias and expresses the normalised tunnelling conductivity as $\frac{dI}{dV} \cdot \frac{V}{I} = \frac{dlnI}{dlnV} \approx \rho_S(E)$, which represents an approximation of the sample LDOS.

2.3 STM: manipulation at the atomic scale

So far, we have only discussed the use of STM as an imaging tool. However, a key use of STMs has been their application to position and manipulate matter at the atomic scale. The following list summarises the basic manipulation processes as identified by IBM Zürich Research Laboratory.

- Lateral manipulation: The transfer of atoms/molecules along the surface employing for example attractive/repulsive forces between the tip and the adsorbate [5].
- Vertical manipulation: The reversible transfer of atoms/molecules between the surface and the STM tip employing additionally electronic/vibrational excitation of the adsorbate by inelastic tunnelling [44].
- Desorption: Similar to vertical manipulation, but desorption of individual adsorbates directly into the surrounding gas phase [12].
- Dissociation: Selective bond breaking within a molecule by means of inelastic tunnelling processes [45], [46].
- Synthesis: Selective bond formation between two molecular units employing lateral manipulation followed by electronic/vibrational excitation [47], [48].
- Change of intramolecular conformation: Attractive/repulsive forces between the STM tip and the adsorbate can be applied to change the intramolecular conformation of usually specially designed molecules [49], [50].

2.4 Silicon

Silicon is one of the most extensively studied materials due to its use in the semiconductor industry. It forms the basis of a huge class of electronic devices such as transistors, microprocessors and solar cells.

The lattice structure of bulk silicon consists of a unit cell with four Si atoms. Each atom is sp^3 hybridised forming a covalent bond to four neighbouring atoms. The lattice type is the diamond type face centred cubic (fcc) Bravais lattice with a two atomic primitive basis of two Si atoms sitting at positions with respective Miller indices of $(0,0,0)$ and $(\frac{1}{4},\frac{1}{4},\frac{1}{4})$.

A three dimensional schematic of bulk Si is shown in Fig. 2.2. The experimental work presented in this thesis has been performed on the Si(100)-2$\times$1 surface reconstruction. In the following, we focus on the properties of the Si(100) surface although a variety of different reconstruction exist [52].

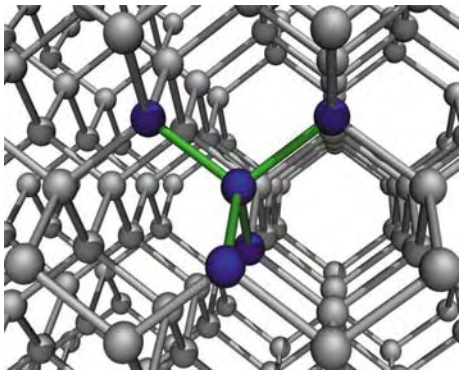

Figure 2.2: A schematic image highlighting the tetrahedral arrangement of silicon atoms in the bulk. Taken from [51].

2.4.1 Si(100) surface

A perfect cut along the Si(100) axis is illustrated in Fig. 2.3 (a). Here, each atom has two broken bonds [Fig. 2.3 (b)] protruding from the surface, which are commonly referred to as *dangling bonds*. These dangling bonds are highly reactive, making this surface energetically unfavourable, thus it undergoes a *reconstruction* to minimise its free energy. The resulting surface configuration is known as the 2×1 reconstruction. Two Si atoms pair up to form a strong, directed σ bond and a weakly coupled π bond. A schematic of the resulting surface is seen in Fig. 2.3 (b). Pairs of Si atoms, called *dimers*, form rows on the surface with a 2×1 periodicity with a distance between Si dimers of 7.6 Å. The energy level diagram arising from the coupling of dangling bond orbital of the Si atoms in Fig. 2.3 (d) shows the two bonding orbitals, σ and π, as well as the two anti-bonding orbitals σ^* and π^*. At low negative bias, electrons mainly tunnel through the π bonding state (filled state image). For low positive bias (empty state imaging), however, the main contribution arises from tunnelling into π^* anti-bonding state. The different spatial energy level distribution of the π and π^* states gives rise to a bias-dependent electronic topography making a Si dimer appear as a bean-shape in filled state or a pair of protrusions in empty state imaging respectively.

The first unequivocal confirmation of the Si(100) 2×1 reconstruction came with the first STM images of the Si(100) surface in 1985 [8], [53] and confirmed earlier theoretical predictions by Chadi [54] that the basis unit of the Si(100) is the Si dimer. Chadi's calculations also predicted, that the surface free energy is further minimised by a transfer of charge from one of the dimer atoms to the other. The charge transfer results in dimer buckling across the surface with a buckling angle of 19 °. However,

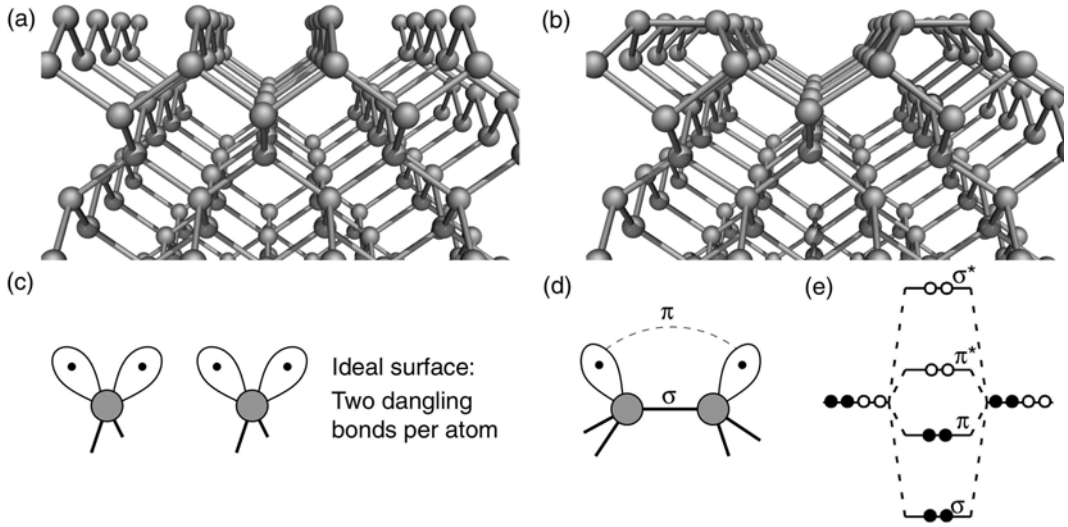

Figure 2.3: Si(100) surface reconstruction. (a) Ideal Si(100) surface. (b) Reconstructed Si(100) 2×1 surface. (c) Dangling bonds of a single Si atoms. (d) Si dimer bonding formation consisting of a directed σ bond and a weak π bond and (e) energy level diagram. Taken from [51].

STM images of the Si(100) surface at room temperature revealed that the majority of Si dimers appeared symmetric with the appearance of a few buckled dimers due to defect sites and step edges. Low temperature STM experiments reported by Wolkow [55] showed that at T = 120 K, 80 % of the Si dimers are found to be buckled. This observation confirmed the conclusion that the Si(100) surface at room temperature exhibits bistable Si dimers with alternating charge transfer between the two Si dimer atoms. This results in a Si dimer oscillation frequency much higher than the sampling frequency of the STM. Therefore the STM averages over many oscillations during the image acquisition resulting in the observation of symmetric Si dimers.

In real life, it is impossible to cut Si exactly along one crystallographic axis with atomic precision. As such, a miscut angle exists on the surface which results in the formation of a series of atomically flat terraces separated by step edges. The monoatomic step height from one terrace to another is ∼1.4 Å. There are two types of step edges [56]. Type S_A exhibits dimer rows which run perpendicular to the step edge, where as type S_B is characterised by dimers running parallel to the step edge. Fig. 2.4 shows ball and stick models of the two step edge types. The blue coloured atoms in the top view indicate the upper atom in the buckled configuration due to the boundary condition given by the step edge. Type S_A step edges induce static buckling whereas dimers at a

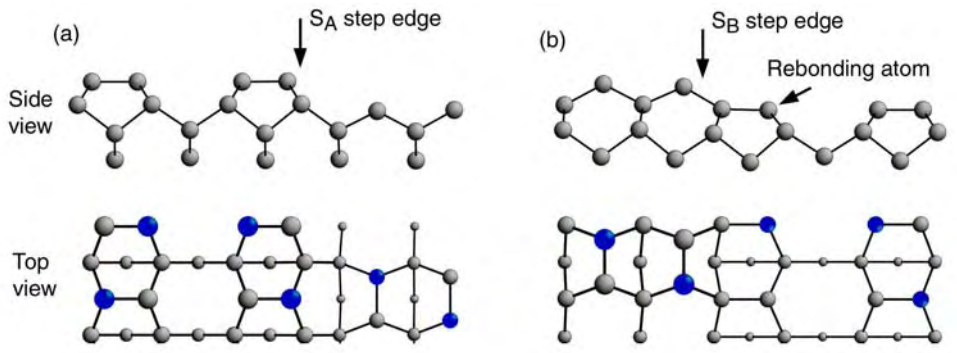

Figure 2.4: Two types of step edges on the Si(100) surface.. Top and side view of type S_A (a) and type S_B (b) step edges. Taken from [51].

type S_B step edge remain free to alternate between different buckling directions. The next section contains an introduction of the basic defects which are generally observed during STM experiments on the Si(100) surface.

2.4.2 Common defects on Si(100)

The characterisation of the three most commonly observed defects on the Si(100) 2×1 surface goes back to the original classification by Hamers and Köhler [57].

Originally, they were labelled type A, B and C defect respectively. The type A defect is simply a missing Si dimer and more appropriately known as the single-dimer vacancy (DV) defect [58]. The type B defect is the result of a double-dimer vacancy. A combination of these two defects separated by a dimer unit is the 1+2-DV defect, known as the split-off dimer. The occurrence of the split-off dimer on Si(100) is generally related to metal contamination with minute amounts of Ni or W [59], [60]. An increased amount of metal contamination or repeated sample preparation tends to increase the number of dimer vacancies. A sufficiently high defect density typically aligns the dimer vacancies at high temperature to form the $2 \times n$ reconstruction. Such regularly spaced trenches between the Si dimers have also been observed due to the presence of carbon on the surface [61]. Figure 2.5 summarises the different bonding arrangements that arise due to the presence of type A and type B DV defects on the Si(100) surface.

The C defect remains the subject of ongoing debate and it is predicted that several types exist. The most recent interpretations of the origin of the C defect include the absence of a Si atom in the second layer [62] or the presence of subsurface impurities

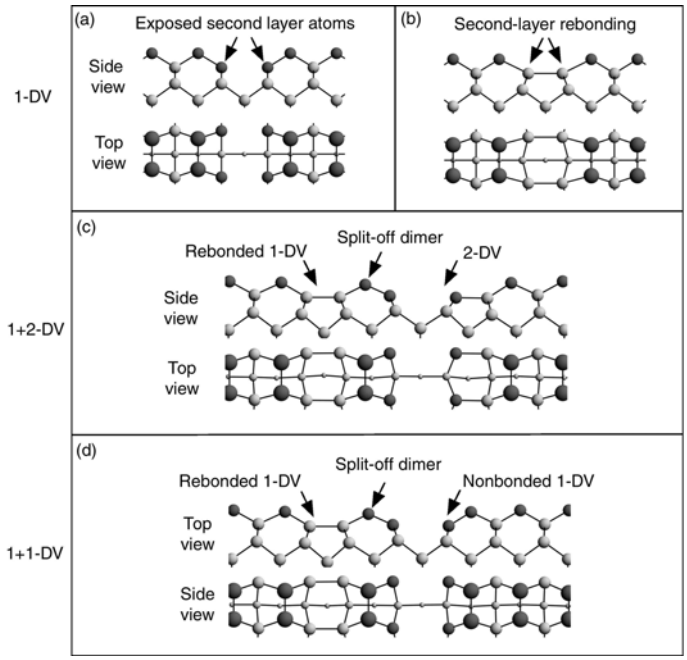

Figure 2.5: Schematic of defect combinations resulting from type A and B dimer vacancy (DV) defects.. Ball and stick models of the (a) non-bonded 1-DV, (b) rebonded 1-DV, (c) 1+2-DV and (d) 1+1-DV. Taken from [51].

such as H, O or B [63]. A summary of three proposals for the structure of the C defect is given in Fig. 2.6. As opposed to the type A and type B defects, the type C defect breaks the mirror symmetry between the two atoms of the Si dimer and introduces buckling of the surrounding dimers.

2.4.3 Interaction and relevance of hydrogen on Si(100)

Hydrogen molecules (H_2) are one of the major residual gas components in any ultra-high vacuum (UHV) system. However, the *sticking coefficient*, i.e. the ability of molecular hydrogen to adsorb on the Si(100) surface, is negligibly small [64]. On the other hand, the sticking coefficient for the adsorption of atomic hydrogen is high. The bonding formation of atomic hydrogen thereby depends on both, its partial pressure and the Si substrate temperature.

Four distinct surface phases of hydrogen on Si(100) are shown in Fig. 2.7 and characterised as follows:

- **Monohydride**: one H atom is bound to each Si atom of the dimer by breaking the weak intradimer π bond [Fig. 2.7 (a)].

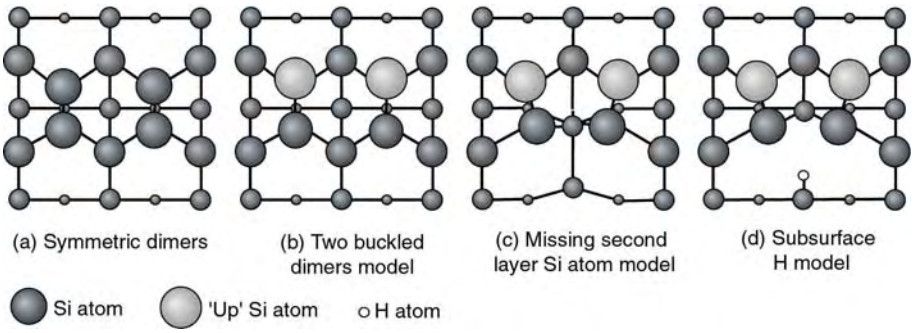

Figure 2.6: Three different models proposed for the C defect of Si(100). (a) Symmetric Si dimers, (b) Buckled dimer model, where two dimers buckle in the same direction to form the C-defect. (c) C-defect due to a sublayer monovacancy. (d) Formation of a C-defect due to substitution a H atom with a sublayer Si atom. Taken from [51].

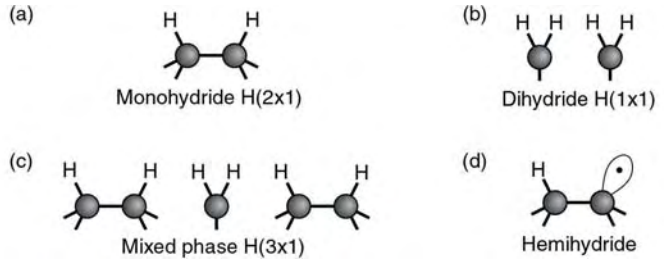

Figure 2.7: The different surface phases of H on Si(100). (a) Monohydride, (b) Dihydride, (c) H(3×1) phase and (d) Hemihydride. Taken from [51].

- **Dihydride**: two H atoms are bound to each Si atom by breaking both the intradimer σ and π bonds [Fig. 2.7 (b)].
- **H(3×1) phase**: this is an intermediate phase originating from mixing of monohydrides and dihydrides [Fig. 2.7 (c)].
- **Hemihydride**: one H atom attaches to only one Si atom of the dimer at very low H coverage [Fig. 2.7 (d)].

The monohydride phase is the predominant hydrogenated surface configuration used for STM-based hydrogen desorption lithography. A monolayer coverage can be formed by exposure to atomic hydrogen (usually created by passing molecular hydrogen through a hot W filament) at an elevated sample temperature of about 600 K. The H atoms prevent intradimer charge transfer which induces dynamic dimer buckling as predicted by Chadi [54]. It is thus a true, static representation of the 2×1 reconstruction. The Si(100) monohydride surface is chemically inert and commonly referred to

as the *H-terminated* or *H-passivated* Si(100) surface.

2.4.4 Selective adsorption of gaseous species using STM lithography

The chemical stability of the monohyride phase makes it a suitable resist layer, blocking the reactivity of the surface, and forming the basis of STM-based hydrogen lithography. STM lithography on the Si(100) surface, resulting in the desorption of H atoms from the surface, was first reported by Lyding, Shen and Tucker [11] in 1995. The underlying Si surface, exposed by STM-based desorption of hydrogen atoms, have since been used as reaction sites for the placement of a large variety of adsorbates such as Ag [16], Al [14], Co [65], Ga [15], NH_3 [13], O_2 [11] and PH_3 [19]. The selective adsorption of PH_3 molecules and the subsequent P atom incorporation from the PH_3 molecule into the top layer of the silicon surface are key steps for the fabrication of STM-patterned, highly P-doped devices in silicon presented in this thesis and will therefore be discussed in detail in Chapter 4.

2.4.5 Thermal desorption of hydrogen from the Si(100) surface

In our group, we have also extensively studied the thermal removal of the monohydride resist [66], [67] due to its adverse effect on subsequent low temperature Si growth quality used for device encapsulation. Atomic hydrogen is found to pair up with another hydrogen on the surface before it can desorb as H_2 [68]. As the density of hydrogen decreases during this thermal desorption process, it becomes increasingly difficult for a single H atom to find a desorption partner whilst diffusing on the Si(100) at the optimised hydrogen desorption temperature of $\sim$470 °C [67]. This leads to the formation of hemihydrides on the surface. A ball and stick model of a hemihydride is shown in Fig. 2.7 (d). Due to the asymmetric bonding nature of the hemihydride, where one H atom is located on one atom with an unsaturated, dangling bond on the other Si atom, the hemihydride is found to induce static buckling on the bare Si(100) surface which leads to a zig-zag appearance as observed in the STM. The hemi-hydride is very similar in appearance to the Si:P heterodimer and thus the two different surface features can only be distinguished using STM-based bias spectroscopy [69].

2.5 Electronic transport in mesoscopic systems

In the following section, the basic electrical transport concepts of two-dimensional (2D) mesoscopic systems are presented. The fabrication of Si:P nanostructures using STM together with the ex-situ alignment of ohmic contacts developed in this thesis has opened up the possibility to electrically characterise STM-fabricated Si:P devices using a conventional dilution refrigerator, thus allowing measurements at low temperatures and high magnetic fields.

The physical concepts relevant to the electrical measurements performed during the course of this thesis will be discussed. *Hall measurements* allow us to determine the carrier density of our samples at liquid helium temperatures. Temperature-dependent magnetotransport measurements enable us to determine the electron dephasing mechanism in our highly P-doped system. We investigate the limits of conduction in STM-patterned wires at the atomic-scale using both *weak* and *strong localisation* theory. Finally, we discuss the phenomenon of *Coulomb blockade*, one of the dominant transport mechanism through STM-defined Si:P island devices.

2.5.1 From classical Drude theory to Fermi liquid theory

The conductivity σ is the proportionality factor between the current density j arising from an the applied electric field **E**, i.e.

$$\mathbf{j} = \sigma \cdot \mathbf{E} \tag{2.12}$$

Ohm's law tell us that the conductance G is related to the measured current and the applied voltage as

$$I = R \cdot V = G \cdot V \tag{2.13}$$

From Eq. 2.12 and 2.13, it is easily seen that the conductance and the conductivity, in a 2D system, are related as:

$$G = \frac{w}{L}\sigma \tag{2.14}$$

for a conductor of width w and length L. The conductivity σ is therefore regarded as a bulk material property. The scaling given in 2.14 holds for large homogenous conductors but eventually breaks down when the device dimensions enter the mesoscopic regime.

Drude's achievement was to be able to relate the macroscopic quantity σ to the diffusive motions of the conduction electrons. In the classical picture, the presence of

an electric field causes electrons to drift diffusively through a crystal. The propagation speed is thereby limited by elastic (momentum conserving) as well as inelastic (momentum changing) scattering processes occurring at the characteristic time-scale τ. Therefore electrons drift with an average velocity $v_d = -\frac{\mu}{E}$, where μ is the electron mobility related to τ as $\mu = \frac{e\tau}{m}$. Making use of $j = nev$, one obtains

$$\sigma = en\mu = \frac{e^2 n\tau}{m} \tag{2.15}$$

In the Fermi-Liquid picture for non-interacting electrons the periodic potential, given by the crystal symmetry, gives rise to energy bands. Electrons in the conduction band are filled up to the Fermi energy E_F as given by the Fermi-Dirac distribution:

$$f(E - E_F) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \tag{2.16}$$

The quasi particle solution of the Schrödinger equation for electrons immersed in a periodic potential are Bloch waves which are essentially plane-waves modulated with the Fourier transform of the crystal potential. In the weak disorder limit electrons propagate freely through the crystal whilst undergoing elastic (momentum randomising processes) and inelastic (electron phase randomising processes) scattering with impurities (such as dopant ions), crystal lattice defects, phonons and other electrons. Only electrons near the Fermi energy E_F contribute to conduction, since electrons states below E_F - kT are filled up and have no states to move to as given by the Fermi-Dirac distribution [Eq. 2.16].

The Einstein relation connects the density of states at the Fermi level to the conductivity as

$$\sigma = e^2 \rho(E_F) D \tag{2.17}$$

where D is the diffusion constant.

2.5.2 Classical Hall effect and Quantum Hall effect

The classical Hall effect is useful for the determination of the carrier density of two dimensional systems. The basic principle underlying the Hall effect is the Lorentz force, which occurs for charged particles in the presence of a magnetic field. Electrons moving in an applied magnetic field experience a force perpendicular to the current direction which results in a transverse voltage, the *Hall voltage*. The Hall voltage depends on the magnetic field B, the applied current I, the electron charge q and the

sheet density n_s as:

$$U_{Hall} = \frac{B \cdot I}{q \cdot n_s} \tag{2.18}$$

or

$$R_{Hall} = \frac{B}{q \cdot n_s} \tag{2.19}$$

where R_{Hall} is the Hall resistance. Note that for a two dimensional system, the Hall resistance is equivalent to the Hall resistivity.

In a ballistic system, the presence of the magnetic field leads to the quantisation of energy levels, called *Landau levels* at low magnetic fields. The presence of Landau levels give rise to formation of plateaux in the Hall resistance manifesting the *quantum Hall effect*:

$$R_{QHE} = \frac{1}{g_s g_V} \frac{h}{e^2} \frac{1}{n} \tag{2.20}$$

where $g_{s,v}$ are the spin and valley degeneracy respectively, $\frac{h}{e^2}$ the resistance quantum and n the energy level quantum number. Due to the diffusive nature of electron transport in the devices structures discussed in this thesis, only the classical Hall effect is observed.

2.5.3 Mesoscopic transport regimes

For small conductors, Ohm's law and therefore the scaling between conductance and conductivity eventually breaks down as transport enters the mesoscopic regime. Mesoscopic objects are of intermediate size, larger than atoms or molecules but smaller than macroscopic, ohmic conductors. Conductors enter the mesoscopic transport regime when their device dimensions become comparable to three characteristic length scales:

- the electron's de Broglie wavelength, $\lambda = \frac{h}{p}$
- the electron's mean free path, l, defined as the distance between two elastic, momentum-randomising collisions
- the electron's phase coherence length, l_φ, defined as the distance between two inelastic, phase-randomising events

The value of these length scales is strongly dependent on parameters such as the device material, temperature and the magnetic field. It is the relative magnitude between l, l_φ and λ which defines different types of transport which is characterised as follows.

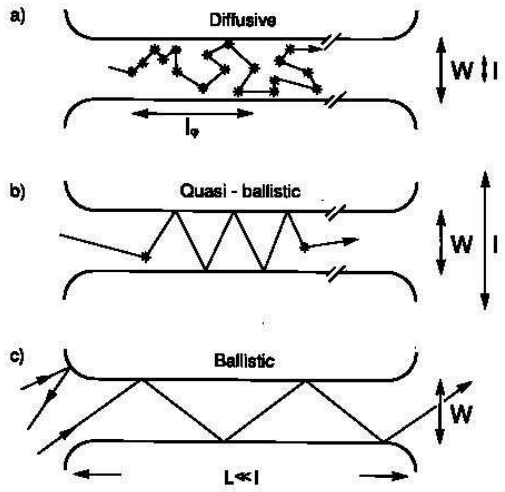

Figure 2.8: Electron trajectories in a) the diffusive, b) the quasi-ballistic and c) the ballistic regime. Taken from [70].

Based only on the mean free path and the width w and length L of the conductor, three transport regimes are identified as:

- *Ballistic*: for $l > L,\ w$
- *Quasi-ballistic*: for $w < l < L$
- *Diffusive*: for $l < L,\ w$

A conductor is called *ballistic* when the electron mean free path exceeds the sample dimensions $(l > w, L)$ and the electron wave travels without undergoing any scattering processes except for scattering at the conductor boundaries. As only the electrons near the Fermi energy contribute to conduction, the speed of the electrons in this case is defined by the Fermi velocity $v_F = \frac{\hbar k_F}{m^*}$. In this equation k_F is the Fermi wave vector and m^* is the effective mass.

In the presence of some degree of disorder, for example due to impurity atoms and lattice defects, the electron mean free path becomes shorter than the length of the conductor but still exceeds the width ($w < l < L$). This regime is called *quasi-ballistic*. For a highly disordered system, the scattering probability for electrons is very high translating into short mean free paths. If the electron's mean free path becomes shorter than the sample dimensions $(l < w, L)$ transport is *diffusive*. In the high temperature limit a diffusive conductor is well described by the classical Drude formula 2.14. However,

at low temperature, a variety of effects alter device transport and their contributions have to be added to the Drude conductance. The temperature-dependent electron phase coherence length, l_φ, is responsible for the occurrence of *weak localisation* which decreases device conductances below the Drude value. A further decrease in conductance is due to the *Coulomb interaction* of conduction electrons which is not included in the basic description of Fermi liquid theory. At lower temperatures, electrons can also become trapped in the presence of the disorder potential which leads to the effect of strong localisation. The effect of *strong localisation* also gives rise to the observation of *Coulomb blockade* behaviour in a double barrier island system.

If one or more device dimensions become comparable to the de Broglie wavelength, size effects causes electrons to become confined which results in energy level quantisation. Given a thermal energy kT much smaller than the energy level spacing, quantum wires and quantum dots are formed. A manifestation of this effect is the occurrence of *resonant tunnelling*, resulting in conductance peaks when the Fermi energy is aligned to an electron energy level given by the confinement.

The devices fabricated and electrically characterised in this work are highly P-doped Si:P systems with a typical doping/carrier density of $n = 1.7 \cdot 10^{14}$ cm^{-2}. Typical samples will have mean free paths in the range of $l \sim 2 - 10$ nm, phase coherence values l_φ of 15 – 150 nm depending on the measurement temperature and Fermi wavelengths between 2 – 3 nm. Hence, the devices reported in this thesis are clearly in the diffusive transport regime, where effects of weak localisation, electron-electron interactions, strong localisation and Coulomb blockade are important. For this reason, the continued discussion of these effects will focus on the diffusive regime.

2.6 Weak localisation

In the presence of scattering in a conductor, there is a finite probability for an electron to return to its point of origin. The backscattering probability is enhanced if no inelastic i.e. phase breaking processes occur along the backscattering trajectory. If this happens, the phase of the electron wave remains well defined, and the backscattering path of the electron interferes with its time-reversed equivalent resulting in an enhanced probability amplitude for the electron to be scattered back to the origin i.e. it is being weakly localised. In this section, we will follow the comprehensive derivation of weak localisation given in [70] and refrain from a discussion of the more involved

Green's function formalism. In light of Feynman's path integral description, the return probability of an electron is expressed as:

$$\begin{aligned} P(\mathbf{r}, \mathbf{r}{=}\mathbf{r'}, t) &= \sum_i \left| A_i^+ + A_i^- \right|^2 \\ &= \sum_i \left[\left| A_i^+ \right|^2 + \left| A_i^- \right|^2 + A_i^{+*} A_i^- + A_i^{-*} A_i^+ \right] \end{aligned} \tag{2.21}$$

A_i^+ and A_i^- are the amplitudes of a trajectory i and its time reversed equivalent respectively. The time-reversal invariance requires that both amplitudes are the same ($A_i^+ = A_i^- = A$). If an inelastic process occurs along the backscattering trajectory, the interference is destroyed and the interference terms in Eq. 2.21 vanish. In this case, the back-scattering probability of an electron is only $P = 2\sum_i |A_i|^2$. Without a phase-breaking process, the interference remains unscathed and there is an enhanced probability for an electron to return to its point of origin:

$$P(\mathbf{r}, \mathbf{r}, t) = 4 \sum_i |A_i|^2 \tag{2.22}$$

This phenomenon is called weak localisation. An applied magnetic field perpendicular to the loop gradually suppresses the time-reversal symmetry of the two interfering electron paths by adding a phase difference. This Aharonov-Bohm phase can be calculated by considering the canonian momentum $\mathbf{p} = m\mathbf{v} + e\mathbf{A}$ of an electron in a magnetic field where $\mathbf{A}$ is the vector potential $\mathbf{B} = \vec{\nabla} \times \mathbf{A}$.

$$\begin{aligned} \phi &= \frac{1}{\hbar} \oint_+ \mathbf{p}^+ d\mathbf{l} - \frac{1}{\hbar} \oint_- \mathbf{p}^- d\mathbf{l} \\ &= \frac{2e}{\hbar} \int (\vec{\nabla} \times \mathbf{A}) d\mathbf{S} = \frac{2eBS}{\hbar} = \frac{2S}{l_m^2} = 4\pi \frac{\Phi}{\Phi_0} \end{aligned} \tag{2.23}$$

The phase difference is twice the area enclosed by the back-scattering trajectory divided by the square of the magnetic length $l_m = \left(\frac{\hbar}{eB}\right)^{\frac{1}{2}}$ or 4π times the enclosed magnetic flux divided by the elementary flux quantum $\Phi_0 = h/e$.

In a two dimensional sample at zero magnetic field ($B = 0$), the coherence length l_φ determines the maximum size of coherent backscattering loops that can form since l_φ is the mean distance electrons travel without undergoing a phase randomising collision. A measure of the enclosed area of such an interference loop at zero magnetic field is given by $S = l_\phi^2$. However, in the presence of a perpendicular magnetic field, the constructive interference of loops bigger than the square of the magnetic length l_m is destroyed, since the time-reversed paths pick up a phase difference of $\phi \cong 1$.

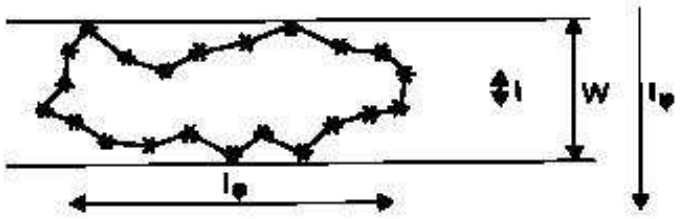

Figure 2.9: Dimensional crossover for $l_\varphi > w$ in a diffusive conductor. The sample geometry determines the maximum size of enclosed electron trajectories [70].

Therefore, for magnetic field values exceeding a critical value ($B > B_C = \frac{\hbar}{2eB\tau_\varphi}$), the maximum size of interfering loops is defined by the magnetic length l_m. For this reason, a characteristic signature of weak localisation is a negative magnetoresistance as a function of the applied, perpendicular magnetic field. The electron phase coherence length is found to increase with decreasing temperature. This leads to a more pronounced peak in the negative magnetoresistance around zero magnetic field since a larger value of l_φ increases both, the size and number of phase coherent loops which can be formed.

2.6.1 Dimensionality of weak localisation

The dimensionality of the weak localisation effect is determined by the relation between the coherence length and the sample size. If l_φ is smaller than the sample width and length ($l_\varphi < w, L$), electrons do not *see* their confinement and the weak localisation correction is essentially two-dimensional. If the coherence length exceeds the sample width $l_\varphi > w$, the sample boundaries constrict the maximum size and shape of the backscattering loops (see Fig. 2.9) since only loops with an area $S = l_\varphi \cdot w$ are formed. In this case the weak localisation effect is said to be one-dimensional.

2.6.2 Crossover from 1D to 2D weak localisation in a magnetic field

In the presence of a magnetic field, another length scale, the magnetic length, also dictates the dimensionality of weak localisation. The maximum size of a constructively interference loop at a certain magnetic field is given by $S = l_m^2$. Therefore, if the magnetic length approaches the width w with increasing magnitude of the magnetic field, the maximum size of constructively interfering loops is no longer constraint by w but by l_m. Therefore, if the phase coherence length is larger than w, a crossover from 1D

to 2D weak localisation occurs if $2l_m \sim w$ at the crossover field

$$B_{1D\rightarrow 2D} = \frac{4\hbar}{ew^2} \tag{2.24}$$

2.6.3 Weak localisation in two dimensions

Weak localisation manifests itself in an increase of the sample resistance at low temperatures. Application of a magnetic field gradually suppresses the weak localisation effect leading to a negative magnetoresistance. There have been several methods to account for the conductance correction stemming from weak localisation. Historically, Hikami *et al.* [71] derived a method within the framework of renormalisation group theory which is only valid in the diffusive regime. Since then, several methods have been developed to extend the description of weak localisation beyond the diffusive regime. Kawabata [72] provided the first method beyond the diffusive limit using Green's function formalism. Wittman [73] formulated a method based on the scaling of the momentum scattering length l. Zduniak [74] expanded Kawabata's model to include spin-orbit effects, whereas most recently, Dmitriev [75] included phase coherent nonbackscattering effects. Since our samples are in the highly diffusive regime, we use Hikami's method for the description of 2D weak localisation in this work. The validity of Hikami's method given for fitting the magnetoresistance data in the magnetic field range below a critical field B_0, given by:

$$B_0 = \frac{\hbar}{2el^2} \tag{2.25}$$

for the mean free paths of $l \sim 2$ – 10 nm, we get a value for B_0 ranging from 3 – 80 T. In this thesis, magnetoconductance ensure that we are well within the validity of Hikami's model. The expression derived by Hikami *et al.* [71] for the magnetic field dependence of the conductance correction in a highly disordered system due to weak localisation in two dimensions is expressed by:

$$\Delta G(B) = \frac{w}{L} g_s g_v \frac{e^2}{4\pi^2\hbar} \left[\Psi\left(\frac{1}{2} + \frac{\tau_B}{2\tau_\varphi}\right) - \Psi\left(\frac{1}{2} + \frac{\tau_B}{2\tau}\right) + \ln\left(\frac{\tau_\varphi}{\tau}\right) \right] \tag{2.26}$$

In this formula L and w are the sample dimensions, $g_{s,v}$ are the spin and valley degeneracy respectively, τ and τ_φ the elastic and the inelastic scattering times and $\tau_B = \frac{\hbar}{2eBD}$ is determined by the magnetic length $l_m^2 = D\tau_B$. The Hikami expression for two-dimensional weak localisation is also expressed as:

$$\sigma(B) = \sigma_0 - \frac{e^2}{\pi h} \left[\Psi\left(\frac{1}{2} + \frac{B_0}{B}\right) - \Psi\left(\frac{1}{2} + \frac{B_\phi}{B}\right) \right] \tag{2.27}$$

where σ_0 is the Drude conductivity. At zero magnetic field, the latter expression for the weak localisation is simplified using the asymptotic behaviour of the digamma function. For $B \to 0$ the arguments of the digamma functions $\Psi(x)$ diverge to infinity. Using the approximation $\Psi(x) \approx \ln(x - \frac{1}{x})$, Eq. 2.27 simplifies to:

$$\Delta\sigma(B=0) = \sigma - \sigma_0 = -g_s g_v \frac{e^2}{4\pi^2\hbar} \cdot ln\frac{\tau_\varphi}{\tau} \tag{2.28}$$

The weak localisation correction to the conductivity in 2D has a logarithmic dependence on the dephasing time, i.e. $\Delta\sigma \sim ln\tau_\varphi$.

2.6.4 Weak localisation in one dimension

The conductance correction due to weak localisation in 1D has been described by Altshuler *et al.* [76] for a wire of width w with a rectangular cross section.

$$\delta G_{loc}(B) = -g_s g_v \frac{e^2}{hL} \left(\frac{1}{L_\phi^2} + \frac{e^2 B^2 w^2}{3\hbar^2} \right)^{-1/2} \tag{2.29}$$

From the latter expression, the zero-field conductance correction in 1D is given by:

$$\delta G_{loc}(B=0) = -g_s g_v \frac{e^2}{hL} l_\varphi \tag{2.30}$$

which is directly proportional to the coherence length l_φ.

2.6.5 Dephasing mechanisms

Since l_φ is the only temperature dependent parameter in Eq. 2.28 and 2.30, the functional form of the conductance/resistance at low temperatures follows the temperature dependence of l_φ. The phase coherence length and the inelastic scattering time are related via the diffusion constant as $\tau_\varphi = \frac{l_\varphi^2}{D}$. The dephasing mechanism of a system can be extracted from the temperature dependence of the dephasing time. Dephasing mechanism are typically approximated by a power law i.e. $l_\varphi \propto T^{-p}$. Extracting the exponent p from temperature-dependent conductance measurements therefore provide a way to identify the dominant dephasing mechanism of a sample.

2.6.6 Dephasing mechanisms in 1D

There are several mechanisms which cause phase randomisation therefore limiting the coherence length. Inelastic and quasi-elastic collisions of conduction electrons with

phonons or electrons or spin-orbit scattering are the major intrinsic dephasing mechanisms. It is generally agreed that all intrinsic causes of dephasing such as electron-phonon scattering and inelastic electron-electron scattering should freeze out as $T \rightarrow 0$ leading to an infinitely large l_φ. However, extrinsic effects like electromagnetic noise or dilute magnetic impurities can cause a non vanishing dephasing at very low temperatures leading to a saturation of l_φ as $T \rightarrow 0$ [77]. In the following, we will briefly describe the mains dephasing mechanism relevant for a 1D disordered system [78].

Nyquist dephasing At low temperatures Nyquist dephasing [79] is believed to be the dominant dephasing mechanism in disordered quasi one-dimensional systems. Nyquist noise arises from scattering of conduction electrons with a fluctuating electromagnetic field produced by the other electrons in the conductor. Altshuler *et al.* [79] showed that the inelastic scattering time τ_φ of this dephasing mechanism in 1D has a temperature dependence of $\propto T^{-2/3}$. The corresponding coherence length is expressed as:

$$l_\varphi = \left(\frac{DG_0\hbar^2 L}{\sqrt{2}e^2 k_B T} \right)^{1/3} \tag{2.31}$$

Electron-electron scattering with large energy transfers: Whereas Nyquist dephasing is the dominant phase breaking mechanism in the regime $k_B T\tau_\phi/\hbar \gg 1$, the sample may leave this regime if the temperature is lowered further. Another dephasing mechanism was proposed [80] which becomes relevant when inelastic electron-electron scattering with large energy transfers, due to screened Coulomb interactions, is dominant. The underlying theory was described by Fukuyama and Abrahams [80]. They found that in the disordered metal limit $k_B T\tau < \hbar$ of a two dimensional system (2D here refers to the effective density of states), the dephasing time is given by:

$$\frac{1}{\tau_\varphi} = \frac{k_B T}{2E_F\tau} ln \frac{T_1}{T} T_1 = 4(E_F\tau)^2 D(2me^2)^2 \tag{2.32}$$

In a thin wire, Abrahams *et al.* reported [81], the temperature dependence of the inelastic scattering time becomes $\tau_\varphi \propto T^{-\frac{1}{2}}$, which results in a $l_\varphi \propto T^{-\frac{1}{4}}$ law for the electron phase coherence length.

Two-level tunnelling modes: Thouless [82] reported a temperature dependence of $T^{-\frac{1}{2}}$ for the electron phase coherence length in quasi one-dimensional disordered

Dephasing mechanism	Temperature dependence
Nyquist phase-breaking 2D	$T^{-1/2}$
Nyquist phase-breaking 1D	$T^{-1/3}$
electron-electron (large energy transfers)	$T^{-1/4}$
two-level systems	$T^{-1/2}$
electron-phonon	T^{-1} to T^{-2}

Table 2.1: Different phase-breaking mechanisms for quasi 2D and 1D samples in the disordered metal limit and the corresponding temperature dependence of the coherence length l_φ.

metal samples based on two-level tunnelling modes. Black *et al.* [83] suggested that this dephasing mechanism should be dominant at low temperatures in a disordered quasi 1D sample.

Electron-phonon scattering: Electron-phonon scattering is expected to play a minor role at lower temperatures as phonons are expected to freeze out with decreasing temperature. At temperatures of ∼10 K, however, electron-phonon scattering in a dirty metal may become dominant over other dephasing mechanisms. Dephasing due to electron-phonon scattering was theoretically predicted [84], [85] to follow a power law $l_\varphi \propto T^{-\frac{p}{2}}$ where p takes the values 2, 3, 4 irrespective of sample dimensionality but depending on the degree of disorder in the sample. The degree of disorder is thereby measured by the value $q_T l$ which is the ratio between the electron mean free path l and the thermal phonon wave length $\lambda_{ph} = \frac{2\pi}{q_T}$. If $q_T l \gg 1$ (l is much bigger than λ_{ph}) the sample is in the low disorder regime (p=3) while $q_T l \ll 1$ (l is much smaller than λ_{ph}) represents the high disorder regime (p=4). Experimentally, a power law dependence of p = 2 has been observed by many groups [86], [87], [88], [89], [90]. This unexpected value was suggested to occur in samples with an intermediate level of disorder, where $q_T l \approx 1$ [78].

Extrinsic dephasing mechanisms and saturation of l_φ: In addition to intrinsic mechanisms of dephasing (i.e. due to physical processes inside the sample), extrinsic effects (i.e. measurement related) can also cause dephasing which may lead to saturation of the electron phase coherence length. The most important causes of extrinsic dephasing are Joule heating or dephasing due to external high-frequency electromagnetic noise or scattering of the conduction electrons with magnetic impurities.

However at very low temperatures, another intrinsic reason for saturation of l_φ is the crossover from the weak localisation regime into the strong localisation regime as predicted by scaling theory [91], [92]. This crossover occurs generally at very low temperatures, when the coherence length reaches the dimension of localised electron states in the sample. An introduction into strong localisation is given in Section 6.4.11.

2.6.7 Electron-electron interactions

An additional quantum correction to the zero-field conductivity is caused by Coulomb interactions of the conduction electrons which is not included in the Fermi-liquid theory of non-interacting electrons. Expressions for this correction for effective one- and two-dimensional systems have been calculated by Altshuler *et al.* [93] and can also be found in Beenakker and van Houten [70].

$$\delta\sigma_{ee,2D} = -\frac{e^2}{2\pi^2\hbar} \cdot g_{2D} ln \frac{\tau_T}{\tau} \tag{2.33}$$

$$\delta\sigma_{ee,1D} = -\frac{e^2}{\sqrt{2}\pi\hbar} \cdot g_{1D} \frac{l_T}{W} \tag{2.34}$$

where g_{1D}, g_{2D} are effective Coulomb interaction parameters which, under typical experimental conditions, are of the order of unity [70]. The effective dimensionality of the interaction correction is determined by the relation between the thermal length $l_T = (\frac{D\hbar}{k_B T})^{\frac{1}{2}}$ and the wire width in the same way as l_φ determines the effective dimensionality in the weak localisation phenomenon. τ_T is correlated to the thermal length $l_T = \sqrt{D\tau_T}$. The change in resistance due to electron-electron interaction is only weakly dependent on the magnetic field in contrast to weak localisation [70]. Therefore it is possible in principle to separate out the effect of electron-electron interaction and weak localisation using magnetotransport measurements. Since both, weak localisation and electron-electron interaction effects independently influence conductance, the combined contribution [94] may be expressed as a linear superposition i.e. $\Delta G_{WL+ee} = \delta G_{WL} + \delta G_{ee}$.

2.7 Strong localisation

By lowering either the carrier-density or the temperature in a diffusive 1D or 2D sample, one may eventually leave the weak localisation regime and enter the strongly

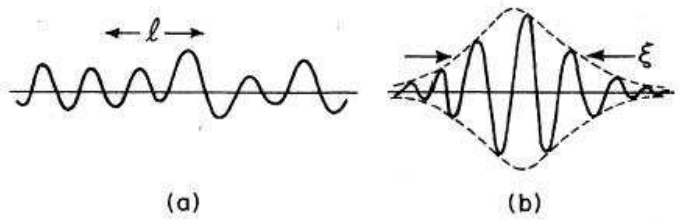

Figure 2.10: Typical electron wave functions: (a) extended electron state and (b) localised electron state with an exponential envelope of the wave function. $\xi = l_\varphi$ is the localisation length.

localised regime. Fig. 2.10 shows the typical electron wave function for both, the conducting (extended state) as well as the localised regime. In the localised regime, the electron becomes trapped in its surrounding potential and its spatial extend is reduced to the localisation length ξ. The crossover point from weak to strong localisation is expected to occur at low temperatures when the temperature-dependent coherence length l_φ becomes comparable to the localisation length ξ, i.e. $l_\varphi \simeq \xi$. The characteristic signature of strong localisation is an exponential rise of the resistance. It has been shown [95],[94], that in a one dimensional system in the presence of the smallest amount of disorder all electron states are eventually localised within a length ξ equal to a wire with a resistance of one resistance quantum $h/e^2 = 25.8\ k\Omega$. The mode of conduction is no longer dominated by a diffuse motion of the conduction electrons, but instead by electrons hopping from one localised state to the next. Hopping thereby can only occur if electron wave functions of two localised states with a similar eigen energy overlap.

Depending on the proximity of different localised states, electrons not only hop to the closest localised site (nearest neighbour hopping NNH) but may also reach sites further away (variable range hopping VRH). The resistance as a function of temperature caused by VRH hopping conduction is shown [96] to be an exponential power law with a cut-off temperature T_0 where T_0 plays the role of the crossover temperature:

$$R(T)_{VRH} = R_0 \cdot e^{(\frac{T_0}{T})^\mu} \tag{2.35}$$

The exponent $\mu = \frac{1}{d+1}$ with the dimensionality d is determined by the relation between the sample width w and the most probable hopping distance $R_0 = (4\alpha N_1 k_B T)^{-\frac{1}{2}}$ as defined by Mott [95] where the 1D DOS $N_1 = wN_2$ is proportional to the 2D DOS

and $\alpha = \xi/2$ is the decay length of the localised wave function.

As a consequence, by reducing the sample width w below the Mott's most probable hopping distance R_0 a crossover from two dimensional ($\mu = \frac{1}{3}$) to 1D variable range hopping conduction ($\mu = \frac{1}{2}$) would be expected and was experimentally confirmed in Si inversion layers by Fowler *et al.* [97].

2.8 Coulomb blockade

So far, we have only considered conduction systems such as wires. However, another interesting type of device is formed when the device dimensions are further constraint to small islands. These islands or dots are typically connected to source-drain leads via tunnelling junctions for charge transfer. The resulting change in the electrostatic potential from adding an additional electron onto the island/dot may result in a gap in the energy spectrum at the Fermi energy leading to the phenomenon of Coulomb blockade. A comprehensive review of the underlying physical concepts is given for example by Ferry and Goodnick [98]. The occurrence of Coulomb blockade behaviour is closely tied in with the effect of strong localisation. The Coulomb blockade model requires that the number N of localised electrons on an island and the average number of electrons <N> on the island satisfies the following inequality:

$$|N - < N > |^2 << 1 \tag{2.36}$$

This means that the tunnelling barriers next to the island must be sufficiently high in order to allow electrons to be localised. The minimum tunnelling resistance R_T that suffices this conditions is derived from the energy-time uncertainty relation [99], i.e.

$$\Delta E \cdot \Delta\tau \sim h \tag{2.37}$$

The characteristic time for charge fluctuations is $\Delta\tau = R_T \cdot C$. The energy gap associated with charging of a single electron is $\Delta E = \frac{e^2}{C}$. Plugging these two equations into Eq. 2.36 yields:

$$R_T \succeq \frac{h}{e^2} = 25.8\, k\Omega \tag{2.38}$$

Therefore, single electron charging effects occurs if the tunnel resistance is larger than the resistance quantum. The energy equation of a double barrier island system is given by:

$$E(N) = \frac{e^2}{2C}\left((N - ℵ)^2 - ℵ^2\right) \tag{2.39}$$

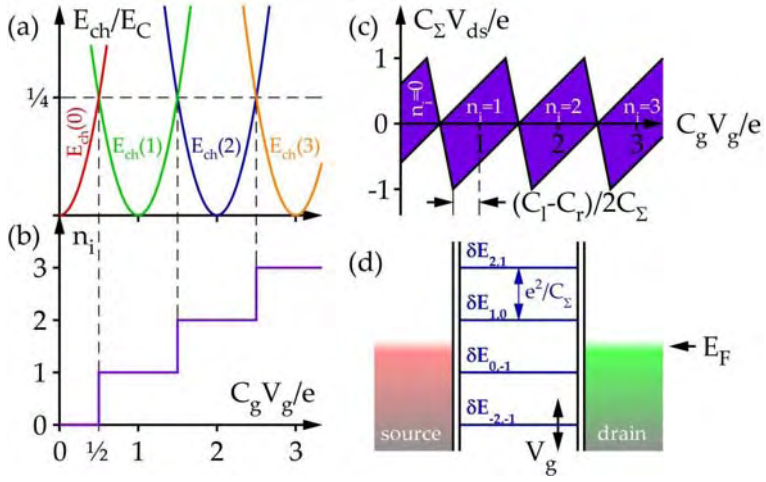

Figure 2.11: Schematic diagram illustrating the origin of Coulomb blockade behaviour. (a,b) Charge transfer occurs when the energies E(N) and E(N+1) are degenerate. (c) Variation of V_{sd} and V_{gate} leads to the well known *Honeycomb* diagram. (d) Energy spacing due to single electron charging. Taken from [100].

where N is an integer referring to the number of electrons on the island and ℵ is the fractional charge induced by the gate. By applying a gate voltage the electrostatic potential of the island system can be changed, thereby shifting the energy levels associated to different numbers on the dot as shown in Fig. 2.11 (d). The potential energy E(N) is minimised if the discrete charging characteristics of the island coincides with the continuous charging characteristic of the gate:

$$\frac{dE(N)}{dN} \doteq 0 \Leftrightarrow N = ℵ \rightarrow E(N) = -\frac{Ne^2}{2C} \tag{2.40}$$

From Fig. 2.11 (a,b) it can be seen, that charge transport from the leads through the island occurs, when the energies for N electrons coincides with the energy for (N+1) on the island. These degeneracy points can be regarded at the crossover point in the energy diagram shown in Fig. 2.11 (a,b). By increasing the gate, more and more electrons can be shifted onto the island at the respective degeneracy points. In between the degeneracy points, no conduction occurs thus the name Coulomb blockade. The continuous variation of the gate therefore leads to the formation of an oscillatory conductance structure known as Coulomb blockade oscillations. The conduction through the island is thereby quantised in equidistant steps of $\frac{e^2}{2C}$. The associated gate voltages between two successive energy minima are given by

$$E(N+1) \doteq E(N) \Longleftrightarrow V_g = \frac{(N+\frac{1}{2})e}{C_g} \tag{2.41}$$

The variation of the gate voltage as well as the source-drain bias lead to the observation of Coulomb blockade oscillations. Fig. 2.11 (c) shows a phase diagram containing the effect of both, the source-drain bias and the gate voltages. Such a representation is called *Honeycomb* diagram or *stability* plot and is useful for the extraction of device capacitances and charging energies. A more device-specific analysis of the Coulomb blockade effect will be given in Chapter 8.

In this chapter, we have given an overview of some of the key theoretical concepts required for understanding subsequent experimental results. In the next chapter, some of the experimental methods and key features of the equipment used to obtain the results in this thesis are described.

Chapter 3

Experimental methods

A brief overview is presented describing the various experimental techniques utilised in this thesis. These include state-of-the-art ultra-high vacuum techniques, cleanroom processing and low temperature electrical characterisation tools which are used for the fabrication and measurement of STM-based devices in silicon. At the core stands a customised UHV imaging and growth system that combines a scanning tunnelling microscope (STM) with a scanning electron microscope (SEM) and molecular beam epitaxy (MBE). Sample processing prior and after introduction into the STM-SEM/MBE system is carried out at the Semiconductor Nanofabrication Facility (SNF) at UNSW, which is a complete optical and electron beam lithography laboratory housed in a class 3.5 clean room. Using the cryogenic measurement facilities provided by the National Magnet Laboratory (NML), STM-fabricated Si:P devices are initially characterised using a 4 K liquid helium dip station. Finally, fully functional devices are further characterised at lower temperatures down to 100 mK using a ^{3}He/^{4}He dilution refrigerator. Whereas this chapter serves as a introduction into the experimental equipment and techniques which were used in this work, a detailed description of the device fabrication process is given in Chapter 4.

3.1 Description of the STM-SEM/MBE system

In this section we describe the unique features of the custom-designed UHV STM-SEM/MBE system manufactured in collaboration with Omicron Nano Technology GmbH, installed at the Atomic Fabrication Facility (AFF) at UNSW in September 2002. The following list summarises the crucial design features of this system which will subsequently be described in more detail.

- A combined scanning electron microscope (SEM) with the same focal point as a scanning tunnelling microscope (STM) system designed for UHV conditions.
- Optical positioning readout that allows precise relative and absolute STM stage positioning with respect to the STM tip with an accuracy of $\sim$10 nm.
- A high-voltage electron beam heater for high temperature preparation of large sample size ($\sim$1 cm^2).
- High-level of vibrational isolation between MBE chamber and STM-SEM chamber for atomic resolution STM imaging.
- A hydrogen cracker for STM-based hydrogen resist lithography.
- A phosphine (PH_3) microdosing unit for controlled, self-terminating molecular surface chemisorption.
- A UHV sample transfer mechanism between MBE chamber and STM-SEM chamber.
- A liquid nitrogen cryoshrouded molecular beam epitaxy chamber capable of growing device quality Si and SiGe layers on industry size 4″ wafers and 1 cm^2 large samples used for STM device fabrication.

Fig. 3.1 shows a schematic overview of the UHV STM-SEM/MBE system. A series of digital photographs which capture the entire system across two rooms of our laboratory is shown in Fig. 3.2 (a-e). The MBE system consists of a growth chamber, a buffer chamber and a load lock for sample loading shown in Fig. 3.2 (d). It is equipped with a permanent liquid nitrogen cryoshroud system to minimise background impurity levels during Si growth and to maintain the background vacuum base pressure in the 10^{-11} mbar region. A Si e-beam evaporator source is used for the growth of atomically controlled, high quality encapsulation of P-doped nanostructures fabricated by STM with growth rates between 0.5 – 2 $\frac{\mathring{A}}{s}$. For the encapsulation of devices by epitaxial silicon using the MBE system, it has been designed to accommodate both 4″ wafers for large-scale production and 1$\times$1 cm^2 samples on a specially designed 4″ wafer holder. The 1$\times$1 cm^2 samples can subsequently be transferred to the STM-SEM system for atomic-scale imaging. Such large sample sizes (1$\times$1 cm^2) for STM imaging are necessary to be compatible with pre- and post-processing techniques in a cleanroom environment such as optical or electron beam lithography. A photograph of a

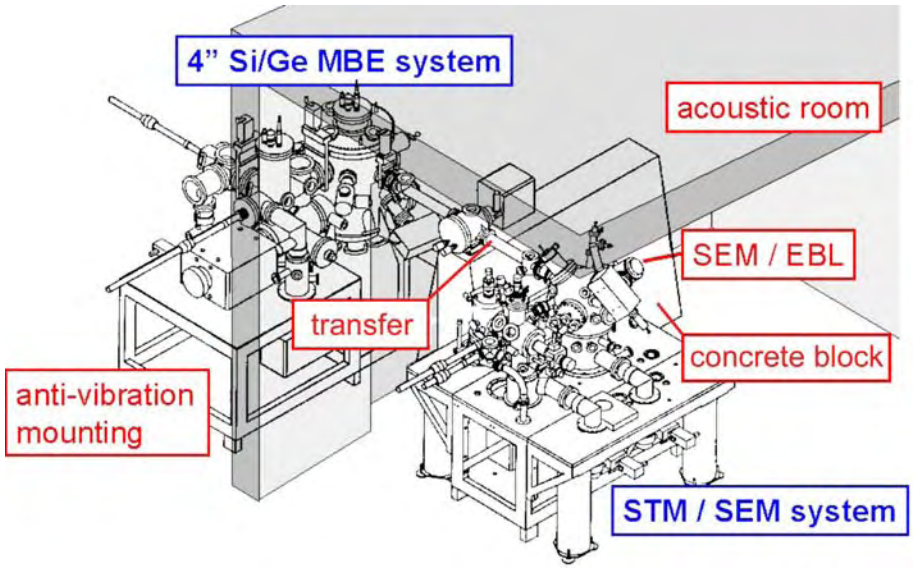

Figure 3.1: A schematic overview of the custom-designed UHV STM-SEM/MBE system. The 4" SiGe MBE system, the combined STM-SEM chamber and the extreme antivibration measures are discussed in the text.

1×1 cm^2 large sample sitting in the transfer trolley, connecting the MBE chamber with the STM-SEM chamber, is shown in Fig. 3.3 – highlighting a unique sample holder design where Ta foils are used to clamp the Si substrate in place. To transfer samples between the STM-SEM and the MBE system, we use a cassetrack system designed by VG SCIENTA which is essentially a trolley system in which samples are transferred under vacuum pressures of $\sim 1 \cdot 10^{-9}$ mbar.

One of the challenges in combining MBE with atomic resolution STM is, that typically MBE systems require the permanent use of mechanical pumps, particularly during growth, to achieve the cleanest possible growth environment. This poses a detrimental source of vibrational noise for the operation of the STM. Therefore rigourous anti-vibrational measures have been taken to isolate the STM system from unwanted sources of noise needed to achieve atomic resolution STM imaging. Firstly the MBE system is located in a separate room sitting on a separate concrete foundation which extends 10 m into the ground. The UHV transfer tube, which houses the sample transfer mechanism and connects the two systems, sits on a large, 3 tonne concrete block to decouple the noise originating from the MBE system. Furthermore air-filled bellows are installed at the outer end of the UHV transfer tube to minimise vibrations transmitted along the stainless steel connection. Furthermore, the STM-SEM room has been

Figure 3.2: Combined STM-SEM/MBE system. (a) The MBE system (left) and the STM-SEM UHV (right) chamber are connected with a UHV sample transfer line. (b) STM-SEM system designed for atomic-scale STM device fabrication. (c) Manipulator arm in the preparation chamber of the STM-SEM system containing the electron-beam sample heater and the STM scanner transfer slot. (d) Si molecular beam epitaxy system for atomically controlled device encapsulation. (e) PH_3 microdosing system attached to the preparation chamber of the STM-SEM system.

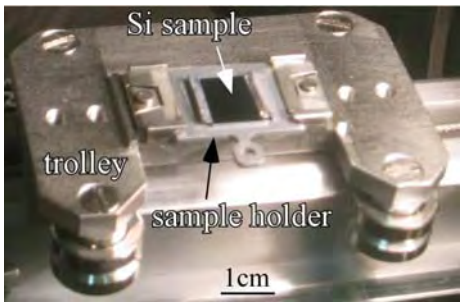

Figure 3.3: A 1 cm^2 Si sample in a custom-designed sample plate inside the UHV sample transfer system between SEM-STM and MBE system.

specially designed to damp acoustic vibrations from outside entering the laboratory, including acoustic walls, flooring, windows and ceiling. The entire STM-SEM system is floating on nitrogen-pressured airlegs which eliminates low frequency noise signals. For high frequency vibration isolation the STM stage itself is mounted on viton rings as sketched in Fig. 3.4 (b).

Fig. 3.2 (b) shows the STM-SEM system consisting of STM-SEM chamber and preparation chamber. The preparation chamber is connected to an entry lock for exchange of samples and STM scanners. High temperature sample preparation, hydrogen passivation, exposure to PH_3 and subsequent P atom incorporation is performed in the preparation chamber. By isolating these processes from the main STM chamber, a high quality vacuum in the 10^{-11} mbar range can be permanently maintained in the STM-SEM chamber.

The large sample size of 1×1 cm^2 makes it difficult to use direct current heating to achieve atomically flat surfaces. This is due to the high currents, exceeding the maximum current ($\sim$5 A) of electrical UHV feedthroughs, needed for such large samples. Therefore we heat the backside of the sample through a rectangular hole in the 1×1 cm^2 sample holder a using a Thorium coated electron beam filament [see Fig. 3.2 (c)] biased at 600 V with respect to the sample. The Th coating lowers the work function for electrons which are emitted at filament currents above $\sim$1.5 A and accelerated towards the backside of the sample under the high voltage. With this technique, we can reproducibly achieve sample temperatures in excess of 1200 °C across a 1×1 cm^2 sample at vacuum pressures $<5\cdot10^{-9}$ mbar.

We use a water-cooled hydrogen cracker GRZ40 made by MBE-Komponenten GmbH to chemically passivate the sample surface with a monolayer of atomic hy-

drogen. During the exposure to ∼140 Langmuir (L) of atomic hydrogen, the sample is heated by the electron beam heater at a temperature of ∼350 °C (as calibrated by an in-situ Pt/Ir thermocouple located on the manipulator arm). A beam of atomic hydrogen is generated by passing ultra-high purity H_2 gas through a ∼1800 °C hot tungsten filament thereby thermally separating the molecules to form an atomic beam of hydrogen. The hydrogenated Si surface is used as the resist for STM-based hydrogen lithography which forms the basis of STM device fabrication.

A PH_3 microdosing systems shown in 3.2 (e) is attached to the preparation chamber as well as the STM-SEM chamber. Double-containment tubes are pressure-monitored and connected to an alarm system for maximum safety in the event of a phosphine leak. Microdosing valves allow precise dose control of phosphine density by monitoring the background vacuum pressure in the chamber. Typically exposure of PH_3 gas to the surface at a chamber pressure of $1.1 \cdot 10^{-9}$ mbar for 15 min, corresponding to 0.74 Langmuir (L), results in a saturation dose of ($2.5{\cdot}10^{14}$ cm^{-2}) phosphine molecules adsorbed to the sample surface.

The preparation chamber is connected to the STM-SEM chamber via a standard Omicron transfer arm mechanism. Several combined STM-SEM setups have been described in the literature, see for example [101], [102]. While previous approaches were based on adding a STM system to an existing SEM system operated at high vacuum, the design of this system is aimed at a high performance of a combined STM-SEM **UHV** system [103]. UHV conditions are necessary to prevent sample contamination by cracking adsorbed molecules or residual gas from the chamber background, in particular hydrocarbons [104], by the electron beam of the SEM. It is also essential to have UHV for the creation of stable and clean Si surfaces for high resolution STM imaging. Previously, we have described that vibration damping is challenging when combining MBE with atomic resolution STM. In the case of a combined STM-SEM system, the demand is even more challenging. In current state-of-the-art STM systems, the STM stage is typically spring suspended with an eddy current damping system ensuring a high level of vibrational isolation. However, for a combined system, where the STM and the SEM have the same focal length, allowing simultaneous imaging operation, the STM stage has to be fixed with respect to the SEM column and eddy current damping cannot be utilised. As such a viton ring damping of the stage in conjunction with airleg damping are essential – even for systems without MBE.

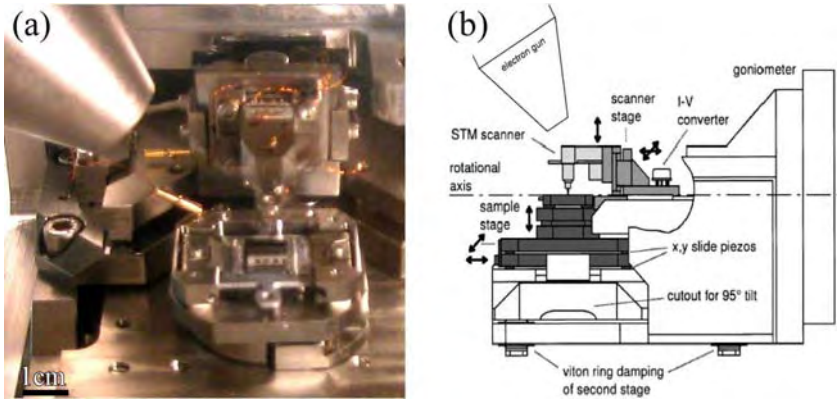

Figure 3.4: Sample stage inside the STM system. (a) Photograph of the STM stage with a 1×1 cm^2 sample and simultaneous SEM imaging. (b) Corresponding schematic of the stage showing essential design features.

Fig. 3.4 (a) shows a digital photograph of a 1 cm^2 large sample inside our STM system, the STM scanner and the electron gun. The crucial design considerations are sketched in Fig. 3.4 (b). The entire STM stage is mounted onto a goniometer, which allows us to tilt the stage from -30° to +90° relative to its horizontal position. The SEM column is fixed at a 30° angle with respect to the STM stage. The rotational axis coincides with the optical axis such that the focal point of the SEM is independent of stage rotation. The tilting angle is large enough to image and position the STM tip without significant tip image shadowing and, at the same time, is low enough to avoid image distortion in the SEM. The electron gun is operated at a beam energy of up to 25 keV with a spot size better than 20 nm. The electron current can be varied from 1 nA to 100 nA. The incident electrons generate secondary electrons which are detected and amplified by a positively biased channel electron multiplier (CEM). The STM stage sits on a viton ring damping system and consists of sample stage, scanner stage, optical positioning read-out, and on-stage tunnelling current I-V converter for low noise operation.

Sample movement is realised by a stack of three linear translation micro piezo slides with a travelling range of 10 mm in X and Y direction and 5 mm in the Z direction. Three shear piezos allow for the coarse positioning of the STM scanner relative to the sample with a range of $5\times12\times5$ mm^3. The STM scanner is fixed to the STM stage by a magnet and two guiding pins. The scanning range of the STM is about $6\times6\times1$ μm^3 for device fabrication depending slightly on the scanner piezo tube size and the length of the STM tip.

The optical positioning read-out provides a way of absolute and relative stage movement. It is mounted on the side of the STM stage and works similar to an optical mouse. Light from a laser diode is guided through a mask pattern and throws Moiré patterns onto an array of photodiodes. By counting the shift in the Moire rings induced by stage translation a precise relative movement with an accuracy of about 10 nm can be detected. The absolute positioning accuracy relative to the stage is below 100 nm. Since the sample positioning in the stage is not fixed, it is difficult to use the absolute position of the read-out for patterning. However, this technique can be used in conjunction with the registration markers developed in this work.

Typical UHV processing steps for a complete device takes about 10 h. During this time, we need to have good quality, stable STM imaging and accurate control over every device parameter such as sample temperature, STM lithography parameters, PH_3 dose and MBE growth rate. A complete calibration of the entire system takes $\sim$1 month before devices can be processed in UHV. Following this, the requirement of the STM tip to be stable for a long time means that a significant amount of devices are lost during STM imaging. Finally pre-processing of registration markers and post-processing of devices require a total of 6 – 7 days in the cleanroom. Devices can be literally described as *hand-made*. During the time of my thesis, the total device yield for functional devices has been about 30 %.

3.2 Cleanroom processing equipment

All pre- and post-processing steps presented in this work were performed at the Semiconductor Nanofabrication Facility (SNF) at UNSW. The SNF consists of a number of class 3.5 and class 350 cleanroom laboratories which house standard cleanroom facilities such as wet benches for chemical sample etching, cleaning and resist spinning, high temperature furnaces for thermal SiO_2 growth and metal evaporators for device contacts. They also include several optical lithography stations and two state-of-the-art FEI electron beam lithography stations.

The Quintel Q6000 optical aligner shown in Fig. 3.5 (a) uses a lithographic wavelength of 365 nm for mask pattern exposure, provided by a mercury lamp. It can be used in two mask-sample contact modes, the vacuum contact mode and the pressure contact mode. In the vacuum contact mode, the sample-mask contact is generated by creating a vacuum between them whereas in the pressure contact mode, the sample-

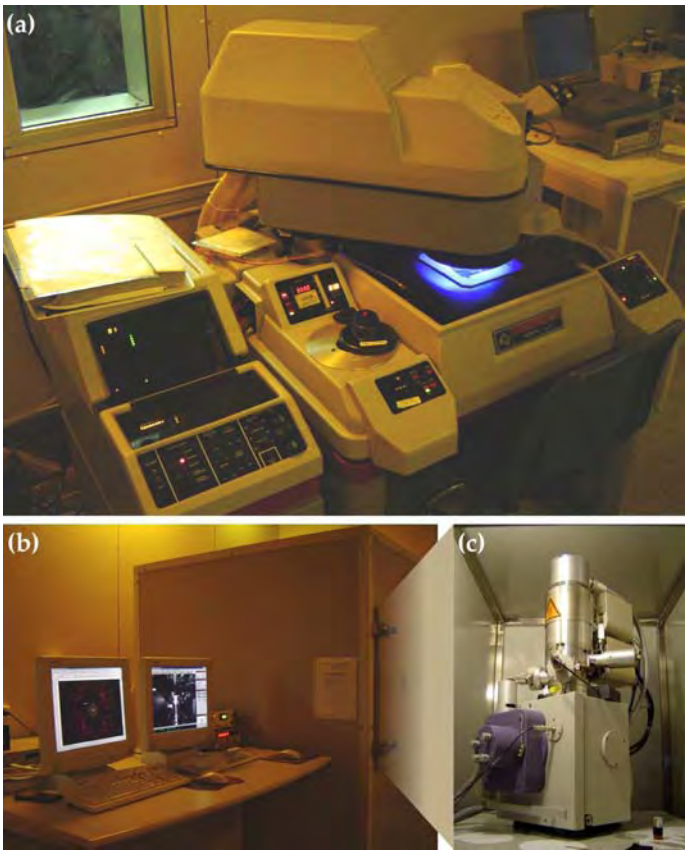

Figure 3.5: Lithography equipment inside the Semiconductor Nanofabrication Facility (SNF). (a) The Quintel Q6000 optical mask aligner. (b) FEI XL 30 control electronics and (c) electron beam lithography station inside electromagnetic shielding.

mask contact is achieved by pressing the sample onto the mask.

We use optical lithography for defining registration markers down to a size of 1 μm on Si device samples prior to introduction into the STM-SEM system. After UHV STM device fabrication, we align Al contacts to STM-fabricated Si:P devices by using the registration markers to indirectly relocate the buried Si:P structures.

The registration marker process was also transferred to be used in combination with electron beam lithography. The FEI EBL XL 30 is depicted in Fig. 3.5 (b,c). The actual electron gun is shielded against electromagnetic radiation. Using beam acceleration voltages of up to 30 kV and electron currents of order 50 pA, electron beam spot sizes $<$5 nm are achieved. The typical working distance between gun and sample is 5 mm. High resolution lithography is performed on organic resists such as PMMA. The exposure doses for the definition of registration markers with sizes down

to 200 nm range from 300 to 600 $\frac{\mu C}{cm^2}$.

The development of a complete UHV-compatible fabrication strategy is described in detail in Chapter 4. Full descriptions of processing parameters will be given there.

3.3 Low temperature electrical device characterisation

Electrical device characterisation generally takes places in two steps. First, a 4 K dip liquid helium dip station (Fig. 3.6) is used to check if the device is contacted. Initial device characterisations include determination of I-V behaviour, contact resistances and magnetotransport up to ± 2 Tesla. The temperature dependence of fully functional devices is subsequently measured using an Oxford Instruments Kelvinox K100 ^{3}He/^{4}He dilution refrigerator (Fig. 3.7).

3.3.1 4K dip station

Fig. 3.6 shows the 4 K liquid helium station. A 20 pin measurement loom (dip rig) is immersed into a liquid helium dewar for quick device characterisation. Both, a Keithley 2410 DC voltage source unit and a Keithley source measurement unit SMU 236 are used for measuring device I-V behaviour. Two Stanford Research Systems SRS SR830 lock-in amplifiers are used for AC measurements. The dip rig is equipped with a two Tesla superconducting magnet to perform Hall and magnetotransport measurements.

3.3.2 Dilution refrigerator

Temperature-dependent electrical device characterisation are carried out using an Oxford Instruments Kelvinox K100 ^{3}He/^{4}He dilution refrigerator equipped with an 8 Tesla perpendicular field, superconducting magnet. The underlying cooling principle for ^{3}He/^{4}He dilution refrigerators is based on the adiabatic dilution of the lighter ^{3}He isotope into the heavier ^{4}He isotope which form a phase boundary below temperatures of 800 mK. This phase boundary is located in the *mixing chamber*. The bottom of the mixing chamber is connected to a *heat still* which allows temperature regulation of the device sample. A closed-loop pumping system circulates the ^{3}He isotope from the still back to top of the mixing chamber. The ^{4}He *1 K pot* condenses the ^{3}He/^{4}He

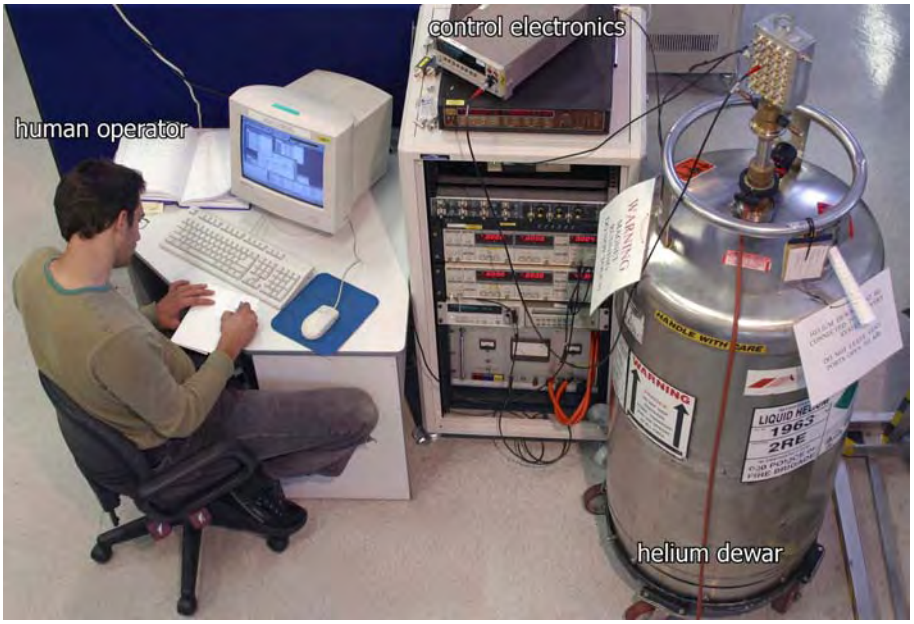

Figure 3.6: A 4 K liquid helium dip station inside the National Magnet Laboratory. The liquid helium dewar, low noise electronics and measurement computer are shown.

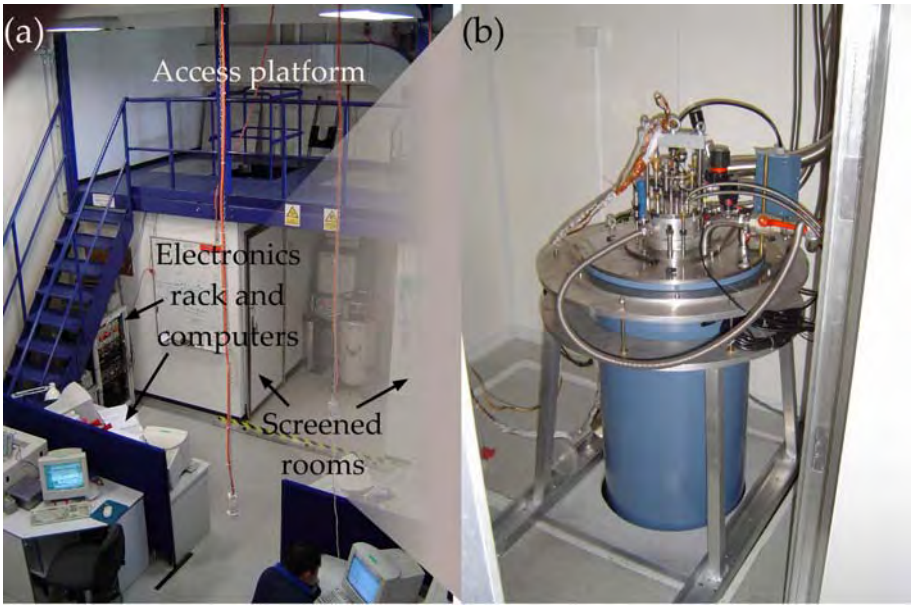

Figure 3.7: Dilution refrigerator setup inside the National Magnet Laboratory. (a) Photograph of a copper electromagnetic screening room housing an Oxford Instruments Kelvinox K100 dilution refrigerator equipped with a top-loading cryostat (b).

mixture providing a continuous flow of ^{3}He. A more detailed description on dilution refrigerators and low temperature measurement techniques is found in [105], [106].

The Kelvinox K100 is capable of cooling down to bath temperatures of about 100 mK. Samples are mounted on the end of a copper cold finger which is connected to the bottom of the mixing chamber. Fig. 3.7 (a,b) shows the Kelvinox K100 platform at the National Magnet Laboratory. Control electronics are located outside a fully enclosed, electromagnetic screening room which houses the actual cryostat. Sample loading and unloading occurs via top access from the upper platform. The setup is used in this thesis to perform temperature-dependent resistance, 2D and 1D weak localisation measurements. Descriptions of the device specific measurement set-ups are given in Chapters 4 – 8 respectively.

Chapter 4

Development of a complete strategy for UHV STM device fabrication

4.1 Introduction

The scanning tunnelling microscope is currently the only tool that allows manipulation of matter at the atomic level. With the aim of a continuing miniaturisation of electronic devices, it is therefore of interest to study the capability of atomic resolution STM for the fabrication of ultra-small devices [19], [24], [25], [26]. To achieve this, any device fabrication strategy must be UHV compatible in order to maintain the advantages of atomic resolution. For the realisation of robust, STM-patterned devices fabricated in UHV, it is also necessary to find a way to electrically contact such devices outside the UHV environment, so that we can perform low temperature measurements in high magnetic fields to characterise their electrical transport properties.

Since 1992, a tremendous research effort [107], [108], [109], [108], [109], [110], [111], [112], [113] has been undertaken to develop a fabrication process aimed at electrically contacting and characterising STM-patterned structures outside the ultra high vacuum environment. Atomically precise STM-patterned structures are very hard to relocate in vacuum and are generally invisible once removed from the UHV environment using standard ex-situ processing techniques. As a result, a successful fabrication process has to incorporate some form of surface pre-pattering technique at, or below, the micron scale to allow relocation of the STM-patterned structure. To date, several methods [28], [107], [109], [111], [114] have been tried, most of which rely on pre-patterning the substrate using metal. Other approaches utilise ion implantation [29] or registration markers etched into the substrate [108].

Whilst a multitude of different approaches have been reported in the literature,

reflecting the difficult task of aligning external macroscopic contacts to STM-fabricated devices, only a few reports [27], [28], [30], [31], [112], [113] of successful electrical measurements exist; two of which are the result of this thesis.

In this chapter, we describe the development of a complete process for the fabrication of planar phosphorus doped silicon devices patterned by STM using STM-based hydrogen lithography and phosphine (PH_3) as the dopant source. We demonstrate how we have used etched registration markers to electrically contact a planar STM-patterned, P-doped silicon device. Electrical measurements show that the complete fabrication scheme is a viable candidate for the fabrication of ultra-small devices in silicon towards the atomic scale. These results have been published in [30], [31] and highlighted by Science Magazine [Vol. 306, p1103 (2004)] and the Materials Today Magazine [Vol. 7, Issue 12, p18 (2004)].

In Section 4.2, we present a detailed overview of previous attempts to electrically contact STM-fabricated devices in silicon. Within this discussion we highlight the stringent requirements to maintain surface quality and achieve atomic resolution on Si(100) that any potential contacting strategy has to meet.

Section 4.3 describes the contacting scheme we have developed in this thesis to contact devices compatible with STM patterning Si at the atomic level. The scheme is based on etching pre-patterned marker structures using optical lithography into the silicon substrate that are subsequently used to relocate precisely positioned, STM-patterned dopant structures. We describe how the markers are compatible with a complete UHV process for the patterning of nano-scale devices. A study to determine the minimum size and etch depth of such registration markers suitable for relocation using our UHV scanning electron microscope is shown. This includes the behaviour of makers during high temperature sample preparation and encapsulation in epitaxial silicon.

Section 4.4 describes the key steps of our STM-based device scheme including STM lithography on a hydrogen resist layer, selective adsorption of PH_3, device encapsulation using silicon MBE and alignment of four terminal external macroscopic contacts patterned by optical lithography.

In Section 4.5, we present electrical results for the first STM-patterned device, a 4×4 μm^2 P dopant square. Comparison of I-V characteristics between a control device - not patterned by STM - and the square device demonstrate that we can contact STM-fabricated structures using this strategy. Our results show it is possible to use etched

registration markers in the silicon surface to align contacts to STM-patterned, buried P dopant devices. We perform four terminal measurements of buried STM-patterned dopant structures and show, that the STM can completely remove the hydrogen resist in the patterned areas and that ohmic conduction through the P dopant square originates from the buried P dopants.

The use of etched registration markers is potentially of much broader interest as it can be used generically as a means for both relocation and device fabrication of STM-patterned structures on the Si(100) surface which may consist of other adsorbates. Considering that our group has recently demonstrated the precise positioning of single P dopant atoms with nanometre precision [32], the fabrication scheme that is presented here shows great potential for the fabrication of STM-based devices on the atomic level.

4.2 Overview of strategies to contact STM devices

For the realisation of robust STM-patterned devices in Si, it is necessary to find a way to establish contact to these devices in order to perform electrical measurements.

Over the past 8 years, significant progress has been made in developing strategies for contacting STM-patterned nanostructures in silicon. Since individual STM-fabricated structures are hard to relocate once they are removed from the UHV environment, most contacting approaches reported in the literature rely on pre-patterning the initial silicon surface. The STM-designed structure is then positioned with respect to this pre-patterned contact or marker in such a way that the STM-fabricated device can be relocated and connected to the outside world.

To date, patterns have been defined using optical or electron beam lithography, followed by either metal deposition [28], [107], [108], [109], [111], [114], ion implantation [110], [115] or by etching the pattern into the silicon substrate [108]. Table 4.1 gives an overview over the main approaches to contact STM-patterned devices reported in the literature to date, their individual characteristics and the potential they have to perform electrical measurements. A critical factor in the choice of how the substrate is pre-patterned is that the method has to be compatible with UHV surface preparation techniques that allows clean surfaces with atomic resolution STM imaging. Pre-patterning the surface either by optical or electron beam lithography typically requires the use of an organic resist. It is necessary to completely remove any traces of

Registration markers	Reference	Comments
Pre-deposited metal		
W	[109]	Trench formation, C contamination
Pt		Incompatible with STM imaging
Co		Low thermal stability ($<$ 700 °C)
CrPt	[27],[107]	Requires low temperature preparation to 550 °C $NiSi_2$ wire: 100 nm $\times$ 1.45 μm; R_{4T} = 32 kΩ
Ti	[111],[114],[116]	Ti diffusion up to 500 nm after heating to 900 °C Trench formation around $TiSi_2$ electrodes
TiW	[28],[117]	Ag clustering forms 10-50 nm wide wires Non-ohmic behaviour $R_{4T} \sim$ 1-4 kΩ
In-situ deposition		
Au	[118]	SiN mechanical mask clamped to sample Incompatible with UHV sample annealing
Ion implantation		
As	[29], [113],[115]	Requires low temperature preparation to 700 °C STM lithography to form PH_3- dosed wire: 50 nm $\times$ 750 nm; R_{2T} = 337 kΩ
Diffused p-n junctions	[110]	STM nanolithography between p-n junction
Etched markers		
Etchant: KOH	[108]	UHV compatible markers etched into Si(100) Low thermal stability ($<$ 1000 °C)

Table 4.1: Summary of the main approaches for relocating and/or contacting STM-fabricated devices created in UHV. A detailed discussion is given in the text.

the resist before sample loading into the UHV system to avoid surface contamination. This requires good chemical resilience of patterned structures towards wet-chemical cleaning methods. Another crucial factor is thermal stability. Standard sample preparation methods to prepare atomically flat surfaces in UHV include a heating step to temperatures of about $\sim$1250 °C. Such high temperatures are necessary to melt the Si surface in order to generate a low-defect Si(100) 2×1 surface reconstruction and remove residues of carbon [119]. Carbon is known to induce strong pinning on the Si surface. Experimental studies and thermal stability simulations [61] have shown that the presence of C atoms increases surface roughness and induces surface reconstruction which hampers subsequent device fabrication. Therefore, the ability for patterned surfaces to survive this high temperatures required to remove C contamination plays a crucial role in the selection of possible materials used for pre-deposited metal patterns.

4.2.1 Metal markers

In the consideration of pre-patterned metal markers or contacts, let's first consider Table 4.2. Table 4.2 shows the melting points of commonly used materials for the fabrication of contacts in the microelectronics industry. Metals such as Au, Al, Ag, Ti-Au [120], CrAu [121] are incompatible to high temperature sample annealing due to their low melting points. Such metals have been shown to diffuse over the entire surface and even evaporate during annealing, thereby contaminating the surface and making it completely unusable for device fabrication. Whilst some metals exhibit melting points above the sample annealing temperature of $\sim$1250 °C, it has been shown that they are still subject to surface diffusion [114], [122] at elevated temperatures thereby smearing out the marker introducing surface contamination. Surface diffusion is a thermally activated process. The diffusion coefficient D is dependent on the activation energy E_{diff} and the pre-exponential factor D_0 with $D = D_0 \times e^{-\frac{E_{diff}}{kT}}$. In semiconductor systems with directional bonding [123], the most important property that affects the diffusion coefficient is the number of bonds that the adsorbate forms with the surface. This means that the diffusion mechanism is dependent not only on the semiconductor material but the diffusion coefficient depends also on the crystal surface direction on which it diffuses. To date specific diffusion coefficients of metals on the Si(100) surface are not well documented. However some diffusion studies of metals on Si(100) have been reported. For example, Wind *et al.* [124] considered Mn, Fe, Cr and Co unsuitable as contact material due to their high diffusivities. Indeed, a report

Name	**Symbol**	**Melting point [°C]**	UHV compatibility
Cobalt	Co	1495	UHV-compatible
Chromium	Cr	1857	
Iron	Fe	1535	
Manganese	Mn	1245	
Molybdenum	Mo	2617	
Nickel	Ni	1453	
Platinum	Pt	1772	
Silicon	Si	1410	
Tantalum	Ta	2996	
Titanium	Ti	1660	
Tungsten	W	3410	
Aluminium	Al	660	Not UHV-compatible
Arsenic	As	817	
Copper	Cu	1083	
Gallium	Ga	30	
Gold	Au	1064	
Indium	In	157	
Phosphorus	P	44	
Silver	Ag	962	

Table 4.2: Melting points of different materials commonly used in both, the semiconductor industry and the research environment. Only a few elements exhibit melting points above the standard silicon sample annealing temperature of ∼1200 °C.

on Co structures evaporated onto silicon shows that Co structures loose their lateral definition upon heating to temperatures above ∼500 °C [122]. A detailed study [114] has also been undertaken using Ti. After heating to 900 °C for 5 s, Ti was reported to diffuse up to 500 nm on the Si(100) surface. Despite wet-chemical sample cleaning with $NH_4OH : H_2O_2$, the presence of metal contamination was seen to damage and partially reconstruct the Si(100) surface [111]. For these reasons, research efforts using Ti have focused on the Si(111) surface where Ti diffusion was seen to be lesser i.e. ∼100 nm [114]. Additionally, surface cleanliness after wet-chemical cleaning with $H_2SO_4 : H_2O_2$ (SP) and $DI : HCl : H_2O_2$ (RCA-2) and UHV sample annealing appears cleaner on the atomic level [116]. Pt was observed [122] to be incompatible with atomic resolution imaging on the Si(100). For materials with high melting points, which preserve their structural shape during annealing, it was found that Si self-diffusion at elevated temperatures of ∼1200 $^{\circ}C$ causes surface reconstruction in the form of trench formation around deposited metal structures [28], [108], [111], [122]. Trench formation makes atomic-scale STM pattering difficult and may also adversely affect electrical device performance. Trench formation was reported when using Ti [111] and W [122] on the Si(100) surface. In the case of depositing W, Palasantzas *et al.* [122] employed the use of hydrogen plasma cleaning at a sample temperature of ∼450 °C in conjunction with a SiO_2 mask layer to reduce organic contamination from the resist used to pattern the contact structures. Whereas surface quality could be improved, C contamination was still observed in their STM images.

Dunn *et al.* [108] developed a sub-micron Ta metal patterning process on the Si(111) substrate using electron beam lithography. After initial sample heating to ∼1000 °C, the presence of carbon and carbon related SiC defects was observed on the surface. Further annealing to ∼1200 °C reduced the amount of carbon on the surface but elevated the Ta structures to a height of ∼100 nm and introduced pronounced step bunching. The Ta markers have enabled them to perform local experiments to study the interaction of Ag with a C_{60} layer but no electrical device results were reported.

Hashizume *et al.* [117], [125] have developed a new technique for the fabrication of electrical contacts that combines an optical lithography process with atomic force microscope (AFM) lithography to pattern an optical resist with large contact pads (UV lithography) and smaller (∼100 nm) electrodes (AFM lithography) connected to the optical pads. This was used to define TiW pre-patterned contacts onto the silicon surface before loading into UHV. After UHV sample heating to ∼1200 °C,

trench formation due to Si diffusion leads to a height increase of the TiW electrodes to ∼100 nm. Between these electrodes, nano-scale wires are defined by STM-based hydrogen lithography. After blanket deposition of Ag atoms, increased clustering of Ag atoms in the exposed Si wire pattern and less clustering on the surrounding hydrogen resist was observed. Four terminal in-situ measurements in vacuum [28] show conductance enhancement after the Ag deposition onto the dangling bond wires. Wires of thickness varying from 10 nm to 50 nm were seen to exhibit non-ohmic I-V characteristics with four terminal resistances ranging from $R_{4T} \sim$ 1-4 kΩ. We note that in these experiments, the silicon substrate at room temperature was also conducting and was subtracted to extract the conduction of the Ag wire. However conduction may also occur through Ag clusters which were deposited onto the entire surface.

Ehrichs *et al.* have shown the use of STM to breakdown molecules on a Ni carbonyl blanket layer to form STM-assisted wire $NiSi_2$ wires [27], [107]. In their study, CrPt contacts were evaporated onto the silicon surface using optical lithography prior to introduction into UHV. The resulting chip was wet-chemically cleaned using $NH_4F : HF$ followed by low temperature surface preparation to ∼550 °C in UHV. No high resolution STM image was provided to show the surface quality. After in-situ deposition of a Ni carbonyl blanket layer, the STM was used to break down the Ni carbonyl molecules to form a $NiSi_2$ wire. The wire with dimensions of 100 nm$\times$ 1.45 μm was found to exhibit a four terminal resistance of R_{4T} = 32 kΩ. Widths of ∼100 nm were the smallest feature size that was achieved with this process, and wires with lower thickness were found to not conduct due to breaks along the length. Table 4.1 summarises these reports of using metal as contacts/markers.

4.2.2 Ion-implanted markers

A different class of approach to contact STM-patterned devices is the use of ion implantation prior to introduction into UHV [also summarised in Table 4.1]. Hersam *et al.* [110] reported on the fabrication of diffused p-type and n-type regions (p-n junction). The tunnelling current of the STM increases by orders of magnitude as a function of applied bias when it is scanned over the p-doped region whereas it remains constant over the n-type region. As a consequence, it was possible to reliably relocate a p-n depletion region in the substrate using the STM tip. Nano-scale lithography was then demonstrated on this surface. In order to obtain the necessary contrast for STM imaging, a voltage bias has to be applied in-situ to the p-n junction producing a leakage

current of order 0.1 nA, which has been identified to limit future *in-situ* direct transport measurements. A general limitation of this approach is the low thermal stability of ion implanted structures necessary for the preparation of contaminant-free, atomically flat surfaces in UHV. It is known [29] that considerable surface diffusion occurs above annealing temperatures significantly higher than ∼700 °C which destroys the structural shape of diffused implanted regions.

Tucker *et al.* have since developed a low temperature sample preparation process compatible with pre-patterned ion implanted structures. The process consists of wet-chemical cleaning before introduction into vacuum [115], Ar sputtering in UHV for further surface cleaning [29] followed by low temperature annealing in order to reconstruct the silicon surface whilst the ion implanted regions retain their shape. Initially, the sample is cleaned using a $DI : HCl : H_2O_2$ (RCA) wet-chemical cleaning procedure, which is known to remove metallic contaminants. After removal of the native oxide layer on the silicon surface using diluted hydrofluoric acid (HF), the sample is introduced into UHV. At an Ar background pressure of 7×10^{-5} mbar, the sample is irradiated with a 400 eV Ar beam with a flux of 3×10^{13} s/cm^2. This is found to reduce the residual amount of carbon on the surface to a minimum. However the resulting surface was completely amorphous due to Ar ion irradiation. In order to flatten the surface for STM patterning, the sample was heated to ∼700 °C for 5 min allowing the Si atoms to diffuse on the surface and re-crystallising the surface. The resulting surface was found to be compatible with UHV STM-based hydrogen lithography. While this result shows promise for low temperature sample preparation methods, it would not result in complete removal of residual surface adsorbates and contaminants that would be expected using standard high temperature preparation to temperatures of ∼1200 °C. In general, this leads to increased defect generation and surface roughness – both of which contribute to a degraded surface quality. We note that the demand to achieve atomically clean surface quality is not as stringent for the fabrication of devices at the nano-scale level. However, it will a crucial role for the fabrication of ultra-small devices on the atomic level.

Most recently Tucker *et al.* [113] successfully demonstrated the use of their low temperature sample preparation process for the fabrication of P dopant wires. 200 pairs of interdigitated fingers contacts and two large-scale 2 mm contact pads were implanted with 40 – 50 keV As ions with an estimated ion density of 10^{20} cm^{-3}. Implanted fingers with a width of 1.25 μm were spaced 750 nm apart. STM lithography

was then performed between a random pair of fingers to pattern dangling bond wires into the hydrogen resist. PH_3 molecules were found to adsorb on the reactive dangling bond sites thus forming a PH_3-dosed wire. The sample was encapsulated with $\sim$3 nm of epitaxial silicon at room temperature, followed by rapid sample annealing to 500 °C. The smallest wire using this technique has dimensions of 50 nm $\times$ 750 nm and exhibited a two terminal resistance of $\sim$337 kΩ.

4.2.3 Etched markers

We have seen that the use of metal causes considerable trench formation and contamination during the high temperature sample anneal. Ion implanted structures have been found to lose their structural integrity by diffusion at temperatures above $\sim$700 °C. This constraint to low temperatures compromises the preparation of high quality surfaces and results in residual surface contamination. As a consequence, it is desirable to investigate a method which does not rely on putting down material prior to UHV STM device fabrication. Dunn *et al.* [108] pursued this idea by developing sub-micron registration marker patterned by EBL and etching the silicon substrate [also summarised in Table 4.1]. Pattern transfer into the silicon substrate occurs by wet-chemical etching using KOH as an etchant. KOH is known to etch anistropically along the Si(111) direction and is widely used in both, the industrial as well as in the research environment. After introduction into UHV, samples were outgassed at $\sim$600 °C followed by sample heating to $\sim$900 °C for 60 s. STM images showed that L-shaped markers of $\sim$400 nm in width and 25 nm in depth survive this heating step. However the anneal was not sufficient to remove SiC defects on the surface. Further annealing to $\sim$1100 °C partially removed the C density on the surface but significantly blurred out the marker structure.

All pre-patterning methods used, whether it is etching, ion implantation or metal deposition, have to survive the high temperature sample preparation step. However, it is possible to circumvent this step by patterning the surface *after* the sample anneal in UHV. There has been one approach in the literature [112], [126], [127] which uses *in-situ* deposition of Ag onto silicon through a diaphragm placed between a MBE source and the sample substrate. The diaphragm consists of a 1 μm thick foil with microholes down to a feature size of 500 nm that prepared using a focused ion beam system (FIB). In the first reports, the sharpness of the pattern boundary was determined to be about $\sim$100 nm on a Cu substrate [127]. This process was also used on the silicon surface

where Ag electrodes were deposited onto the Si(111) surface after sample preparation by annealing to ∼1200 °C. Subsequently, an Au-coated cantilever of an atomic force microscope (AFM) (in contact mode) was used to literally scratch a 4 nm wide Au wire between two electrodes separated by 7 μm. The width of the wire was found to be independent of the contact force and depended solely depends on the particular shape of the cantilever. Conductance measurements performed on the Au wire at 4 K and revealed non-ohmic I-V characteristics with two terminal resistances ranging from 170 to 250 MΩ. No conduction was observed on samples without wire patterning [112].

In a more recently published report by the same group, tests on the Si(111) 7×7 reconstruction showed that considerable Ag atom migration occurred at room temperature preventing the formation of well-defined patterns on this surface. However it was found that on an In induced metal/semiconductor reconstructed surface, namely the Si(111)-4×1-In surface, sharply defined Ag electrodes could be formed by means of low temperature deposition at 120 K [126] preventing Ag migration. A couple of issues of this method make it unusable for robust STM-patterned device fabrication. Robust devices, which can be operated outside UHV, require encapsulation to preserve the device structure. It is known that epitaxial encapsulation occurs by 3D nucleation on the Si(111) surface. It is desirable to show if a deposition process can be developed on the Si(100) surface exhibiting little metal migration. Therefore different deposition metals have to be considered which exhibit less diffusion at room temperature than Ag.

4.3 Registration markers developed in this thesis

From the results of the literature survey described in the previous section we can draw the following conclusions:

- The use of pre-patterned metal contacts on the surface prior to UHV device fabrication deteriorates the surface at the atomic level, causing either surface reconstruction or trench formation and step bunching due to Si mobility at elevated temperatures.
- The use of pre-patterned ion-implanted markers require a low temperature sample preparation process in UHV, which cannot achieve high quality surfaces at

the atomic scale.

- The usability of etched registration markers is promising for achieving the highest surface quality but, prior to this thesis, thermal stability was only demonstrated up to 1000 °C which is not sufficient to remove traces of carbon contamination from the surface.

- Whilst in-situ methods are a viable alternative to pattern the surface after the UHV sample preparation step, no successful process has been demonstrated for Si surfaces.

Since the aim of this thesis is to provide a pathway for the fabrication of atomic-scale devices, atomically clean surface quality plays a major role in the choice of our registration process. Therefore, we have pursued the fabrication of registration markers that are compatible with heating to ∼1200 °C. The markers are defined by optical lithography and wet-chemically etched into the silicon substrate. We will show how a SiO_2 mask is used to critically protect the silicon surface during resist patterning of the registration markers. A rigourous wet-chemical treatment is used to remove the oxide and therefore any organic or metal contamination from the sample prior to its introduction into the UHV environment. This process has been patented during my thesis and I am the lead author (40 %) on this patent (see page **xix** for details).

Initially, in Section 4.3.1, we describe a series of calibration tests which were undertaken to determine the minimal marker size using our in-house optical lithography facilities and the minimal etch depth which survives the high temperature anneal. Section 4.3.2 describes the fabrication process of the registration markers in detail. Following on from this the properties of our registration markers during the critical steps of a STM-based fabrication process in silicon are discussed in Section 4.3.3.

4.3.1 Optimisation of pattern structures etched into Si

The focus of this section lies on the optimisation of process parameters that influence the quality and shape of features defined by our in-house optical lithography system and subsequent etching into the silicon substrate. The parameters we have investigated are sample size, sample to mask distance, exposure time, UV light intensity and etching time. The optimal process parameters to create suitable features were subsequently used for the fabrication of registration markers.

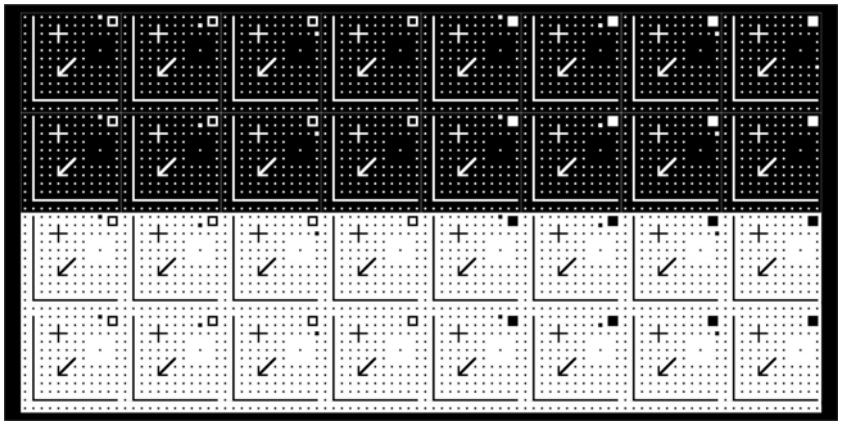

Figure 4.1: Test mask for etched registration markers. The mask investigates the best way to pattern features down to a minimal structure size of 1 μm.

For this purpose, an optical mask was designed for optical lithography to determine which shape and size of markers are suitable for use as registration markers. The final designs in TurboCAD were performed with technical support from Andrei Skougaresky. The masks was fabricated by Photronics Ltd based in Manchester, UK. It consists of a quartz glass plate which is laser-beam patterned with a chrome layer. Chrome is impenetrable by ultra-violet (UV) light rays which are used in the optical lithography process. As a consequence, the optical resist is only exposed to the UV light where the mask is not patterned by the chrome layer. According to their specification, the relative chrome pattern positioning error is of order $\sim$50 nm determined using a Leica IPRO tool, which is accurate to $\pm$5 nm.

Fig. 4.1 shows the test mask pattern for etched and protruding features. A dark-field mask design was used where black represents the chrome layer and white stands for the area exposed to UV on the chip. That means the blocks in the first two rows are used for the fabrication of etched features, whereas the blocks in the lower two rows produce protruding features in the silicon substrate. Different structures such as arrows, crosses, outlined and solid squares were chosen to test which particular features can be best relocated using the SEM and/or the STM. In particular, asymmetric structures which can *point* into a certain direction are useful in order to assist with the navigation to the active device region. The mask is divided into elementary blocks of 48×48 μm^2 in size. In order to navigate between blocks, each one has a unique pattern represented by the 5×5 μm^2 and the 2×2 μm^2 square in the upper right corner.

Fig. 4.2 shows the process flow of the crucial fabrication steps. More details about

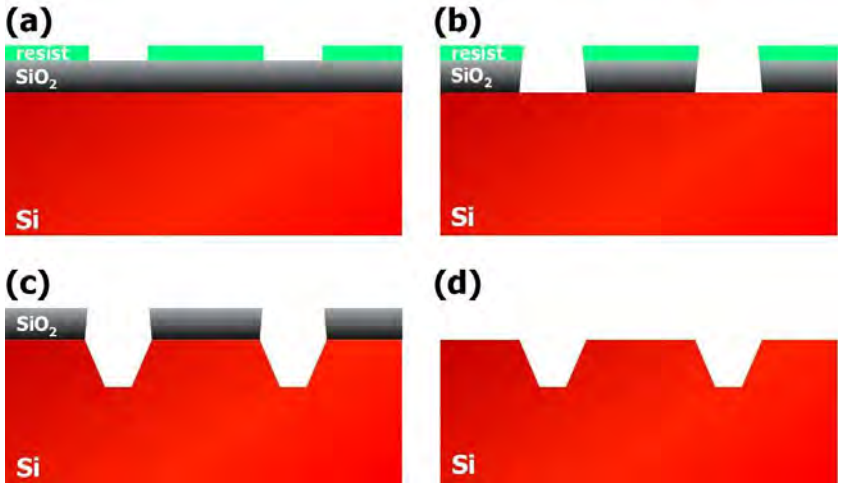

Figure 4.2: Process flow for the fabrication of registration markers. (a) Optical resist patterning using optical lithography. (b) Pattern transfer into the SiO_2 layer using NH_4:HF with slight etch undercut. (c) The SiO_2 layer serves as a mask during the TMAH etch of markers into Si followed by optical resist removal. (d) Final chip with etched markers after SiO_2 removal using another NH_4:HF etch step.

this fabrication process will be presented in the subsequent section where the fabrication of registration markers and the wet-chemical processing steps outlined below will be discussed in detail. The starting point is a phosphorous-doped (10 Ωcm), n-type Si(100) wafer with a 100 nm SiO_2 grown in dry oxygen at 1100 °C. An optical resist (AZ 6112, 1 μm thickness) on top of the oxide is patterned by optical lithography using a Quintel Q6000 aligner [Fig. 4.2 (a)]. After resist development, the test pattern is transferred into the SiO_2 layer using a NH_4:HF etch [Fig. 4.2 (b)]. Thereafter the optical resist is wet-chemically removed [Fig. 4.2 (c)]. Subsequently, the test pattern is etched into the silicon substrate along the Si(111) direction using tetramethyl ammonium hydroxide (TMAH) as an etchant. Prior to introduction into the UHV STM-SEM/MBE system, the protective SiO_2 layer [Fig. 4.2 (d)] is removed during another NH_4:HF etch step followed by wet-chemical sample cleaning to remove residues of metal and organic traces. Five parameters were found to affect the ability to transfer the pattern from the mask to the optical resist – sample size 5.1 cm (2”), sample-mask distance, UV light dose, the integrity of the optical resist and the thickness of the SiO_2 layer. Larger sample sizes were found to improve the sample-mask contact in the centre. After optimising these parameters, we could reproducibly transfer patterns with precision ∼50 nm precision into the resist. After development with MIF 300 developer,

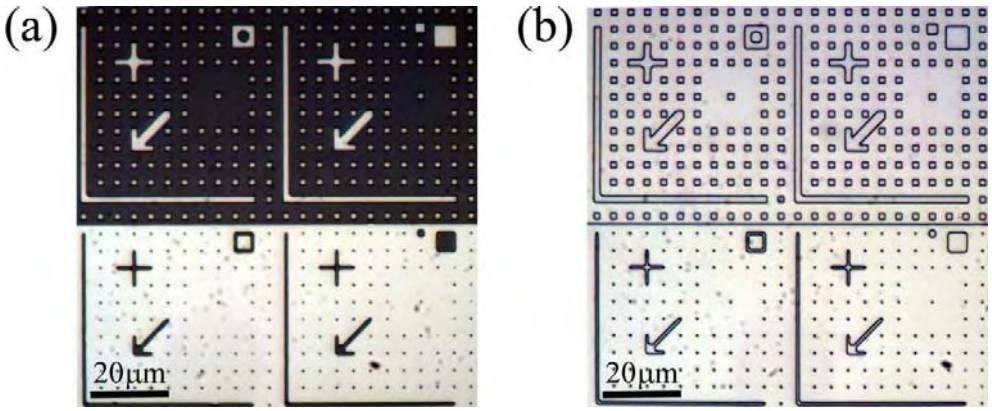

Figure 4.3: Optical microscope images of test pattern etched in silicon before and after SiO_2 layer removal. Test sample after (a) pattern transfer into silicon and after (b) consecutive removal of the SiO_2 layer .

we transfer the pattern to the SiO_2 layer as shown in Fig. 4.2 (b). Two variables mainly influenced this process: the adhesion and integrity of the optical resist and the thickness of the SiO_2 layer. We found that a thickness of $\sim$1 μm of the optical resist proved to be robust during NH_4:HF etching used for pattern transfer. It was found that there is a slight undercut during etching of the SiO_2 layer which increases the feature size by $\sim$200 nm during pattern etching into silicon. This increase in feature size was directly related to the thickness of the oxide layer. The effect of the undercut was minimised by reducing the oxide layer thickness. The oxide layer was reduced from an initial $\sim$500 nm to $\sim$100 nm minimising the increase in feature size to $\sim$100 nm.

Figure 4.3 (a) shows a typical optical microscope image of the test pattern after the pattern was wet-chemically etched into the silicon substrate to a depth of $\sim$380 nm using TMAH. The etch rate at 60 °C was determined to be 150 $\frac{nm}{min}$. Subsequently the 100 nm oxide layer was removed as shown in Fig. 4.3 (b). Whereas the smallest etched features are somewhat enlarged to $\sim$1.3 μm, the feature size of the protruding counterpart is reduced in size to about 800 nm. The difference in feature size is a result of undercut for both, the SiO_2 layer etching and the latter TMAH etching. Reducing the SiO_2 layer thickness and control of the Si etch depth were the two main factors that minimised the undercut giving us better size control.

The chip as shown in Fig. 4.3 (b) was subsequently introduced into the UHV STM-SEM/MBE system. The scanning electron microscope is adjusted to the same focal point as the scanning tunnelling microscope which allows simultaneous STM and SEM imaging. In addition, the SEM can be used for precise positioning of the STM

tip. Fig. 4.4 demonstrates the image quality of the markers obtained from the UHV SEM attached to the STM chamber. The images were taken at a beam energy of 25 keV with an imaging current of 1 nA and an estimated beam spot size of 20 nm. Fig. 4.4 (a) and (b) depict SEM images of etched and protruding building blocks respectively. An enlarged section of an etched and protruding 3×3 array is shown in (c) and (d) respectively. Here, it is apparent that the etched markers are enlarged to ∼1.5 μm whereas the protruding markers are of ∼800 nm in size. The effect of prolonged sample heating to ∼1200 °C in both cases can be seen in fig. 4.4 (e) and (f). At temperatures of ∼1200 °C, the Si atoms on the surface are highly mobile and contribute to significant Si mass transfer which distorts the sharp contours of the markers. Whereas the etched markers only blur out slightly and stay intact, the protruding dot array smears out to about twice the dot size. This effect is mostly due to their smaller size, but it is clear that Si diffusion for etched and protruding features is not identical. We have found that the minimum marker depth/height required to produce sufficient contrast using the UHV SEM for identification of either etched or protruding features is of ∼80 nm. The geometric relation between the feature size, l and etch depth, d is given by $l = \frac{2d}{tan[\alpha]}$, where α denotes the etch angle of 54.7 °. Therefore, the maximum depth for 1 μm wide markers is geometrically limited to 700 nm. Deeper etch depths require a larger feature size. In a separate experiment, we found that the feature size is indeed enlarged at an etch depth of 2.4 μm. Therefore we have chosen an etch depth of about 350 nm, which we have seen to be sufficient to preserve the smallest etched structures of ∼1 μm after the high temperature anneal.

In summary, we have discussed the influence of the most crucial process parameters for the reliable fabrication of etched structures into the Si(100) surface. The main problem was to maximise the contact between mask and sample. By increasing the sample size from 1×1 cm^2 to 5.1 cm (2″), switching from pressure contact mode to vacuum contact mode, adjusting exposure time and light intensity, it is possible to simultaneously create protruding and etched features down to 1 μm and below on a silicon surface patterned by optical lithography. By decreasing the SiO_2 layer thickness from 500 nm to 100 nm and reducing the etch depth of initially 2.4 μm to 380 nm, undercut was significantly reduced ensuring pattern reproducibility of the etched features. The smallest features fabricated with our in-house optical lithography process to date are protruding squares of ∼800 nm in size and etched squares of about 1 μm. Both structures survive the UHV sample heating preparation step and can be used

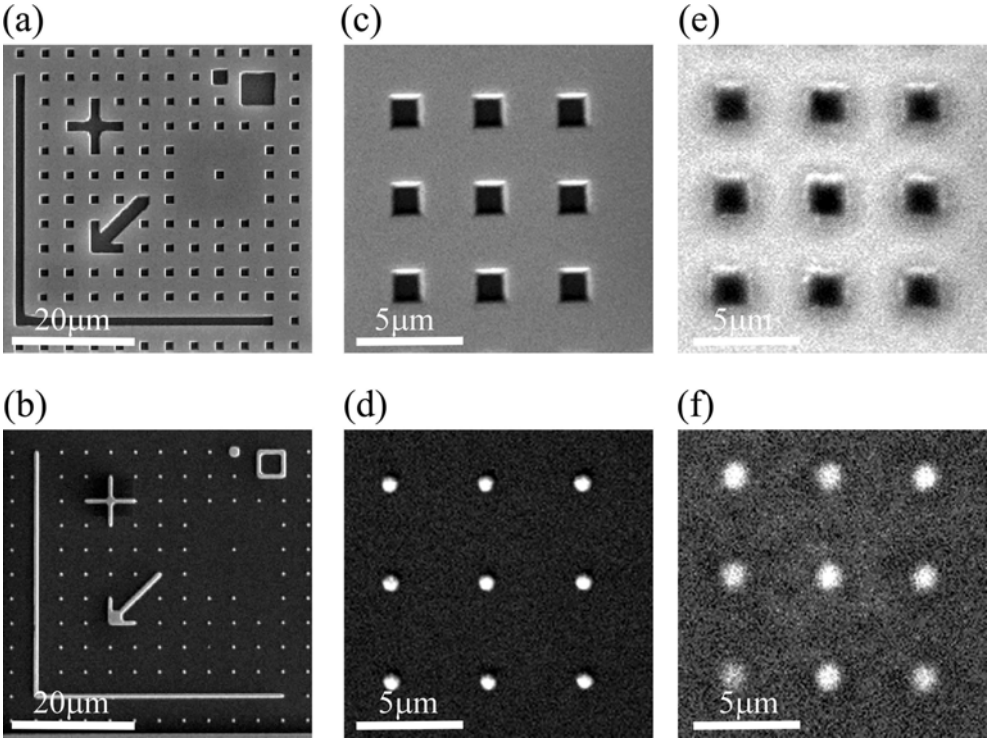

Figure 4.4: Scanning electron microscope images of typical test patterns. UHV SEM images of etched (a,c,e) and protruding (b,d,f,) features. Comparison of features after initial outgassing at 400 °C and after extended sample heating to 1200 °C for etched (c,e) and protruding (d,f) markers.

separately or in combination for device and contact alignment. A crucial advantage of the etched features over protruding features is the protection of the device surface from contamination by the SiO_2 layer during the fabrication process. This is why we have chosen etched features to serve as registration markers. The following section describes in detail the registration marker fabrication process, as used for STM-fabricated devices, based on the optimised parameters from this work.

4.3.2 Fabrication of registration markers

Following the understanding gained from the behaviour of the test pattern, a second mask was designed for the fabrication of registration markers which were subsequently used for STM-patterned devices.

It is first interesting to discuss how best to make the mask compatible with the STM scan ranges and clean-room processing. Typically, an STM uses samples that are of about 3 mm$\times$9 mm in dimension which allows sample preparation by directly passing a current through it thereby heating the sample to the required annealing temperature of $\sim$1250 °C. However samples of these dimensions pose difficulties for clean-room processes such as beading of resist around the edges of the sample and inhomogeneous sample-mask contact during optical lithography due to the small sample size. Therefore for the samples used in this thesis, the STM system was specially designed to accommodate larger, 1$\times$1 cm^2 sample sizes. This size is a good compromise to achieve both, high quality atomic resolution STM imaging and reproducible clean-room processing. However the larger sample size makes sample preparation by direct current heating problematic. Therefore we employ an electron beam heater which heats the sample from the backside.

The mask was designed such that four 1$\times$1 cm^2 sample areas would fit onto a single 2″ wafer and can be processed simultaneously thereby avoiding the problem with sample-mask contact during optical exposure. Each sample consists of a 3$\times$3 array of registration markers. The position of a small transparent square in the four largest squares, 50$\times$50 μm^2 in size, labels the set of registration markers from one to nine. A complete pattern of registration markers is shown Fig. 4.5. The 50 μm wide square structures are used for locating the respective registration marker set using the SEM prior to STM imaging. All other structures help to guide towards the active device area. The active device area is encompassed by four 4 μm wide triangles and four 1 μm wide squares compatible with the 6$\times$6 μm^2 scan range of the STM. Using the

SEM, the STM tip is guided to the active device area, where the absolute position can then be verified using STM imaging itself for tip positioning with respect to the markers. The dimensions of one quarter of the registration mask for one marker set (out of nine) are given in units of [μm] in Fig. 4.5 (b). The dimensions and distances of the complete pattern is given by mirror symmetry. To test the quality of this mask, we used the standard procedure as developed in Section 4.3.1. We use P-doped (1 – 10 Ωcm) 2″ Si(100) wafers as the starting material for the fabrication of registration markers. Initially, the substrate is cleaned using a wet-chemical cleaning cycle consisting of sulfuric peroxide (SP) $(H_2SO_4 : H_2O_2\ 3:1)$, deionised water (DI) rinse and RCA-2 $(DI : HCl : H_2O_2\ 6:1:1)$ at 80 °C. SP is known to remove organic remnants from the silicon surface. The RCA-2 procedure developed by W. Kern [128] is the industry standard for removing metal contaminants on semiconductor surfaces. We thermally grow a 100 nm thick SiO_2 blanket at 1100 °C (50 min) in dry oxygen to protect the sample surface. Thereafter we pattern registration markers in a 1 μm-thick AZ 6112 photo resist using optical lithography at low UV light intensities of $\sim$10 $\frac{mW}{cm^2}$ and an exposure time of 500 ms. Using vacuum contact mode which minimises the distance between the mask and the sample, we achieve the best possible pattern resolution with our in-house Quintel Q6000 aligner. After development in MIF 300, we employ an O_2 plasma etch for 20 min to remove residues of exposed organic resist from the developed pattern. The pattern is then transferred from the optical resist into the 100 nm thick SiO_2 layer using a $NH_4F : HF$ 15 : 1 solution.

Thereafter, we completely remove the optical resist using SP. In the next step, the SiO_2 layer acts as a mask for pattern transfer to the underlying silicon preventing the silicon wafer from being directly exposed to the organic resist. We use tetramethyl ammoniumhydroxide (TMAH 25 %) [129], [130], [131], [132] to etch the registration markers embedded in the SiO_2 mask into the silicon substrate. TMAH is a wet-chemical etchant similar to KOH but exhibits a lower etch rate. The etch rate can be adjusted by varying the temperature. For our experiments, we used a bath temperature of 60 °C resulting in an etch rate of $\sim$150 $\frac{nm}{min}$ which gave sufficient control over the etch depth. Etching for 2.5 min results in anisotropically etched patterns along the Si(111) crystal axis of $\sim$350 nm in depth. The anisotropic etching angle α of 54.7° determines the relation between the marker size l and the maximum etch depth d as $l = \frac{2d}{tan[\alpha]}$. The 2″ wafer is then cleaved into four 1×1 cm^2 samples. Before introduction into the STM-SEM/MBE system, the SiO_2 layer is removed using $NH_4F : HF$ 15 : 1.

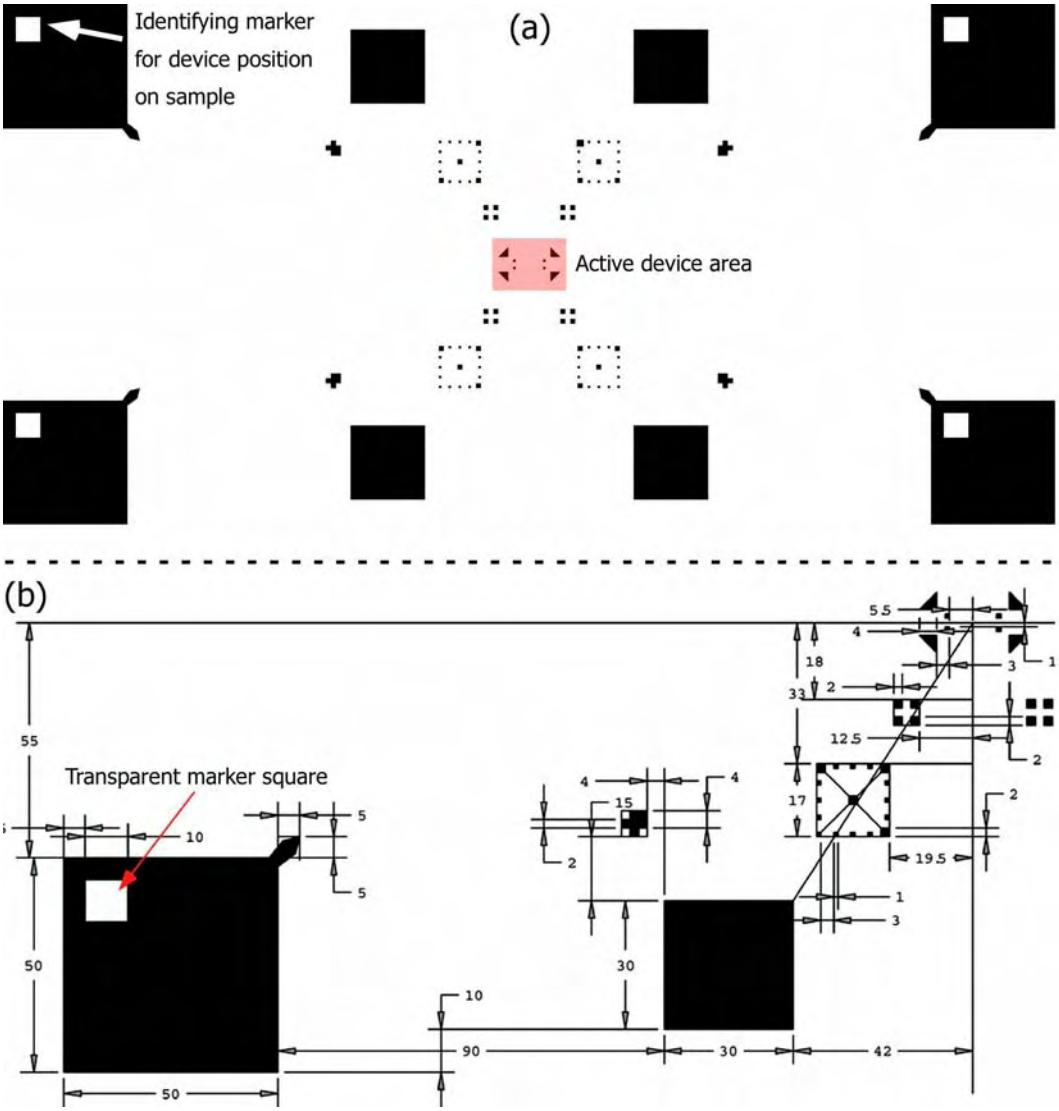

Figure 4.5: A schematic of the optical mask developed for registration markers. (a) A complete image of the registration markers including dimensions, showing the large 50 μm squares for device location. The active device region is shown by the red shaded area. (b) Details of dimensions of the lower left quarter of the mask in micrometres.

The silicon substrate undergoes another cleaning cycle with an added cleaning step of DI:HF (5 %) between the SP and RCA-2 treatment. DI:HF (5 %) has been found to further decrease residual carbon traces from the silicon surface.

4.3.3 Properties of registration markers during UHV fabrication process

Once the sample is introduced into the STM-SEM/MBE system, it is initially outgassed for ∼2 h below 500 °C. This step mainly removes water from the chip which has been accumulated during ambient transfer in air from the clean-room to UHV. It is important to note that at this low temperature, the protecting native oxide is not removed from the sample surface [133]. We then anneal the sample to ∼1200 °C giving rise to a peak vacuum pressure of $\sim 5 \cdot 10^{-9}$ mbar by heating the backside of the sample using an electron beam heater to remove residual traces of carbon and to form the Si(100) 2×1 reconstruction. The relatively high pressure of $\sim 5 \cdot 10^{-9}$ mbar is mainly caused by indirect heating of the manipulator arm by the electron beam rather than the Si sample itself. We found that the peak pressure was largely independent of the initial base pressure in the chamber before the annealing step.

The properties of our registration markers in the UHV environment were investigated using the custom-designed UHV STM-SEM/MBE system. Initially, the markers are subject to the high temperature sample preparation procedure in UHV. The markers also have to survive device encapsulation in epitaxial silicon (∼25 nm) at low temperatures of ∼250 °C. Fig. 4.6 contains SEM images of a series of registration marker images at different magnification during these different stages of processing. All images that were obtained with the SEM in this section were taken at a beam energy of 25 keV with an imaging current of ∼1 nA and an estimated electron beam spot size of 20 nm. Fig. 4.6 (a) shows an SEM image of a complete set of etched registration markers after initial sample outgassing at below 500 °C showing how the SEM can be used to position the STM tip with respect to the registration markers. The central registration markers point the way to the device area and are shown again with increasing detail in Fig. 4.6 (b,c).

The central registration markers, consisting of 1 μm wide squares, 4 μm width triangles and 2×2 arrays of 2 μm wide squares, are shown before the high temperature annealing step in Fig. 4.6 (d). Fig. 4.6 (e) shows the same markers after annealing to ∼1200 °C and Fig. 4.6 (f) after consecutive growth of ∼25 nm of epitaxial silicon at 250 °C. This series of SEM images shows that the shape of the markers is preserved.

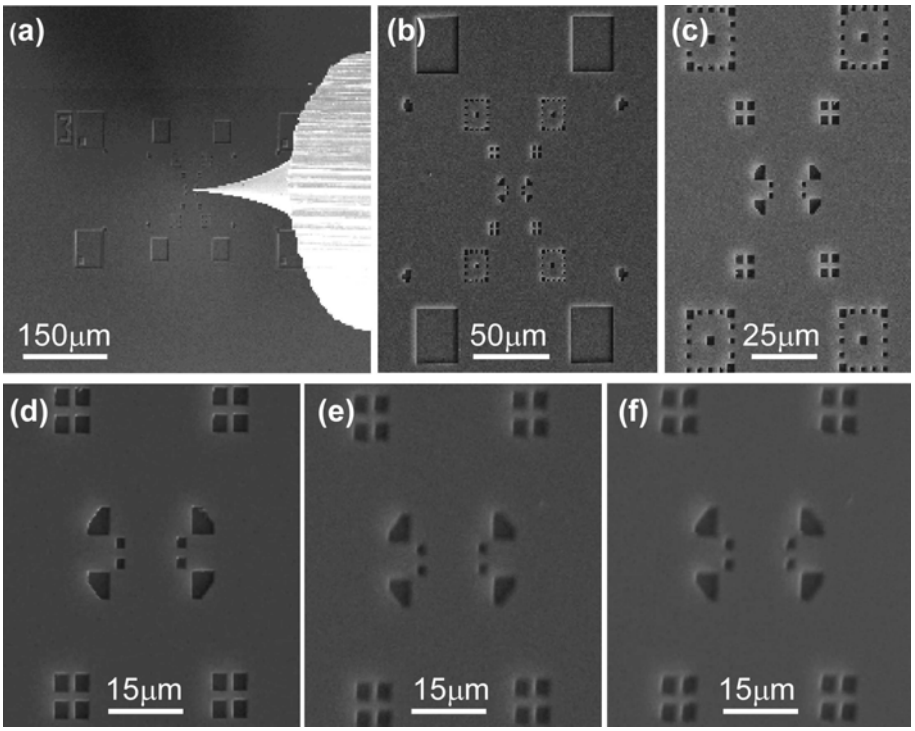

Figure 4.6: SEM images of etched registration markers during the fabrication process. SEM images of etched registration markers before sample annealing, (a) complete set of registration markers including aligned STM tip and (b) and (c), higher magnification images of the central region. SEM images of the device region before (d), after (e) sample heating to 1200 °C and subsequent (f) epitaxial growth of 25 nm Si.

However, the SEM images in Fig. 4.6 (e,f) are slightly blurred due to smoothed marker edges during the annealing step leading to a decrease in imaging contrast. We have also grown thicker layers of Si up ∼100 nm over the markers and observed that the appearance of the markers is the same as shown in Fig. 4.6 (f). The markers which are shown here and which will be used for the fabrication of devices later on exhibit an etch depth of ∼350 nm which decreases after the annealing step as will be discussed in detail below. We have also varied the etch depth from 2.4 μm down to 40 nm and found that the minimum marker depth to produce sufficient contrast for identification in our UHV SEM is of order ∼80 nm. However we would like to note that markers with shallower depths can still be used for alignment since the markers remain visible for the STM (see also Section 8.2).

Fig. 4.7 (a) shows how the position of the STM tip is monitored using the SEM with respect to the registration markers. Later on, we will show how this allows us to STM-pattern nano-scale structures at precise locations. We also use the STM to investigate the silicon surface quality around the registration markers. Fig. 4.7 (b) shows a filled state STM image of the reconstructed Si surface after the high temperature sample preparation. The image shows that the surface quality in the device area close to the two smallest, left registration markers is atomically clean with a low defect density of order 0.5 %. Seven step edges, caused by the sample miscut resulting in eight Si terraces, are visible. From this we can conclude that the markers have not adversely affected the structural quality of the surface in the device area. Fig. 4.7 (c) is a high resolution filled state STM image demonstrating atomic resolution on the large, 1×1 cm^2 samples with two missing dimer vacancies (DV). The ability to achieve atomic resolution is important since it allows us to perform atomic-scale STM manipulation on large sample sizes compatible with standard clean room processing.

Simultaneous SEM and STM imaging enables us to observe the surface morphology due to the presence of the markers. Fig. 4.7 (d) shows an SEM image of the two smallest ∼1 μm wide registration markers before sample annealing. Looking at the same area with the STM after sample annealing is shown in Fig. 4.7 (e), where the anisotropy of the TMAH etch becomes visible. The TMAH etch carves out - layer by layer - inverted pyramids into the silicon substrate along the Si(111) axis. Their opening angle, given by the anisotropic etch angle of ∼54.7°, enables us to image both, inside and outside the markers using the STM.

We find that after our standard sample preparation anneal to 1200 °C for 10 s, the

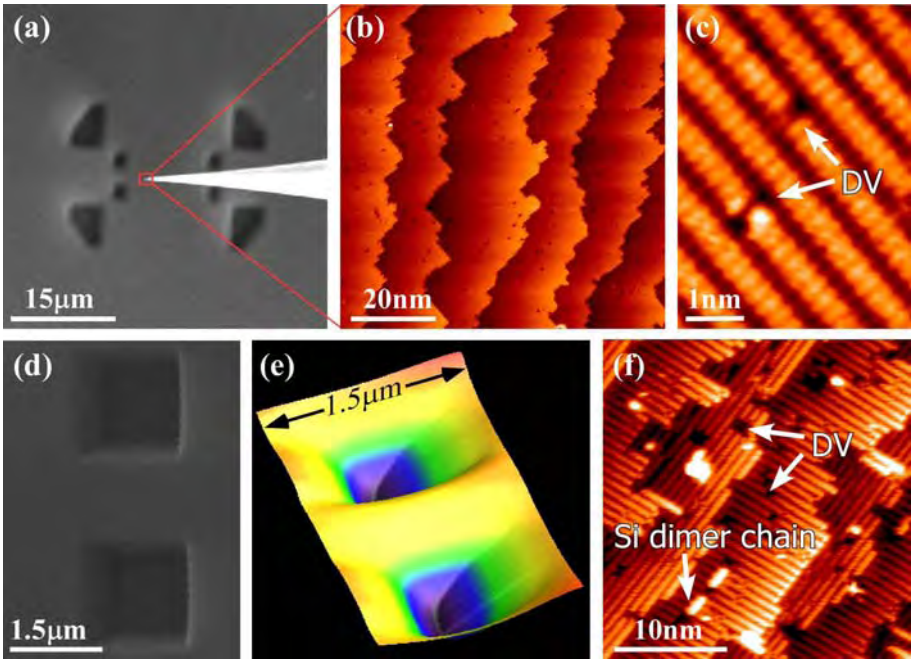

Figure 4.7: Surface quality and morphology of registration markers. (a) SEM image of the STM tip aligned to central square markers. (b) STM image of highlighted area illustrating typical surface quality in the device region. (c) High quality STM image demonstrating atomic resolution on 1×1 cm^2 samples used for device fabrication. SEM image of the smallest $\sim$1 μm wide markers before sample annealing (d) SEM image of two 1 μm sized registration markers and (e) corresponding 3D STM contour plot after annealing. (f) STM image *inside* the markers showing nanometre wide terrace structures. STM imaging conditions: V $\sim$ -2 V, I $\sim$ 0.2 nA.

Feature size L [μm]	Time
0.5	0.1 s
1-1.5	2-10 s
2	32 s
4	8.5 min
30	448 hr

Table 4.3: Relationship between time and feature size for the decrease in marker depth from 350 nm to 100 nm by annealing to 1200 °C. After the diffusion model suggested by Keeffe *et al.* [135].

depth of the etched markers decreases from initially ∼350 nm to ∼100 nm. In order to understand this decrease in marker depth, we present a higher resolution STM image shown in Fig. 4.7 (f) of the surface structure inside the registration markers. This image shows a series of steep, short nanometre wide terraces, extending to the bottom of the etch pit. Additionally, a few Si dimer chains are visible on the surface. Such a silicon dimer pattern is related to the presence of C [61] which is only found in the exposed marker region but is not seen in the device area due to its protective SiO_2 layer. It is expected that during the anneal, silicon atoms diffuse from the edges to the bottom of the etch pits via adatom transfer. Tromp *et al.* [134] have shown that at elevated temperatures thermal diffusion adatoms occurs across the Si(100) surface in the form of Si dimers i.e. pairs of silicon atoms. The decrease in depth was seen in previous annealing studies of square-wave gratings etched into the Si(100) surface by reactive ion etching [135]. In their study, a grating was defined using electron beam lithography. The grating amplitude Z was found to decreases exponentially during sample annealing as $Z(t, T, L) = Z_0 \cdot e^{-\lambda}$, where λ denotes the decay constant. The decay constant λ depends linearly on annealing time t, exponentially on the annealing temperature and to the inverse fourth power on the feature size L i.e. $\lambda = \frac{Fct(e^T)}{L^4} \cdot t$. For the smallest markers used in our experiments, this simple diffusion model predicts a decrease in marker depth from 350 nm to 100 nm during heating to ∼1200 °C for 10 s, in good agreement with our results. Table 4.3 illustrates the strong dependence of the marker depth on the marker size L. The time it takes for a decrease in marker depth from ∼350 nm to ∼100 nm by annealing to ∼1200 °C is shown for various feature sizes. Whereas structures of size $L \sim$ 1-1.5 μm exhibit a decrease in marker depth in about 2-10 s, the same decrease takes about 450 hr for 30 μm wide markers. From the strong dependence of the depth decrease on the feature size illustrated in Table 4.3, it can also be seen that registration markers much smaller than 1 μm will fill up really

quickly due to silicon diffusion at elevated temperatures. This shows that the ultimate size of registration markers that we can feasibly observe clearly in the SEM is of order 1 μm.

So far we have seen that our etched registration markers survive all the critical steps necessary for STM device fabrication. Another critical factor is the alignment accuracy that this technique allows for the positioning of STM-patterned structures. One elegant way to confirm the absolute position of the STM tip is by approaching the STM tip to a registration marker while tracking its position with the SEM as is indicated in Fig. 4.7 (a). When the STM tip reaches the edge of the marker, the tunnelling current drops dramatically. Comparing the SEM image of the location of the STM tip at this point allows us to estimate an alignment accuracy of order 100 nm which can be regarded as the limit of our SEM-monitored STM positioning technique.

Alignment can be improved by having shallower markers closer to the device area which are only visible to the STM. Indeed, we patterned smaller markers using an electron beam lithography process which will be discussed as part of Chapter 8. With such a self-aligned process, the alignment is improved below the 100 nm level. Further strategies are known to improve alignment such as small grids of registration markers and/or the use of the optical positioning read-out of the STM stage. The use of grids helps to statistically reduce misalignment. The optical positioning read-out of the STM-SEM/MBE system was designed to be able provide absolute positioning of the STM tip down to the sub 20 nm level. To this end, initial test have proven the ability to relocate the same area within 100 nm after the stage has been moved back and forth by 5 mm. Whilst initial investigations have been conducted, the incorporation of grids and optical position readout into the device fabrication process is beyond the scope of this thesis.

4.4 Outline of complete fabrication strategy

Fig. 4.8 outlines the complete fabrication strategy we have developed to fabricate STM devices [30], [136] using the registration markers developed above. The creation of registration markers enables the precise positioning of the STM tip with respect to the registration markers as shown in Fig. 4.8 (a). Following passivation of the surface with a monolayer of hydrogen, we can use the STM to pattern the surface. An example of STM-based lithography is shown in Fig. 4.8 (b). Phosphine gas (PH_3) se-

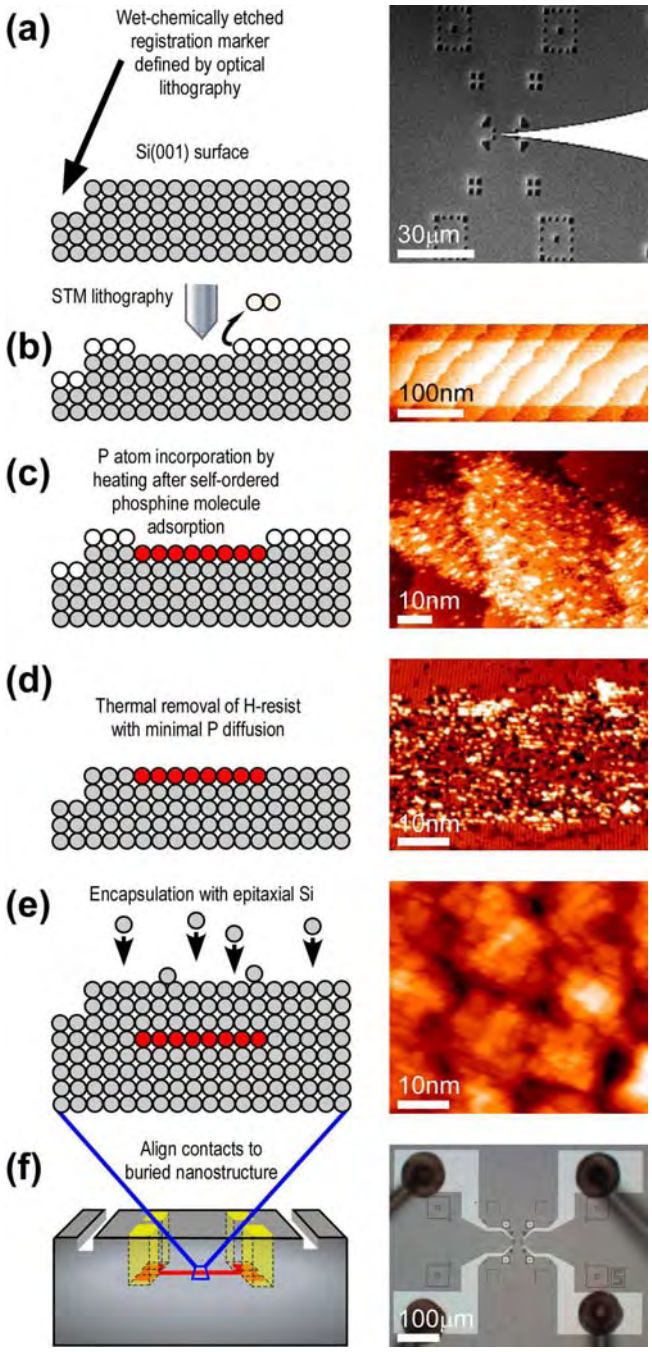

Figure 4.8: Outline of a novel device fabrication strategy for the creation of Si:P nano-scale devices using scanning probe microscopy. *Left:* (a)-(e) Cross-sectional schematics of essential fabrication steps and (f) 3D sketch of final device. *Right:* Corresponding (a) SEM image of STM tip (white) aligned to registration markers, (b) STM image of lithographically-patterned wire, STM images of P incorporated wires, before (c) and after (d) hydrogen resist removal and (e) 25 nm MBE Si overgrowth; concluded by an optical microscope image of the final device with bonded contact wires (f).

lectively adsorbs onto the exposed Si surface. Using an anneal step, we are able to incorporate phosphorus atoms from the adsorbed phosphine into the silicon crystal with nanometre precision. The incorporation is accompanied by the ejection of silicon forming chains on the surface and appear as bright lines in Fig. 4.8 (c). This anneal helps to electrically activate the excess electron provided by the P atom, which is incorporated into the bulk of the silicon matrix at a temperature below which diffusion out of the STM-patterned structure would occur. The presence of the hydrogen resist has been found to be detrimental for the growth of epitaxial silicon layers. A further annealing step allows removal of the hydrogen resist layer without significant P atom surface diffusion as shown in Fig. 4.8 (d). The Si:P nanostructures are then encapsulated using low temperature silicon MBE which was shown to lead to complete electrical activation of the buried phosphorus atoms in a δ-doped layer [137], [138]. The Si surface after growth of 25 nm of epitaxial Si is shown in 4.8 (e). The final step in the fabrication process is the ex-situ alignment of four macroscopic Al contacts to the buried structures using the registration markers. Ohmic contacts are formed using a low temperature heating step in which the aluminium diffuses to the buried, STM-fabricated P-doped contact pads. An optical microscope image of the final device structure is shown in Figure 4.8 (f). In the following sections, we will describe each stage of the process in detail.

4.4.1 UHV sample preparation

After thorough wet-chemical cleaning, the sample, patterned with nine sets of registration markers, is loaded into the STM-SEM/MBE vacuum system. Initial sample outgassing at temperatures around $\sim$400 °C for several hours in the preparation chamber mainly serves to desorb remnants of water vapour which cannot be avoided by sample transfer from the clean-room into the UHV system. Immediately afterwards the silicon chip undergoes a high temperature annealing profile peaking at a temperature of $\sim$1200 °C for 10 s. Due to the large sample size, this is achieved by using the electron beam heater which enables us to homogeneously heat the backside of the sample thereby desorbing remaining adsorbates, such as residual traces of carbon and organic resist, from the surface. This is the most severe process step that the registration markers have to survive. The heating step is necessary to form the Si(100) 2×1 surface reconstruction and to achieve the highest possible surface quality for STM lithography.

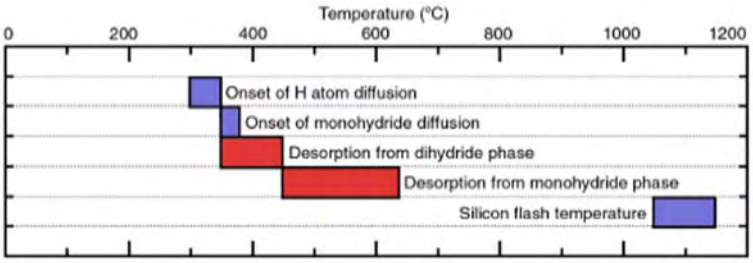

Figure 4.9: Temperature-dependent bonding phases of hydrogen on Si(100) relevant for the formation of hydrogen resist and thermal hydrogen removal. Dihydrides are present for substrate temperatures below ∼400 °C. Monohydrides start to diffuse at temperatures above 350 °C and exhibit a desorption peak at about 550 °C; taken from [51].

4.4.2 Formation of the hydrogen resist

Hydrogen resist technology has been used by many groups as a means to passivate the highly reactive Si(100) surface. Using atomic hydrogen, it is possible to terminate the Si(100) surface to create an inert surface. High resolution STM imaging allows the study of selective adsorption of molecules on dangling bond sites. More importantly, dangling bond sites for the adsorption of molecules can also be created using STM lithography – a key step for the formation of atomic-scale devices. The hydrogen-passivated surface is typically formed by in-situ exposure of atomic hydrogen to the clean Si surface. The resulting reconstruction depends on the substrate temperature during atomic hydrogen exposure [139]. There are two distinct surface phases, the *monohydride* phase and the *dihydride* phase. For the formation of the monohydride phase, the π-bond between the Si dimer atoms is broken and a single H atom bonds to each end of the Si dimer. However the σ-bond between the two Si atoms, forming the dimer, stays intact. For the formation of the dihydride phase, the σ-bond between the dimers is broken, such that each Si atoms ends up with two H atoms. The monohydride [Si(100)-2×1:H] surface is chemically inert and more stable than the dihydride [Si(100)-3×1:H] phase. It is therefore the most desirable reconstruction for the formation of STM-patterned devices. Fig. 4.9 elucidates the dependence of hydrogen density on the substrate temperature relevant for both, the formation of hydrogen resist and thermal removal of hydrogen discussed in Section 4.4.5. Temperature-dependent hydrogen desorption studies [140], [141] reveal two H-desorption peaks. The first desorption peak occurs around 400 °C and is related to dihydride desorption. The second desorption maxima around 550 °C is related to monohydride desorption. It

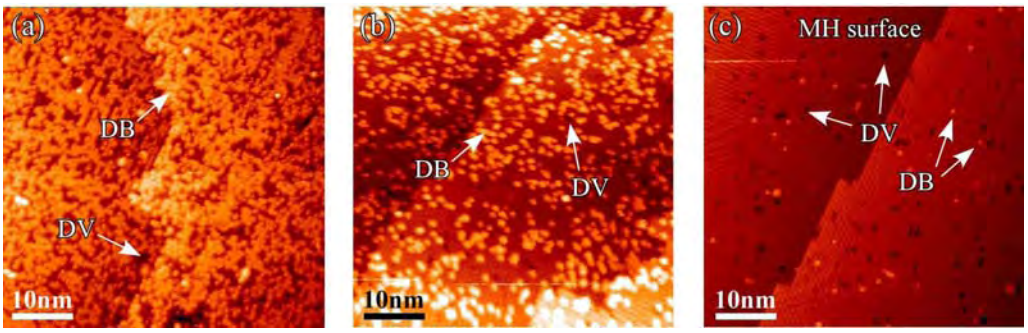

Figure 4.10: Hydrogen termination quality for various substrate temperatures.
(a) Partial hydrogen termination at a substrate temperature of 450 °C. The majority of the Si dimers are clean Si(100) surface, while the hydrogen terminated dimers appear as dark depressions. (b) Intermediate regime dosed at a temperature of 400°C. Single and double dangling bonds appear as bright protrusions. (c) Near perfect hydrogen termination at a substrate temperature of 350 °C. Only a few single dangling bond sites appear as bright protrusions; imaging conditions: V $\sim$ -2.0 V, I $\sim$ 0.2 nA.

follows that the formation of dihydrides is avoided when the substrate temperature is held within the dihydride desorption regime, i.e. between 350 °C – 450 °C. The upper substrate temperature limit is governed by monohydride desorption in the range from 450 °C – 650 °C. Therefore the ideal substrate temperature lies on the onset of dihydride formation around 350 °C. For substrate temperatures significantly higher than 380 °C, incomplete hydrogen passivation results in high dangling bond densities which eventually makes the surface unusable for the formation of controlled STM-patterns.

Since temperature control is crucial for optimally H-terminated surfaces, we performed a number of experiments to calibrate the optimal hydrogen passivation temperature for the STM-SEM/MBE system. Fig. 4.10 consists of a series of STM images of hydrogen terminated surfaces for different substrate temperatures. All Si:H(100) surfaces in this thesis were obtained by exposure to atomic hydrogen at a chamber pressure of $\sim 5 \cdot 10^{-6}$ mbar for $\sim$6 min. Such a dose of 135 Langmuir of atomic hydrogen was found to result in a monolayer coverage by a previous study performed in our group [51]. Fig. 4.10 (a) was prepared at a substrate temperature of $\sim$450 °C as measured by a calibrated K-type thermocouple close to the sample holder. The Si(100) is only covered with few monohydrides on the surface. Hydrogen passivation at a sample temperature of $\sim$400 °C [Fig. 4.10 (b)] yields a better terminated surface where single and double dangling bonds sites are seen as bright protrusions on the surface.

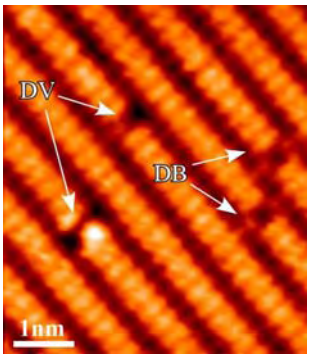

Figure 4.11: Atomic resolution image of a hydrogen terminated Si(100):H surface. Near perfect hydrogen terminated surface free of dangling bond sites. Two dihydrides can be seen in the right hand corner which occur when dosing at temperatures below 400 °C. Two single missing dimer defects are shown on the left hand side; imaging conditions: V ∼ -2.0 V, I ∼ 0.2 nA.

A near perfect hydrogen-terminated surface is shown in Fig. 4.10 (c) as a result of passivation at ∼350 °C. Only very few single dangling bonds are found on this surface and these are known to be practically inert to the adsorption of PH_3 molecules [66]. A high resolution image of a hydrogen surface which was prepared in this way is seen in Fig. 4.11. The image shows the presence of two dihydride units in the right hand corner, which is evidence that further attempts to decrease the single dangling bond density by reducing the substrate temperature would come at the cost of increasing the dihydride density on the surface. Therefore such a surface represents an optimal surface for subsequent formation of STM-defined atomic-scale lithography.

4.4.3 STM-based hydrogen lithography

In the following, we will discuss the method of STM-based hydrogen lithography for STM device fabrication. For this purpose, STM lithography parameters were optimised to achieve both, nano- and atomic-scale patterning of small device structures *and* micrometre-scale pattern formation used to form electrical contact to external four terminal leads. The use of electron stimulated desorption (ESD) of hydrogen from a monohydride surface using an STM tip was first reported by Becker *et al.* [9]. They found that by applying several volts to the STM tip, they could promote electrons to the anti-bonding level of the Si:H bond, thereby desorbing hydrogen from the surface. Snow *et al.* [10] performed the first STM-stimulated hydrogen desorption experiments on the Si(100):H surface immediately followed by the well-known work of Lyding,

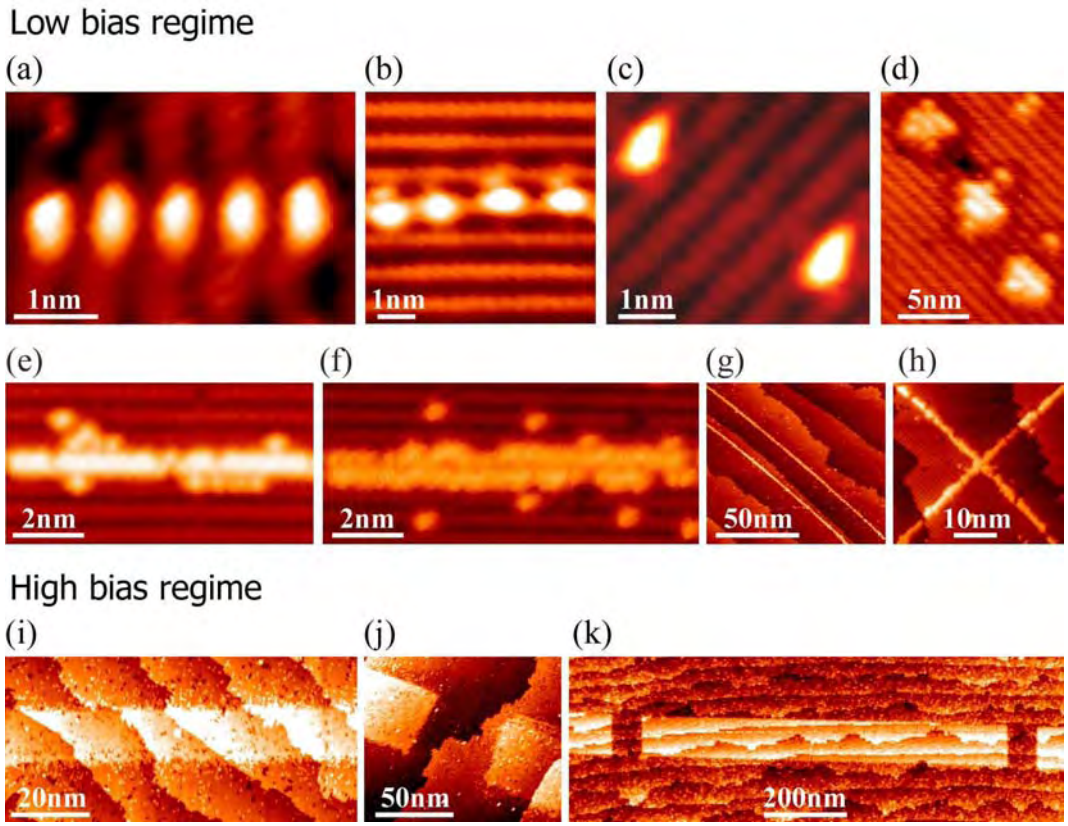

Figure 4.12: Atomic- and nano-scale STM lithography created in this work employing different bias regimes. *Low bias regime [2V – 5.5V]*: Creation of single dangling bond adsorption sites perpendicular (a) and parallel (b) to Si dimer rows. Single (c) and few (d) dangling bond sites. Single (e) and double (f) Si dimer row atomic wire pattern. (g) Two parallel (g) and perpendicular (h) atomic wires. *High bias regime [>6V]*: (i) 15 nm wide nano-scale wire pattern. (j) 40 nm wide wire with a 40 nm wide tunnelling gap. (h) single electron transistor pattern showing two 50 nm wide tunnelling junctions and a 100 nm wide and 800 nm long island. Imaging conditions: V∼-2 V, I ∼0.2 nA.

Shen, Tucker and others [11], [12]. In 1995, Shen *et al.* [12] identified two different mechanisms separated by two different voltage regimes by which STM-stimulated hydrogen desorption occurs on the surface. The first desorption mechanism occurs by excitation of the Si:H bond originating from vibrational heating of the lattice by tunnelling electrons. This occurs at sample biases between +2 V and +5.5 V (*low voltage regime*), where inelastic tunnelling processes excite the vibrational mode of the Si:H bond. Multiple excitations (from a number of electrons) eventually lead to desorption of the hydrogen atom. The second hydrogen desorption mechanism occurs at higher sample bias above +6 V (*high voltage regime*), where electrons emitted from the STM

tip have sufficient energy to directly excite the σ bond between the Si and H atom. For the fabrication of STM devices, we choose between the two regimes depending on the particular pattern size and structure. The low voltage desorption mechanism is used for the removal of individual hydrogen atoms allowing the formation of truly atomic-scale devices. Fig. 4.12 (a,b) illustrate our capability using this technique for the selective removal of *single* hydrogen atoms. By increasing the number of electrons emitted from the STM tip with increasing current, dots of few missing hydrogen atoms can be created as seen in Fig. 4.12 (c,d). Atomic wires of single [Fig. 4.12 (e)] and double Si dimer [Fig. 4.12 (f)] linewidths are also possible. Figure 4.12 also shows the lithographic precision when combining two atomic wires patterned parallel (g) and perpendicular (h) to each other. All lithographic patterns in Fig. 4.12 (a) – (h) were obtained by using a sample bias of 4 V and 1 nA, except in (d) where 2 nA was used. Fig. 4.12 also demonstrates examples of nano-scale patterning using the *high voltage* desorption regime at a sample bias of 7 V and 3 nA. Specifically, a 15 nm wide wire (i), a 40 nm wide wire with a 40 nm tunnelling gap (j) and an SET structure (k) are shown. Using this mechanism generally achieves complete hydrogen desorption in the lithographic area at the cost of an increased number of stray dangling bonds created at the pattern boundaries. This can readily be seen in Fig. 4.12 (i).

One of the ultimate challenges in the device formation process is to maintain a hydrogen desorption efficiency close to 100% for the formation of large, micrometre-scale lithographic patches which are used to contact the nano-scale or atomic-scale device to the outside world. Since the device fabrication process is very long, it is desirable to achieve complete hydrogen desorption of micrometre scale structures in a minimal amount of time. We performed an initial large scale desorption optimisation study based on the variation of the following parameters:

STM tip bias and tunnelling current: Both higher tip bias and higher tip current increase desorption efficiency. Higher tip bias tends to increase the lithographic width but also introduces more stray electrons. Higher tip current increases electron dose. Both high bias and currents require a highly stable tip.

Scan line spacing: The horizontal and vertical scan line spacing is adjusted by the number of data points taken in the horizontal and vertical scan direction at a given scan frame.

Scan velocity: Adjusting the scan velocity provides a means of adjusting the electron

dose. Smaller velocities increase desorption efficiency but become impractical for large scale lithography.

Fig. 4.13 (a,b) show the difference in hydrogen desorption efficiency for a 100 nm wide patch and a 2 μm wide patch for the same desorption parameters. Due the larger scan frame, the scan line spacing with the same number of scan points increases from initially 0.25 nm to 5 nm. Increasing STM bias and tunnelling current from 5 V and 2 nA [Fig. 4.13 (c)] to 6 V and 4 nA [Fig. 4.13 (d)] does not increase the lithographic linewidth sufficiently to compensate for the increased line spacing thus hydrogen desorption is not improved significantly in the large patch. Decreasing the linewidth from 5 nm to 2.5 nm (by doubling the number of scan points) almost completely removes the hydrogen from the surface with some hydrogen (black depressions) still present on the surface. For these lithographic parameters (6 V, 4 nA), we observe a lithographic linewidth of 4 nm [Fig. 4.13 (e)] in agreement with previous reports in the literature [142]. Combining a linewidth of 2.5 nm with increased lithographic parameters (6 V, 4 nA) leads to near complete hydrogen desorption as seen in Fig. 4.13 (f,g). A critical issue with increasing the number of scan points (in vertical and horizontal scan direction) is, that it increases the scan time *quadratically*, whereas increasing the scan velocity lowers the scan time only linearly. Soukiassian *et al.* [143] found that the number of desorbed hydrogen atoms per emitted electron is constant up to a scan speed of 800 $\frac{nm}{s}$ but falls dramatically above this value. As a consequence, we have initially chosen a scan speed of 700 $\frac{nm}{s}$ in our experiments in conjunction with an STM bias of 6 V and a tunnelling current of 4 nA. The desorption time for a 2.5 μm $\times$ 2.5 μm large lithographic contact patch is about 3 h using the latter parameters. For highly stable tips we have gone on to increase the STM bias voltage a bit further to 7.5 V while decreasing the tunnelling current to 3 nA. Using these parameters, we further improve the desorption efficiency as shown in Fig. 4.13 (h). More recently [144], we investigated large scale desorption at higher scan speeds up to 4000 $\frac{nm}{s}$ (STM tip bias of 7.5 V and tunnelling current of 3 nA) which was found to be sufficient to incorporate the maximum number of P dopants into the Si layer determined from Hall measurements of STM-patterned Van-der-Pauw type devices. This means that large scale contact patches with similar structural quality can be desorbed in 20 % of the time ($\sim$ 30 min for a 2.5 μm $\times$ 2.5 μm large square) – an important improvement of the device fabrication process.

We have seen that by adjusting the STM tip voltage and current and the scan line

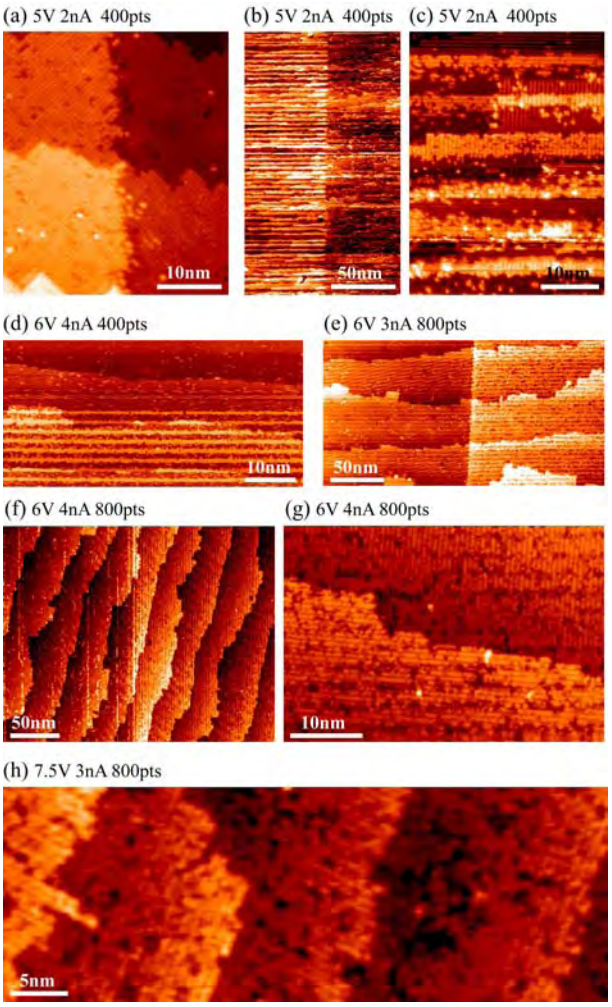

Figure 4.13: Micrometre-scale STM lithography for buried device contacts. Dependence of STM lithography on scan size, tunnelling voltage and tunnelling current and scan line spacing. Comparison between nano-scale lithography (a) with a scan line spacing of 2.5 nm and (b,c) 2 μm large lithography with a scan line spacing of 5 nm. (d) Increasing the single line lithographic wire width to 4 nm. (e) Decreasing the scan line spacing to 2.5 nm. (f) Combination of (d) and (e) leads to near complete hydrogen resist removal for large scale desorption as can be seen in (g). (h) Increasing the desorption voltage to 7.5 V increases hydrogen desorption efficiency further. Imaging conditions: V $\sim$ -2.2 V, I $\sim$ 0.2 nA.

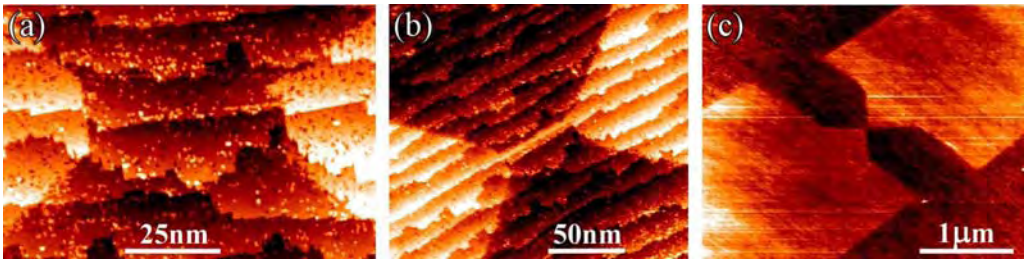

Figure 4.14: Multi-step STM lithography for atomic wire device formation. (a) Initially, nano-scale lithography is used to create two triangular patterns with a 50 nm wide tunnelling gap. (b) Thereafter, a single atomic wire, 3 nm wide and 50 nm long is patterned. (c) In a third step, the device pattern is completed by the formation of micrometre-scale contact patches, 2 μm $\times$ 2 μm in size. Imaging conditions: V$\sim$-2 V, I$\sim$0.15 nA.

spacing, STM-based hydrogen desorption is tunable to perform lithography from the micrometre-scale down to the atomic-scale. It is worth noting that the exact correlation between linewidth, bias voltage and tunnelling current is still tip dependent. This means, that the desorption parameters have to be slightly optimised for each STM tip individually.

Performing STM lithography at various length scales is an important prerequisite for our device fabrication process. Fig. 4.14 nicely illustrates, for each device pattern, the combination of STM lithography at the various length scales. Here the multi step procedure for the fabrication of an atomic wire pattern is shown. Initially the STM tip is centred in between the registration markers using the SEM. By using a script-based pattern generator provided with the *Omicron Scala* STM software, any desired two dimensional device layout can be patterned into the hydrogen resist. In this case, we chose to write two opposing triangles with a base line of 150 nm separated by 50 nm as shown in Fig. 4.14 (a). Using a smaller STM scan frame, we precisely place a single atomic wire with a width of 3 nm and perfect alignment parallel to the Si dimer rows between the two triangles. For both lithographic structures so far, we used an STM voltage of 6 V and a current of 4 nA. Micrometre-scale contact pads are then aligned to each triangle in a subsequent step. An STM image shown in Fig. 4.14 (c) confirms the successful large area pattern written with the higher STM voltage of 7.5 V at a current of $\sim$3 nA. The rationale behind the three step process is that STM pattern alignment accuracy depends on the scan size. One major factor of misalignment is the piezo drift induced in the STM scanner. Since the absolute misalignment is related to the scan frame size, small structures are best aligned using small scan frames. The use

of intermediate scale features (in this case the two triangles) allows us to relocate the small structures in larger scan frames so that we can make an interconnect between micrometre-scale and nano-scale patterns. The micrometre-scale contact pads themselves are subsequently aligned using SEM-assisted STM tip positioning with respect to the registration markers.

The preparation of a *stable* STM tip is essential for a reliable STM lithography process and the main factor governing device yield. *Stable* means that the tip shape and the robustness of the tunnelling junction, formed between STM tip and silicon substrate, is relatively insensitive towards bias voltage changes ranging from -2 V to +8 V as well as tunnelling current changes from 0.1 nA – 4 nA. Stability over such a wide range of imaging conditions is necessary to switch from normal STM imaging to STM lithography.

4.4.4 Adsorption of PH_3 molecules and P atom incorporation

In this thesis we have pursued the use of phosphine gas (PH_3) as the dopant source for Si:P dopant devices since the selective adsorption of phosphine molecules on dangling bond sites has been demonstrated in our group [19]. The interaction of PH_3 with the Si(100) surface has been studied intensively for almost two decades [51], [145], [146], [147], [148], [149], [150]. It is widely known (for example [145]), that PH_3 adsorbs on the highly reactive, bare Si(100) surface with a sticking coefficient approaching unity. At room temperature, the adsorption process of PH_3 is accompanied by the dissociation of the molecule on the surface into PH_x species. The identification of the various species that occur after surface exposure to PH_3 has been the subject of research by a number of groups. Whilst contradictive reports exist, the most recent and arguably the most complete interpretation [151] suggests, that the three main species are to be identified as PH_2, PH and P. Whilst the individual dissociation pathways are governed by the complexity of the underlying molecular energetics, the average density of P atoms, stemming from this self-arranged assembly, saturates after a certain dose of PH_3. Surface exposure to phosphine at the *saturation dose* yields $2.5 \cdot 10^{14}$ cm^{-2} of P containing molecules. Given the density of Si atoms on the Si(100) surface, namely $6.78 \cdot 10^{14}$ cm^{-2}, this P coverage is equivalent to 0.37 monolayer (ML) [150]. STM studies, performed in our group [32], have shown that this saturation value is due to a two-fold, self-terminating mixture of phosphine species ordering, namely a $c(4\times2)$ periodicity corresponding to 0.25 ML coverage and a $p(2\times2)$ periodicity, correspond-

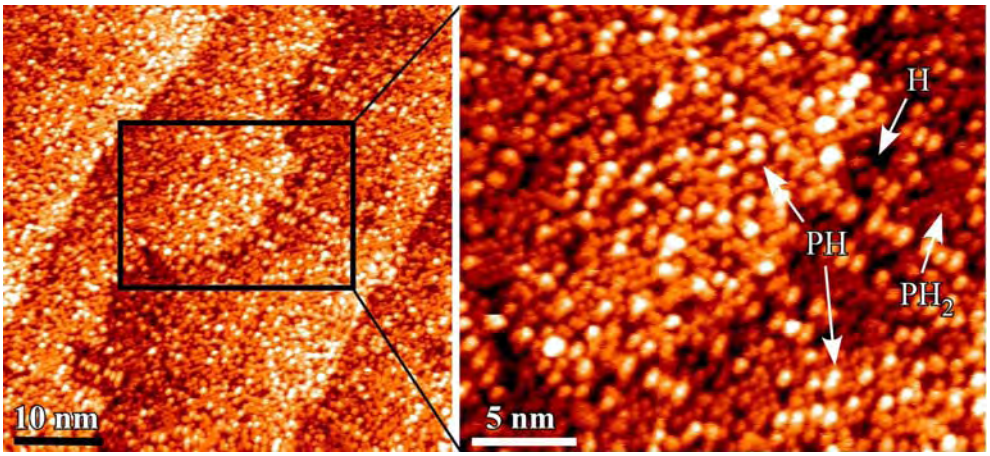

Figure 4.15: Molecular species on Si(100) after exposure to a saturation dose of PH_3. STM images of the bare Si(100) surface after a saturation dose of phosphine. *Inset:* A high resolution STM image shows the $p(2\times2)$ arrangement of PH_2 and PH which orders with a $c(4\times2)$ periodicity. The black depressions are hydrogen arising from the PH_3 dissociation process. Imaging conditions: V∼-2 V, I∼0.15 nA.

ing to 0.5 ML coverage. Recently [151], these two phosphine species were identified as PH and PH_2 respectively. Fig. 4.15 shows the Si(100) surface after exposure to a saturation dose of PH_3. For our combined SEM-STM/MBE system with a base pressure of $9 \cdot 10^{-11}$ mbar, the saturation dose point was identified to be the exposure of PH_3 gas to the surface at a chamber pressure of $1.1 \cdot 10^{-9}$ mbar for 15 min, corresponding to 0.74 Langmuir (L). The interaction complexity can readily be seen by the occurrence of various species on the surface. Atomic resolution STM imaging allows the identification of the dominant dissociation species according to the interpretation of Wilson *et al.* [151]. It can clearly be seen that PH_2 orders with a $p(2\times2)$ periodicity. The bright protrusions, centred over the Si dimer, is PH. Its $c(4\times2)$ ordering is less obvious since it is less abundant on the surface. The dark depressions which can be seen across the surface comes from hydrogen left over from the PH_3 dissociation process.

The usability of phosphine for the fabrication of devices patterned by hydrogen-based STM lithography relies on two important findings. The first is, that PH_3 molecules selectively adsorb only on the reactive, exposed silicon area of the patterned surface [19]. The surrounding, non-reactive H-terminated surface blocks the adsorption PH_3 thus acting truly as a resist. This enables the formation of controlled adsorption regions of PH_3 molecules on the Si surface using STM lithography which can readily be confirmed from Fig. 4.16. Here, STM lithography was used to desorb a patch from a

hydrogen-terminated surface, thereby exposing the underlying Si(100) surface. After a saturation dose of PH_3 in the preparation chamber, the lithographic area is relocated using the SEM in combination with the registration markers. The surface structure in the patch area shown in Fig. 4.16 looks essentially the same as the bare Si(100) surface shown in Fig. 4.15. The sharp lithographic boundary stays intact during the PH_3 adsorption process. The atomic resolution image [Fig. 4.16 (inset)] also demonstrates that no phosphine has adsorbed to single dangling bonds (DB). This is important, since the presence of DB cannot be entirely avoided due to incomplete hydrogen termination or stray removal of hydrogen atoms during the lithographic process.

The second finding is that the P atom from the adsorbed P-containing species can be thermally incorporated into the top layer of the silicon surface [32]. The incorporation process provides stronger bonding as three covalent bonds are formed between the P atoms and the silicon surface and therefore minimises phosphorus diffusion and segregation in subsequent processing steps. X-ray photoemission (XPS) spectroscopy studies on the bare (unpatterned) silicon surface [145], [150] have shown that the P atom density after subsequent annealing over a temperature range between 450 °C and 625 °C is constant, namely 0.25 ML or $1.7 \cdot 10^{14}$ cm^{-2}. This implies that some PH_3 molecules from the 0.37 ML coverage obtained by phosphine exposure at room temperature desorb recombinatively. At 625 °C, phosphorus starts to desorb from the Si(100) surface and is found to be completely removed at a temperature of 825 °C [150]. Schofield *et al.* [32] optimised the P incorporation process for Si(100):H surfaces patterned by STM-based hydrogen lithography. By carefully annealing the silicon surface to ∼350 °C, P is incorporated into the silicon surface whereas the surrounding hydrogen resist remains unchanged. This optimised process has allowed the placement of individual P dopants within an unprecedented accuracy of ∼1 nm [32]. The importance of this step is, that P dopants are incorporated into the silicon surface without disrupting the integrity of the hydrogen resist – thus allowing precise dopant patterning. Once the P atoms are sitting on a Si crystal site, they are less like to move/diffuse due to the covalent bonds they have formed with the surrounding silicon atoms. The use of registration markers allows us to easily observe the same area of the surface, shown in Fig. 4.16, after the incorporation anneal at 350 °C using the electron beam heater in the preparation chamber. Fig. 4.17 clearly demonstrates that the boundary between the hydrogen resist and the P atom structure remains unchanged. Whilst the incorporated P atoms are difficult to observe on the surface due to the appearance of

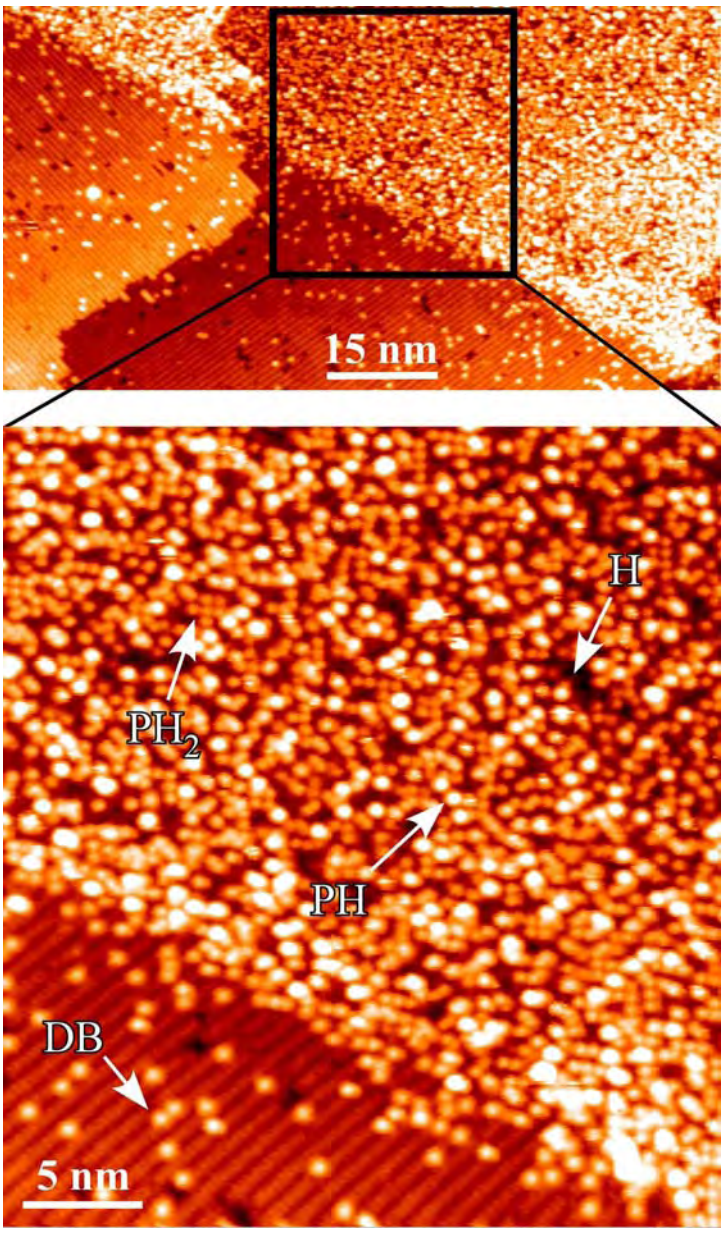

Figure 4.16: Filled state STM images of phosphine adsorption on a lithographically patterned hydrogen passivated Si(100):H surface. The sharp boundary created by STM lithography between the hydrogen-terminated surface and the hydrogen-depassivated area allows selective PH_3 adsorption. A high-resolution STM image (inset) allows identification [151] of PH_2, PH and H. Importantly, no adsorption of PH_3 molecules on single dangling bonds (DB) is observed. Imaging conditions: V∼-2 V, I∼0.15 nA.

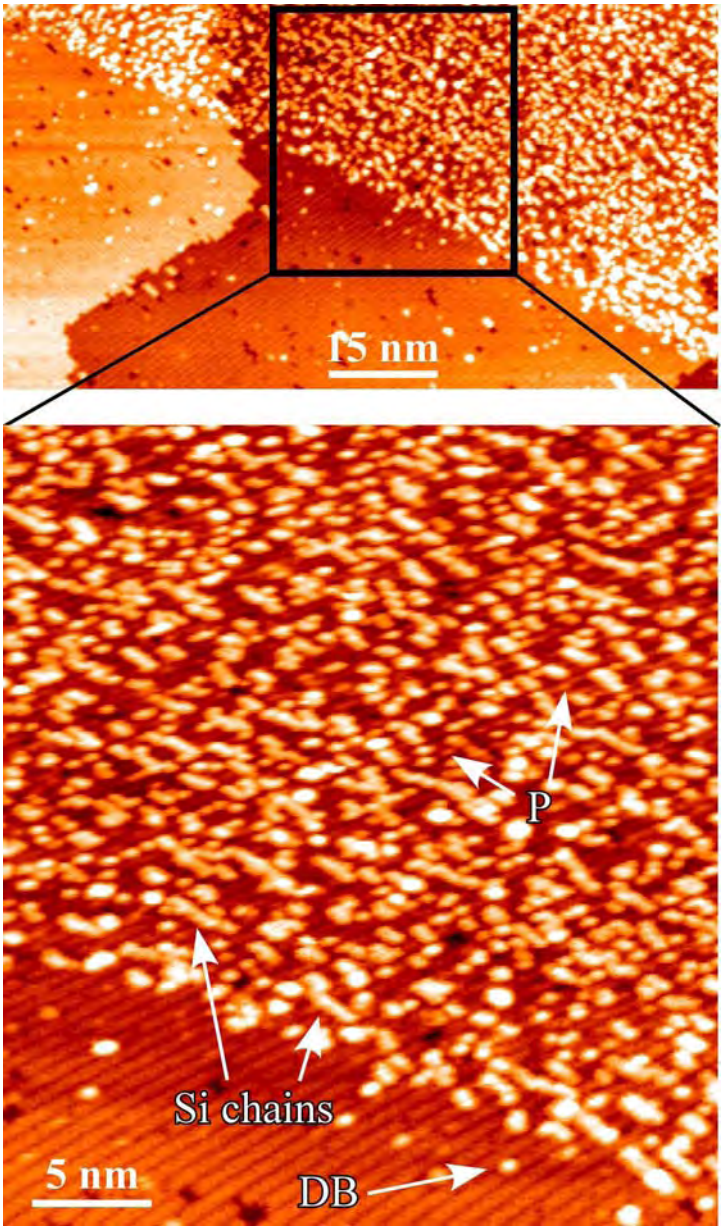

Figure 4.17: Filled state STM images of phosphorus incorporation on the patterned Si:H(100) surface. Thermal incorporation of P atoms into the top Si(100) layer at a temperature of $\sim$ 350 °C. Importantly, the hydrogen resist stays intact. A high-resolution STM image (inset) shows ejected Si dimer chains on the surface. The incorporated P atoms are still visible but obscured by the ejected Si chains. Imaging conditions: V$\sim$-2 V, I$\sim$0.15 nA.

Si chains (with a geometric height increase of 0.14 Å) stemming from Si ejected during the P incorporation process, we know from high resolution STM images that they are there [32]. The occurrence of ejected Si dimers on the surface accompanied with P incorporation was first reported by Lin *et al.* [150]. Parts of the lithographic region around the Si chains appear identical to the surrounding hydrogen resist. The reason for this is partial re-termination of the desorption area by hydrogen atoms coming from the PH_x species.

4.4.5 Thermal hydrogen resist removal

Previous studies of Si epitaxial growth [152], [153], [154] have shown that the presence of hydrogen on the initial surface can deteriorate the Si growth quality. Hydrogen atoms are known to hinder Si surface diffusion which results in inferior epitaxial growth as compared to the clean Si surface. It is desirable to maximise the silicon growth quality by completely removing the hydrogen resist layer from the patterned Si(100):H surface. Prior to device encapsulation, P incorporation is an essential step to ensure dopant pattern integrity during the hydrogen removal step. Hallam *et al.* [67] have shown that thermal hydrogen resist removal is achieved by carefully heating a patterned surface to $\sim$470 °C. It has been shown that the desorption process is a result of a recombinative interdimer mechanism [68], in which two hydrogen atoms from adjacent dimers combine and desorb from the surface as H_2. The pairing of hydrogen to desorb via this pathway arises from an attractive force between hydrogen atoms on the surface [155] leading to a rearrangement of H atoms into a desorption configuration at elevated temperatures due to the low activation barrier for interdimer diffusion [156]. Fig. 4.18 shows a patterned P-dopant area surface after the hydrogen removal step. While some residual hydrogen is still present on the surface, it is important that the P dopant structure maintains its integrity. The two annealing steps for P incorporation and hydrogen resist removal may also be combined by heating the silicon sample controllably to 470 °C for 10 – 60 s. Initially the phosphorus atoms incorporate from the PH_3 dissociation products, PH and PH_2, into the top Si layer at a temperature of $\sim$350 °C. Subsequently, the hydrogen resist is removed from the surface at a temperature of 470 °C. Fig. 4.18 shows that such a process preserves the carefully created STM-patterned P-dopant structure and provides a high quality surface for subsequent epitaxial overgrowth.

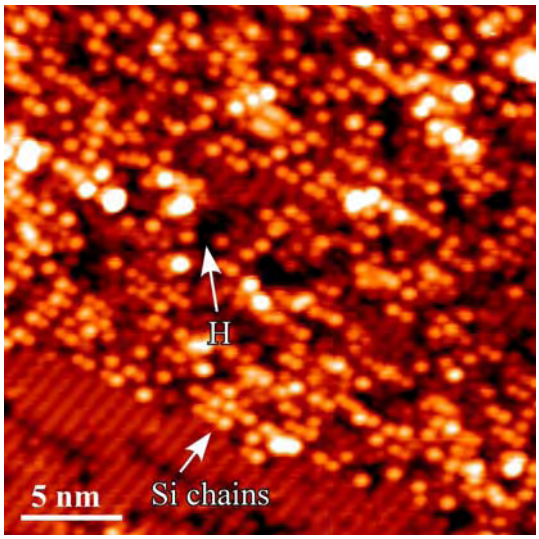

Figure 4.18: Filled state STM images of thermal desorption of the hydrogen resist. Annealing the surface to 470 °C desorbs the hydrogen resist, whereas the P dopant structure maintains its integrity. Imaging conditions: V∼-1.6 V, I∼0.15 nA.

4.4.6 Encapsulation of P dopant structures with epitaxial Si

The final UHV device fabrication step is to encapsulate the patterned phosphorus device structure with epitaxially grown silicon. This fulfills a number of purposes. Firstly, one can move the conducing layer away from complex surface states and residual surface defects which can have significant influence on the electrical properties of devices. Secondly, the robustness of the patterned structure is greatly enhanced by protectively burying it avoiding ambient exposure and potential contamination. Thirdly, by incorporating the P atoms into the silicon bulk, it donates its excess electron to contribute to conduction, thus electrically activating the P dopant.

The latter advantages come at the price of having to find a high-quality Si encapsulation process which preserves the underlying dopant structure. Generally, high-quality silicon epitaxy is achieved at elevated growth temperatures of ∼650 °C due to thermally activated Si surface migration. At these high temperatures however, the P atoms are also subject to surface segregation [157] and thermally activated diffusion [158]. Lowering the growth temperature results in sub-optimal crystal quality, since less Si migration takes place, increasing the residual defect density, which is a known mechanism to contribute to dopant diffusion [159]. It is worth noting, that the abundance of P atom in the top silicon layer can also adversely affect the epitaxial thickness

further contributing to a decreased growth quality. As can already be seen from this brief discussion, the silicon encapsulation process is ultimately a compromise between dopant structure integrity and crystal quality.

At low temperatures, Eaglesham *et al.* [152] found that Si deposition on Si(100) is only epitaxial up to a certain layer thickness. For a growth rate of 0.7 $\frac{\mathring{A}}{s}$, the critical thickness was found to be 30 nm for a growth temperature of 250 °C [160]. Beyond this critical thickness, a crystalline-amorphous transition occurs and surface quality deteriorates. They also studied the qualitative effect of hydrogen on Si growth and suggested that hydrogen suppresses Si surface diffusion, thereby increasing surface roughness. This assumption is substantiated since the activation energy for Si diffusion on the hydrogen-terminated surface [161] increases from 0.6 eV and 1.0 eV on the bare Si(100) surface [162] to 1.5 eV and 1.7 eV along and perpendicular to the Si dimer row direction respectively. Oberbeck *et al.* [153] compared the surface quality after growth of a few monolayers of Si at a temperature of 250 °C on a bare Si surface and on a hydrogen-terminated surface. Using atomic resolution STM imaging, it was found that the surface roughness is increased on the hydrogen-terminated surface also doubling the density of surface defects. A recent STM study [154] showed that hydrogen significantly segregates to the surface during Si growth thus staying as a surfactant to inhibit Si diffusion during the entire growth process. All of these studies suggest that the hydrogen resist is detrimental to the Si growth quality and should therefore be removed as indicated in the previous section. Fig. 4.19 (a) shows an STM image of a device sample after hydrogen removal and subsequent encapsulation with a few monolayers (ML) of epitaxial silicon at a temperature of 250 °C using a growth rate of 0.5 $\frac{\mathring{A}}{s}$. Note that the silicon encapsulation step was conducted by the research fellow responsible for MBE in our group, Dr. Lars Oberbeck. Two-dimensional growth of epitaxial Si where the Si atoms conform to the underlying terrace structure is seen. After further encapsulation to an epitaxial layer thickness of 25 nm, the Si growth mode changes towards the growth of three dimensional Si islands although we can see for this thickness, the silicon is still epitaxial. Si device encapsulation is the last step in the UHV STM device fabrication process. After the growth, the sample is removed from the UHV system for the alignment of four terminal metal contacts to the buried P dopant device.

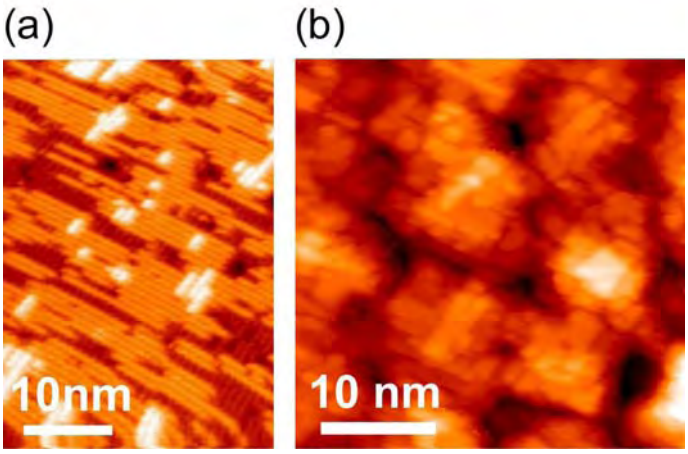

Figure 4.19: Low temperature epitaxial Si growth for device encapsulation. Filled state STM images of homoepitaxial Si growth. (a) Two dimensional growth quality after a few initial monolayers (ML) at 250 °C. (b) Surface morphology towards three dimensional islands after growth of 25 nm at 250 °C. Imaging conditions: V∼-2 V, I∼0.15 nA.

4.4.7 Electrical activation of P dopants

A practical obstacle for the fabrication of functional atom-scale electronic devices is their sensitivity towards surface states, interface states, charged and/or spin defects [163], [25]. A natural way to circumvent this problems is to encapsulate the patterned dopants in high quality, epitaxial silicon thereby minimising these effects. A challenge regarding the encapsulation process is to overgrow and incorporate the dopants whilst limiting dopant redistribution by thermally activated dopant surface segregation or diffusion. Shallow donor and acceptor atoms in silicon exhibit large Bohr radii of 3 nm [163]. Dopant wavefunctions will therefore overlap at separation distances of ∼10 nm. Carrier freeze-out does not occur down to doping densities of $\sim 10^{12}$ cm^{-2}, which corresponds to one dopant per 10 nm^2 area. δ-doped layers of Si:P provide a useful testbed for the systematic study of key device parameters such as dopant density, electron mobility and electron phase coherence length. A δ-doped layer is essentially a thin 2D sheet of dopant atoms incorporated at substitutional lattice sites in the silicon lattice vertically confined to act as a two-dimensional electron system. Recently, a few research groups have performed systematic studies on δ-doped layers to determine important device parameters using Hall measurements [137], weak localisation measurements in parallel [164] and perpendicular magnetic fields [137], [138], [164], SIMS [137], [138] and STM characterisation [137], [165].

What are the criteria to find the optimal temperature window for the encapsulation of functional STM-patterned P dopant devices? A perhaps obvious criterium is the electrical activation of the P dopants. By measuring the dopant density at various Si growth encapsulation temperatures, it is possible to determine the appropriate Si growth temperature to achieve the maximum number of electrically active P dopants. Another criterium is the electron mean free path l or the electron mobility μ. The electron mean free path is correlated to the structural quality of its environment, that is the presence of defects and dislocations that can disrupt the crystal symmetry which decreases the electron mean free path. Another measure for structural quality is the electron phase coherence length. Inelastic collisions related to defects, traps and crystal imperfections influence the magnitude of the electron phase coherence length.

P δ-doped layer studies in our group by Goh et al. [138], [166] showed that an encapsulation temperature of $\sim$250 °C gives full electrical dopant activation equivalent to the maximum achievable carrier density of $1.7 \cdot 10^{14}$ cm^{-2}. Encapsulation at $\sim$250 °C also maximises the electron mobility, μ, of $\sim$40 $\frac{cm^2}{Vs}$ and the phase coherence length, l_φ, of $\sim$70 nm with minimal P diffussion/segregation. More recently, our group [167] has shown that complete electrical activation of the P dopants can still be achieved in Si:P δ-doped layers despite the presence of hydrogen on the Si(100) surface. However electron mobilities are reduced by a factor of three attributed to the lower surface quality.

Initially, we have adopted an encapsulation scheme at 250 °C for the fabrication of STM-patterned devices after the *removal* of the hydrogen resist layer. However, for fabrication of ultrathin Si:P wires, we have encapsulated immediately after the P incorporation anneal at $\sim$350 °C (i.e. without hydrogen removal) for minimal P diffusion. Results from functional STM-patterned devices show complete electrical activation confirming the findings from P δ-doped layers fabricated in our group. A more detailed comparison of the electrical results of P-δ doped layers from various groups with those obtained from STM-patterned devices is given in Chapter 5.

4.4.8 Alignment of surface contacts to buried Si:P devices

The alignment of surface contacts outside the UHV system relies on the use of the etched registration markers. The metal contacts patterns were designed on the same optical mask to match with the registration marker pattern. A variety of two terminal and four terminal contact structures differing in contact spacing are available

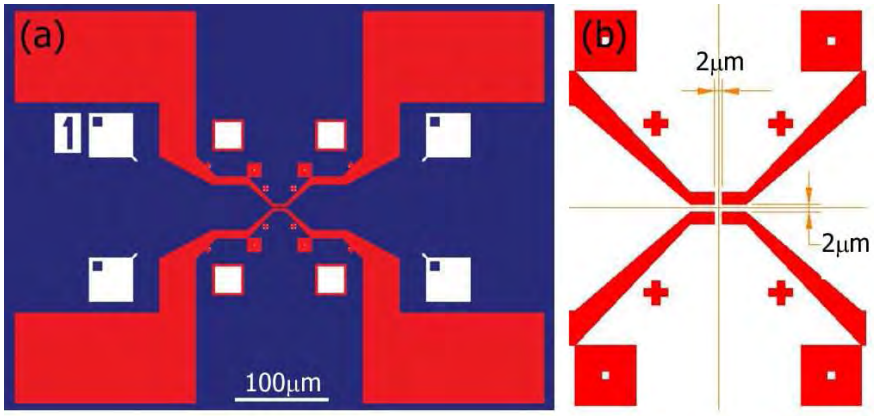

Figure 4.20: Four terminal contact mask pattern. (a) Four terminal contacts designed to match to registration markers for pattern alignment. (b) Central area where contact leads connect to buried Si:P device structures.

to suit multiple STM device designs. The optical mask for contact and registration marker patterns consists of a combined dark- and clear- field design. The dark field area is used for the fabrication of registration markers down to a size of 1 μm. For easier alignment navigation, the contact structures were placed on the clear field area. Two terminal contact structures with horizontal separations of 2, 3, 4 and 6 μm and four terminal structures with the same horizontal separations and respective vertical separation variations of 2, 3 and 5 μm are available. Contact structures with small separation values were placed closer to the centre of the mask where contact between mask and sample is maximal and therefore pattern resolution is best. The complete mask design spanned over an area of 4×4 cm^2. All devices presented in this thesis were contacted using a four terminal device structure with a nominal spacing of 2 μm between contacts forming a Van-der-Pauw square type configuration, thereby eliminating difficulties arising from unknown contact resistance in the electrical measurements. Therefore, the focus of this section will be on this particular geometry but the fabrication details holds true for all contact pattern designs.

Fig. 4.20 (a) shows the mask for the contact pattern which has been designed to match the registration marker pattern. The exact contact structure, as located on the mask, is pictured in red colour, whereas the markers are white in colour. Optical microscope images of actual devices are presented later on in Fig. 4.21. A blow-up of the four terminal contact structure is given in Fig. 4.20 (b) having a separation of 2 μm in both, vertical and horizontal direction. The STM-fabricated device is located

in the centre between the four leads. The area of the metal contacts (100×200 μm^2 in size) were designed to allow for multiple bonding attempts using a conventional ball bonder.

The patterned region on a 1×1 cm^2 sample consists of nine sets of registration markers ordered in a 3×3 array spread over a 5×5 mm^2 area around the centre of the sample. Fig. 4.21 (a) shows the array of nine possible devices that can be fabricated simultaneously on one chip. The best alignment accuracy between the metal contacts and the registration markers, using the in-house optical lithography facility, is of order $\sim$500 nm over the entire area of 5×5 mm^2. Individual device alignment however can be as good as 100 nm [see Fig. 4.21 (d)]. The alignment between registration markers and STM-patterned devices on the other hand is of order 100 nm. Since the devices fabricated in this thesis allows us to define micrometre-sized buried conducting areas using STM lithography, overall alignment within $\sim$500 nm is sufficient for contacting multiple devices individually on the same chip. It is important to note that the smallest feature size for devices, patterned with the STM between the patches, can still be on the atomic scale.

We now discuss the various stages of the metal contact fabrication process. After removal from the UHV system, the sample undergoes a dehydration bake at $\sim$200 °C for at least 30 min. Before spin-on of $\sim$1 μm thick resist AZ5214E, the chip is spin coated with the resist adhesion promoter HMDS. After a 5 min pre-exposure resist bake at 95 °C, the sample is ready for contact pattern alignment using optical lithography. To alleviate the alignment process, the contact patterns are placed on the light-field area of the mask which facilitate sample navigation. This implies that the resist, AZ5214E, is used in the positive resist mode. Using the Quintel Q6000 aligner in vacuum contact mode, the pattern is transferred from the mask to the resist using a light intensity of 12 – 14 $\frac{mW}{cm^2}$ using an exposure time of 0.8 s. Both, a reversal bake and a subsequent *flood exposure* at the same light intensity for 90 s transforms AZ5214E from a negative to a positive resist. Resist development takes place in a bath of AZ300 MIF for 90 s. Fig. 4.21 shows the central part of a device after development of the resist structure representing the level of alignment achievable between the registration markers and the contact structure. The smallest, $\sim$1 μm wide registration markers provide a measure of alignment accuracy which is of order 100 nm.

After development, a O_2 plasma ash is performed for further residual resist removal in the exposed area. Before the sample is metallised using a high-vacuum

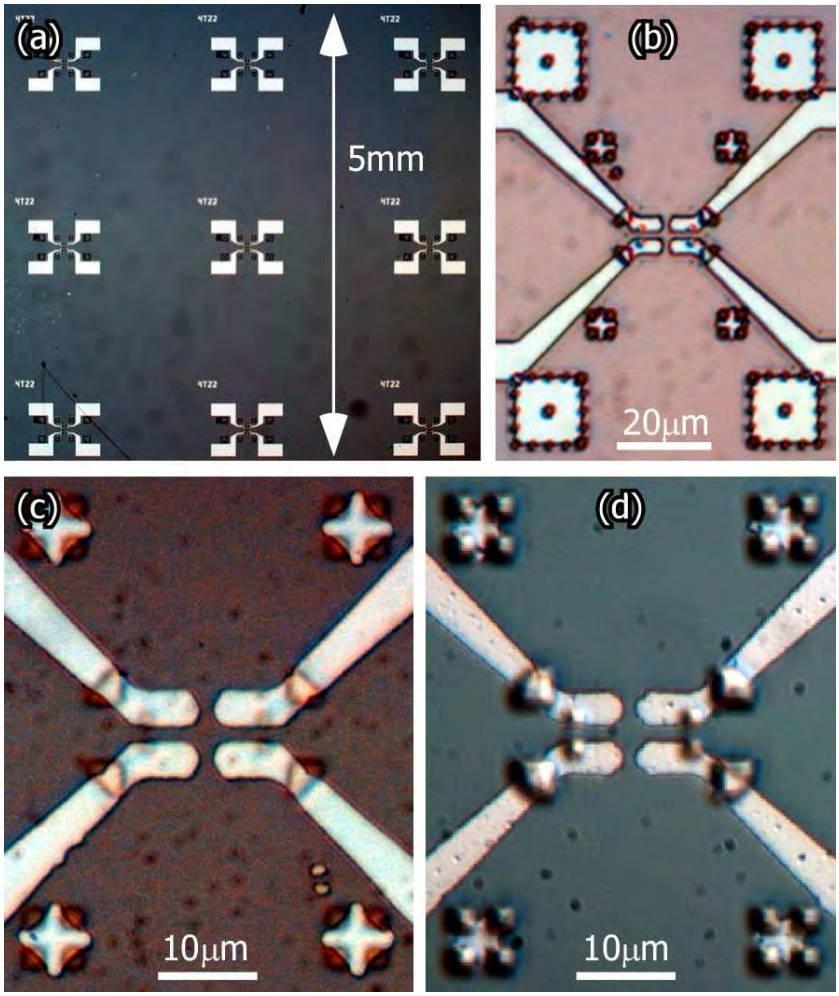

Figure 4.21: Contact alignment for STM-fabricated devices. Optical microscope images of (a) a complete set of nine devices on one chip, (b) central device region after resist development (c) subsequent Al metallisation and (d) contact annealing to 350 °C for 15 min. The blurry bubbles in (c,d) stem from dust particles on the highest magnification lens of the microscope and are not present on the sample surface.

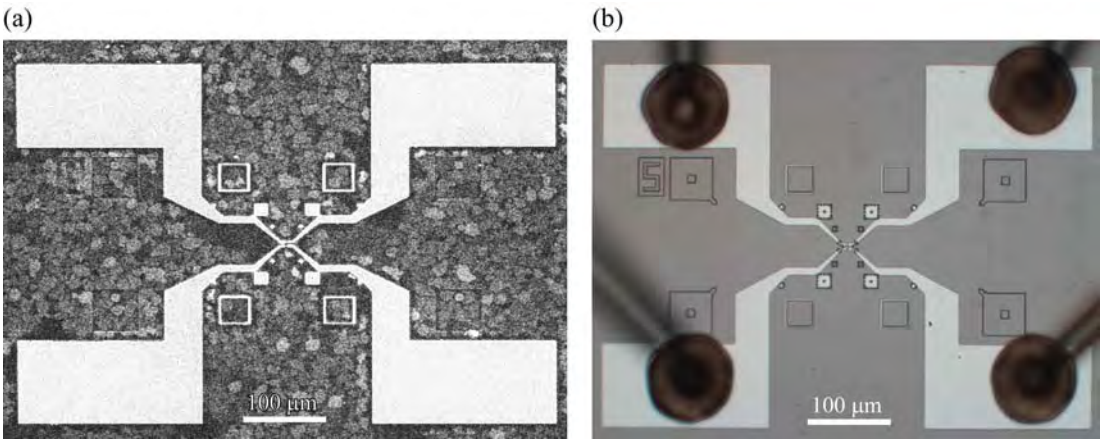

Figure 4.22: Contacted STM-patterned device. (a) SEM image of final device. (b) Optical microscope image of the complete device after gold ball bonding.

e-beam evaporator, the native SiO_2 layer is removed in a HF bath. We evaporate a 300 nm thick layer of 5N (99.999 %) purity Al as the metal contact material. Metal lift-off in the non-patterned areas occurs in an acetone bath followed by IPA and DI water rinse. The four terminal, metallised contact pattern is shown in Fig. 4.21 (c). Ohmic contacts to the buried Si:P device is formed during a heating step in a N_2 atmosphere at 350 °C for 15 min in which the aluminium diffuses [168] to the buried STM-fabricated P-doped contact pads. The Al spikes down and creates tiny holes on the metal surface which can be observed using a standard optical microscope as shown in Fig. 4.21 (d). The chip is finally cleaved to size [maximum dimensions: 5×5 mm^2] to fit into a chip carrier package onto which the chip is glued using a conducting two-component silver epoxy cured at 120 °C. Fig. 4.22 (a) shows an SEM image of the STM-patterned device after contact annealing. From the image, we can see the characteristic three dimensional island growth of the Si encapsulation layer. An optical microscope image of the final device structure after gold wire bonding to the chip package pins is shown in Fig. 4.22 (b).

We have shown each stage of the process development and optimisation of the device fabrication strategy from registration marker fabrication, UHV device fabrication using STM lithography, phosphine dosing, P incorporation and Si encapsulation to the alignment of metal contacts for the electrical characterisation of patterned Si:P devices. The next section describes the electrical results of the first STM-patterned device demonstrating that STM-patterned Si:P structures can be contacted and electri-

cally characterised.

4.5 Electrical characterisation of a patterned STM device

In this section, the electrical characterisation of the first STM-patterned device is presented. Measurements were performed in a liquid helium 4 K dip station equipped with a 2T superconducting magnet using a standard DC source measurement unit. Using our novel fabrication technique, we have fabricated a 4×4 μm^2 P-doped square using STM lithography. By comparing the I-V characteristics of this device with an unpatterned control device, we show that electrical conduction comes from the STM-patterned buried dopant layer. Fig. 4.23 shows images of the critical fabrication steps for the buried P dopant square. Using the inner triangular and square registration markers as a guide [Fig. 4.23 (b)], we position the tip into the device area. In order to create such a large device (by STM standards), we desorbed and stitched together four 2×2 μm^2 squares. An example of such a large scale pattern of 1×1 μm^2 in size is shown in Fig. 4.23 (d). The sharp lithographic boundary achievable using STM lithography is clearly visible in the inset. After P dopant incorporation, four Al contacts are aligned to the corners of the dopant square [Fig. 4.23 (e,f)] forming a Van-der-Pauw measurement configuration. Since up to nine devices can be contacted individually on the same chip, it allows us to fabricate and compare multiple devices which underwent exactly the same processing steps. In this case, we have also contacted an unpatterned control device on the same chip which consists of four metal contacts sitting on top of a previously hydrogen covered Si surface which has not been patterned by STM i.e. where phosphine adsorption was blocked by the hydrogen resist.

4.5.1 I-V characteristics of control device

Our control device allows us to check the reliability of the hydrogen layer as a lithographic resist. O'Brien *et al.* have shown that PH_3 [19] molecules adsorb on dangling bonds exposed on the lithographic sites. Consequently, no PH_3 was observed to adhere to the silicon surface which is protected by the hydrogen resist. Therefore, there should be no P dopant incorporation and as a result, no current should flow through the Si surface between the contacts.

Fig. 4.24 shows the I-V characteristics of the control device measured at 4 K. On the left side, we can see the current flow that arises by applying a DC voltage in the

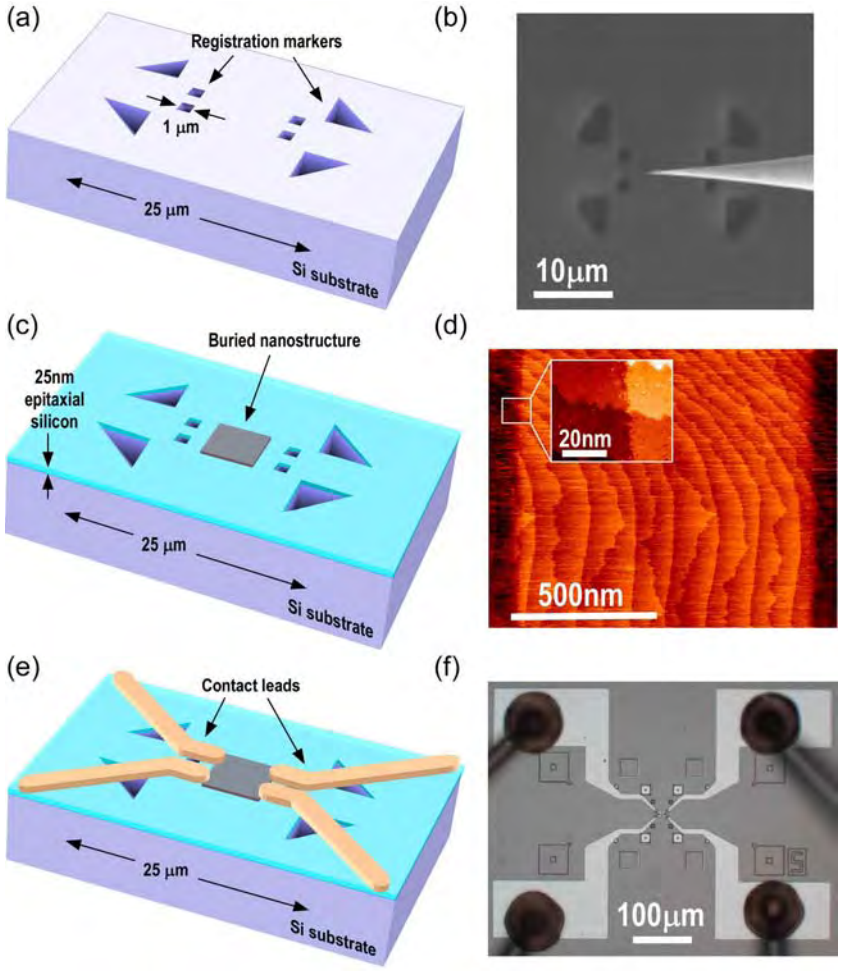

Figure 4.23: Process flow for the first STM-patterned device. (a) Schematic of 4 μm size triangular and 1 μm size square registration markers etched into Si. (b) SEM image of registration markers showing the STM tip (white). (c) Schematic of the registered, buried dopant structure STM-patterned on a Si:H surface under 25 nm epitaxial Si. (d) STM image of a 1×1 μm^2 Si:H square (inset: an example of the sharp lithographic boundary). (e) Schematic of the final device after alignment of external ohmic contacts using optical lithography. (f) Optical microscope image of the final device after gold ball bonding.

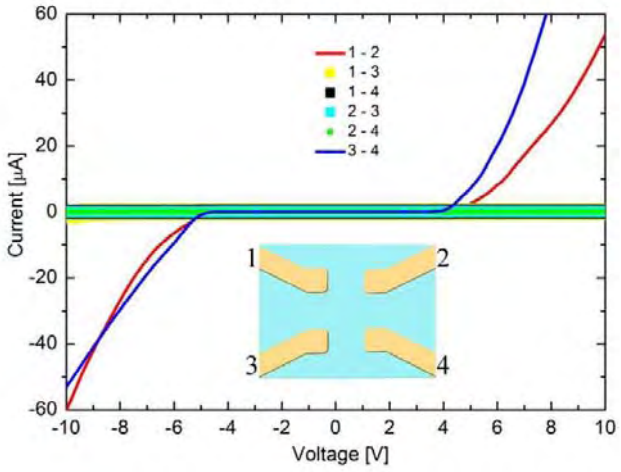

Figure 4.24: I-V characteristics of the control device. The insulating behaviour of the control device up to voltages of ± 5 V shows that the hydrogen resist efficiently stops phosphine adsorption.

range of ± 10 V between two respective Al contact leads. The contacts are labelled from one to four as indicated in the inset. Thus there are 6 different two terminal contact combinations. It is seen that there is no significant current flow in the range between ± 5 V regardless of the contact combination i.e. current direction. However, the 1-2 current direction as well as the 3-4 current direction give rise to significant current flow above 5 V. This insulation breakdown first occurs for opposing contacts due to their closer proximity. The observed substrate conduction that occurs at these high voltages is a result of avalanche breakdown caused by impact ionisation of electron-hole pairs through the application of a high electric field across the device. The breakdown voltage is related to the background doping density of the substrate. Note that our measurement biases for STM-patterned device measurements are generally below 10 mV and therefore well below the threshold of avalanche breakdown. Avalanche breakdown can in principle be avoided up to higher voltages using intrinsic substrates. However some background doping density is necessary to provide a conducting substrate for room temperature filled state STM imaging of the hydrogen terminated surface. We found that conduction due to background doping freezes out at cold temperatures depending on the doping density.

For our devices we use wafers with a room temperature resistivity of 1 – 10 Ωcm

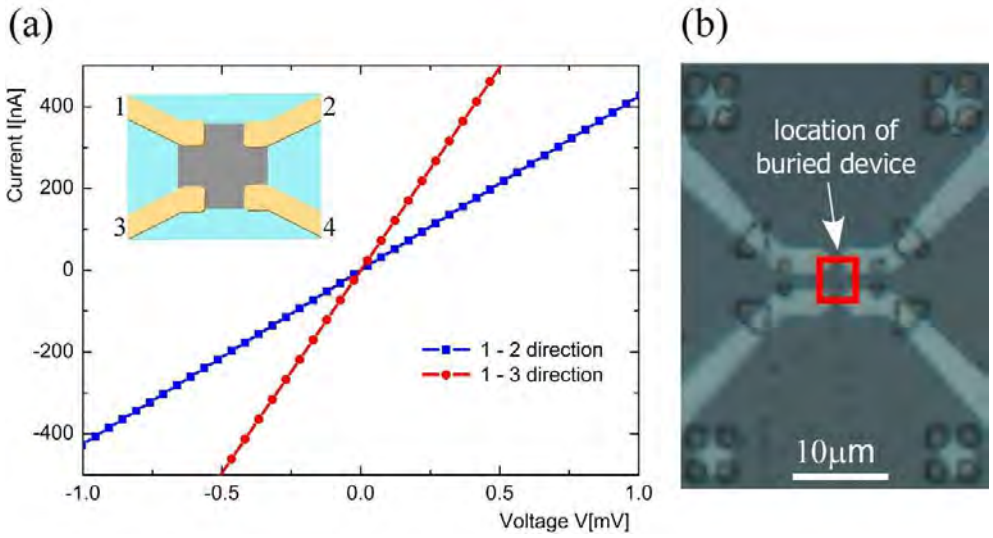

Figure 4.25: I-V characteristics of a 4×4 μm^2 P dopant square. (a) Four terminal measurements exhibit ohmic behaviour. For geometrical reasons, the resistance of R = 1 kΩ for the horizontal current path (current contacts: 1-2, voltage contacts 3-4) differs from R = 2.4 kΩ for vertical current direction (current contacts: 1-3, voltage contacts: 2-4). (b) Optical microscope image indicating the position of the buried P dopant square (red square) with respect to the four terminal leads.

stemming from a bulk P doping density of $\sim 3 \cdot 10^{15}$ cm^{-3}. The breakdown voltage thus presents the characteristic onset of avalanche conduction at this doping level. The highly insulating behaviour of the control device confirms the effectiveness of the hydrogen resist at blocking the adsorption of phosphine gas to the silicon surface.

4.5.2 I-V characteristics of P dopant square

The 4×4 μm^2 P-doped square device is measured at 4 K in the same thermal cycle as the control device discussed previously. Four terminal measurements, using a DC voltage source, allow us to eliminate unknown contact resistances. From the difference between two terminal and four terminal measurements, we were able to determine the contact resistances and found them to be uniform and low, ranging from 3 – 3.5 kΩ per contact electrode.

Fig. 4.25 (a) shows the four terminal I-V characteristics of our device. Only two current directions are shown for clarity. For the 1-2 (1-3) current direction, contacts 3-4 (2-4) were used as voltage probes. It is noteworthy, that the opposite contact configuration 3-4 (2-4) as current probes with 1-2 (1-3) as voltage probes yields identical I-V

curves. We conclude that the device is symmetric and homogenous.

The four terminal resistance between the 1-2 direction of R_{1-2} = 1 kΩ differs from the resistance R_{1-3} = 2.4 kΩ measured in the 1-3 direction. Fig. 4.25 (b) shows an optical microscope image of the final contact pattern of this device. The location of the buried P dopant square is indicated by the red square. It shows that the distance between opposing electrodes is larger than the distance of parallel electrodes resulting in a lower resistance for opposing contacts. Note, that we also see a difference for the current for different directions in the I-V characteristics of the control device shown in Fig. 4.24. Comparing the ratio between the vertical (1-2) and horizontal (1-3) separation of ∼0.5 with the ratio of the vertical and horizontal resistance of ∼0.4 shows that the difference in resistance can be accounted for by the difference in contact separation. A more precise estimate could be possible by taking the individual contact shape into consideration.

The most striking feature of the I-V curves is that they are perfectly ohmic. Ohmic behaviour confirms both, the fact that we can establish ohmic contact from Al electrodes down to buried P dopant regions and that the P dopant regions themselves are conducting. The density of buried P dopants is high enough to provide significant overlap between the (excess) electron wavefunctions of neighbouring P atoms. This behaviour was expected since the Bohr radius is ∼3 nm [163] and the P dopant spacing for a doping density of $1.7 \cdot 10^{14}$ cm^{-2} is much smaller, namely 0.77 nm. Finally, the insulating behaviour of the control device together with ohmic I-V characteristics of the P dopant square unequivocally proves that the conduction stems from the buried P dopants themselves.

4.6 Chapter conclusion

We have presented a complete strategy for the fabrication of robust devices using a combination of etched registration markers, SEM-controlled STM tip positioning, STM-based hydrogen lithography and Si molecular beam epitaxy. Optimisation of wet-chemically etched registration markers into the silicon surface enable the precise positioning and relocation of STM-patterned dopant structures under SEM control with accuracies of order ∼100 nm. Optimisation of STM-lithography for the formation of micro-, nano- and atomic-scale patterns on the hydrogen-passivated Si(100):H surface was shown. The formation of ultra-dense dopant patterns is achieved using

the self-terminating nature of our gaseous phosphine dopant source. A critical anneal incorporates a 0.25 monolayer (ML) density of P into the top layer of the Si(100) surface following saturation exposure of PH_3. A low temperature epitaxial Si encapsulation process enables electrical dopant activation away from surface states, defects and unsaturated dangling bonds. Ex-situ alignment of metal leads with an accuracy up to 100 nm, with respect to the registration markers, form ohmic contact to the buried STM-patterned device.

Comparison of I-V characteristics at 4 K of an STM-patterned, 4×4 μm^2 P-doped square device with an unpatterned, control device confirms that the hydrogen resist successfully blocks PH_3 adsorption. Ohmic conduction through the P dopant square thus originates from the buried P dopants. We will characterise electrical device parameters of this device in more detail using magnetotransport measurements in Chapter 5.

Chapter 5

Magnetotransport properties of STM-defined devices

In this chapter, we discuss the research outcomes of Si:P δ-doped layers [137], [138], [164], [167], [169]. Comparison of key device parameters obtained from Si:P δ-doped layers with STM-patterned devices allows us to specifically address what happens to the device properties when the dopants in the 2D plane are further confined in size and dimension by STM-patterning.

In Section 5.1.1, we will give an overview of recent studies in P δ-doped layer devices and their respective electrical characteristics at 4 K. We then discuss what happens to the electrical properties of the devices when we pattern the dopants into a 4×4 μm^2 P-doped square using STM. Initial results highlighting how we electrically contact such devices structures were already described in Chapter 4. In Sections 5.2.2 and 5.2.3, we go on to determine what effect the patterning has on the magnetotransport characteristics of such STM-patterned devices.

Further confinement of the dopants is then discussed using the STM to form a Si:P nanowire. In particular, we designed a wire of 90 nm width to try and observe a crossover from 2D to 1D magnetotransport. A comparison of the temperature-dependent magnetotransport data between the 4×4 μm^2 P-doped square and the 90 nm wire is shown in Section 5.3.2 demonstrating this dimensional crossover. These results allow us to give an estimate of the electronic width of the buried wire structure which is shown to be in excellent agreement with the lithographic width patterned by STM lithography. The implication of this result reflects that removing Si:P devices away from surface states, defects and dislocations by epitaxial Si encapsulation results in minimal lateral electrical depletion.

5.1 2D δ-doped Si:P devices

In this section, we will discuss important device parameters reported from using PH_3 as the dopant source for the fabrication of P δ-doped structures.

5.1.1 Summary of electrical characteristics of Si:P δ-doped devices

Table 5.1 contains an overview of the electrical results of P δ-doped layer devices using PH_3 as the dopant source and Si MBE for encapsulation.

Author	n_s [10^{14} cm^{-2}]	μ [cm^2/Vs]	l [nm]	l_φ [nm]	Growth T [°C]
Shen [169]	0.36	13			
	0.88	38			155
	1.31	28			
Oberbeck [137]	2.0±0.4	100			250
Sullivan [164]	1.4	104	30	101	high T
Goh [138]	(S1) 1.67	23	3	52	RT
	(S2) 1.64	61	9	72	250
Goh [167]	(S3) 0.8	10	1	18	250
	(S4) 1.53	27	4	62	250
	(S5) 1.62	23	3	54	250

Table 5.1: A summary of key transport properties (carrier density n_s, electron mobility μ, mean free path l, phase coherence length l_φ and MBE growth temperature) for phosphorus in silicon δ-doped layers fabricated by different research groups. All values are determined from measurements at 4 K except for [169] determined at 300 mK. The various fabrication methods differ in the MBE growth temperature, phosphine dose and different sample heating strategies. Details are given in the text.

The resulting device parameters such as electron density n_s, mobility μ, mean free path l and phase coherence length l_φ are listed for several different fabrication methods and encapsulation temperatures using Si MBE. In order to compare these values, it is necessary to discuss the different growth process for each device.

Shen *et al.* [169] conducted one of the first studies on P dopant δ-doped layers using PH_3 and low temperature Si MBE. By dosing the bare Si(100) surface with PH_3 at room temperature (RT), full (100 %) P dopant activation was reported up to a P coverage for 0.04 ML which reduced to 80 % when the coverage was increased to 0.16 ML. Further increase of the P coverage to 0.4 ML was achieved by repeated dosing in combination with a post-dosing anneal to 520 °C. By heating the substrate above T = 350 °C [32], the P atoms from the PH_3 molecules incorporate into the silicon top layer, thereby making

room for further surface adsorption in the next PH_3 cycle. However dopant activation dropped further to ∼50 %, which could be due to increased defect generation caused by excessive P doping. The electrical device parameters for each doping density are summarised in Table 5.1.

Full electrical activation with a mobility of ∼100 cm^2/Vs [see also Table 5.1] was reported by Oberbeck *et al.* [137] using a similar approach with a somewhat higher encapsulation temperature of T = 250 °C for the Si overgrowth. After a single saturation dose of PH_3 the substrate was annealed to 530 °C for dopant incorporation. Note that at this temperature, the hydrogen from the phosphine molecules will also be completely desorbed. The higher encapsulation temperature increases epitaxial quality and reduces the amount of P on the surface to 0.25 ML.

A similar value of electron mobility was recently obtained by Sullivan *et al.* [164] as can be seen from Table 5.1. The Si:P layer was grown at a temperature of 320 °C and encapsulated at higher growth temperature (value not stated) resulting in a carrier density of $1.4 \cdot 10^{14}$ cm^{-2}. They were able to determine the thickness of their Si:P layers to be ∼5 nm using magnetotransport measurements in parallel magnetic field, which indicates that their 2D system approaches 3D like behaviour.

From studies on Sb δ-doped layers [170], it was found that full electrical activation is achievable for true 2D δ-doped system but a deviation from full activation is found for 3D samples at higher doping density. Thermally activated dopant segregation and a higher presence of defects at higher doping densities are likely to be the determining factors that prevents full electrical dopant activation in the studies by both Shen *et al.* [169] and Sullivan *et al.* [164]. So far the study by Oberbeck *et al.* [137] is the only one achieving complete dopant activation, reinforcing the importance of the P incorporation anneal after saturation dosing of PH_3. In addition, low growth temperatures minimises dopant segregation, while optimising surface and epitaxial Si interface quality.

More recently, Goh et al. [138], [167] reported on a series of electrical transport measurements of P δ-doped layers moving away from the Van-der-Pauw design, used in previous reports [137], [169], [164] to etched Hall bar mesas. The first systematic study [138] targeted the influence of the encapsulation temperature on transport parameters. It showed that full electrical activation is achieved with encapsulation at RT [sample S1 in Table 5.1] as well as at 250 °C [sample S2 in Table 5.1]. However, the mean free path l, electron mobility μ and the phase coherence length l_φ were found

to be optimal for a growth temperature of 250 °C – the same growth temperature as originally used by Oberbeck *et al.* [137].

In a second study [167], the importance of the P incorporation anneal and the influence of hydrogen on the transport properties were investigated. The first sample [S3 in Table 5.1], encapsulated after phosphine saturation exposure without a P incorporation anneal, showed a measured electron density of only $n_s = 0.8 \cdot 10^{14}$ cm^{-2}, corresponding to ∼32 % electrical activation[1]. Compared with the first study [138] [S1, S2 in Table 5.1], where complete electrical activation is achieved, this results further consolidates the importance of P incorporation into the silicon lattice. The second and third sample in this study [S4 and S5 in Table 5.1] exhibit partial removal of hydrogen and complete re-termination with hydrogen respectively. Note that re-termination in sample S5 was achieved by performing a hydrogen termination after the P incorporation anneal. Both samples exhibit full activation and comparable values of l, μ and l_φ. Interestingly, the device parameters for the δ-doped layer grown at RT [S1 in Table 5.1] are very similar to device parameters obtained for the δ-doped layer encapsulated with complete hydrogen passivation grown at 250 °C [S5 in Table 5.1]. Eaglesham *et al.* [152] pointed out that hydrogen is known to stop Si migration/diffusion on the surface during growth, thereby degrading the quality of the epitaxial growth and increasing surface roughness. Comparing the transport parameters of S1 and S5 in Table 5.1, it appears, that the effect of hydrogen on the surface alters the epitaxial growth quality in a similar fashion as Si encapsulation at room temperature alters epitaxial growth.

The overall conclusions from these δ-doped layer studies are that the optimal fabrication strategy entails P incorporation after PH_3 dosing, thermal hydrogen removal from the surface before encapsulation to optimise electron mobility and a growth temperature of about 250 °C to limit P dopant segregation.

5.2 Lateral confinement of dopants using STM lithography

In this section, we investigate what happens to the transport properties if we constrict electron transport in the plane by using STM patterning to locally control the doping area. For this purpose, we compare the electrical transport properties of the 4×4 μm^2 P dopant square described in Chapter 4/Section 4.5 with a 90 nm wide wire.

[1] This ratio is due to a higher phosphorus coverage of $2.5 \cdot 10^{14}$ cm^{-2} (0.37 ML) [150] after PH_3 dosing without incorporation anneal.

Initially Hall measurements are used to extract the carrier density which allows us to determine electrical dopant activation and directly compare it to those obtained from Si:P δ-doped layers. We also compare other key device parameters such as the electron mean free path and mobility. Finally, we present results from four terminal magnetotransport measurements in a ^{3}He/^{4}He dilution refrigerator. Fitting the magnetoresistance data to 2D weak localisation theory enables us to extract the electron phase coherence length at both, 4 K and 50 mK.

5.2.1 Hall measurements of 4×4 μm^2 P dopant square

A critical aspect for the use of the STM fabrication process is whether the P dopants are electrically active. STM device schemes are attractive since they ultimately allow patterning of device structures at the few and single atom level. For functional atomic-scale devices, it will be essential that all or almost all P dopants are electrically active. We have undertaken four terminal Hall measurements at 4 K on the P dopant square device in a Van-der-Pauw configuration to determine the electrical P dopant activation. The basic principle underlying the Hall effect is the Lorentz force, which occurs for charged particles in the presence of a magnetic field. Electrons moving perpendicular to an applied magnetic field experience a force perpendicular to the current direction which results in a transverse voltage, the Hall voltage. The Hall voltage depends on the magnetic field B, the applied current I, the electron charge q and the sheet density n_s as:

$$U_{Hall} = \frac{B \cdot I}{q \cdot n_s} \tag{5.1}$$

or

$$R_{Hall} = \frac{B}{q \cdot n_s} \tag{5.2}$$

Fig. 5.1 shows the correlation of the Hall resistance in a perpendicular magnetic field for the P dopant square. The change in Hall resistance varies linearly with the magnetic field as predicted by Eq. 5.2. By performing a linear fit to the experimental data, we can extract the slope which, from Eq. 5.2, corresponds to $\frac{1}{q \cdot n_s}$. From this procedure, we obtain a sheet density n_s of $1.79 \cdot 10^{14}$ cm^{-2}. Since the presence of the P atom in the Si crystal has one excess electron compared to Si, the density of P atoms in the plane can be represented by the number of free electrons for conduction. The extracted value of n_s is consistent with the maximum density of incorporated P atoms, namely $1.7 \cdot 10^{14}$ cm^{-2} or a saturation coverage of 0.25 ML respectively. This

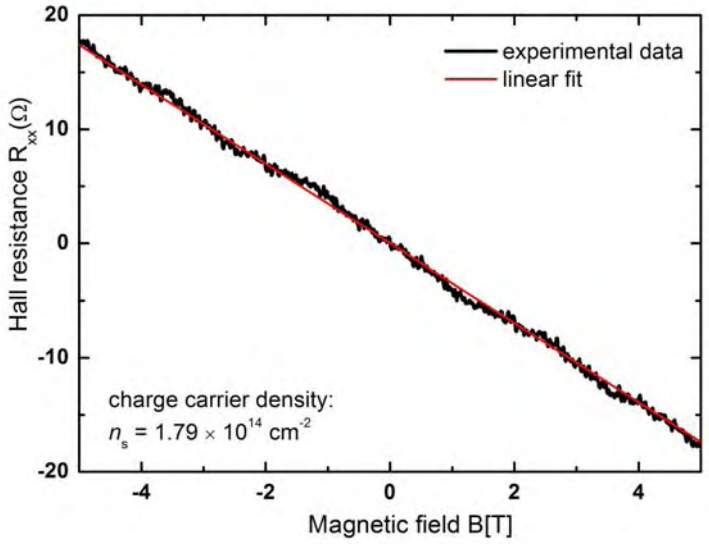

Figure 5.1: Electrical dopant activation of first STM device. Hall resistance of the 4×4 μm^2 P-doped square corresponding to a carrier density n_s of $1.79 \cdot 10^{14}$ cm^2 equivalent to complete electrical P dopant activation.

value corresponds to full electrical activation and directly compares to the values of full electrical activation obtained from Si:P δ-doped samples, fabricated in our group [137], [138], [167] and from other groups [164], [169]. These results demonstrates that the STM removes all the hydrogen resist in the lithographic area, so that we obtain the same doping density as in Si:P δ-doped layers, where no hydrogen resist is present.

5.2.2 Electron mobility and mean free path of P dopant square

From the zero-field resistance[2], we can extract the electron mobility using:

$$\mu = \frac{1}{\rho \cdot n_s \cdot e} \tag{5.3}$$

where ρ stands for the sheet density. From Fig. 5.2, we extract a sheet resistivity of ρ = 1.6 kΩ per square after applying a correction factor of 4.53 for the Van-der-Pauw structure. Using Eq. 5.3, we get an electron mobility μ of 22 cm^2/Vs. The

[2]The Van-der-Pauw correction factor for a square device is 4.53 i.e. $R_{xx} = R_{actual} \cdot 4.53$.

corresponding mean free path is given by:

$$l = \frac{\hbar \cdot \mu \cdot \sqrt{\pi \cdot n_s}}{e} \tag{5.4}$$

For the carrier density n_s of $1.79 \cdot 10^{14}$ cm^{-2} from the Hall measurements, we obtain a mean free path of l = 3.4 nm. We compare l and μ from our doped square with the values from P-doped δ layers reported by Goh *et al.* [138], [167] stated in Table 5.1. Both l and μ are lower than the full activation sample [S2 in Table 5.1] grown at 250 °C. However they compare well with samples [S4, S5 in Table 5.1] which retained partial presence of hydrogen and complete hydrogen re-termination respectively. These results suggest, that the combined P incorporation (350 °C) and the subsequent hydrogen removal anneal to 470 °C, which we performed on the P dopant square device, has not been sufficient to completely remove the hydrogen resist from the surface. Such an anneal temperature was previously found to remove hydrogen from the surface whilst keeping the structural integrity of a Si:P STM-patterned nanostructure [67]. Whilst a temperature of 470 °C does not seem optimal for complete hydrogen resist removal at this point, the prevention of dopant distribution has been a key factor in the choice of this anneal temperature.

5.2.3 Weak localisation measurements of P dopant square

We performed four terminal magnetotransport measurements of the P dopant square device in a ^{3}He/^{4}He dilution refrigerator at both, 4 K and 50 mK, using standard lock-in techniques at a measurement frequency of 10 Hz. Fig. 5.2 shows the magnetoresistance of the P dopant square device at 4 K and 50 mK. If we consider the magnetoresistance at 4 K, we can see a peak centred around B = 0 (red squares). The magnetoresistance decreases with increasing perpendicular magnetic field leading to the observation of negative magnetoresistance – the characteristic signature of weak localisation. The effect of weak localisation arises from coherent backscattering of forward and time-reversed electron waves around a loop as electrons diffuse through the sample. The application of a magnetic field breaks the time reversal symmetry in these loops, suppressing the coherent backscattering, and resulting in a drop in the magnetoresistance as the magnetic field increases. We can extract the phase coherence length l_φ of the electrons by fitting the magnetoresistance to the Hikami [71] expression for conductance correction due to weak localisation for a two dimensional, diffusive system (see green line in Fig. 5.2). The conductance correction is obtained

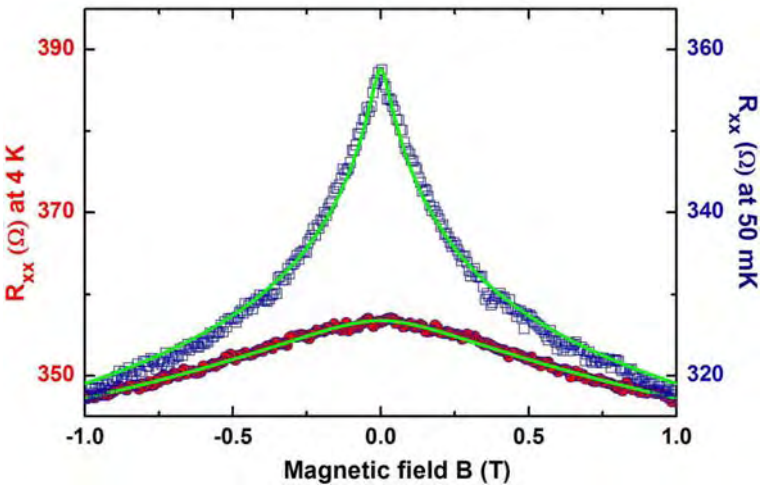

Figure 5.2: Magnetotransport for the 4×4 μm^2 P-doped square. Measurements of the four terminal magnetoresistance at sample temperatures of 4 K (red squares) and 50 mK (blue circles) are shown. The green lines represent fits to the Hikami 2D weak localisation theory [71].

from the difference between the inverse sheet resistivity at a given magnetic field and the inverse, zero-field sheet density as:

$$\Delta\sigma = \frac{1}{\rho_{xx}(B)} - \frac{1}{\rho_{xx}(0)} \tag{5.5}$$

For electron transport in a highly diffusive 2D system [$l \ll$ feature dimensions], the Hikami model is given by:

$$\Delta\sigma = \frac{\alpha e^2}{\pi h}\left[\Psi\left(\frac{1}{2}+\frac{\tau_B}{2\tau}\right) - \Psi\left(\frac{1}{2}+\frac{\tau_B}{2\tau_\varphi}\right)\right] \tag{5.6}$$

where $\tau_B = \frac{\hbar}{2\cdot e\cdot B\cdot D}$ is the magnetic dephasing time and Ψ is the *digamma* function. α denotes a numerical prefactor of order unity.

We fit this function to the experimentally obtained form of $\Delta\sigma$ by varying the values of τ, τ_ϕ and α. The values of τ, τ_ϕ and α for our system are those values that give the best fit of the model to the experimental data. From the fitted value of τ = 4·10^{-15} s, the diffusion constant D follows from $D = \frac{\tau}{2\cdot v_f^2}$. Using the relation

$$l_\varphi = \sqrt{D\cdot\tau_\varphi} \tag{5.7}$$

and the fitted, inelastic dephasing time τ_φ = 1.6 ps, we find l_φ to be ∼39 nm at 4 K. Comparing the extrapolated electron mobility and phase coherence length with those obtained from the P-doped δ layers shown in Table 5.1, we see that the l_φ obtained

is comparable to the δ-doped samples S1 and S5 exhibiting hydrogen re-termination and encapsulation at room temperature respectively. In these two samples, values of l = 3 nm, μ = 23 cm^2/Vs and l_φ = 52 – 54 nm were obtained.

We have shown that the device parameters of the first STM-fabricated P dopant square device compares best with the electrical results at 4 K from P δ-doped layers prepared in our group which exhibit hydrogen coverage on the surface or which were encapsulated at room temperature. This result suggests that the epitaxial growth in our device was of slightly lower quality than an ideal δ-doped layer of comparable growth temperature. This could be due to the fluctuations of the sample temperature during hydrogen resist removal or due to STM patterning. However, the measured STM device parameters, l, μ and l_φ, are of the same order as those obtained for the Si:P δ-doped layers which implies that the influence due to STM patterning is not significant.

We now turn our attention to the magnetotransport data at 50 mK also shown in Fig. 5.2. As the temperature is lowered from 4 K to 50 mK, the phase coherence length increases leading to the formation of more, and longer, phase coherent loops producing a more pronounced drop in the magnetoresistance. Note that the overall resistivity is similar at both temperatures, as expected for a highly-doped 2D metallic system. By fitting the data to the Hikami expression, we can extrapolate the device

T	n_s [10^{14}cm^{-2}]	μ [cm^2/Vs]	l [nm]	l_φ [nm]
4 K	1.79	22	3.4	39
50 mK	1.79	22	3.4	136

Table 5.2: Summary of n_s, μ, l and l_φ for a 4×4 μm^2 STM-patterned P dopant square at temperatures of 4 K and 50 mK.

parameters μ, l and l_φ, which are summarised for both 4 K and 50 mK in Table 5.2. It is worth noting that, whereas the same values are obtained for n_s, μ and l, the values for the electron phase coherence length l_φ increases as predicted by Altshuler [79], giving a value of 136 nm. The longer phase coherence length is manifested in the rise of the magnetoresistance peak around zero-field with respect to the trace at 4 K as clearly seen in Fig. 5.2. In practical terms , the increase of l_φ at lower temperatures means that our samples are in the mesoscopic regime where phase coherence plays a dominant role. The high level of disorder characterised by the small mean free path is due to the high density of dopants in the conducting plane. By designing a device with

dimensions below l_φ at low temperatures, we can observe the dimensional crossover from 2D to 1D magnetotransport as we lower the measurement temperature.

5.3 Crossover from 2D to 1D in an STM-patterned wire

This section describes the effectiveness of the STM to form laterally constricted P dopant regions. We present an STM image of the device and explain the entire UHV fabrication process. One of the strengths of STM device fabrication is the precise knowledge of the device dimensions. This allows us to relate the geometric shape patterned by the STM with the electrical results of the device.

5.3.1 Patterning of a 90 nm wide wire

Using the fabrication developed in this thesis, we fabricated a 90 nm wide wire with a length of 900 nm. Both, the P-doped square and this 90 nm wide wire were fabricated on the same chip, which makes them directly comparable to each other. Fig. 5.3 shows a schematic of the wire device. In addition to the wire, at each end of the wire, a 1.5 μm long and a 3 μm wide rectangular side contact patch has also been patterned to enable us to connect to the four terminal external metal leads (shown in gold) subsequently created by optical lithography. The desorption parameters for STM lithography were 6 V for the gap voltage and 4 nA for the tunnelling current. An STM image of the lithographic area of the wire can be seen in Fig. 5.4 indicating the sharp boundary where the underlying Si has been exposed. The exposed Si surface appears bright due to the additional tunnelling current contributed by the Si surface states which are not accessible on the hydrogen terminated surface [171]. Further UHV device processing consists of PH_3 dosing at 1.1×10^{-9} mbar for 15 min, combined P incorporation and thermal hydrogen resist removal by annealing the surface to 470 °C for 60 s followed by encapsulation with 25 nm of epitaxial Si grown at 250 °C.

5.3.2 Magnetotransport behaviour

In Fig. 5.4 we present the magnetoresistance of the 90 nm wide wire device processed on the same chip as the STM-patterned square device. We can see that the overall four terminal resistance of the wire of R = 5 kΩ is much higher than for the P-doped square device (shown in Fig. 5.2), as expected from the wire geometry. At 4 K (red

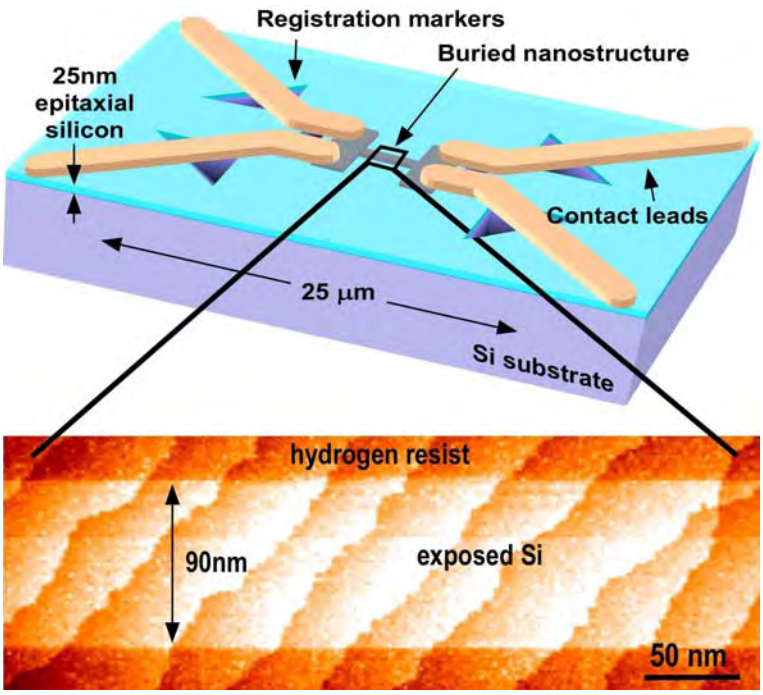

Figure 5.3: STM patterning of a 90 nm × 900 nm P-doped wire. *above:* A schematic diagram of the wire pattern is shown. The wire is attached to dopant contact patterns which allows connection of the wire to four terminal leads created by optical lithography (shown in gold colour). *below:* A filled state STM image of the lithographic wire pattern of the real device; imaging conditions: V = -2.3 V, I = 0.18 nA.

trace), the resistance of the wire device shows a similar peak in the magnetoresistance around zero magnetic field as for the square device. By fitting this behaviour to the Hikami expression (Eq. 5.6), we can extract a phase coherence length of l_φ = 32 nm. Since both devices were fabricated on the same chip exposed to the same dose of PH_3 gas, we assume the same carrier density as measured from Hall measurements on the square device. We extract a slightly higher mobility of μ = 70 cm^2/Vs and a mean free patch of l = 11 nm. The increase in l and μ might be due to a higher level of hydrogen desorption since this device is located in the very centre of the chip, where the temperature due to the electron beam heater in the UHV chamber is expected to be the hottest. The phase coherence length l_φ of 32 nm is in good agreement with the results obtained for the P-doped square device, highlighting that electron transport in the wire at 4 K is essentially the same as for the two-dimensional square device, i.e. electrons are unable to distinguish if they are travelling through a 4 μm wide square or a 90 nm wide wire.

As the temperature is reduced to 50 mK, we find l_φ increases and becomes larger than the wire width of 90 nm. At this point, the lateral confinement of the wire limits the maximum size of electron loops that can contribute to weak localisation. Thus although the negative magnetoresistance starts to become stronger as the temperature is reduced (blue trace in Fig. 5.4), it does not produce such a pronounced peak around $B = 0$. This is clearly highlighted if we consider the 2D Hikami fit applied to the wire (green line in Fig. 5.4) which gives an increased phase coherence length l_φ = 135 nm. Here we can clearly see a suppression of the 2D weak localisation around $B = 0$ due to a crossover from two-dimensional to one-dimensional magnetotransport. Importantly, we can use the suppression of the 2D weak localisation to *independently* measure the width of the wire. Constructive interference is destroyed when a magnetic flux quantum threads a loop of radius r, i.e. when

$$r^2 = \frac{\hbar}{eB} = l_B^2 \tag{5.8}$$

When the magnetic length l_B is much larger than the wire width w, the magnetic field has relatively little effect, which results in the plateau around $B = 0$. As the magnetic field increases the size of the constructively interfering loops becomes smaller, so that it is B, and not the wire width, that determines the magnitude of the weak localisation effect. Thus the wire approaches two-dimensional behaviour when $2 \cdot l_B \sim w$. From Fig. 5.4, we see that the measured data merges with the green line of the 2D the-

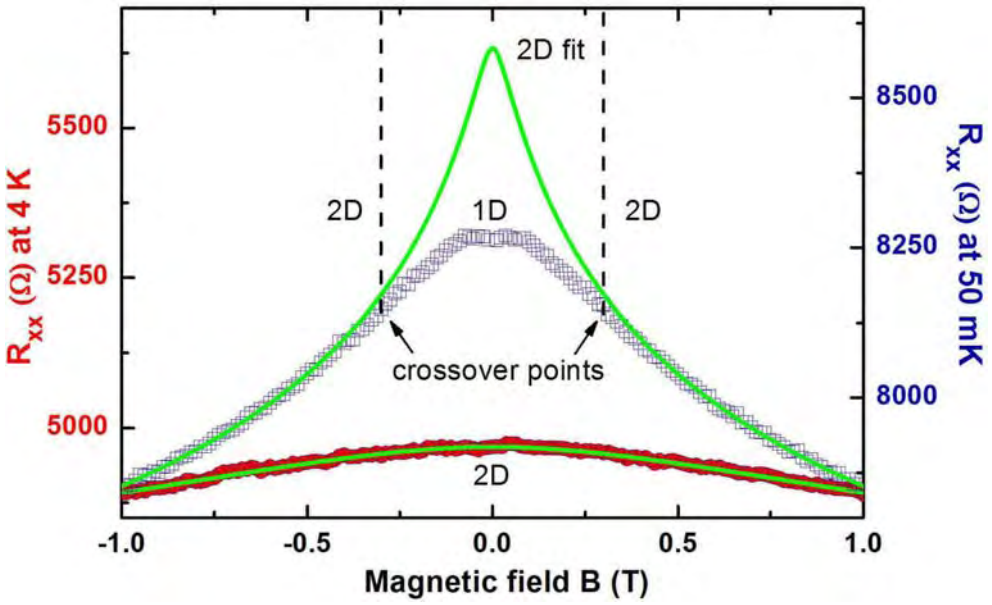

Figure 5.4: Magnetotransport for a 90 nm × 900 nm P-doped wire. Measurements of the four terminal magnetoresistance at sample temperatures of 4 K (red squares) and 50 mK (blue circles) are shown. The green lines represent fits to 2D weak localisation theory.

ory at $|B| \sim 0.3$ T, giving a wire width of ∼90 nm, in excellent agreement with the STM-defined geometry. It is worth noting that a wire width <100 nm was chosen as the ideal geometry, which is dictated by the phase coherence length, to observe the crossover from one dimensional to two dimensional electron transport in a our highly doped Si:P system.

T	n_s [10^{14}cm^{-2}]	μ [cm^2/Vs]	l [nm]	l_φ [nm]
4 K	1.79	70	11	32
50 mK	1.79	42	7	135

Table 5.3: Summary of n_s, μ, l and l_φ for a 90 nm wide and 900 nm long P dopant wire at temperatures of 4 K and 50 mK.

5.4 Chapter summary

In this chapter, we investigated the use of the STM to confine dopants laterally in the 2D plane and determined the magnetotransport properties of STM-patterned devices. Initially we discussed the key UHV fabrication steps from a comparison between Si:P δ-doped layers reported in the literature and those fabricated in our group. We found

that transport parameter, such as l, μ and l_φ, are optimised for δ-doped layers using a saturation dose of PH_3, employing a P incorporation anneal at 350 °C and using a low temperature of 250 °C for the device encapsulation with epitaxial Si. Independently, Hallam *et al.* [67] conducted an STM study and found that the hydrogen resist layer can be removed by annealing the Si surface to 470 °C. We compared the critical transport parameters (n_s, l, μ and l_φ) from a δ-doped layer using the optimised UHV fabrication steps with those obtained from a 4×4 μm^2 P-doped square patterned by the STM.

Hall measurements showed that all buried P dopant are electrically active demonstrating that STM patterning does not adversely affect electrical device characteristics. Whilst the carrier density, n_s, emerging from the P-doped square of 1.79×10^{14} cm^{-2} and the electron phase coherence, l_φ of 39 nm remain almost unchanged, the mobility, μ of 21 cm^2/Vs obtained in the STM-fabricated P-doped square resembles those obtained for δ-doped layers where hydrogen exposure has deliberately been applied as well as those encapsulated at room temperature. The reduction in mobility for STM-fabricated devices is therefore attributed to incomplete removal of the hydrogen resist layer which inhibits silicon diffusion during the encapsulation step thus decreasing epitaxy and ultimately device quality.

Following this, we used the STM to pattern the P dopants to form a wire of 90 nm width and 900 nm length. From the magnetotransport, we observe, that, at low temperatures, where $l_\varphi > 100$ nm, there is a suppression of the formation of phase coherent loops as indicated by a saturation of the zero-field resistance compared with the expected 2D behaviour which we attribute to 1D weak localisation. The crossover between 1D and 2D weak localisation allowed us to indirectly confirm the width of the wire as patterned by the STM. These results were published in Nano Letters [30], the Journal of Molecular Simulation [172] and appeared in the peer-reviewed Proceedings of SPIE [136]. Our results confirm the viability of using an STM to pattern dopants in silicon and reinforce the enormous potential of STMs for device fabrication down to the atomic level.

Chapter 6

Nano- and atomic-scale wires

This chapter is concerned with the electrical properties of Si:P nanowires of different widths. For this purpose, we will give an overview of different techniques with which P-doped Si nanowires have been realised by other research groups and compare their key properties. We then go on to present an STM study that investigates the structural integrity of STM-patterned Si:P nanowires down to a width of 7 nm. Using constant imaging tunnelling spectroscopy (CITS), we are able to discern the structural integrity of P-doped wires buried under a few monolayers of epitaxial Si. These results highlight, that the P dopants maintain their structural integrity during device encapsulation confirming that the electrical results we obtain are directly related to the STM-patterned dopants.

The main focus of this chapter lies in a detailed electrical characterisation of a 27 nm wide wire over a large temperature range from 200 mK to 65 K. We will see that transport through the wire can be divided into three regimes. By extracting the electron phase coherence using weak localisation theory, we identify a crossover from 1D to 2D magnetotransport at 4 K. Above 4 K, 2D magnetotransport is dictated by a dephasing mechanism stemming from electron-phonon interaction. Below 4 K, the wire conductance is well described by a combination of 1D weak localisation theory and 1D electron-electron interaction theory. At temperatures below 450 mK, we observe a saturation in l_φ which is likely to result from a crossover from weak localisation to strong localisation.

Finally, we present recent results from the fabrication of sub 10 nm wide Si:P wires patterned by the STM.

6.1 Resistivity of different P-doped nanowires in silicon

It is difficult to comprise a summary that does good justice to the field of nanowires since numerous approaches have been reported in the literature. However, we have summarised approaches which, arguably, stand out in the limit of narrow nanowires below <100 nm. Only nanowires in silicon using phosphorus as a dopant will be discussed.

6.1.1 EBL-defined nanowires

A *top-down* approach for the fabrication of nanowires has naturally been pursued by many groups. Advanced electron beam lithography (EBL) is used to pattern wire structures into P-doped substrates which were either obtained by thermal P diffusion or by P ion implantation. Patterning of the P-doped Si occurs using an anisotropic etching method such as reactive ion etching (RIE). A representative example using P ion implantation is the work by Smith *et al.* [173]. Nanowires down to a width of 60 nm with side gates reaching along the entire wire length of 200 nm were fabricated. At low temperatures, Coulomb blockade effects were observed due to the presence of small islands and barriers along the length of the wire. These barriers resulted from the randomly fluctuating potential in the wires originating from inhomogeneous dopant distribution from the P ion implantation process and the presence of charge traps. At higher temperatures (T = 46 K), a similarly manufactured 70 nm wide wire showed ohmic behaviour using a side gate voltage of -21 V, whereas 60 nm wide wire still showed non-ohmic I-V characteristics.

Pescini *et al.* [174] defined a suspended P-doped Si wire by etching down a highly P-doped device layer using RIE. A rectangular nanowire (140 nm wide and 150 nm thick) showed metallic behaviour with a two terminal resistance of 1 kΩ on an silicon on insulator (SOI) substrate down to 2 K.

Park *et al.* [175] fabricated a 30 nm wide wire using a combination of electron beam lithography and P ion implantation to create a rectangular wire (30 nm wide and 30 nm thick) . After a rapid thermal anneal to 1000 °C for dopant activation and crystal repair, the silicon wire was found conducting at T = 4 K with two-terminal resistances varying between 300 - 500 kΩ for a wire length of 200 nm.

Nanowires made of recrystallised amorphous silicon on thermal SiO_2 based on a p-type Si substrate were fabricated by Kawamura *et al.* [176]. P doping was carried out

by $POCL_3$ diffusion at 900 °C. A 100 nm wide and 82 nm thick rectangular wire was created by EBL and etching in an electron cyclotron resonance etcher. At 10 K, metallic I-V behaviour was recorded whereas a blockaded region around zero bias was seen for smaller wire thicknesses.

6.1.2 Template growth

Another way to define silicon nanowires is to selective grow them on a pre-patterned surface template. Beckman *et al.* [177] grew such a template using an epitaxial GaAs / Al $_{0.5}Ga_{0.5}As$ superlattice. Pt was evaporated to act as a shadow mask. Pattern transfer to form silicon nanowires from a P-doped SOI substrate occurred using RIE. Typically 2 – 4 rectangular Si nanowires, 10 nm wide and 30 nm thick, with lengths of 3 μm, were contacted simultaneously showing ohmic behaviour with resistances of order 200 kΩ at room temperature.

6.1.3 Catalytic growth method

Growth of free standing silicon nanowires ranging from thickness of 20 nm to 90 nm were reported by Lieber's research group in Harvard [178]. This laser-assisted vapour-liquid-solid catalytic growth technique (VLS method) uses gold nanoparticles to seed circular nanowires of multiple microns in length. Tromp and coworkers [179] recently reported that Au diffusion from the gold nanoparticles determines the length, shape and sidewall properties of the nanowires grown using low pressure catalytic vapour deposition (CVD), whereas the adsorption of contaminants or oxygen prevents Au migration in conventional high pressure CVD systems. This means that cleanliness of the growth environment has a strong influence on the properties of the nanowires. The Si-P doping ratio was adjusted from heavily P-doped to lightly P-doped wires using a Au-P target at the gas inlet to the silane (SiH_4) growth atmosphere. Exhibiting rather large contact resistances of several hundred kΩ, most likely originating from an oxidised SiNW shell, the conductivity was found to be varied over several orders of magnitude depending on the dopant level. The room temperate resistance of a highly-doped Si nanowire of 20 nm in diameter was found to be 200 kΩ [180].

group\reference	P dose or P doping	diameter [nm]	length [nm]	temperature [K]	resistance [kΩ]	resistivity [10^{-6}Ωm]	comments
Ahmed – Cambridge, UK							
Smith *et. al.* J. Appl. Phys. 81(6) 2699 (1997)	7.2×10^{18} cm^{-3}	60	4000	46K	~2650 (2T)	n.a.	almost ohmic behaviour at high temperature
	7.2×10^{18} cm^{-3}	70	6000	46K	~1100 (2T)	n.a.	ohmic only with applied side gate voltage (-21V)
Lieber – Harvard, USA							
Cui *et. al.* J. Phys. Chem. 104, 22 (2000)	unknown, low	60	unkown	RT	$\sim2\times10^{6}$ (2T)	3×10^{10}	non-linear
	unknown, high	90	unkown	RT	~130 (2T)	2.3×10^{6}	linear
Zheng *et. al.* Adv. Mat. 16, 21 (2004)	P (lightly) (Si:P 4000:1)	20	typical 1000	RT	300 (4T), 1000 (2T)	94	based on electrode length of ~1000 µm
	P (heavily) (Si:P 500:1)	20	typical 1000	RT	200 (2T,4T)	63	
Schenkel – Berkeley, USA							
Park *et. al.* J. Vac. Sci. B 22(6), 3115 (2004)	5×10^{14} cm^{-2}	30×30	200	4.2	300-500 (2T)	1400-2400	metallic
Yokoyama- Hiroshima, Japan							
Kawamura *et. al.* J. Appl. Phys. 91(8), 5213 (2002)	$>3\times10^{20}$ cm^{-3}	100×82	5000	10K	166 (2T)	272	polycrystalline silicon (metallic to Coulomb blockade)
Heath – CALTECH, USA							
Beckman *et al.* J. Appl. Phys. 81(10) 5921 (2004)	10^{20} cm^{-3}	10×30	3000	RT	3-4 wires: 200	60-80	nanowire array
Tucker – Illinios, USA							
Shen *et. al.* J. Vac. Sci. Technol. B 22 (6) 2004	10^{14} cm^{-2}	50×4	750	0.3	~337 (2T), 220 (4T)	$59^{**}/9^{*}$	metallic
	10^{14} cm^{-2}	95×4	750	0.3	~180 (2T), 50 (4T)	$25^{**}/4^{*}$	R_{4T} estimated values, metallic
Kotthaus – Munich, Germany							
Pescini *et. al.* Nanotechnology 10, 418 (1999)	5×10^{19} cm^{-3}	140×150	1500	2K	1 (2T)	14	almost metallic at 2K
Simmons – Sydney, Australia							
Ruess *et. al.* Nanotechnology 16, 2446 (2005)	1.8×10^{14} cm^{-2}	90x0.6	900	4.2	21 (2T), 10 (4T)	1^{*}	metallic
	1.8×10^{14} cm^{-2}	50x0.6	310	4.2	48 (2T), 34 (4T)	3^{*}	metallic
	1.8×10^{14} cm^{-2}	27x0.6	320	4.2	58 (2T), 50 (4T)	3^{*}	metallic

Figure 6.1: Key device parameters of P-doped silicon nanowires. Device parameters of Si:P nanowires manufactured using different *top-down* and *bottom-up* fabrication techniques are compared to STM-fabricated wires presented in this thesis. [*Resistivity values calculated with a thickness of 0.6 nm as determined from STM studies using the Si growth conditions in our group [181]. **Resistivity values calculated with a thickness of 4 nm as reported by Tucker *et al.* [29].]

6.1.4 STM-patterned nanowires

An STM-based fabrication method to create planar Si nanowires, similar to the one presented in this work, is currently being pursued by Shen *et al.* [29]. Interdigitated contacts made from pre-implanted As lines in the silicon substrate serve as two terminal leads for contacting the device. P-doped Si wires between the As regions were fabricated using STM lithography on a hydrogen resist in a UHV environment. Doping occurred by selective adsorption of PH_3 onto the exposed Si area whereas the hydrogen resist blocked molecule adsorption. After encapsulation of the wire structure with several monolayers of epitaxial silicon, the donors are activated by annealing to 500 °C. A 95 nm and a 50 nm wide wire, both 750 nm long with a reported thickness of 4 nm, were created using this technology. The 95 nm wire displays ohmic conductance at T = 300 mK whereas the 50 nm wide wire behaves slightly non-ohmic. Contact resistances were estimated from an array of implanted As wires and found to be $\sim$100 kΩ.

The most crucial difference between the latter approach and the one [30] developed in this thesis is the use of registration markers to relocate the nanowires instead of prefabricated contact patterns. The registration marker technique has 4 main advantages. (1) It allows the use of standard Si sample preparation technique which includes annealing to T = 1200 °C to obtain high quality, low defect density crystal. (2) It enables us to perform four terminal measurements which eliminates unknown contact resistances. Wires of 90, 50 and 27 nm width were found to obey ohmic behaviour at 4 K and below with four terminal resistances of 10, 34 and 50 kΩ respectively [31]. Contact resistances are found to be $\sim$10 kΩ. (3) Precise knowledge of the exact dimensions and location of the device allows us to contact several devices on the same chip individually and directly compare their electrical properties. (4) Since we know where the device is, we are able to align contacts directly to the STM-patterned device and, in the future, gate electrodes above the device.

6.1.5 Resistivity of silicon nanowires

Table 6.1 summarises essential device parameters of the nanowires fabricated with the approaches discussed previously. The table is ordered with the highest resistivity at the top and also includes details about doping density, wire diameter, wire length, measurement temperature and wire resistance. Note that most P concentra-

tions quoted are areal doping densities and do not necessarily reflect the carrier density of the device. Only for STM-patterned wires fabricated in this thesis, they exists a one to one correspondence between dosing and carrier density, since we have previously shown 100 % electrical P dopant activation.

STM-patterned fabrication [29], [31] allows the fabrication of planar nanowires, where conduction is confined to a thin 2D region in the P dopant plane. Whilst Tucker *et al.* [29] reports wire thicknesses of 4 nm [29] using this technique, recent studies by our group [181] have shown that for our growth conditions, the thickness of the Si:P δ-doped layers is $\sim$0.6 nm as determined from STM-based P diffusion studies.

The resistivity of the wire (rather than the resistance) is more likely to provide a comparable benchmark for the quality of dopant wires given the variety of fabrication approaches of P-doped Si nanowires. However the temperature at which the various wires were characterised ranges from as little as 300 mK up to room temperature. Within this temperature range, the resistivity of the wire may decrease by one order or more in magnitude. The different measurement temperatures have to be critically taken into account when comparing resistivities of wires fabricated by different techniques.

Both Beckman's [177] template technique and the VLS technique [180] from Lieber's group produce highly P-doped wires with similar resistivity of $\sim 63 \cdot 10^{-8}$ Ωcm at room temperature. However the resistivity is expected to increase at low temperature which makes it hard to compare with other wires characterised at liquid helium temperatures.

Before our work, Pescini *et al.* [174] reported the lowest resistivity for EBL-defined wires with a value of $14 \cdot 10^{-8}$ Ωcm. Although the I-V behaviour of this 140 nm wide and 150 nm thick wire was observed to behave slightly non-ohmic at 2 K. The next best resistivity is given by Tucker and Shen's [29] STM-fabricated wires with similar resistivities of $25 \cdot 10^{-8}$ Ωcm based on a thickness of 4 nm as stated. The values obtained from STM-patterned wires fabricated in this thesis and measured at 4 K represent the lowest resistivity wires to date with values as low as $1 \cdot 10^{-8}$ Ωcm. Wires fabricated by ion implantation, reported by Park *et al.* [175], exhibit high resistivities ranging from 1400 to $2400 \cdot 10^{-8}$ Ωcm. This is most likely due to structural damage and ion straggle in the ion implantation process through the SiO_2 mask.

The low resistivity value obtained for planar STM-fabricated wires make this technique a promising candidate for the formation of conducting wires down to the atomic

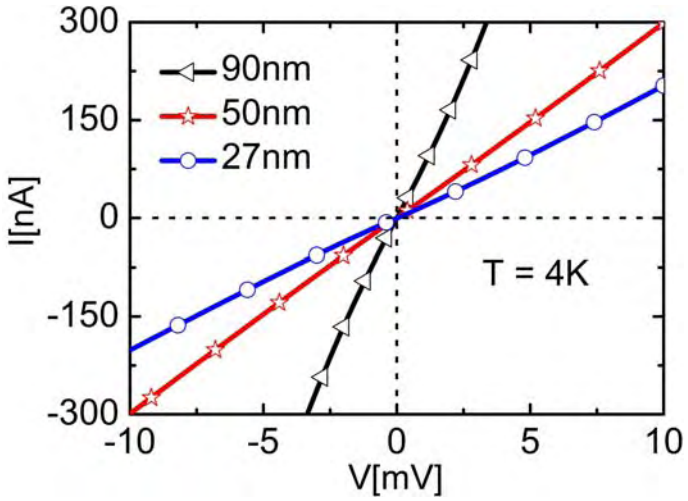

Figure 6.2: Four terminal I-V characteristics of a 90 nm × 900 nm wire (triangles), a 50 nm × 310 nm wire (stars) and a 27 nm × 320 nm wire (circles) at 4 K.

level.

6.2 Si:P nanowires fabricated in this thesis

In this section, the electrical device properties of three STM-fabricated P-doped wires will be summarised. Apart from the 90 nm × 900 nm wire discussed in Chapter 5 and the 27 nm × 320 nm wire presented in more detail later on in this chapter, another wire of intermediate dimensions of 50 nm × 310 nm was measured. Fig. 6.2 shows the four terminal DC I-V characteristics of the three wires at 4 K clearly revealing that all wires demonstrate ohmic behaviour over the entire voltage range and up to currents of several hundred nanoampere. The corresponding current densities (based on a wire thickness estimate of 0.6 nm [181]) are quite high, in excess of 1250 kA/cm^2 for the 27 nm wire and comparable to the capacity of highly doped Si nanowires [182] and 50 times higher than the current densities measured by Tucker *et al.* [29]. This high current density corresponds to a power of several nanowatts. The four terminal resistances emerging from Fig. 6.2 show a resistance increase from 10 kΩ for the 90 nm wire, to over 34 kΩ for the 50 nm wire and up to 50 kΩ for the 27 nm wire.

Important device parameters such as doping density n_s, mobility μ, mean free path l and electron phase coherence length l_φ for these devices are summarised in Table 6.1. The doping density of our wires is estimated to be the same for all wires since

wire [nm^2]	n_s [$\frac{10^{14}}{cm^2}$]	μ [$\frac{cm^2}{Vs}$]	l [nm]	l_φ [nm]	R_{4T} [kΩ]	J [$\frac{kA}{cm^2}$]	$\frac{l_\varphi}{w}$
90×900	1.8	70	11	32	10	560	0.4
50×310	1.8	10	2	30	34	980	0.6
27×320	1.8	11	2	24	50	1250	0.9

Table 6.1: A summary of key device characteristics for the 90, 50 and 27 nm wires at T = 4 K. Note for the 50 nm and the 27 nm wires, the hydrogen resist was not removed prior to device encapsulation hence the lower electron mobility.

we have a standard, well calibrated PH_3 saturation dosing procedure. The value of $n_s = 1.8 \cdot 10^{14}$ cm^{-2} has been confirmed from Hall measurements (Chapter 5) for the 4×4 μm^2 P-doped square device using the Van-der-Pauw technique, which was made on the same chip as the 90 nm wide wire. Independently, Hall bar measurements on δ-doped Si:P layers by Goh *et al.* [138], using the same conditions have given n_s to be $1.7 \cdot 10^{14}$ cm^{-2}. For a 0.25 ML coverage, equating to a so-called *saturation* dose of P atoms in the silicon matrix , the theoretical value is $1.7 \cdot 10^{14}$ cm^{-2} after the P incorporation anneal – in good agreement with our results.

We see from Table 6.1 that the values of μ and l are of order 70 cm^2/Vs and 10 nm for the 90 nm wire respectively, whereas for the 50 nm and the 27 nm wires, we get values of order 10 cm^2/Vs and 2 nm. This difference in mobility is very likely to be related to the different hydrogen content on the surface before Si encapsulation. The 90 nm wire was created by annealing the Si substrate to a temperature of 470 °C to incorporate the P atoms *and* to simultaneously remove the hydrogen resist layer; also demonstrated by Hallam *et al.* [67]. The 50 nm and 27 nm wire however were only annealed to a temperature of 350 °C sufficient to incorporate the P atoms [32] but leaving the hydrogen resist intact. This strategy was pursued to maximally ensure the wire integrity by minimising thermally activated P diffusion. The presence of hydrogen on the Si surface, however, not only hinders P diffusion but also Si migration [152]. This adversely affects the silicon crystal growth at a temperature of T = 250 °C which we use to encapsulate all our devices. A lower crystal quality results in more diffusive transport which is reflected in the lower values of the mobility and the mean free path. Similar values for the mobility of a Si:P δ-doped layer where the layer was deliberately exposed to atomic hydrogen before device encapsulation [167] were achieved. Here, the mobility and the mean free path was observed to drop by a factor of three from 61 cm^2/Vs and 9 nm to 25 cm^2/Vs and 3 nm due to the presence of hydrogen, whilst the electron phase coherence was observed to stay the same.

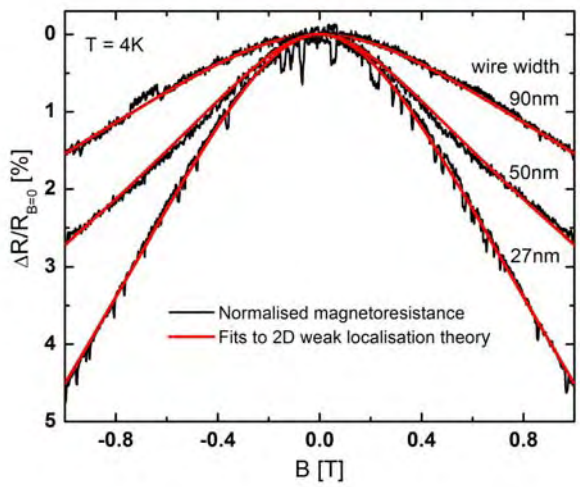

Figure 6.3: Extraction of the electron phase coherence length at T = 4 K. Normalised magnetoresistance (black traces) and corresponding fits to 2D weak localisation (red traces) of a 90 nm×900 nm wire (triangles), a 50 nm×310 nm (stars) and a 27 nm×320 nm wire (circles).

Finally, we discuss the variation of l_φ as a function of the wire width. The values for the electron phase coherence are obtained from magnetotransport measurements at T = 4 K and respective fits to the 2D weak localisation model by Hikami [71].

Fig. 6.3 shows the normalised magnetoresistance (black traces) in good agreement with the corresponding fits to 2D weak localisation theory (red traces) for the 90, 50 and 27 nm wire. The extracted values of l_φ are 32, 30 and 24 nm respectively as listed in Table 6.1.

For a 2D system, l_φ is independent of the device geometry as long as $l_\varphi \ll \{\text{system dimensions}\}$ to ensure 2D magnetotransport behaviour. From Table 6.1, we see that the electron phase coherence for the 90 and the 50 nm wire are similar, whereas the 27 nm wire is slightly lower. Since the number of wires we are comparing is not large, it is difficult to make more than a qualitative statement that the electron phase coherence decreases with decreasing wire width. However, we observe from Table 6.1, that lowering the wire width increases the ratio $\frac{l_\varphi}{w}$. From Fig. 6.3, it can be seen that the resistance correction due to weak localisation becomes more pronounced with increasing values of $\frac{l_\varphi}{w}$. For the 27 nm wire, the ratio $\frac{l_\varphi}{w}$ is 0.9 i.e. transport in the wire is in the crossover regime between 2D and 1D magnetotransport, which occurs when $l_\varphi \sim w$. Therefore, we also fitted the magnetotransport in this wire with 1D

weak localisation theory [79] and obtain exactly the same electron phase coherence length of 24 nm. A more detailed temperature-dependent characterisation of 1D weak localisation for the 27 nm wire will be discussed in Section 6.4.8.

6.3 STM study of the wire integrity as a function of wire width

The ability to contact STM-fabricated nanostructures using registration markers makes it possible to study their electrical properties accessible outside the UHV environment. This ability to measure devices in conventional cryostats allows us to perform temperature-dependent measurements allowing us to determine what scattering mechanisms limit the conduction in nanowires down to the atomic scale. Ohmic behaviour is related to the overlap of the electron wavefunction [163] between neighbouring dopant atoms so that conduction electrons can propagate from one end of the wire to the other. Therefore the formation of conducting nanowires is closely related to the preservation of the wire integrity which is influenced by P dopant placement and diffusion during the fabrication process. The atomic-resolution capability of the STM in combination with the ability to return to the same surface area after each subsequent fabrication step, using registration markers, provides an ideal tool to monitor the influence of each fabrication step on the wire integrity. We have performed separate atomic resolution imaging studies using CITS, in collaboration with Dr. Matt Butcher, to determine the smallest wire structure which remains intact using the current fabrication parameters. The narrowest wire width which we observe experimentally with the STM to be intact gives an upper bound for the smallest wire we expect to be conducting. Fig. 6.4 shows STM images of four wire patterns of 50, 36, 27 and 7 nm in width after each fabrication step. Fig. 6.4 (a) shows a hydrogen-terminated Si(100):H surface, where the hydrogen resist was locally removed using STM lithography with a tip bias of 6 V and a current of 4 nA. The exposed bare silicon dimers appear bright in 6.4 (a). The same wires are shown in Fig. 6.4 after the surface is exposed to a saturation dose of PH_3 molecules. Whilst it is not the aim of this thesis, our group has performed extensive studies investigations of the bare PH_3 dosed surface and found that all PH_3 molecules at room temperature immediately dissociate to form PH_x species (where x = 0, 1, 2) [151]. The excess hydrogen atoms thereby partially re-terminate the surface. The wire patterns shown in Fig. 6.4 (b) thereby contains a mixture of dissociative products, namely PH and PH_2. The appearance of faint, darker lines in some areas of

the wires is due to incomplete desorption of hydrogen during the lithography step.

Subsequently, the surface is annealed to 350 °C to incorporate individual P atoms from the PH_x species into the top layer of the silicon substrate. The incorporation process is accompanied by the ejection of Si [32]. The ejected Si atoms migrate on the surface to form Si chains on top of the incorporated wire pattern. Whilst these are difficult to see at this resolution, we can see from the STM images that the wires are structurally intact down to the smallest wire of 7 nm in width. We also see that the hydrogen resist remains mostly unchanged during the thermal P incorporation process.

Now, we investigate what happens to very narrow wires when they are encapsulated by a few monolayers of epitaxial silicon. We use low temperature Si molecular beam epitaxy at a temperature of 250 °C to encapsulate the incorporated P atoms to electrically activate the excess P electron. Dopant atoms are known to diffuse [158] laterally and segregate [157] to the surface at elevated temperatures. In a separate study of our group, we determined the optimal encapsulation temperature to be 250 °C [137] since this provides a balance to ensure minimal P dopant redistribution whilst providing epitaxial growth quality. Fig. 6.4 (d) shows the same surface area after the deposition of 3-5 monolayers (ML, 1 ML = 0.14 nm) of epitaxial silicon. Only a few ML of Si were initially chosen in order to facilitate imaging of the buried P-dopant wires.[1] From the STM image, the remnants of wires are barely visible and, using this standard form of imaging, it is not possible to determine if wire structures stayed intact. This STM image shows that direct STM observation of buried P-doped nanostructures at normal imaging conditions after Si encapsulation is extremely difficult.

One way to determine what happens to the position of the dopants after they are encapsulated is to perform buried dopant imaging (BDI) [183] at low STM biases. Dopant atoms in subsurface layers can locally induce band bending which changes the tunnelling current between the STM tip and the sample. As a result, buried dopants can appear as enhancements or depressions superimposed on the surfaced lattice. Brown *et al.* [183] have recently observed individual, random subsurface P dopants using P-doped Si(100) wafers with a high doping density of 5×10^{17} cm^{-3}. They found that buried P dopants appear as bright protrusions both in empty and

[1] We assume that any P atom redistribution occurs in the first few ML, but is assumed to be negligible once the P atoms are integrated into the silicon matrix due to increased bonding with the surrounding silicon.

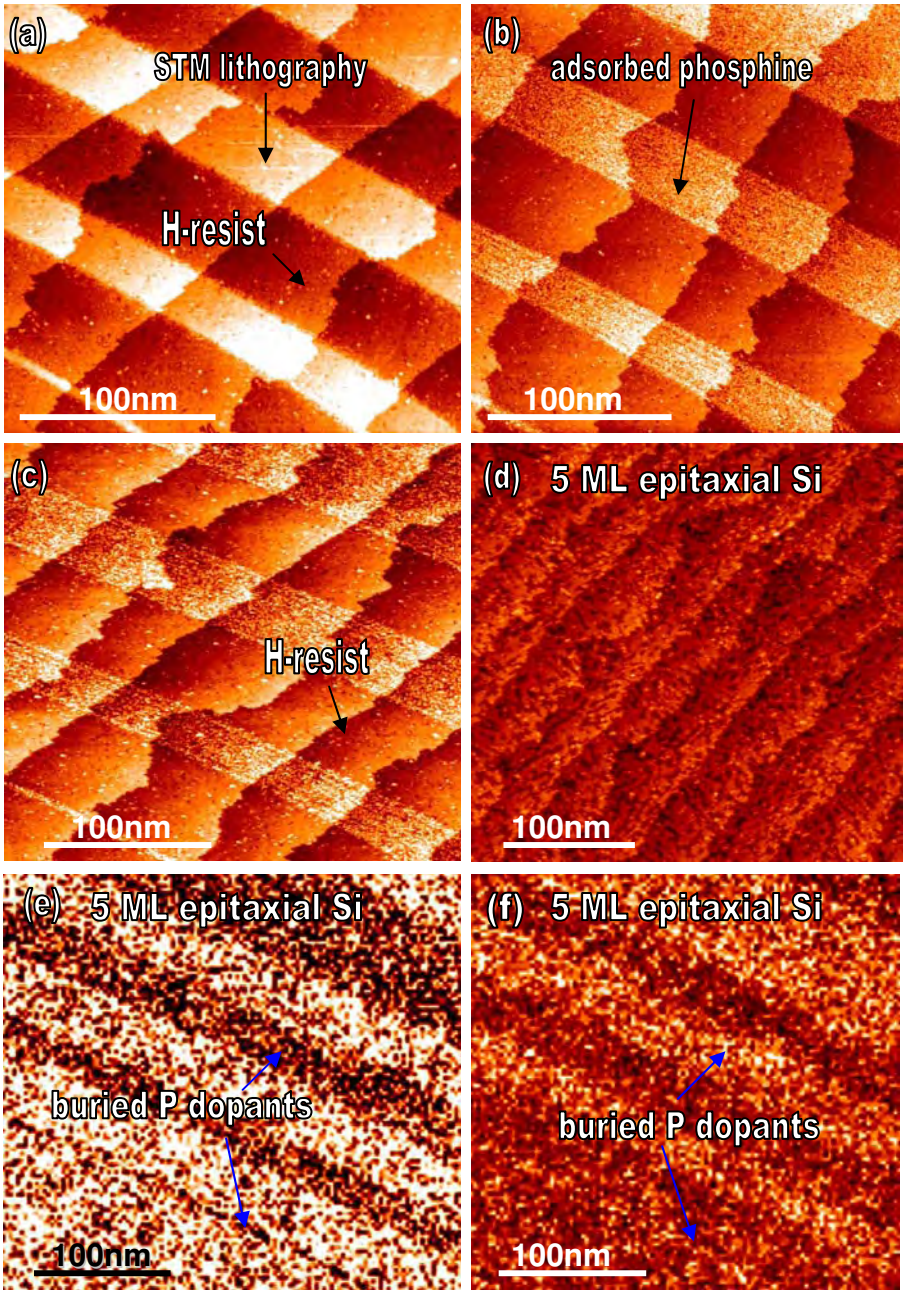

Figure 6.4: STM study of STM-patterned PH_3-dosed wires. (a) STM image of 50, 36, 27 and 7 nm wide lithographic wire patterns. (b) STM image of the same area after adsorption of PH_3 molecules onto the lithographic regions. (c) STM image after subsequent thermal P incorporation into the Si surface at 350 °C. (d) STM image of the same area after encapsulation with 5 ML of epitaxial silicon at 250 °C, where the buried P-doped wires are practically invisible. All images were taken with a bias voltage of -1.5 V and a tunnelling current of 0.15 nA. CITS images of the buried P-dopant wires for a bias voltage of (e) -0.3 V and (f) +0.22 V respectively.

filled state imaging at low biases of ∼0.5 V. In their study of the clean Si(100) surface, they also observed that the buried dopant signature was not apparent using standard bias conditions of ∼1.5 V.

Oberbeck *et al.* [184] also performed buried dopant imaging experiments on single P atoms. Here, the P atoms were introduced using PH_3 molecules on the Si(100) surface, followed by P incorporation at 350 °C, epitaxial Si encapsulation of 5 ML at 250 °C and a rapid thermal anneal at 450 °C for surface flattening. Then the surface was hydrogen terminated to terminate the Si surface states which may obfuscate the effect of buried charge due to Fermi level pinning [171]. A bright protrusion over a few Si dimers, assigned to a single buried P atom, was found in empty state imaging (positive bias) whereas no signature was found using filled state imaging at -2 V. It is possible that a signature may be found using lower bias voltage but lower bias imaging was not performed in this study.

To inspect the structural quality of our wires, we take a slightly different approach to the methods described above. Instead of imaging the silicon surface using a small, constant positive/negative voltage across the sample, we use a form of scanning tunnelling spectroscopy (STS) known as constant imaging tunnelling spectroscopy (CITS). The basic mode of operation is to keep the STM tip at a fixed point above the sample surface using a fixed tunnelling current I_0 and then measure the tunnelling current superimposed on I_0 while the bias voltage is swept from a set negative to a set positive voltage. By stepping and repeating this procedure, the I(V) response is mapped across the entire scan frame. Tersoff *et al.* [38], [39] have shown that, in the limit of small voltages and low temperature, the differential tunnelling current is proportional to the local density of states (LDOS) close to the fermi level E_F i.e.

$$\frac{dI}{dV} \sim \rho(E_F, V, \overrightarrow{r}) \tag{6.1}$$

where $\rho(E_F, V, \overrightarrow{r})$ is the LDOS for a given bias voltage at the Fermi level evaluated at the tip surface. In this picture, the STM tip is simplified as a point surface for low bias voltages such that the tunnelling barrier formed between the tip and the sample is not distorted due to the presence of the tip.

For semiconducting surfaces however, the finite bias voltage cannot be ignored, but is accommodated by an energy-dependent tunnelling coefficient $T(E, eU)$ as introduced by Hamers *et al.* [36].

$$I \propto \int \rho_s(E_F + \varepsilon)\rho_t(E_F - eU + \varepsilon) \mid T(\varepsilon, eU) \mid^2 d\varepsilon \tag{6.2}$$

Since $T(E, eU)$ favours states of higher energy, the resulting I(V) map created in our measurements may be regarded as a measure for the LDOS itself. It is well known that buried charges induce band bending. We therefore expect a different tunnelling current dependence in those areas where P dopants are buried i.e. on top of the buried wire structures. The excess electrons of the P dopants locally increase the quasi Fermi level. Such behaviour is observed for two different sample biases in Fig. 6.4 (e) and (f) respectively. Fig. 6.4 (f) presents an I(V) map of the same area as shown in Fig. 6.4 (d) taken at a voltage slice of +0.22 V (empty state). The buried wires are clearly visible down to the smallest width of 7 nm. To understand this appearance, we have to consider STM-induced band bending effects. In empty state bias, the STM tip creates an accumulation layer underneath the silicon surface which effectively pulls up the quasi Fermi levels. Since the P-doped wire regions have a slightly higher Fermi level, more electrons tunnel into the wire region. Consequently, the wires appear as bright contrast with respect to the surrounding surface. The integrity of the 50, 36 and 27 nm wires is clearly visible. For the smallest 7 nm wire, it is not clear from these images if the contrast is smeared out due to the noise in the STM image or if the P dopant have diffused such that the wire is not completely intact. The noise in the STM data is due to low contrast between topographic and electronic structure and the small tunnelling current at low biases. The resolution may be improved in future experiments by averaging over many I(V) curves and by increasing the number of scan points.

A complimentary picture is given using filled state imaging. Fig. 6.4 (e) shows the I(V) map at a voltage slice of -0.3V. Here, the buried P-doped wires appear darker attributing to a lower tunnelling current into the buried wire regions. This appearance can also be understood if we consider STM-induced band bending. In filled state imaging, the STM tip creates a depletion layer underneath the Si surface. At low biases as applied here, the excess electrons from the P dopants partially compensate for the depletion charge. This is the reason why in this case, the P-doped wire regions appear darker than the surrounding Si area. Again, the larger wires are structurally intact and the small 7 nm wire can just be distinguished from the background.

Our findings are consistent with the picture of STM-induced band bending. Similar results have been reported by Lyding and coworkers [185] who were able to map subsurface boron dopants on a hydrogen-terminated Si(100):H surface. Since boron is

STM Lithography	PH_3 dosing	Incorporation anneal	Buried STS
49 nm	50 nm	50 nm	50 nm
36 nm	39 nm	34 nm	44 nm
27 nm	27 nm	25 nm	30 nm
7 nm	6 nm	6 nm	8 nm

Table 6.2: Variation of wire dimensions after STM lithography, phosphine adsorption, P incorporation anneal at 350 °C and after 5 ML of Si encapsulation at 250 °C .

a p-type dopant, they see a current increase in filled state imaging and a decrease in empty state imaging.

Finally, we compare the changes in the wire width extracted from the STM images for each fabrication step individually. Table 6.2 summarises the variation of the wire dimensions after STM lithography, phosphine adsorption, P incorporation anneal at 350 °C and after Si encapsulation. The width of the wires stays constant within a variation of $\pm$3 nm except for the width extracted from the I(V) data for which the width is typically $\sim$5 nm longer. This increase is expected since the electrical signal is broadened due to donors being buried 5 ML underneath the surface. This finding is consistent with the observation of single P atoms by Oberbeck *et al.* [184], where the charge signature for a single P atom is spread out over 2-3 Si dimers, corresponding to a distance of $\sim$2 nm. In a subsequent overgrowth step, we have deposited a few more ML of silicon and found further broadening of the wire widths in agreement with this explanation. Despite this explanation, it is difficult to separate out any effect of lateral diffusion of the P dopants. From the STM images however, we can extract an upper bound for P diffusion of $\sim$1 nm for 5 ML of Si encapsulation at 250 °C.

We have demonstrated that our fabrication process including our optimal conditions produces P-doped nanowires that remain intact down to a width of at least 27 nm. The signature emerging from the CITS data is not conclusive for the 7 nm wire and remains the subject of further investigation. Future experiments are aimed at investigating the limits of the CITS technique and also to move towards more refined scanning tunnelling spectroscopy (STS). We will come back to the formation and electrical characteristics of sub 10 nm wires in Section 6.5. The focus of the following section is devoted to a detailed, temperature-dependent electrical characterisation of the 27 nm wide wire.

6.4 Detailed electrical characterisation of a 27 nm wide wire

This section is dedicated to detailed measurements of a 27 $\times$ 320 nm^2 wire. Fig. 6.5 (a) shows a high-resolution STM image of the Si(100) surface after sample preparation and hydrogen termination on a 1$\times$1 cm^2 sample patterned with registration markers. This image demonstrates, that we can achieve atomic resolution imaging on large sample sizes, with a near perfect hydrogen resist layer consisting of monohydrides with the occasional occurrence of dihydrides (DH) i.e. two hydrogen atoms forming a bond with a single Si atom. Low defect densities are achieved in the device area, where only a few defects are present which are mainly single dimer vacancies (DV). Using STM lithography (6 V, 4 nA), we pattern the hydrogen resist layer into a 27 nm wire structure between prefabricated registration markers as shown in Fig. 6.5 (b). At each end of the wire, a 2.5 μm wide square is patterned to subsequently make external contacts to the device. The exposed area of bare Si(100) surface, which is highly reactive to the adsorption of molecular species such as PH_3, appears brighter than the surrounding, hydrogen resist layer due to the additional tunnel current contributed by the Si surface states [171].

It is noteworthy that the presence of monoatomic steps in the device area in Fig. 6.5 (b) is not due to the registration markers causing step bunching of the surface but is due to the wafer miscut. A similar step structure is seen on unpatterned samples of the same wafer. After dosing with PH_3, we anneal the substrate to $\sim$350 °C to incorporate P atoms in the silicon surface layer. The device is then encapsulated with $\sim$25 nm of epitaxial silicon grown at 250 °C [137] at a growth rate 0.5 $\frac{\mathring{A}}{s}$ by our MBE postdoctoral researcher Dr. Lars Oberbeck. Once the sample is removed from the UHV environment, we use the registration markers to align macroscopic Al contacts defined by optical lithography to the buried structure. Subsequent annealing to $\sim$350 °C for 15 min causes the Al to diffuse to the buried structure thereby forming an ohmic contact [168]. Optical microscope images after the alignment of Al contacts are shown in Fig. 6.5 (c,d). From Fig. 6.5 (c) we can estimate the alignment accuracy of the metal contacts with respect to the triangular and square markers to be $\sim$500 nm. This alignment accuracy is sufficient to allow the alignment of external metal contacts by optical lithography to the 2.5 μm wide squares defined by STM lithography. After the device is packaged, a gold ball bonder is used to connect Au wires from the four Al terminals to the chip package. Thereafter, the device chip is ready to be loaded into

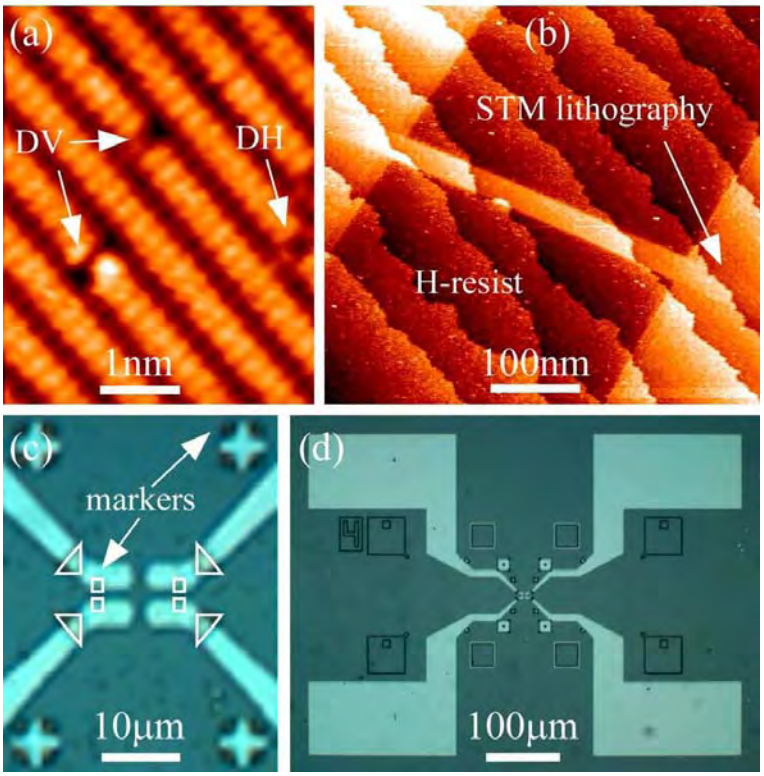

Figure 6.5: Fabrication process of a 27 nm wide Si:P wire. (a) High resolution STM image (bias voltage: -1.5 V, current: 0.2 nA) of the hydrogen-terminated surface, where each Si atom bonds to a single hydrogen atom. A few dihydrides (DH), where each Si atom forms a bond with two hydrogen atoms are present. A low defect density (<1.5 %) of only two single dimer vacancies (DV) is visible. (b) STM image (bias voltage: -2 V, current: 0.15 nA) of a 27 nm wide exposed Si wire pattern (bright area) after performing STM lithography on a Si(100):H surface. (c) Optical microscope images of the central device area after alignment of Al contacts to the registration markers. The original etched registration markers are outlined in white for clarity. (d) Optical microscope image of the completed device.

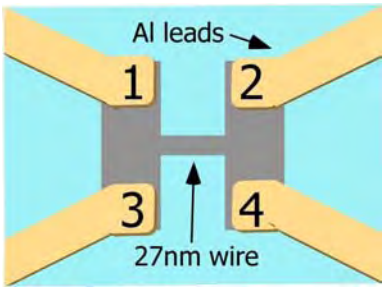

Figure 6.6: Schematic of the 27 nm wire device. Four Al leads (1-4) form ohmic contact to two buried P-doped side patches connected to the 27 nm wide and 320 nm long wire.

current direction	1-3	2-4	1-2	3-4	1-4	3-2
R_{2T} [kΩ]	12	11	60	60	61	62

Table 6.3: Two terminal resistances of the 27 nm wide wire. AC measurements of the six contact combinations (see Fig. 6.6): the P-doped side contacts (1-3, 2-4), across the device (1-2, 3-4) and diagonally across (1-4, 3-2) using an excitation voltage of 100 μV and a lock-in frequency of 4 Hz at T = 4 K

a 4 K, in-house manufactured, liquid helium magnet dip rig for initial device characterisation.

6.4.1 Device characterisation at 4 K

The standard test for each device chip is to check the current for each of the six two terminal combinations given by the four terminals at a fixed AC excitation voltage of 100 μV using standard lock-in amplifiers at a measurement frequency of 4 Hz. Fig. 6.6 shows a schematic of the device including terminal labels. This test allows us to check if the device is properly contacted and allows us to identify if there are any bad contacts. The results are counterchecked with a control sample, where no STM patterning has taken place to eliminate if potential current flow may arise from improper processing which could potentially result in shortening of some terminals. Performing this test in addition to an optical microscope inspection of the final device is good practice to conclude that device conduction truly stems from the buried P-dopant structures patterned by the STM. Table 6.3 summarises the six two terminal resistances of the 27 nm wire device. The two P doped side patches (1-3, 2-4) exhibit a resistance of 12 kΩ and 11 kΩ for the left and the right patch respectively. The values of R_{2T} for contacts 1-2 are slightly lower than the resistance for contacts 1-4 diagonally across the device as expected. The measured resistances are symmetric across the device and

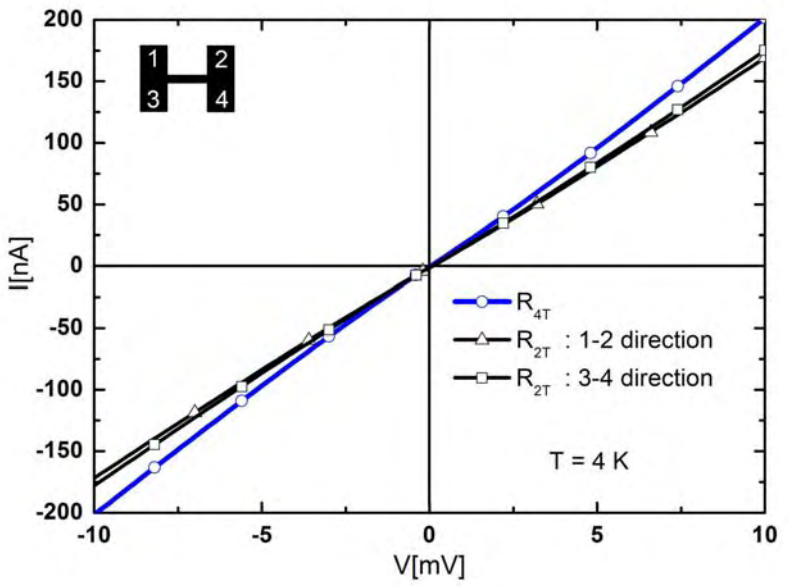

Figure 6.7: Two and four terminal I-V characteristics of the 27 nm wide wire at 4 K. Ohmic behaviour is found up to a DC voltage of 10 mV giving a four terminal resistance of 50 kΩ for both current directions. The DC voltage was limited to 10 mV due to high current densities in excess of 1200 $\frac{kA}{cm^2}$. The corresponding two terminal I-V curves with current flowing in the 1-2 and 3-4 direction respectively show a slightly higher resistance of 57 kΩ due to the contact resistances of ∼7 kΩ.

exhibit similar contact resistances for both sides. The current for the control device at 100 μV was below the current measurement limit of 1 pA, giving resistances in excess of 100 MΩ, highlighting that conduction in the 27 nm wire stems from the buried P dopants.

We then go on to measure the four terminal resistance and the contact resistance of the 27 × 320 nm^2 wire device. Fig. 6.7 shows a four terminal DC I-V trace up to 10 mV for the 27 nm wide wire at 4 K. Ohmic conduction with four terminal resistance of 50 kΩ is observed up to sample currents as high as 200 nA, equating to high current densities in excess of 1200 $\frac{kA}{cm^2}$ comparable to the capacity of highly doped Si nanowires [182]. We have also included the two terminal I-V characteristics for both the 1-2 and 3-4 current direction. The two I-V curves are slightly different due to slightly different contact resistances. By comparing the two terminal and the four terminal traces we extract contact resistances of ∼3.5 kΩ/contact.

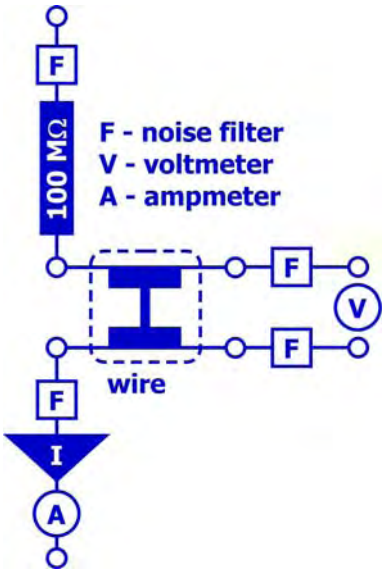

Figure 6.8: Schematic of the electronic circuit for magnetotransport measurements in the dilution refrigerator.

6.4.2 Electrical measurement setup for low temperature measurements

Millikelvin magnetotransport measurements were then performed in a Kelvinox K100 He_3/He_4 dilution refrigerator equipped with a 10 Tesla superconducting magnet fabricated by Oxford Instruments, UK. Fig. 6.8 shows a diagram of the electric circuit. As will be discussed in more detail in Section 6.4.3, all measurements are performed in constant current mode to avoid measurement artifacts arising from sample heating. We use a 100 MΩ resistor to define the constant current of 200 pA for all temperatures. Passive, low-pass filters (Minicircuits BLP 1.9 MHz labelled (F) in Fig.8.10) are employed for each electric line leading to the fridge core to minimise the influence of environmental electromagnetic noise. Further filtering is applied using *cold filters* installed at the 1 K pot plate close to the device. They consist of a passive, R-C circuit (with C = 30 nF and R = 100 Ω) exhibiting a turn-over frequency of 50 Mhz. A Stanford current preamplifier (SR 570) is used for signal enhancement before the current is fed to a Keithley 5210 lock-in amplifier with a chosen operating frequency of 5 Hz. Another Keithley 5210 lock-in amplifier reads the voltage drop at the wire device thus allowing four terminal resistance measurements.

During the course of the measurements, we found three main challenges had to be overcome for accurate temperature-dependent magnetoresistance (MR) measure-

ments of such thin wires. These were sample heating, avoiding the influence of adiabatic demagnetisation effects and protection from electromagnetic noise. By using appropriate external and internal electromagnetic noise filters, electromagnetic noise was eliminated above frequencies of order MHz. In the following two sections, we demonstrate how we measured and minimised the effects of Joule heating and adiabatic demagnetisation.

6.4.3 Effect of Joule heating on the resistance at millikelvin temperature

Joule heating, caused by the diffusive motion of the conduction electrons, is known to be a critical issue for device heating at low temperatures. High currents can cause sample heating through the wire leading to a significantly higher sample temperature and thus sample resistance compared to the bath temperature. We performed a calibration experiment by varying the device current at a temperature of 300 mK to rule out sample heating in our device. Fig. 6.9 shows the measured the four terminal R_{27}[I] as a function of the sample current through the wire measured at a lock-in frequency of 11 Hz. A large resistance variation ranging from 120 kΩ to 58 kΩ was found as the driving current was changed from ∼100 pA to 14 nA. We can see that as the current is increased, the resistance decreases since there is heating in the sample giving rise to lower resistance values at higher temperatures. At 14 nA, Joule heating was observed to cause an observable increase of the mixing chamber temperature of the fridge, proving that the resistance variation is indeed due to heating.

Fig. 6.10 represents a magnified version of Fig. 6.9 on a semi-logarithmic scale for device currents <500 pA. For measurement currents below 200 pA, the measured four terminal resistance becomes independent of the device current indicating that heating is no longer occurring. Therefore, we have chosen a constant current measurement technique with a current amplitude of 200 pA for all future experiments. Finally, the importance of a suitable device current to obtain reliable data is summarised in Fig. 6.11. Here, we measured the temperature dependence of the device resistance between 150 mK and 4 K for various device currents from 0.2 nA, 0.5 nA, 5 nA to 15 nA. At 4 K, the measured resistance is independent of the sample current. For lower temperature however, device currents of 0.5 nA and above lead to a saturation of the four terminal resistance R_{27}[T,I] at lower temperatures due to heating. Only for a sample current as little as 0.2 nA was the resistance found to increase continually down to the minimum measured temperature of 150 mK. For a device current of 0.2 nA, we have

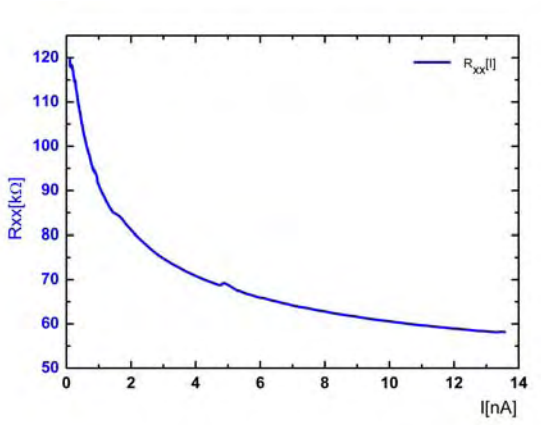

Figure 6.9: Four terminal resistance R_{27}(I) at T = 300 mK as a function of the sample current . Current induced sample heating varies the actual sample temperature such that a large resistance variation occurs ranging from 120 kΩ to 58 kΩ.

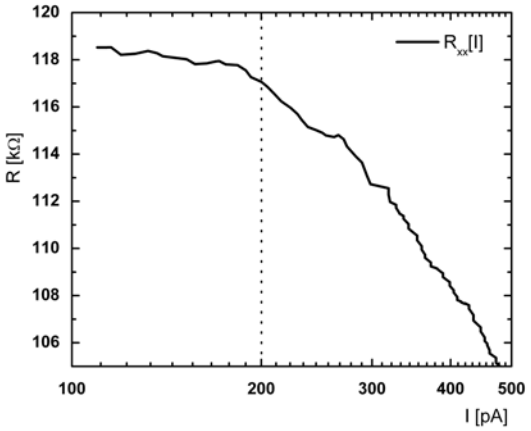

Figure 6.10: Four terminal R_{27}(I) dependence for smaller device currents at T = 300 mK. Below currents of 200 pA, the device resistance becomes independent of the driving current.

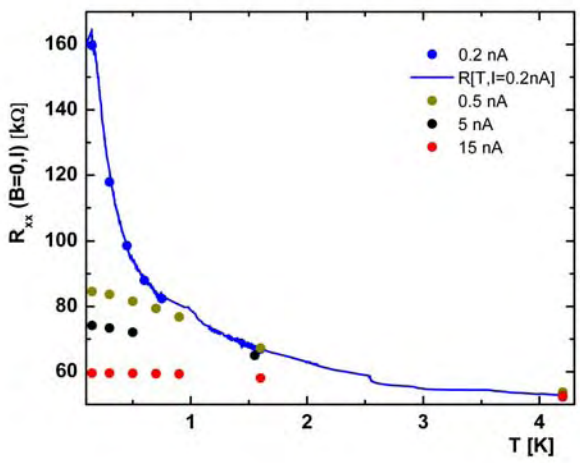

Figure 6.11: Comparison of the temperature-dependent four terminal device resistance R_{27}(T,I) for different currents to illustrate the effect of sample heating. At 4 K, the device resistance is independent of the sample current. For lower temperatures, different sample current leads to resistance saturation due to Joule heating. For a sample current of 200 pA, the device resistance shows no saturation over the whole measured temperature range. Blue trace is a continuous R_{xx} measurement during fridge warm-up.

also determined R_{27}[T] in a continuous temperature-dependent measurement of the fridge warm-up (blue trace) – rather than at fixed temperatures. The acquired resistance curve fits beautifully onto the same points discrete temperatures confirming the reproducibility of our measurements.

6.4.4 The influence of magnetic field sweep rate

At low temperatures, the presence of magnetic impurities either in the device, the contact material or the chip package may lead to the observation of an effect known as *adiabatic demagnetisation*. Potential candidates are the sample holder (shantec) used in some Kelvinox dilution refrigerators manufactured by Oxford Instruments, magnetic contamination in the metals used to contact the device or the presence magnetic trace elements in the chip package. For the MR measurements presented in this section, we have used a non-magnetic shantec holder and Al metal contacts of 5N or 99.999% purity Al (for more details see also Section 6.4.11). As such, both of these are not a likely source of magnetic traces. The most likely source of magnetic material comes from the commonly used chip packages (type: leadless chip carrier LCC02034 fabricated

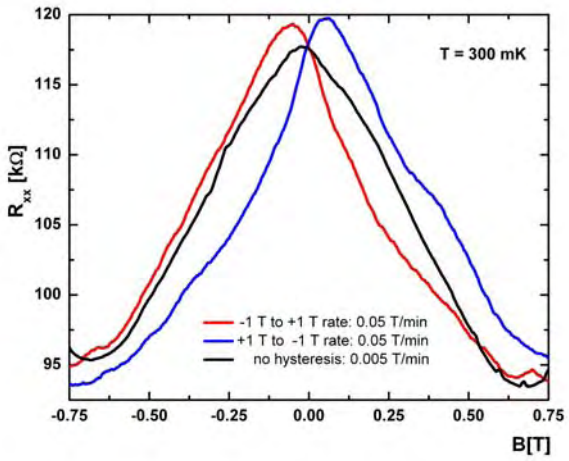

Figure 6.12: Sweep rate dependence of the observed magnetoresistance at T = 300 mK. Adiabatic magnetisation and demagnetisation of magnetic impurities in the sample holder and stage (shantec) lead to cooling when sweeping the magnetic field towards zero magnetic field and induce heating whilst sweeping away from zero-field. The effect is eliminated by slowly sweeping the magnetic field such that the temperature bath becomes coupled non-adiabatically.

by Spectrum Semiconductor), where residues of nickel (Ni) are known to be present. Indeed, measurements[2] performed at the University of Cambridge, UK, of the magnetoresistance of such chip carriers without a device present showed the occurrence of adiabatic heating effects which can affect the sample temperature.

Adiabatic demagnetisation causes sample heating and cooling when the magnetic field is swept quickly around B = 0. The key for the temperature change arises from magnetisation of the magnetic particles in the chip package. Generally a thermodynamic process is thought of being adiabatic if they occur so quickly that the system under investigation is not coupled to its environment, the temperature bath. The red trace in Fig. 6.12 shows the magnetoresistance as the magnetic field is swept from -1 T to +1 T at a constant sweep rate of 0.05 T/min, whereas the blue trace shows the MR when swept in the opposite direction. In both cases, the resistance increases, when sweeping towards zero and decreases significantly while sweeping away from zero magnetic field. This effect is a direct consequence of local temperature change originating from adiabatic demagnetisation of the magnetic impurities in the chip package.

[2]Private conversation with A/Prof. Alex Hamilton

As a consequence of this demagnetisation, the sample temperature is not constant but decreases as the magnetic field is swept towards B = 0. As such, the resistance of the 27 nm wire increases, whereas sweeping away from B = 0 causes sample heating which lowers the device resistance again.

We have found that we can maintain a constant sample temperature when sweeping the magnetic field slowly enough, such that the sample is in quasi-equilibrium with the temperature bath of the dilution refrigerator. This is shown as the black trace in Fig. 6.12. Here the forward and backward sweep sit on top of each other when the sweep rate is reduced to 0.005 T/min. Interestingly, the zero-field resistance does not change significantly for all traces. However the general shape is affected which is important since the shape dictates the phase coherence lengths of l_φ extrapolated from weak localisation fitting. Therefore it is crucial to prevent effects due to adiabatic demagnetisation. This can be achieved using sweep rates of 0.005 $\frac{T}{min}$ and lower.

6.4.5 Four terminal resistance from 200 mK to 110 K

Having established the magnetic field sweep rate and the sample current necessary to prevent heating of the sample, we have characterised the wire resistance over a large temperature range during the slow warm-up of our dilution refrigerator. This process takes about four days during which the resistance was measured in intervals of 10 s. Since we use conducting substrates for STM-based device fabrication for imaging with a room temperature resistivity of 1 – 2 Ωcm (corresponding to a substrate doping level of 10^{15} cm^{-3}), the substrate will conduct at higher temperatures. In order to determine at what temperatures the substrate starts to conduct, we fabricated an unpatterned, four terminal control device, where Al contacts are evaporated and annealed into the substrate only. Fig. 6.13 shows the measured device resistance for the 27 nm wide wire from 10 K to 110 K. We also measured the current through the control device for a constant AC excitation voltage of 100 μV. From the graph, it is seen that the substrate starts to conduct for temperatures above ∼70 K. Therefore we restrict the discussion of the electrical results of the 27 nm wire to temperatures below 65 K (dotted line in Fig. 6.13).

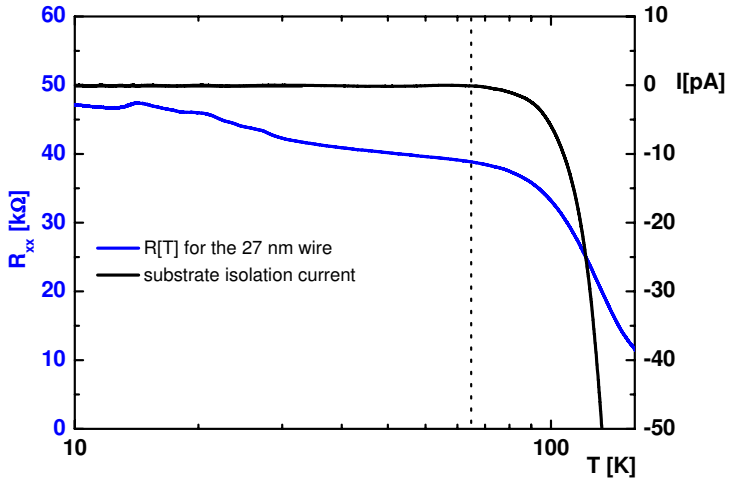

Figure 6.13: Four terminal resistance as a function of temperature for 27 nm×320 nm wire control device. The onset of substrate conduction (black trace) above ∼70 K makes electrical measurements of the wire (blue trace) above this temperature unreliable.

6.4.6 Overview of the temperature-dependent resistance

Fig. 6.14 shows the zero-field four terminal resistance of the 27 nm wire from 200 mK to 65 K. Over this temperature range, the resistance decreases from 150 kΩ to 39 kΩ. Note that some *bumps* in the resistance data stem from differences between the actual sample electron temperature and the thermometer and are not expected to be a characteristic feature of the observed resistance. In the following, we will give an outline of the different transport regimes that take place in this wire. A detailed analysis and derivation of the emerging device parameters will be discussed in the following sections. At low temperatures, conductance corrections from the Drude conductance arise due to both, weak localisation and electron-electron interaction. The effective dimensionality of the sample and thus of weak localisation is determined by the relation between the coherence length, l_φ, and the wire width, w. If l_φ is much smaller than w, the conduction electrons do not *see* their confinement and the weak localisation correction is essentially two-dimensional. If the coherence length exceeds w i.e. $l_\varphi > w$, the wire boundaries constrict the maximum size and shape of the backscattering loops since only loops with an area $S = l_\varphi \cdot w$ are formed. In this case the weak localisation effect is said to be one-dimensional.

From 1D weak localisation measurements, which will be discussed in Section 6.4.8, the phase coherence length was found to be 24 nm at T = 4 K comparable to the wire width w. Note, that we have obtained the same l_φ from 2D weak localisation theory

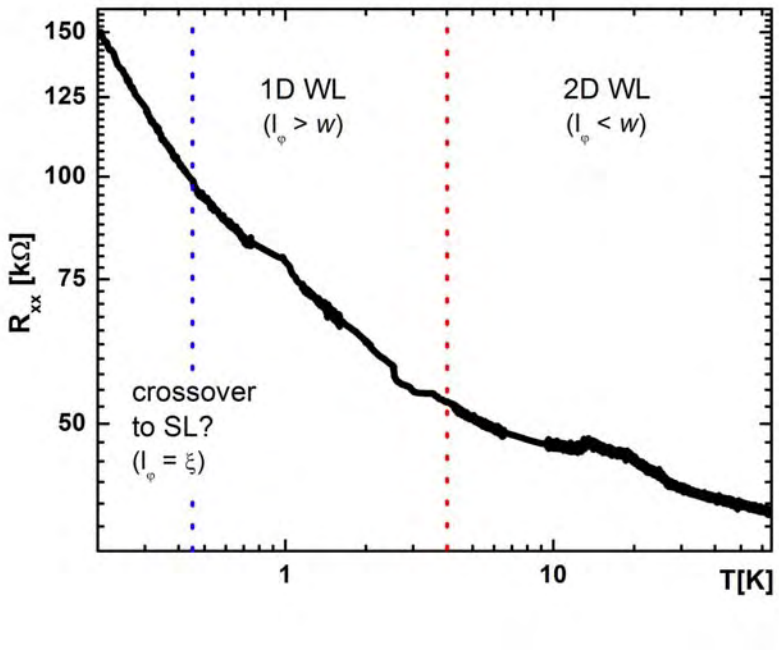

Figure 6.14: Four terminal resistance of the 27 nm wire from 200 mK to 65 K. The dotted lines divide the resistance into three regimes. Above 4 K, the resistance behaviour of the wire with width w = 27 nm is described by 2D weak localisation ($l_\varphi < w$), where electron-phonon interactions dominate dephasing. Below 4 K, the sample crosses over into the 1D weak localisation regime ($l_\varphi > w$). At very low temperatures, we propose a crossover to strong localisation as the phase coherence length, l_φ, approaches the localisation length, ξ.

[71] at this temperature. However, at temperatures below 4 K, the magnetotransport data could only be fitted with 1D weak localisation theory. At very low temperatures, l_φ becomes $\sim$50 nm i.e. longer than the wire width. Whilst we are in the 1D magnetotransport regime, we also propose a crossover from weak localisation to strong localisation. Such a crossover occurs if the electron's localisation length ξ becomes comparable to the temperature-dependent phase coherence length. The localisation length for this device is $\xi \approx 100$ nm, whereas l_φ = 50 nm at T = 450 mK. Given that the crossover condition $\xi \sim l_\varphi$ gives only an order of magnitude character, it is possible that we observe the onset of strong localisation at temperatures below 450 mK. The three different conductance regimes for the 27 nm wire as a function of temperature are shown in Fig. 6.14 and can be identified as follows:

1. **2D weak localisation: 4 K – 65 K:**
   Above $\sim$4 K, the electron phase coherence length l_φ becomes comparable to the wire width w and the conductance correction due to weak localisation is found to be in a crossover regime between 1D and 2D magnetotransport. At higher temperatures, weak localisation becomes clearly two dimensional and can only be fit using 2D theories. In Section 6.4.7, we will see that we can explain the dominating dephasing mechanism at higher temperatures is due to electron-phonon interaction.

2. **1D weak localisation and electron-electron interactions: 4K – 450 mK:**
   Below $\sim$4 K, the electron phase coherence length l_φ becomes smaller then the wire width w and we enter the regime of 1D weak localisation. A detailed analysis of magnetotransport measurements at temperatures from 300 mK to 4 K is presented in Section 6.4.8. At low temperatures, *electron-electron interactions* present a further correction to the Drude resistance. The dimensionality of electron-electron interactions is given by the thermal length, defined as $l_T = \sqrt{\frac{\hbar D}{kT}}$. Similar to the crossover for weak localisation, a crossover from 1D to 2D interaction theory occurs when l_T becomes comparable to the wire width w, i.e. $l_T \sim w$. For the 27 nm wire, the thermal length is l_T = 30 nm at 4 K. Therefore 1D theory will be used in Section 6.4.10 to describe the conductance correction due to electron-electron interaction below 4 K.

3. **Crossover to strong localisation: $<$450 mK:**
   In Section 6.4.11 we apply a variable range hopping model to investigate the

possible onset of a strong localisation crossover at very low temperatures, when the localisation length, ξ becomes comparable to the electron phase coherence length l_φ.

6.4.7 Electron-phonon interaction above 4 K

From the phase coherence length of l_φ = 24 nm obtained from 1D weak localisation measurements at T = 4 K (Section 6.4.8), we deduce that a temperature-dependent crossover from 1D to 2D weak localisation occurs at a temperature of about 4 K. At this temperature, the fitted electron phase coherence length becomes comparable to the wire width i.e. $l_\varphi \sim w$ and the formation of phase coherence loops in the sample is no longer restricted by the wire width.

The formulation of 2D weak localisation theory predates 1D weak localisation going back to the original work by Anderson. Whereas Anderson *et al.* [186] developed their theoretical concepts embedded in a scaling theory description of conductance, Gorkov *et al.*'s [187] provided a complementary approach to conductance behaviour utilising perturbation theory. Later on, Bergmann's [188] and Khmel'nitskii's [189] picture of weak localisation as a consequence of enhanced coherent backscattering resulting from quantum-mechanical interference provided an insightful interpretation of this macroscopically observable quantum effect. Lee and Ramakrishnan [94] have written a review concerning the scaling theory approach. Beenakker and van Houten [70] provide an excellent review of weak localisation. Altshuler *et al.* [190] provided an expression derived for the conductivity correction in a two dimensional, disordered metal:

$$\Delta\sigma_{2D} = -g_s g_v \frac{e^2}{4\pi^2\hbar} ln\frac{\tau_\varphi}{\tau} \tag{6.3}$$

with $\Delta\sigma = \sigma_{xx} - \sigma_0$, where σ_0 is the Drude conductivity, $g_{s,v}$ are the spin and valley degeneracy respectively. τ_φ and τ are the electron phase relaxation and the momentum relaxation time respectively. Assuming g_v = 1 and g_s = 2 and since $\tau_\varphi \sim T^{-p}$ is typically assumed for all dephasing mechanisms, Eq. 6.3 reduces to:

$$\Delta\sigma = p\frac{e^2}{2\pi^2\hbar} ln\frac{T}{T_0} \tag{6.4}$$

where T_0 is a measure of the strength of the inelastic coupling [81]. The measured conductivity therefore is expected to follow

$$\sigma_{xx} = cst + p\frac{e^2}{2\pi^2\hbar} lnT \tag{6.5}$$

with $cst := \sigma_0 + p\frac{e^2}{2\pi^2\hbar} lnT_0$.

By fitting the measured conductivity, it is possible to extract the value of the parameter p which gives direct information about which temperature-dependent dephasing mechanism is prevalent in our wires over this broad temperature regime.

It is interesting to note that the Hikami expression used for fitting 2D magneto-transport data in this thesis also reduces to 6.5 in the limit $B \rightarrow 0$. Recall the familiar Hikami expression:

$$\Delta\sigma = \frac{e^2}{2\pi^2\hbar}\left[\Psi\left(\frac{1}{2}+\frac{\tau_B}{2\tau}\right) - \Psi\left(\frac{1}{2}+\frac{\tau_B}{2\tau_\varphi}\right)\right] \tag{6.6}$$

where $\tau_B = \frac{\hbar}{2\cdot e\cdot B\cdot D}$ and Ψ is the *digamma* function. In the zero-field limit, the digamma function behaves asymptotically as $\Psi(x) \approx lnx - \frac{1}{x}$. Assuming also, that $\tau_\varphi \gg \tau$, Eq. 6.5 is recovered.

Electron-phonon interaction becomes important at higher temperatures and eventually becomes the governing dephasing mechanism dictating the temperature dependence of τ_φ and thus the conductance correction due to 2D weak localisation. The theoretical foundation of electron-phonon scattering was laid out by Pippard. In his pioneering work, Pippard [85] considered the interaction between phonons and electrons scattering from impurities and defects. According to [85], the electron-phonon interaction depends essentially on the parameter $q_T l$, where q_T is the transversal phonon wave vector, and l is the electron mean free path. In the large disorder/dirty limit $q_T l << 1$, the electron-phonon coupling is a factor of $q_T l$ weaker than the coupling in the pure/clean limit, where $l \rightarrow \infty$. Therefore a theoretical temperature-dependence of $\tau_\varphi \propto T^{-4}$ is obtained in the *high disorder* limit, whereas a $\tau_\varphi \propto T^{-3}$ is predicted for the *pure metal* limit characterised by $q_T l >> 1$. Following on from Pippard's work, Rammer and Schmid [84] showed that the phase breaking rate due to electron-phonon interaction is identical to the inelastic collision rate. Only a few reports exist which actually observe the high disorder limit. For example, Komnik *et al.* [191] showed that τ_φ converged to the T^{-4} dependence dictated by electron-phonon dephasing in disordered bismuth films. More recently, Gershenson *et al.* [192] reported that the electron cooling time, related to the electron-phonon coupling, also follows the T^{-4} law.

Most groups [86], [87], [88], [89], [90] experimentally observed neither a T^{-4} or a T^{-3} dependence as suggested by theory. Instead, they found that the experimental data could be well described by a T^{-2} law of the dephasing time τ_φ. Lin and Bird [78] have written a comprehensive review on this discrepancy between theory and

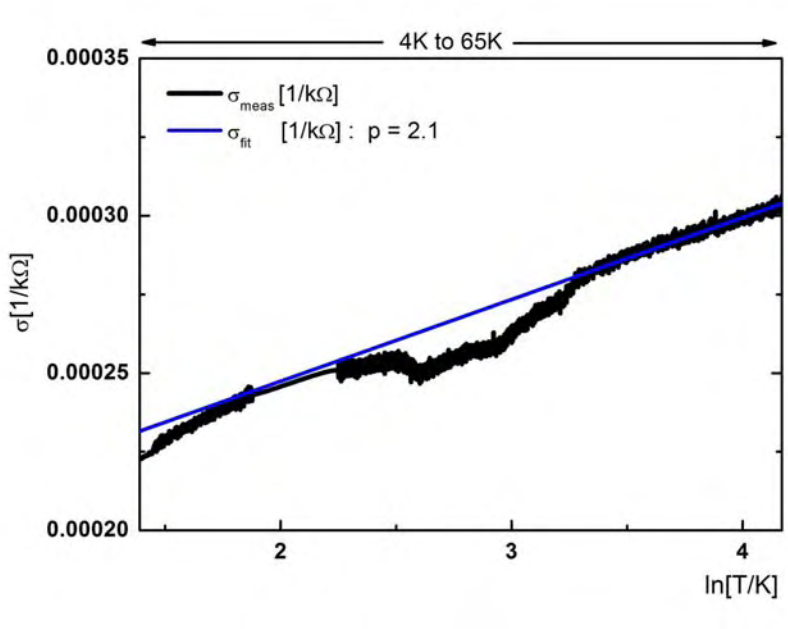

Figure 6.15: The temperature dependence of the conductivity of the 27 nm × 320 nm wire from 4 K to 65 K. The observed conductance change (black trace) is due to electron-phonon dephasing in the intermediate disorder limit (blue fit with p ∼ 2).

experiment, also summarising many experiments. It is believed, that the origin of the T^{-2} law arises from an intermediate level of disorder but no theoretical fundament has been established to confirm this assumption to date.

We can estimate the level of disorder in our system using

$$q_T l = \frac{k_B T l}{\hbar v_s} \tag{6.7}$$

from [78], [85], [84] we obtain

$$q_T l = 0.044 \cdot T[K] \tag{6.8}$$

where we have used the estimate the velocity of sound in Si(100) after Saviot *et al.* [193], namely v_s = 9017 ± 230 $\frac{m}{s}$, and a mean free path l of 3 nm. In the temperature range between 4 K to 65 K, the value for $q_T l$, using Eq. 6.8, changes from 0.2 to 2.9 and becomes unity at T ∼23 K . Therefore, it might be expected we have an intermediate level of disorder as observed in other experiments with a T^{-2} dependence. Fig. 6.15 shows the conductivity for the 27 nm wide and 320 nm long wire plotted as a function of lnT. Such a plot allows us to identify the region of constant p values as easily seen

from Eq. 6.5. A linear region extending from 7 K to 65 K is immediately visible. Applying a linear fit, using Eq. 6.5, we obtain a p value of 2.1 $\pm$ 0.03. Note that the *bumps* in the data are a consequence of a discrepancy between the thermometer and the actual electron temperature of the sample. It is worth noting that the extrapolated p values are directly proportional to the valley degeneracy g_v which allows us to confirm a valley degeneracy of $g_v = 1$. A valley degeneracy of $g_v = 1$ is also obtained from weak localisation fitting in Section 6.4.8. A p value of 2 corresponds to a power law of T^{-2}, thus confirming that the dominant dephasing mechanism in the wire at higher temperatures up to 65 K is caused by electron-phonon scattering in the intermediate disorder regime as observed by many other groups [78]. At low temperatures, τ_φ is seen to deviate from the T^{-2} law [191], [194] as electron-phonon interactions become negligible. In the following section, we discuss what happens below 4 K.

6.4.8 1D weak localisation corrections below 4 K

One dimensional weak localisation occurs when the electron phase coherence length l_φ becomes larger than the sample width w, i.e. $l_\varphi > w$. In the presence of a magnetic field, the constructive interference between forward and time-reversed loop is destroyed for loop sizes larger than the square of the magnetic length $l_m^2 = \frac{\hbar}{eB}$ since both paths pick up different Aharanov-Bohm phases resulting in a phase difference of $\phi \sim 1$ [70]. As a consequence, 1D weak localisation in the presence of a magnetic field only occurs if both, the electron phase coherence length and the magnetic length are larger than the wire width that is $l_\varphi \wedge l_m > 0$.

At sufficiently high magnetic fields, a transition from 1D to 2D weak localisation can occur if l_m becomes comparable to w. This dimensional crossover happens when $l_m = \frac{1}{2}w$. Recalling the definition of the magnetic length $l_m = \sqrt{\frac{\hbar}{eB}}$, the crossover condition becomes

$$B_{1D\rightarrow 2D} = \frac{4\hbar}{ew^2} \tag{6.9}$$

For a 27 nm wire, $B_{1D\rightarrow 2D}$ = 3.6 T. We constraint our fits in this section to a magnetic field range of $\pm$0.5 T, so that we are far away from a transition from 1D to 2D weak localisation in the presence of a magnetic field.

Altshuler *et al.* [76] provided an expression for 1D weak localisation in highly

disordered metals (dirty limit) as

$$\delta G_{WL}(B) = -g_s g_v \frac{De^2}{hL}\left(\frac{1}{\tau_\varphi^2}+\frac{1}{\tau_B^2}\right)^{-\frac{1}{2}} \tag{6.10}$$

where g_s and g_v are the spin and valley degeneracies respectively, D is the diffusion constant, L the wire length, τ_φ the inelastic scattering time and τ_B is the characteristic decay time of the correlator of the time-reversal operator in the presence of a magnetic field. τ_B is defined over the wire geometry. For a wire with rectangular cross section [76], [70], which we assume to be the most suitable geometry for our planar P-doped wires,

$$\tau_B = \frac{3l_m^4}{Dw^2} \tag{6.11}$$

Using the definition of l_m, equation 6.10 then becomes

$$\delta G_{WL}(B) = -g_s g_v \frac{e^2}{hL}\left(\frac{1}{l_\varphi^2}+\frac{e^2B^2w^2}{3\hbar^2}\right)^{-\frac{1}{2}} \tag{6.12}$$

The zero-field conductance correction due to 1D weak localisation reduces to

$$\delta G_{WL}(B=0) = -g_s g_v \frac{e^2}{hL}\cdot l_\varphi \tag{6.13}$$

We can see from Eq. 6.13 that the zero-field conductance correction due to weak localisation is proportional to the phase coherence length l_φ. Therefore the temperature-dependent evolution of the sample conductance is expected to follow the same behaviour as $l_\varphi[T]$. We will return to this interesting observation at the end of the analysis of the weak localisation data.

For the fitting of the magnetoresistance data, we subtracted Eq. 6.13 from Eq. 6.12 to obtain the following conductance correction, also used by Pooke *et al.* [195]

$$\Delta G(B) = \delta G_{loc}(B=0) - \delta G_{loc}(B) = \alpha\frac{2e^2}{hL}\left[L_\phi - \left(\frac{1}{l_\varphi^2}+\frac{e^2B^2w^2}{3\hbar^2}\right)^{-1/2}\right] \tag{6.14}$$

Here we have set $g_s = 2$ and $g_v = 1$, such that α is a prefactorial fit parameter of order of unity.

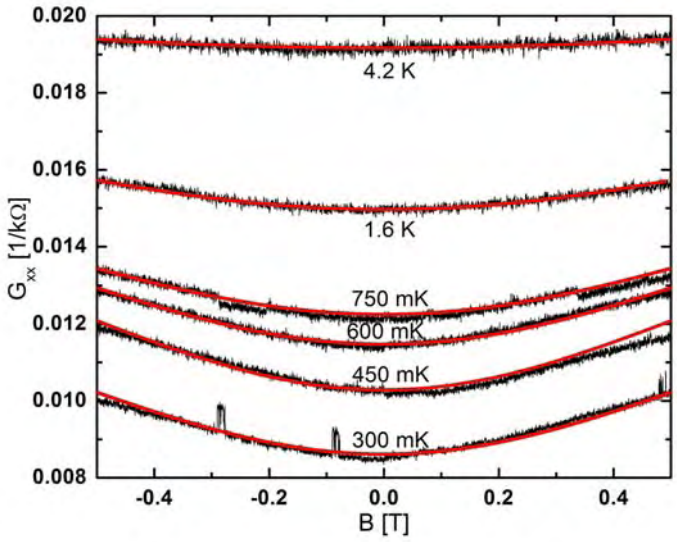

Figure 6.16: Four terminal magnetoconductance in the temperature range from 300 mK to 4 K for a 27 nm wire. Red lines are fits to Altshuler's 1D weak localisation theory [76] given by Eq. 6.14.

6.4.9 Temperature dependent electron phase coherence

We have performed magnetotransport measurements over the temperature range from 300 mK to 4 K in a dilution refrigerator using the measurement setup described in Section 6.4.2. Employing a constant current of 200 pA, we are able to avoid Joule heating as discussed in Section 6.4.3. Weak localisation traces were taken at six distinct temperatures over a magnetic field range of ± 1 T. We use a very small magnetic field sweep rate of 0.005 T/min to exclude adiabatic demagnetisation effects (see also Section 6.4.4) originating from Ni impurities in commercially available chip packages. The conductance change arising from weak localisation is then fitted to the 1D Altshuler model according to Eq. 6.14.

The fitting procedure is divided into a two step procedure. In the first fitting round, both the prefactorial α and the electron phase coherence length l_φ are allowed to vary. This allows to determine if our assumptions about a valley degeneracy of $g_v = 1$ is correct. Indeed, we observe that the best fitting results for all temperatures were obtained with the prefactorial fit parameter α oscillating around unity and $g_v = 1$. Therefore we have fixed α to unity for the second fitting round to make the fits comparable at differ-

ent temperatures. Fig. 6.16 shows the raw magnetoconductance data for six different measurement temperatures (black traces). The magnetoconductance observed at B = 0 increases with increasing magnetic field leading to the observation of negative magnetoresistance – the characteristic signature of weak localisation. The effect of weak localisation arises from coherent backscattering of forward and time-reversed electron waves around a loop as electrons diffuse through the sample. The application of a perpendicular magnetic field breaks the time reversal symmetry in these loops, suppressing the coherent backscattering, and resulting in an increase of the magnetoconductance. For 1D weak localisation, the maximum size of the loops is given by the product of the wire width w and the electron phase coherence length l_φ, i.e. $w \cdot l_\varphi$. Since l_φ increases with decreasing temperature, more and larger loops can be formed which results in more a more pronounced drop in the zero-field magnetoconductance as the temperature is lowered from 4 K to 300 mK. Both the negative magnetoconductance and more pronounced drops for zero-field magnetoconductance are seen in Fig. 6.16 in accordance with our understanding. The fitted 1D weak localisation results over the fitting range of $\pm$0.5 T are overlayed as red curves. From Fig. 6.16, it can be readily seen that the 1D weak localisation theory fits the data well over the entire temperature range. This indicates that the magnetoconductance is in the 1D regime over the magnetic field range of $\pm$0.5 T and for temperatures up to $\sim$4 K.

In Fig. 6.17, we present the temperature-dependent values of l_φ for six data points on a log-log scale. We see that l_φ increases as the temperature is lowered. However, there appears to be an apparent saturation of l_φ below 450 mK. The temperature dependence of the electron phase coherence length depends on the dominant dephasing mechanism in our samples. There are three potential dephasing mechanisms:

- ***Nyquist phase-breaking:*** *At low temperatures Nyquist dephasing [79] is believed to be the dominant dephasing mechanism in disordered quasi one-dimensional systems. Nyquist noise arises from scattering of conduction electrons with a fluctuating electromagnetic field produced by the other electrons in the conductor. Altshuler et al. [79] showed that the inelastic scattering time τ_φ of this dephasing mechanism in 1D has a temperature dependence of $\propto T^{-2/3}$.*
  The corresponding coherence length is expressed as:

$$l_\varphi^N = \left(\frac{D G_0 \hbar^2 L}{\sqrt{2} e^2 k T} \right)^{\frac{1}{3}} \tag{6.15}$$

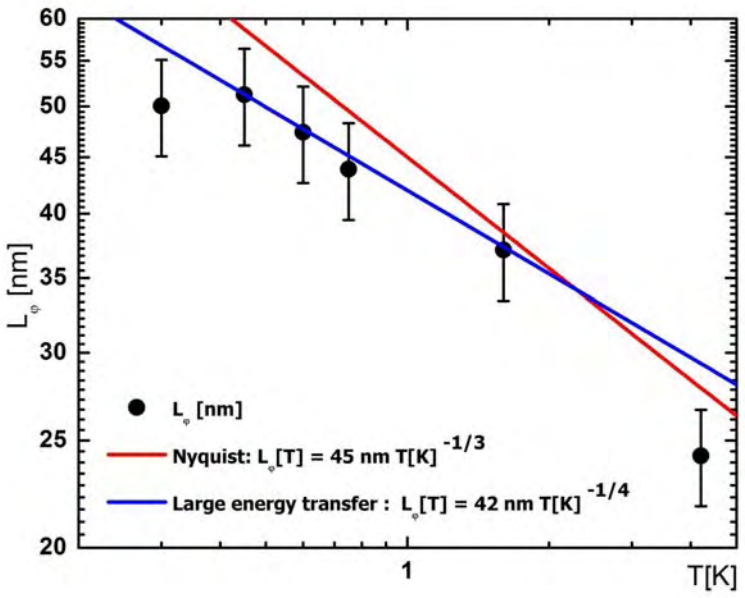

Figure 6.17: Temperature dependence of 6 different l_φ(T) values obtained from 1D weak localisation fitting. The red line represents the predicted temperature dependence for Nyquist dephasing according to Altshuler *et al.* [79], whereas the blue line is the predicted temperature dependence for large energy transfers dephasing as proposed by Abrahams *et al.* [81].

where D is the diffusion constant, G_0 is the Drude conductance and L is the wire length.

- ***Electron-electron scattering with large energy transfers:*** *Another dephasing mechanism was proposed [80] to become relevant where inelastic electron-electron scattering with large energy transfers, due to screened Coulomb interactions, is dominant. The underlying theory was described by Fukuyama and Abrahams [80]. In a thin wire, Abrahams et al. reported [81], the temperature dependence of the inelastic scattering time becomes $\tau_\varphi \propto T^{-\frac{1}{2}}$ and the resulting expression for the electron phase coherence length is given by:*

$$l_\varphi^{LET} = \left(\frac{\pi \hbar G_0 L}{\sqrt{2} a e^2} \sqrt{\frac{\hbar D}{kT}} \right)^{\frac{1}{2}} = C^{LET} \cdot T^{-\frac{1}{4}} \tag{6.16}$$

where D is the diffusion constant, G_0 is the Drude conductance and L is the wire length. The parameter a is predicted to be of order unity at T = 0 K.

- ***Two-level tunnelling modes:*** *Thouless [82] reported a temperature dependence of $T^{-\frac{1}{2}}$ for the electron phase coherence length in quasi one-dimensional disordered metal samples based on two-level tunnelling modes. According to Black* et al. *[83] this temperature dependence should be dominant at low temperatures in a disordered quasi 1D sample.*

The predicted $T^{-\frac{1}{2}}$ temperature dependence predicted for a dephasing mechanism arising from two-level tunnelling modes can be disregarded since it is not consistent with our experimental observation. Therefore, we concentrate our analysis on the Nyquist dephasing and dephasing due to electron-electron scattering with large energy transfers.

Estimating $D = 5 \cdot 10^{-4}\ m^2 s^{-1}$ from 2D weak localisation fitting of wires fabricated in this thesis, approximating the Drude conductance, G_0 from the high temperature resistance R_0 = 39 kΩ at T = 65 K and L = 320 nm, we obtain a numerical expression for the 1D Nyquist dephasing behaviour in this wire, namely

$$l_\varphi^N(T) = 45\ nm \cdot T^{-\frac{1}{3}} \tag{6.17}$$

Fig. 6.17 shows this theoretically predicted Nyquist behaviour (red curve) with the fitted phase coherence values obtained at 6 different temperatures. The predicted Nyquist mechanism is slightly over-estimating the phase coherence behaviour but it is evident, that the prediction is generally in good agreement with our measurement

T[mK]	$l_\varphi[nm]$	$l_T[nm]$	$\left(\frac{l_\varphi}{l_T}\right)^2$
4200	24	30	0.64
1600	37	49	0.57
750	44	71	0.38
600	47	80	0.35
450	51	92	0.31
300	50	113	0.20

Table 6.4: Temperature-dependent values of the fitted electron phase coherence length l_φ, the thermal length l_T for the 27 nm wire and the ratio $\left(\frac{l_\varphi}{l_T}\right)^2$.

results except for an apparent saturation of the electron coherence length obtained below 450 mK. Nyquist dephasing has been observed by several groups in various other systems such as δ-doped GaAs wires [196], Ag metal wires [197], Al and Au metal wires [198], AuPd metal wires [199], [200] and boron-doped semiconducting multi-walled carbon nanotubes [201]. Moreover, we have observed 2D Nyquist dephasing behaviour in P-doped δ layers fabricated in our group [166].

Now we consider dephasing arising from electron-electron collisions with large energy transfers [81]. This dephasing mechanism was observed for example by Graaf *et al.* [202] in 1D silicon MOSFETs, where they experimentally found a value of a of 10 in Eq. 6.16. The uncertainty of a with temperature (a is expected to be unity at T = 0) allows us to adjust the predicted magnitude C^{SET} to match our data. Using Eq. 6.16 and a = 2.7, we get

$$l_\varphi^{LET}(T) = 42\ nm \cdot T^{-\frac{1}{4}} \tag{6.18}$$

The blue line in Fig. 6.17 represents the functional dependence of the electron phase coherence length resulting from this large energy transfer mechanism. We can see excellent agreement with the data in the range from 1.5 K down to 450 mK. The data point at T = 300 mK again lies outside the predicted dependence.[3] However, at 4 K, the Nyquist temperature shows better agreement. Nyquist behaviour is expected to dominate in the regime [195], where $\left(\frac{l_\varphi}{l_T}\right)^2 \gg 1$, where $l_T = \sqrt{\frac{\hbar D}{kT}}$ is the thermal length. Table 6.4 shows the extracted values of the electron phase coherence length, the thermal length and the ratio $\left(\frac{l_\varphi}{l_T}\right)^2$. We can see that at 4 K, $\left(\frac{l_\varphi}{l_T}\right)^2$ is 0.64 decreasing to 0.20 at 300 mK. Therefore it is possible that we initially observe some Nyquist dephasing which is then dominated by large energy transfer dephasing at lower temperatures.

[3] We shall discuss this apparent saturation in detail in Section 6.4.11.

A combination of the two dephasing mechanisms has also been observed in Si MOSFETs by Pooke *et al.* [195] and in GaAs/Al_xGa_{1-x} 1D wires by Choi *et al.* [203]. We also perform a power law fit on the l_φ[T] behaviour emerging from 1D weak localisation theory and obtain a power law of the form $l_\varphi(T) = 40nm \cdot T^{0.31}$. The exponent of n = 0.31 is slightly closer to n = $\frac{1}{3}$ ascribed to Nyquist behaviour than n = $\frac{1}{4}$ characteristic for larger energy transfer scattering but this tendency is not significant enough to allow a clear decision on the dominant dephasing mechanism.

We conclude that both, Nyquist and large energy transfer dephasing describe the data well, whereas the predicted $T^{-\frac{1}{2}}$ temperature dependence based on two-level tunnelling modes did not fit the data and can therefore be ruled out. Whilst it is likely that both mechanisms are present with a dominating effect due to larger energy transfer scattering at lower temperatures, it is very difficult to discern the two dephasing mechanisms using the temperature dependence of l_φ in our limited temperature range. Now that we have analysed the conductance correction due to weak localisation, we turn our attention to the conductance corrections arising from both, weak localisation and electron-electron interaction arising from Coulomb interaction of the conduction electrons.

6.4.10 Conductance corrections due to electron-electron interactions

In the previous section, we extracted the temperature dependence of the electron phase coherence length between 450 mK and 4 K from 1D weak localisation theory. Now we want to see how we can explain the total conductance correction that we observe in our wire. The zero-field conduction correction due to weak localisation in 1D is given by:

$$\delta G_{WL}(B = 0) = -g_s g_v \frac{e^2}{hL} \cdot l_\varphi \tag{6.19}$$

We immediately see that $\delta G_{WL}(B = 0)$ is directly proportional to l_φ. Fig. 6.18 depicts the conduction correction $\Delta G = G(T) - G_0$ in the low temperature regime from 200 mK to 5 K. G_0 is again taken from the high temperature resistance R_0 = 39 kΩ at T = 65 K approximating the Drude value. The blue data points in Fig. 6.18 are the calculated conductance correction values using the fitted l_φ values, where we use g_s = 2, g_v = 1 as confirmed from 1D weak localisation fitting. Whereas we are able to reproduce the general trend of ΔG, we find that the predicted conductance correction given by $\delta G_{WL}(B = 0)$ underestimates the magnitude of ΔG. This observation indicates that

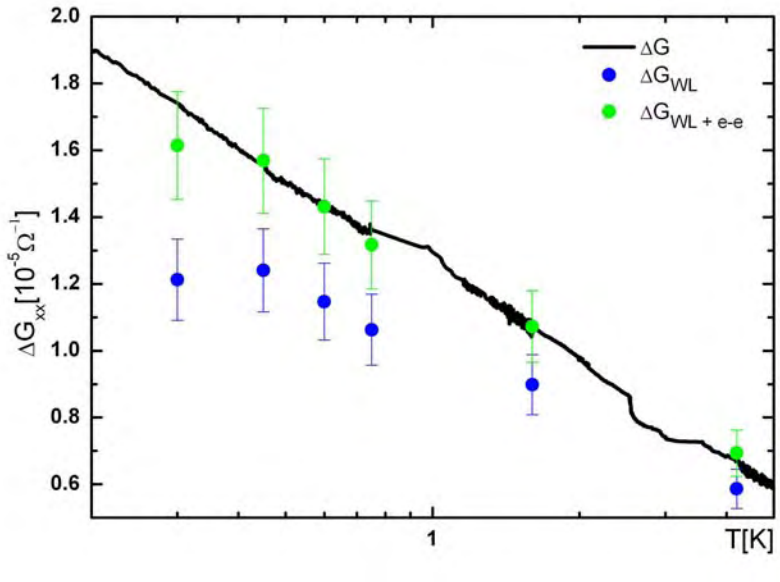

Figure 6.18: The temperature dependence of the conduction correction ΔG. ΔG_{WL} (blue points) from 1D weak localisation taken at 6 different temperatures, whereas ΔG_{WL+ee} (green points) is composed of the contribution from 1D weak localisation and a component originating from 1D electron-electron interaction. The black traces is the measured conductance correction.

another correction to the conductance must be occurring. Electron-electron interaction effects originating from Coulomb interaction between conduction electrons are also known to result in a conductance correction in a disordered wire system [204]. The dimensionality of the electron-electron interaction effects is given by the magnitude of the thermal length compared to the wire width w [70], defined as

$$l_T = \sqrt{D \cdot \tau_T} = \sqrt{\frac{\hbar D}{kT}} \tag{6.20}$$

where τ_T^{-1} reflects the characteristic time 6.20 in which the wave function of two conduction electrons (in different energy eigenstates separated by kT) interfere before they loose their phase correlation.

Table 6.4 shows the temperature-dependence of the thermal length calculated from Eq. 6.20 from which we can determine that we are in the 1D regime of electron-electron interaction i.e. $l_T > w$. For completeness, the fitted electron phase coherence values are also shown. From Table 6.4, we can see that a crossover from 1D to 2D occurs

at T $>$ 4 K, where l_T = 30 nm is comparable to the wire width w = 27 nm. If we want to take electron-electron interaction into account to explain the total conductance corrections in our wires below 4 K, we have to use 1D electron-electron interaction theory.

An analytical expression for the 1D electron-electron interaction correction to the conductivity was provided by Altshuler *et al.* [204] (also found in [70], [94]) and is given by:

$$\delta G_{ee}(T) = -g_{1D}\frac{e^2}{\sqrt{2}\pi\hbar L}\cdot l_T = -g_{1D}\frac{e^2}{L}\sqrt{\frac{D}{\pi hk}}\cdot T^{-\frac{1}{2}} \tag{6.21}$$

where g_{1D} is an interaction parameter of order unity. Altshuler provided a derivation for g_{1D} in 1D [205], [206], which is

$$g_{1D} = \frac{4.91}{\pi}\left(1 - 12\cdot\frac{1+\frac{1}{4}F-(1+\frac{F}{2})^{\frac{1}{2}}}{F}\right) := \frac{4.91}{\pi}\cdot\alpha_{ee} \tag{6.22}$$

where F reflects the Coulomb interaction between conduction electrons. F becomes unity for short-range interaction and vanishes for long screening lengths [93]. α_{ee} plays the role of a screening factor typically between zero and unity.

We can extract the contribution due to 1D electron-electron interaction by combining the conductance correction due to 1D weak localisation (Eq. 6.19) and 1D electron-electron interaction (Eq. 6.21):

$$\Delta G_{WL+ee} = \delta G_{WL} + \delta G_{ee} \tag{6.23}$$

With Eq. 6.23, we are able to fit the total conductance correction using α_{ee} as a fit parameter to extract the electron-electron interaction contribution. The result of this interpolation is also shown in Fig. 6.18. The green data points, representing the combined contribution ΔG_{WL+ee}, describe the continuously measured conductance (black trace) very well over the entire temperature regime except for a deviation at the lowest temperature of T = 300 mK due to the low electron phase coherence values extracted from 1D weak localisation fitting. The screening factor was determined to be α_{ee} = 0.13. Our results are in good agreement with a recent analysis on etched 1D Si δ-doped GaAs wire arrays with widths of $\sim$50 nm reported by Khavin *et al.* [196]. Their system is also a planar δ-doped system, where conduction also takes place in the dopant plane. Therefore we expect a high degree of comparability with our P-doped wires. A combination of weak localisation and electron-electron interaction was also observed to fit the conductance behaviour with a comparable screening factor of α_{ee}

= 0.37. Our results show that the observed conductance correction can be completely explained by a combination of 1D weak localisation effects accompanied by a weaker influence arising from 1D electron-electron interaction effects.

6.4.11 Potential crossover to strong localisation below 450 mK

As a last step in our analysis, we take a look at the apparent saturation of the phase coherence length at T = 300 mK. Note that whereas the electron phase coherence length, l_φ is observed to saturate at this point, the measured resistance does not saturate down to the lowest available temperature of 200 mK as can be seen from Fig. 6.14. We should add that whilst we have only one data point at 300 mK and it is not wise to overinterpret the data, there exists a controversial discussion in the literature that speculates about the possible limitations to obtain reliable magnetotransport data at low temperatures of a few hundred millikelvin. Quite a few groups observe a saturation of l_φ at low temperatures [207], [196], [208], [195]. Lin and Bird [78] have recently written an exhaustive review on this topic and we will briefly discuss the possible causes for this phenomenon which remains the subject of ongoing research:

- Joule heating
- Electromagnetic noise
- Magnetic impurities
- Crossover from weak to strong localisation

Joule heating:

Joule heating arises from the diffusive motion of the conduction electrons which can cause sample heating. High measurement currents can therefore lead to an apparent saturation if the associated sample temperature due to heating deviates from the bath temperature of the dilution refrigerator. Several other groups [199], [207], [209] have observed weaker or saturated electron phase coherence values while ruling out sample heating. By measuring the effect of the sample current on the device resistance in Section 6.4.3, we have determined that a measurement current of 200 pA was found to be in the regime where the resistance is independent of the device current i.e. no heating occurs. Indeed the measured four terminal device resistance does not saturate

down to the lowest measurement value of T = 200 mK. Therefore, we believe that Joule heating is not responsible for any apparent saturation of l_φ.

Electromagnetic noise:

Altshuler *et al.* [77] suggested that non-equilibrium high-frequency noise is responsible for the observed saturation of l_φ at low temperatures. However several groups [210], [211] found that this dephasing mechanism is independent of external electromagnetic noise indicating that, at least in their samples, the electromagnetic noise is not the governing dephasing mechanism at low temperatures. We employed the use of cold filters (Section 6.4.2) to avoid the influence of extrinsic electromagnetic noise. According to Altshuler, electromagnetic noise becomes important if

$$\hbar w \cdot \tau_\varphi \sim \hbar \tag{6.24}$$

For typical dephasing times τ_φ = 1 ps measured in our samples, the corresponding frequencies at which electromagnetic noise can cause saturation are $\sim$1 THz. It is not very likely that a THz source is close to our measurement environment. Additionally, the low-pass filter setup of our measurement is designed to suppress frequencies larger than a few MHz. From these arguments, we conclude that electromagnetic noise is not a likely cause for saturation in our samples.

Magnetic impurities:

Spin scattering of the conduction electrons with magnetic impurities can cause decoherence leading to a saturation of l_φ in a sample [78]. Pierre *et al.* [197] examined the effect of dilute magnetic impurities in Au, Ag and Cu wires and found that even any extremely small concentration of below one part per million (ppm) of magnetic impurities (which could mean just a few atoms per sample) leads to saturation at low temperatures. Their samples were made using standard e-beam lithography techniques. The metal was deposited by evaporators used only for nonmagnetic metals through an e-beam defined mask. For the fabrication of the wire metal sources of different purities 99.999% (5N) and 99.9999% (6N) have been used. Pierre *et al.* conducted MR-measurements and found that all Cu samples and Ag samples made by lower purity sources showed a saturation of τ_ϕ below $\simeq$ 400 mK while purer Ag and all (lower and higher purity) Au samples showed the expected 1D Nyquist temperature dependence down to 40 mK.

Ca	Cu	Mg	Mn	Si	Fe
1 ppm	1 ppm	2 ppm	2 ppm	1 ppm	2 ppm

Table 6.5: Trace elements in our 5N (99.999 %) Al electron beam evaporation source in parts per million (ppm).

The only possible source of magnetic impurities in our samples could stem from the Al electron beam evaporation process during contact metallisation. E-beam evaporation is generally considered the cleanest form of evaporation as the evaporation takes place from the middle the melted aluminium inside the crucible. As the crucible is water cooled, the Al in contact with the crucible walls should be much cooler than that in the centre which is evaporate. Therefore contamination from the (copper) crucible walls should not occur. Table 6.5 summarises the results of a trace element analysis performed on our 5N i.e. 99.999 % purity level Al source. It shows that the material is very pure containing only minute magnetic impurities of 2 parts per million in the form of manganese and iron atoms. It is important to note that the device area has previously been encapsulated with epitaxial silicon under ultra-high vacuum conditions. In addition, the Al contacts are only in contact with the P-doped contacts separating the actual wire from the Al contacts by about $\sim$2 μm. As such it is unlikely, that magnetic impurities are present in the vicinity of the P-doped wire. Therefore, we conclude that the presence of magnetic impurities is not a likely problem in our samples.

Having ruled out the *extrinsic* dephasing mechanism due to Joule heating, electromagnetic noise and magnetic impurities, we now consider an *intrinsic* cause for the observed saturation of l_φ, namely a crossover form weak to strong localisation.

Crossover from weak to strong localisation:

In 1958, Anderson [91] put forward the ingenious thought, that a quantum particle may become localised by a random potential. According to scaling theory, the dramatic consequence, even for non-interacting 1D or 2D systems, is that the smallest amount of disorder will result in a complete localisation of all states [92]. The ramification of this theory holds a vanishing conductivity $\sigma(T)$ at finite temperatures in both 1D and 2D. Non-zero conductivity can still be observed above the transition to strong localisation due to the presence of inelastic processes such as electron-phonon interaction or electron-electron interaction. At sufficiently high temperatures, inelas-

tic dephasing processes continuously drive a strongly localised system into the well-known weak localisation regime. This opens up the possibility of a crossover from weak localisation to strong localisation in our samples at low temperatures.

Mott [95] provided an analytical expression for the intermediate conduction regime, where particles are not completely localised but tunnel from one localised state to another instead. This transport mechanism is known as variable range hopping (VRH).

$$\sigma_{VRH} = \sigma_0 \cdot e^{-(\frac{T_0}{T})^{\mu}} \tag{6.25}$$

or

$$R_{VRH} = R_0 \cdot e^{(\frac{T_0}{T})^{\mu}} \tag{6.26}$$

with $\mu = \frac{1}{1+d}$ where d is the system dimensionality. T_0 reflects the strong localisation crossover temperature and R_0 is related to σ_0, the classical Drude value. Initially this formula was derived to explain the intermediate conduction regime due to electron-phonon scattering. Later on the model was also applied to inelastic processes involving electron-electron interaction [212]. Even until today, the range of systems and dephasing mechanisms which can be described by Mott's formula is still under investigation [213]. Fowler *et al.* [97] used Mott's formula to describe conduction in a silicon MOSFETs. By varying the channel width via the use of gate, they observed a crossover from 2D to 1D VRH by continuously reducing the channel width.

Thouless [82] and coworkers followed on from Anderson's work on localisation and started to formulate a scaling description of the localisation problem. The emerging scaling theory was soon combined with perturbation theory in the seminal work of Abrahams , Anderson, Licciardello and Ramakrishnan [92] during their time at Bell labs. Thouless [82] proposed that a wire can be considered as a series of smaller subsystems of wires of length ξ if electrons are sufficiently localised. Conduction between the different subsystems is a thermally activated process. It is this Arrhenius type of thermally activated transport that is captured in the VRH model.

The crossover from strong to weak localisation occurs when the localisation length, ξ, becomes comparable to the electron phase coherence length l_φ, i.e. $\xi \sim l_\varphi$. The localisation length ξ is traditionally defined as the envelope of the electron wavefunction in real space:

$$|\Psi(\overrightarrow{r})| \propto e^{\frac{\overrightarrow{r} - \overrightarrow{r_0}}{\xi}} \tag{6.27}$$

where $\Psi(\overrightarrow{r})$ is the electron wavefunction. A convenient expression [214], [215] to

estimate the length of a subsystem wire is related to ξ as

$$\xi = \frac{h}{2e^2} \cdot \frac{L}{R_0} \tag{6.28}$$

where $\frac{h}{e^2}$ is known as the resistance quantum also known as the von-Klitzing constant $R_k = \frac{h}{e^2} = 25.8\,\text{k}\Omega$, L is the wire length and R_0 is again obtained from the highest available temperature at T = 65 K. For the 27 nm wide wire with $L = 320$ nm and $R_0 = 39\,\text{k}\Omega$, we obtain a localisation length of $\xi \approx 100$ nm. The value of l_φ at lower temperature is of order 50 nm (see Table 6.4) which is only half the value of ξ. However Khavin *et al.* [196] pointed out that the relation $\xi \sim l_\varphi$ leading to a transition from weak to strong localisation has merely order of magnitude character and found a crossover from weak to strong localisation in Si δ-doped GaAs wires already for l_φ 2 – 3 times smaller than ξ. As such, it is feasible to assume that the 27 nm wire approaches the strongly localised regime at temperatures of T $\sim$ 300 mK and below. Gershenson *et al.* [196], [214] have shown that in their Si δ-doped GaAs wires, the electron phase coherence length extracted from weak localisation theory follows 1D Nyquist behaviour until it saturates at a temperature of $\sim$1 K. It is shown that the saturation of l_φ coincides with a crossover from weak to strong localisation. We have tested this hypothesis of a potential crossover to strong localisation by fitting our data to VRH models of different dimensionality given by Eq. 6.26. The green curve in Fig. 6.19 shows the results for a generic VRH-type equation R_{VRH} (d = 0), the correct VRH equation R_{2D} for two dimensions with $\mu = \frac{1}{3}$ (blue curve) and the respective equation for 1D, R_{1D}, with $\mu = \frac{1}{2}$ (red curve). The R_{1D} fit (red curve) represents the measured resistance very well over the entire temperature range – much better than the other two models. The fitted value of R_0 = 43 kΩ corresponds nicely to the measured high temperature value of R_0 = 39 kΩ. The transition temperature from weak localisation to strong localisation of T_0 = 312 mK is very close to the last measurement point of T = 300 mK, where we observe an electron phase coherence value below the predicted Nyquist behaviour. It should be noted that both other fits seem inconsistent either due to a high R_0 value (R_{VRH}) or a high T_0 (R_{2D}). However to completely confirm a crossover to strong localisation, a wider temperature range below 300 mK is needed. Alternatively narrower wires with a higher resistance R_0 leading to lower localisation length ξ are suitable for an investigation into strong localisation. We will present the I-V characteristics of one such wire with a width of 8 nm in Section 6.5.

In the previous section, we have seen that the conductance correction in the tem-

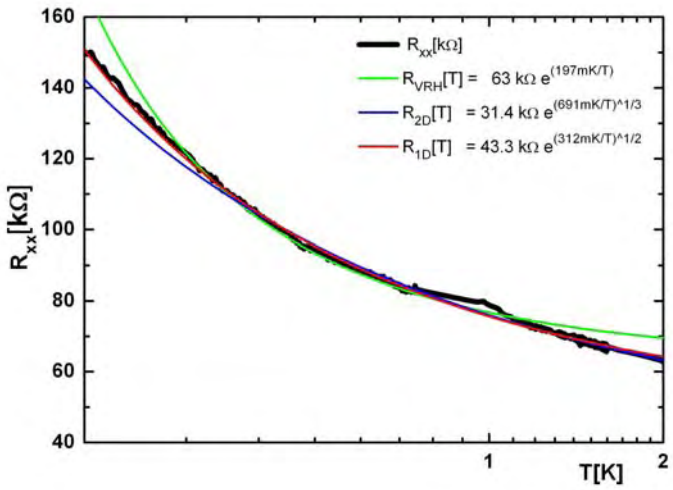

Figure 6.19: Strong localisation crossover at low temperatures. R_{27}(T) is well fitted to the 1D variable range hopping (VRH) model R_{1D}, whereas the general type VRH model R_{VRH} and the 2D VRH model R_{2D} produce inconsistent fit results. The extracted value of T_0 = 312 mK indicates that the lower electron phase coherence observed at T = 300 mK stems from a beginning crossover from weak to strong localisation.

perature range from 450 mK to 4 K is well described by 1D weak localisation and electron-electron interaction. The results shown in Fig. 6.19 suggest a crossover from weak to strong localisation at T $<$ 300 mK. We note that for the same data set, the observed resistance from 200 mK to 2 K is also well described by a 1D VRH fitting model. The fact that the same data fits both a combination of 1D weak localisation and 1D electron-electron interaction, as well as a strong localisation model should not be surprising since the transition to strong localisation is not sharp. Only at temperatures between 200 mK and 450 mK, the data is better described by the VRH model. Moreover the fitted transition temperature of T_0 = 312 mK suggests that the 27 nm wire enters the strong localisation regime for the lowest accessible measurement temperatures. This is a feasible explanation as to why the electron phase coherence length at T = 300 mK lies below the expected values as seen in the studies of Gershenson *et al.* [196], [214].

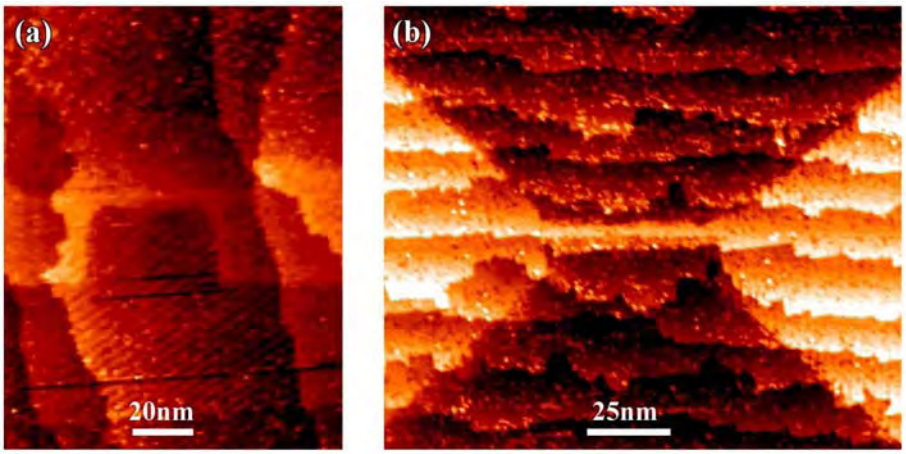

Figure 6.20: STM lithography for wires with widths approaching the atomic scale: (a) 8 nm×57 nm and (b) 3.5 nm×50 nm. Imaging conditions: V ∼ -2 V, I ∼ 0.2 nA.

6.5 Outlook: towards atomic-scale wires

In the following section, the most recent results on the fabrication of sub 10 nm wires is reported. The aim of this ongoing study is to determine what mechanisms ultimately limit the conduction of dopant silicon wires at the atomic level. Fig. 6.20 shows two lithographic patterns of sub 10 nm wires using STM lithography. The first wire pattern [Fig. 6.20 (a)] is an 8 nm wide wire bridging a 57 nm wide gap formed by two source-drain leads of 45 nm in width. The two 45 nm wide source-drain leads are connected to 3 μm×3 μm large lithographic side patches which serve as contact areas for the four Al contacts subsequently fabricated in the optical lithography process aligned to previously fabricated registration markers. An initial electrical characterisation of this wire is presented in the following section.

In addition, we have optimised the STM patterning to allow for an improved device geometry. Fig. 6.20 (b) shows an STM image representing the improved design for connecting narrow wire widths. Since the resistance significantly increases with narrower wires, we have decreased the wire length from ∼300 nm for the wires discussed previously to ∼50 nm for sub 10 nm wires. This reduction in length was chosen to obtain wire resistances which are still suitable for measurements at low temperatures. The idea behind the triangular contact design is to rule out potential conduction not arising through the narrow wire itself but through tunnelling through the P-doped

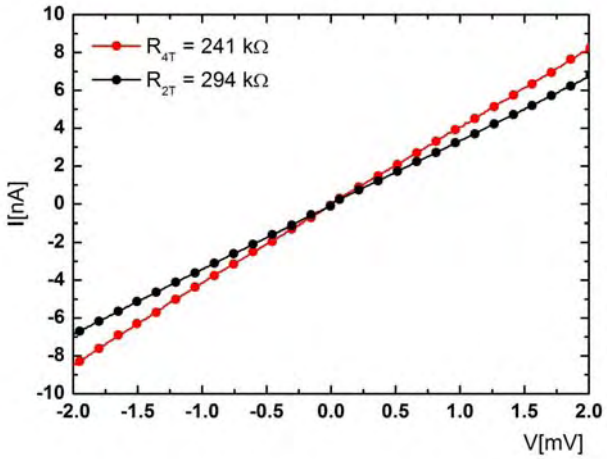

Figure 6.21: I-V characteristics of the 8 nm × 57 nm wire. The device exhibits a four terminal resistance of R_{4T} = 241 kΩ, a two terminal resistance of R_{2T} = 294 kΩ and a resistivity of $20 \cdot 10^{-6}$ Ωcm.

leads[4] for lead separations ∼50 nm. Indeed, we will show in Chapter 7 that clearly non-ohmic behaviour is observed for triangular source-drain contacts separated by ∼50 nm. Fig. 6.20 (b) depicts a 3.5 nm wide wire perfectly aligned to the Si dimer rows on a single terrace, which we believe will allow the measurement of optimal conduction properties unhindered by the conduction path crossing dimer rows or silicon terraces. However the measurement of such devices and the influence of wire direction on the Si(100) surface and terrace structure on the electrical properties is beyond the scope of this thesis. Therefore we only present preliminary electrical results from the 8 nm wide wire in the following section.

6.5.1 I-V characteristics of an 8 nm wide Si:P wire

The I-V characteristics of the 8 nm × 57 nm wire pattern shown in Fig. 6.20 (a) at 4 K were determined using a Keithley 2410 DC voltage source unit. The voltage is slowly varied up to ±2 mV in steps of 10 μV. The resulting I-V traces exhibit perfectly ohmic behaviour showing that the wire is indeed conducting without the presence of small tunnelling gaps along the wire. Fig. 6.21 shows the four terminal and the two terminal

[4]The device shown in Fig. 6.20 (a) has a side patch separation of 300 nm sufficient to exclude significant influence on the measured conduction properties.

I-V traces. From the slope of the respective I-V curve, we can extract the four terminal and the two terminal resistance respectively. The four terminal resistance turns out to be R_{4T} = 241 kΩ, whereas R_{2T} equates to 294 kΩ. Subtracting R_{4T} from R_{2T} we obtain a contact resistance of R_C = 53 kΩ.

Assuming a layer thickness of 0.6 nm determined from STM studies by L. Oberbeck [181], we obtain a resistivity of $20 \cdot 10^{-6}$ Ωcm which is one order of magnitude higher than those obtained for the 27 nm, 50 nm and 90 nm wires presented in Table 6.1. A potential challenge for measuring this device at low temperatures is to ensure that sample heating is not affecting the resistance. For the 27 nm wire, we use currents of ∼200 pA to exclude sample heating. For this 8 nm wide wire, we would have to apply a current of 60 pA to obtain the same current density.

It is interesting to note, that for a 1D wire, the electron phase coherence is expected to decrease with decreasing wire width as:

$$l_\varphi \propto \left(\frac{w}{T}\right)^{\frac{1}{3}} \tag{6.29}$$

According to Eq. 6.29, the electron phase coherence length for the 8 nm wide wire would be ∼16 nm at 4 K. Therefore this wire is expected to be clearly in the 1D weak localisation regime at T = 4 K. With this wire, it might also be possible to better access the crossover region to strong localisation at low temperature, where it is anticipated that strong localisation limits conduction at the atomic level. Future magnetoconductance measurements in a dilution refrigerator will provide new insights into the 1D conduction properties of these narrow wires.

6.6 Chapter summary

This chapter presented:

- A summary of key properties of P-doped Si nanowires fabricated by different methods
- An STM study of the structural integrity of wires during the fabrication process developed in this thesis
- A detailed, temperature-dependent magnetotransport characterisation of a 27 nm wide Si:P nanowire to determine the main scattering mechanisms affecting conduction

- An outlook of the most recent sub 10 nm wide Si:P wires

We compared key properties like electron mobility, electron phase coherence length, size and resistivity of P-doped Si nanowires fabricated by different methods such as EBL and etching, template growth, catalytic growth and STM-patterning. We found that whereas resistivity values are quoted from room temperature down to liquid helium temperatures, highly P-doped, planar STM-patterned nanowires [29], [31], measured at 4 K and below, currently exhibit the lowest resistivities compared to nanowires fabricated with other techniques. The low resistivity makes STM-patterned nanowires useful for the study of the ultimate limit of conduction in dopant wires.

We went on to investigate the structural integrity of nanowires for widths ranging from 50 nm down to 7 nm during the STM-based fabrication process developed in this thesis. We found that wires of 27 nm in width still appear intact after device encapsulation using CITS, whereas for wires of 7 nm it becomes increasingly difficult to distinguish the electrical signal from the buried dopants from the topographic signal due to insufficient contrast from our CITS measurement. Further experiments are aimed at a more detailed investigation of the resolution limits of the CITS technique.

Particular focus was given to an in-depth analysis of a 27 nm wide wire over a large temperature range from 200 mK to 65 K. Above 65 K, the silicon substrate becomes conducting (needed for STM imaging at room temperature). Three different temperature regimes were identified to explain the conductance behaviour of the wire. From 4 K to 65 K, electron-phonon dephasing was found to be the dominant 2D dephasing mechanism dictating the conductance behaviour at higher temperatures. Below 4 K, the wire enters the 1D magnetotransport regime, where electron dephasing was found to be well described by both inelastic scattering processes with small energy transfer known as Nyquist dephasing and electron-electron collision with large energy transfer. Whilst the limited temperature range makes it very difficult to discern the two dephasing mechanisms, it was found that the dephasing mechanism due to electron scattering with larger energy transfers describes the data better in the temperature range between 450 mK and 1.5 K, whereas Nyquist dephasing describes the temperature dependence better between 1.5 K and 4 K. Subsequently, the total conduction correction measured in this wire could be well described by a conductance correction due to both, 1D weak localisation and 1D electron-electron interaction effects. At temperatures below 450 mK, the extracted phase coherence length was observed to saturate. We have identified that a crossover from weak to strong localisation is likely

to be responsible for the apparent saturation of l_φ. We showed that the conductance of the wire between 200 mK and 2 K is also well described by a 1D VRH model which predicts a crossover temperature to strong localisation at $\sim$300 mK. It is interesting to note that the conductance behaviour between 2 K and 450 mK is well described by both, a combination of weak localisation and electron-electron interaction but also by a VRH model describing the crossover to strong localisation. This finding suggests that both descriptions can describe the conductance behaviour regime in our wire, which is expected due to the fact that the high density of P dopants in the plane means, we are in an intermediate conduction regime between weak and strong localisation.

We concluded this chapter by discussing the I-V behaviour of the smallest conducting wire which we fabricated to date. This wire with a width of 8 nm obeys ohmic I-V behaviour with a four terminal resistance of 241 kΩ. Future experiments are planned to explore the transition to strong localisation in this wire which is expected to be more pronounced due to its higher resistivity.

An interesting pathway for future research is studying the dependence of the electrical properties on the wire orientation with respect to the Si dimer row direction as well as its dependence on the P doping level away from saturation dosing (with a carrier density of $1.8 \cdot 10^{14}$ cm^{-2}). The variation of the doping density towards the metal-insulator transition (MIT), corresponding to densities of 10^{11} cm^{-2} – 10^{12} cm^{-2}, will probe the conduction limit as a function of dopant density. In this context, the implementation of a reliable gating strategy will be of importance. Potential realisations of such a gate could be a silicon-on-insulator (SOI) blanket wafer with a degenerately doped backgate or a local side or top gate defined by electron beam lithography. Another relevant area for the future use of gating techniques is presented in the next chapter, where the formation and electrical characterisation of planar, STM-patterned Si:P tunnel junctions will be discussed.

Chapter 7

Electrical characterisation of STM-patterned tunnel junctions

The previous chapters was devoted to the characterisation of ultra-dense P-doped nanowires. Using STM lithography and the self-terminating assembly properties of PH_3, we were able to produce highly doped wires exhibiting carrier densities of up to $1.7 \cdot 10^{14}$ cm^{-2} which corresponds to P-P nearest neighbour distances of $\sim$1 nm. We now investigate how to form insulating regions between highly doped source-drain leads. The Bohr radius gives a measure of the lateral extension of the electron wave-function and is given by:

$$a_B = \frac{4\pi\epsilon_s\hbar^2}{m^* e^2} \approx 3nm \tag{7.1}$$

for m^*=0.19·m_0 along the Si(100) axis. As a consequence it should be possible to construct lateral tunnel junctions or nanogaps with a gap size of order several Bohr radii which corresponds to a tunnelling gap of $\sim$10 nm. The height of the tunnelling barrier is determined by the dimensions of the gap, the presence of doped regions nearby, the doping density of the source-drain leads and substrate background doping in the Si barrier. The realisation of buried, planar source-drain leads allows us to investigate the electrical properties of the substrate itself at low temperatures, since the tunnelling barrier is formed by the gap geometry and the potential landscape in the gap given by the substrate.

A variety of techniques [216], [217], [218], [219] to fabricate very small planar nanogaps have been demonstrated. They typically consist of a pair of metal leads on a insulating layer such as SiO_2 or Al_2O_3 [219] on top of a Si wafer. As an example, Liu *et al.* were able to fabricate sub-10 nm gaps between Ti/Au source-drain leads on a SiO_2 substrate using electron beam lithography with an optimised e-beam dose and a careful lift-off technique. Single Co nanoparticles were then deposited in the

nanogaps to measure their I-V characteristics. Au nanogaps [217] of ∼1 nm size were fabricated using EBL in combination with electrochemical etching in a $KAuCN_2$ bath. The gaps were then coated with organic molecules such as oligo(cyclohexylidene)-disulfides and the I-V curves were compared before and after. The gap resistance was observed to drop from a very high resistance (not stated) to 1 MΩ. It is worth noting that whilst the I-V characteristics for nanogaps covered by the molecules was very stable, the stability of the bare nanogap deteriorated over the course of ∼1 h in ambient conditions. A third method was reported by Morpurgo *et al.* [219]. Here Ti/Au metal contacts were prepared with a spacing of order 100 nm on a Al_2O_3 substrate using EBL. Electrodeposition of Au from an electrolyte solution was then used to close the gap while the gap resistance was monitored. Whilst granular electrodes with separation down to ∼1 nm could be fabricated, the shape around the metal contact edges was random and therefore difficult to reproduce.

Tunnel junctions may also be realised using ion implantation techniques [220] that allow the implantation of single phosphorus ions in silicon through pre-patterned apertures. However, with lateral and longitudinal straggles of 8 nm and 11 nm respectively, these devices are neither atomically precise nor planar. A careful characterisation of STM-patterned, planar, P-doped nanogaps is an important step to enable the subsequent, reliable electrical characterisation of transport properties of STM-patterned Si:P dot devices. Such devices are interesting for the observation of single electron charging effects leading to Coulomb blockade [221], [222] and resonant tunnelling behaviour [223], [224]. The precise alignment of a dot region between source-drain leads in the same lithography step is important since this ability will become useful for alignment issues associated for the realisation of other atomic-scale devices in silicon, such as a solid state quantum computer proposed by Kane [33]. In Kane's concept, the nuclear spin of individual P dopants embedded into a silicon matrix have to be addressed and manipulated separately to act as qubits. A key component of this proposal is the ability to measure single charge transfer between two single P dopants in the Si crystal. Metallic dots between source-drain leads or SETs are regarded as the most sensitive electrometers, able to sense a fraction of the electron charge. As a consequence, SETs are an essential tool towards the measurement of single electron charge movement between P dopants [225] embedded in the silicon crystal.

In this chapter, we demonstrate the fabrication of tunnel junctions using STM lithography with gap sizes of ∼17 nm and ∼48 nm respectively. We performed a

detailed investigation of the 48 nm tunnel junction including its robustness to thermal cycling and a reproducibility study of the I-V characteristics. The junction is patterned by the STM onto a $5 \cdot 10^{14}$ – 10^{15} cm^{-3} P-doped substrate; and the sample packaged using conducting epoxy onto Au-coated chip carrier. We investigate the influence of the metal plane of the chip package $\sim$300 μm away from the tunnel junction. We found that applying voltages between +5 V and -9 V to the gate has little effect on the conductance of the tunnelling gap. Higher voltages lead to electron impact ionisation causing avalanche breakdown of the substrate [226]. We did find however that the conductance of the junction could be altered using bias cooling, i.e. where the substrate is cooled with a fixed bias, which demonstrates that significant gating action would be expected if the backgate distance could be reduced to $\sim$1 μm or less.

Illumination of the tunnelling gap with a light emitting diode (LED) of wavelength $\lambda \sim 650$ nm (which emits photon energies between the indirect and direct band gap of silicon) was found to increase tunnelling conductance due to electron-hole pair generation. Finally, we present preliminary data suggesting that single charging events significantly alter the potential landscape around the tunnelling barrier which highlights the potential use of STM-patterned tunnelling junctions as local charge sensors. Further measurements reveal that tunnelling gaps can be maintained down to a gap size down of $\sim$17 nm — the narrowest junction we fabricated to date.

7.1 Tunnel junction with 48 nm gap

7.1.1 STM fabrication and device dimensions

The fabrication steps and the exact device dimensions shown in Fig. 7.1 are briefly summarised below. Starting out with a P-doped (1 – 10 Ωcm, $5 \cdot 10^{14}$ – 10 ^{15}cm^{-3}), hydrogen terminated Si(100):H surface, the UHV SEM is used to centre the STM tip in the device region between the prefabricated registration makers. STM lithography for this device is performed in three steps. Initially, two triangular patterns with 48 nm separation are written into the hydrogen resist in an STM scan frame of 500×500 nm^2 using an STM voltage of 7 V and a current of 3 nA. Fig. 7.1 describes the overall geometry of the tunnel junction – an STM image of the central region being shown in Fig. 7.1 (c). Subsequently, a 680 nm sized square is connected to each triangular pattern as shown in Fig. 7.1 (b), simply by scanning over the entire scan frame of 680×680 nm^2. A 3.5 μm sized contact patch is then connected onto each of the desorbed squares in

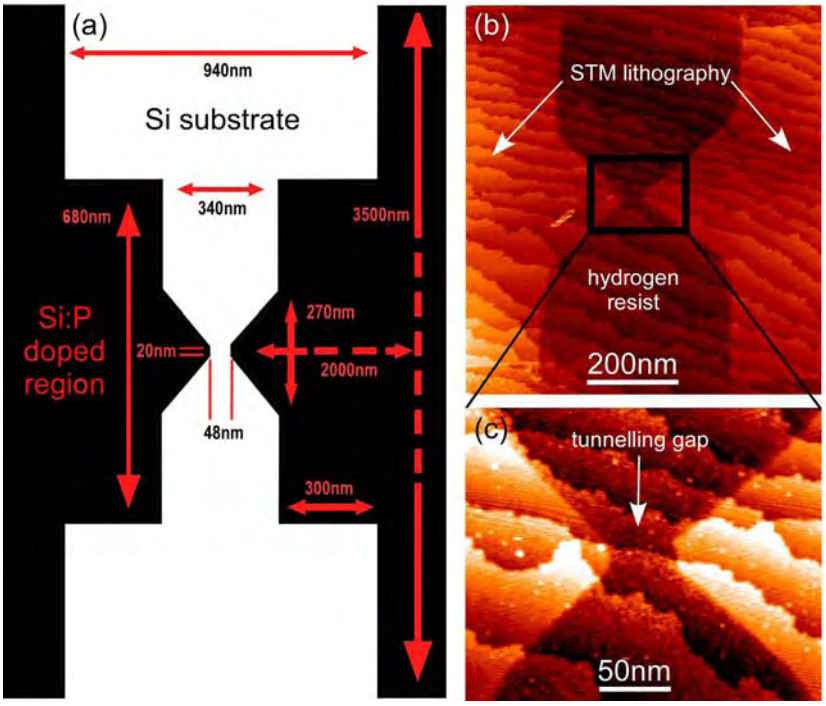

Figure 7.1: Four terminal tunnel junction device. (a) A schematic of the device (not to scale) with exact dimensions, showing the three patterned regions, triangles with a 270 nm wide base, 300×680 nm^2 rectangles and 3.5 μm wide contact pads. (b) STM image of the device and small side contact patches. Note that the large (3.5 μm) contact patches are not shown. (c) STM image of the 48 nm tunnelling gap showing dimer row resolution. Imaging conditions: V$\sim$ -2.2 V, I $\sim$ 0.2 nA.

the same fashion as sketched in Fig. 7.1 (a). A combination of triangular and medium-sized contact pads is chosen to maximise the distance between the large side patches thereby avoiding tunnelling between these regions whilst minimising electron diffraction effects caused by the device geometry. The entire STM lithography step for this particular device takes about 5 h. Subsequently, the lithographic area is exposed to PH_3 for 30 min at a chamber pressure of 1.1×10^{-9} mbar (Note: background chamber pressure is 2×10^{-10} mbar). Following P incorporation at 350 °C, the device is encapsulated with 25 nm of epitaxial silicon grown at a temperature of 250 °C using Si MBE by fellow PhD student, responsible for the MBE system, K. E. J. Goh. Standard optical lithography is then used to align four terminal Al contacts to the large (3.5 μm) P-doped contact patches. Then device is then packaged to a chip carrier and contact between the pins and the device and also the Au-coated backgate is made using gold ball bonding.

7.1.2 Electrical device characteristics

The electrical characterisation of this device was carried out at 4 K. Direct current (DC) I-V data is taken using a Keithley source measurement unit SMU 236. For the differential conductance/resistance measurements, standard lock-in techniques are used at a fixed lock-in frequency of 77 Hz and an excitation voltage of 50 μV. Lock-in measurement techniques are advantageous due to higher sensitivity as compared to DC measurements which are prone to white noise.

Fig. 7.2 shows a typical conductance trace which is obtained by sweeping the DC component of the source-drain voltage from -4 mV to +4 mV while measuring the differential conductance ($\frac{dI}{dV}$) at a fixed AC excitation voltage of 50 μV. It is important to note, that the differential conductance of the device is free from jumps, random telegraph (RTS) signals or resonances such as resonant tunnelling [223], [224]. This shows that the substrate between the two P-doped leads provides a stable potential landscape with the absence of active charge traps and tunnelling resonances through P dopants which might indicate the presence of active P dopants or charge traps in the gap. The I-V characteristic as shown in Fig. 7.2 (red trace) is obtained by simply integrating the conductance data over the given voltage range, i.e.

$$I(V) = \int_{V_{min}}^{V_{max}} \frac{dI}{dV_{sd}} dV_{sd} \tag{7.2}$$

The device conductance increases with increasing source-drain bias as indicating by a

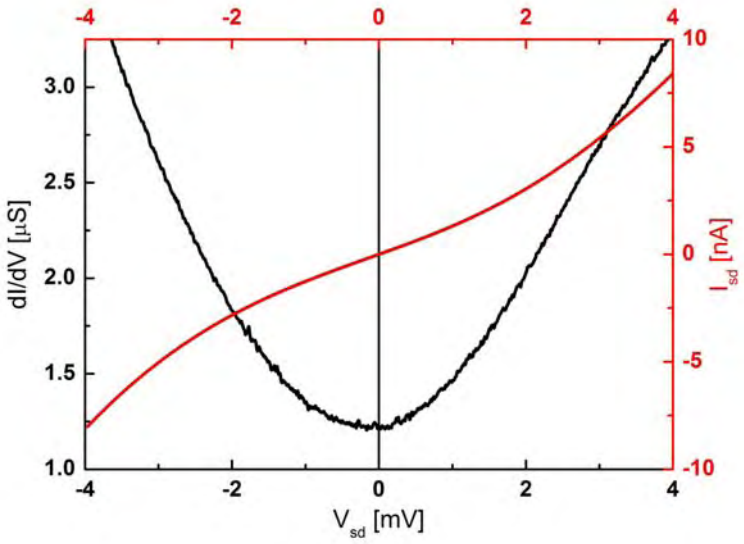

Figure 7.2: Four terminal differential conductance of a 48 nm wide STM-patterned tunnel junction (black) and integrated I-V curve (red) exhibiting non-ohmic behaviour.

monotonously raising I-V curve. The rise in tunnelling current is thereby mainly due to a higher particle energy at higher biases with respect to the tunnelling barrier. However, it is also possible that the tunnelling potential itself is influenced by application of a source-drain bias. This is due to two reasons. Firstly, the density of states (DOS) in semiconductors is energy dependent [34], [227] and the barrier is more transparent for higher particle energies due a lower barrier height. Secondly, the variation of the source-drain bias might result in self-gating [226] of the barrier thereby lowering the tunnel barrier with increasing bias. The resulting *four terminal* I-V curve is compared with a *two terminal* I-V trace obtained using the DC setup and shows good qualitative agreement as is evidenced in Fig. 7.3. This shows that contact resistances do not play a governing role in the device characteristics, which will be further discussed below. Closer inspection reveals that the integrated I-V curve is smoother than the differential conductance trace which is partially a result of the higher accuracy of the lock-in measurements in combination with the integration process and the limited sweep step size of 100 μV of the SMU 236. Most importantly, the I-V curves show non-ohmic behaviour, the characteristic signature of quantum tunnelling, and demonstrates that tunnelling junctions can be formed using a low doped Si substrate at a temperature,

where substrate conduction is frozen out[1]. We found that an unpatterned control device shows no current flow up until bias voltages above $\pm$2.5 V. Whereas we might expect such tunnelling behaviour for gaps between two P-doped region by several Bohr radii of order $\sim$10 nm, a quantitative description of the tunnelling mechanism is not straight forward.

Powerful concepts such as Bardeen's 1D perturbative approximation have been used to describe the tunnelling current through vacuum between a metallic STM tip and a sample. However, such an approach is not applicable for our samples, since we do not tunnel though a vacuum barrier. Instead tunnelling occurs through low doped silicon that is no longer conducting at 4 K but which, from the doping density, contains about $\sim$5 P dopants in the gap. Similarly, Fowler and Nordheim (see for example in [226]) described one dimensional tunnelling between metal-semiconductor junctions with a thin SiO_2 barrier approximated by a triangular tunnelling potential. The tunnelling properties between two highly-doped P-doped triangular leads through a lightly doped substrate requires us to self-consistently and iteratively solve both, Poisson's equation and the associated Schrödinger equation in three dimensions. Whilst recent simulations [228] were undertaken to solve such type of equations for two single P atoms embedded in silicon, where the corresponding single particle wavefunction are well understood, a similar calculation for highly doped, planar P-doped structures remains the subject of further research and is beyond the scope of this thesis.

The four terminal nature of our device allows us to exclude poor electrical contacts as the origin for the observed non-ohmic behaviour. We have measured the two terminal I-V characteristics of the P-doped contact regions connecting the tunnel junction on each side. Fig. 7.4 shows the I-V characteristics of the two P-doped contact regions for both, the 1-3 and 2-4 current direction. Linear I-V behaviour can clearly be seen in both cases which unequivocally confirms that the non-ohmic I-V behaviour originates from the STM-patterned tunnelling junction. The two terminal resistances are quite different for the P-doped regions, namely 40 kΩ for the left side (1-3 direction) and 4 kΩ for the right hand side (2-4 direction). Whilst the exact cause of this resistance difference is unknown, it is likely to be due to different overlap areas between the P-doped regions and the respective metal contacts resulting in different contact resistances. The influence of different contact resistances on the actual device characteristics is however nullified by the use of a four terminal measurement.

[1]For our P-doped Si wafers with a resistivity of 1 – 10 Ωcm, the substrate stops conducting at $\sim$65 K.

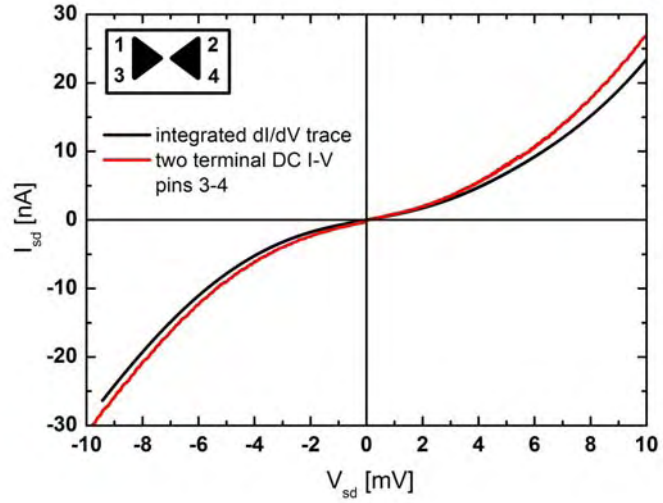

Figure 7.3: Comparison between four terminal (integrated $\frac{dI}{dV}$) conductance data (black curve, current: 1-2, voltage: 3-4) and two-terminal I-V data (red curve, 1-2 direction) obtained from DC measurements.

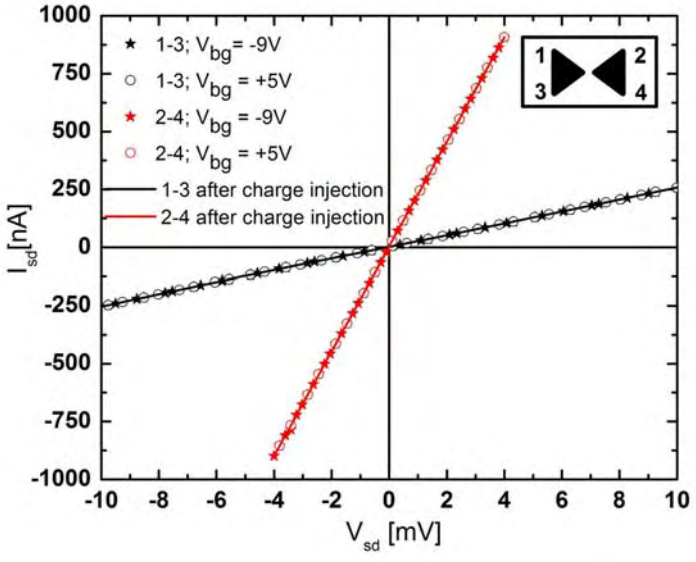

Figure 7.4: Two terminal DC characterisation of the P-doped contact patches. The conductance of the contact patches shows ohmic behaviour and is unaffected by both the application of backgate voltages in the range from -9 V to +5V and even after deliberately induced gate leakage. Note: the two terminal resistance of contacts 1-3 is 40 kΩ and 4 kΩ for contacts 2-4.

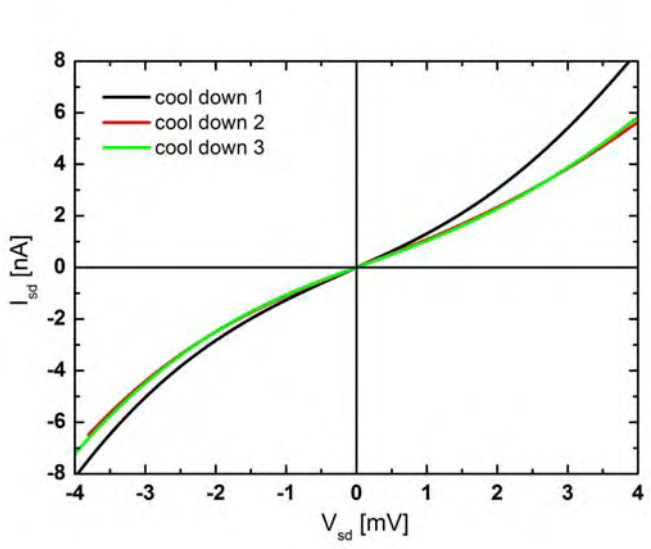

Figure 7.5: Reproducibility of electrical characteristics of 48 nm tunnelling junction. The I-V characteristics (integrated conductance traces) for 3 separate measurement cool downs are shown, indicating the level of stability towards thermal cycling.

We have also tested the stability of the I-V characteristics of the P-doped contact patches towards gating action using the conducting Au-coated bottom of the chip package as a backgate. As can be seen from Fig. 7.4, applying voltages in the range from +5 V to -9 V does not change the observed ohmic I-V behaviour of the P-doped side patches. Furthermore, it was found that even application of higher voltages of about +7 V, where electron impact ionisation from the backgate into the substrate causes charge motion due to significant gate leakage, has no influence on the I-V characteristics. Fig. 7.4 shows that the I-V characteristics of the side contacts are completely robust against the application of moderate backgate voltages and even gate-induced leakage currents through the substrate. This result will become important for the following sections, where gating of the tunnel junction will be discussed.

7.1.3 Electrical device reproducibility

It is well known that mesoscopic devices are sensitive towards thermal cycling, since the electrical characteristics may fluctuate due to small changes of the potential landscape at the atomic level. In the case of tunnel junctions formed by the silicon substrate, it is easy to understand that the number and charging states of dislocations,

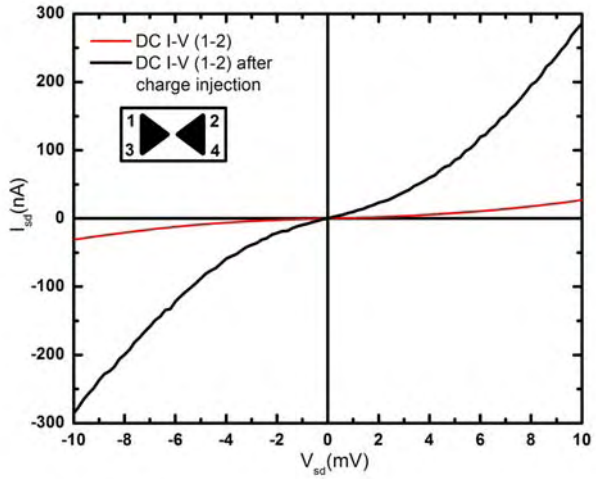

Figure 7.6: Influence on leakage-induced charge injection on I-V characteristics. Two terminal DC I-V characteristics before (red trace) and after (black trace) forced gate leakage shows that charge injection significantly increases the measured tunnelling current.

traps, defects and dopants have a significant influence on the potential landscape and therefore device conductance. Cooling the device from room temperature to 4 K freezes the P dopants in the substrate in a random, stress-induced, non-equilibrium state. Slower cool-downs allow the substrate to relax towards equilibrium leading to more reproducible device characteristics. In Fig. 7.5, the integrated I-V curves of three different thermal cycles are shown. For each of these cycles, we cool down the sample to 4 K over a period of 2 h to allow the substrate relaxation towards equilibrium. From Fig. 7.5, we found that the reproducibility of the I-V characteristics of the device was found to be about 30%; measured at a source-drain bias of 4 mV.

7.1.4 Effect of external backgate on device conductance

Commonly, the conductance of a tunnel junction can be manipulated by means of a capacitively coupled gate. Generally, this implies either a back gate, side gate or a top gate. In this section, we explore the possibility of the most simple gating technique which uses the conducting bottom of the chip package as a backgate. At 4 K, the substrate carriers are frozen out and the conducting bottom of the chip carrier is used to act as a gate which is located 300 μm away as given by the wafer thickness.

We find that we can apply a voltage range at 4 K for our back gate from -9 V to +5 V

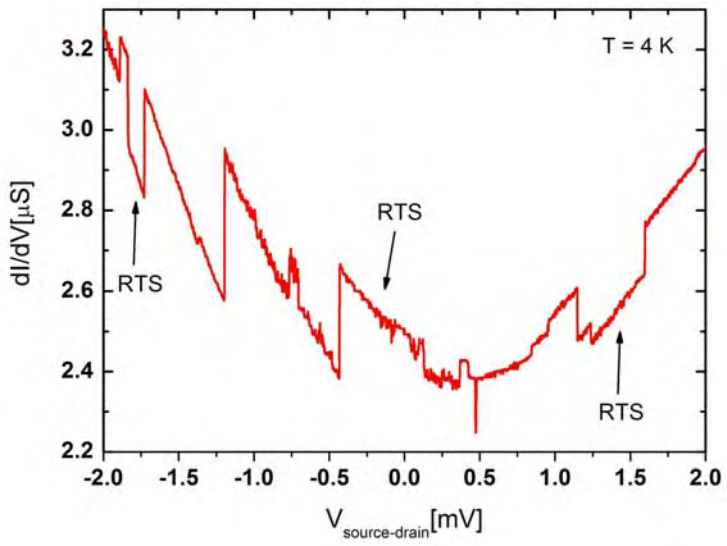

Figure 7.7: Random telegraph signals (RTS) arising from substrate charging. Induced gate leakage evokes charge motion in the vicinity of the tunnelling gap. RTS' result due to charge motion in the gap highlighting how the tunnel junction may be used as a sensitive charge detector.

for our P-doped substrates (room temperature resistivities of 1 – 10 Ωcm). In this voltage range, gate leakage currents are limited to <100 pA over the entire 1×1 cm^2 sized chip. Outside this voltage range, the substrate starts to break down due to electron impact ionisation which results in avalanche breakdown [226]. Consequently, charge injection into the substrate occurs which can be monitored using the gate leakage current. The substrate acts as a capacitor which exhibits a long charge relaxation time over several hours. This charge motion is sensed by the tunnel junction leading to a conductance increase. Fig. 7.6 shows the current increase in the tunnelling junction after deliberate charge injection. The current increase due to charge injection as shown in Fig. 7.6 (black curve) is not reproducible and depends on the specific conditions of the charge injection and avalanche breakdown paths. It is important to note that no change is observed in the P-doped contact region for the same backgate voltage as shown in Fig. 7.4. The increase in tunnelling current that occurs after leakage is caused by charge in the substrate lowering the potential barrier in the vicinity of the P-doped leads.

The influence of induced charge motion is further evidenced when considering the change in differential conductance with source-drain voltages as shown in Fig. 7.7. Here, we see the appearance of random telegraph signals (RTS) after induced substrate break down, which shows that charge movement takes place in the vicinity of the tunnelling junction, locally changing the potential landscape and resulting in sharp jumps in the differential conductance. The jumps in the differential conductance are most likely due to charging and discharging of a two-level system within the tunnelling gap. Similar behaviour has also been observed also reported to be observed in narrow silicon MOSFETs by Ishikuro *et al.* [229].

To test the effect of the backgate without going into the leakage regime, measurements were taken between $\pm$4 V. The change in differential conductance at a fixed DC source-drain bias of V_{sd} = - 1 mV was measured as a function of the backgate voltage using an AC source-drain excitation voltage of 50 μV at a lock-in frequency of 77 Hz. The backgate voltage is ramped from initially -4 V to -3 V using a ramp time of 30 min. Then, the differential conductance is measured as a function of time for 10 min to check if some leakage-induced charge relaxation takes place. Thereafter the backgate is swept by another 1 V followed by a 10 min time sweep up to a backgate of +4 V. By doing this, we can map out the conductance change of the tunnelling junction at a fixed source-drain bias of 1 mV in the backgate range from -4 V to 4 V.

Fig. 7.8 (a) shows the change in differential resistance for negative gate voltages (V_{bg}) between 0 V to -4 V. It can be seen that the differential resistance changes by about 60 % for V_{bg} between 0 V and -1 V. However, below -1 V, the differential resistance stays constant up to V_{bg} = -4 V. The upward and downward sweeps lie on top of each other. The absence of a hysteresis indicates negligible substrate charging due to gate leakage. A very similar effect is seen for the positive sweep direction in Fig. 7.8 (b) with the only difference being that the initial change in differential resistance between 0 V and +1 V is reduced to only $\sim$20 %. At present, the initial increase around $\pm$1 V in the conductance is not understood. It is possible, that initial substrate charging effects take place which saturates around $V_{bg} \sim \pm 1$ V but further investigation is needed to explore the origin of the change in conductance around zero gate voltage. The most striking feature, however, is that above $\pm$1 V, the backgate no longer affects the device conductance. Above V_{bg} = +3 V, there is bump in the $\frac{dV}{dI}$, which could be due a higher likelihood of charging approaching the gate breakdown voltage of +5 V. The negligible effect of the backgate can also be extracted from the time sweeps in Fig. 7.8 (c,d).

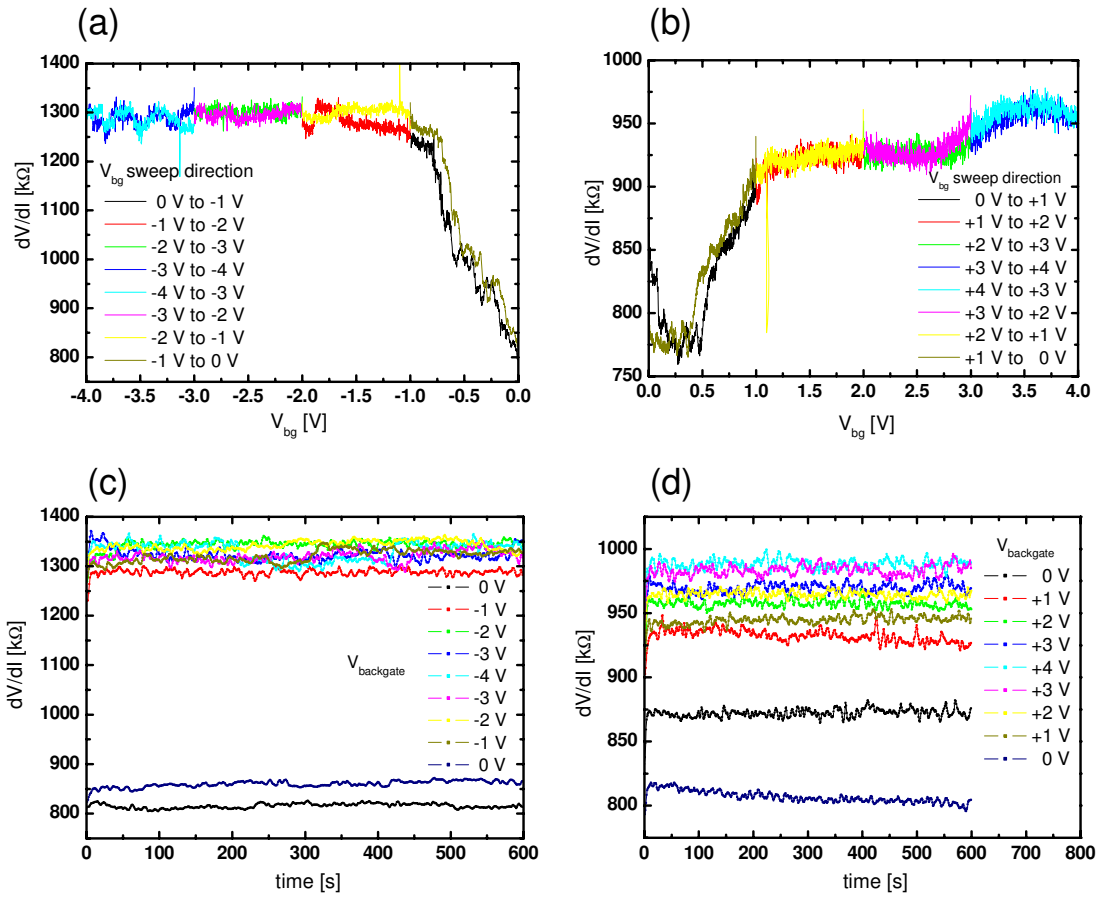

Figure 7.8: Effect of the chip backgate onto the differential resistance ($\frac{dV}{dI}$). The carrier backgate V_{bg} in the range from (a) -4 V to (b) +4 V (located 300 μm away from the device) initially increases the differential resistance in the range for $V_{bg} = \pm 1$ V but has little effect on the differential resistance outside this range. The differential resistance at fixed backgate voltages is shown as a function of time in (c) and (d) demonstrating that no substrate charging occurs.

The differential resistance is not changing above ± 1 V. Additionally, the differential resistance values at a fixed backgate voltage are very stable over the sweep time of 10 min showing no relaxation effects, therefore reinforcing our understanding that no gate-induced charge injection takes place and we have stable device characteristics.

In summary, the conducting bottom of the chip package, located 300 μm away given by the sample thickness, does not provide gating action of the conducting layer or the tunnel junction. This is mainly due to the fact that avalanche break down of the substrate occurs above -9 V and 5 V respectively – i.e. before gating has a significant effect. The critical control parameter needed to be considered is not the backgate voltage range but the electric field, that is applied before substrate breakdown occurs. According to the simple plate capacitor equation, the electric field is given by

$$E = \frac{V_{bg}}{d} \tag{7.3}$$

where d is the device-gate distance. The resulting electric field for a backgate voltage of $\sim$10 V and d = 300 μm is E $\sim$30 $\frac{kV}{m}$. From Eq. 7.3, we can see that the electric field scales with $\frac{1}{d}$ such that reducing the device-gate distance will not provide better gating action before avalanche breakdown. However, since avalanche breakdown is related to the substrate doping density, the use of lower doped substrates towards intrinsic silicon is a way to increase the critical electric field and represents a more promising pathway to observe gating action in our samples. Further studies are needed to determine what minimal substrate doping density is required to still be able to fabricate and image devices using STM.

7.1.5 Substrate bias cooling

Substrate bias cooling provides a proof-of-principle technique to investigate if significant gating action could be expected in the absence of substrate breakdown. The concept of bias cooling is simple. The underlying idea is to bias the substrate at room temperature and to maintain this applied potential during the device cool down to 4 K. As a result, the applied potential can be *frozen* into the substrate, thus the name *bias cooling*. The main advantage of this technique is to move the quasi Fermi level of the substrate with respect to the fixed Fermi level of the P-doped electrodes. Bias cooling has recently been applied to gated $GaAs/Al_xGa_{1-x}As$ [230] structures to reduce gate-induced noise performance by electrically saturating charge traps and impurities in the vicinity of the gate. More importantly, it has been used to change the

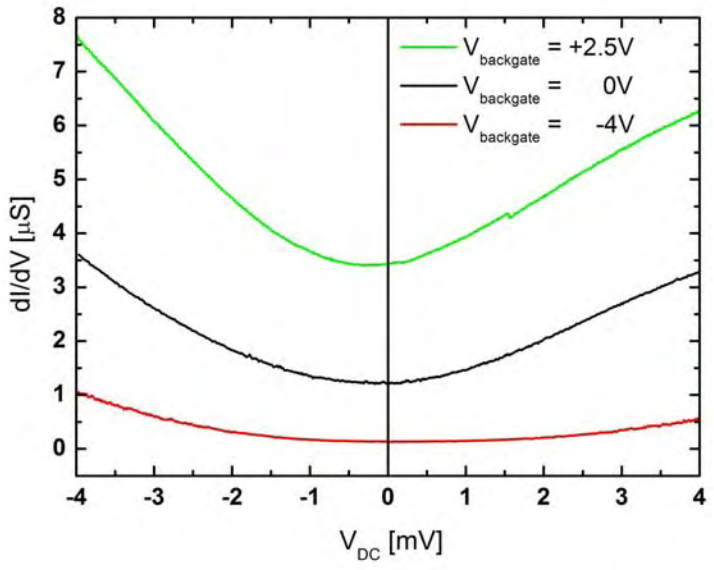

Figure 7.9: Bias cooling as a means of modulating device conductance. Summary of conductance data for different thermal cycles with the substrate frozen in with +2.5 V (green trace), 0 V (black trace) and -4 V (red trace) is shown. Positive substrate bias increases conductance whereas negative substrate bias decreases the device conductance well beyond thermal reproducibility indicating that proper gating action can be obtained using a gate in device proximity.

channel conductance in silicon inversion layers [231]. Applying a positive/negative bias effectively increases/depletes the carrier concentration in the silicon substrate region between the ultra-high P-doped contact regions. Due to the high doping level and Fermi level pinning by the source-drain metal leads, bias cooling affects the substrate potential much more than the P-doped STM-patterned nanostructure. Consequently, the barrier potential can be manipulated by application of different bias voltages. However changing the bias necessitates us to thermally cycle the device for each bias voltage, since the bias needs to be applied when the substrate is conducting at room temperature in order to locally change the Fermi level of the substrate between the tunnel junction. Therefore effects of bias cooling are intertwined with device reproducibility, since it is only possible to draw a significant conclusion on bias cooling if its effect exceeds the device fluctuations due to thermal cycling.

In Section 7.1.3, we determined that the device reproducibility towards thermal cycling is 30% indicating that the effect of bias cooling has to be well beyond this

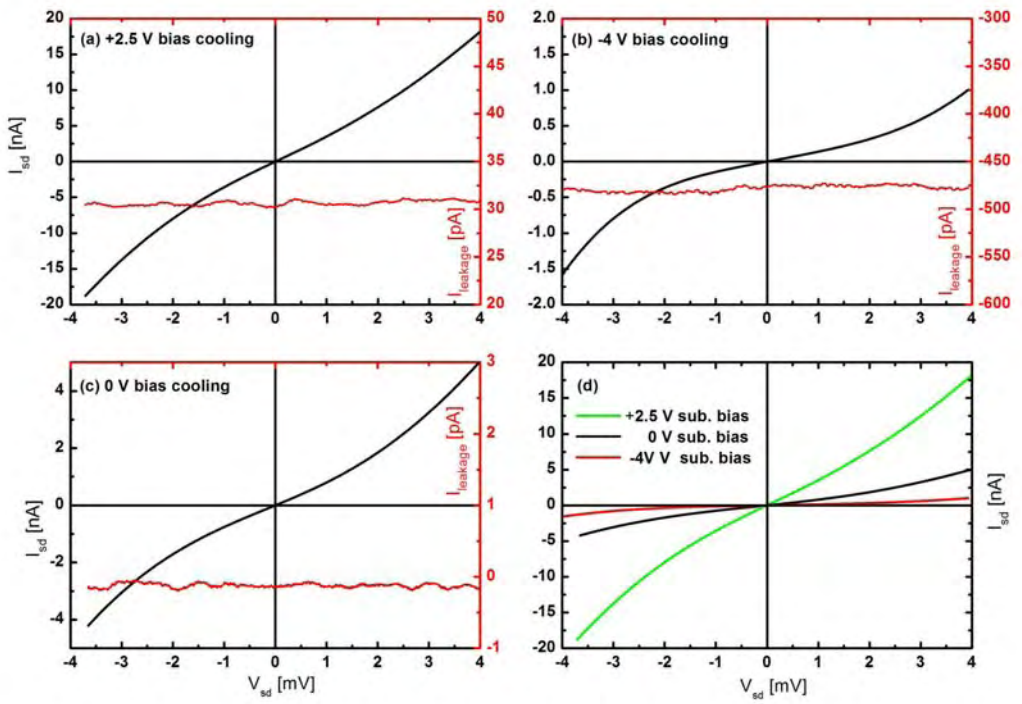

Figure 7.10: Comparison between bias cooling and leakage current. Integrated I-V characteristics and backgate residual leakage current for three frozen substrate biases of +2.5 V (a), 0 V (b) and -4 V (c) showing no correlation between bias source leakage (red traces) and resulting tunnelling current. A summary of the different I-V traces is shown in (d).

value to be significant. Fig. 7.9 shows a summary of differential conductance traces for three different thermal cycles cooled with biases of -4 V, +2.5 V and 0 V respectively. First, let's consider the conductance trace cooled down with zero applied bias (black curve), which lies within the 30 % thermal reproducibility compared to Fig. 7.2. The trace taken using a substrate bias of -4 V (red curve) lies distinguishably below the 0 V trace. On the contrary, a significant conductance increase is seen for the measurements using a substrate bias of +2.5 V (green curve).

A clearer picture of the bias cooling effect is gained from Fig. 7.10 (a-c). In Fig. 7.10, the three I-V curves integrated from the differential conductance traces [from Fig. 7.9] are shown. The respective leakage current as measured from the back gate to the substrate using a voltage source (SMU236) is also shown (red traces). The residual leakage current is very different for different biases, it is important to note that

the absolute leakage current value is neither correlated to the current change in the device nor dependent on the source-drain voltage. A lower leakage current is observed for a bias of +2.5 V as opposed to the -4 V data but the resulting tunnelling current compares to be one order of magnitude higher providing further evidence that the change in the non-ohmic I-V curves is not drawn from potential leakage of the back gate. Encouraged by this result, we compare the integrated I-V curves in Fig. 7.10 (d). From this graph, we see that bias cooling to +2.5 V increases device conductance fourfold whereas a bias of -4 V decreases conductance threefold compared to an applied bias of 0 V. This behaviour is expected since applying a positive/negative bias effectively increases/depletes the carrier concentration in the silicon substrate region thereby lowering/increasing the tunnelling barrier. We conclude that bias cooling is a means of changing the conductance of a P-doped STM-patterned tunnelling junction. Furthermore, the effect of bias cooling shows promise that a back gate in combination with a significantly lower substrate doping or in combination with an embedded SiO_2 layer i.e. a silicon on insulator (SOI) substrate, where the critical electric field is much higher, provides the ability to observe gating action in STM-fabricated tunnel junctions.

7.1.6 Photon-assisted carrier generation

Another way of controlling the conductance through the tunnelling barrier is the use of photon-assisted carrier generation. It is well known that photons with an energy above the Si band gap can be used to create electron-hole pairs [226] thereby increasing the number of free charge carriers. To give an idea about the mechanism behind photon-assisted carrier generation, we will provide an quantitative example for Si after [232]. Assuming, that the rates $G_{n,p}$ for creation of electrons and holes is equal, the carrier generation due to photon-assisted carrier generation is expressed by:

$$G_n = G_p = \alpha \frac{P_{opt}}{E_\vartheta} \tag{7.4}$$

where α is the photon absorption coefficient, P_{opt} is the light intensity, E_ϑ the photon energy. Typical values for our experiment are $\alpha = 10^{-3}$ cm^{-1}, $P_{opt} = 1 - 10$ mW/cm^2, $E_\vartheta \sim 1.8 - 2.0$ eV. It is possible to estimate the increase in carrier density due to photon-assisted carrier generation, δn, using

$$\delta n = \tau \cdot G_n \tag{7.5}$$

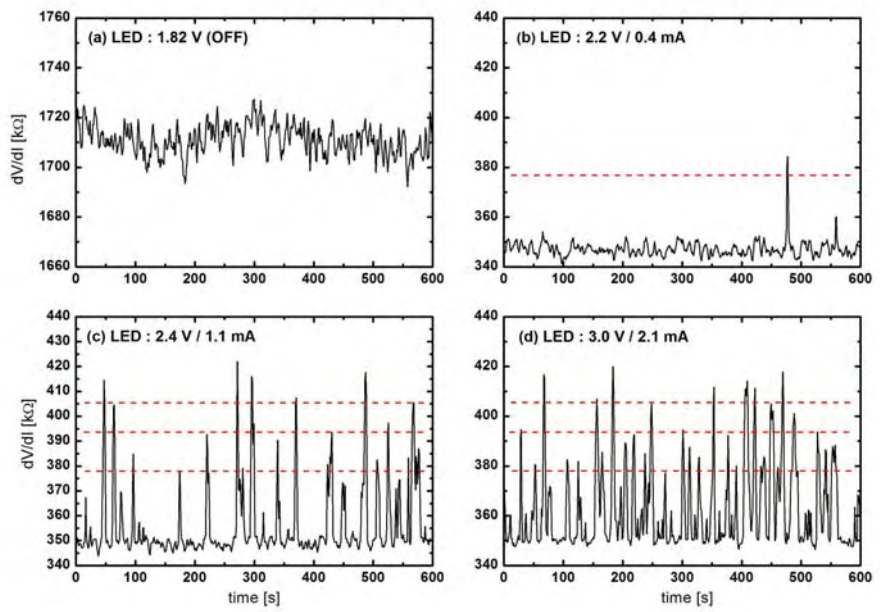

Figure 7.11: Photosensitivity of the 48 nm tunnelling junction. The differential resistance is shown as a function of time for a fixed source-drain DC bias of 1 mV (a). Upon switch-on of the light emitting diode (LED), the differential resistance reduces significantly (b). Further increase of the photon intensity retains the same resistance baseline but also exhibits superimposed conductance peaks. Dotted lines in (b)-(d) may indicate different potential states of the junction due to photon-induced charging/ionization and decharging/deionization of nearby traps/donors.

using a minority carrier lifetime of $\tau = 10\ \mu$s. As a consequence the number of generated carriers per cubic centimetre is of order $\delta n = 10^7 - 10^8\ \mathrm{cm}^{-3}$.

The generation of electron-hole pairs in the tunnel region is expected to have the highest effect on the substrate conductance due to the low doping compared to the highly P-doped leads. However charge carriers are also generated across the entire surface, such that a quantitative analysis of photon-assisted carrier generation on our tunnel junction is difficult to obtain. Therefore we restrict ourself only to a qualitative description of the effect of photons exposure on the differential resistance of the tunnel junction. Fig. 7.11 outlines the effect of photon adsorption in our sample at 4 K. A red LED is used which is capable of operating at 4 K emitting photons with an energy of $\sim$1.9 eV corresponding to a wavelength of 650 nm. It is worth noting that whereas the indirect band gap of Si is 1.1 eV, the direct band gap is higher at 3.4 eV. This means that

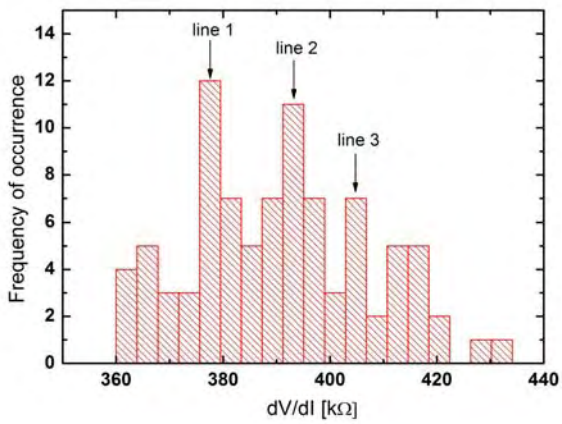

Figure 7.12: Combined peak height distribution from Fig. 7.11. Red lines in Fig. 7.11 correspond to the three peak heights at 378 kΩ (line 1), 393 kΩ (line 2) and 405 kΩ (line 3) respectively.

for generated carriers to contribute to conduction, they must undergo a significant change in momentum involving the crystal lattice via electron-phonon interaction. This will become increasingly difficult for lower temperatures as the phonon density decreases.

Fig. 7.11 (a) shows the differential resistance ($\frac{dV}{dI}$) at a fixed DC source-drain bias of V_{sd} = -1 mV with an AC source-drain excitation voltage of 50 μV at a lock-in frequency of 77 Hz. At an LED voltage of 1.8 V shown in 7.11 (a) (below the turn-on voltage), the differential resistance across the device remains constant at 1710 kΩ within a time sweep of 10 min which can be regarded as the baseline of our measurement. Fig. 7.11 (b) shows $\frac{dV}{dI}$ after LED turn-on at a voltage of 2.2 V at a LED current of 0.4 mA. The differential resistance has dropped by a factor of five to a new baseline at 350 kΩ. This decrease in the differential resistance is expected due to the generation of photon-induced charge carriers. Fig. 7.11 (c,d) represent time sweeps of the differential resistance for higher LED powers of 2.6 mW and 6.3 mW respectively. Comparing the behaviour of $\frac{dV}{dI}$ for a LED power of 2.6 mW with that of 0.4 mA, we immediately see that the baseline of 350 kΩ has not changing significantly. However, we do observe the presence of a series of sharp oscillatory spikes superimposed on the baseline. At photon energies of ∼1.9 eV, the photon energy is only sufficient to generate carriers via the indirect Si band gap. It is likely, that these resistance spikes are due to changes

in the potential landscape in the vicinity of the P-doped leads. The occurrence of resistance spikes increases with increasing photon intensity as seen by comparing Fig. 7.11 (c) and (d). A histogram showing the occurrence of resistance spikes as a function of the peak height is shown in Fig. 7.12. From the histogram (with a bin size of 4 kΩ), we can see that two peaks occur more than others – those at 378 kΩ and 393 kΩ. There is possibly a third peak occurring at 405 kΩ. The respective peak heights are indicated as red, dotted lines in Fig. 7.11 (b-d). Whilst the analysed number of peaks is not statistically significant enough to draw a solid conclusion, it appears that there may be three characteristic adsorption and charging events in the vicinity of the tunnel gap which are responsible for the occurrence of the resistance spikes in Fig. 7.11 (c,d).

Charging and discharging of charge traps or ionisation and deionisation of nearby P donors might be possible candidates for changes in the potential landscape in the vicinity of the gap. The formation of three distinct peak amplitudes as indicated by the red, dotted lines could indicate different charge systems (i.e. a charge trap or a P dopant) located at different distances or possibly even multiple charging events. It is clear that these observations are very speculative and that further research has to be undertaken to clarify our understanding. One such experiment may be to determine the response of the tunnelling characteristics not only for the photon density but also for the photon energy using a tunable laser. Another important experiment will be to measure the conductance of the gap as a function of temperature to determine the complex nature of charge transport.

7.2 Tunnel junction of 17 nm gap size

In this section, we present results from the smallest tunnelling junction fabricated to date. We will briefly discuss the fabrication process before presenting initial electrical characterisation measurements.

7.2.1 STM fabrication and device dimensions

Sample preparation and in-situ device preparation and processing is analogue to the 48 nm wide tunnelling junction as described in 7.1.1. Fig. 7.13 shows two STM images illustrating the main device features. The tunnelling junction consists of a ∼77 nm wide wire with a gap of ∼17 nm in size. Here, the parameters for STM lithography were chosen to be +6 V and 4 nA. The STM image shows the occurrence of an in-

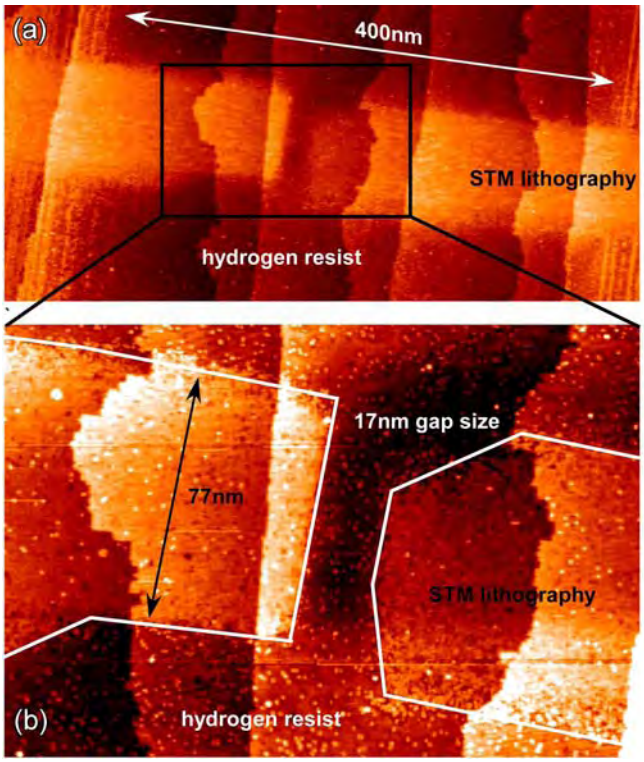

Figure 7.13: 17 nm gap four terminal tunnel junction. (a) Filled state STM image of a tunnelling junction consisting of a 400 nm long wire of 77 nm in width with a 17 nm gap. (b) a close-up STM image of the tunnelling gap is shown. Imaging conditions: -2 V, 0.18 nA.

creased dangling bond density around the edges of the lithographic pattern. These are due to incomplete hydrogen passivation and stray desorption during STM lithography. However, most of the desorption sites in the gap are single dangling bonds, where only one hydrogen atom has been removed. These are found unlikely to adsorb phosphine molecules at a dose of $1.1 \cdot 10^{-9}$ mbar for 15 min as found in a detailed study of PH_3 adsorption on a hydrogen terminated surface [66]. The lithography extends to about 200 nm on each side of the tunnelling gap, where it is met by a large lithographic contact patch of about 3.5×3.5 μm^2 in size. The lithographic pattern on the right side of the gap is not completely rectangular which is the result of piezo drift and a somewhat unreliable STM tip in that particular experiment.

The conditions for the (3.5 μm) side patches were 7 V and 3 nA with 800×800 points at a scanning speed of 3000 nms^{-1}. The upper STM image in Fig. 7.13 shows that the lithography in the side contacts is incomplete since individual desorption lines can still be seen. This is caused partly from initial piezo creep and an insuffi-

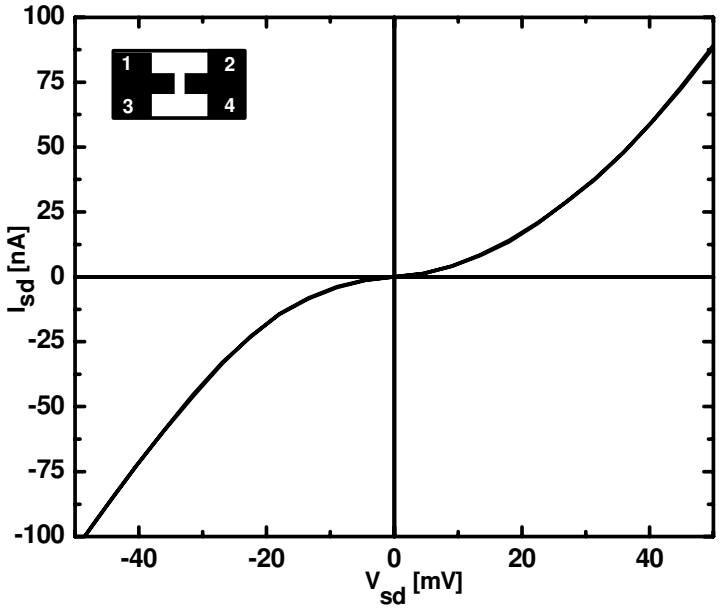

Figure 7.14: Two terminal DC I-V characteristic of a 17 nm tunnel junction.

ciently small separation between lithographic scan lines of 4.5 nm at a relatively high speed of 3000 nms^{-1}. However the quality of the desorption is sufficient to contact the wire ends (with an overlap of 200 nm) and to incorporate enough P atoms for ohmic conduction in the side contact regions as shown in the following section.

After STM lithography, the device is exposed to a saturation dose of PH_3, followed by a 5 min anneal using the e-beam heater of the SEM-STM system to about 350 °C which incorporates the P atoms while the hydrogen resist is left intact. Device encapsulation of 25 nm of epitaxial Si using MBE at 250 °C, undertaken by PhD student K. E. J. Goh, finalises the UHV fabrication process. Standard ex-situ device contacting procedures were performed as described in 7.1.1.

7.2.2 Electrical characterisation

All electrical measurements are carried out at 4 K. DC I-V data is taken using a Keithley source measurement unit SMU 236. Standard lock-in techniques are used at a fixed lock-in frequency of 4 Hz and excitation voltages up to 200 μV.

Initial device characterisation showed that the P-doped side patches were successfully contacted using the optical lithography process. The two terminal side contacts are found to be ohmic for AC excitation voltages up to 200 μV with resistances of 67 kΩ

and 38 kΩ respectively. The difference in these two terminal resistances is due to different overlap regions between the P-doped side patches and the Al contacts originating in different contact resistances. More importantly, the ohmic nature of conduction in the side contacts proves, that the buried P-doped device has been contacted properly i.e. the electrical characteristics across the tunnelling junction truly stems from conduction through the tunnelling gap. The two terminal resistance of the tunnelling junction is ∼3 MΩ at 200 μV for all contact combinations both across and diagonally across the device. For the 48 nm gap discussed previously we get a lower (four terminal) resistance of 820 kΩ at 200 μV which is counterintuitive since we would expect a higher resistance for the larger gap size. However, this discrepancy is most likely due to the different geometric shape of the two tunnelling junctions and emphasises that a quantitative description of the tunnelling process is needed for future comparison of tunnel junctions embedded in the silicon crystal.

The following measurements to characterise the I-V characteristics of the tunnelling junction are performed using the Keithley DC voltage source. A typical trace taken for DC voltages in the range ±50 mV is shown in Fig. 7.14. Clearly, non-ohmic diode-like behaviour is observed below voltages of ±35 mV. Outside this region, the device approaches linear behaviour with two terminal resistances of 570 kΩ at 50 mV and 480 kΩ at -50 mV.

An accidental voltage spike of 200 mV destroyed the tunnelling gap so that further electrical characterisation of this device was made impossible. Two terminal resistances afterwards showed linear behaviour with values down to 300 Ω which is of the same order as the internal loom resistance of the electrical setup i.e. the tunnelling junction was shorted. On the positive side, the sensitivity of the device towards voltage spikes further proves, that initial device characterisation indeed was performed on the 17 nm tunnelling gap.

The four terminal characterisation is not expected to be very different from the two terminal since the contact resistances of this device are of order 50 kΩ, whereas the device resistance is found to vary from several hundred kΩ to a few MΩ. It is anticipated that such a narrow tunnel junction will show similar gating characteristics as previously seen for a 48 nm gap.

In summary, we showed that the P-doped side patches show low resistance ohmic behaviour whereas the I-V behaviour across the tunnelling junction is non-ohmic exhibiting high resistance values. Future research will be directed towards narrower

gaps to investigate the minimal source-drain separation which still shows insulating behaviour at low source-drain bias.

7.3 Chapter summary and further work

The possibility of creating tunnel junctions using STM lithography and local P-doping by selective adsorption was investigated in this chapter. Two gap sizes of 48 nm and 17 nm were electrically characterised using DC voltage sources and standard AC lock-in methods. For both gap sizes non-ohmic behaviour is found. These devices are the first of its kind to be demonstrated following the initial proposal by Tucker *et al.* to use P δ-doping in conjunction with STM lithography to realise planar single electron transistors (SETs) [163] in 2000.

Due to the use of a four terminal contact method, it has been possible to show that the non-ohmic behaviour observed is indeed caused by the tunnel junction formed using STM lithography. Gating using the conducting bottom of the chip package, located about 300 μm away from the device region, has little effect on the conductance behaviour of the junction. However by applying the method of substrate bias cooling, the conductance can be varied by an order of magnitude. These results indicate that gates in close device proximity in conjunction with lower doped substrates and/or a SiO_2 barrier are likely to show controllable gating action. We also tried to modulate the conductance of the junction by photon-induced carrier generation emitted by a LED, which was found to increase the device conductance fivefold. The increasing occurrence of conductance spikes with increasing photon intensity might be related to charging/decharing events of traps and/or the presence of P dopants in the vicinity of the tunnel gap. Both, charge sensitivity and photosensitivity observed in STM-fabricated P-doped tunnel junctions will need to be investigated further. Future possible applications of buried P-doped tunnel junctions may therefore include their use as local charge sensing devices.

The complex shape of the tunnel barrier formed by the Si substrate does not lend itself easily to a functional, quantitative description. Theoretical efforts in collaboration with A/Prof. Lloyd Hollenberg at the University of Melbourne, Australia are under way to employ modelling of such devices but remains the subject of future research.

Further work also includes the measurement of the 48 nm gap conductance at fixed biases over a large temperature range i.e. from 1 K to 40 K using a variable temper-

ature insert in combination with a ^{3}He/^{4}He liquid helium dilution fridge. At higher temperatures, the tunnelling current is expected to increase due to thermally activated tunnelling. However, the tunnelling barrier height formed by the substrate is also temperature dependent. From the temperature-dependent I-V behaviour, the tunnelling gap can be extrapolated for a fixed source-drain biases, so that by successive repetition at various biases, the energy dependence of the tunnelling barrier could be mapped out. The experimental results could then be used to test the outcomes of the device modelling.

Since the tunnelling current also strongly depends on the device geometry, the current devices cannot be directly compared with each other. Further work includes the systematic measurement of various gap size with the same geometry down to the sub 10 nm regime. Another interesting pathway to pursue is the variation of the substrate doping density as well as the use of p-type substrates as opposed to n-type substrate used currently.

We have seen that the differential conductance of the 48 nm junction has a smooth functional form without a resonant or a noisy structure. Now that we have characterised highly P-doped source-drain leads, we can also create small P-doped cluster or islands in-between. The formation of such devices is the subject of the next chapter, which will allow the study of effects such as coulomb blockade and resonant tunnelling behaviour.

Chapter 8

Formation and electrical characterisation of STM-defined Si:P islands

This chapter presents results from the formation of nano-scale, highly doped Si:P islands aligned between two Si:P leads, following the results from tunnel junctions presented in the previous chapter. Initially, we present a detailed STM study of the fabrication process for a $\sim$9 nm Si:P island showing all UHV device fabrication steps. In particular, we address the integrity of the island after hydrogen resist removal and try to determine how easy it is to align multiple structures in the same STM lithography step.

After this, we discuss the development of smaller registration markers, fabricated by electron beam lithography (EBL) to improve the alignment of electrical contacts to the buried device. Such markers are designed to improve alignment of the STM-patterned region to the registration markers which ultimately translates to better overall ex-situ contact alignment. In addition, the proximity of EBL-fabricated markers to the active device region opens up the possibility of Si terrace engineering in the device region. Finally, we apply a combination of optical and EBL markers to position a 90×70 nm^2 Si:P island with source-drain leads on a single, defect-free terrace. These large terraces are formed as a result of the pre-patterned EBL markers which cause stress-induced step-bunching on the surface. The electrical characteristics of the 90×70 nm^2 island device at 4 K are presented together with an interpretation of the nature of electron transport.

8.1 STM study on the formation of highly-doped Si:P islands

The aim of the following study is to determine how it is possible to measure/improve the alignment accuracy of lithographic structures patterned by STM and observe what happens to small nanostructures during the various UHV fabrication steps. These results provide vital information about some of the smallest structures that maintain their integrity during the UHV fabrication steps before device encapsulation. We also demonstrate that STM-induced local hydrogen resist removal is a viable alternative to thermal hydrogen resist removal for small devices since it completely avoids the issue of thermal processes which may lead to P diffusion.

The use of registration markers [31] in Chapter 4 was shown to be an elegant method of returning to the same area of the surface after each successive step of the device process thus allowing us to monitor the device structure as it is made. Fig. 8.1 represents a series of STM images during the fabrication of a 9×9 nm^2 island patterned between source-drain leads after each successive process step. Starting out with a hydrogen-terminated Si(100):H surface, we use an STM voltage of +6 V and a tunnelling current of 3 nA to selectively desorb hydrogen [11] from the surface in order to form the lithographic dot pattern. As shown in Fig. 8.1 (a), the pattern consists of a 9×9 nm^2 sized dot, centred with sub-nanometre precision between source and drain electrodes separated by 50 nm. To achieve this level of alignment, the STM lithography is performed in a single step write[1] within a scan frame of 500×500 nm^2 at a writing speed of 50 $\frac{nm}{s}$.

After saturation dosing for 20 min at a pressure of $1 \cdot 10^{-9}$ mbar (UHV base pressure $<5 \cdot 10^{-11}$ mbar) with PH_3 molecules [19], the dot size is reduced to about 8.5 nm as shown in Fig. 8.1 (b). This small reduction in size is due to some re-termination of the exposed Si surface with hydrogen arising from the dissociation process of PH_3 molecules to PH_x species. [151]. Fig. 8.1 (c) shows the incorporation of the P atoms from the PH_3 molecules into the top layer of the silicon crystal by annealing the sample to 350 °C [32]. At this temperature, the P atom from the adsorbed PH_x species incorporates into the silicon top layer [233], accompanied by further re-termination of neighbouring Si dimers with hydrogen atoms originating from the dissociation of the PH_3 species. A characteristic signature of P incorporation arises from the subsequent

[1] Beforehand, STM piezo relaxation is achieved by continuously scanning over the same pattern area for a few scan frames.

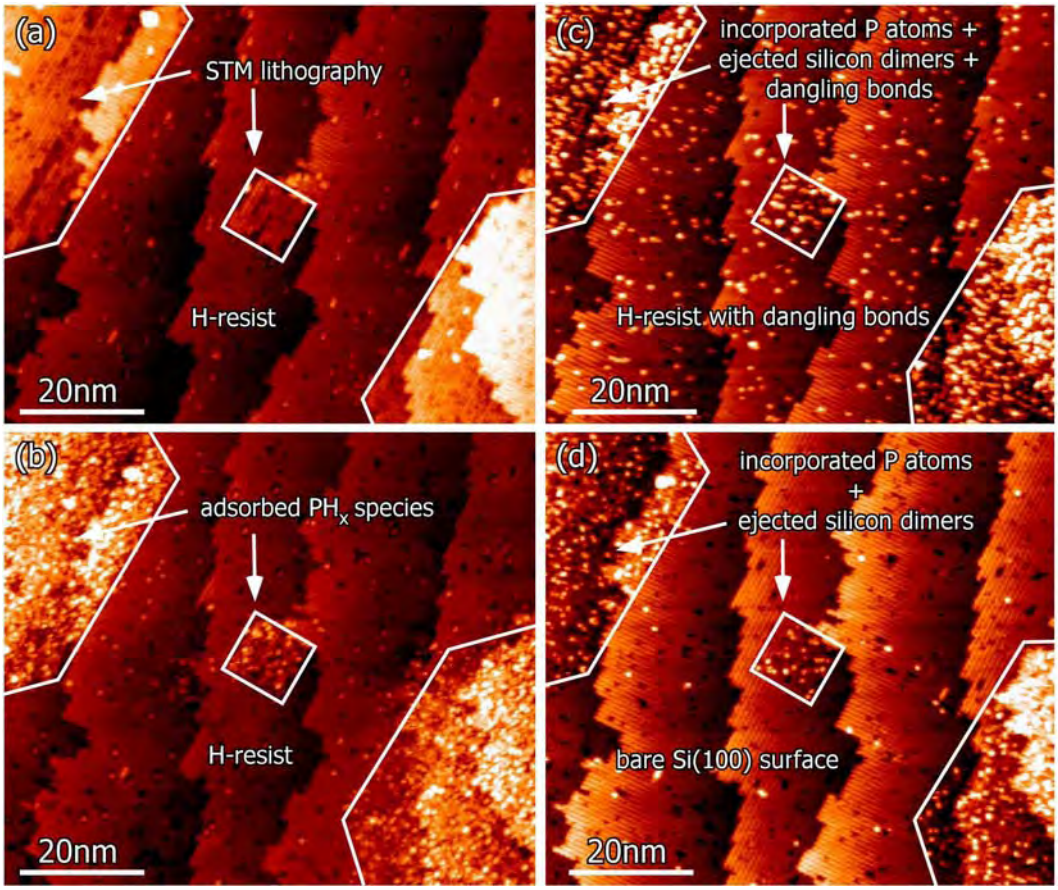

Figure 8.1: STM study of a ∼9 nm Si:P island with source-drain leads. (a) Filled state STM image of a Si(100):H surface after selective hydrogen removal to form source, drain and island pattern. (b) Same area after saturation dosing with PH_3. (c) After the P incorporation anneal to 370 °C, few dangling bonds are created in the hydrogen resist. (d) After STM-induced local removal of the hydrogen resist, the residual structures are incorporated P atoms and ejected Si chains. Imaging conditions: V ∼ -1.8 V, I ∼ 0.15 nA.

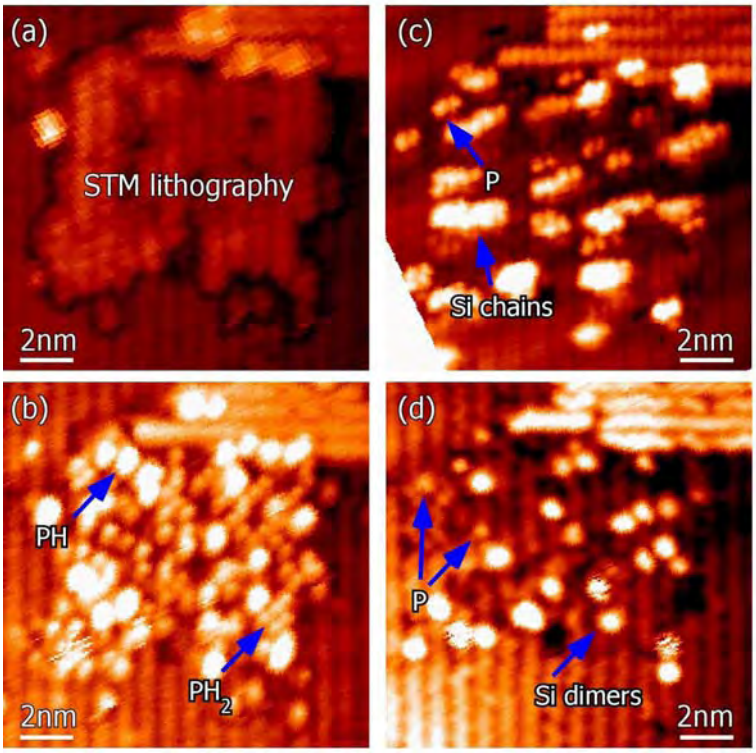

Figure 8.2: High resolution STM images of the ∼9 nm Si:P island. Filled state STM images after (a) STM lithography, (b) saturation dosing with PH_3. (c) STM image after thermal P incorporation at ∼370 °C (with double tip imaging artefact) and after (d) STM-induced hydrogen resist removal. Imaging conditions: V ∼ -1.8 V, I ∼ 0.15 nA.

ejection of Si atoms which form Si chains on the next silicon layer. These Si chains align perpendicular to the underlying Si dimers and have a characteristic height of 1.4 Å. The Si chains are generally much more visible than the incorporated P atoms, since they lie on the next terrace up and appear very bright in STM imaging. The presence of Si dimers and a few Si chains on the Si top layer can be seen from Fig. 8.1 (c) [and later on in more detail from Fig. 8.2 (c)] in both, the Si:P island and the Si:P source-drain leads respectively. We note that we also observe random hydrogen desorption events on the resist due to a slight overshoot in annealing temperature to ∼370 °C. These random dangling bonds make it difficult to distinguish the incorporated P atoms in the doped region, since the geometric height for Si dimers is comparable to the electronic height of the dangling bonds. However, from Fig. 8.2 (c), we can see that the structural integrity of the dot is still maintained despite the temperature overshoot. An elegant way to facilitate the identification of the surface species is to locally remove the hy-

drogen resist using the same STM parameters as previously used for the creation of the lithographic pattern itself. Other hydrogen removal techniques discussed in the literature include optical stimulation [234], [235], removal using electron beam lithography [236] and thermal removal [67]. Provided that the STM tip is stable during the lithographic process, STM-assisted removal allows complete and contaminant-free removal of the hydrogen resist and comprises an interesting technique for careful, local resist removal. The effect of STM-assisted hydrogen removal using a bias of 6 V, a current of 3 nA and a scan speed of 100 $\frac{nm}{s}$ is shown in Fig. 8.1 (d). From this, we can readily see that the initial device integrity is maintained.

We now focus on the evolution of the island during the process using high resolution STM images shown in Fig. 8.2 (a-d). Comparing Fig. 8.2 (a) and (b), it is readily seen that PH_3 precisely adsorbs on the exposed Si area and not on the surface protected by the hydrogen resist. Fig. 8.2 (b) also shows local regions of $p(2 \times 2)$ ordering of PH_2 and $c(4 \times 4)$ ordering of PH. Fig. 8.2 (c,d) show the different appearance of the Si:P island before and after STM-stimulated hydrogen resist removal. Note that Fig. 8.2 (c) shows a slight double tip imaging artefact which makes the STM image somewhat blurry. However, we can see clear signs of silicon ejection as evidenced by 1D chains perpendicular to the underlying dimer rows. After STM-induced hydrogen removal, these Si chains become circular in nature [237]. The bright appearance of Si dimers makes it impossible to obtain a reliable estimate of the incorporated P atoms, since the STM resolution shown in Fig. 8.2 (d) is not high enough.

From Fig. 8.1 (d), it is not possible to clearly identify the individual P atoms themselves. However, the Si:P islands and the respective leads appear structurally equivalent which allows us to estimate[2] the number $\aleph_{9nm}$ of P atoms forming the island:

$$\aleph_{9nm} = 8.5 \cdot 8.6\ nm^2 \times 1.7 \cdot 10^{14}\ cm^{-2} \approx 120\ P\ atoms \tag{8.1}$$

where $\aleph_{9nm}$ is simply given by $1.7 \cdot 10^{14}$ cm^{-2}, the saturation P density, multiplied by the island size taken from Fig. 8.1 (d).

A summary of the apparent island dimensions[3], its separation to the neighbouring leads and their respective width is given in Table 8.1. It is worth noting that the island dimensions are maintained through the entire fabrication process with an accuracy of $<$1 nm. For the right lead-island separation, there is one fluctuation between the

[2]Here we assume that the source and drain density corresponds to the P saturation density as confirmed from Hall measurements of an STM-fabricated Van-der-Pauw structure.

[3]Values are evaluated from Fig. 8.1 and Fig. 8.2

Structure	Lithography	PH_3 dosed	P incorporation	H desorption
island	9×9 nm^2	8.6×8.6 nm^2	8.4×8.3 nm^2	8.6×8.5 nm^2
left junction	20.5 nm	20.4 nm	20.8 nm	21 nm
right junction	20.5 nm	17 nm	21.8 nm	21.5 nm
width left lead	34 nm	34 nm	34 nm	35 nm
width right lead	34 nm	30 nm	33 nm	34 nm

Table 8.1: Fluctuations in device dimensions after STM lithography, PH_3 dosing, P incorporation anneal at 370 °C and after STM-induced, local removal of the hydrogen resist.

lithographic step (20.5 nm gap) and after PH_3 dosing (17 nm gap). Comparison of the initial dimensions with that after P incorporation and STM-induced hydrogen removal reveal, that the initial width (20.5 nm) of the gap remains the same. A plausible explanation for this may be that PH_x initially adsorbs on some induced stray hydrogen desorption sites located between the source-drain leads. However, an insufficient number of dangling bond sites around the PH_x species causes the molecules to desorb during the annealing step rather than the P atom to incorporate. Whilst it is possible to image PH_3 fragments on H-terminated surfaces, it is not easy to obtain high resolution images, which is most likely due to PH_x adsorbates attaching/detaching to/from the STM tip while imaging.

These images demonstrate, that it is possible to align a sub 10 nm Si:P island next to source and drain leads with a high accuracy of $\sim$1 nm in the same lithographic step. The following section is dedicated to improve the alignment of the STM-fabricated structure to registration markers by extending the existing registration marker process to incorporate electron beam lithography.

8.2 Combining registration markers created by optical and electron beam lithography

So far in this thesis, all devices have been fabricated on Si(100) samples with etched registration markers defined by optical lithography. The smallest etched features achieved using our in-house optical lithography process are of order $\sim$1 μm. This $\sim$1 μm limit is set by the UV wavelength of 365 nm used for pattern exposure and the contact quality between sample and optical mask. To reduce the feature size below $\sim$1 μm, we have developed a registration marker process which uses electron beam lithography (EBL) to define the markers. In these initial studies, we have combined

the use of smaller EBL-defined registration markers aligned to existing markers defined by optical lithography. Future devices are envisaged to be fabricated completely using only EBL for its increased alignment accuracy, smaller feature sizes and design flexibility.

The starting point is a sample that already contains etched registration markers defined by optical lithography before oxide layer removal [see also Fig. 4.2 (c)]. These existing markers are subsequently used for alignment of smaller markers created by EBL as shown in Fig. 8.3.

Below is a brief summary of the necessary developmental challenges overcome in collaboration with PhD student Mladen Mitic, who performed the EBL steps:

- Develop non-contaminating, metal free fabrication process using EBL
- Evaluate PMMA resist thickness and corresponding electron doses for reliable pattern writing
- Determine relation between oxide mask thickness and final, etched feature size
- Develop a suitable etch rate allowing few nanometre control of marker depth

A crucial stepping stone for the development of an EBL registration marker process is a UHV compatible fabrication procedure. Generally, electron beam lithography is used after sample growth where the required sample cleanliness is mainly determined by the need for high-resolution pattern writing. For STM devices fabricated in a UHV environment, device cleanliness at the atomic level is essential for devices so that no contamination of the UHV system occurs and that we can perform atomic resolution STM imaging on patterned samples. Therefore, great care was taken to avoid physical contact of the Si substrate with contaminating substances, such as traces of organic resist and residues of metal. Primarily to avoid metal contamination, typical steps like resist spin-on, sample transfers are performed using ultra-clean plastic tweezers. Additionally a cleaned 2" wafer piece is used as a spacer between sample and metal parts during all stages of resist spin on, resist bake and pattern writing.

Au clusters, normally deposited on samples to facilitate electron beam focussing before lithography, are placed on identical height, adjacent samples, so that beam optimisation is possible without sample contamination. Finally, wet-chemical cleaning steps are used to clean wafers such as SP and RCA-2 clean (for details see Chapter 4)

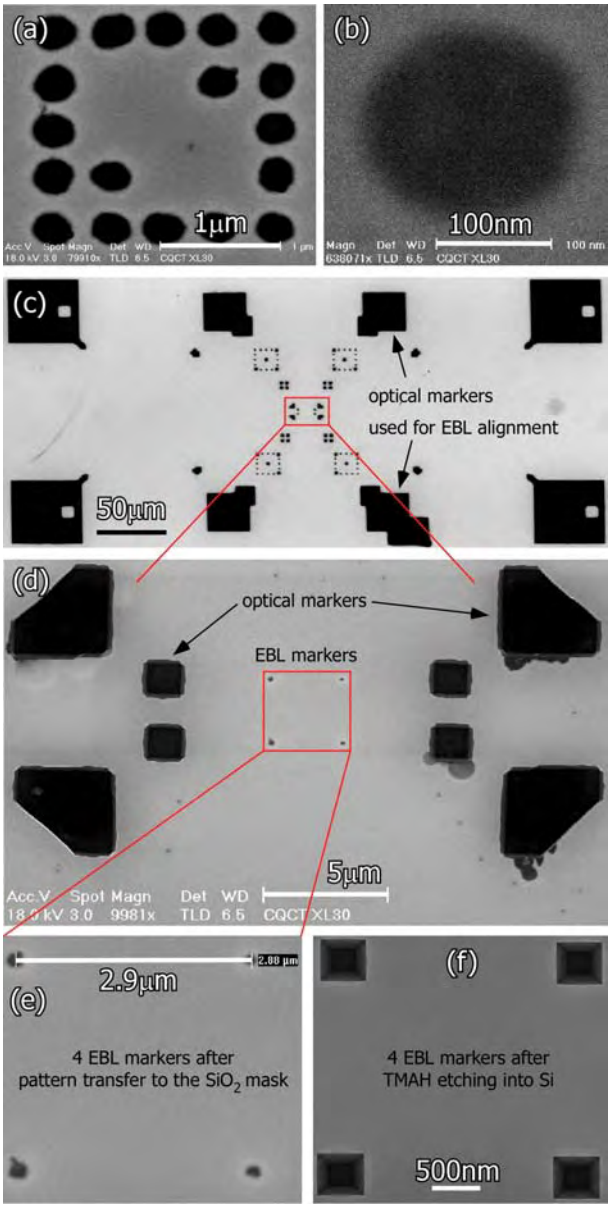

Figure 8.3: Aligning EBL-fabricated markers to optical registration. Series of SEM images showing (a) an array of 200 nm wide circles etched into SiO_2 layer and (b) a close-up of one of small registration marker forming the array. (c) SEM image of the combined optical and EBL marker set. The smaller squares on the inside corners of the optical markers are created during the EBL alignment procedure. SEM images of (d) central device area showing four EBL-fabricated apertures. Four EBL-fabricated apertures (e) before and (f) after TMAH etching.

aimed to eliminate traces of organic and metal residues before introduction into the UHV environment of the STM-SEM system.

To align EBL markers to the existing optical markers, the optical markers have to be clearly visible in the scanning electron microscope (SEM) underneath the PMMA resist used for electron beam lithography. Electron doses of 300 $\frac{\mu C}{cm^2}$ were found to provide a sufficient dose for reproducible marker definition in the EBL resist. We found this was possible for resist thicknesses of <60 nm. Initially, we used a low PMMA resist thickness of 20 nm. However, we found that a thickness of 20 nm is not sufficient to reproducibly define markers during pattern transfer from the resist to the SiO_2 mask layer in a HF bath, since the robustness of the PMMA resist was affected by the etch. This leads to a variation of feature sizes due to an etch undercut attributed to a lack of adhesion and integrity of the PMMA as shown in the variation of the diameter of the individual dots in Fig. 8.3 (a,b). Using an increased PMMA thickness of 60 nm and thinning down the SiO_2 mask from initially ∼100 nm to ∼60 nm significantly improved pattern definition.

The four optically defined squares (30μm in size) in Fig. 8.3 (c) were used to align four apertures of about ∼200 nm in size in the central area between the smallest, optical registration markers shown in Fig. 8.3 (d,e). The smaller squares (15μm in size) on the inside corners of the optical markers are created during the EBL alignment procedure. After the marker pattern is transferred to the SiO_2 mask, we use the same etch, TMAH, as for the initial Si etching of the optical markers. Better control over the final marker depth requires a slow etch rate. Reducing the temperature of the TMAH etch bath, from the standard 60 °C, used for the optical markers, to room temperature, the etch rate is reduced from ∼150 $\frac{nm}{min}$ to ∼8 $\frac{nm}{min}$ which represents a much more controllable etch rate for marker depths of order several tens of nanometres. It is important to note that the size and depth of the registration markers after the TMAH wet etch into Si is mainly determined by the etch time rather that the initial marker size. Once an aperture has been opened, it will seed the formation of an inverted pyramid-like etch pit (along the Si(111) axis) depicted in Fig. 8.3 (f).

We have tested two different EBL registration marker designs on the Si surface structure. Fig. 8.4 (a,c) are SEM images taken in the UHV STM -SEM system and (b,d) are the respective STM images after sample annealing to 1200 °C for 30 s. Fig. 8.4 (a,b) consist of a six squares structure of 500×500 nm^2 squares. The inner two registration markers close to the device centre were designed to facilitate alignment of smaller

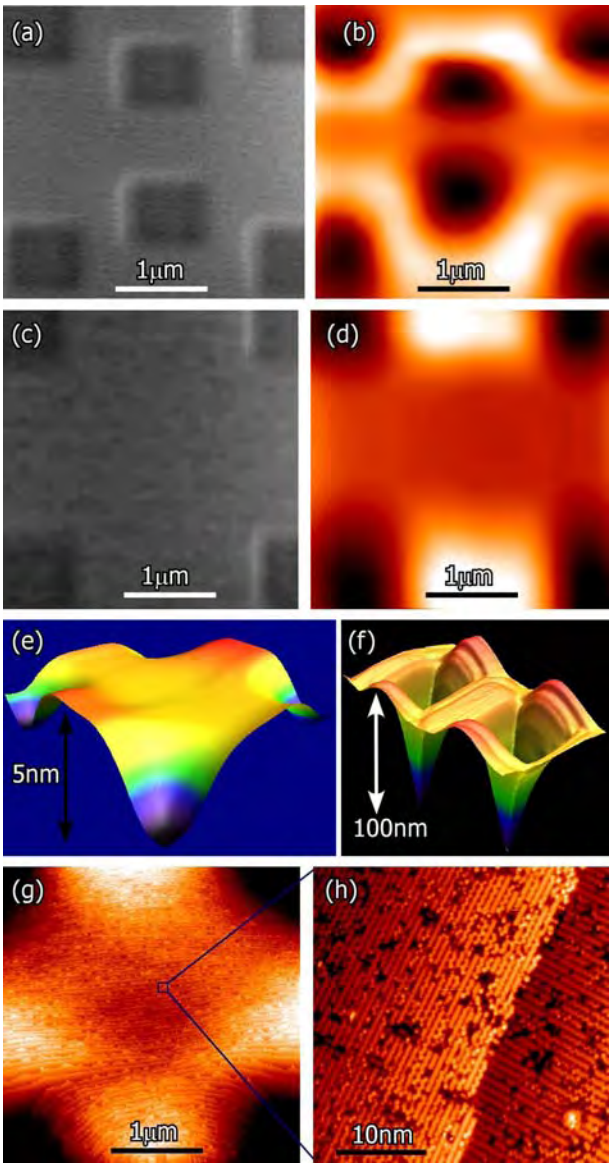

Figure 8.4: SEM and STM images of optical- and EBL-fabricated markers. SEM images (a), (c) and corresponding STM images (b), (d) of two different sets of EBL markers. (e) 3D plot of four shallow EBL markers. STM images of (f) deep markers defined by optical lithography, (g) shallow markers created by EBL and (h) high resolution image of (g) demonstrating the surface quality.

STM-fabricated nanostructures. Fig. 8.4 (c,d) show the second structure, a four squares structure. Apparent marker depth from STM profiling after sample annealing to to 1200 °C is about 70 nm with an initial etch depth of 400 nm after TMAH etching. These two test structures revealed an important difference in their influence on the terrace structure of the resulting surface which seems to depend on both, the marker arrangement and their relative location. The four squares structure in Fig. 8.4 (d) exhibits more diffusion alongside the Si dimer row direction than perpendicular to the dimer rows due to a lower diffusion activation energy [134]. We also note that a large, circular terrace structure is formed in the central area and we will show in the following section how we can use Si terrace engineering to create devices on single, mono atomic terraces. The minimal etch depth for markers still visible in the SEM of the STM-SEM

Etch depth	marker depth after annealing	marker definition after annealing
400 nm	70 nm	800 nm
200 nm	8 nm	500 nm
40 nm	4 nm	1000 nm

Table 8.2: Initial etch depth, etch depth after annealing to 1200 °C and marker extension on the Si surface after annealing for three different EBL marker depths.

system was found to be ∼80 nm. Markers exhibiting depths significantly smaller can still be imaged using the STM. Fig. 8.4 (e) shows a 3D STM contour plot of a shallow four dot structure. The initial marker depth after TMAH etching was ∼40 nm, which significantly reduced to ∼4 nm after UHV sample annealing to 1200 °C for 30 s. Whereas the markers are invisible to the UHV SEM, they remain clearly visible using the STM. It is worth noting that their definition has been blurred out significantly to a size of ∼1 μm such that further size reduction is not likely to increase device alignment. Increasing the Si etch depth to 200 nm using the same pattern design results in a final depth of ∼8 nm, making the markers more defined and confined to about 500 nm in diameter as shown in the 3×3 μm^2 sized STM image in Fig. 8.4 (g). Table 8.2 summarises the relationship between initial etch depth, marker depth after annealing to 1200 °C and marker extension on the Si surface after annealing for initial EBL marker depths of 400 nm, 200 nm and 40 nm respectively. From Table 8.2, we can see that a marker depth of 200 nm provides the best marker definition of ∼500 nm after the surface preparation anneal to 1200 °C. The lower etch depth of 40 nm significantly washes out marker definition to ∼1000 nm due to Si diffusion during the high temperature anneal, whereas a deeper etch depth of 400 nm increases the marker ex-

tension to ∼800 nm due to the anisotropical etch behaviour of TMAH. For comparison of marker definition, we also show a 3×1.5 μm^2 large 3D contour plot of two of the smallest 1 × 1 μm^2 sized optical markers on the same chip, which are much more well defined due to their bigger size. Finally, we demonstrate that EBL patterning has not adversely affected the surface quality. Fig. 8.4 (h) shows a high resolution STM image. From this image, we can see that the surface exhibits an acceptable defect level of 5 % in this particular example.

We conclude, that it is possible to fabricate UHV compatible registration markers using EBL. Such markers facilitate device alignment since they can be positioned close to the device region allowing the placement of STM-patterned structures in the same scan frame as the markers themselves. Shape preservation and marker definition at the scale of typically several hundred nanometres is mainly governed by the marker size and less dependent on the marker etch depth. The reason for this is the strong size dependence of the marker depth due to silicon diffusion at high temperatures [135] which we saw for the optical markers in Chapter 4. We found that using a standard wet chemical etch (TMAH), we can define markers in the surface to a resolution of 500 nm with a depth of 8 nm after high temperature surface preparation in UHV. Future development should investigate markers etched using reactive ion etching (RIE), where the ability to etch isotropically may form deeper well-defined markers.

The absolute alignment accuracy between STM-patterned device and metal contacts that can be achieved with this registration technique is currently about ∼100 nm. Further improvement of the alignment below 100 nm remains the subject of future work. One of the limiting factors for future alignment improvement is the ability to create highly defined, small markers due to inherent Si self-diffusion at high temperatures needed for atomically clean sample preparation.

A self-aligned STM process such as the one presented in Section 8.1 and in the following section where the essential device elements are all aligned in the same STM lithography step with ∼1 nm precision provides the highest level of alignment.

8.3 90×70 nm^2 Si:P island between source-drain leads

Whilst several devices were made, in the following the formation and electrical characterisation for a 90×70 nm^2 Si:P island will be discussed. For this device, we changed the previously used 1 – 10 Ωcm, n-type Si(100) with a Si(100) silicon-on-insulator

(SOI) substrate with the aim of trying to modulate the device conductance using a backgate. The SOI substrate consists of a degenerately As-doped handle wafer (backside) of 500 μm thickness with a resistivity of 0.001 – 0.004 Ωcm (doping density 2 – $5 \cdot 10^{-19}$ cm^{-3}), such that wafer backside conduction does not freeze out at liquid helium temperatures for backgating purposes. A 500 nm thick buried oxide (BOX) separates the handle wafer from a P-doped Si(100) device layer with a thickness of 2 μm and a room temperature resistivity >100 Ωcm (bulk doping density $<4 \cdot 10^{13}$ cm^{-3}). Such a doping level is used to enable room temperature conduction to facilitate STM lithography but provides an insulating substrate for measurements at low temperatures.

8.3.1 Device fabrication

Following the patterning of 150 nm deep registration markers created by UV optical lithography, electron beam lithography is used to define four apertures with a diameter of 200 nm aligned to the existing, optical markers. The four apertures are separated by 2.5×2.5 μm^2 to form a square within which the device is centred. After another TMAH etch, the previously etched, optical markers are now 450 nm deep whereas the EBL markers exhibit a thickness of 300 nm.

After initial outgassing at T $\sim$ 400 °C in the UHV environment for several hours, the device sample is annealed to 1200 °C for 10 s, followed by hydrogen termination using a beam of atomic hydrogen. Fig. 8.5 (a) shows the hydrogen-terminated, device region including the four depressions arising from the four patterned EBL markers. After sample annealing the marker depth reduces from initially 300 nm to an average depth of 25 nm. In Chapter 4, we have seen that the optical markers leaves the terrace structure in the active device area unaffected, since the markers are located 5.5 μm away from the active device region. However, the proximity of the EBL markers to both, themselves and the active device region in this sample allows us to influence the terrace structure in the device area. The result is best seen in Fig. 8.5 (b) which represents a high-pass filtered STM image to enhance edge contrast of a larger region of Fig. 8.5 (a). During the high temperature sample anneal, the silicon atoms are highly mobile causing them to diffuse in the direction of the topographic gradient given by the highly inhomogeneous surface profile due to the presence of the markers. Compensation diffusion will eventually fill the markers holes as is observed by the decrease in marker depth during the annealing step. This leads to the formation of a

saddle point protrusion in the central device area, the very centre of which consists of a monoatomic, circular terrace with a diameter of up to 1 μm. Similar structures were reported by Blakely and coworkers [238], [239]. In their study, the formation of saddle points and circular bottom pits was found after annealing a 400 nm grating fabricated by electron beam lithography and reactive ion etching and substrate annealing to a temperature of 950 °C.

The topmost terrace, depicted in Fig. 8.5 (c), exhibits a clean, almost defect free terrace with a diameter of about 500 nm. From the STM images taken in this experiment, no dimer rows are seen on the topmost terrace. However, this might simply be due to a lack of STM resolution. This is the ideal surface structure for the fabrication of the active device region on a single terrace. Fig. 8.5 (d) shows the lithographic pattern of the 90×70 nm^2 island structure created by STM including triangular source and drain leads. The actual device dimensions are illustrated in Fig. 8.5 (e). The left island-lead separation is 50 nm, whereas the right one is slightly less with 48 nm. From the island dimensions, the estimated number of P atoms after P incorporation is given by:

$$\aleph_{90\ nm\times 70\ nm} = 90 \cdot 70\ nm^2 \times 1.7 \cdot 10^{14}\ cm^{-2} \approx 11000\ P\ atoms \tag{8.2}$$

The lithography conditions for the central device pattern are chosen to be 6 V and 3 nA slightly lower than the 4 nA used for most devices in this thesis to further minimise the formation of accidental dangling bonds in the gaps. To contact the device, 800×800 nm^2 side patches are added to the opposite ends of the triangular source-drain leads. These patches are themselves connected to 3 μm wide and 2 μm long squares which provide sufficient overlap to the four Al metal contacts created in the subsequent optical lithography alignment process. For both lithography steps, we use a higher STM voltage of +7.5 V to allow for a higher writing speed of 2000 $\frac{nm}{s}$. The entire device patterning process takes about 6 h, followed by PH_3 dosing, P incorporation and Si encapsulation using low temperature MBE at T = 250 °C. Note that the device encapsulation by Si MBE was performed by research fellow Dr. G. Scappucci. The results of the electrical characterisation of this device are presented in Section 8.4.

8.4 Electrical characterisation of a 90×70 nm^2 Si:P island

In the following, the electrical characteristics of the 90×70 nm^2 island device at T = 4 K will be discussed. Initially, the DC I-V behaviour of the large P-doped side patches is

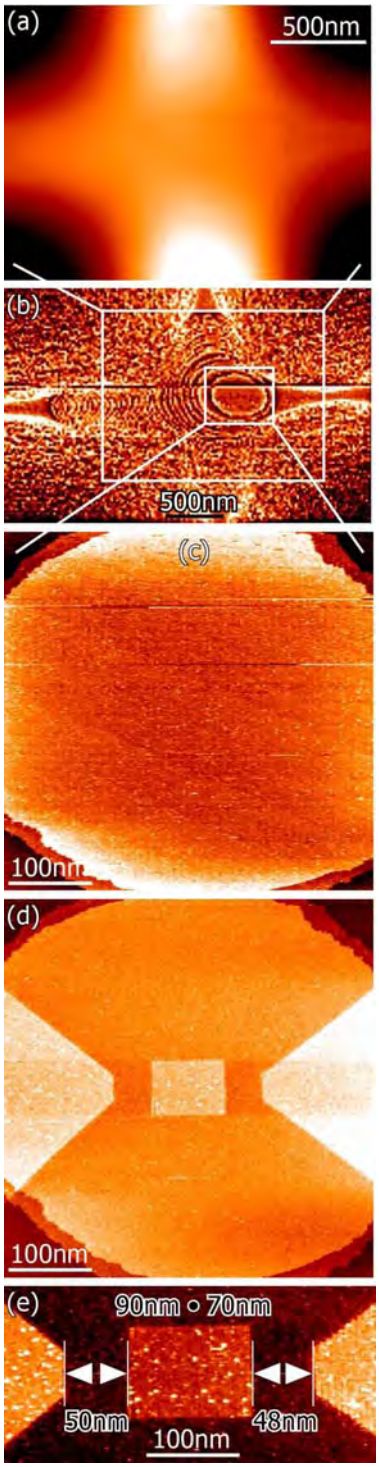

Figure 8.5: STM pattern alignment on a single terrace engineered using EBL-fabricated markers. (a) STM image of the central device between EBL markers of depth ∼25 nm. (b) High-pass filtered STM image of the device region showing the central terrace. (c) Central terrace with a diameter of ∼500 nm. (d) Same terrace after patterning of a 90×70 nm^2 dot including source-drain leads. (e) High resolution image of the dot region with dimensions. Imaging conditions: V ∼ -2.2 V, I ∼ 0.2 nA.

presented, followed by the different lead combinations across the device. Thereafter, the differential conductance ($\frac{dI}{dV}$) across the island is determined and the effect of the backgate is shown. We will elaborate on the nature of transport of this device and conclude this chapter with an outlook of the future research direction of this project.

8.4.1 Two terminal DC I-V characteristics

After a careful cool-down of the device from room temperature to 4 K, using a liquid helium dip station, the DC I-V characteristics for all six combinations is measured using a Keithley 236 source measurement unit (SMU). This allows us to determine if the device has been contacted successfully during the optical lithography process, where four Al metal contacts are aligned to the two large P-doped side patches. Fig. 8.6 shows the I-V characteristics of the two respective P-doped side patches. We note that if the STM pattern alignment and the metal contact alignment worked well, we should get ohmic behaviour. The left contact patch shows a two terminal resistance of 1.5 MΩ originating from a large contact resistance. This is most likely due to insufficient overlap between the leads and the P-doped contact patch which causes a slight non-linearity in the I-V curve around zero bias. The right side patch shows a linear I-V curve with a considerably lower resistance of $R_{2T} = 75\,k\Omega$. Generally the resistance of a P-doped patch is found to have a resistance of $1 - 2\,k\Omega$ determined from four terminal resistance measurements of a P-doped square. This means that most of the resistance of the P-doped contact patches is provided by the contact resistance of the device. Fig. 8.7 depicts the two terminal DC I-V behaviour along and across the 90×70 nm^2 Si:P island for different pin combinations. From this graph, two important conclusions can be drawn.

1. The I-V curves are all identical and highly non-ohmic as expected for a device which has a tunnel junction. These results indicate that the I-V properties are dictated by the STM-patterned device structure rather any transport related to the side patches or the contact resistances.

2. There are two bumps, indicated by black arrows, which are not characteristic for pure, single tunnelling junction behaviour which we have previously seen from measurements of tunnelling junctions in this work. We conclude that the origin of these bumps is related to the presence of the 90×70 nm^2 Si:P island.

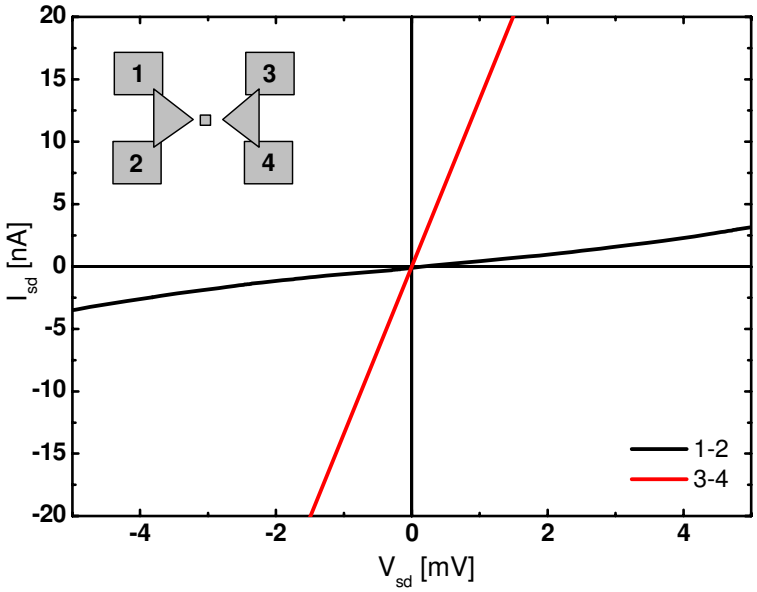

Figure 8.6: Two-terminal DC I-V curve of the large P-doped side patches. Transport through the left side patch (1-2, black trace) shows slightly non-ohmic behaviour around zero bias with a high two terminal resistance of R_{2T} of 1.5 MΩ . The right side patch (3,4 red trace) is perfectly ohmic with R_{2T} of 75 kΩ

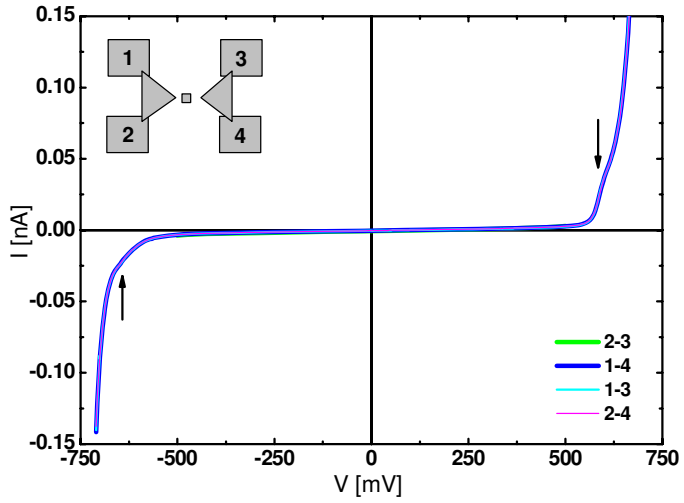

Figure 8.7: Two-terminal DC I-V curve across the 90×70 nm² Si:P island. All four pin combinations across the island reveal identical I-V traces showing that device conductance is governed by the dot system.

The large tunnelling gap around zero bias is likely to stem from either, a Coulomb blockade type phenomenon or simply as a result of large tunnel barriers. In order to test these assumptions, we have performed differential conductance measurements using a more accurate measurement setup than the initial DC measurements with a step size of 4 mV presented here.

8.4.2 Differential conductance behaviour at 4 K

For the differential conductance measurements (dg = $\frac{dI}{dV}$), standard lock-in techniques are used at a constant lock-in frequency of 14 Hz by adding a fixed AC excitation voltage to a DC source-drain voltage. A differential conductance trace is obtained by sweeping the DC component of the source-drain voltage from -875 mV to +875 mV while measuring the differential current at a fixed AC excitation voltage of 480 μV.

Fig. 8.8 shows the differential conductance behaviour of the 90×70 nm^2 Si:P island with leads at T = 4 K. A large conductance gap manifests itself around zero-bias extending almost symmetrically around the origin from +650 $\pm$ 10 mV to -680 $\pm$ 10 mV. Asymmetry around zero-bias is usually explained by the presence of parasitic background polarisation caused by random charges near the junctions as reported by Wilkins et al. [240]. Only a slight asymmetry of the gap is seen reflecting a high level of similarity between the two tunnelling gaps in our device implying a low level of parasitic background charges.

Outside the gap, three peak structures are observed at biases of -720 mV, -830 mV and +780 mV as indicated in Fig. 8.8. These peaks are superimposed on the increasing transconductance through the two $\sim$50 nm wide tunnel junction and the island. Future measurements will target if the rising background is due to breakdown of the $\sim$50 nm wide tunnelling junctions or if further peaks may be observed at higher source-drain voltages. In principle, it it also possible that more peaks are located inside the conductance gap, which lie beyond the measurement resolution of the current setup.

The reproducibility of the conductance was also tested during separate cool-downs of the device. Fig. 8.9 shows the results for two thermal cycles. A high degree of reproducibility is seen for both, the general shape and the position of the peaked structure. The two main peaks have now shifted from initially -830 mV and +780 mV to -800 mV and +770 mV respectively. The smallest peak moved from -720 mV to -710 mV and is only visible on a logarithmic scale.

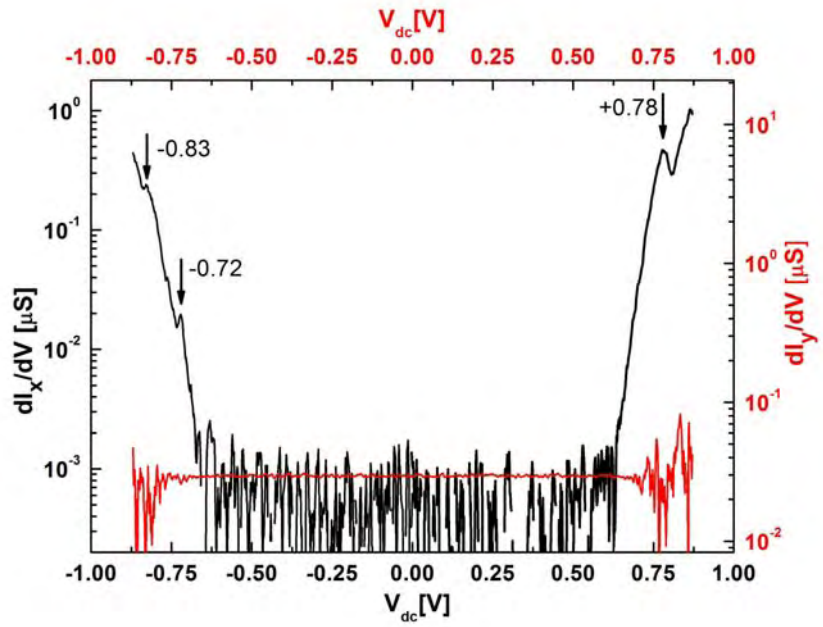

Figure 8.8: Differential conductance of the 90×70 nm^2 Si:P island at 4 K. The x-component of the differential conductance shows three peaks at V_{DC} of -720 mV, -830 mV and +780 mV superimposed on a rising conductance background. The y-component shows an oscillatory behaviour related to the rising conductance behaviour of the x-component.

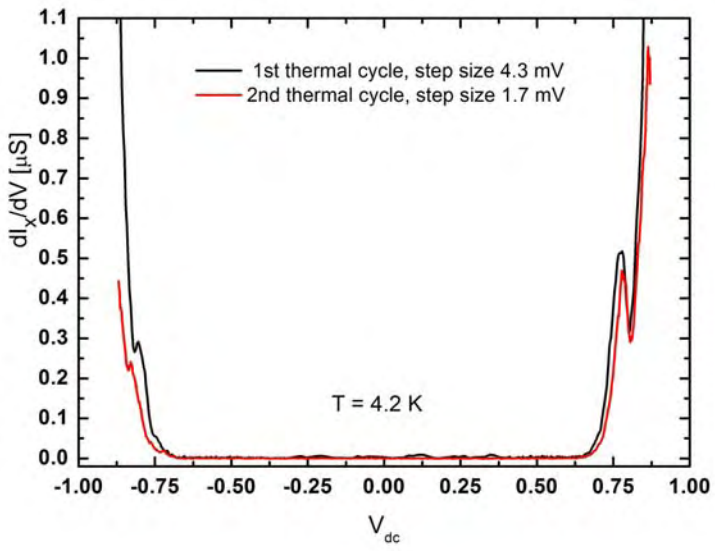

Figure 8.9: Reproducibility after thermal cycling of the 90×70 nm^2 Si:P island at T = 4 K. Comparison of the differential conductance behaviour shows a high level of reproducibility towards thermal cycling.

8.4.3 Interpretation of electrical results

In principle, there are four possible reasons for the observed conductance peaks of the 90×70 nm^2 Si:P island:

1. **Coulomb blockade**
   For small isolated systems such as an island connected to leads, via tunnel junctions, the addition of a single electron may result in a significant change in the electrostatic potential. If the change in the electrostatic potential is larger than the thermal energy kT, the energy spectrum at the Fermi energy becomes quantised leading to the phenomenon of *Coulomb blockade*. A comprehensive review of the underlying physical concepts is given for example by Ferry and Goodnick [98].

   An equivalent circuit of an island with leads system along with the backgate is depicted in Fig. 8.10. Here the tunnelling junctions are replaced by capacitors with capacities C_l and C_r for the left and right junction respectively. The charg-

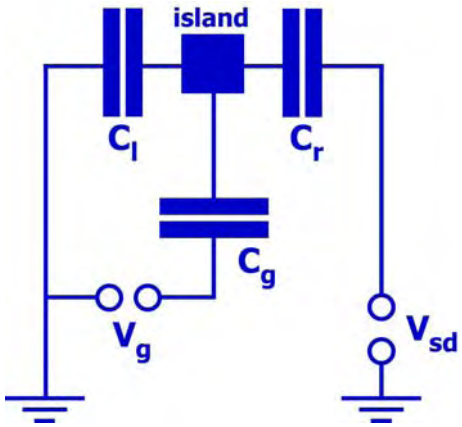

Figure 8.10: Equivalent circuit for a double barrier island system showing the capacitive coupling between source, drain and gate leads.

ing energy of a capacitor is given by

$$E_C = \frac{Q^2}{2C} \tag{8.3}$$

The coupling of the island to the backgate is treated just like another capacitor with C_g and gate voltage V_g. Within this model, the energy of the island system is characterised by:

$$E(Q) = \frac{Q^2}{2C} - V_g \cdot \frac{C_g}{C} Q \tag{8.4}$$

Where the total capacitance is $C = \sum C_i$. The charge on the island may only be varied in discrete steps of the elementary charge leading to the formation of periodic conductance maxima. Individual capacitances can be extracted from the distance between two consecutive conductance maxima as follows:

$$\frac{C_i \cdot \Delta V_i}{C} = E(N+1) - E(N) \Longleftrightarrow \Delta V_i = \frac{e}{C_i} \tag{8.5}$$

Variation of the gate voltage leads to the observation of periodic conductance oscillation whereas variation of the source-drain voltage leads to a staircase type I-V behaviour. We can roughly estimate the capacitances C_l, C_r and C_g of our device using a simple parallel plate capacitor model of area A and plate separation d, where C is given by:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{8.6}$$

$\varepsilon_0 = 8.85 \times 10^{-12}\,\mathrm{Fm}^{-1}$ is the dielectric constant and $\varepsilon_r = 12$ the dielectric constant of silicon. Admittedly, the parallel plate capacitor model does not do proper

justice to the actual device structure since it neglects any effects arising from the finite extension of the plates. As such, this model will only give an order of magnitude approximation. However, a more realistic calculation in 3D is rather difficult and beyond the scope of this work. A next step could entail the use of a simulation program such as FASTCAP to obtain a better estimate of the device capacitances.

The electrical thickness of the δ-doped device layer is correlated to the P redistribution during the Si device encapsulation step using MBE at a growth temperature of T = 250 °C. From SIMS measurements, Oberbeck *et al.* [137] determined the P segregation length to be of order 4 nm limited by the instrumental accuracy. More recently, a careful STM study of the P segregation revealed a lower value of 0.6 nm [181].

Assuming a layer thickness of 0.6 nm i.e. A = 0.6 × 70 nm^2 and d = 50 nm for the lead-island capacitance, we obtain

$$C_{junction} = C_l = C_r = 0.1\ aF \tag{8.7}$$

Using Eq. 8.5, the required source-drain voltage between two conductance maxima becomes,

$$\Delta V_{sd}^{0.6nm} \approx 1.6\ V \tag{8.8}$$

Let's recall, that the two main peaks in the differential conductance plot arise at +780 mV, -830 mV with a small peak at -720 mV which is only visible on a logarithmic scale. We can conclude that a peak separation of 830 mV - 720 mV = 110 mV is much lower than the estimated voltage separation of 1.6 V. Therefore it is likely that the peak at -720 mV does not originate from Coulomb blockade but may be an artefact of the current measurement amplified on the logarithmic graph. Therefore, the estimated voltage separation of 1.6 V should be equivalent to the Coulomb gap, given by the distance of the two conductance peaks at +780 mV and -830 mV. Indeed, the measured Coulomb gap of

$$\Delta V_{gap} = 780\ mV + 830\ mV = 1.61\ V \tag{8.9}$$

is in remarkable agreement with the predicted value from the plate capacitor model. It is the extremely small thickness of the patterned δ-doped layer structure which manifests itself in the very small capacitances responsible for the rather large Coulomb gap.

Estimating the gate capacitance is somewhat easier from a geometrical point of view, since the lateral island dimensions are well defined. The estimate for the backgate capacitance evaluates to

$$C_g = 0.3\ aF \tag{8.10}$$

where A is the island area of 90×70 nm^2 located d = 2 μm away from the backgate. We note that the gate capacitance is of the same order as the lead-island capacitances. From the evaluated capacitance values, we can calculate the charging energy of the device using Eq. 8.3:

$$E_C = \frac{e^2}{2(2C_{junction} + C_g)} = \frac{e^2}{2(2 \cdot 0.1\ aF + 0.3\ aF)} \approx 160\ meV \tag{8.11}$$

The agreement of the conductance gap with the predicted Coulomb gap around zero bias strongly suggest that the observed transport properties of the device is caused by Coulomb blockade behaviour. We briefly elaborate about other possible mechanisms such as resonant tunnelling and quantum dot transport to consolidate our current picture.

2. **Resonant tunnelling through energy levels of the island**
   In a few electron dot system, the electron energy levels become quantised due to their confinement arising from the potential given by the dimensions of the island. Resonant tunnelling due to quantum size effects was first observed by Esaki and coworkers [223] in a narrow, vertical GaAs/$Ga_{1-x}Al_x$As double barrier structure. Assuming a simple 3D infinite wall potential, the energy levels are

$$E_{xyz} = \sum_{i=1}^{3} \frac{h^2}{8md_i^2} \cdot n_i^2 \tag{8.12}$$

   d_i denotes the confinement, m = 0.315 m_e and n_i refers to the energy level in the i^{th} direction. Inserting the values for the Si:P island as d_x = 90 nm, d_y = 70 nm and d_z = 0.6 nm, the ground state energies in every direction evaluate to E_{100} = 148 μeV, E_{010} = 244 μeV and E_{001} = 3 eV.

   From this simple calculation, it can be seen that the confinement in the x-y plane of the 90 × 70 nm^2 sized dot is still quite small, whereas the strong confinement in the z direction gives rise to significant energy level spacing of several eV. Energy quantisation in the z-direction could be probed in a vertical measurement arrangement but for our planar source-island-drain system, only the

energy levels in the x-y plane may be accessed experimentally due to momentum conservation. In the latter derivation, we have ignored the presence of the electrons which are already on the island. Previously, we have estimated the number of electron to be around 11 000. Treating the electron on the island as a two-dimensional Fermi gas, one obtains an expression for the Fermi energy E_F, representing the energy of the highest occupied state to be:

$$E_F = \frac{\pi\hbar^2}{m g_v} \cdot n_s = 648\ meV \tag{8.13}$$

where we have used a valley degeneracy g_v of 2, the electron density n_s of $1.7 \cdot 10^{18}$ m^{-2} and an effective electron mass of m = 0.315 m_e. A general expression for the energy level spacing δE in d dimensions is given by

$$\delta E = \frac{1}{D(E) \cdot L_i^d} \tag{8.14}$$

Using the expression for the density of states in two dimensions, namely

$$D(E) = g_v \frac{m}{\pi\hbar^2} \tag{8.15}$$

and $\aleph_e = L^2 \cdot n_s$, another way of obtaining the energy level spacing is given by comparing equations 8.14 and 8.13:

$$\delta E = \frac{E_F}{\aleph_e} = \frac{648\ meV}{11000} \approx 60\ \mu eV \tag{8.16}$$

The energy-time uncertainty equation based on the inelastic scattering rate τ_φ allows us to estimate the natural energy level broadening, which is of the same order as the level spacing i.e.

$$\Delta E \sim \frac{\hbar}{\Delta\tau_\varphi} \sim 70\ \mu eV \tag{8.17}$$

where we have used a typical inelastic scattering time τ_φ = 1 ps extrapolated from our weak localisation experiments of nano-scale Si:P wires. Additionally, the thermal energy kT $\sim$ 350 μeV at T = 4 K would only enable to clearly resolve energy level spacings above a few meV.

From the above calculations, we can safely conclude that it is not possible to resolve energy level spacings in the dot at 4 K. As expected for such a dot with such a large number of electrons, the 90×70 nm^2 Si:P island essentially behaves like a metal dot embedded in a semiconductor environment.

3. **Resonant tunnelling through energy levels located in the tunnelling barriers**
   Resonant tunnelling does not only occur via energy levels located on the Si:P island itself but may also originate through energy levels located in the tunnelling barriers. Resonant tunnelling though the bound states of a single donor atom within a tunnelling barrier has been observed in GaAs/AlGaAs resonant tunnelling diodes by M. W. Dellow *et al.* [224]. However, differential conductance measurements of our single 48 nm tunnelling junction, discussed in Chapter 7 (Fig. 7.2), show no such resonances. From these previous measurements, we believe that the presence of energy levels in the tunnelling barriers are not a likely cause for the observed resonances in the 90×70 nm^2 dot device.

4. **Quantum dot transport**
   Transport in quantum dots is a direct manifestation of the particle-wave duality which forms the basis of quantum mechanics. The particle property of the electron gives rise to Coulomb blockade oscillations whereas the wave property leads to the formation of energy levels on a dot when the island dimensions are comparable to the electron Fermi wavelength.

   In the presence of discrete energy eigenstates, the energy Eq. 8.4 is modified as follows:

$$E(Q) = \frac{Q^2}{2C} - V_g \cdot \frac{C_g}{C} Q + \sum_i E_i \tag{8.18}$$

   where E_i are the discrete energy levels of the dot. The conductance peaks are now separated by:

$$V_g = \frac{(N + \frac{1}{2})e}{C_g} + E_{N+1} \tag{8.19}$$

   If, the discrete energy level spacing is significant compared to the charging energy E_C, the conductance fluctuations become both irregular in peak spacing and in peak height. If, on the other hand, the charging energy is negligible, the resonant tunnelling picture is obtained as discussed previously.

   By comparing the estimated charging energy of $E_C \approx 160$ meV, determined in the previous section, with the energy level spacing derived from the Fermi energy of $\delta E = 60$ μeV, one can immediately see that quantised electron energy levels do not play a role in our system. Therefore Eq. 8.19 reduces to the familiar expression [Eq. 8.4] for Coulomb blockade type transport.

Energy level broadening of 70 μeV due to the diffusiveness of the Si:P system and thermal energy level broadening at T= 4 K of ∼350 μeV smear out the Fermi energy level separation of δE = 60 μeV. Finally, we are unable to resolve such energies with an AC amplitude of 480 μeV with which the device was measured. Generally, quantum dots are measured at low temperatures such as T = 100 mK, where kT reduces to ∼10 μeV.

We conclude, that the observed transport properties of the device is most likely caused by Coulomb blockade behaviour. The most convincing proof of Coulomb blockade in general is the occurrence of conductance oscillations as a function of an applied gate voltage a fixed source-drain voltage. The variation of both, the source-drain voltage and the gate voltage leads to the formation of Coulomb blockade diamonds. So far, we have not shown the results for varying backgate voltage. The next section is devoted to the measurement of the differential conductance due to the influence of the variation of the backgate of the SOI wafer.

8.4.4 Influence of the backgate

The degenerately doped handle wafer of the SOI wafer was initially implemented to act as an overall gate of the island-lead system. Measurements are performed at T = 4 K. Differential conductance measurements (dg = $\frac{dI}{dV}$) were performed as a function of backgate voltage using standard lock-in techniques at a fixed lock-in frequency of 14 Hz with an AC excitation voltage of 480 μV.

Differential conductance measurements in the range between a source-drain voltage from -875 mV to +875 mV for backgate voltages from -80 V to +80 V in steps of 20 V were taken to observe the occurrence of conductance modulation. Fig. 8.11 summarises the measured differential conductance traces for various backgate voltages. For clarity, the individual graphs are offset from each other by 0.05 μS. We find, that no conductance modulation is observed up to the highest gate voltages of ±80 V and can see no change in position of the peaks at -830 mV and 780 mV respectively. These results demonstrate that the backgate does not work. From our estimate of the gate capacitance $C_g \approx 0.3\ aF$ in the previous section, given by Eq. 8.10, we would expect to have a spacing between two conductance maxima of:

$$\Delta V_g = \frac{e}{C_g} \approx 0.5\ V \tag{8.20}$$

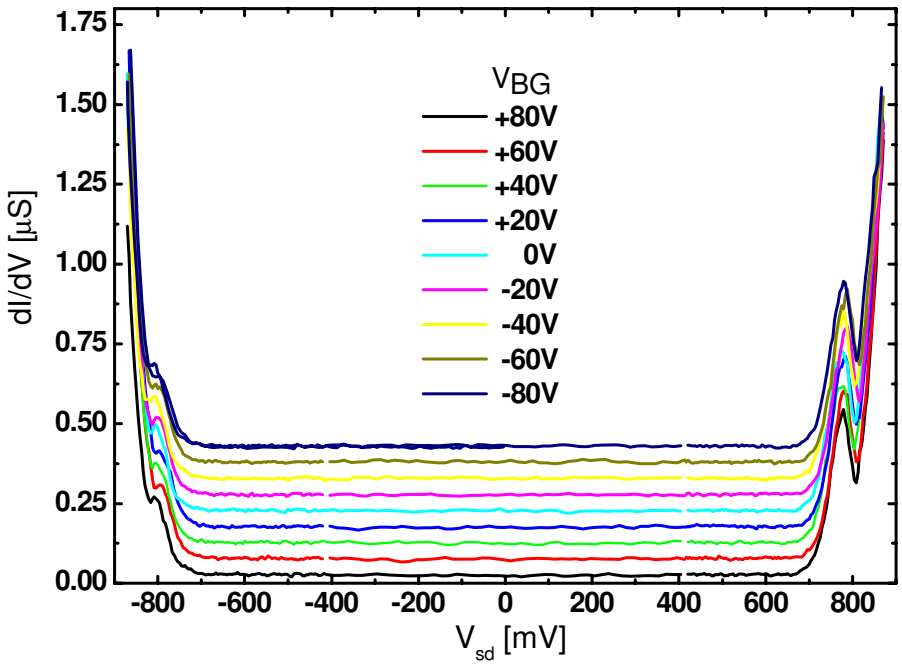

Figure 8.11: Differential conductance for various backgate voltages. Differential conductance measurements ($\frac{dI}{dV}$) at 4 K show no influence or gating effects of the backgate for voltages ranging from -80 V to +80 V. Note that individual traces are shifted by 0.05 μS for clarity.

Even if the estimated capacitance is inaccurate by one order of magnitude, we would expect to see quite a few conductance oscillations between $\pm$80 V. We also determine the change in conductance due to the backgate voltage at a fixed source-drain bias of 420 mV – a position towards the end of the observed conductance gap. Measurements for a backgate voltage range of $\pm$30 V shown in Fig. 8.12 do not show any conductance modulation but instead exhibit a flat line demonstrating the noise level. We have also tried to modulate the conductance at the position of the observed conductance peaks by manually varying the backgate. Again, no change in conductance is found. Therefore, we can report that for this SOI substrate, no modulation of the potential in the device is present using the current experimental setup.

A possible explanation for the absence of any modulation may be that the trap density at the Si/SiO_2 interface is sufficiently large to screen the backgate voltage. Another possibility is that charge motion in the device layer itself accommodates for the applied backgate voltage. A third possibility, from discussing with the SOI wafer supplier, Ultrasil Corporation (California, USA), is that significant As dopant diffusion from the degenerately doped As handle wafer occurs through the oxide layer into the

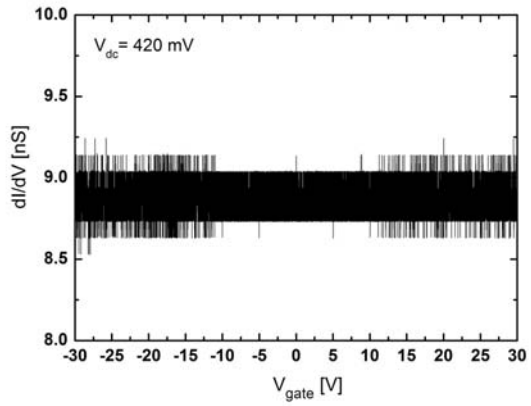

Figure 8.12: Differential conductance at fixed source-drain voltage. Differential conductance measurements ($\frac{dI}{dV}$) at a fixed source-drain voltage of 417 mV. No gate modulation is observed for voltages ranging from -30 V to +30 V in agreement with the results from Fig. 8.11.

Si device layer. This diffusion may arise during the high temperature (T $\approx$ 1000 °C) wafer bonding process. The As dopants may then screen the voltages applied by the backgate. It is also possible that the device, located 2 μm away from the SiO_2 layer, is too far away in order for the backgate to have an effect. At present, we conclude that the SOI wafer used for this device is not suitable for backgating.

In summary, we have established that the large conductance gap seen in our device is due to Coulomb blockade behaviour. Experiments to consolidate this interpretation using backgated conductance measurements turned out to be unsuccessful, most likely due to dopant diffusion within the SOI wafer material. Currently, the development of a functional backgate is being actively pursued in our research group.

8.5 Outlook

The integrity of Si:P islands down to a size of 9×9 nm^2 was demonstrated, showing that the island was found to be preserved throughout all the crucial UHV fabrication steps. With the help of Si surface engineering using registration markers, created by electron beam lithography, the critical device features can be patterned on a monoatomic terrace of circular shape with diameters of ∼500 nm.

The electrical properties of a 90×70 nm^2 large Si:P source-island-drain device was presented at T = 4 K. Preliminary electrical results show that transport through the

source-island-drain device is likely to be governed by Coulomb blockade behaviour. From the width of the conductance gap around zero bias, the electrical thickness of the patterned δ-doped P layer structure is found to be in excellent agreement with the measured layer thickness of 0.6 nm extracted from STM studies of P segregation.

To confirm if conductance oscillation arise from the Coulomb blockade type behaviour, backgated measurements were performed. Unfortunately, no conductance modulation was found for a large backgate voltage range from -80 V to +80 V. From a simple estimate of the gate capacitance, conductance oscillations are expected in this device to be modulated with a gate voltage change of order 1 V. Future work to determine the device capacitances using FASTCAP simulations will provide more accurate estimates. Future temperate-dependent conductance measurements over a larger source-drain voltage range will help to determine if Coulomb blockade behaviour is responsible for the large conductance gap. Since device capacitances are temperature-independent (as long as the substrate is insulating), the conductance gap due to Coulomb blockade is also expected to be fairly temperature independent apart from thermal smearing.

We conclude that the *current* SOI wafer is not a suitable backgate implementation. Current research efforts in our group are aimed at developing a reliable gating method. This involves testing and characterising more appropriate SOI wafer materials from other suppliers, where trap densities and dopant diffusion from the handle wafer is minimised. Another way forward is to move the STM-patterned device layer closer to the backgate from currently 2 μm to a few hundred nanometres. In the long term, the group is pursuing the goal of fabricating and electrical characterising single electron transistor devices. To achieve this, three top gates have to be aligned, one for each junction and one for the island, using electron beam lithography. The longer term goal also encompasses shrinking down the Si:P island to the atomic level to form a gated array. The construction of such an array with near atomic precision may prove that an STM-based method represents a suitable technology for the fabrication of a solid state quantum computer of the Kane type architecture [33].

Chapter 9

Conclusion and future work

We have developed a novel, UHV compatible STM device fabrication process for the realisation of nano- and atomic-scale devices in silicon [30], [31], [172], [136]. By combining a custom-designed STM-SEM/MBE system with the use of etched registration markers in the silicon substrate, developed in this thesis, we are able to align external metal contacts to STM-patterned Si:P devices. In particular, we can position the STM-patterned device with respect to the registration markers under SEM control. We then evaporate four Al metal contacts outside the UHV environment, thereby making ohmic contact to the buried device using the markers for alignment. Multiple devices can be patterned with the STM on the same chip allowing us to compare different device structures and measure their electrical characteristics simultaneously. We employ the use of unpatterned control devices and four terminal device measurements to unequivocally determine if the observed conductance truly arises from the buried P dopants of the device. We successfully demonstrated the viability of this novel fabrication strategy on the basis of eight functional, STM-patterned devices presented here and more devices that we have not had time to characterise electrically.

In Chapter 4, we outlined the development of a UHV compatible marker process [31] that allowed the relocation of STM-patterned structures. In this process, we use conventional optical lithography to pattern a SiO_2 layer on a large 1×1 cm^2 Si(100) surface. This SiO_2 layer is then etched to act as a mask for subsequent silicon etching, thereby protecting the silicon surface from contact with the organic resist and metal contamination. Using SiO_2 as a mask, we can wet-chemically etch registration markers to a depth of 350 nm and sizes down to 1 μm into the silicon surface. The SiO_2 mask in combination with a rigourous wet-chemical cleaning procedures prevents the silicon surface from contamination of organic and metallic residues, the presence of which

is known to adversely affect the surface quality in UHV. The thermal stability of the registration markers to temperatures above 1250 °C enabled us to use the standard silicon surface preparation anneals to temperatures up to 1200 °C in UHV to prepare an atomically flat surface. The registration markers were found to leave the surface structure in the device area unaltered allowing us to obtain atomic-resolution STM imaging on 1×1 cm^2 samples exhibiting low defect densities and atomically clean Si(100) 2×1 reconstructed surfaces. By monitoring the position of the STM tip with respect to the registration markers using the SEM, we were able to align the STM-patterned P dopant region to the markers with an accuracy of order 100 nm. Devices are created using STM-based hydrogen resist lithography, selective adsorption of phosphine onto the lithographic pattern, followed by thermal P incorporation from the phosphine molecule into the top layer of the Si(100) surface. Device encapsulation using low temperature Si MBE effectively moves the buried Si:P way from the surface states, defects and dislocations, thereby ensuring complete electrical activation of the P dopants.

Electrical contact to the devices was achieved in another optical lithography step outside UHV using four Al contacts aligned to the registration markers with individual device alignment as low as $\sim$100 nm. Initially, we demonstrated the success of the process developed by fabricating a 4×4 μm^2 large P-doped square device. Comparing the I-V characteristics between an unpatterned control device and this device, we found insulating behaviour between the contact electrodes of the control device, but ohmic behaviour with resistances of order 1 kΩ for the P-doped square device.

Hall measurements, performed on this 4×4 μm^2 large P-doped square device, presented in Chapter 5, gave a carrier density of $1.79 \cdot 10^{14}$ cm^{-2}, corresponding to 100 % electrical activation of the buried dopants in agreement with previous studies of Si:P δ-doped devices [138]. This proves that all P dopant are located on substitutional sites in the silicon crystal and that electrical dopant activation is not affected by the STM lithography process. Magnetotransport measurements of this device showed mobilities of 21 cm^2/Vs and an electron phase coherence l_φ of 39 nm at 4 K comparable to other Si:P δ-doped layers fabricated in our group highlighting that STM patterning did not adversely affect the device performance [136]. The effect of further confinement of conduction electrons by patterning a 90 nm wide P-doped wire using STM lithography was examined. Magnetotransport measurements performed at liquid helium temperatures showed a crossover from 2D to 1D behaviour at low temperatures,

where the electron phase coherence length (∼135 nm) is larger than the wire width (90 nm). This crossover allowed us to determine the width of the wire from electrical measurements which was found to be in excellent agreement with the lithographic width of 90 nm patterned by STM [30]. These results reinforce the enormous potential of STMs for device fabrication down to the atomic level.

In Chapter 6, we investigated what happens to the conductivity as we reduce the wire width below 10 nm. STM studies of the buried dopants using CITS confirmed that the structural integrity of the wires remain intact. However, for the narrow wire structure with a width of ∼7 nm, it became increasingly difficult to distinguish the electrical signal from the buried dopants from the topographic signal. We independently confirmed the structural wire integrity by measuring the I-V behaviour of such highly doped, planar wire devices with widths from 90 nm to 8 nm, showing ohmic behaviour at T = 4 K with very low resistivities as low as $1 \cdot 10^{-8}$ Ωcm compared to other P-doped silicon nanowires reported in the literature. The importance of this result is, that by encapsulating planar, STM-patterned Si:P devices, it is possible to avoid the effects of surface depletion which is inherent to many other nanowire fabrication techniques.

A detailed investigation of the conduction properties of a 27 nm wide wire over a temperature range from 200 mK to 65 K was undertaken. We identified three different conduction regimes, dictated by the relation between the wire width w, the temperature-dependent electron phase coherence length l_φ and the localisation length ξ. We found electron-phonon scattering to be the governing dephasing mechanism at temperatures from 4 K to 65 K. Below 4 K, l_φ = 24 nm was found to be comparable to w = 27 nm, so that the wire conductance crossed from the 2D regime into the 1D regime, where the magnetoconductance of the wire could be well described by 1D weak localisation theory. In this intermediate regime, electron dephasing could be explained by both, inelastic scattering processes with small energy transfers known as Nyquist dephasing and inelastic scattering due to electron-electron collisions with large energy transfers. These results are in agreement with studies of other disordered 1D systems, such as 1D Si MOSFETs by Pooke *et al.* [195] and 1D wires$GaAs/Al_xGa_{1-x}$ reported by Choi *et al.* [203]. The total conduction correction measured in this regime was fitted to conductance corrections due to both, 1D weak localisation and 1D electron-electron interaction effects. Our results lead to an extracted value of the Coulomb screening factor α_{ee} = 0.13 in agreement with an analysis

of etched 1D Si δ-doped GaAs wire arrays with widths of $\sim$50 nm reported by Khavin *et al.* [196]. At temperatures below 450 mK, the electron phase coherence length l_φ of 50 nm became comparable to the localisation length ξ of 100 nm, suggesting the onset of strong localisation. We observed two pieces of evidence for such a transition. First, we observed an apparent saturation of l_φ at 300 mK also observed by Gershenson *et al.* [214]. Secondly, we found that from 200 mK to 2 K, the wire conductance could also be fitted by a 1D variable range hopping model. In this temperature range, we found that the same data could be fit by both, a combination of 1D weak localisation and 1D electron-electron interaction effects and with a 1D variable range hopping model. Since we are in the crossover regime from weak to strong localisation, the fact that the data could be fit by both theories is perhaps not surprising. Future low temperature measurements of the 8 nm wide wire will allow us to enter the strong localisation regime and study the conduction limit at the atomic scale.

The Bohr radius in our system of $\sim$3 nm allows the fabrication of planar tunnel junctions or nanogaps with a gap size of order several Bohr radii corresponding to a tunnelling gap of $\sim$10 nm. In Chapter 7, we studied the effect of tunnelling between P-doped leads with gap sizes of 48 nm and 17 nm respectively. Non-linear I-V behaviour was observed at T = 4 K due to quantum tunnelling between the P-doped leads, demonstrating the first realisation of tunnel junctions in this system. A careful study of the 48 nm tunnelling gap up to biases of $\pm$4 mV showed a high level of reproducibility towards thermal cycling. Conductance modulation was achieved by employing the method of substrate bias cooling. Here, the conductance was found to increase fourfold when cooling the device with a bias of +2.5 V whereas cooling with a bias of -4 V resulted in a threefold decrease in conductance compared to cooling at zero bias. The ability to modulate the conductance bodes well for the future integration of gating techniques. Differential conductance measurement demonstrated clean, low noise traces. The absence of resonances or random telegraph signals indicated no active charge traps in the vicinity of the tunnel junction thus providing a good environment for the study of more sophisticated devices designed for the observation of effects such as resonant tunnelling or Coulomb blockade behaviour.

A Coulomb blockade type device architecture was pursued in Chapter 8, where we showed the formation of STM patterned Si:P islands of various size between P-doped leads. Initially we showed that a source-island-drain structure with a P-doped island of 9×9 nm^2 in size remained intact during each UHV fabrication step. We em-

ployed the use of EBL makers to improve the alignment of STM-patterned devices to the registration markers. We observed that the STM itself allowed the fabrication of Si:P islands between source-drain leads with internal alignment precision of $\sim$1 nm. Preliminary electrical characterisation of a 70×90 nm^2 Si:P island device on a SOI substrate at T = 4 K showed that the occurrence of a large conductance gap of $\sim$1.6 V was likely to be due to Coulomb blockade behaviour. Whereas conductance oscillations using the SOI backgate were not observed due to the unsuitability of the SOI wafer material, future studies will target the temperature dependence of the device conductance to further establish if the device characteristics were indeed governed by Coulomb blockade behaviour.

The enormous potential of the fabrication strategy developed in this thesis lies in its capability to access device structures of atomic dimensions beyond any other existing fabrication technique to date. Individual device structures can be monitored with atomic precision as they are made allowing, for the first time, to correlate actual dopant distributions with their electrical characteristics. Our technique is not restricted to the use of phosphine gas but may be applied to other adsorbates which are compatible with the hydrogen resist technology. This opens up the possibility to fabricate atomic-scale devices using other gaseous dopant sources and may also lend itself for the fabrication of hybrid organic devices in silicon.

9.1 Future work

9.1.1 Planar nanowires

Future work on the subject of P-doped nanowires contains the fabrication and measurement of narrower wires to further investigate the conduction limit of our wires towards the atomic scale. In particular, the behaviour of both narrower and lower doped wires will give access to the study of strong localisation which is the likely mechanism that will limit conduction in these wires. In this context but also for the pursuit of tunnel junctions and Si:P islands devices, it is interesting to implement a proper gating strategy into the device fabrication process.

9.1.2 Implementation of a gating strategy

Current research efforts in our group are under way to target different gating architectures. Possible candidates are:

- **Back gate:** A blanket back gating structure was already investigated in this thesis using SOI substrates. However gating was not achieved most likely due to significant As dopant diffusion from the degenerately doped handle wafer through the SiO_2 layer into the device layer. Future work involves testing and characterising more appropriate SOI wafer materials from different suppliers, where interface trap densities and dopant diffusion from the handle wafer are minimised.

- **Top gate:** Another possibility is the development of a top gate which necessitates the development of a low temperature insulating surface barrier. A low temperature process is necessary to prevent thermally activated P dopant diffusion. Our group currently investigates the formation of a thin, in-situ SiO_2 layer in UHV using a recently installed oxygen plasma source. Initially a blanket top gate can be realised with such a barrier but intermediate research goals encompass the alignment of EBL-defined gates on top of the STM-patterned device with the use of EBL-defined registration markers such as those we have used for the alignment of the Si:P source-island-drain devices in Chapter 8.

- **In-plane gate:** STM-patterned in-plane gates provide a way to achieve high alignment accuracy between gates and device. They can be patterned in a multi step lithography process in the same plane as the device structure. Such an approach may currently be the only way to achieve gate alignment accuracy below the 10 nm scale. EBL lithography can be used to contact both the device and the gates from the surface. Demonstration of capacitive coupling between the gate and device over a sufficiently large gating range is crucial for in-plane gating to be successful.

9.1.3 Atomic-scale devices

The true potential of this fabrication strategy is the possibility to create semiconducting devices at the single atom level. Incorporation of electron beam lithography for the fabrication of registration markers and for alignment of surface contact structures will

allow the future realisation of more sophisticated devices such as single electron transistors, quantum dots or solid state quantum computers. Fabrication of such devices entails EBL-aligned top gates for control of electron transfer between P dopants. By reducing the size of the Si:P island from the nanometre scale towards the single atom level, it is possible to leave the regime dominated by Coulomb blockade behaviour and enter the regime where energy level quantisation effects become important.

The fabrication of ordered dopant arrays with currently $\sim$40 P dopants per dot to study the effects of controlled doping on the turn-on characteristics of transistors is already under way in our group. The long term goal of the research group's activity is the STM-based fabrication of the ultimate atomic scale device – a solid state quantum computer of the Kane type architecture [33]. Such a device consists of a single P dopant array with gates on top and in between the individual P dopants separated from each other by $\sim$20 nm. It is likely that such a high level of alignment accuracy between individual P dopants and gates can only be realised using a multi-step STM patterning approach for both, the dopant array and the respective gating structure.

Finally, another exciting class of devices can be pursued with this fabrication method. Since both, STM-patterning and molecular beam epitaxy allow atomic precision, multi-level STM patterning followed by successive atomic layer MBE growth will enable, for the first time, to allow the formation and characterisation of 3D devices with truly atomic precision.

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Appendix A

Units and prefixes

A.1 SI units

The International System of Units (Système International d'Unités, SI) is based on a choice of seven well-defined units which by convention are regarded as dimensionally independent: the metre, the kilogram, the second, the ampere, the kelvin, the mole and the candela. These SI units are called *base units* (Tab. A.1), and they provide a reference in terms of which all other units can be defined. Details of the definition of the SI base units can be found in the 7^{th} edition of the International System of Units (including addenda and corrigenda) [241, 242], along with details on SI derived units, non-SI units and SI prefixes (see below).

A second class of SI units is that of *derived units*. These are units that are formed as products of powers of the base units according to the algebraic relations linking the quantities concerned. The names and symbols of some derived units may be replaced by special names and symbols which can themselves be used to form expressions and symbols for other derived units (see e.g. Tab. A.2).

Base quantity	Name	Symbol
Length	meter	m
Mass	kilogram	kg
Time	second	s
Electric current	ampere	A
Thermodynamic temperature	kelvin	K
Amount of substance	mole	mol
Luminous intensity	candela	cd

Table A.1: SI base units. The SI is founded on seven SI base units for seven base quantities assumed to be mutually independent.

Derived quantity	Name	Symbol	In other SI units
Frequency	hertz	Hz	s^{-1}
Force	newton	N	$m{\cdot}kg/s^2$
Pressure, stress	pascal	Pa	N/m^2
Energy, work	joule	J	$N{\cdot}m$
Power, radiant flux	watt	W	J/s
Electric charge	coulomb	C	$A{\cdot}s$
Electric potential difference	volt	V	W/A
Capacitance	farad	F	C/V
Electric resistance	ohm	Ω	V/A
Electric conductance	siemens	S	A/V
Magnetic flux	weber	Wb	$V{\cdot}s$
Magnetic flux density	tesla	T	Wb/m^2
Inductance	henry	H	Wb/A
Celsius temperature	degree Celsius	°C	K
Plane angle	radian	rad	1

Table A.2: Some SI derived units. For ease of understanding and convenience, some SI derived units have been given special names and symbols. The numerical value of a Celsius temperature t, in relation to a thermodynamic temperature T, is given by: $t/°C = T/K - 273.15$.

Each physical quantity has only one SI unit, even if this unit can be expressed in different forms. The inverse, however, is not true; in some cases the same SI unit can be used to express the values of several different quantities. The base units together with the derived units and other SI units form a coherent set of units with the effect that unit conversions are not required when inserting particular values for quantities in quantity equations.

A.2 Non-SI units

Some non-SI units are widely used in various literature, while others, such as the units of time, are very commonly used in every day life. Hence a range of such non-SI units is accepted for use with the International System. SI units are always to be preferred to non-SI units. It is desirable to avoid combining non-SI units with units of the SI – in particular the combination of such units with SI units to form compound units. Tab. A.3 lists some commonly used non-SI units.

Name	Symbol	Value in SI units
minute	min	$1\,\mathrm{min} = 60\,\mathrm{s}$
hour	h	$1\,\mathrm{h} = 60\,\mathrm{min} = 3600\,\mathrm{s}$
day	d	$1\,\mathrm{d} = 24\,\mathrm{h} = 86400\,\mathrm{s}$
degree	$^\mathrm{o}$	$1\,^\mathrm{o} = (\pi/180)\,\mathrm{rad}$
litre	l,L	$1\,\mathrm{l} = 1\,\mathrm{dm}^3 = 10^{-3}\,\mathrm{m}^3$
tonne	t	$1\,\mathrm{t} = 10^3\,\mathrm{kg}$
electronvolt	eV	$1\,\mathrm{eV} = 1.602\ldots\times 10^{-19}\,\mathrm{J}$
unified atomic mass unit	u	$1\,\mathrm{u} = 1.660\ldots\times 10^{-27}\,\mathrm{kg}$
bar	bar	$1\,\mathrm{bar} = 1000\,\mathrm{hPa} = 10^5\,\mathrm{Pa}$
ångström	Å	$1\,\mathrm{Å} = 0.1\,\mathrm{nm} = 10^{-10}\,\mathrm{m}$
torr	Torr	$1\,\mathrm{Torr} = (101325/760)\,\mathrm{Pa}$
neper	Np	$1\,\mathrm{Np} = 1$
bel	B	$1\,\mathrm{B} = \frac{1}{2}\ln 10\,\mathrm{Np}$

Table A.3: Some non-SI units. These units are accepted for use with the International System. The use of "torr", however, is not encouraged. The neper and the bel are used to express values of logarithmic quantities (e.g. field level, power level, sound pressure level and attenuation) in terms of the natural logarithm and logarithms to base ten, respectively. The neper is coherent with the SI, but not yet adopted as an SI unit. The submultiple decibel, dB, is commonly used.

A.3 SI prefixes

A series of prefixes (Tab. A.4) was adopted to form the decimal multiples and submultiples of SI units by using the SI units combined with these *SI prefixes*. As an exception, the multiples and submultiples of the kilogram are formed by attaching prefix names to the unit name "gram", and prefix symbols to the unit symbol "g". The SI prefixes refer strictly to powers of 10. They should not be used to indicate powers of 2 (for example, one kilobit represents 1000 bits and not 1024 bits).

Factor	Name	Symbol	Factor	Name	Symbol
10^{24}	yotta	Y	10^{-1}	deci	d
10^{21}	zetta	Z	10^{-2}	centi	c
10^{18}	exa	E	10^{-3}	milli	m
10^{15}	peta	P	10^{-6}	micro	μ
10^{12}	tera	T	10^{-9}	nano	n
10^{9}	giga	G	10^{-12}	pico	p
10^{6}	mega	M	10^{-15}	femto	f
10^{3}	kilo	k	10^{-18}	atto	a
10^{2}	hecto	h	10^{-21}	zepto	z
10^{1}	deca	da	10^{-24}	yocto	y

Table A.4: SI Prefixes. These prefixes and prefix symbols define some of the decimal multiples and submultiples of SI units.

Appendix B

Fundamental and material properties of aluminium

B.1 Fundamental constants

Tab. B.1 lists a relevant selection of the current set of self-consistent values of the basic constants recommended by the Committee on Data for Science and Technology (CODATA). The values for these and more constants are listed in Ref. 243, along with methods of obtaining them.

B.2 Material properties of aluminium

Some material properties of aluminium (Al), which we use as our contact material are given in Tab. B.2.

Quantity	Symbol	Value	Unit
Speed of light in vacuum	c,c_0	299792458	m/s
Magnetic constant	μ_0	$4\pi \times 10^{-7}$	$\mathrm{N/A^2}$
Electric constant $1/\mu_0 c^2$	ε_0	$8.854187817\ldots \times 10^{-12}$	F/m
Planck constant	h	$6.62606876(52) \times 10^{-34}$	Js
$h/2\pi$	$\hbar$	$1.054571596(82) \times 10^{-34}$	Js
Elementary charge	e	$1.602176462(63) \times 10^{-19}$	C
Conductance quantum $2e^2/h$	G_0	$7.748091696(28) \times 10^{-5}$	S
Von Klitzing constant h/e^2	R_K	25812.807572(95)	Ω
Electron mass	m_e	$9.10938188(72) \times 10^{-31}$	kg
Avogadro constant	N_A,L	$6.02214199(47) \times 10^{23}$	$\mathrm{mol^{-1}}$
Boltzmann constant	k	$1.3806503(24) \times 10^{-23}$	J/K

Table B.1: A selection of fundamental constants. The values of the constants provided in this table are recommended for international use by CODATA (1998).

Quantity	Symbol	Value	Unit
Relative atomic mass	M	26.98	u
Density	ϱ	2702	$\mathrm{kg/m^3}$
Melting temperature	T_m	933.47	K
Boiling temperature	T_b	2792	K
Resistivity at RT	ρ	2.65×10^{-8}	Ωm
Critical temperature	T_c	1.175	K
Critical magnetic field	B_c	0.011	T
Work function	Φ_m	4.20	eV
Fermi energy	E_F	11.65	eV
Relative effective mass	m^*/m_e	~ 0.97	

Table B.2: Material properties of bulk Al. [244–247]