Single-Phase Grid-Connected Battery-Supercapacitor Hybrid Energy Storage System

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Single-Phase Grid-Connected Battery-Supercapacitor Hybrid Energy Storage System

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Battery technology is popular in distributed energy storage systems (ESSs) due to its ease of implementation. However, batteries have limited power capabilities, and the lifetime of batteries deteriorates due to high and fluctuating battery currents.

Battery-supercapacitor hybrid energy storage systems (HESSs) become a promising way of increasing the battery lifetime and system power capability. The HESSs can be divided into two groups, DC link based and direct AC line integrated HESSs. The direct AC line integrated HESSs have been proposed to eliminate multiple power processing stages associated with the DC link based HESSs.

The objective of this research is to develop a direct grid-connected battery-supercapacitor HESS able to allocate fast power fluctuations to the supercapacitor while maintaining the state of charge of the ESSs within a safe operating region. Since the lifetime of ESSs deteriorates with ripple current components, ways of reducing the current ripple components of the ESSs are studied.

In this thesis, a boost inverter based battery-supercapacitor HESS is proposed. A supercapacitor voltage controller and a filter based method is used to allocate the fast power fluctuations to the supercapacitor. Then, a supercapacitor energy controller (SCEC) based power allocation method facilitating the HESS dynamic analysis and precise supercapacitor sizing is proposed. Later, a sliding mode controlled HESS with a SCEC based power allocation method is proposed to achieve better output voltage reference following performance.

To mitigate the second-order harmonic current components in the boost inverter based HESSs, a rule-based control method and a novel current feedback method are proposed. Both methods achieve a significant ripple current reduction without being affected by the output capacitor tolerances while the latter method mitigates the current ripple even during the output power transients.

The proposed HESS is the first experimentally verified single-phase direct grid-connected HESS able to reduce the switching frequency and the second-order harmonic current ripples.

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Abstract

Battery based ESSs are popular among distributed network ESSs due to ease of implementation and geographical independence as compared to other energy storage technologies. However,due to its chemical properties batteries have limited power capabilities compared to other energy storage technologies such as supercapacitors. Hence, a large number of batteries may need to be connected in parallel in order to meet the required power capabilities. Furthermore, the lifetime of the battery deteriorates due to high battery currents and battery current fluctuations as explained in Chapter 1.

Battery-supercapacitor hybrid energy storage systems (HESS) become a promising way of battery lifetime extension since they can effectively minimize the battery current variations. HESSs combine individual advantages of both the battery and the supercapacitor and create a single ESS with both higher power and energy capabilities. The HESSs can be divided into two basic groups, namely, DC link based and direct AC line integrated HESSs. The direct AC line integrated ESSs have been proposed in literature as a way of eliminating the multiple power processing stages associated with the DC link based ESSs.

The objective of this research is to develop a single phase direct grid integrated battery-supercapacitor HESS which is able to allocate the fast power fluctuations to the supercapacitor. Furthermore, the battery and the supercapacitor state of charge (SOC) have to be maintained within a safe operating region. Since the lifetime of the DC ESSs deteriorates due to the ripple current components as explained in Chapter 1, it is vital to identify ways of reducing the switching frequency ripple components and the second-order harmonic components of both the battery and the supercapacitor currents.

A boost inverter based battery-supercapacitor HESS is proposed in this thesis. The boost inverter provides both boosting and inversion functions in a single power processing stage allowing the direct grid integration of low voltage DC sources. A supercapacitor voltage controller (SCVC) and a filter based power allocation method is used to allocate the fast power fluctuations and the second-order harmonic ripple component to the supercapacitor. An interleaved operation for the boost inverter is proposed to reduce the switching frequency ripple components of the DC source currents.

Then, a supercapacitor energy controller (SCEC) and a filter based power allocation method is proposed to circumvent the issues associated with the SCVC and filter based power allocation method. The proposed method enables the dynamic analysis of the HESS, precise sizing of the DC sources and selection of the power allocation parameters.

A novel fixed frequency sliding mode (SM) controller is proposed for the boost inverter based HESS. The SM controller is able to achieve better output capacitor voltage reference

tracking and reduce the implementation complexity of the HESS controller. A SCEC based power allocation method, a power allocation parameter selection method, and an energy storage element sizing method are proposed for the SM controlled HESS.

Then, ways of mitigating the second-order harmonic ripple component in the HESS are studied. With the conventional HESS operation, the ripple current component is allocated to the supercapacitor which deteriorates its lifetime. A rule-based control method is proposed to overcome the limitations associated with the existing waveform control ripple reduction method. The proposed method is able to achieve a significant ripple current reduction without being affected by the output capacitor tolerances and inductor ESR values. However, the method requires a specific time period to reduce the ripple component once a change in the active or reactive power reference occurs. Then, a novel current feedback ripple reduction method is proposed, and the method achieves superior performance compared to the existing ripple reduction methods. The current feedback method is able to reduce the second-order harmonic ripple current even during the output power transient conditions and hence it is suitable for the HESS operation.

All the proposed systems are verified experimentally to illustrate the applicability of the proposed HESS in grid ESS applications. The proposed HESS is the first experimentally verified single phase direct grid connected HESS which is able to reduce both the switching frequency ripple components and also the second-order harmonic ripple components in both the battery and the supercapacitor currents. Furthermore, the proposed SCEC based power allocation strategy enables the accurate HESS power allocation parameter selection and precise energy storage element sizing.

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Nomenclature

AC	Alternating current
DC	Direct current
DL	Double loop
ESR	Equivalent series resistance
ESS	Energy storage system
FFT	Fast Fourier transform
HESS	Hybrid energy storage system
$LiFePO_4$	Lithium iron Phosphate
OCV	Open circuit voltage
P&O	Perturb and observe
PCC	Point of common coupling
PI	Proportional integral
PLL	Phase lock loop
PR	Proportional resonant
PV	Photovoltaic
PWM	Pulse width modulation
QSG	Quadrature signal generator
SCEC	Supercapacitor energy controller
SCVC	Supercapacitor voltage controller
SM	Sliding mode

SOC	State of charge
SOGI	Second-order generalized integrator

List of Variables and List of Greek Symbols

ω	Frequency of the inverter output voltage in rads^{-1}
δ	Phase angle of the inverter output voltage in rad
η	Efficiency of the HESS
ω_{HPF}	Cut-off frequency of the high-pass filter used for HESS power allocation in rads^{-1}
$\nabla P_{batt,limit}$	Predefined maximum allowable gradient value for the battery power profile in W/s
C_1	Left hand side output capacitor in μF
C_2	Right hand side output capacitor in μF
C_{batt}	Energy capacity of the battery in Ah
C_{sc}	Capacitance of the supercapacitor in μF
d_1	Duty cycle time average value of the switch $Sw_{1,B}$
d_{batt1}	Duty cycle time average value of the switch $Sw_{batt1,B}$
d_{sc1}	Duty cycle time average value of the switch $Sw_{sc1,B}$
dE_{batt}	Change in the stored energy in the battery in J
dE_{sc}	Change in the stored energy in the supercapacitor in J
E_o	Open circuit voltage of the battery in V
E_{sc}	Energy stored in the supercapacitor in J
$E_{sc,init}$	Initial stored energy of the supercapacitor in J

$E_{sc,max}$	Maximum stored energy of the supercapacitor in J
$E_{sc,min}$	Minimum stored energy of the supercapacitor in J
$E_{sc,ref}$	Reference energy level for the supercapacitorin J
$E_{sc,u}$	Utilized energy of the supercapacitor in J
f	Grid voltage frequency in Hz
f_{sw}	Switching frequency in kHz
i_{batt}	Battery current in A
i_{C1}	Current through capacitor C_1 in A
i_{L1}	Current through inductor L_1 in A
i_{Lbatt1}	Current through the inductor L_{batt1} in A
i_{Lsc1}	Current through the inductor L_{sc1} in A
i_{o1}	Output current from the left hand side boost converter leg(s) in A
i_{sc}	Supercapacitor current in A
K	Feedback gain for the current feedback ripple reduction method
k_{batt1}	SM controller gain for the battery connected converter legs
$k_{batt1,m}$	SM controller gain for the battery connected converter legs
$K_i(PI_{batt})$	Integral gain of the inner i_{Lbatt} current controller
$K_i(PI_P)$	Integral gain of the active power controller
$K_i(PI_Q)$	Integral gain of the reactive power controller
$K_i(PI_{sc})$	Integral gain of the inner i_{Lsc} current controller
$K_i(PI_{scv})$	Integral gain of the supercapacitor voltage controller
$K_i(PI_{SOC})$	Integral gain of the battery SOC controller
$K_i(PR)$	Integral gain of the PR controller
$K_{i,Esc}$	Integral gain of the supercapacitor energy controller
K_{Kalman}	Kalman filter gain for the battery SOC estimator

$K_p(PI_{batt})$	Proportional gain of the inner i_{Lbatt} current controller
$K_p(PI_P)$	Proportional gain of the active power controller
$K_p(PI_Q)$	Proportional gain of the reactive power controller
$K_p(PI_{sc})$	Proportional gain of the inner i_{Lsc} current controller
$K_p(PI_{scv})$	Proportional gain of the supercapacitor voltage controller
$K_p(PI_{SOC})$	Proportional gain of the battery SOC controller
$K_p(PR)$	Proportional gain of the PR controller
$K_{p,Esc}$	Proportional gain of the supercapacitor energy controller
$K_{p,vsc}$	Supercapacitor voltage controller gain
$k_{sc1,a}$	SM controller gain for the supercapacitor connected converter legs
$k_{sc1,b}$	SM controller gain for the supercapacitor connected converter legs
$k_{sc1,c}$	SM controller gain for the supercapacitor connected converter legs
$k_{sc1,m}$	SM controller gain for the supercapacitor connected converter legs
L_1	Left hand side boost inductor in μH
L_2	Right hand side boost inductor in μH
L_{batt1}	Left hand side battery connected boost inductor in μH
L_g	Grid interfacing inductor in μH
L_{sc1}	Left hand side supercapacitor connected boost inductor in μH
N_φ	Gain for the rule based controller
N_B	Gain for the rule based controller
P	Active power supplied by the inverter in W
P_{batt}	Power supplied by the battery in W
P_{HESS}	Active power supplied by the HESS in W
P_{Kalman}	Kalman filter error covariance matrix for the battery SOC estimator
P_{sc}	Power supplied by the supercapacitor in W

P_{tot}	Total input power supplied by both the battery and the supercapacitor in W
P_{tot1}	Total instantaneous power requirement from the left hand side boost converter legs in W
Q	Reactive power supplied by the inverter in VAr
Q_{HESS}	Reactive power supplied by the HESS in VAr
Q_{Kalman}	Kalman filter process covariance matrix for the battery SOC estimator
R_{C1}	ESR value of the output capacitor C_1 in Ω
R_{Kalman}	Kalman filter measurement covariance matrix for the battery SOC estimator
R_{L1}	ESR value of the inductor L_1 in Ω
R_{Lbatt1}	ESR value of the inductor L_{batt1} in Ω
R_{Lsc1}	ESR value of the inductor L_{sc1} in Ω
R_{RBC}	Second-order harmonic input current ripple amplitude with the rule based control method in A
R_{WFC}	Second-order harmonic input current ripple amplitude with the waveform control method in A
SOC_{batt}	SOC of the battery
T_D	Time delay between the perturbations and measurements for the rule based controller in s
T_s	Switching time period in s
v_{batt}	Battery terminal voltage in V
$V_{DC,ref}$	Reference DC shift of the output capacitor voltage in V
V_{DC1}	DC shift of the voltage across the output capacitor C_1 in V
V_{DC2}	DC shift of the voltage across the output capacitor C_2 in V
V_g	Grid voltage amplitude in V
v_{in}	Input voltage to the boost inverter in V

v_{Lbatt1}	Voltage across the inductor L_{batt1} in V
v_{Lsc1}	Voltage across the inductor L_{sc1} in V
v_o	Inverter output voltage in V
V_o	Amplitude of the inverter output voltage in V
v_{o1}	Voltage across output capacitor C_1 in V
v_{o2}	Voltage across output capacitor C_2 in V
v_{sc}	Supercapacitor terminal voltage in V
$v_{sc,init}$	Initial terminal voltage of the supercapacitor in V
$v_{sc,max}$	Maximum allowed supercapacitor voltage in V
$v_{sc,min}$	Minimum allowed supercapacitor voltage in V
$v_{sc,ref}$	Reference level for the supercapacitor voltage in V

Chapter 1

Introduction

1.1 Background and Motivation

Grid connected energy storage systems (ESSs) have many applications in modern electric grid such as renewable energy time shifting, intermittency handling, and power quality improvement [1–3]. Many energy storage technologies are available for grid connected applications depending on the required power density and energy density [4]. Battery ESSs are popular in residential and distributed level power networks due to its ease of implementation and geographical independence as compared to other energy storage technologies.

Battery ESSs for renewable energy applications should be designed with a higher power density to withstand the high and rapid power variations associated with the intermittent renewable power generation [5]. However, batteries have limited power capability and hence, a large number of batteries may need to be connected in parallel to obtain the required power capability. Additionally, battery ESSs should have a sufficient energy capacity to support the renewable energy time shifting.

However, the battery ESSs have a limited cycle life and the lifetime depends on the operating conditions of the battery. Numerous battery lifetime degradation factors can be identified as follows.

1. *High current amplitude*: High current amplitudes are identified as a major battery lifetime degradation factor [6, 7]. In renewable energy applications, battery ESSs have to handle high power variations and hence battery has to sustain high current rates even with a large number of parallel battery modules.

2. *Battery current fluctuations and micro-cycles*: Battery current fluctuations are another factor affecting the battery lifetime [8–10]. Furthermore, such current fluctuations can increase the number of battery charge discharge micro-cycles (short

charge-discharge cycles [11]) which reduces the effective cycle life of the battery [11, 12]. Due to the intermittency of renewable power generation, battery current fluctuations and micro-cycles are imminent in such battery ESSs.

3. *Ripple current*: Continuous ripple components in the battery current can increase the internal heating of the battery which causes a degradation in battery lifetime [13, 14]. In single phase grid connected applications, a second-order harmonic ripple component appears in the battery current. Second-order harmonic component in the battery current increases as the inverter output power increases. Additionally, a switching frequency ripple current is also present in the battery current waveform due to the operation of the power converters. Both the second-order harmonic ripple current as well as the switching frequency current component adversely affect the lifetime of the battery [13–15].

Recently the supercapacitor technology has become popular in ESS applications due to its higher power capability and superior cycle life compared to the battery technology [16]. Typically, supercapacitors have 1 to 10 Wh/kg specific energy and 1000 to 5000 W/kg specific power. The charge/discharge efficiency of supercapacitors is very high, ranging from 85% to 98% [17]. In contrast, Lithium batteries usually have 50 to 500W/kg specific energy and 10 to 500W/kg specific power. Additionally, its charge/discharge efficiency is typically between 75% to 90%. [17]. Battery-supercapacitor hybrid energy storage systems (HESSs) have been proposed in the literature as a way of increasing the power capability of the energy storage systems and extending the lifetime of the battery [6,10,12,16–53]. HESSs combine individual advantages of both the battery and the supercapacitor and create a single ESS with increased power and energy capabilities. These HESSs are classified based on the power converter configuration and power allocation methods in Section 11.1 and Section 11.2.

Battery-supercapacitor HESSs have been proposed for various applications such as electric vehicles and grid energy storage systems. In both electric vehicle and grid energy storage system applications, the supercapacitors increase the energy storage system power capability and the battery lifetime. Numerous battery-supercapacitor HESSs were studied in the literature, and they can be classified based on the power converter configuration as shown in Figs. 1.1 and 1.2.

1.1.1 Power Converter Configurations for HESSs

HESS can be categorized into two main groups, namely passive HESSs and active HESSs [18]. In passive HESSs, the battery and the supercapacitor terminals are

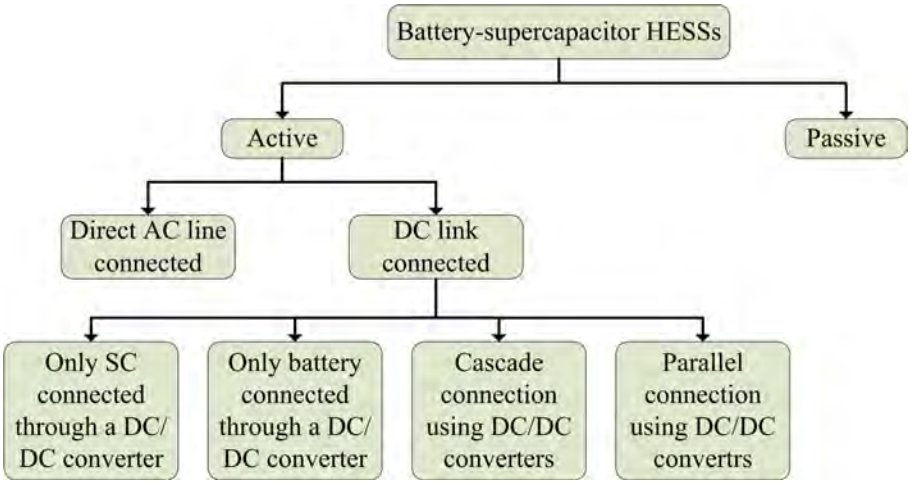

Fig. 1.1: Types of hybrid energy storage systems

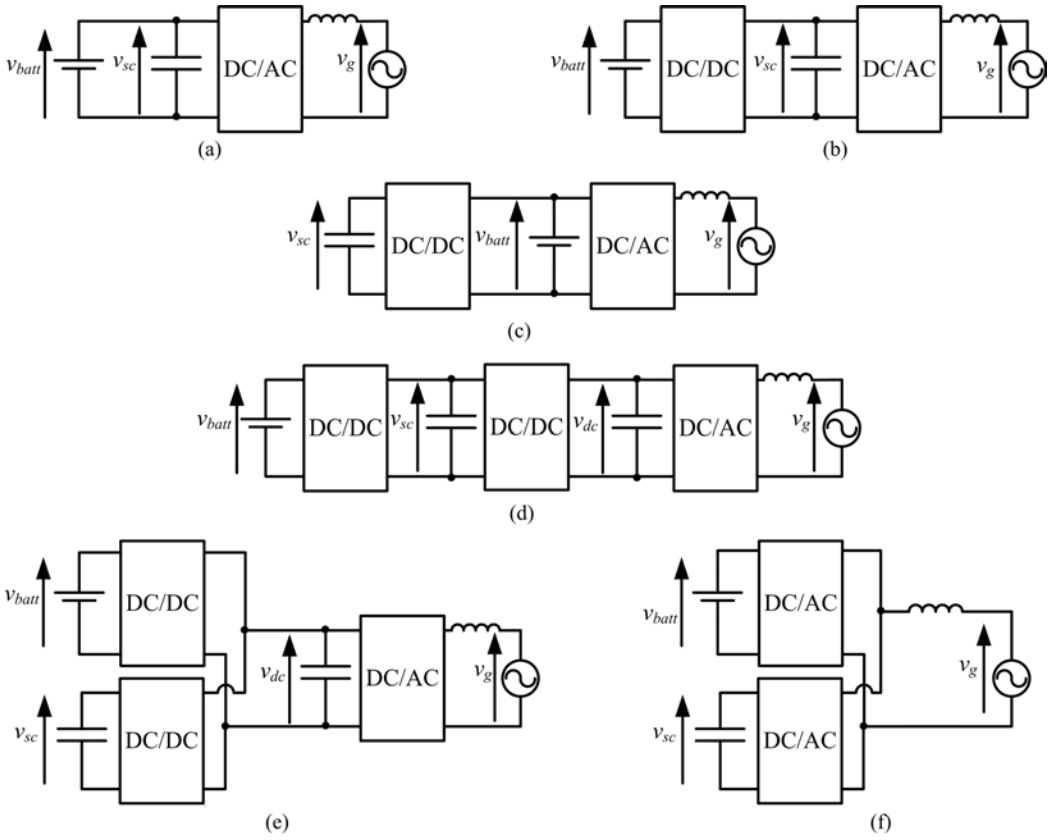

Fig. 1.2: Types of hybrid energy storage system based on the power converter configuration

interconnected without using an interfacing power converter as illustrated in Fig. 1.2(a) [18, 51–53]. In this configuration, power allocation between the battery and the supercapacitor is uncontrollable and depends on the impedance of the battery and the supercapacitor. The battery voltage has to be controlled in a range suitable for the DC/AC converter operation. Hence, the complete operating range of the battery may not be utilized. The supercapacitor voltage is controlled by the battery voltage,

and hence, the supercapacitor cannot charge or discharge independently. Because of that energy stored inside the supercapacitor cannot be utilized properly in passive HESSs [17]. To alleviate the inherent disadvantages of the passive HESS, active HESSs have been proposed. In the active HESS, power converters are used to interface the battery and/or the supercapacitor to a DC link or to an AC line. DC link connected battery-supercapacitor HESSs can be categorized into four groups as illustrated in Figs. 1.1 and 1.2.

1. *Only the battery is connected through a DC/ DC converter*: In this case, the battery is connected through a DC/DC converter and the supercapacitor is directly connected to the DC/AC converter as shown in Fig. 1.2(b) [17–22]. The battery interfacing DC/DC converter enables the maximum utilization of the battery operating region and usage of low voltage battery modules. However, voltage variation of the supercapacitor has to be controlled to maintain the required DC link voltage. Hence, the energy stored in the supercapacitor cannot be utilized properly. Additionally, a large number of supercapacitor cells may need to be connected in series to support the required DC link voltage.

2. *Only the supercapacitor is connected through a DC/DC converter*: The battery is directly connected to the DC link while the supercapacitor is connected through a DC/DC converter as depicted in Fig. 1.2(c) [12, 23–26]. A high voltage battery system may be required due to the direct DC link connection of the battery. Furthermore, the operating range of the battery may have to be limited to maintain the DC link voltage. However, a low voltage supercapacitor module can be employed as a result of the interfacing DC/DC converter and also this enables a broader operating voltage range to the supercapacitor which helps to increase its energy utilization.

3. *Cascade connection using DC/DC converter*s: A cascaded battery-supercapacitor HESS is illustrated in Fig. 1.2(d) and an alternative cascaded system can be obtained by interchanging the battery and the supercapacitor positions [18, 30, 42]. Both the battery and the supercapacitor modules can have lower voltages compared to the DC link voltage. Moreover, the DC/DC converters enable the full utilization of the operating regions of the battery as well as the supercapacitor. However, the introduction of the additional DC/DC converter can reduce the efficiency of the system compared to the previous solutions and the DC/DC converter connected to the DC link should be designed such that it can handle the full amount of HESS

power.

4. *Parallel connection using DC/DC converters*: Parallel connection is an alternative way to the cascade connection and in this configuration, two DC/DC converters are used to interface the battery and the supercapacitor to a DC link as shown in Fig. 1.2(e) [6, 10, 16, 18, 27–43]. The battery and the supercapacitor can have lower voltages compared to the DC link voltage and the full operating regions of the DC sources can be utilized. Since only a fraction of the total HESS power is supplied by the battery and the supercapacitor, the interfacing DC/DC converters can be designed with a lower power rating than the DC/AC converter power rating. The battery and the supercapacitor currents can be controlled individually based on the power requirement and the configuration has a degree of fault tolerance since the system can operate even when a failure occurs in the battery or the supercapacitor system. This structure has been widely used in the battery-supercapacitor HESSs proposed in the literature due to the above mentioned advantages.

Foregoing active HESS structures in the single phase grid connected applications contain at least a DC/DC converter and a DC/AC converter. Hence, a DC to DC power conversion stage followed by a DC to AC power conversion stage can be identified and this leads to a reduction in the conversion efficiency. Direct AC line connected ESSs were proposed in the literature as a way of increasing the system power conversion efficiency by minimizing the number of power processing stages [44, 49, 54–56]. Authors in [57] reported approximately 5% greater power conversion efficiency for a single stage ESS compared to a two stage ESS. Various types of direct AC line connected battery-supercapacitor HESSs were proposed in the literature using numerous power converter topologies [44–50].

Two parallel inverter based battery-supercapacitor HESS topology is shown in Fig. 1.2(f) [47–50]. In this topology, the battery and the supercapacitor operating voltage ranges have to be selected based on the DC/AC power converter configuration. For example, if the H-bridge inverters are used as the DC/AC converters, the battery and the supercapacitor must have higher voltage values compared to the peak output voltage. Alternatively, DC/AC converters with boosting capability allow using low voltage battery and supercapacitor modules. The parallel inverter configuration provides redundancy and independent control of the battery and the supercapacitor currents.

Few direct AC line connected battery-supercapacitor HESSs were proposed using three level neutral point calmed inverter [44, 45] and matrix converter [56] for three phase applications.

However, most of the battery-supercapacitor HESSs proposed in the literature are based on the DC link connected structure and consequently, many design issues related to the implementation of the direct grid integrated battery-supercapacitor HESSs such as second-order harmonic ripple current reduction and controller implementation have not been addressed.

1.1.2 HESS Power Allocation Methods

Various power allocation methods were studied for the HESSs. The most basic battery-supercapacitor HESS power allocation approach is a filter based method. In the filter based power allocation method, a low pass filter or a high pass filter is employed to divert the high frequency power variations to the supercapacitor while the battery responds to the low frequency power requirement [12, 27, 37, 43, 46, 58]. The filter based HESSs reduce the battery current fluctuations, the second-order harmonic ripple component of the battery current and also indirectly reduce the peak power requirement of the battery. In some cases, an additional supercapacitor voltage controller is employed with the power allocation filter to maintain the supercapacitor voltage around a reference value [12, 27].

Battery power limiting based HESS power allocation is another commonly used approach. In this method, the power supplied by the battery is limited to a pre-defined maximum power value and the required balance power component is allocated to the supercapacitor [6, 17, 24, 59]. This method reduces the peak power requirement of the battery and hence reduces the peak battery current. For example, authors in [6] reported 49% to 80% peak battery current reduction. However, the battery current waveform is not smoothened and furthermore, this method is not effective in reducing the battery current ripple components.

Many other alternative power allocation methods were studied in the literature. In [10], a battery power ramp rate control method was proposed to allocate the power components between the battery and the supercapacitor. Predictive algorithms were used to allocate the power components in [28, 30] while [35, 60] employed fuzzy logic control algorithms. In [23], the authors used neural networks to achieve the power allocation and the authors in [34,42] used optimization methods. The authors in [50] employed a wavelet based power allocation method for battery-supercapacitor HESS. Even though many different power allocation methods were studied for the battery-supercapacitor HESSs, the main objective of all the methods can be identified as limiting the battery current fluctuations and the peak battery power while the supercapacitor responds to the fast, high and varying power components.

After studying the existing battery-supercapacitor HESSs, the following main

limitations can be identified in the previously proposed single phase battery-supercapacitor HESSs.

1. Majority of the HESSs were designed using the DC link based converter configurations. In the DC link based ESSs, multiple power processing stages can be observed which reduces the efficiency of the system. Hence, direct AC line integrated ESSs were proposed as a way of reducing the power processing stages. Even though a few direct AC line integrated HESSs were studied in the literature, power allocation methods and energy storage element sizing were not analyzed. Furthermore, none of the single phase direct grid connected battery-supercapacitor HESSs were justified using experimental results.

2. None of the previously proposed battery-supercapacitor HESSs considered the switching frequency ripple component reduction in the battery and the supercapacitor currents. The switching frequency ripple current component increases the DC source internal temperature and degrades its lifetime.

3. In the battery-supercapacitor HESSs proposed for single phase applications (DC link based and direct AC line integrated), the second-order harmonic ripple current component was allocated to the supercapacitor. However, according to [61], such continuous ripple current leads to supercapacitor overheating which in turns reduces its lifetime [61].

1.2 Objectives and Contributions

1.2.1 Objectives of the Research

The key objective of the research is to study and develop a single phase direct grid integrated battery-supercapacitor HESS and the associated sub-objectives of the research can be identified as follows.

1. *Develop a power allocation strategy between the battery and the supercapacitor, and identify a suitable storage elements sizing method.*

   Power allocation strategy is one of the key aspects of the HESS design. In the HESS, fast and large power fluctuations has to be allocated to the supercapacitor while the battery supplies the steady power requirement. This helps to reduce the power requirement from the battery and also the reduction in battery current fluctuations helps to increase the battery lifetime. Energy storage element sizing is strongly coupled with the HESS power allocation method. The battery and the

supercapacitor have to be properly sized based on the designed power allocation method to ensure proper operation of the HESS for a considered application.

2. *Design the HESS with a proper battery and supercapacitor SOC control method.*

   The battery and the supercapacitor SOC control is essential in HESSs to avoid energy storage element over-charging and over-discharging. Over-charging of the energy storage elements can lead to hazardous situations while over-discharging leads to a degradation of the battery and the supercapacitor lifetime. Furthermore, low battery and supercapacitor voltages reduce the efficiency of the HESS. Hence, it is important to control the battery and the supercapacitor SOC to achieve the desired HESS performances.

3. *Apply advanced control methods to achieve better performance and ease of implementation.*

   Advanced control methods are essential in HESSs in order to incorporate the non-linear behavior of the power converters and also to improve the performance of the system.

4. *Identify ways of reducing the switching frequency ripple components in the battery and the supercapacitor current.*

   Due to the switching operation of the power converters, the battery and the supercapacitor have to sustain a switching frequency ripple current component. The ripple current components increase the internal heating of the energy storage elements. Hence, by developing a suitable switching frequency ripple current reduction method, both the battery and the supercapacitor internal heating can be reduced.

5. *Develop ways of mitigating the second-order harmonic ripple component from the supercapacitor current.*

   Due to the single phase operation of the HESS, a second-order harmonic power component has to be supplied by the HESS and the relevant second-order harmonic current component appears in the DC side of the power converter. The second-order harmonic ripple current component adversely affects the lifetime of both the battery and the supercapacitor. Hence, it is important to identify suitable ways to mitigate the ripple current component in both the battery and supercapacitor currents.

6. *Experimentally validate the designed single phase grid connected battery-supercapacitor HESS.*

In order to demonstrate the applicability of the proposed HESS and control methods in an actual environment, it is important to validate the performance of the HESS experimentally.

1.2.2 Contributions of the Research

The contributions of this research can be summarized as follows.

1. Chapter 2 and Chapter 3: An interleaved boost inverter based single phase grid integrated battery-supercapacitor HESS was proposed in [62–64]. The interleaved boost inverter based HESS provided both boosting and inversion functions in a single power processing stage and the interleaved operation reduced the switching frequency ripple component of both the battery and the supercapacitor currents. The proposed HESS was able to allocate the fast power fluctuations to the supercapacitor while the battery responds to the slow varying power component. In this thesis, power fluctuations greater than a pre-determined cut-off frequency is considered as fast power fluctuations. The cut-off frequency or the power allocation frequency is a design parameter of the HESS which is selected at the design phase of the HESS. The proposed HESS controller enabled the HESS operation within the battery SOC limits. A supercapacitor voltage controller (SCVC) was employed to maintain the supercapacitor voltage around a reference voltage level to reduce the risk of supercapacitor over-charging and over-discharging. The performance of the proposed HESS was experimentally verified in [64]. The proposed HESS was the first single phase direct grid integrated battery-supercapacitor HESS which was validated experimentally. Furthermore, the proposed HESS was the only battery-supercapacitor HESS which was able to reduce the switching frequency ripple components of both the battery and the supercapacitor current waveforms using a phase shifted interleaved operation [64].

2. Chapter 4: A supercapacitor energy controller (SCEC) and a high-pass filter based power allocation strategy was proposed in [65] to circumvent the issues associated with the nonlinearity of the conventional SCVC and a high-pass filter based power allocation method. The dynamic performance of the supercapacitor energy controlled filter based battery-supercapacitor HESS was extensively analyzed. Then, a HESS power allocation parameter selection method and an energy storage element sizing method were proposed for a supercapacitor energy controlled filter based HESS [65]. The proposed method enabled the dynamic analysis of the power allocation method and precise selection of power allocation parameters and energy

storage element sizes for a considered application.

3. Chapter 5: A novel fixed frequency sliding mode (SM) controlled boost inverter based HESS was proposed in [66] to achieve better output capacitor voltage reference following performance and hence to reduce the risk of DC current injection to the grid. The fixed frequency SM controller was able to overcome the issues associated with the traditional SM controllers for the boost inverter topology such as high and variable frequency switching operation and component selection complexity. In order to allocate the high frequency power components to the supercapacitor, a PI controller based SCEC was proposed and the dynamic performance of the HESS power allocation method was analyzed. Furthermore, compared to the existing fixed frequency SM controllers for the boost DC/DC converters, the SM controller was implemented using variable amplitude PWM carrier signals generated using the output capacitor voltage and inductor current measurements thus eliminating the requirement of the output capacitor currents measurement.

4. Chapter 6: A rule-based controller was proposed and analyzed to reduce the second-order harmonic ripple component of the boost inverter input current [67]. The method was designed to eliminate the limitations associated with the existing waveform control ripple reduction method. The ripple reduction performance of the waveform control method was affected by the boost inverter internal resistance and parameter variations. The rule-based controller was able to reduce the second-order harmonic ripple current by at least a factor of 6.

5. Chapter 7: A novel current feedback ripple reduction method was proposed to mitigate the second-order harmonic ripple component in the boost inverter input current [68]. The method demonstrated superior performance compared to the existing methods by achieving a significant second-order harmonic ripple current reduction without increasing other harmonic current components. The current feedback ripple reduction method was able to reduce the second-order harmonic current component by at least a factor of 20. Additionally, the method was able to achieve ripple current reduction even during output power transient conditions. Then, the current feedback ripple reduction method was applied to the boost inverter based HESS to mitigate the second order harmonic ripple component in the supercapacitor current [69]. None of the existing battery-supercapacitor HESSs designed for single phase applications considered the second-order harmonic ripple component reduction in the supercapacitor current.

1.3 List of Publications

1.3.1 Journal Publications

[J1] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "Single-Phase Grid-Connected $LiFePO_4$ Battery-Supercapacitor Hybrid Energy Storage System with Interleaved Boost Inverter," in *IEEE Transactions on Power Electronics*, vol.30, no.10, pp.5591-5604, Oct. 2015 doi: 10.1109/TPEL.2014.2372774

[J2] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "A Rule-Based Controller to Mitigate DC-Side Second-Order Harmonic Current in a Single-Phase Boost Inverter," in *IEEE Transactions on Power Electronics*, vol.31, no.2, pp.1665-1679, Feb. 2016 doi: 10.1109/TPEL.2015.2421494

[J3] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "An Input Current Feedback Method to Mitigate the DC-Side Low-Frequency Ripple Current in a Single-Phase Boost Inverter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4594-4603, June 2016. doi: 10.1109/TPEL.2015.2473170

[J4] Abeywardana, D.B.W; Hredzak, B.; Agelidis, V.G., "A Fixed Frequency Sliding Mode Controller for a Boost Inverter Based Battery-Supercapacitor Hybrid Energy Storage System," in *IEEE Transactions on Power Electronics*, vol.PP, no.99, pp.1-1 doi: 10.1109/TPEL.2016.2527051

[J5] Abeywardana, D.B.W; Hredzak, B.; Agelidis, V.G; Demetriades, G., "Supercapacitor Sizing Method for Energy Controlled Filter Based Hybrid Energy Storage Systems," in IEEE Transactions on Power Electronics , vol.PP, no.99, pp.1-1 doi: 10.1109/TPEL.2016.2552198

1.3.2 Conference Publications

[C1] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "An Integration Scheme for a Direct AC Line Battery-Supercapacitor Hybrid Energy Storage System," in 2*013 Australasian Universities Power Engineering Conference (AUPEC)*, vol., no., pp.1-6, Sept. 29 2013-Oct. 3 2013 doi: 10.1109/AUPEC.2013.6725474

[C2] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "A Single Phase Grid Integration Scheme for Battery-Supercapacitor AC Line Hybrid Storage System," in *2014 IEEE International Conference on Industrial Technology (ICIT)*, vol., no., pp.235-240, Feb. 26 2014-March 1 2014 doi: 10.1109/ICIT.2014.6894873

Table 1.1: The publications relevant to this thesis

Thesis Chapter	**Publication**
Chapter 2	[J1]
Chapter 3	[J1],[C1],[C2]
Chapter 4	[J5]
Chapter 5	[J4]
Chapter 6	[J2]
Chapter 7	[J3], [C3]

[C3] Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G., "Battery-supercapacitor hybrid energy storage system with reduced low frequency input current ripple," *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, Palermo, Italy, 2015, pp. 328-332. doi: 10.1109/ICRERA.2015.7418719

The journal and conference publications related to the thesis chapters are as follows.

1.4 Thesis Outline

The remainder of the thesis is organized as follows.

- Chapter 2 discusses operation of the boost inverter topology which is used to design the single phase grid connected battery-supercapacitor HESS. Switching frequency ripple component of the boost inverter DC side current is analyzed with the conventional in-phase PWM operation. Then, a phase shifted interleaved operation for the boost inverter topology is proposed and its effectiveness in reducing the switching frequency ripple component of the boost inverter DC side current is illustrated.

- Chapter 3 presents the proposed interleaved boost inverter based single phase grid connected battery-supercapacitor HESS. At the initial stage of the research, a filter based power allocation method with a SCVC is employed to achieve the power allocation between the battery and the supercapacitor. A double-loop (DL) control strategy is used to control the power converter structure. A battery SOC controller with an extended Kalman filter based battery SOC estimation method is developed. Experimental results are used to validate the operation of the proposed interleaved boost inverter based battery-supercapacitor HESS.

- Chapter 4 analyzes the power allocation between the battery and the supercapacitor for a supercapacitor SOC controlled filter based battery-supercapacitor HESS. A

SCEC and a filter based power allocation method is proposed to circumvent the challenges associated with the non-linearity of the SCVC and a filter based HESS power allocation method [65]. Furthermore, a power allocation parameter selection method and an energy storage element sizing method for a supercapacitor energy controlled filter based HESS are proposed for a given HESS application.

- Chapter 5 presents the proposed fixed-frequency SM controller for the boost inverter based battery-supercapacitor HESS. A better output capacitor voltage reference following performance is achieved with the SM controller mitigating the risk of DC current grid injection when the boost converter leg parameters are non-ideal. DC current grid injection can cause adverse effects such as transformer saturation and power quality issues. The fixed frequency SM controller is able to mitigate the issues associate with the traditional SM controllers for the boost inverters such as high and variable switching frequency operation and component selection complexity. The SM controller considers the non-linear behavior of the boost inverter topology and also simplifies the controller implementation.

- Chapter 6 studies the second-order harmonic ripple component reduction in the DC side current of the battery-supercapacitor HESS. In the initial stages of the HESS, the second-order harmonic ripple current component was allocated to the supercapacitor. However, this ripple current component can adversely affect the lifetime of the supercapacitor [61]. Hence, a suitable second-order harmonic ripple reduction method has to be identified for the HESS. For that, the existing second-order harmonic ripple reduction methods for a single boost inverter are studied. Chapter 6 evaluates performance and limitations of the existing waveform control ripple reduction method. Then, a rule-based control method is proposed to overcome the limitations of the waveform control ripple reduction method. The performance of the rule-based controller is validated using experimental results.

- Chapter 7 proposed a novel current feedback ripple reduction method for the boost inverter topology. Compared to the rule-based control method and the waveform control method, the current feedback method is able to achieve a significant second-order harmonic ripple current reduction in the boost inverter DC side current without increasing other harmonic components. Furthermore, the current feedback method is able to mitigate the second-order harmonic current component even in output power transient conditions and hence the method can be applicable to the boost inverter based battery-supercapacitor HESS. Then, a boost inverter based battery-supercapacitor HESS with reduced low frequency input current ripple is

proposed using the current feedback ripple reduction method.

- Chapter 8 summarizes the conclusions of the research and presents a discussion on possible future work.

Chapter 2

Operation of the Boost Inverter

In this chapter, operation of a grid connected boost inverter is discussed. The boost inverter topology provides means of low voltage DC source grid integration by providing both boosting and inversion functions in a single power processing stage. The switching frequency ripple component of the boost inverter with the conventional in-phase PWM operation is extensively analyzed in Subsection 2.3.1. Subsection 2.3.2 presents the proposed phase shifted interleaved operation for the boost inverter topology [64] and the component selection for the proposed interleaved boost inverter is discussed in Subsection 2.3.3. Finally, the input current switching frequency ripple reduction performance of the interleaved boost inverter is presented in Subsection 2.3.4.

2.1 Introduction

Power converter topologies are essential to integrate low voltage DC energy storage devices to single phase AC power grid, and numerous DC/AC power converter topologies have been studied for grid connected energy storage system applications. Depending on the power flow direction, DC/AC power converters can be classified in to two groups namely, unidirectional power converters and bidirectional power converters. Bidirectional power flow is essential in a battery storage system to facilitate the charging and discharging of the battery.

H-bridge inverter is a widely used DC/AC power converter topology in grid applications [70]. The amplitude of the H-bridge inverter output voltage is less than the inverter input voltage and hence, additional DC/DC power converters are required to boost the DC source voltage when low voltage energy storage devices are used. In this type of power conversion systems, two power processing stages can be observed. Further, the output voltage of the H-bridge inverter has to be properly filtered to obtain the required sinusoidal output voltage and current.

Boost inverter is an alternative DC/AC power converter topology which can be used to integrate low voltage DC energy storage systems to a single phase AC line [55]. The boost inverter topology facilitates the DC source AC line integration by providing both the boosting and inversion functions in a single power processing stage. Further, the boost inverter naturally generates a sinusoidal output voltage and hence reduces the output filter requirement.

Numerous boost inverter based energy storage systems were studied in the literature both for stand-alone applications as well as for grid connected applications [54, 55, 57, 71–79].

A variable frequency sliding mode (SM) controlled stand-alone boost inverter was presented in [55] and in [54], the authors presented a double loop (DL) control strategy for a stand-alone boost inverter. A dynamic SM controller for the stand-alone boost inverter topology was studied in [71]. In [72] and [73] the authors presented grid integrated boost inverter systems using variable frequency SM control method and grid current control method respectively. A waveform control ripple reduction method was studied for the boost inverter topology in [74–77]. Boost inverter based fuel cell-battery energy storage systems were presented in [57, 78]. A modified boost inverter based multi input energy storage system was discussed in [79].

In the boost inverter topology, two inductors are connected to the input DC source. The switching frequency ripple amplitude of the input current depends on the individual ripple components of the inductor currents. As a result of the in-phase PWM operation of the boost inverter, the inductor current switching frequency ripple components are also in-phase and hence the DC source switching frequency ripple current component is greater than each individual inductor current ripple due to addition of the two ripple components.

Interleaving is a widely accepted concept used to reduce the switching frequency ripple component in the DC source current by using parallel power converters [80]. Interleaving concept for the conventional DC/DC boost converter topology has been well documented in literature [80, 81]. In this research, the interleaving concept is applied to the boost inverter topology as a way of reducing the DC source switching frequency ripple current.

In this chapter, the basic operation of the conventional grid connected boost inverter is discussed first. Subsection 2.3.1 provides a detailed analysis on the switching frequency ripple component in the DC source current with the conventional in-Phase PWM operation. The proposed phase shifted interleaved operation for the boost inverter is discussed in Subsection 3.3.2 while the component selection for the interleaved boot inverter is presented in Subsection 2.3.3. Subsection 2.3.4 evaluates the switching frequency ripple current reduction performance of the proposed phase shifted interleaved

operation while conclusions of the chapter are summarized in Section 2.4.

2.2 Operation of the Single Phase Grid Connected Boost Inverter

The boost inverter configuration consists of two boost converter legs as shown in Fig. 2.1 [55]. The left hand side boost converter leg is denoted by subscript 1. Each boost converter leg has two power switches, and gate signals for the top switches (subscript T) and the bottom switches (subscript B) of each converter leg are complimentary. The two switches in the each boost converter leg ensure the continuous conduction mode operation and facilitate the bi-directional power flow.

Objective of the boost inverter is to generate a differential sinusoidal output voltage given by,

$$v_{o,ref} = V_o sin(\omega t + \delta) \tag{2.1}$$

where V_o, ω and δ are the inverter output voltage amplitude, frequency and phase angle respectively. In order to obtain the required differential output voltage, the left hand side boost converter legs and the right hand side boost converter legs are required to follow the voltage references $v_{o1,ref}$ and $v_{o2,ref}$ across the output capacitors C_1 and C_2;

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2} sin(\omega t + \delta) \tag{2.2}$$

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2} sin(\omega t + \delta). \tag{2.3}$$

$V_{DC,ref}$ is a reference DC shift introduced to ensure the boost mode operation and v_{in} is the DC input voltage to the boost inverter. Hence, $V_{DC,ref} \geq v_{in} + \frac{V_o}{2}$. The main

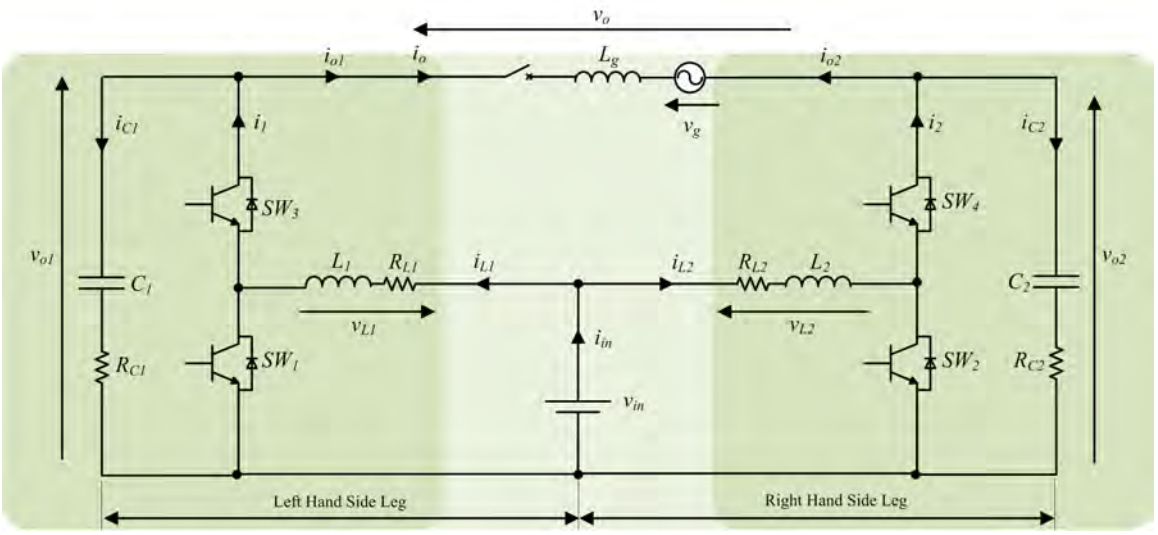

Fig. 2.1: Single phase grid connected boost inverter

disadvantage of using independent voltage references as in (2.2) and (2.3) is that the inverter output voltage v_o is not directly controlled and in order to alleviate the problem, the voltage across the output capacitor C_2 can be controlled using the reference signal given as [55],

$$v_{o2,ref} = v_{o1} - v_{o,ref}. \tag{2.4}$$

The average mode of the left hand side boost converter leg can be illustrated as in Fig.2.2, and the model equations of the boost converter leg can be written as,

$$v_{in} - v_{L1} = (1 - d_1)v_{o1} \tag{2.5}$$

$$i_{C1} + i_{o1} = (1 - d_1)i_{L1} \tag{2.6}$$

where v_{o1} and i_{C1} are the voltage and current of the output capacitor C_1, and v_{L1} and i_{L1} are the voltage and current of the inductor L_1, respectively. d_1 is the duty cycle time average values of the switch $Sw_{1,B}$, and i_{o1} is the output current from the left hand side boost converter leg. The inductor and capacitor differential equations can be written as,

$$v_{L1} = R_{L1}i_{L1} + L_1\frac{di_{L1}}{dt} \tag{2.7}$$

$$i_{C1} + R_{C1}C_1\frac{di_{C1}}{dt} = C_1\frac{dv_{o1}}{dt} \tag{2.8}$$

where R_{L1} and R_{C1} are the internal resistance of the inductor L_1 and capacitor C_1, respectively.

The grid integration of the boost inverter can be achieved through an interfacing inductor as shown in Fig.2.1. Equivalent circuit of the grid connected boost inverter can be obtained by replacing the inverter and the grid using AC voltage sources as shown in Fig.2.3 In the figure, V_g, V_o, and δ are the grid voltage amplitude, inverter voltage amplitude, and phase angle of the inverter voltage with respect to the phase angle of the grid voltage, respectively. The active power (P) and the reactive power (Q) delivered to the grid can be calculated as,

$$P = \frac{V_g V_o}{2\omega L_g} sin\delta \tag{2.9}$$

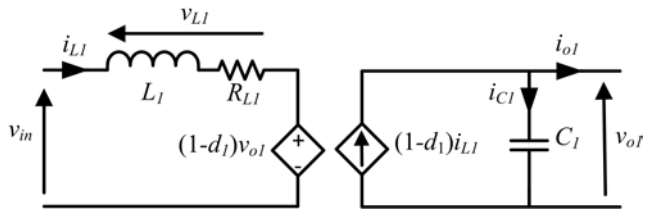

Fig. 2.2: Average model of the left hand side boost converter leg.

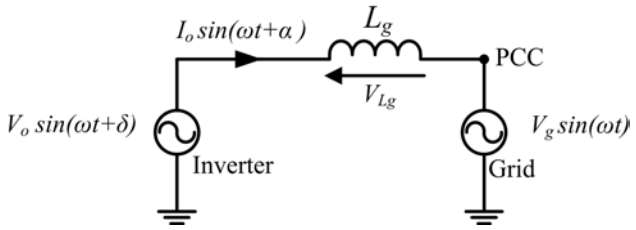

Fig. 2.3: Equivalent circuit of the grid connected boost inverter

$$Q = \frac{V_g V_o}{2\omega L_g} cos\delta - \frac{V_g^2}{2\omega L_g}. \tag{2.10}$$

Note that, the peak voltage and current values are considered for the calculations. Then, for small δ values (2.9) and (2.10) can be approximated as,

$$P = \frac{V_g V_o}{2\omega L_g}\delta \tag{2.11}$$

$$Q = \frac{V_g(V_o - V_g)}{2\omega L_g}. \tag{2.12}$$

Hence, by proper control of the inverter output voltage amplitude and phase-angle with respect to the grid voltage, the active and reactive power exchange between the grid and the inverter can be achieved.

Fig.2.4 depicts the operation of the boost inverter when the inverter supplies active power to the grid. v_{o1} and v_{o2} waveforms are DC shifted, and the DC shift is selected such that v_{o1} and v_{o2} are always greater than the input voltage v_{in}. The output capacitor voltage AC component amplitude equals to half of the required output voltage amplitude. A second-order harmonic ripple current component can be observed in the boost inverter input current in Fig.2.4 due to the single phase grid integration.

2.3 Switching Frequency Ripple Component of the Boost Inverter DC Side Current

The DC side switching frequency ripple current component of the boost inverter depends on the individual ripple components of the currents through inductors L_1 and L_2, which are connected to the DC source. In the boost converter operation, the switching frequency ripple component of i_{L1} and i_{L2} are in-phase and hence, the DC source switching frequency ripple component is greater than each individual inductor current ripple due to addition of the two ripple components.

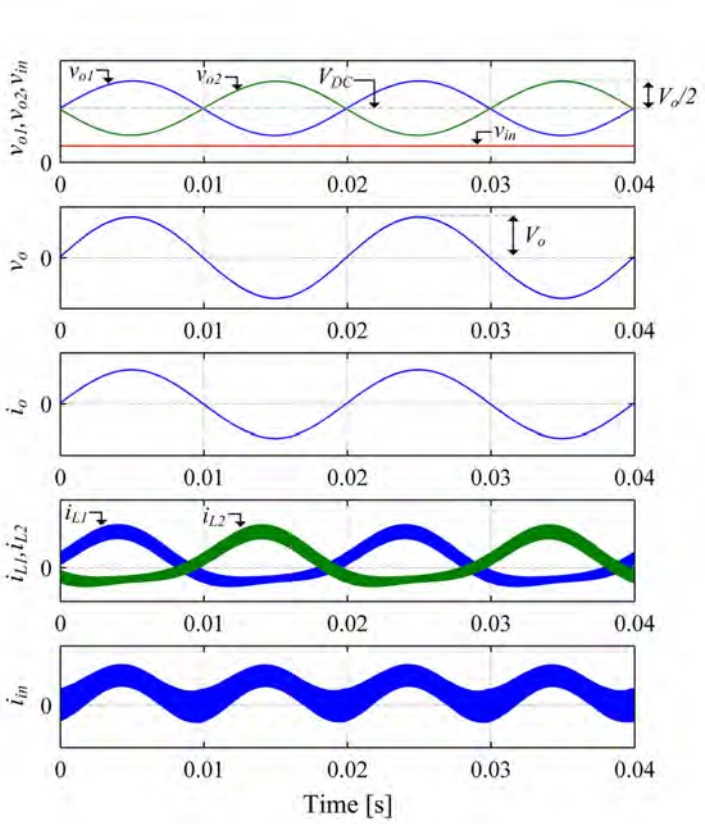

Fig. 2.4: Boost inverter operating waveforms

2.3.1 In-phase PWM Operation

Fig. 2.5 illustrates the gate signals of the switches $Sw_{1,B}$ and $Sw_{2,B}$ with the inductor current and DC source current switching frequency ripple waveforms. In this thesis, PWM is achieved by comparing the duty ratio values with symmetric triangular carrier signals which range between 0 and 1. It can be observed that two gate signals are in-phase (i.e., the centers of the logic high levels of the two gate signals and the centers of the logic low levels of the two gate signals are aligned separately). Duty ratio values of the switches $Sw_{1,B}$ and $Sw_{2,B}$ are d_1 and d_2, respectively. Inductor currents i_{L1} and i_{L2} can be written as,

$$\begin{aligned} i_{L1} &= I_{L1} + \Delta i_{L1} \\ i_{L2} &= I_{L2} + \Delta i_{L2}. \end{aligned} \tag{2.13}$$

Hence, the total DC source current is,

$$i_{in} = I_{in} + \Delta i_{in} \tag{2.14}$$

where I_{in}, I_{L1}, and I_{L2} are the average values of the DC source current and inductor currents over one switching period, T_s. I_{in} is the sum of two average components I_{L1} and

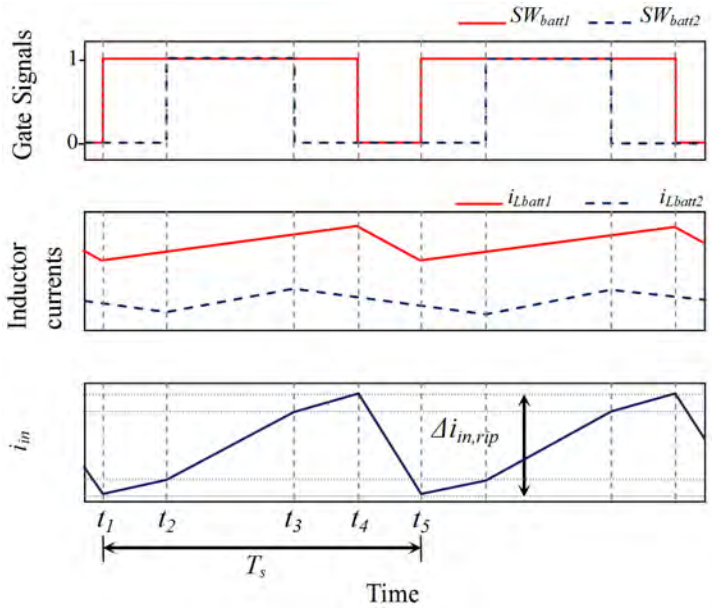

Fig. 2.5: Ripple current waveforms when the PWM signals for two converter legs are in-phase

I_{L2}. Δi_{in} is the instantaneous ripple component of the DC source current which is given by $\Delta i_{in} = \Delta i_{L1} + \Delta i_{L2}$.

In this converter structure, d_1 and d_2 are changing over the time. First, $d_1 \geq d_2$ situation is considered as shown in Fig. 2.5. The change of the DC source current from time t_x to t_y can be written as,

$$\Delta i_{in,tx,ty} = i_{in}(t_y) - i_{in}(t_x) \tag{2.15}$$

where, $i_{in}(t_x)$ and $i_{in}(t_y)$ are the instantaneous DC source currents at time t_x and t_y respectively.

From time t_1 to t_2, $Sw_{1,B}$ is ON and $Sw_{2,B}$ is OFF. Hence, i_{L1} is increasing and i_{L2} is decreasing. The total DC source current can either increase or decrease depending on the amount of increment in i_{L1} and amount of decrement in i_{L2}. Fig. 2.5 shows the waveforms related to the situation where the total DC source current is increasing.

From time t_2 to t_3, both switches are ON, and therefore, both inductor currents are increasing. Because of that, the total DC source current is also increasing.

$Sw_{1,B}$ is ON and $Sw_{2,B}$ is OFF from time t_3 to t_4. Hence, i_{L1} is increasing while i_{L2} is decreasing. In this case also, the total DC source current can either increase or decrease depending on i_{L1} and i_{L2}.

From t_4 to t_5, both switches are OFF and both inductor currents are decreasing. Hence, the total DC source current is decreasing.

Without a loss of generality, the DC source current switching frequency ripple

magnitude $\Delta i_{in,rip}$ can be written as,

$$\Delta i_{in,rip} = max(|\Delta i_{in,t1,t2}|, |\Delta i_{in,t2,t3}|, |\Delta i_{in,t3,t4}|, |\Delta i_{in,t4,t5}|). \tag{2.16}$$

It can be observed that,

$$\Delta i_{in,t1,t2} = \Delta i_{in,t3,t4}. \tag{2.17}$$

Moreover,

$$\Delta i_{in,t1,t2} + \Delta i_{in,t2,t3} + \Delta i_{in,t3,t4} + \Delta i_{in,t4,t5} = 0. \tag{2.18}$$

Because of that, (2.16) can be reduced to

$$\Delta i_{in,rip} = max(\Delta i_{in,t2,t3}, \Delta i_{in,t4,t5}) \tag{2.19}$$

$$\Delta i_{in,t2,t3} = \left(\frac{2v_{in}}{L}\right) d_2 Ts \tag{2.20}$$

$$\Delta i_{in,t4,t5} = \left(\frac{(v_{o1} - v_{in})}{L} + \frac{(v_{o2} - v_{in})}{L}\right)(1 - d_1)T_s \tag{2.21}$$

where, $L_1 = L_2 = L$. Since the left-hand side and right-hand side output capacitor voltages are DC shifted sinusoidal waveforms and they are phase shifted, the duty ratio values d_1 and d_2 are changing over the time. Hence, d_1 can be greater than or equal to d_2 or less than d_2. These two situations should be analyzed separately when calculating the switching frequency ripple amplitudes. Using (2.19), (2.20), and (2.21), a general equation for the DC source switching frequency ripple amplitude when $d_1 \geq d_2$ can be written as,

$$\Delta i_{in,rip} = \begin{cases} \dfrac{2v_{in}T_s d_2}{L} & \text{if } d_2 \geq 0.5 \\ \left|\dfrac{v_{in}T_s}{L}\left(\dfrac{d_1 + d_2 - 2d_1 d_2}{1 - d_2}\right)\right| & \text{if } d_2 < 0.5. \end{cases} \tag{2.22}$$

Similarly, when $d_2 > d_1$,

$$\Delta i_{in,rip} = \begin{cases} \dfrac{2v_{in}T_s d_1}{L} & \text{if } d_1 \geq 0.5 \\ \left|\dfrac{v_{in}T_s}{L}\left(\dfrac{d_1 + d_2 - 2d_1 d_2}{1 - d_1}\right)\right| & \text{if } d_1 < 0.5. \end{cases} \tag{2.23}$$

2.3.2 Phase Shifted Interleaved Operation

Interleaving is a popular concept, which is used to reduce the switching frequency ripple component of power converter input current [80, 81]. In a conventional interleaved boost DC/DC converter configuration, N number of boost converter modules are connected in parallel so that all the converters have the same input voltage and the same output voltage. Moreover, the duty ratio and the switching frequency are same for all the parallel power converters. The PWM signals for the converters are phase shifted by $2\pi/N$ rad and hence,

the inductor current ripple components are also phase shifted, and when summed, the current ripples partially cancel each other, resulting in a lower input current ripple. As a result, the maximum input current ripple equals to $1/_N$ times the inductor current ripple of each boost converter module.

In this research, the interleaving concept is applied to the boost inverter topology to reduce the high frequency ripple component of the DC source current. Before studying the interleaved operation for the boost inverter topology, it is worth to consider the differences between the traditional interleaved boost DC/DC converter operation and the interleaved boost inverter operation.

In the traditional interleaved DC/DC boost converter, the boost converter modules are connected in parallel and hence, all the modules have the same input voltage and the same output voltage, and the modules operate with the same duty ratio value. However, in the boost inverter topology, both left-hand side and right-hand side boost converter legs have the same input voltage v_{in}, but different output capacitor voltages, v_{o1} and v_{o2}. The two boost converter legs operate at different duty ratio values and hence, a detailed analysis on the boost inverter phase-shifted operation is required.

Analysis of the switching frequency ripple component of the interleaved-boost inverter DC source current depends on the summation of two duty ratio components, d_1 and d_2. Since two boost converter legs are connected to the DC source, relevant PWM signals are phase shifted by 180° from each other. Assuming that $v_{L1,2} = 0$, (i.e. neglecting losses and energy stored in the inductor), the sum of the two duty ratios can be approximated as,

$$d_1 + d_2 = \frac{v_{o1} - v_{in}}{v_{o1}} + \frac{v_{o2} - v_{in}}{v_{o2}}. \tag{2.24}$$

***Case 1*:** $d_1 + d_2 \geq 1$

Using (2.24), (2.1), (2.2), and (2.3), condition for *Case1* can be written as,

$$d_1 + d_2 = \frac{V_{DC} + \frac{V_o}{2}sin(\omega t + \delta) - v_{in}}{V_{DC} + \frac{V_o}{2}sin(\omega t + \delta)} + \frac{V_{DC} - \frac{V_o}{2}sin(\omega t + \delta) - v_{in}}{V_{DC} - \frac{V_o}{2}sin(\omega t + \delta)} \geq 1. \tag{2.25}$$

By simplifying (2.25)

$$2V_{DC}^2 - 4v_{in}V_{DC} + \left(\frac{V_o}{2}\right)^2 cos(2\omega t + \delta) \geq 0. \tag{2.26}$$

If the DC shift of the output capacitor voltages satisfies (2.27), the total operating region of the boost inverter can be defined by *Case 1*.

$$V_{DC} \geq v_{in} + \sqrt{v_{in}^2 + \left(\frac{V_o}{2}\right)^2} \tag{2.27}$$

Fig. 2.6 depicts the gate signals and current waveforms related to the *Case 1*. The center of the logic high region of $Sw_{1,B}$ gate signal is aligned with the center of the logic low region of $Sw_{2,B}$ gate signal and illustrates the 180° phase shift between the two gate signals.

From t_1 to t_2, both switches $Sw_{1,B}$ and $Sw_{2,B}$ are ON. Hence, both the inductor currents and the DC source current are increasing.

From t_2 to t_3, $Sw_{1,B}$ is ON while $Sw_{2,B}$ is OFF, resulting in increasing inductor current i_{L1} while decreasing inductor current i_{L2}. However, the resulting DC source current can either increase or decrease depending on i_{L1} and i_{L2}. Fig. 2.6 shows the DC source current increase from t_2 to t_3.

From t_3 to t_4, the inductor currents and the DC source current are increasing since both switches are turned ON.

From t_4 to t_5, i_{L1} is decreasing as $Sw_{1,B}$ is OFF and i_{L2} is increasing as $Sw_{2,B}$ is ON. The total DC source current can either increase or decrease as explained earlier. Equations (2.16)-(2.19) are valid for *Case 1* as well where,

$$\Delta i_{in,t2,t3} = \left(\frac{v_{in}}{L} - \frac{v_{in}}{L}\left(\frac{d_2}{1-d_2}\right)\right)(1-d_2)T_s \tag{2.28}$$

$$\Delta i_{in,t4,t5} = \left(\frac{v_{in}}{L} - \frac{v_{in}}{L}\left(\frac{d_1}{1-d_1}\right)\right)(1-d_1)T_s. \tag{2.29}$$

Using (2.19), (2.28), and (2.29), a general equation for the interleaved operation DC source current switching frequency ripple for the *Case 1* can be written as,

$$\Delta i_{in,rip} = \begin{cases} \dfrac{v_{in}T_s(2d_2-1)}{L} & \text{if } d_2 \geq d_1 \\ \dfrac{v_{in}T_s(2d_1-1)}{L} & \text{if } d_2 < d_1. \end{cases} \tag{2.30}$$

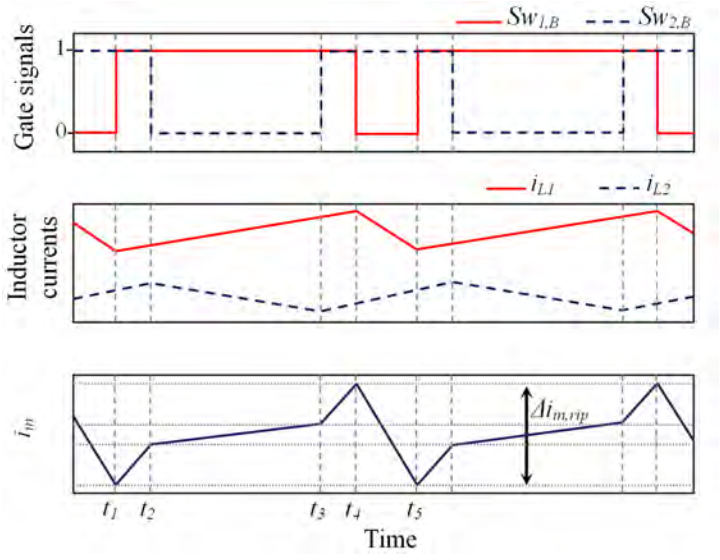

Fig. 2.6: Ripple current waveforms for interleaved operation when $d_1 + d_2 \geq 1$

The maximum switching frequency ripple amplitude of the DC source current for *Case 1*, $max(\Delta i_{in,rip})_{Case1}$can be obtained as,

$$max(\Delta i_{in,rip})_{Case1} = \frac{v_{in}T_s}{L}(2d_{max} - 1) \tag{2.31}$$

where d_{max} is the maximum duty ratio of the boost inverter which corresponds to the maximum voltage across the output capacitors.

***Case 2*:** $d_1 + d_2 < 1$

Fig. 2.7 illustrates the relevant gate signals and the current waveforms for the *Case 2*. From t_1 to t_2, both switches are OFF and hence both inductor currents are decreasing and a decrement in the total DC source current can be observed.

From t_2 to t_3, $Sw_{1,B}$ is OFF while $Sw_{2,B}$ is ON. Hence, i_{L2} is increasing while i_{L1} is decreasing. The DC source current will increase or decrease depending on the i_{L1} and i_{L2}. Fig. 2.7 illustrates the situation where the DC source current is decreasing.

From t_3 to t_4, again both switches are OFF and the current waveforms are decreasing.

From t_4 to t_5, $Sw_{1,B}$ is ON and $Sw_{2,B}$ is OFF. Hence, i_{L1} is increasing while i_{L2} is decreasing. The total DC source current will either increase or decrease as explained earlier.

Similar to *Case 2*, the analysis provide in equations (2.16)-(2.19) are valid for the *Case 2* as well, where,

$$\Delta i_{in,t2,t3} = \left(\frac{v_{in}}{L} - \frac{d_1}{(1-d_1)}\frac{v_{in}}{L}\right) d_2 T_s \tag{2.32}$$

$$\Delta i_{in,t4,t5} = \left(\frac{v_{in}}{L} - \frac{d_2}{(1-d_2)}\frac{v_{in}}{L}\right) d_1 T_s. \tag{2.33}$$

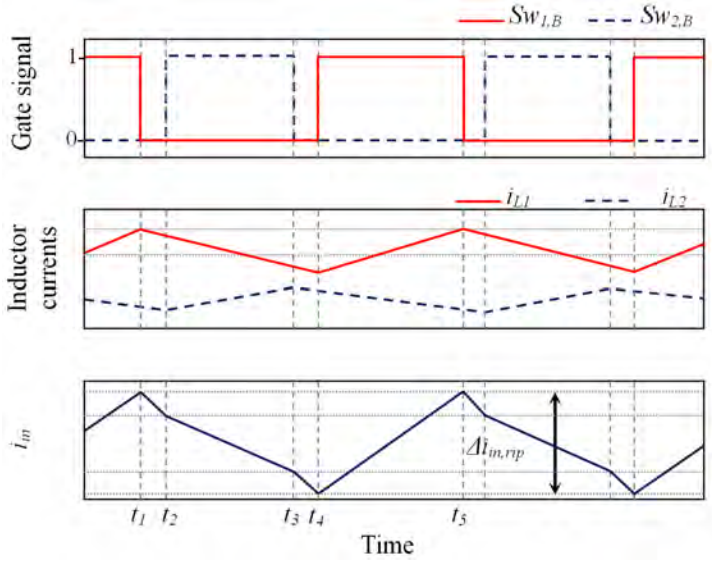

Fig. 2.7: Ripple current waveforms for interleaved operation when $d_1 + d_2 < 1$

Using, (2.19), (2.32), and (2.33), the DC source switching frequency ripple amplitude with the interleaved operation for the case $d_1 + d_2 < 1$ can be written as,

$$\Delta i_{in,rip} = \begin{cases} \frac{v_{in}T_s}{L}\frac{d_1(1-2d_2)}{(1-d_2)} & \text{if } d_1 \geq d_2 \\ \frac{v_{in}T_s}{L}\frac{d_2(1-2d_1)}{(1-d_1)} & \text{if } d_1 < d_2. \end{cases} \tag{2.34}$$

The maximum switching frequency ripple amplitude of the DC source current for *Case 2*, $max(\Delta i_{in,rip})_{Case2}$ is given by,

$$max(\Delta i_{in,rip})_{Case2} = \frac{v_{in}T_s}{L}\frac{d_{max}(1-2_{dmin})}{(1-d_{min})} \tag{2.35}$$

where d_{max} is the maximum duty ratio of the boost inverter which corresponds to the maximum voltage across the output capacitors and d_{min} is the minimum duty ratio of the boost inverter which corresponds to the minimum voltage across the output capacitors.

2.3.3 Boost Inverter Component Selection with the Interleaved Operation

The required inductors for the interleaved boost inverter can be selected to limit the switching frequency ripple amplitude of the DC source current. Once the DC source voltage v_{in}, the inverter output voltage amplitude V_o and the required output capacitor DC shift V_{DC} are determined, the maximum and the minimum duty ratio values of the boost inverter can be calculated as,

$$d_{max} = \frac{v_{o1,max} - v_{in}}{v_{o1,max}} = \frac{V_{DC} + \frac{V_o}{2} - v_{in}}{V_{DC} + \frac{V_o}{2}} \tag{2.36}$$

$$d_{max} = \frac{v_{o1,min} - v_{in}}{v_{o1,min}} = \frac{V_{DC} - \frac{V_o}{2} - v_{in}}{V_{DC} - \frac{V_o}{2}}. \tag{2.37}$$

Then, the required minimum inductor value to limit the DC source current switching frequency ripple amplitude to $max(\Delta i_{in,rip})$ can be calculated as,

$$L_{min} = \begin{cases} \frac{v_{in}T_s}{max(\Delta i_{in,rip})}(2d_{max} - 1) & \text{for } \textit{Case 1} \\ \frac{v_{in}T_s}{max(\Delta i_{in,rip})}\frac{d_{max}(1-2_{dmin})}{(1-d_{min})} & \text{for } \textit{Case 2} \ . \end{cases} \tag{2.38}$$

For both in-phase PWM operation and interleaved operation, the switching frequency ripple amplitudes $\Delta v_{o1,rip}$ and $\Delta v_{o2,rip}$ of the output capacitor voltages v_{o1} and v_{o2} are determined by the output capacitor values. The switching frequency voltage ripple amplitude of v_{o1} is given by,

$$\Delta v_{o1,rip} = \frac{I_{o,max}d_{1,max}T_s}{C_1}. \tag{2.39}$$

Then using the maximum allowable switching frequency ripple amplitude in the output capacitor voltage, $max(\Delta v_{o1,rip})$, the required minimum output capacitor value $C_{1,min}$ can be calculated as,

$$C_{1,min} = \frac{I_{o,max} T_s}{max(\Delta v_{o1,rip})} \left(\frac{V_{DC} + \frac{V_o}{2} - v_{in}}{V_{DC} + \frac{V_o}{2}} \right). \tag{2.40}$$

2.3.4 Comparison Between the In-Phase PWM Operation and the Interleaved Operation

A comparison of the DC source current switching frequency ripple amplitude with in-phase PWM operation and with the interleaved operation is illustrated in Fig. 2.8. Parameters of the considered boost inverter are summarized in Table 2.1. A DL control strategy as explained in [55] is used to control the boost inverter. Fig. 2.8 (a) illustrates the output capacitor voltage waveforms. Figs. 2.8 (b) and 2.8 (c) illustrate the DC source current waveforms with the in-phase PWM operation and with the interleaved operation, respectively. Fig. 2.8 (d) compares the switching frequency ripple current amplitude for the two operating methods. A significant reduction in the switching frequency ripple amplitude can be observed with the interleaved operation. A switching frequency ripple reduction factor R_{sf} is defined as (2.41) to compare the performance of the two configurations.

$$R_{sf} = \frac{\Delta i_{in,rip(In-phasePWM)}}{\Delta i_{in,rip(Interleaved)}} \tag{2.41}$$

During the interleaved operation, the DC source switching frequency current ripple component is reduced at least 1.6 times compared to the in-phase PWM operation.

2.4 Conclusions

Boost inverter topology enables the integration of low voltage DC sources to a single phase grid by providing both boosting and inversion functions in a single power processing

Table 2.1: Boost inverter parameters

Parameter	**Value**	**Parameter**	**Value**
V_o	40 V	V_{DC}	40 V
v_{in}	12.8 V	C_1,C_2	60 uF
L_1,L_2	1 mH	f	50 Hz
T_s	50 us	R_{L1}, R_{L2}	0.24Ω
R_{C1}, R_{C2}	0.01 Ω		

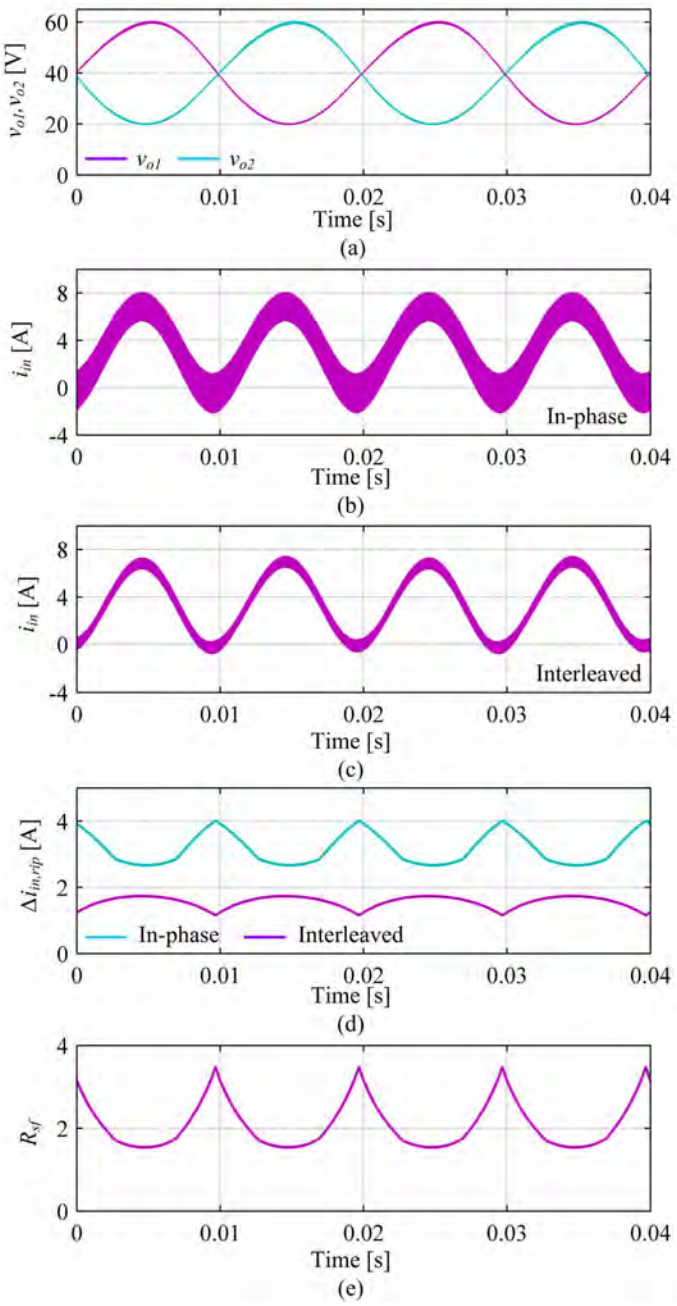

Fig. 2.8: Switching frequency ripple current amplitude comparison with the interleaved and in-phase PWM operation. (a) Output capacitor voltage waveforms, (b) DC source current waveform with in-phase PWM operation, (c) DC source current with interleaved operation, (d) DC source current switching frequency ripple amplitude and (e) ripple reduction factor.

stage.

It was shown that the conventional in-phase PWM operation of the boost inverter leads to a higher switching frequency ripple component in the DC source current due to the addition of the ripple components of the two inductor currents. The switching frequency ripple current component increases the internal heating of the DC source and

adversely affects its lifetime.

In this chapter, a novel phase-shifted PWM operation for the boost inverter topology was presented. A detailed analysis on the switching frequency ripple current amplitude with the in-phase PWM operation and with the phase-shifted interleaved operation was presented. Furthermore, the component selection for the proposed interleaved boost inverter was discussed. The proposed interleaved operation achieved a significant switching frequency ripple component reduction in the DC source current. The reduction in the switching frequency ripple amplitude helps to reduce the internal heating of the boost inverter DC power source.

Chapter 3

Interleaved Boost Inverter Based Battery-Supercapacitor Hybrid Energy Storage System

This chapter presents the proposed interleaved boost inverter based battery-supercapacitor HESS [64]. The interleaved operation reduces the switching frequency component of the battery and the supercapacitor currents and helps to reduce the internal heating of both the battery and the supercapacitor. Section 3.3 presents the proposed HESS control system which allocates the fast power variations to the supercapacitor while the battery supplies the slow varying power component. A high pass filter based power allocation method is used where the second-order harmonic ripple current component is allocated to the supercapacitor. A supercapacitor voltage controller (SCVC) is employed to reduce the risk of supercapacitor over-charging and over-discharging by maintaining its voltage around a reference voltage level. An Extended Kalman filter based battery SOC estimator is designed for the selected battery module. The proposed system is able to satisfy the output power requirements while operating within the battery and the supercapacitor SOC limits. The proposed battery-supercapacitor HESS is able to increase the battery lifetime by reducing the battery current fluctuations and peak currents. The proposed boost inverter based HESS is the first experimentally verified single phase direct grid integrated battery-supercapacitor HESS available in the literature.

3.1 Introduction

Boost inverter topology provides means of DC source grid integration by providing both boosting and inversion functions in a single power processing stage [55]. Chapter 2 presented the basic operating principles of a grid connected boost inverter system. Furthermore, a detailed analysis on the in-phase PWM operation of the boost inverter was provided and an interleaved operation for the boost inverter topology was proposed to reduce the DC source switching frequency current component.

In this chapter, an interleaved boost inverter based single phase grid connected battery-supercapacitor HESS is proposed [64]. The interleaved operation helps to reduce the switching frequency ripple component of both the battery and the supercapacitor currents. None of existing battery-supercapacitor HESSs considered the switching frequency ripple reduction in the DC source currents. The proposed controller for the HESS is presented in Section 3.3. The controller contains two double loop (DL) controllers to control the left hand side and the right hand side boost converter legs. A high pass filter based power allocation method is employed to allocate the fast power fluctuations to the supercapacitor. The high pass filter allocates the second-order harmonic current component to the supercapacitor since such ripple current component adversely affect the battery lifetime due to internal heating [13] Since it is important to avoid supercapacitor over-charging and over-discharging, a SCVC is used. An active and reactive power controller is implemented using the droop control theory to control the power exchange between the grid and the HESS as presented in Subsection 3.3.2. A second order nonlinear RC battery model used to model the $LiFePO_4$ battery and an extended Kalman filter based battery SOC estimation method are described in Section 3.4. A battery SOC controller is implemented to ensure the operation of the battery within a safe operating region. The operation of the interleaved boost inverter based battery-supercapacitor HESS is validated using experimental results obtained from a laboratory HESS prototype in Section 3.5.

3.2 Boost Inverter Based Battery- Supercapacitor Hybrid Energy Storage System

The system configuration of the boost inverter based single phase grid connected battery-supercapacitor HESS is shown in Fig. 3.1. The configuration contains two boost inverters one for the battery and one for the supercapacitor. Each boost inverter has two boost converter legs; namely the left hand side boost converter leg (subscript 1) and the right hand side boost converter leg (subscript 2).

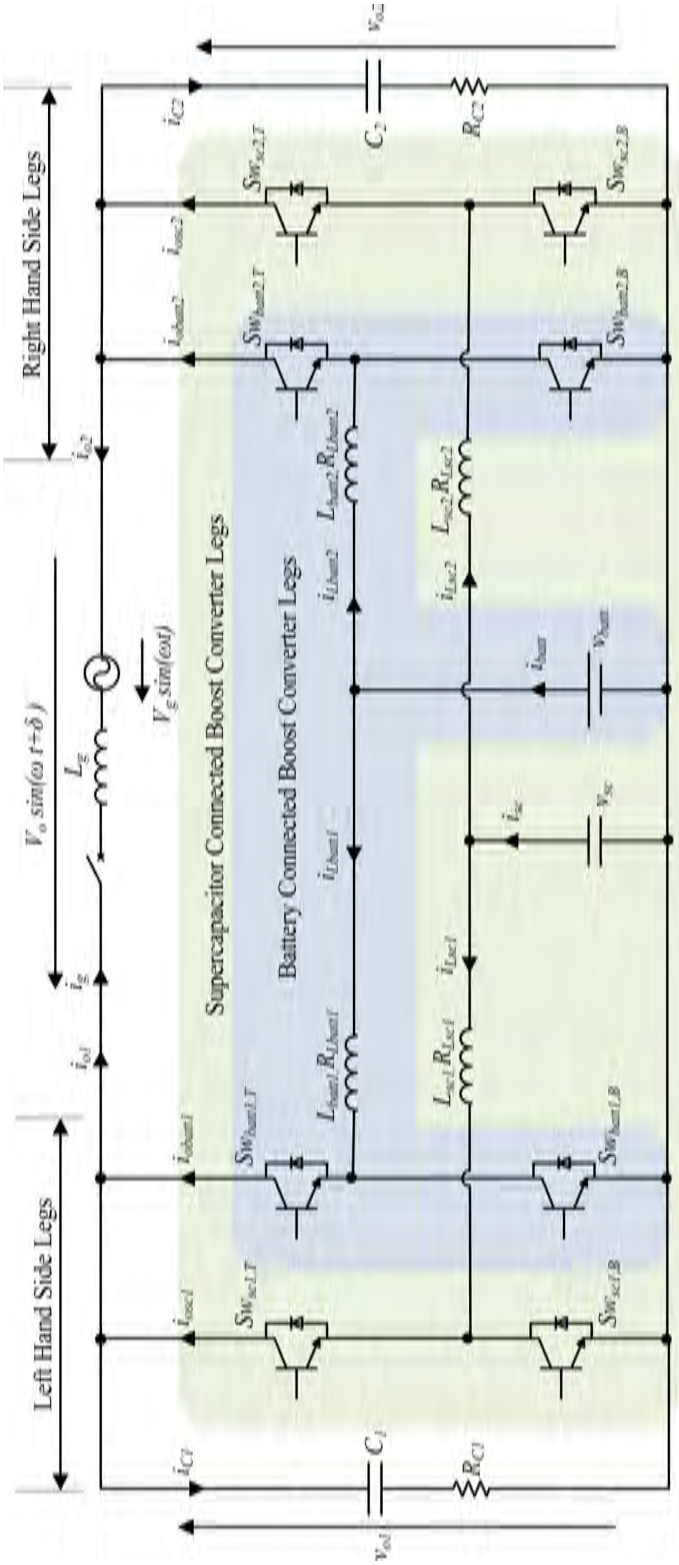

Fig. 3.1: Single phase grid connected battery-supercapacitor hybrid energy storage system

Dynamic behavior of the boost converter legs can be described by the boost converter average model. The model equations for the left-hand-side boost converter legs can be expressed as follows:

$$v_{sc} - v_{Lsc1} = (1 - d_{sc1})v_{o1} \tag{3.1}$$

$$v_{batt} - v_{Lbatt1} = (1 - d_{batt1})v_{o1} \tag{3.2}$$

$$i_{C1} + i_{o1} = (1 - d_{batt1})i_{Lbatt1} + (1 - d_{sc1})i_{Lsc1} \tag{3.3}$$

where v_{o1} and i_{C1} are the voltage and current of the output capacitor C_1, and v_{Lbatt1} and i_{Lbatt1} are the voltage and current of the inductor L_{batt1}, respectively. v_{Lsc1} and i_{Lsc1} are the voltage and the current of the inductor L_{sc1}, and v_{batt} and v_{sc} are the battery voltage and the supercapacitor voltage, respectively. Duty cycle time average values of the gate signals for the switches $Sw_{batt1,B}$ and $Sw_{sc1,B}$ are denoted as d_{batt1} and d_{sc1}, respectively. i_{o1} is the output current from the left hand side boost converter legs. The inductor and capacitor differential equations can be written as,

$$L_{batt1}\frac{di_{Lbatt1}}{dt} = v_{Lbatt1} - R_{Lbatt1}i_{Lbatt1} \tag{3.4}$$

$$L_{sc1}\frac{di_{Lsc1}}{dt} = v_{Lsc1} - R_{Lsc1}i_{Lsc1} \tag{3.5}$$

$$C_1\frac{dv_{o1}}{dt} = i_{C1} + R_{C1}C_1\frac{di_{C1}}{dt} \tag{3.6}$$

where R_{C1}, R_{Lbatt1}, and R_{Lsc1} are the ESR values of the capacitor C_1 and the inductors L_{batt1} and L_{sc1}, respectively.

3.3 Control System Description

3.3.1 Power Converter Control Strategy

The overall block diagram of the HESS controller is illustrated in Fig.3.2. The objective of the HESS controller is to maintain the inverter output voltage such that the HESS fulfills the active and reactive power requirements. Additionally, the controller has to allocate the second-order harmonic ripple component and fast power fluctuations to the supercapacitor. Further, the controller has to maintain the SOC of the battery and the supercapacitor within a safe operating region to ensure safe and sustainable operation of the HESS.

The HESS output voltage has to follow a sinusoidal reference voltage,

$$v_{o,ref} = V_o \sin(\omega t + \delta) \tag{3.7}$$

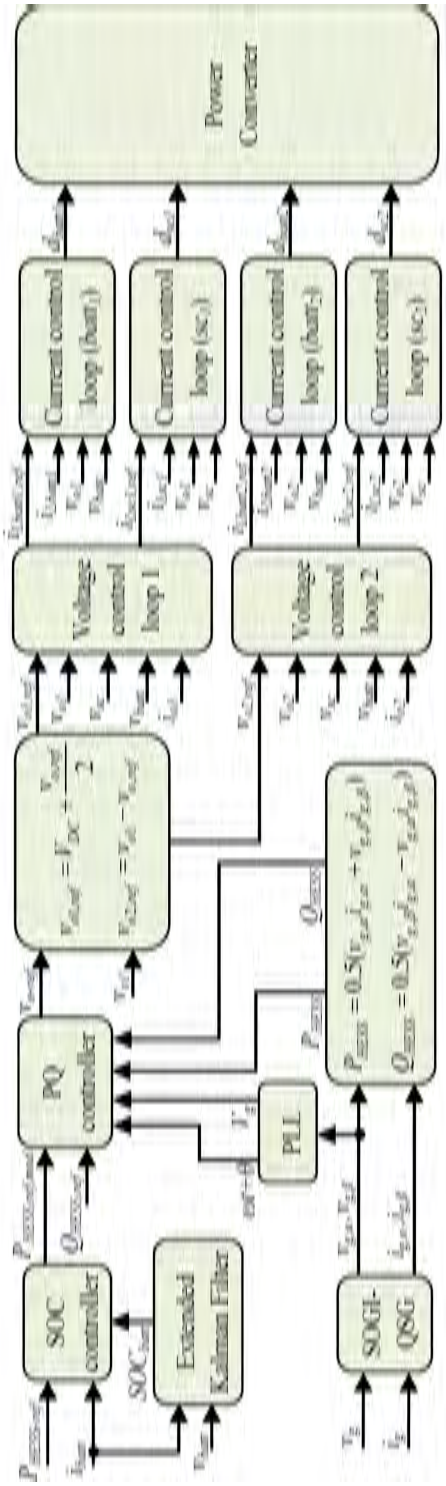

Fig. 3.2: Overall block diagram of the proposed controller.

where the HESS output voltage amplitude, frequency, and phase angle with respect to the grid voltage are denoted as V_o, ω, and δ, respectively. In order to obtain the required HESS differential output voltage, the left hand side and the right hand side boost converter legs are required to follow voltage references $v_{o1,ref}$ and $v_{o2,ref}$ across the output capacitors C_1 and C_2.

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2}\sin(\omega t + \delta) \tag{3.8}$$

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2}\sin(\omega t + \delta) \tag{3.9}$$

The DC shift of the output capacitor reference voltages $v_{o1,ref}$ and $v_{o2,ref}$ is selected as,

$$V_{DC,ref} \geq v_{in} + \frac{V_o}{2} \tag{3.10}$$

where v_{in} is the input voltage to the boost converter legs (v_{batt} or v_{sc}). In order to achieve direct control over the HESS output voltage v_o, the voltage v_{o2} across the capacitor C_2 can be controlled using (3.11) as mentioned in Chapter 2.

$$v_{o2,ref} = v_{o1} - v_{o,ref} \tag{3.11}$$

Two DL controllers are used to control the left hand side and right hand side boost converter legs. Each DL controller has two inner current control loops and an outer voltage control loop. The objective of the voltage control loop for the left hand side boost converter legs is to generate such inductor current reference signals for the current control loops that, 1) maintain the reference voltage v_{o1}, 2) allocate the high frequency current variations to the supercapacitor, 3) maintain the supercapacitor voltage around a pre-defined reference voltage, and 4) supply the initial supercapacitor charging current from the battery. The block diagram of the outer voltage control loop and the inner current control loops for the left hand side boost converter legs is illustrated in Fig. 3.3 where,

$$H_{Lsc1}(s) = \frac{1}{(R_{Lsc1} + L_{sc1}s)} \tag{3.12}$$

$$H_{Lbatt1}(s) = \frac{1}{(R_{Lbatt1} + L_{batt1}s)} \tag{3.13}$$

$$H_{C1}(s) = \frac{1 + R_{C1}C_1 s}{C_1 s} \tag{3.14}$$

The voltage and current measurements are filtered using low pass filters as shown in Fig. 3.3 where T_F is filter parameter.

A proportional resonant (PR) controller with a transfer function $H_{PR}(s)$ is used in the voltage control loop to achieve better sinusoidal tracking performance.

$$H_{PR}(s) = K_{p,PR} + \frac{2sK_{i,PR}}{s^2 + \omega^2} \tag{3.15}$$

where $K_{p,PR}$ and $K_{i,PR}$ are constants and ω is the frequency of the output voltage in rad/s.

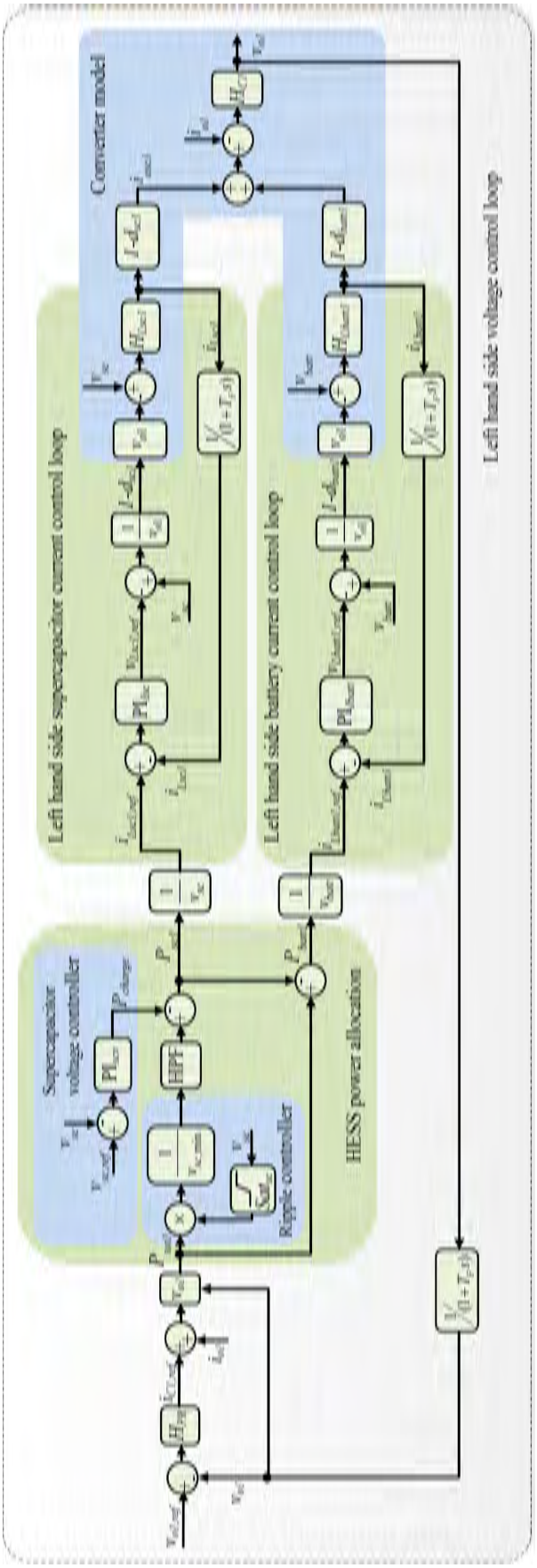

Fig. 3.3: Block diagram of the left hand side outer voltage control loop and inner current control loops.

The total instantaneous power requirement from the left hand side boost converter legs is given by P_{tot1}. A high pass filter with a cut off frequency ω_{HPF} is employed to divert the second-order harmonic ripple component and fast power fluctuations to the supercapacitor while battery supplies the slow varying power requirement.

The supercapacitor tends to fully discharge or fully charge during the operation of the HESS, if the supercapacitor voltage is not maintained around a reference voltage value [29]. Hence, a PI controller is implemented to maintain the supercapacitor voltage around a pre-defined reference voltage $v_{sc,ref}$. Additionally, the controller compensates for the supercapacitor self-discharging. By selecting the supercapacitor operating voltage range between 50% and 100% of its rated voltage $v_{sc,max}$, 75% of the overall supercapacitor stored energy can be utilized [19]. Then the supercapacitor reference voltage $v_{sc,ref}$ is selected such that equal amount of energy is available above and below the reference level for future power delivering or absorbing situations [18].

A constant saturation block Sat_{sc} (see Fig. 3.3) based ripple current controller is used to allocate the ripple current to the battery, when the supercapacitor voltage is less than a pre-defined voltage $v_{sc,min}$. The constant saturation block saturates at the voltage $v_{sc,min}$ and if the supercapacitor voltage is less than $v_{sc,min}$, the ripple current controller allocates a fraction of the ripple current to the battery. In the initial supercapacitor charging process, the total required current and the supercapacitor charging current are supplied by the battery and as the supercapacitor gets charged, the ripple current is gradually allocated to the supercapacitor.

The PR controller for the outer voltage control loop is designed to achieve 400 Hz bandwidth and the PI controllers for the inner current control loops are implemented with 4 kHz bandwidth. These values enable the accurate tracking of 50 Hz reference voltages. The Bode diagram of the outer voltage control loop is shown in Fig. 3.4 (a). The Bode diagrams of the inner current control loops for the left hand side battery connected boost converter leg and for the left hand side supercapacitor connected boost converter leg are illustrated in Figs. 3.4 (b) and 3.4 (c), respectively.

The SCVC has to suppress the low frequency voltage errors and at the same time it has to be insensitive to high frequency errors so that it will not affect the smoothness of the battery current. For this reason, SCVC is designed to have 0.01Hz crossover frequency as shown in Fig. 3.4 (d).

3.3.2 Hybrid Energy Storage System Grid Integration

The HESS is connected to the grid through an interfacing inductor as shown in Fig. 3.1. The active power and the reactive power delivered from the HESS to the grid are denoted

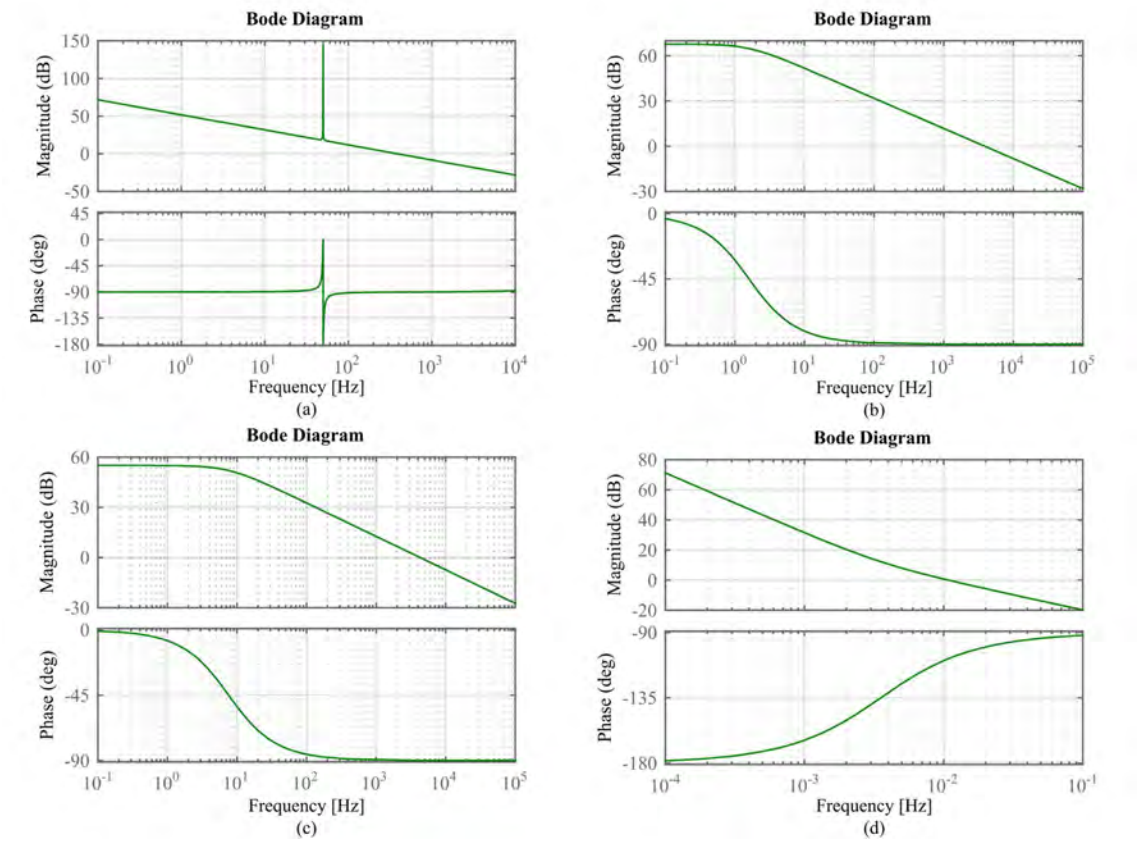

Fig. 3.4: Bode diagrams of the HESS controller. (a) Open loop Bode plot of the left hand side voltage control loop, (b) open loop Bode plot of the current control loop for the left hand side battery connected boost converter leg, (c) open loop Bode plot of the current control loop for the left hand side supercapacitor connected boost converter leg and (d) open loop Bode plot of the SCVC.

as P_{HESS} and Q_{HESS}. For small δ values, P_{HESS} and Q_{HESS} can be approximated as,

$$P_{HESS} \approx \frac{V_g V_o}{2\omega L_g}\delta \tag{3.16}$$

$$Q_{HESS} \approx \frac{V_g(V_o - V_g)}{2\omega L_g} \tag{3.17}$$

Hence, by proper control of the inverter output voltage amplitude and phase-angle with respect to the grid voltage, the active and reactive power exchange between the grid and the HESS can be achieved. Furthermore, the fast and accurate measurement of the active and reactive power is essential to achieve an accurate power exchange between the grid and the HESS. P_{HESS} and Q_{HESS} can be calculated using orthogonal components of the grid voltage and current at the point of common coupling (PCC) as [78],

$$P_{HESS} = \frac{1}{2}(v_{g,\alpha} i_{g,\alpha} + v_{b,\beta} i_{g,\beta}) \tag{3.18}$$

$$Q_{HESS} = \frac{1}{2}(v_{g,\beta} i_{g,\alpha} - v_{g,\alpha} i_{g,\beta}) \tag{3.19}$$

where $v_{g,\alpha}$, $v_{g,\beta}$, and $i_{g,\alpha}$, $i_{g,\beta}$ are the orthogonal components of the instantaneous grid voltage and current at the PCC, respectively. The orthogonal components are generated using a second order generalized integrator based quadrature signal generator (SOGI-QSG) [82]. Two PI controllers are designed based on (3.16) and (3.17) to control the active and reactive power delivered to the grid by controlling the inverter output voltage amplitude and phase angle with respect to the grid voltage. The block diagram of the active and reactive power PI controllers along with the battery SOC controller, which will be described in Section 3.4 are illustrated in Fig.3.5. The PI controllers are designed to achieve rise time less than 0.1s for better reference following.

3.4 Battery State of Charge Estimation and Control

3.4.1 Battery Model

A Lithium iron phosphate ($LiFePO_4$) battery by K2 Energy with 6.4Ah capacity and 12.8V rated voltage is used in the experimental setup. A suitable battery model for the selected battery should be identified to design a battery SOC estimation algorithm. Various types of battery models have been studied in the literature depending on the battery chemistry. A second-order RC battery model shown in Fig. 3.6, which is proven to be a suitable battery model for $LiFePO_4$ batteries is selected for the SOC estimation algorithm [83]. The effects of temperature on battery SOC estimation are not considered

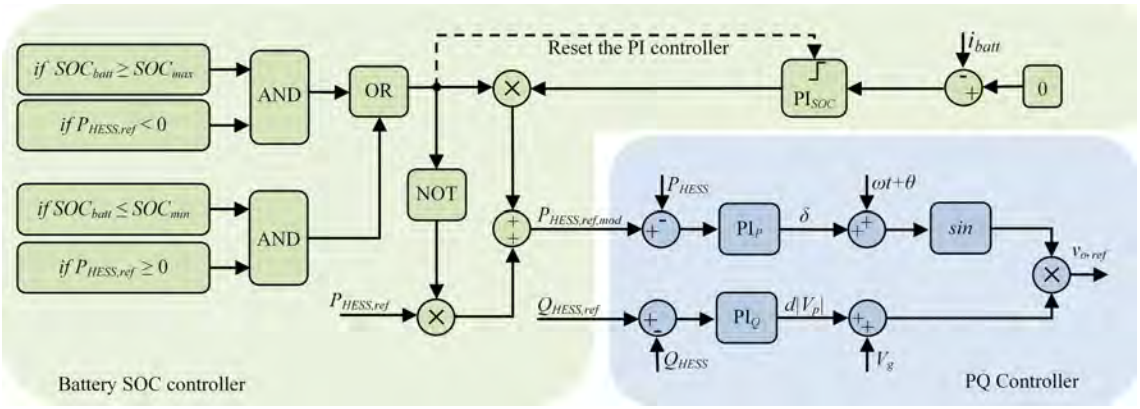

Fig. 3.5: Active and reactive power controller (PQ controller), and battery SOC controller

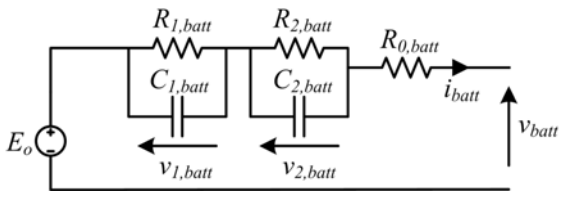

Fig. 3.6: Second order RC battery model

in this thesis. The battery open circuit voltage (OCV), E_o is a nonlinear function of the battery SOC, SOC_{batt} and can be written as,

$$E_o = f(SOC_{batt}). \tag{3.20}$$

From the RC battery model, following equations can be written.

$$v_{batt} = E_o - v_{1,batt} - v_{2,batt} - i_{batt}R_{0,batt} \tag{3.21}$$

$$i_{batt} = \frac{v_{1,batt}}{R_{1,batt}} + C_{1,batt}\frac{dv_{1,batt}}{dt} = \frac{v_{2,batt}}{R_{2,batt}} + C_{2,batt}\frac{dv_{2,batt}}{dt} \tag{3.22}$$

where $R_{0,batt}$, $R_{1,batt}$, $R_{2,batt}$, $C_{1,batt}$, and $C_{2,batt}$ are the battery internal parameters which reflect the battery dynamic response. $v_{1,batt}$ and $v_{2,batt}$ are the voltages across the capacitors $C_{1,batt}$ and $C_{2,batt}$, respectively. Then the state space equations for the considered battery model can be written as (23) by selecting the capacitor voltage drops and the battery SOC as the state variables.

$$\dot{x} = \begin{bmatrix} \frac{-1}{R_{1,batt}C_{1,batt}} & 0 & 0 \\ 0 & \frac{-1}{R_{2,batt}C_{2,batt}} & 0 \\ 0 & 0 & 0 \end{bmatrix} x \times \begin{bmatrix} \frac{1}{C_{1,batt}} \\ \frac{1}{C_{2,batt}} \\ -\eta \end{bmatrix} i_{batt} \tag{3.23}$$

where $x = \begin{bmatrix} v_{1,batt} & v_{2,batt} & SOC_{batt} \end{bmatrix}^T$, $\eta = \left(\frac{1}{3600C_{batt}}\right)$, and C_{batt} is the total battery capacity in Ah. A discretized state space model of the RC battery model can be found as,

$$x_k = Ax_{k-1} + Bi_{batt.k-1} \tag{3.24}$$

where $A = \begin{bmatrix} \frac{-\Delta t}{R_{1,batt}C_{1,batt}} + 1 & 0 & 0 \\ 0 & \frac{-\Delta t}{R_{2,batt}C_{2,batt}} + 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$, $B = \begin{bmatrix} \frac{\Delta t}{C_{1,batt}} \\ \frac{\Delta t}{C_{2,batt}} \\ -\eta\Delta t \end{bmatrix}$, and Δt is the sampling interval.

3.4.2 Battery Model Parameter Estimation

In this section, the relationship between the battery OCV and the battery SOC, and the battery RC model parameter estimation are presented.

The relationship between the battery OCV and the battery SOC is identified by conducting a battery charge and discharge test as explained in [83]. A 3A, 14.4V $LiFePO_4$ battery charger from Fuyuan and a PLZ1004WH Kikusui DC electronic load are used to charge and discharge the $LiFePO_4$ battery. For the charge test, the battery is charged from 0% SOC to 100% SOC using C/2 charge pulses which last for 5min, followed by a rest period of 45 min which allows the battery to reach the charge equilibrium condition

before applying the next cycle. The battery terminal voltage is measured after each rest period. In the discharge test, the battery is discharged from 100% SOC to 0% SOC by using 1C discharge pulses which last for 5min followed by a 45min rest period. After each rest period, the battery terminal voltage is measured. It is assumed that the measured battery terminal voltage values can be considered as the battery OCV at each time instant since the battery is in the charge equilibrium condition [83]. The measured voltage values at different SOC values are plotted in Fig. 3.7. It can be observed that the charging OCV curve is different from the discharging OCV curve. Hence, the average OCV values are considered, and a monotonically increasing approximated OCV curve as shown in Fig. 3.7 is used for future calculations. The approximated OCV curve can be represented by a seventh order polynomial equation as

$$E_o = a_1 SOC_{batt}^7 + a_2 SOC_{batt}^6 + a_3 SOC_{batt}^5 + a_4 SOC_{batt}^4 + a_5 SOC_{batt}^3 + \\ + a_6 SOC_{batt}^2 + a_7 SOC_{batt}^1 + a_8 \quad (3.25)$$

The curve parameters can be obtained by curve fitting using least square method as a_1=-41.263, a_2=203.702, a_3=-393.99, a_4=384.57, a_5=-200.36, a_6=52.823, a_7=-5.063, and a_8=12.99. The battery model developed using the approximated curve is able to estimate the battery SOC accurately as demonstrated later in the chapter. The battery RC model parameters are identified by conducting a battery discharge test as illustrated in Fig. 3.8. Each discharge cycle consists of 5min discharge phase and 45 min rest phase. A least square estimation technique is employed to obtain the RC model parameters as described in [83, 84] and the obtained RC model parameters are summarized in Table 3.1.

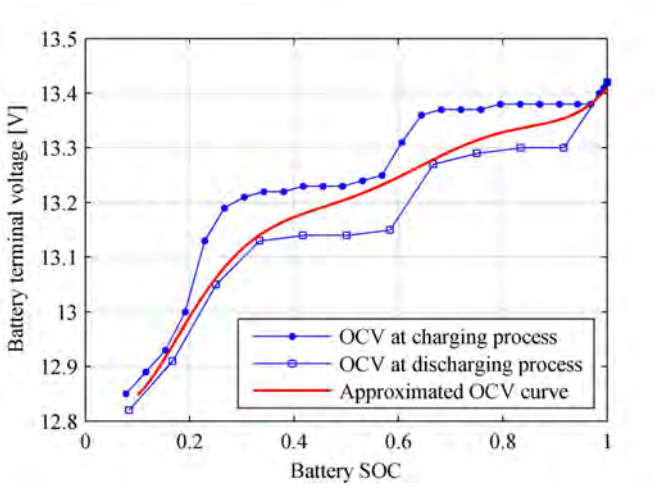

Fig. 3.7: Relationship between the battery OCV and SOC

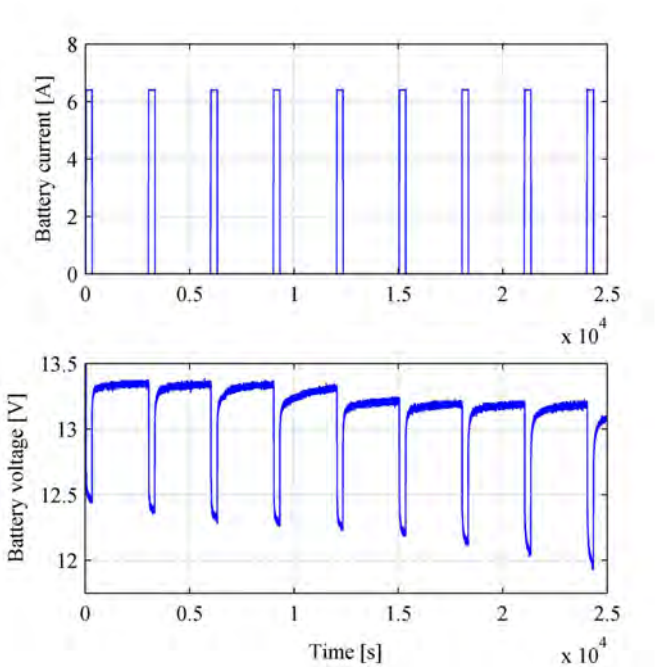

Fig. 3.8: Battery current and voltage profile for the battery RC model parameter estimation

Table 3.1: Estimated battery RC model parameters

Parameter	**Estimated Value**
$R_{0,batt}$	0.1028 Ω
$R_{1,batt}$	0.061 Ω
$R_{2,batt}$	0.008 Ω
$C_{1,batt}$	1772 F
$C_{2,batt}$	52.2 F

3.4.3 Extended Kalman Filter Based Battery SOC Estimation

Battery SOC indicates the available battery capacity as a ratio of the total battery capacity and it can be defined as,

$$SOC_{batt} = SOC_{batt,init} - \frac{\int_0^t i_{batt}(\tau)d\tau}{3600C_{batt}} \tag{3.26}$$

where $SOC_{batt,init}$ and C_{batt} are the initial battery SOC and the capacity of the battery in Ah. Knowledge of the battery SOC is important in energy storage system operation to prevent possible battery overcharging which can lead to hazardous situations or over discharging condition which can lead to battery degradation. However, battery SOC calculation using (3.26) is not practical due to possible error and noise accumulation with the integration of the battery current. [85]. Moreover, (3.26) requires the initial battery SOC which may not be available for the SOC calculation. Hence, a reliable battery SOC

estimation algorithm is vital to ensure proper and sustainable operation of the HESS.

In this research, an extended Kalman filter based battery SOC estimation method is used to accurately estimate the SOC of the battery. The battery current i_{batt} is taken as the input and the measured battery voltage v_{batt} is taken as the measured output of the Kalman filter. Then, the battery state space model can be re-written as,

$$\begin{aligned} x_{k+1} &= Ax_k + Bi_{batt,k} + w_k \\ y_k &= v_{batt,k} = E_{o,k} - v_{1,batt,k} - v_{2,batt,k} - i_{batt,k}R_{0,batt} + v_k \\ y_k &= f(SOC_{batt}) - v_{1,batt,k} - v_{2,batt,k} - i_{batt,k}R_{0,batt} + v_k = g(x_k, i_{batt,k}) + v_k \end{aligned} \tag{3.27}$$

where $g(x_k, i_{batt,k})$ is a nonlinear function. w_k and v_k are zero-mean white Gaussian processes with covariance matrices Q_{Kalman} and R_{Kalman}, respectively. To design an extended Kalman filter for the system in (3.27), a measurement matrix C_k is defined as (3.28) to linearize the nonlinear system model around the last state estimate [83, 85].

$$C_k = \left.\frac{\partial g(x_k, i_{batt,k})}{\partial x_k}\right|_{x=\hat{x}_k^-} \tag{3.28}$$

Using (3.27), (3.28) can be written as [83],

$$C_k = \begin{bmatrix} -1 & -1 & \left.\dfrac{\partial f(SOC_{batt,k})}{\partial SOC_{batt,k}}\right|_{SOC_{batt,k}=\hat{SOC}_{batt,k}^-} \end{bmatrix} \tag{3.29}$$

where superscript '∧' denotes the estimated states. The Kalman filter generates an error covariance matrix $P_{Kalman} = E\left[\tilde{x}_k\tilde{x}_k^T\right]$ where $\tilde{x}_k = x_k - \hat{x}_k$ and $E[.]$ is the statistical expectation operator. The error covariance matrix indicates the uncertainty of the estimated states. In each time step, Kalman filter produces two set of estimations for the states as well as for the error covariance matrix. The first estimation is computed before any system measurements are made and the estimate is denoted by superscript '-'. After obtaining the system measurements, Kalman filter produces updated state estimation which is denoted by superscript '+'

The extended Kalman filter is initiated by providing information about the system states and the error covariance matrix. In each time interval, the extended Kalman filter performs two steps of estimation. In the first step, the extended Kalman filter generates an expected state value at the time instant k as,

$$\hat{x}_k^- = A\hat{x}_{k-1}^+ + Bi_{batt,k-1} \tag{3.30}$$

This prediction step is known as the 'time update'. Then, the error covariance is calculated as,

$$P_{Kalman.k}^- = AP_{Kalman,k-1}^+A^T + Q_{Kalman} \tag{3.31}$$

The Kalman filter gain K_{Kalman} is calculated as,

$$K_{Kalman,k} = P^{-}_{Kalman,k} C^{T}_{k} [C_k P^{-}_{k} C^{T}_{k} + R_{Kalman}]^{-1} \tag{3.32}$$

Following the system measurements, the state estimation is updated as,

$$\hat{x}^{+}_{k} = \hat{x}^{-}_{k} + K_{Kalman,k}[y_k - g(\hat{x}^{-}_{k}, u_k)] \tag{3.33}$$

Finally, the error covariance matrix is updated as,

$$P^{+}_{Kalman,k} = (I - K_{Kalman,k} C_k) P^{-}_{Kalman,k} \tag{3.34}$$

where I is the identity matrix.

Using the above calculations, the SOC of the battery can be estimated accurately. In the designed extended Kalman filter, initial parameters are selected as follows. The measurement covariance R_{Kalman} is tuned to 1000 in order to cope with measurement errors and noises. A diagonal process covariance matrix Q_{Kalman} is selected assuming uncorrelated noises, disturbances and model imperfections. Initially, all the diagonal elements were set to a constant value and elements of the matrix are tuned by obtaining the estimated states using a real-time system. After some tuning, the process variance matrix Q_{Kalman} is selected as,

$$Q_{Kalman} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 10^{-3} \end{bmatrix} \tag{3.35}$$

A pulse discharge test is carried out to verify the performance of the extended Kalman filter based battery SOC estimation system. Fig. 3.9 compares the estimated SOC using the extended Kalman filter ($SOC_{batt,K}$) with the SOC calculated using the current integration method ($SOC_{batt,i}$).

3.4.4 Battery SOC Controller

The battery SOC has to be maintained within a safe operating region in order to eliminate possible negative impacts on the battery. The battery SOC controller illustrated in Fig. 3.5 is employed to maintain the battery operation in a safe operating region. If the battery SOC estimated using the extended Kalman filter is less than or equal to a minimum allowable level $SOC_{batt,min}$ and if the battery is continuing to discharge due to a positive or zero reference power signal, the actual reference power signal $P_{HESS,ref}$ is ignored. Then, a modified active power reference $P_{HESS,ref,mod}$ is generated using a PI controller as shown in Fig. 3.5, which maintains the total battery current at zero

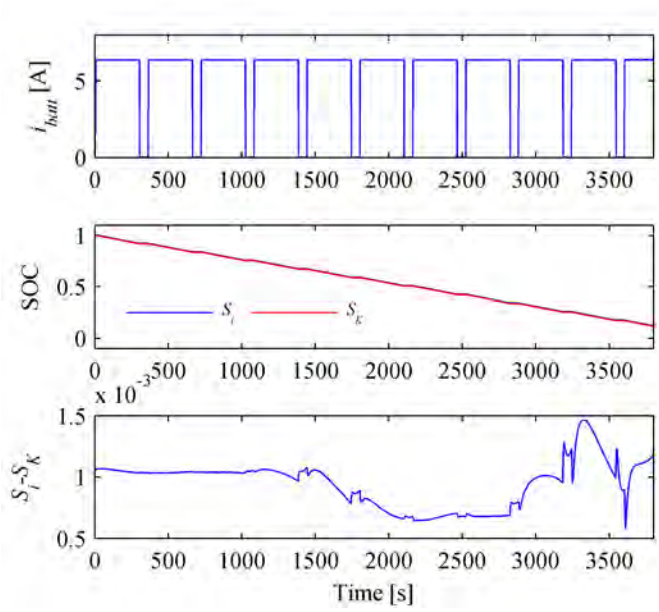

Fig. 3.9: Estimated battery SOC using the extended Kalman filter ($SOC_{batt,K}$) and the current integration method ($SOC_{batt,i}$).

avoiding the battery discharge. Similarly, if the battery SOC is greater than or equal to a maximum SOC level $SOC_{batt,max}$ and if the battery is continuing to charge due to a negative reference power signal, the SOC controller ignores the actual reference power signal and maintains the battery current at zero.

3.5 Experimental Results

The performance of the proposed interleaved boost inverter based battery-supercapacitor HESS is verified using the experimental prototype illustrated in Fig. 3.10. A 6.4Ah, 12.8V, 81.92Wh $LiFePO_4$ battery from K2 Energy and a 16V, 58F, 7424J Maxwell supercapacitor module are used in the prototype, and the parameters of the HESS prototype are summarized in Table 3.2. The power electronics converter is implemented using Semikron SEMiX 302GB066HD IGBT modules. LEM LV20 voltage sensors and LEM LA 55-P current sensors are used in the experimental setup. The HESS control system is implemented on a DSpace DS1006 system using Matlab Simulink and the control system parameters are summarized in Table 3.2. Since the experimental setup is a low voltage prototype, the grid integration of the HESS is achieved through a step-up transformer.

Fig. 3.11 depicts the HESS output voltage, grid voltage and current at the PCC when the HESS delivers 30W active power to the grid. It can be observed the active and reactive power control is achieved by modifying the HESS output voltage amplitude and

phase angle with respect to the grid voltage.

Fig. 3.12 illustrates the inductor current waveforms i_{Lbatt1} and i_{Lbatt2} when the HESS supplies 30W active power to the grid.

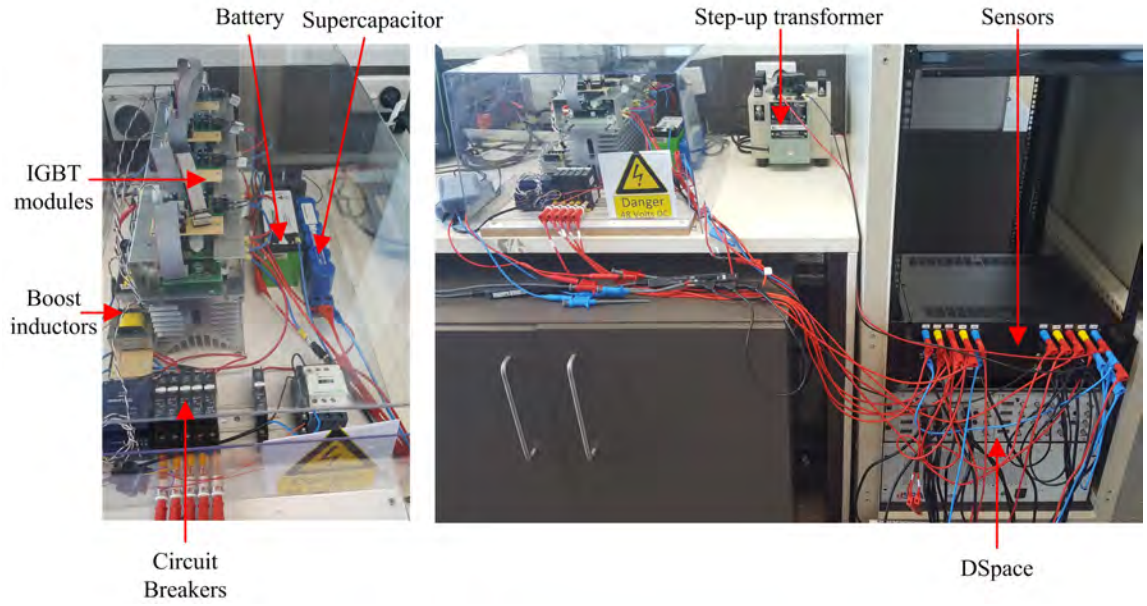

Fig. 3.10: HESS experimental setup

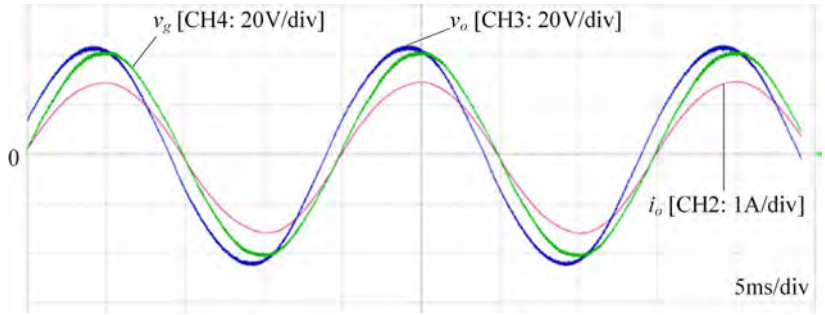

Fig. 3.11: Current waveform of the grid interfacing inductor, i_g (CH2), HESS output voltage, v_o (CH3), and grid voltage, v_g (CH4), when the HESS with interleaved operation delivers 30W active power to the grid.

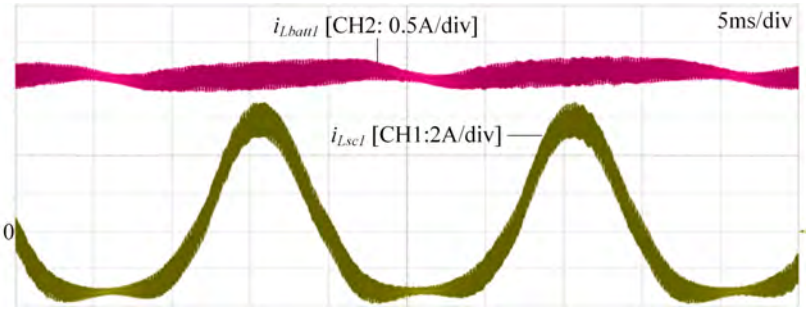

Fig. 3.12: Inductor current waveforms i_{Lsc1} (CH1) and i_{Lbatt1} (CH2) when the HESS with interleaved operation delivers 30W active power to the grid.

Furthermore, the total supercapacitor current and the battery current are shown in Fig. 3.13 with the interleaved operation. It is evident that the HESS controller allocates the second-order harmonic current component to the supercapacitor while battery supplies the required average power component.

Total supercapacitor current and the total battery current with the in-phase PWM operation at 30W active power output is shown in Fig. 3.14. When compared with the interleaved operation illustrated in Fig. 3.13, a significant reduction in the switching frequency ripple component of the battery and the supercapacitor current can be observed with the interleaved operation of the boost inverter based HESS.

Operation of the HESS with a step changing power reference signal is shown in Fig. 3.15. The high pass filter cut-off frequency is set to 0.05rads^{-1} in this experiment. It is evident that the proposed control system is able to properly track the output power reference signals. The supercapacitor responds to the sudden power changes while the battery current gradually increases to supply the required output power. Due to the initial supercapacitor response to the step power change, its voltage diverts from the reference value. The battery supplies an additional amount of current to recharge the supercapacitor to the reference voltage level. After supplying the required charging current to the supercapacitor, the battery current gradually reduces and settles down to provide the required average output power component. It can be observed that throughout the

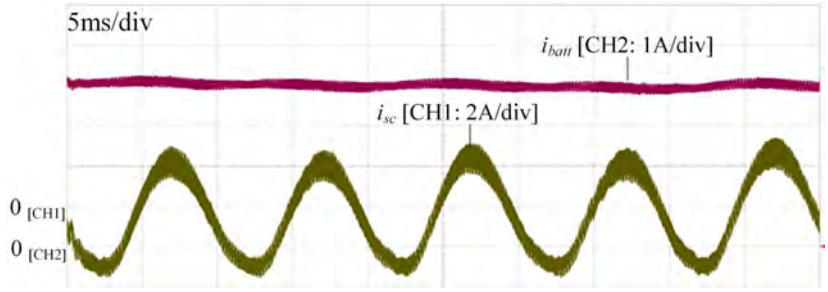

Fig. 3.13: The total battery current, i_{batt} (CH2) and the total supercapacitor current, i_{sc} (CH1) when the HESS with interleaved operation delivers 30W active power to the grid.

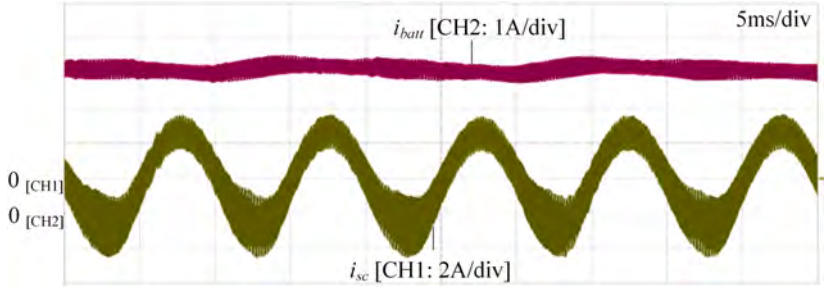

Fig. 3.14: The total battery current, i_{batt} (CH2) and the total supercapacitor current, i_{sc} (CH1) when the HESS with in-phase PWM operation delivers 30W active power to the grid.

Table 3.2: Hybrid energy storage system parameters

Parameter	**Value**	**Parameter**	**Value**
Power converter parameters			
V_o	40 V	$V_{DC,ref}$	40 V
L_{batt1},L_{batt2}	1 mH	L_{sc1},L_{sc2}	210 μH
C_1, C_2	60 μF	f	50 Hz
T_s	50 μs	T_F	0.001
$V_{sc,ref}$	11.3 V	R_{Lsc1}, R_{Lsc2}	0.24Ω
R_{Lbatt1}, R_{Lbatt2}	0.24Ω		
Grid parameters			
V_g	40 V	L_g	20 mH
Voltage control loop parameters			
$K_p(PR)$	0.1	$K_p(PI_{scv})$	50
$K_i(PR)$	4	$K_i(PI_{scv})$	1
Current control loop parameters			
$K_p(PI_{Ibatt})$	15.529	$K_p(PI_{Isc})$	2.615
$K_i(PI_{Ibatt})$	8.44×10^{-5}	$K_i(PI_{Isc})$	8.44×10^{-5}
PQ controller parameters			
$K_p(PI_P)$	2×10^{-6}	$K_p(PI_Q)$	1×10^{-5}
$K_i(PI_P)$	0.14	$K_i(PI_Q)$	4
Battery SOC controller parameters			
$K_p(PI_{SOC})$	0.8	$K_i(PI_{SOC})$	0.5

experiment, the supercapacitor voltage is maintained around the reference voltage level. In the supercapacitor current waveforms, the second-order harmonic current component is filtered out so that the supercapacitor response to the fast power changes can be clearly seen.

Next, operation of the HESS in a renewable power generation scenario as illustrated in Fig. 3.16 is considered and the power reference signals are generated to emulate the PV power generation. The PV power generation data was obtained from [86] and scaled down to fit the power range of the low voltage low power prototype. The cut-off frequency of the high-pass filter is set to 3.3×10^{-3} rads^{-1} so that the battery responds to the average power requirement while the supercapacitor responds to the fast PV power changes. Fig. 3.17 illustrates the experimental waveforms and as expected, the battery is charged using the average power component generated by the PV source while the supercapacitor handles

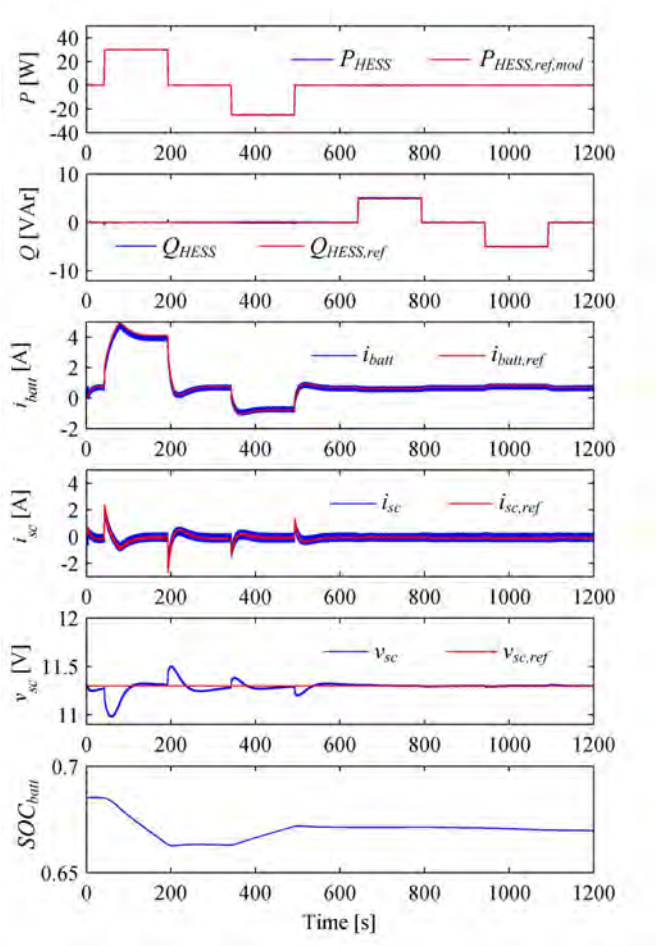

Fig. 3.15: Operation of the HESS with step changing output power reference signals.

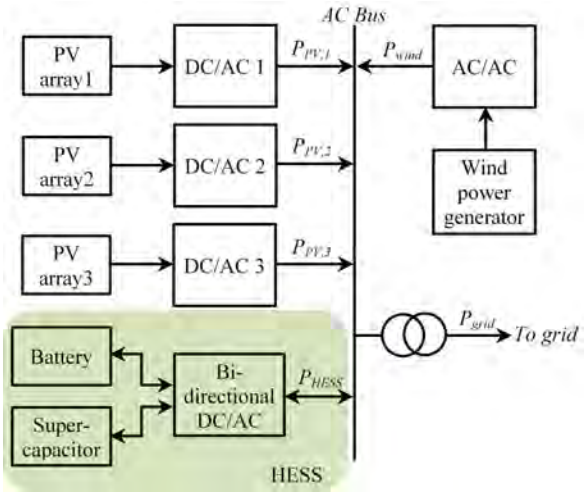

Fig. 3.16: Example application of a direct AC line integrated battery-supercapacitor HESS with a renewable power generation system.

the fluctuating current component due to the intermittency of the PV power generation.

Fig. 3.18 demonstrates the operation of the battery-supercapacitor HESS when the

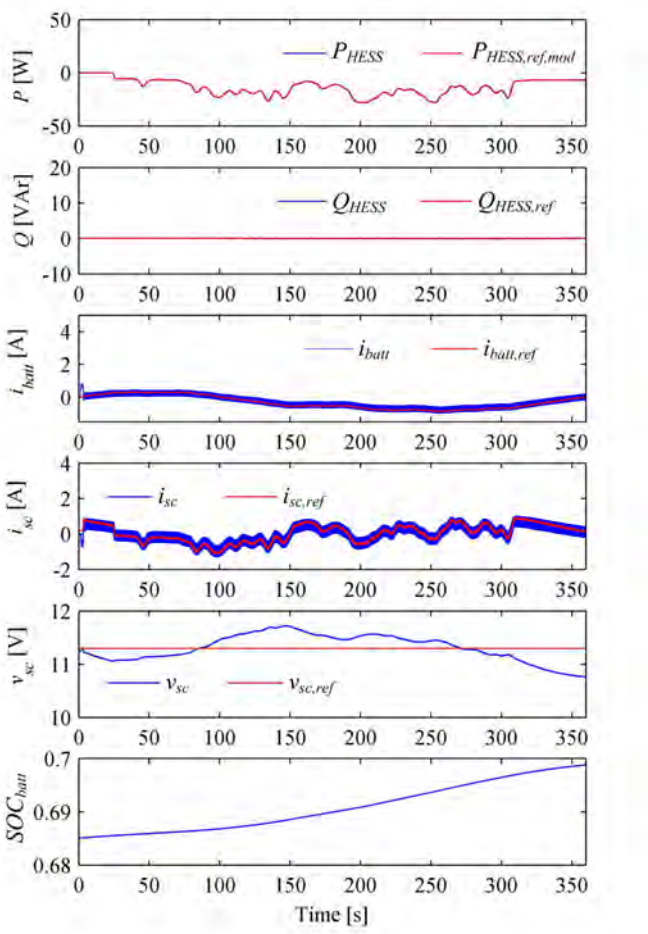

Fig. 3.17: Operation of the HESS when the power reference signals are generated to emulate PV power generation situation.

battery SOC limits are reached. For the illustrative purposes, the maximum battery SOC limit, $SOC_{batt,max}$ and the minimum battery SOC limit $SOC_{batt,min}$ are selected as 0.7 and 0.65 respectively. In the experiment, initially HESS absorbs active power from the grid and hence the battery gets charged. Once the battery reaches its maximum SOC limit, the HESS reference power signal is modified by the SOC controller to bring the battery current to zero so that the battery SOC will not increase over the maximum limit. Next, active power is supplied by the HESS to the grid in order to illustrate the operation of the HESS at the minimum battery SOC limit. When the battery SOC reaches its minimum value, the active power reference signal is modified by the SOC controller to avoid further discharging of the battery as illustrate in Fig. 3.18.

3.6 Conclusions

A single phase grid connected battery-supercapacitor HESS was proposed in this chapter. The HESS was designed using the interleaved boost inverter topology proposed

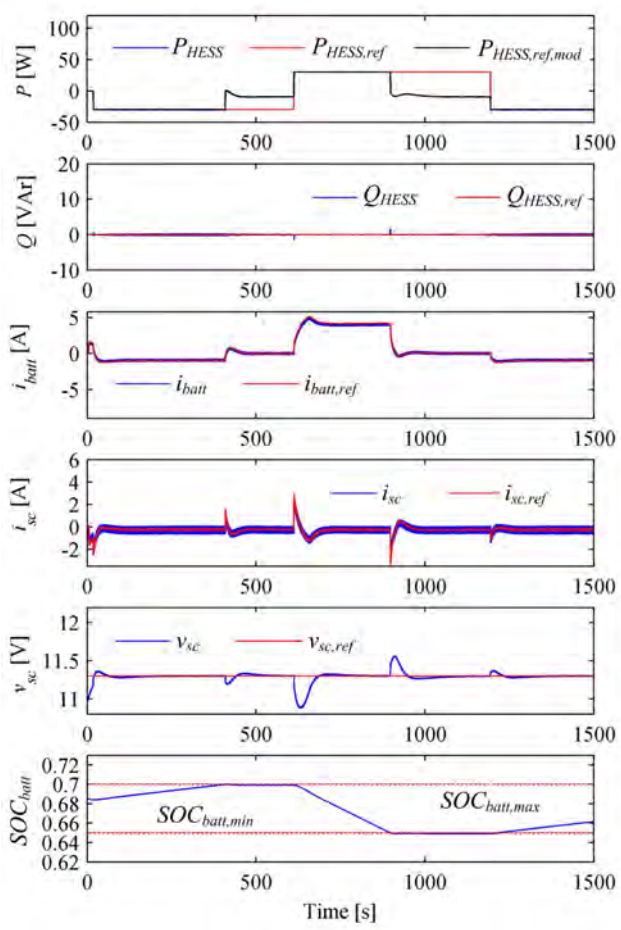

Fig. 3.18: Operation of the HESS when the battery SOC limits are reached.

in Chapter 2 which reduces the switching frequency ripple current component in both the battery and the supercapacitor currents and helps to reduce the internal heating of the DC energy storage devices. A filter based power allocation method and a DL control strategy were used to control the HESS. A SCVC was employed to reduce the risk of supercapacitor over-charging and over-discharging by maintaining the supercapacitor voltage around a reference voltage level. Furthermore, an extended Kalman filter based battery SOC estimator was employed to maintain the battery SOC within a safe operating region.

Experimental results showed that the HESS operated as required and allocated the fast current variations and the second-order harmonic current to the supercapacitor while the battery responded to the slow varying current demands. This in turn increases the battery lifetime due to reduction in its internal heating. Moreover, the results demonstrated that the control system maintained the supercapacitor voltage at around a reference voltage value and additionally, the battery SOC was maintained within the specified SOC limits. The proposed interleaved HESS is the first experimentally verified single phase direct grid

integrated HESS with reduced switching frequency ripple current component in literature.

Chapter 4

Supercapacitor Energy Controlled Filter Based Battery-Supercapacitor Hybrid Energy Storage System

The power allocation parameter selection and energy storage element sizing are important aspects of a battery-supercapacitor HESS design. Furthermore, it is vital to control the SOC of the supercapacitor to avoid supercapacitor over-charging and over-discharging. A SCVC and a high-pass filter based power allocation strategy was used in the proposed HESS in Chapter 3. Due to the non-linearity of the SCVC, it is challenging to accurately size the energy storage elements as well as to identify the suitable high-pass filter and SCVC parameters. In this chapter, a supercapacitor energy controller (SCEC) is proposed which helps to circumvent the issues associated with the non-linearity of the SCVC and filter based power allocation method [65]. The effects of the SCEC on the filter based HESS is extensively analyzed. Then, a HESS power allocation parameter selection method and an energy storage element sizing method are proposed for a given application. Experimental results are used to validate the operation, parameter selection and sizing of the supercapacitor energy controlled filter based HESS.

4.1 Introduction

The operation of an interleaved boost inverter based, single phase grid integrated battery-supercapacitor HESS was proposed in Chapter 3. A high pass filter based power allocation strategy along with a supercapacitor voltage controller (SCVC) was used to

allocate the fast power variations and the second-order harmonic current component to the supercapacitor. A DL controller strategy was used to control the boost converter legs and a droop control method was used to control the HESS power exchange with the grid. The battery SOC estimation obtained from an extended Kalman filter based SOC estimator was used to control the battery SOC within a predefined safe SOC range.

In this chapter, energy storage element sizing and HESS power allocation parameter selection for a supercapacitor SOC controlled filter based batter-supercapacitor HESS is considered.

Energy storage sizing is an important aspect of the HESS design. Numerous researches have been conducted to identify suitable energy storage sizing methods for battery-supercapacitor HESSs and the sizing methods are strongly coupled with the employed power allocation methods [10, 24, 26, 29, 31, 34, 37, 38, 49, 50]. The energy storage sizing methods presented in [10, 24, 29, 31, 34, 38, 50] were studied using non-filter based power allocation methods and hence cannot be used in filter based battery-supercapacitor HESSs. In [34], authors presented a HESS cost minimization method to select the power allocation frequency and the supercapacitor size. In [37, 49] the filter based HESS design was done based on the Ragone theory. A supercapacitor sizing method for a filter based HESS with a pulsed power load was analyzed in [26]. However, in these papers, the supercapacitor SOC control was not considered.

In the battery-supercapacitor HESSs, the supercapacitor voltage tends to fluctuate in a large range due to the supercapacitor power fluctuations. Hence, the supercapacitor SOC control is important to reduce the risk of supercapacitor over-charging or over-discharging [29, 87, 88]. Using a supercapacitor SOC controller, the SOC can be maintain within a safe SOC region. SCVCs were used as supercapacitor SOC controllers in filter based HESSs presented in [12, 20, 27]. However, the effect of SCVC on HESS power allocation or energy storage element sizing was not presented in the papers. Due to the non-linearity introduced by the SCVC, it is challenging to analyze the dynamic behavior of the power allocation method. Furthermore, the relationship between the power component supplied by the supercapacitor and the total HESS output power depends on the supercapacitor size and hence, accurate supercapacitor sizing is difficult. The effect of the supercapacitor SOC controllers on the HESS power allocation and dynamic performance are not analyzed in the current literature.

Studying the effects of the supercapacitor SOC controller on the HESS power allocation and dynamic performance is important, *a*) to select the high pass filter cut-off frequency and the supercapacitor SOC controller parameters required to achieve the desired HESS performance and *b*) to obtain the required energy storage sizes for a considered HESS

application.

In this chapter a HESS power allocation parameter selection method and an energy storage element sizing method are studied for a supercapacitor SOC controlled, filter based battery-supercapacitor HESS. The operation and associated challenges of a filter based HESS with the conventional SCVC are presented first. Then, a SCEC is proposed to circumvent the issues associated with the non-linearity of the SCVC and filter based power allocation method. The effects of the SCEC on the filter based HESS is analyzed. Then, a HESS power allocation parameter selection method and an energy storage element sizing method are proposed for a given application. Experimental results are used to validate the operation, parameter selection and sizing of the supercapacitor energy controlled filter based HESS.

4.2 HESS Operation with SCVC

The block diagram of the outer voltage control loop for the left-hand side boost converter legs is shown in Fig. 4.1. In this chapter, a simplified voltage control loop is considered. The ripple allocator presented in Chapter 3 is not considered in the analysis since it is only used for the initial supercapacitor charging as discussed in Chapter 3 Further, a proportional controller is considered in the SCVC. In the voltage control loop, P_{tot1} is the total input power supplied by the left-hand side boost converter legs. A high-pass filter is employed to allocate the high frequency power variations to the supercapacitor. The high pass filter transfer function is given by,

$$H_{HPF} = \frac{as}{as+1} \tag{4.1}$$

where $a = \dfrac{1}{\omega_{HPF}}$ and ω_{HPF} is the high pass filter cutoff frequency. To maintain the supercapacitor voltage around a reference voltage value, the power reference signal is then modified using the SCVC. The supercapacitor reference voltage is given by $v_{sc,ref}$ which

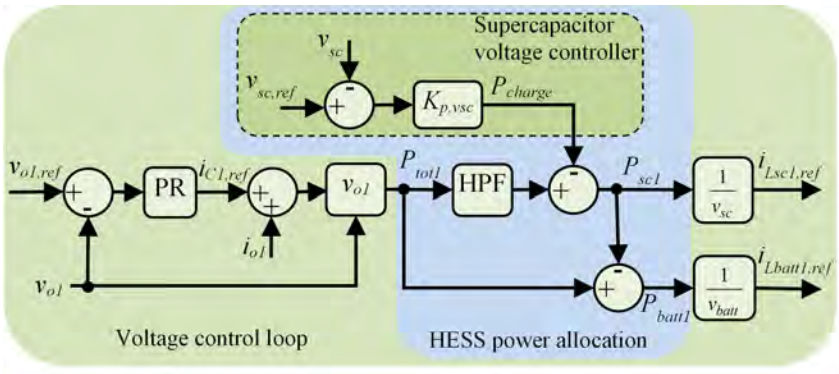

Fig. 4.1: Outer voltage control loop for the left-hand side boost converter legs with SCVC

can be selected as explained in Chapter 3. Additionally, the SCVC helps to handle the self-discharging of the supercapacitor. The safe operating region of the supercapacitor is given by,

$$v_{sc,min} \leq v_{sc} \leq v_{sc,max} \tag{4.2}$$

where $v_{sc,min}$ and $v_{sc,max}$ are the minimum and maximum allowed supercapacitor voltages, respectively.

The total power supplied by the left hand side and the right hand side boost converter legs, P_{tot} can be written as,

$$P_{tot} = P_{tot1} + P_{tot2} = \frac{1}{\eta} P_{HESS}. \tag{4.3}$$

P_{HESS} is the total HESS output power and η represents the efficiency of the HESS where $\eta = \left(\frac{P_{HESS}}{P_{tot}}\right)$. In this analysis, power components are considered as the average values over one output voltage cycle.

A simplified model of the HESS power allocation method is considered as shown in Fig. 4.2 to analyze the dynamic behavior of the HESS. The supercapacitor is modeled as an ideal capacitor by neglecting the ESR value of the supercapacitor. The simplification is valid due to relatively small supercapacitor ESR and the simplification can have an impact on the analysis when ESR of the supercapacitor cannot be neglected [26, 89]. Using the model, the relationship between the total power supplied by the supercapacitor, P_{sc} and its voltage can be written as,

$$v_{sc} = v_{sc,init} - \frac{1}{C_{sc}} \int \frac{P_{sc}}{v_{sc}} dt \tag{4.4}$$

where $v_{sc,init}$ and C_{sc} are the initial supercapacitor voltage and the capacitance of the supercapacitor, respectively. A factor of '2' is used in the model shown in Fig. 4.2 since the SCVC modifies both the left hand side and the right hand side boost converter legs.

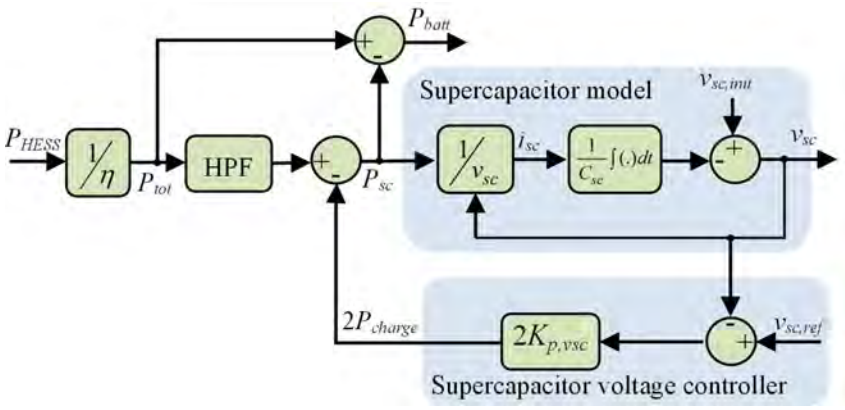

Fig. 4.2: Simplified block diagram of the HESS power allocation with the SCVC

Then, the relationship between P_{tot} and P_{sc} can be obtained by,

$$P_{sc} = HPF\left(P_{tot}\right) - 2K_{p,vsc}\left[\left(v_{sc,ref} - v_{sc,init}\right) + \int \frac{P_{sc}}{v_{sc}C_{sc}}dt\right] \tag{4.5}$$

where $HPF\left(P_{tot}\right)$ is the output from the high pass filter.

In order to obtain the required energy storage element sizes and also to select the high pass filter cut-off frequency and SCVC gain value, the dynamic relationship between P_{tot} and the power supplied by the individual energy storage elements (P_{sc} and P_{batt}) has to be obtained. But, due to non-linearity in (4.4) and (4.5), it is challenging to obtain the relationships between P_{tot} and power components supplied by the battery and the supercapacitor.

4.3 Supercapacitor Energy Controller

In this section, a SCEC is analyzed for the filter based battery-supercapacitor HESS and the SCEC is used to overcome the issues related to the non-linearity of the SCVC. The modified voltage control loop for the left hand side boost converter leg with the SCEC is illustrated in Fig. 4.3. Instead of controlling the supercapacitor voltage around a reference voltage value, the energy stored in the supercapacitor E_{sc} is controlled around a reference energy level $E_{sc,ref}$. The stored energy in the supercapacitor E_{sc} is calculated using the simplified supercapacitor model and can be written as,

$$E_{sc} = \frac{1}{2}C_{sc}v_{sc}^2 \tag{4.6}$$

A simplified block diagram as illustrated in Fig. 4.4 is considered to obtain the dynamic behavior of the HESS power allocation method. Using the simplified model, the relationship between the power supplied by the supercapacitor and its stored energy can be written as,

$$E_{sc} = E_{sc,init} - \int P_{sc}dt \tag{4.7}$$

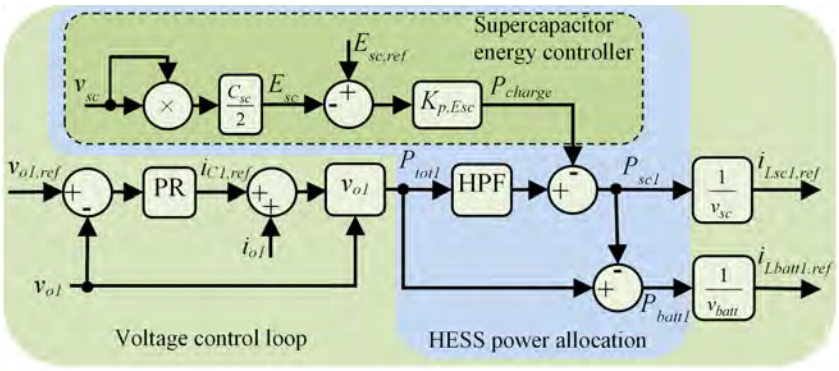

Fig. 4.3: Outer voltage control loop for the left-hand side boost converter legs with SCEC

where $E_{sc,init}$ is the initial stored energy of the supercapacitor which corresponds to $v_{sc,init}$ value. Then using Fig. 4.4, the relationship between the HESS output power and the power component supplied by the supercapacitor can be written as (refer Appendix A.1.1),

$$P_{sc} = \frac{as^2}{as^2 + (1 + 2aK_{p,Esc})s + 2K_{p,Esc}} \frac{1}{\eta} P_{HESS} - \frac{2K_{p,Esc}s}{(s + 2K_{p,Esc})}(E_{sc,ref} - E_{sc,init}) \quad (4.8)$$

Assuming,

$$E_{sc,init} = E_{sc,ref}, \quad (4.9)$$

the transfer function between P_{HESS} and P_{sc} can be obtained from (4.8) as,

$$H_{Psc}(s) = \frac{P_{sc}}{P_{HESS}} = \frac{as^2}{as^2 + (1 + 2aK_{p,Esc})s + 2K_{p,Esc}} \frac{1}{\eta} \quad (4.10)$$

Similarly, the transfer function between P_{batt} and P_{HESS} is,

$$H_{Pbatt}(s) = \frac{P_{batt}}{P_{HESS}} = \frac{(1 + 2aK_{p,Esc})s + 2K_{p,Esc}}{as^2 + (1 + 2aK_{p,Esc})s + 2K_{p,Esc}} \frac{1}{\eta} \quad (4.11)$$

Further, the transfer function between the supercapacitor energy change, dE_{sc} and P_{HESS} is,

$$H_{dEsc}(s) = \frac{dE_{sc}}{P_{HESS}} = \frac{as}{as^2 + (1 + 2aK_{p,Esc})s + 2K_{p,Esc}} \frac{1}{\eta} \quad (4.12)$$

4.3.1 Effects of the Supercapacitor Energy Controller on the HESS Power Allocation Strategy

In order to identify the effects of the SCEC on the HESS power allocation strategy, obtained transfer functions in (4.10),(4.11), and (4.12) are further analyzed.

It can be observed that (4.11) has a zero z_1 and two poles p_1 and p_2 where,

$$z_1 = \frac{-2K_{p,Esc}}{(1 + 2aK_{p,Esc})}; \qquad p_1 = \frac{-1}{a}; \qquad p_2 = -2K_{p,Esc} \quad (4.13)$$

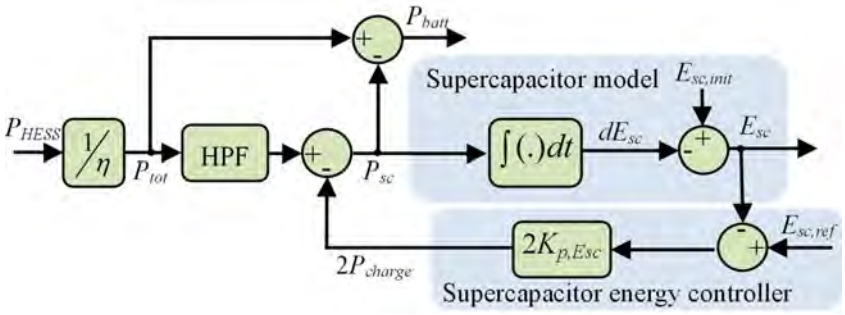

Fig. 4.4: Simplified block diagram of the HESS power allocation with the SCEC.

It can be shown that,

$$\begin{aligned} |z_1| &< |p_1| \\ |z_1| &< |p_2| \end{aligned} \tag{4.14}$$

for non-negative, non-zero a and $K_{p,Esc}$ values. Then, an asymptotic Bode plot of H_{Pbatt} can be drawn as shown in Fig. 4.5. It can be observed that the transfer function H_{Pbatt} demonstrates low pass filter characteristics. Since $H_{Psc} = 1 - H_{Pbatt}$, the transfer function H_{Psc} demonstrates high pass filter characteristics. Using the Bode plot shown in Fig. 4.5, following relationship can be obtained.

$$\frac{\omega_c}{max(|p_1|, |p_2|)} = \frac{min(|p_1|, |p_2|)}{|z_1|} \tag{4.15}$$

where ω_c is the gain cross-over frequency of the transfer function H_{Pbatt}. Substituting p_1 and p_2 from (4.13) to (4.15), the gain cross-over frequency can be obtained as,

$$\omega_c = \frac{1 + 2aK_{p,Esc}}{a} \tag{4.16}$$

The gain cross-over frequency of the HESS without any supercapacitor SOC control method can be obtained by substituting $K_{p,Esc}$=0 to (4.16) as,

$$\omega_c' = \frac{1}{a} = \omega_{HPF} \tag{4.17}$$

which is similar to the cut-off frequency of the high pass filter. Superscript '$\prime$' denotes the HESS operation without any supercapacitor SOC controller. From (4.16) and (4.17), it is evident that the introduction of SCEC leads to a modification of the HESS power allocation frequency by a factor of $(1 + 2aK_{p,Esc})$. To further investigate the effect of the SCEC on HESS power allocation,(4.11) can be re-written as,

$$H_{Pbatt} = \left[\frac{\omega_c s + \gamma}{s^2 + \omega_c s + \gamma}\right] \frac{1}{\eta} \tag{4.18}$$

where

$$\gamma = \frac{2K_{p,Esc}}{a} \tag{4.19}$$

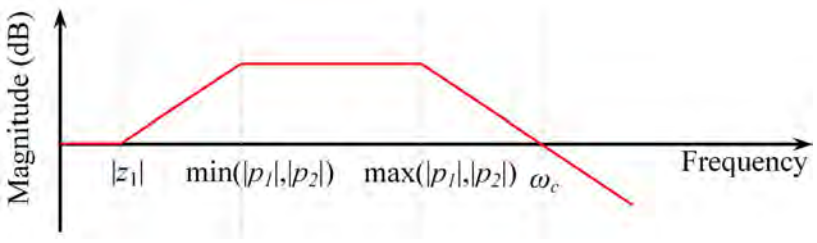

Fig. 4.5: Asymptotic Bode plot of the transfer function H_{Pbatt}.

Assume the required H_{Pbatt} gain cross-over frequency is $\omega_{c,req}$. Then, the high pass filter parameter, a and SCEC gain $K_{p,Esc}$ have to be selected such that

$$\frac{1 + 2aK_{p,Esc}}{a} = \omega_{c,req} \tag{4.20}$$

However, from (4.18), infinite number of H_{Pbatt} transfer functions with $\omega_{c,req}$ gain cross-over frequency can be obtained by changing the γ value. Substituting $K_{p,Esc}$ from (4.19) into (4.20) and solving for a gives,

$$a = \frac{\omega_{c,req} \pm \sqrt{\omega_{c,req}^2 - 4\gamma}}{2\gamma} \tag{4.21}$$

It can be observed from (4.21) that there are two combinations of a and $K_{p,Esc}$ values which result in the same H_{Pbatt} transfer function. Moreover from (4.21), for a required gain cross-over frequency $\omega_{c,req}$, γ has to satisfy,

$$0 \leq \gamma \leq \frac{\omega_{c,req}^2}{4} \tag{4.22}$$

Using,

$$n = \frac{\gamma}{\omega_{c,req}^2} \tag{4.23}$$

and (4.22), a set of all possible H_{Pbatt} transfer functions can be obtained by changing n in the following range.

$$0 \leq n \leq 0.25 \tag{4.24}$$

Figs. 4.6 (a) and 4.6 (b) demonstrates the effect of n on the step response of the transfer functions H_{Pbatt} and H_{dEsc} for a sample gain cross-over frequency $\omega_{c,req} = 0.05\text{rads}^{-1}$. The battery power profile demonstrates a low pass filter response to a step output power change as shown in Fig. 4.6 (a). The supercapacitor supplies the balance power component to meet the output power requirement, and hence, the stored energy in the supercapacitor changes as shown in Fig. 4.6 (b). It can be observed that when $n = 0$, the supercapacitor energy is not controlled and it does not reach the reference energy level (at the steady state $dE_{sc} \neq 0$). When $n = 0.25$, the fastest battery response can be observed. Further, when $n = 0.25$, change in the supercapacitor energy dE_{sc} is also minimum.

4.3.2 Calculating the Capacitance of the Supercapacitor C_{sc} for a Set of HESS Power Allocation Parameters and for a Given HESS Power Profile

Next, the supercapacitor sizing for a set of HESS power allocation parameters ($\omega_{c,req}$ and n) and for a given HESS output power profile is considered.

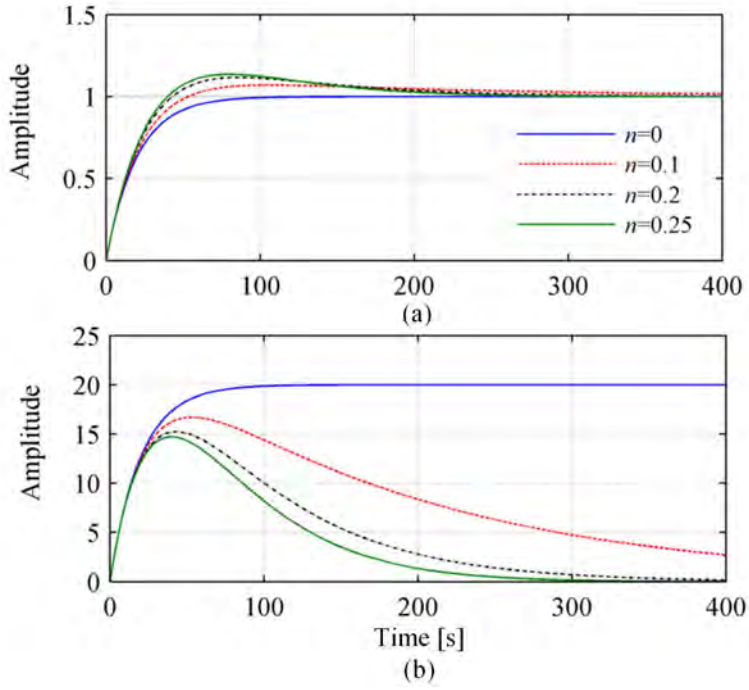

Fig. 4.6: Step response of (a) H_{Pbatt} and (b) H_{dEsc} for various n values for a sample gain cross-over frequency $\omega_{c,req} = 0.05$ rads^{-1}.

First, the maximum and minimum supercapacitor voltage limits $v_{sc,max}$ and $v_{sc,min}$ have to be selected based on the operation and specifications of the power converter. For the considered boost inverter based HESS, $v_{sc,min}$ can be selected based on the maximum possible gain of the converter while $v_{sc,max}$ has to satisfy,

$$v_{sc,max} \leq V_{DC,ref} - \frac{V_o}{2} \tag{4.25}$$

Please refer to (3.10). Using the maximum and minimum supercapacitor voltage limits $v_{sc,max}$ and $v_{sc,min}$, the utilized energy of the supercapacitor $E_{sc,u}$ can be calculated as

$$E_{sc,u} = E_{sc,max} - E_{sc,min} = 0.5C_{sc}(v_{sc,max}^2 - v_{sc,min}^2). \tag{4.26}$$

$E_{sc,max}$ and $E_{sc,min}$ are the supercapacitor energy levels corresponding to the maximum and minimum supercapacitor voltage limits $v_{sc,max}$ and $v_{sc,min}$, respectively. If the supercapacitor reference energy level is chosen as,

$$E_{sc,ref} = E_{sc,min} + 0.5E_{sc,u} \tag{4.27}$$

then equal amount of energy ($0.5E_{sc,u}$) is available for supercapacitor charging and discharging. The supercapacitor voltage level corresponding to the reference energy level can be obtained as,

$$v_{sc,ref} = \sqrt{0.5(v_{sc,min}^2 + v_{sc,max}^2)} \tag{4.28}$$

Then, using the considered HESS power profile and the set of HESS power allocation parameters ($\omega_{c,req}$ and n), the supercapacitor energy variation profile dE_{sc} can be obtained using the transfer function (4.12). Since only half of the utilized energy is available for either the supercapacitor charging or discharging,

$$0.5E_{sc,u} = max(|dE_{sc}|) \tag{4.29}$$

Using (4.26) and (4.29), the required supercapacitor value for the considered HESS output power profile and for the set of power allocation parameters, can be obtained as,

$$C_{sc} = \frac{4max(|dE_{sc}|)}{(v_{sc,max}^2 - v_{sc,min}^2)} \tag{4.30}$$

4.3.3 Calculating the Battery Specifications for a Set of HESS Power Allocation Parameters and for a Given HESS Output Power Profile

For a given HESS output power profile and for a set of HESS power allocation parameters ($\omega_{c,req}$ and n), the corresponding battery power profile P_{batt} can be obtained from (4.11). Then, the required power rating of the battery $P_{batt,rated}$ can be selected as,

$$P_{batt,rated} \geq max(P_{batt}) \tag{4.31}$$

Further, the change in the battery energy dE_{batt} due to the considered HESS operation can be obtained using

$$H_{dEbatt} = \frac{dE_{batt}}{P_{HESS}} = \frac{1}{s}\left[\frac{(1+2aK_{p,Esc})s + 2K_{p,Esc}}{as^2 + (1+2aK_{p,Esc})s + 2K_{p,Esc}}\right]\frac{1}{\eta} \tag{4.32}$$

Then, the required energy rating of the battery $E_{batt,rated}$ should be selected such that,

$$E_{batt,rated} \geq max(|dE_{batt}|). \tag{4.33}$$

4.4 HESS Power Allocation Parameter Selection and Supercapacitor Sizing for a PV Power Smoothing Application

This section presents a HESS power allocation parameter selection and supercapacitor sizing method for a HESS operation in a PV power smoothing application. The power allocation parameters and the required supercapacitor size are selected to achieve required smoothness of the battery power profile. As a measure of smoothness, the gradient of the battery power profile is considered. The filter and SCEC based power allocation strategy

considered in this chapter reduce the variability of the battery power profile. Additionally, the power allocation method indirectly reduces the peak power requirement from the battery as presented later in the chapter.

Fig. 4.7 illustrates an example application of the HESS where it is used to smooth the PV power injected to the grid at the common coupling point. The PV power profiles are obtained by scaling the data available in [86] to match the HESS experimental setup parameters summarized in Table 4.2. The compensating power supplied by the HESS can be obtained as the difference between the generated PV power and the power supplied to the grid. In this research, a simple rate limiter is used to limit the per minute ramp rate to 10% of the rated power of the PV plant [90]. Relevant power profiles P_{PV}, P_{grid} and P_{HESS} are illustrated in Fig. 4.8 (a) where P_{PV} and P_{grid} are the generated power from the PV plant and the power injected to the grid at the common coupling point respectively. Fig. 4.8 (b) depicts the total power supplied by the battery and the supercapacitor, P_{tot}. The gradient of the P_{tot} power profile is considered to quantify the variability, and the histogram of non-zero gradient values of the P_{tot} power profile is shown in Fig. 4.9.

To observe the relationship between the HESS power allocation parameters and the battery power gradient, a set of battery power profiles is obtained using the P_{HESS} power profile in Fig. 4.8 and (4.18) for a set of ω_c and n values. Then, the maximum gradient value of the battery power profile $max(|\nabla P_{batt}|)$ is plotted against ω_c and n as illustrated in Fig. 4.10 (a). Additionally, the required supercapacitor values for each set of power allocation parameters are calculated and shown in Fig. 4.10(b).

Then, a linear search method and the data in Fig. 4.10 are used to obtain the required HESS power allocation parameters which minimizes the required capacitance value of the supercapacitor, C_{sc} subject to $max(\nabla P_{batt}) \leq \nabla P_{batt,limit}$. Here $\nabla P_{batt,limit}$ is a predefined maximum allowable gradient value for the battery power profile. In the linear search method, first a set of HESS power allocation parameters which satisfy $max(\nabla P_{batt}) \leq$

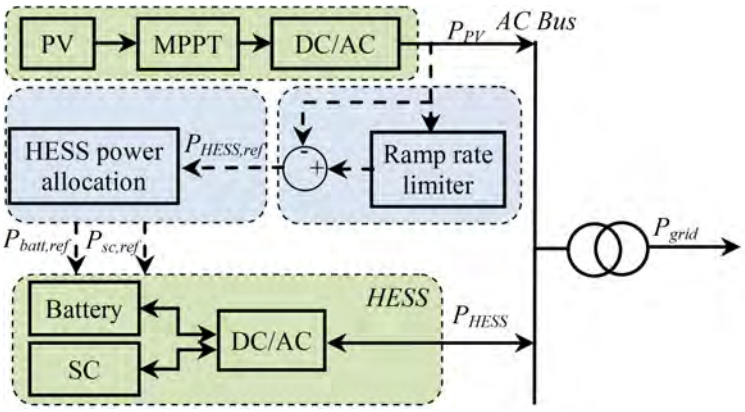

Fig. 4.7: Block diagram of the HESS in a PV power smoothing application

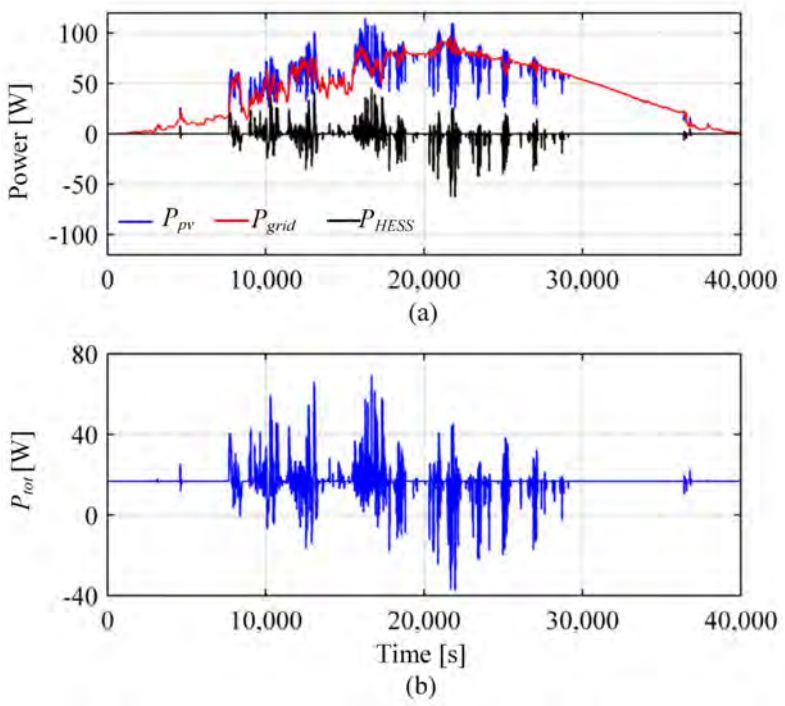

Fig. 4.8: Power profiles considered for the HESS parameter selection. (a) PV power, power injected to the grid and the HESS power and (b) the total power profile of the battery and the supercapacitor

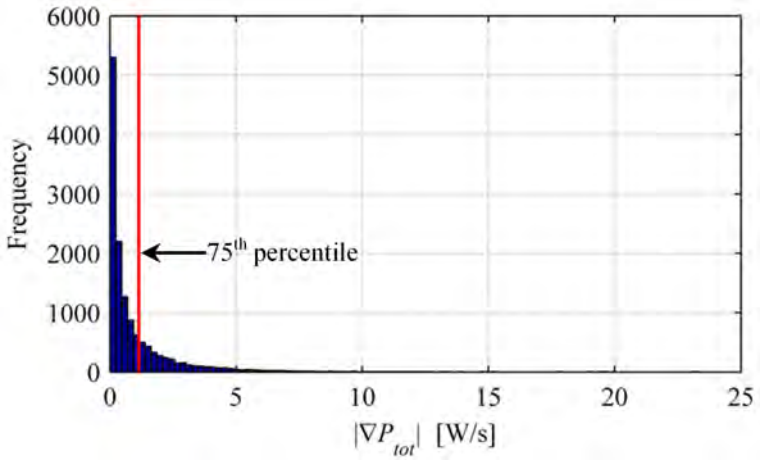

Fig. 4.9: Histogram of the non-zero gradient values of the P_{tot} power profile

$\nabla P_{batt,limit}$ is selected and then the ω_c and n values corresponding to the minimum required supercapacitor value, $C_{sc,req}$ in the selected set are identified. After the required $\omega_{c,req}$ and n_{req} are identified, the high pass filter parameter and the SCEC gain can be found using (4.16), (4.21), and (4.23) as,

$$a = \frac{\omega_{c,req} + \sqrt{\omega_{c,req}^2 - 4n_{req}\omega_{c,req}^2}}{2n_{req}\omega_{c,req}^2} \tag{4.34}$$

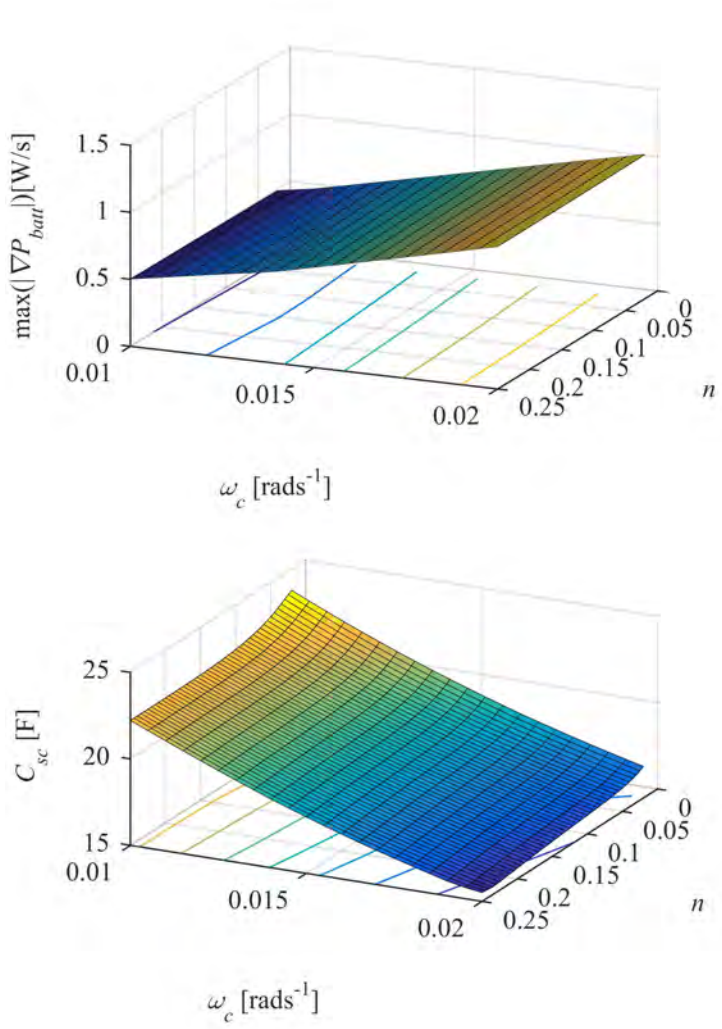

Fig. 4.10: Variation of (a) $max(|\nabla P_{batt}|)$ and (b) C_{sc} with n and ω_c.

$$K_{p,Esc} = \frac{a\omega_{c,req} - 1}{2a} \tag{4.35}$$

Table 4.1 summarizes the high pass filter parameter a, SCEC gain $K_{p,Esc}$, and the required supercapacitor values, $C_{sc,req}$ obtained for various values. The $\nabla P_{batt,limit}$ is calculated as the ρ^{th} percentile value of the non-zero gradient values of the P_{tot} power profile. The considered maximum and minimum supercapacitor voltage limits $v_{sc,max}$ and $v_{sc,min}$ are given in Table 4.2.

The operation of the HESS with the selected power allocation parameters and the supercapacitor value for the 75$^{\text{th}}$ percentile value is illustrated in Fig. 4.11. The percentile value ρ can be selected based on the required smoothness of the battery power profile. From Fig. 4.11 (a) it can be observed that the battery supplies only the low frequency power component of the P_{tot} power variation. The selected HESS power allocation

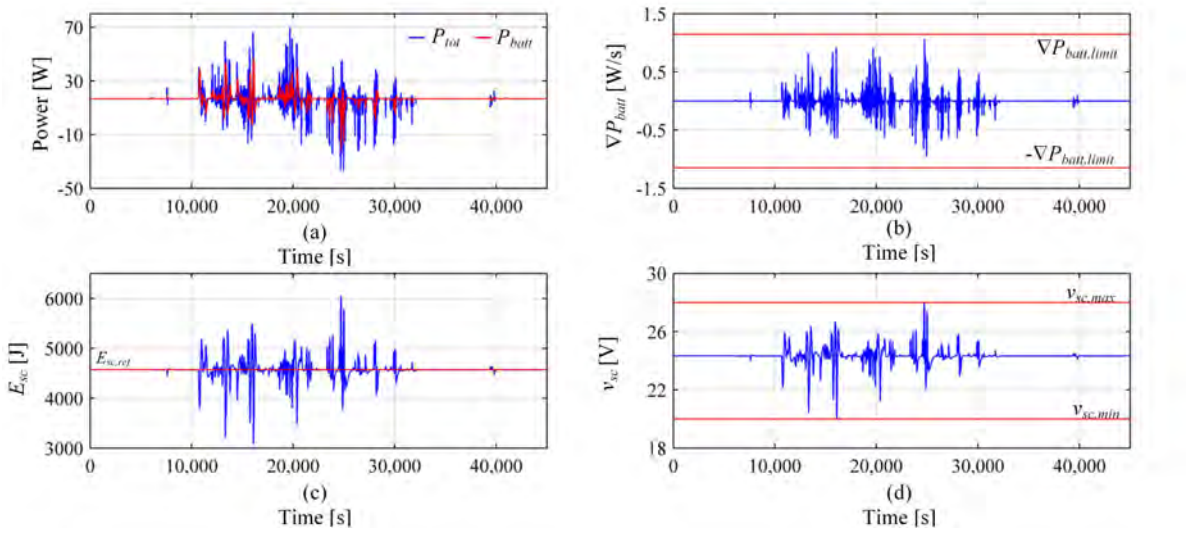

Fig. 4.11: Operation of the HESS when $\rho = 75$. (a) P_{tot} and P_{batt} power profiles, (b) gradient of the battery power profile, (c) supercapacitor energy variation and (d) voltage variation of the supercapacitor.

parameters ensure the HESS operation within the battery power gradient limits as shown in Fig. 4.11 (b). The SCEC maintains the supercapacitor energy variation around the reference energy level as illustrated in Fig. 4.11 (c). Furthermore, the selected power allocation parameters and the supercapacitor value ensures the supercapacitor operation within the pre-defined voltage limits as shown in Fig. 4.11 (d)

Next, the HESS power allocation parameter selection and the supercapacitor sizing for the HESS operation with the SCVC is considered. When the conventional SCVC is used it is difficult to properly size the supercapacitor due to the nonlinear relationship between

Table 4.1: HESS power allocation parameters and supercapacitor values for various $\nabla P_{batt,limit}$ values with and without SCEC

ρ	$\nabla P_{batt,limit}$ [W/s]	HESS operation with SCEC			HESS operation without any supercapacitor SoC controller	
		a	$K_{p,Esc}$	$C_{sc,req}$ [F]	a'	$C'_{sc,req}$ [F]
90$^{\text{th}}$	2.5863	244.88	0.0230	8.35	19.42	11.09
85$^{\text{th}}$	1.9098	325.82	0.0160	11.13	28.57	15.28
80$^{\text{th}}$	1.4571	191.89	0.0099	13.66	37.74	18.83
75$^{\text{th}}$	1.1451	132.44	0.0062	15.44	47.62	22.06
70$^{\text{th}}$	0.8979	117.65	0.0043	16.97	60.61	25.60
65$^{\text{th}}$	0.7177	142.86	0.0035	18.96	71.43	28.25
60$^{\text{th}}$	0.5825	628.57	0.0052	20.77	86.96	31.79

P_{HESS} and P_{sc}. Hence, the only way to estimate a suitable size of the supercapacitor is to size it without considering the effects of the SCVC. The transfer function between the supercapacitor energy change dE'_{sc} and P_{HESS} for the operation of the HESS without any supercapacitor SOC controller can be written as,

$$H'_{dEsc} = \frac{dE'_{sc}}{P_{HESS}} = \left[\frac{a'}{a's+1}\right]\frac{1}{\eta} = \left[\frac{\frac{1}{\omega'_c}}{\frac{1}{\omega'_c}s+1}\right]\frac{1}{\eta} \tag{4.36}$$

The superscript '$\prime$' denotes the HESS operation without supercapacitor SOC controllers. It can be observed that the power allocation frequency is equal to the high pass filter cut-off frequency. The energy variation of the supercapacitor dE'_{sc} for the HESS output power profile and any ω'_c value can be obtained using (4.36). Then the required supercapacitor value can be obtained from,

$$C'_{sc} = \frac{4max\left(|dE'_{sc}|\right)}{(v^2_{sc,max} - v^2_{sc,min})} \tag{4.37}$$

Similar to the HESS operation with the SCEC, the required power allocation frequency $\omega'_{c,req}$ is calculated to minimize the supercapacitor value C'_{sc}, subject to $max(|\nabla P'_{batt}|) \leq \nabla P_{batt,limit}$. The corresponding minimum required supercapacitor values $C'_{sc,req}$ are summarized in Table 4.1 and compared against the required supercapacitor values calculated for the HESS operation with the SCEC. It is evident that using the SCEC not only allows the precise supercapacitor sizing but also the required supercapacitor value with the SCEC is significantly lower compared to the estimated values for the operation with the SCVC.

4.5 Experimental Results

The performance of the proposed system is verified using the experimental prototype illustrated in Fig. 4.12. A 9.6Ah, 25.6V $LiFePO_4$ battery from K2 Energy and two 16V, 58F Maxwell supercapacitor modules connected in series are used in the prototype and the parameters of the HESS prototype are summarized in Table 4.2. The controllers are implemented on a DSpace DS1006 platform.

A 900s HESS power profile was considered in the experiments as shown in Fig. 4.13 (a). For the filter and SCEC parameter calculation, $\nabla P_{batt,limit}$ was chosen as the 75^{th} percentile of the non-zero gradient values of the P_{tot} power profile (0.6986W/s). Then, the required HESS power allocation parameters were obtained as $\omega_{c,req}$=0.013rads^{-1} and n_{req}=0.208 using the linear search method. The corresponding a and $K_{p,Esc}$ values are 255.81 and 0.0045, respectively. The required supercapacitor value for the considered HESS output power profile and for the calculated HESS power allocation parameters is

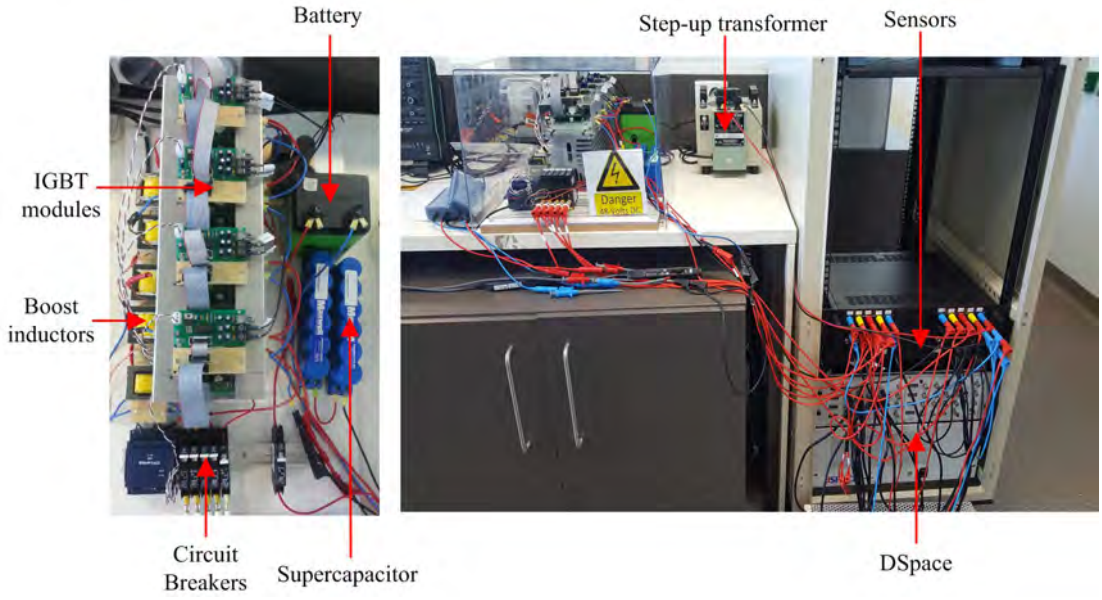

Fig. 4.12: HESS experimental setup

27.19F. Hence, a commercially available 29F supercapacitor was used in the experiments.

Fig. 4.13 depicts the operation of the HESS with the calculated power allocation

Table 4.2: Hybrid energy storage system parameters

Parameter	**Value**	**Parameter**	**Value**
Power converter parameters			
V_o	60 V	$V_{DC,ref}$	60 V
L_{batt1},L_{batt2}	210 μH	L_{sc1},L_{sc2}	210 μH
C_1, C_2	60 μF	f	50 Hz
$v_{sc,max}$	28 V	$v_{sc,min}$	20 V
Grid parameters			
V_g	60 V	L_g	20 mH
Voltage control loop parameters			
$K_p(PR)$	0.1	$K_i(PR)$	4
Current control loop parameters			
$K_p(PI_{Ibatt})$	2.615	$K_p(PI_{Isc})$	2.615
$K_i(PI_{Ibatt})$	8.44×10^{-5}	$K_i(PI_{Isc})$	8.44×10^{-5}
PQ controller parameters			
$K_p(PI_P)$	2×10^{-6}	$K_p(PI_Q)$	1×10^{-5}
$K_i(PI_P)$	0.14	$K_i(PI_Q)$	4

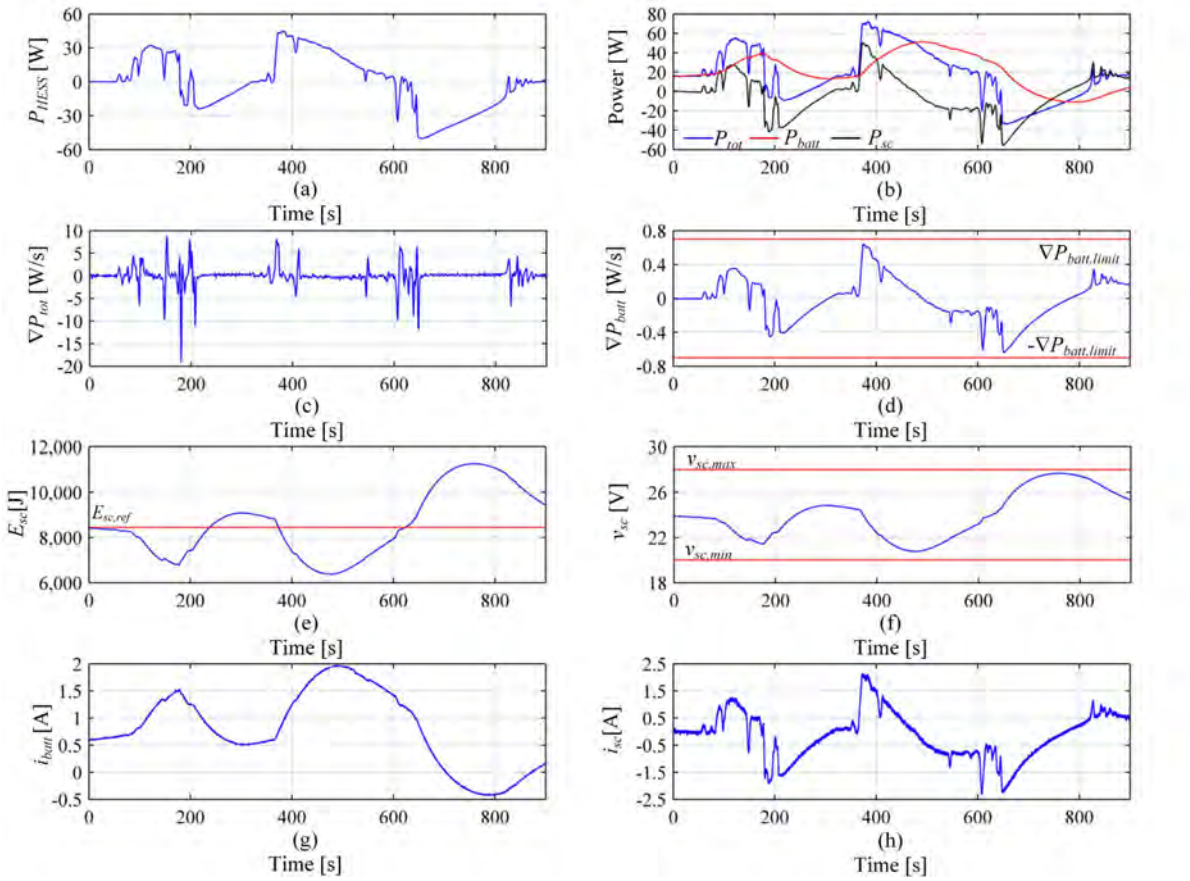

Fig. 4.13: Operation of the HESS with SCEC (a) power reference of the HESS, (b) variation of P_{tot}, P_{batt} and P_{sc}, (c) gradient of the P_{tot} profile, (d) gradient of the battery power profile, (e) supercapacitor energy variation, (f) supercapacitor voltage variation, (g) battery current variation and (h) supercapacitor current variation.

parameters and the 29F supercapacitor. According to Fig. 4.13 (b) the battery supplies the slow varying power component of the P_{tot} power profile while supercapacitor supplies the fast power fluctuations. According to Fig. 4.13 (c), the maximum gradient of the P_{tot} power profile is close to 20W/s which is clearly higher than the $\nabla P_{batt,limit}$ value. However, the battery power gradient remains within the predefined limits as illustrated in Fig. 4.13 (d). The energy variation of the supercapacitor is depicted in Fig. 4.13 (e) and it is evident that the SCEC maintains the supercapacitor energy around the reference energy level. Fig. 4.13 (f) shows the supercapacitor voltage which lies within the maximum and minimum voltage limits throughout the experiment. The battery and the supercapacitor current waveforms are illustrated in Figs. 4.13(g) and 4.13 (h) respectively. As expected, the battery supplies the slow varying current while the supercapacitor supplies the high frequency current fluctuations. Further from Figs. 4.13(b) and 4.13(g), it can be observed that, by limiting the maximum gradient of the battery power profile, the peak battery power and the number of charge/discharge cycles of the battery are also reduced.

4.6 Conclusions

In this chapter, the HESS power allocation parameter selection and energy storage element sizing for a supercapacitor SOC controlled filter based HESS was considered. None of the existing literature studied the power allocation parameter selection, energy storage element sizing and dynamic behavior of a supercapacitor SOC controlled filter based battery-supercapacitor HESS.

Due to the nonlinearity of the conventional SCVC and filter based HESS power allocation method, it was difficult to properly design the HESS power allocation parameters as well as size the supercapacitor. Hence, a SCEC is proposed in this chapter to circumvent the issues associated with the SCVC and its effects on the HESS power allocation method were extensively analyzed. It was shown that the SCEC has a significant impact on the HESS power allocation frequency. Subsequently, a HESS power allocation parameter selection and energy storage element sizing method for a given HESS output power profile were proposed. Finally, the experimental results were presented to validate the operation of the filter based HESS with the SCEC and it was shown that the selected power allocation parameters and the supercapacitor size can ensure the operation of the HESS within the supercapacitor voltage limits as well as within the battery power gradient limits.

Chapter 5

A Fixed Frequency Sliding Mode Controller for the Boost Inverter Based Hybrid Energy Storage System

This chapter presents a fixed frequency SM controller for the boost inverter based battery-supercapacitor HESS [66]. The SM controller enables better output capacitor reference following and the main advantage of the proposed SM controller, as compared with the traditional DL control method, is in eliminating possible DC current injection into the grid when the equivalent series resistance (ESR) values of the boost inductors become unequal due to the tolerances and temperature variations. The SM controller is implemented using variable amplitude PWM carrier signals which are generated using the output capacitor voltage and inductor current measurements which allow operation without using the output capacitor currents measurement. The battery connected inductor reference currents for the SM controller are generated by a supercapacitor energy controller (SCEC) which is responsible for the HESS power allocation. A supercapacitor sizing method for a given application is also presented for the SM controlled boost inverter based battery-supercapacitor HESS. The performance of the proposed SM controlled, grid connected battery-supercapacitor HESS is experimentally verified using a laboratory prototype.

5.1 Introduction

The operation of an interleaved boost inverter based battery-supercapacitor HESS was discussed in Chapter 3. A filter based power allocation strategy along with a SCVC was employed to allocate the power components among the two energy storage elements. As a way of circumventing the issues related to the non-linearity of the SCVC, a SCEC was introduced in Chapter 4 and the power allocation parameter selection and the energy storage element sizing for a filter based HESS with the SCEC was extensively analyzed for a PV power smoothing application. A double loop (DL) control method with proportional resonant (PR) controller based outer voltage control loops and PI controller based inner current control loops were used to control the boost inverter based HESS. However, the voltage drop across the boost converter leg inductors were neglected when designing the outer voltage control loop, which leads to a DC current injection into the grid when the ESR values of the left hand side and right hand side boost converter legs are not equal.

The SM techniques were extensively used to control the boost inverter topology [54,71,72]. Unlike the DL control method, the SM control methods are robust to parameter variations and modeling errors and achieve better reference following performance. However, the existing SM controllers for the boost inverter were based on the traditional SM control technique which leads to a high and variable switching frequency operation which can increase the power losses and system components design complexity [91]. Fixed frequency SM controllers were studied in literature for the boost DC/DC converters but not for the boost inverter. The fixed frequency SM controller in [92] was designed for a constant load and hence the method is not applicable to a grid connected boost inverter based HESS. A fixed frequency SM current controller was proposed in [93] for the boost DC/DC converter, however, the method required a PI controller based outer voltage control loop to generate the required inductor current reference signals. A pulse width modulation (PWM) based fixed frequency SM controller was proposed for the boost DC/DC converter in [94], but the controller required a capacitor current measurement which increased the required number of current sensors in the system and this may also influence the filter performance of the capacitor due to the impedance modification of the capacitor path [91].

A few SM controlled battery-supercapacitor HESS were proposed in literature. A simulation based comparison documented in [39] reveals that SM controller based HESS has a higher robustness and stability compared to the HESS operation with PI controllers. SM controlled battery, supercapacitor and fuel cell HESSs were presented in [25, 40], however the design procedure of the SM controller was not analyzed. A SM coefficient modification method was discussed in [41] for a battery-supercapacitor HESS in order to

control the SOC of the energy storage elements, but the possible modification ranges were not presented in the paper. None of the above mentioned SM controllers proposed for the HESSs were validated using experimental results and none of the papers analyzed the power allocation between the battery and the supercapacitor. Further, all the proposed SM controlled HESSs were DC link based structures and hence, many design issues related to the implementation of the SM controlled direct grid integrated HESSs have not been sufficiently covered.

In this chapter, a fixed frequency SM controlled boost inverter based battery-supercapacitor HESS is presented [66]. The SM controller is implemented using variable amplitude PWM carrier signals which are generated using the output capacitor voltage and inductor current measurements which allow operation without using the output capacitor currents measurement. The battery connected inductor reference currents for the SM controller are generated by a SCEC which is responsible for the HESS power allocation. A supercapacitor sizing method for a given application is also presented. The performance of the proposed SM controlled, grid connected battery-supercapacitor HESS is experimentally verified using a laboratory prototype. Furthermore, the performance of the SM controller is compared against a DL controlled boost inverter based battery-supercapacitor HESS. The main advantage of the proposed SM controller, as compared with the traditional DL control method, is in eliminating possible DC current injection into the grid when the ESR values of the boost inductors become unequal due to the tolerances and temperature variations.

5.2 Effect of the Inductor ESR Values on Output Capacitor Reference Voltage Tracking with DL Control Method

The DL controller for the HESS presented in Chapter 3 was designed using PR controller based outer voltage control loops and PI controller based inner current control loops. However, in the voltage control loop design, the voltage drops across the ESR of the boost inductors were neglected [55, 63, 64]. This results in a DC shift tracking error in the output capacitor voltages when the ESR values are significant. A simulation test was conducted to observe the effect of the boost inductor ESR values on the output capacitor voltage DC shift error using the prototype parameters summarized in Table 5.1 and the DL controller presented in [64]. In the simulation, the ESR values of the boost inductors L_{sc1}, L_{sc2}, L_{batt1}, and L_{batt2} are assumed to be equal. Fig. 5.1 illustrates the effect of the boost inductor ESR values on the DC shift of the output capacitor voltage

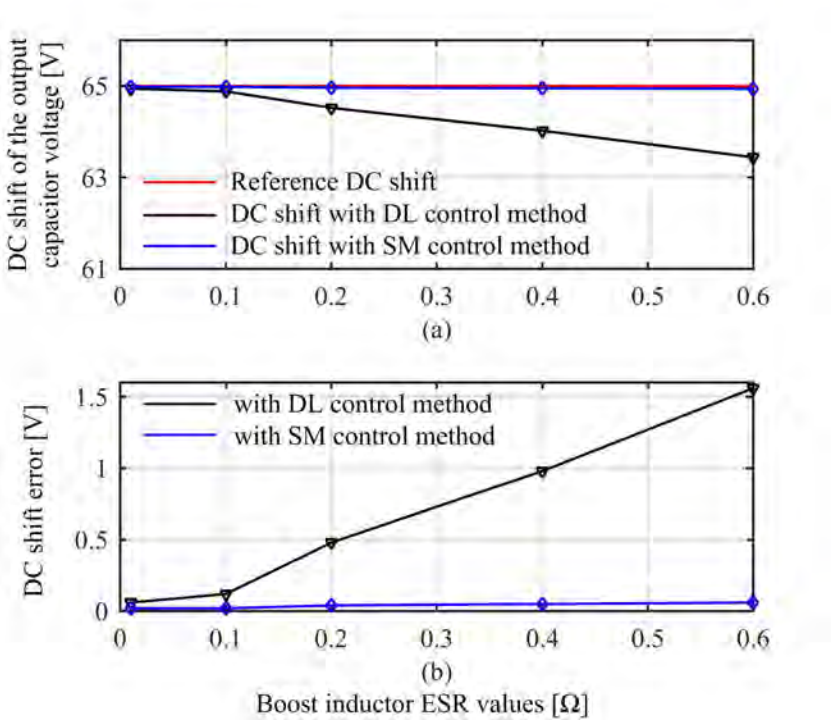

Fig. 5.1: Comparison of the effect of the boost inductor ESR on the output capacitor voltage reference tracking with the double loop control method and with the sliding mode control method, (a) DC shift of the output capacitor voltage and (b) DC shift error of the output capacitor voltage

for a sample case when the HESS supplies 50W active power and 25VAr reactive power to the grid. A significant increment in the output capacitor DC shift error can be observed with the increasing boost inductor ESR values. If the ESR values of the left hand side boost converter leg inductors are different from the right hand side boost converter leg inductors, due to the tolerances and temperature variations, then there are unequal DC voltage shifts in v_{o1} and v_{o2} and hence a DC voltage component ΔV_{DC} appears in the HESS differential output voltage. The DC voltage component results in undesirable DC current flowing into the grid.

The DC component of the HESS output voltage ΔV_{DC}, is given by,

$$\Delta V_{DC} = V_{DC1} - V_{DC2} \tag{5.1}$$

where V_{DC1} and V_{DC2} are the DC shifts of the output capacitor voltages v_{o1} and v_{o2} respectively. Then, the current supplied to the grid, i_g can be written as,

$$i_g = I_o \sin(\omega t + \alpha) + \frac{\Delta V_{DC}}{R_{Lg}} \tag{5.2}$$

where R_{Lg} is the ESR value of the grid interfacing inductor L_g. Hence, a slight DC shift in the HESS output voltage can lead to a significant output current DC component due to the low ESR of the grid interfacing inductor (less than 1Ω). According to the IEEE

standards, it is required to limit the DC current injection to 0.5% of the rated current of the inverter [95].

5.3 Sliding Mode Controller Analysis

The configuration of the boost inverter based battery-supercapacitor HESS is illustrated in Fig. 5.2 and the gate signals for the top switches (subscript T) and for the bottom switches (subscript B) of each converter leg are complementary. In order to design a SM controller for the HESS, the four boost converter legs of the HESS configuration are considered as four subsystems with unique objectives and each boost converter leg can be defined as a single input system. This way of sub-dividing a complex system into several independent single input subsystems is known as decentralized switching scheme and widely used in SM controller design for complex power converters [27,29].

In the SM controller design, the supercapacitor connected left hand side and right hand side boost converter legs are controlled to track the output capacitor reference voltages $v_{o1,ref}$ and $v_{o2,ref}$ where,

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2}\sin(\omega t + \delta) \tag{5.3}$$

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2}\sin(\omega t + \delta). \tag{5.4}$$

The battery connected boost converter legs are controlled in the inductor current controlled mode to facilitate the power allocation of the HESS. In this chapter, SM controller analysis is provided only for the left hand side converter legs, but a similar analysis can be performed for the right hand side converter legs as well.

5.3.1 Left Hand Side Supercapacitor Connected Boost Converter Leg

The objective of the SM controller for the left hand side supercapacitor connected boost converter leg is to follow the output capacitor reference voltage given by (5.3). Equivalent circuit of the left hand side boost converter leg is illustrated in Fig. 5.3. The left hand side battery connected boost converter leg is operated in the inductor current controlled mode as explained later and hence the effect of the left hand side battery connected boost converter leg operation on the supercapacitor connected boost converter leg can be modeled using a current source with i_{obatt1} current as shown in Fig. 5.3. The left hand side supercapacitor connected boost converter leg controller has to control v_{o1} according to the reference voltage $v_{o1,ref}$, irrespective of the current i_{obatt1} which acts as a disturbance to its operation. The internal resistance of the output capacitors, R_{C1}, and R_{C2} are neglected to simplify the analysis.

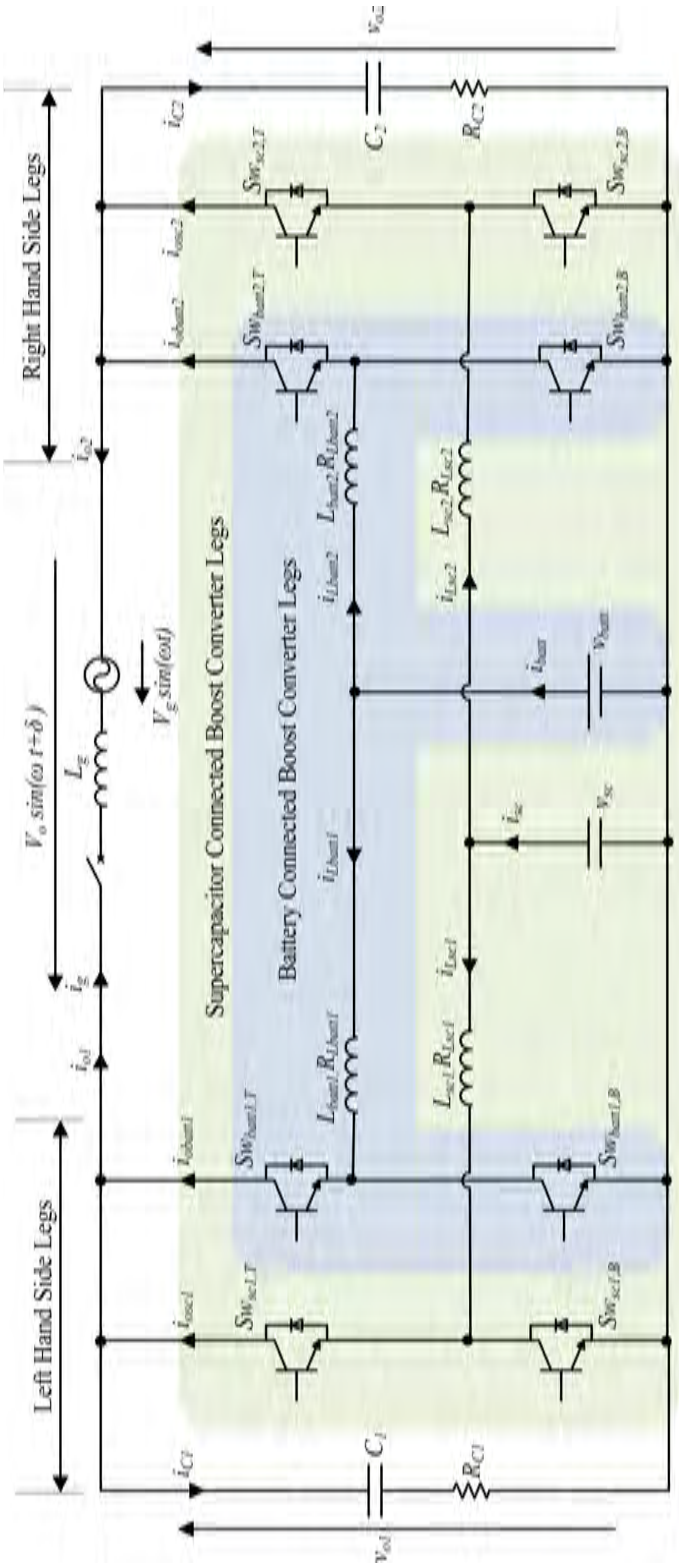

Fig. 5.2: Single-phase grid-connected battery-supercapacitor hybrid energy storage system

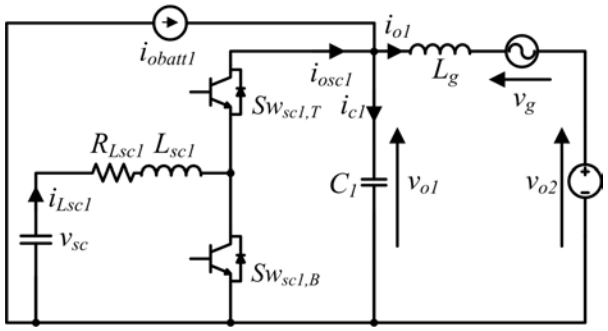

Fig. 5.3: Equivalent circuit of the HESS in the viewpoint of the left hand side supercapacitor connected boost converter leg

The dynamic behavior of the system in the viewpoint of the left hand side supercapacitor connected boost converter leg can be described by following differential equations.

$$\frac{di_{Lsc1}}{dt} = \frac{v_{sc} - i_{Lsc1}R_{Lsc1} - (1-u_{sc1})v_{o1}}{L_{sc1}} \tag{5.5}$$

$$\frac{dv_{o1}}{dt} = \frac{i_{obatt1} - i_{o1} + (1-u_{sc1})i_{Lsc1}}{C_1} \tag{5.6}$$

where u_{sc1} is the logic state of the switch $S_{wsc1,B}$. Sliding surface for the left hand side supercapacitor connected boost converter leg, S_{sc1} is chosen as,

$$S_{sc1} = K_{sc1,a}(v_{o1} - v_{o1,ref}) + K_{sc1,b}\int(v_{o1} - v_{o1,ref})dt + K_{sc1,c}i_{Lsc1} \tag{5.7}$$

with the switching low,

$$u_{sc1} = \begin{cases} 1 & S_{sc1} < 0 \\ 0 & S_{sc1} > 0 \end{cases} \tag{5.8}$$

where $K_{sc1,a}$, $K_{sc1,b}$, and $K_{sc1,c}$ represents the sliding coefficients. Similar sliding surfaces were used in literature to control various power converter configurations with SM control techniques [39, 71, 96–99]. In (5.7), the integral of the voltage error is introduced to reduce the output capacitor voltage tracking error as well as to retain the voltage reference information in the equivalent control input which is obtained by solving $\frac{dS_{sc1}}{dt} = 0$ [96]. Once the sliding mode operation is achieved ($S_{sc1} = 0$), the left hand side supercapacitor connected inductor current is given by,

$$i_{Lsc1} = \frac{K_{sc1,a}}{K_{sc1,c}}(v_{o1,ref} - v_{o1}) + \frac{K_{sc1,b}}{K_{sc1,c}}\int(v_{o1,ref} - v_{o1})dt \tag{5.9}$$

which is similar to traditional inductor current control using the voltage tracking error and its integral [71].

The existence condition of the SM controller for the left hand side supercapacitor connected boost converter leg can be written as,

$$\lim_{S_{sc1}\to 0}\left(S_{sc1}\frac{dS_{sc1}}{dt}\right) < 0 \tag{5.10}$$

Then,

$$\begin{cases} \dfrac{dS_{sc1}}{dt} < 0 & \text{if } S_{sc1} > 0 \\ \dfrac{dS_{sc1}}{dt} > 0 & \text{if } S_{sc1} < 0 \end{cases} \tag{5.11}$$

When $S_{sc1} > 0$, $u_{sc1} = 0$ according to the switching low given in (5.8). Then using (5.5), (5.6), (5.7), and (5.11)

$$K_{sc1,a}\left(\frac{i_{obatt1} - i_{o1} + i_{Lsc1}}{C_1}\right) + K_{sc1,c}\left(\frac{v_{sc} - i_{Lsc1}R_{Lsc1} - v_{o1}}{L_{sc1}}\right) < 0. \tag{5.12}$$

Since the switching frequency is high compared to the frequency of the output capacitor reference voltage, $\dot{v_{o1,ref}} \approx 0$ for SM controller analysis [54]. When $S_{sc1} < 0$, according to the switching law in (5.8), $u_{sc1} = 1$. Using (5.5), (5.6), (5.7), and (5.11),

$$K_{sc1,a}\left(\frac{i_{obatt1} - i_{o1}}{C_1}\right) + K_{sc1,c}\left(\frac{v_{sc} - i_{Lsc1}R_{Lsc1}}{L_{sc1}}\right) > 0. \tag{5.13}$$

The sliding coefficients $K_{sc1,a}$, $K_{sc1,b}$, and $K_{sc1,c}$ must comply with the inequalities (5.12) and (5.13) to satisfy the existence condition of the SM for the left hand side supercapacitor connected boost converter leg. In order to reach the sliding surface from all possible initial conditions, it is sufficient that $(K_{sc1,a}, K_{sc1,b}, K_{sc1,c}) > 0$ provided that SM exists [54].

The equivalent control concept is employed to design the fixed frequency SM controller for the boost inverter based HESS and the equivalent control input for the SM controller is obtained by solving,

$$\frac{dS_{sc1}}{dt} = 0 \tag{5.14}$$

Then, using (5.5), (5.6), and (5.7), the equivalent control input can be obtained as,

$$\bar{u}_{sc1,eq} = \frac{k_{sc1,a}(i_{obatt1} - i_{o1}) + k_{sc1,b}(v_{o1} - v_{o1,ref}) + k_{sc1,c}(v_{sc} - i_{Lsc1}R_{Lsc1})}{k_{sc1,c}v_{o1} - k_{sc1,a}i_{Lsc1}} \tag{5.15}$$

where,

$$\begin{cases} k_{sc1,a} = K_{sc1,a}L_{sc1} \\ k_{sc1,b} = K_{sc1,b}L_{sc1}C_1 \\ k_{sc1,c} = K_{sc1,c}C_1 \end{cases} \tag{5.16}$$

are the fixed gain parameters of the proposed SM controller for the left hand side supercapacitor connected boost converter leg. $\bar{u}_{sc1,eq} = (1 - u_{sc1,eq})$ where $u_{sc1,eq}$ is the equivalent control input to the switches $Sw_{sc1,B}$. Please refer Appendix A.1 for the derivation. If the SM exists for the left hand side supercapacitor connected boost converter leg, $0 < \bar{u}_{sc1,eq} < 1$.

In this chapter, the fixed frequency operation of the SM controller is achieved by using a pulse width modulator. In the pulse width modulation, the duty ratio d is obtained by comparing a control signal against a triangular carrier signal with amplitude v_{tri} [94].

Symmetrical triangular carrier signals in the range of 0 and 1 are used in pulse width modulation. Then,

$$0 < \left[d = \frac{v_c}{v_{tri}} \right] < 1 \tag{5.17}$$

The equivalent control input for the SM controller corresponds to the duty ratio of the PWM control method [94]. By equating $\bar{u}_{sc1,eq} = d$ and using (5.15) and (5.17), the SM controller can be implemented using a control signal $v_{c,sc1}$ and a triangular carrier signal with $v_{tri,sc1}$ amplitude as,

$$\begin{aligned} v_{c,sc1} &= k_{sc1,m}[k_{sc1,a}(i_{obatt1} - i_{o1}) + k_{sc1,b}(v_{o1} - v_{o1,ref}) + k_{sc1,c}(v_{sc} - i_{Lsc1}R_{Lsc1})] \\ &= k_{sc1,ma}(i_{obatt1} - i_{o1}) + k_{sc1,mb}(v_{o1} - v_{o1,ref}) + k_{sc1,mc}(v_{sc} - i_{Lsc1}R_{Lsc1}) \end{aligned} \tag{5.18}$$

and

$$\begin{aligned} v_{tri,sc1} &= k_{sc1,m}\left[k_{sc1,c}v_{o1} - k_{sc1,a}i_{Lsc1}\right] \\ &= k_{sc1,mc}v_{o1} - k_{sc1,ma}i_{Lsc1} \end{aligned} \tag{5.19}$$

where $k_{sc1,m}$ is a scaling factor introduced to scale the carrier signal amplitude to a practical magnitude level. The controller gains $k_{sc1,a}$, $k_{sc1,b}$ and $k_{sc1,c}$ have to be selected to ensure the reaching and existence condition of the SM.

5.3.2 Left Hand Side Battery Connected Boost Converter Leg

The equivalent circuit of the battery-supercapacitor HESS in the viewpoint of the left hand side battery connected boost converter leg can be illustrated as in Fig. 5.4. The battery connected boost converter legs are controlled in the inductor current control mode in order to facilitate the power allocation between the battery and the supercapacitor. Since the left hand side supercapacitor connected boost converter leg is used to control the output capacitor voltage v_{o1}, the effect of the left hand side supercapacitor connected boost converter leg on the left hand side battery connected boost converter leg operation can be modeled using a voltage source with v_{o1} amplitude as illustrated in the equivalent circuit shown in Fig. 5.4. The dynamic behavior of the left hand side battery connected boost converter leg can be described by following differential equation.

$$\frac{di_{Lbatt1}}{dt} = \frac{v_{batt} - i_{Lbatt1}R_{Lbatt1} - (1 - u_{batt1})v_{o1}}{L_{batt1}} \tag{5.20}$$

where, the logic state of the switch $Sw_{batt1,B}$ is denoted as u_{batt1}. The sliding surface for the left hand side battery connected boost converter leg is selected to mitigate the inductor current tracking error and its integral as

$$S_{batt1} = (i_{Lbatt1} - i_{Lbatt1,ref}) + K_{batt1}\int (i_{Lbatt1} - i_{Lbatt1,ref})dt \tag{5.21}$$

with the switching law,

$$u_{batt1} = \begin{cases} 1 & S_{batt1} < 0 \\ 0 & S_{batt1} > 0 \end{cases} \tag{5.22}$$

where K_{batt1} represents the sliding coefficient. $i_{Lbatt,ref}$ is the inductor current reference signal which is generated by the HESS power allocation method explained in Section 5.3.4. Existence condition of the considered SM is given by,

$$\lim_{S_{batt1} \to 0} \left(S_{batt1} \frac{dS_{batt1}}{dt} \right) < 0 \tag{5.23}$$

Using (5.20), (5.21), and (5.22), the existence condition in (5.23) when $S_{batt1} < 0$ and $S_{batt1} > 0$ can be simplified as,

$$\frac{v_{batt} - i_{Lbatt1} R_{Lbatt1}}{L_{batt1}} > 0 \tag{5.24}$$

and

$$\frac{(v_{batt} - i_{Lbatt1} R_{Lbatt1}) - v_{o1}}{L_{batt1}} < 0 \tag{5.25}$$

respectively. With the inherent operation of the boost converter, it can be seen that $v_{batt} - i_{Lbatt1} R_{Lbatt1} > 0$ and $(v_{batt} - i_{Lbatt1} R_{Lbatt1}) - v_{o1} < 0$. Because of that, the existence condition for the SM is satisfied. Similar to the previous case, the equivalent control input for the SM can be obtain as,

$$\bar{u}_{batt,eq} = \frac{v_{batt} - i_{Lbatt1} R_{Lbatt1} + k_{batt1}(i_{Lbatt1} - i_{Lbatt1,ref})}{v_{o1}} \tag{5.26}$$

where

$$k_{batt1} = K_{batt1} L_{batt1} \tag{5.27}$$

is the fixed gain parameter for the left hand side battery connected boost converter leg. Please refer Appendix A.1 for the derivation. $\bar{u}_{batt1,eq} = (1 - u_{batt,eq})$ where $u_{batt,eq}$ is the equivalent control input to the switch $Sw_{batt1,B}$. Then,

$$0 < \left[\bar{u}_{batt,eq} = \frac{v_{batt} - i_{Lbatt1} R_{Lbatt1} + k_{batt1}(i_{Lbatt1} - i_{Lbatt1,ref})}{v_{o1}} \right] < 1. \tag{5.28}$$

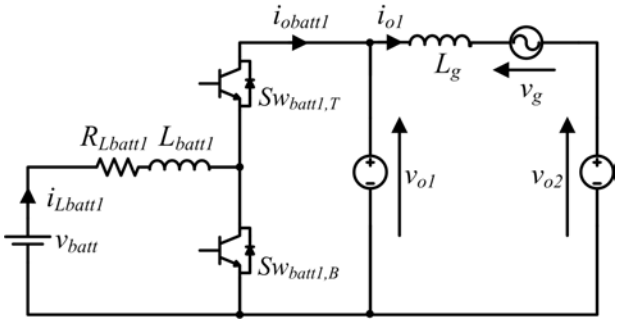

Fig. 5.4: Equivalent circuit of the HESS in the viewpoint of the left hand side battery connected boost converter leg

The SM controller for the left hand side battery connected boost converter leg can be implemented using a control signal $v_{c,batt1}$ and a triangular carrier signal with amplitude $v_{tri,batt1}$ as,

$$v_{c,batt1} = k_{batt1,m}\left[v_{batt} - i_{Lbatt1}R_{Lbatt1} + k_{batt1}(i_{Lbatt1} - i_{Lbatt1,ref})\right] \tag{5.29}$$

and

$$v_{tri,batt} = k_{batt1,m}v_{o1}. \tag{5.30}$$

In equations (5.29) and (5.30), a scaling factor $k_{batt1,m}$ is used to scale the carrier signal amplitude to a practical magnitude level.

Fig. 5.5 represents the block diagram of the SM controller for the boost inverter based battery-supercapacitor HESS.

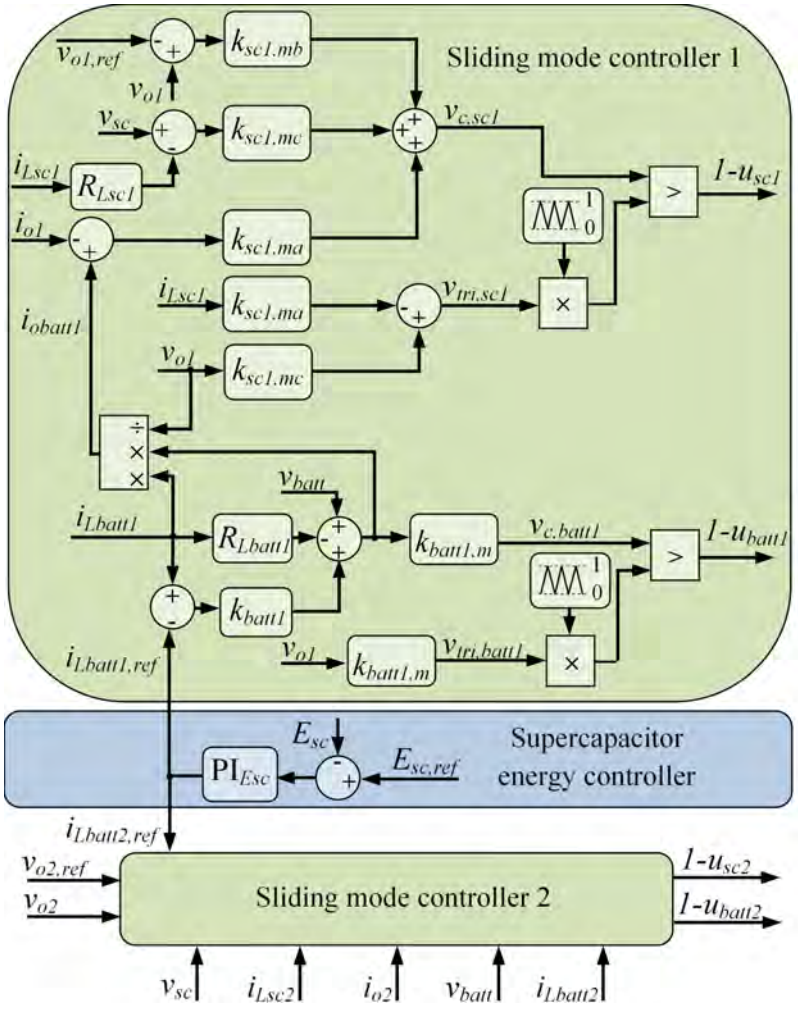

Fig. 5.5: Block diagram of the proposed sliding mode controller.

5.3.3 Sliding Coefficients Selection for the HESS

The sliding coefficients of the SM controller have to be selected properly to satisfy the SM existence and reaching conditions. This has to be done considering the worst case operation of the system. The worst case operation of the supercapacitor connected boost converter leg occurs when the total power requirement of the HESS is allocated to the supercapacitor. Then, the existence condition for the left hand side supercapacitor connected boost converter leg SM controller can be re-written as,

$$max\left[K_{sc1,a}\left(\frac{-i_{o1}+i_{Lsc1}}{C_1}\right)+K_{sc1,c}\left(\frac{v_{sc}-v_{o1}}{L_{sc1}}\right)\right]<0 \tag{5.31}$$

$$min\left[K_{sc1,a}\left(\frac{-i_{o1}}{C_1}\right)+K_{sc1,c}\left(\frac{v_{sc}}{L_{sc1}}\right)\right]>0 \tag{5.32}$$

The HESS output current is given by,

$$i_{o1}=I_o\sin(\omega t+\alpha) \tag{5.33}$$

Then, the supercapacitor current when the total power requirement is allocated to the supercapacitor can be written as,

$$i_{Lsc1}=\frac{v_{o1}(i_{o1}+i_{c1})}{v_{sc}} \tag{5.34}$$

In order to simplify the analysis, the effect of the output capacitor current on i_{Lsc1} and the switching frequency ripple component can be neglected [72]. Furthermore, $\delta\approx 0$ and $V_o\approx V_g$. Then using (5.31), (5.32), and (5.34), the existence condition of the left hand side supercapacitor connected boost converter leg SM controller can be simplified as,

$$0<\frac{K_{sc1,a}}{K_{sc1,c}}<\frac{v_{sc,min}C_1}{I_{o,max}L_{sc1}} \tag{5.35}$$

Using (5.16), the controller gains $k_{sc1,a}$ and $k_{sc1,c}$ have to be selected such that,

$$0<\frac{k_{sc1,a}}{k_{sc1,c}}<\frac{v_{sc,min}}{I_{o,max}} \tag{5.36}$$

The inequality (5.36) provides the basis for the selection of the controller gains.. Then, a simulation and experimental analysis based empirical approach can be followed as explained in [94] to obtain the exact values for the SM controller gains.

5.3.4 HESS Power Allocation

The objective of the HESS power allocation method is to divert the second-order harmonic ripple current component and the fast power fluctuations to the supercapacitor while the battery supplies a slow varying power component. The power variations

greater than a pre-determined cut-off frequency, $\omega_{c,req}$ are considered as fast power fluctuations. Since the supercapacitor connected boost converter legs are used to control the output capacitor voltages, the second-order harmonic ripple component is supplied by the supercapacitor. In this chapter, a supercapacitor energy controller is used i) to maintain the stored energy in the supercapacitor around a reference energy level and ii) to allocate the fast power fluctuations to the supercapacitor. To achieve foregoing objectives, a PI controller is required in the SCEC as explained later. The current reference signals for the battery connected boost converter legs $i_{Lbatt1,ref}$ and $i_{Lbatt2,ref}$ are generated as,

$$i_{Lbatt1,ref} = i_{Lbatt2,ref} = \left(K_{p,Esc} + \frac{K_{i,Esc}}{s}\right)(E_{sc,ref} - E_{sc}) \tag{5.37}$$

where, $K_{p,Esc}$, $K_{i,Esc}$, E_{sc}, and $E_{sc,ref}$ are the proportional and integral gains of the PI controller, stored energy in the supercapacitor, and the reference energy level of the supercapacitor, respectively (See Fig. 5.5). The stored energy in the supercapacitor is given by,

$$E_{sc} = \frac{1}{2}C_{sc}v_{sc}^2 \tag{5.38}$$

where C_{sc} is the capacitance value of the supercapacitor.

In order to analyze the dynamic behavior of the HESS power allocation method, an equivalent block diagram as illustrated in Fig. 5.6 is considered. In Fig. 5.6, P_{HESS}, η, P_{tot}, P_{sc}, P_{batt}, dE_{sc}, and $E_{sc,init}$ are the output power supplied by the HESS, efficiency of the HESS, total power requirement from the battery and the supercapacitor, power supplied by the supercapacitor, power supplied by the battery, change in the supercapacitor energy, and the initial energy level of the supercapacitor, respectively. Then, the relationship between the power supplied by the battery and P_{tot} can be obtained as,

$$P_{batt} = \left(\frac{A_1 s + A_2}{s^2 + A_1 s + A_2}\right)P_{tot} + \left(\frac{A_1 s^2 + A_2 s}{s^2 + A_1 s + A_2}\right)(E_{sc,ref} - E_{sc,init}) \tag{5.39}$$

where, $A_1 = 2v_{batt}K_{p,Esc}$, $A_2 = 2v_{batt}K_{i,Esc}$ and $P_{tot} = P_{batt} + P_{sc}$. Please refer Appendix A.1 for the derivation. A transfer function between the power supplied by the battery,

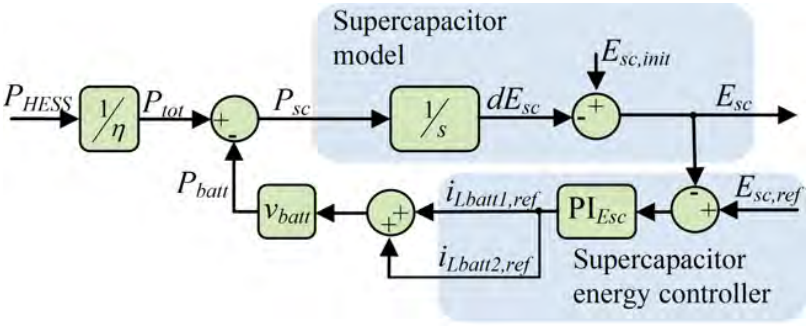

Fig. 5.6: Equivalent block diagram of the HESS power allocation

P_{batt} and the total output power of the HESS, P_{HESS} can be obtained assuming $E_{sc,init} = E_{sc,ref}$ as,

$$H_{Pbatt} = \frac{P_{batt}}{P_{HESS}} = \left(\frac{A_1 s + A_2}{s^2 + A_1 s + A_2}\right)\frac{1}{\eta} \tag{5.40}$$

Further, a transfer function between the power supplied by the supercapacitor, P_{sc} and P_{HESS} can be obtained as,

$$H_{Psc} = \frac{P_{sc}}{P_{HESS}} = \left(\frac{s^2}{s^2 + A_1 s + A_2}\right)\frac{1}{\eta} \tag{5.41}$$

Then, the transfer function between dE_{sc} and P_{HESS} can be written as,

$$H_{dEsc} = \frac{dE_{sc}}{P_{HESS}} = \left(\frac{s}{s^2 + A_1 s + A_2}\right)\frac{1}{\eta} \tag{5.42}$$

It can be observed that H_{Pbatt} has one zero z_1 and two poles p_1 and p_2,

$$z_1 = \frac{K_{i,Esc}}{K_{p,Esc}} \tag{5.43}$$

$$p_1, p_2 = -v_{batt}K_{p,Esc} \pm \sqrt{v_{batt}^2 K_{p,Esc}^2 - 2v_{batt}K_{i,Esc}}. \tag{5.44}$$

For real system poles,

$$K_{i,Esc} \leq \frac{v_{batt}K_{p,Esc}^2}{2} \tag{5.45}$$

and further it can be shown that $p_1, p_2 < z_1$ for positive non zero $K_{p,Esc}$ and $K_{i,Esc}$ values. Using the relationships, an asymptotic Bode plot of H_{Pbatt} can be drawn as Fig. 5.7 when poles of the H_{Pbatt} are real. Using the Bode plot, the gain cross-over frequency of H_{Pbatt}, ω_c can be derived as,

$$\omega_c = \frac{|p_1| \times |p_2|}{|z_1|} = 2K_{p,Esc}v_{batt} \tag{5.46}$$

In order to observe the dynamic behavior of H_{Pbatt} with different PI controller parameters, a sample gain cross-over frequency of 0.05 rads^{-1}, the same gain cross-over frequency considered in Chapter 4, is considered. Figs. 5.8 (a), 5.8 (b) and 5.8 (c) illustrate the pole-zero plot of H_{Pbatt}, the step responses of H_{Pbatt}, and the step response of H_{dEsc} for the considered sample gain cross-over frequency. When $K_{i,Esc} = 0$, the system

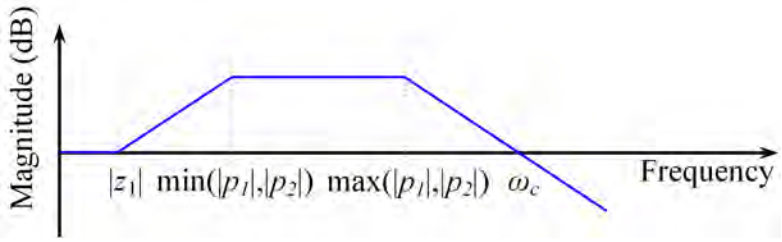

Fig. 5.7: Asymptotic Bode plot of H_{Pbatt} with real system poles

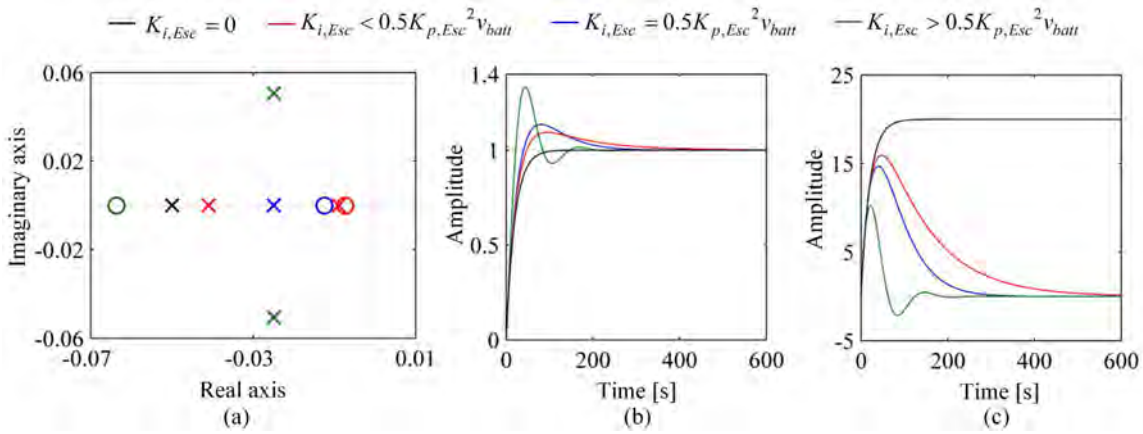

Fig. 5.8: Effect of $K_{p,Esc}$ and $K_{i,Esc}$ on H_{Pbatt} and H_{dEsc}. (a) pole zero plot of H_{Pbatt}, (b) step response of H_{Pbatt} and (c) step response of H_{dEsc}.

is first order and the step response of H_{Pbatt} demonstrates a low pass filter characteristic. Further it can be observed from Fig. 5.8 (c) that the battery does not recharge the supercapacitor and hence, in the steady state $d_{Esc} \neq 0$. When $K_{i,Esc} < 0.5K_{p,Esc}^2 v_{batt}$, the system is second order and the system poles are real. According to the step response in Fig. 5.8 (b), the battery response shows a low pass filter characteristic and the battery supplies an additional amount of power to recharge the supercapacitor to the reference energy level. When $K_{i,Esc} = 0.5K_{p,Esc}^2 v_{batt}$, the poles of the system coincide and the system is critically damped. When $K_{i,Esc} > 0.5K_{p,Esc}^2 v_{batt}$, the poles of the system becomes imaginary and hence, an oscillatory behavior can be observed in the step response which is not desirable in the battery-supercapacitor HESS operation. It can be observed that the fastest battery response with supercapacitor recharging is occurred in the critically damped system.

In this chapter, the PI controller parameters for the SCEC are calculated to obtain the critically damped operation as follows. First, the proportional gain $K_{p,Esc}$ is calculated to achieve the required gain cross-over frequency $\omega_{c,req}$ using,

$$K_{p,Esc} = \frac{\omega_{c,req}}{2v_{batt}} \tag{5.47}$$

Then, $K_{i,Esc}$ is selected to obtain the critically damped system as,

$$K_{i,Esc} = \frac{K_{p,Esc}^2 v_{batt}}{2}. \tag{5.48}$$

5.3.5 Supercapacitor Selection for the SM Controlled HESS

Using the parameters selected for the SCEC, the required capacitor value for the supercapacitor can be calculated for a given application as follows.

First, the maximum and minimum voltage limits for the supercapacitor, $v_{sc,max}$ and $v_{sc,min}$ has to be identified based on the power converter specification. Based on the

voltage limits, the utilized energy of the supercapacitor can be obtained by,

$$E_{sc,u} = 0.5C_{sc}\left(v_{sc,max}^2 - v_{sc,min}^2\right) \tag{5.49}$$

The reference energy level for the supercapacitor can be selected such that equal amount of energy is available for both the supercapacitor charging and discharging as,

$$E_{sc,ref} = 0.5C_{sc}v_{sc,min}^2 + 0.5E_{sc,u} \tag{5.50}$$

For a considered application, the supercapacitor energy variation due to the HESS operation, dE_{sc} can be estimated from (5.42). Then, using the maximum value of the supercapacitor energy variation, $max(|dE_{sc}|)$ the required capacitance value for the supercapacitor can be calculated as,

$$C_{sc,req} = \frac{4max(|dE_{sc}|)}{v_{sc,max}^2 - v_{sc,min}^2} \tag{5.51}$$

5.4 Experimental Results

The performance of the SM controlled HESS is verified using a low voltage low power prototype. A 9.6Ah, 25.6V $LiFePO_4$ battery from K2 Energy and two 16V, 58F Maxwell supercapacitor modules connected in series are used in the prototype and the parameters of the HESS prototype are summarized in Table 5.1. The controllers are implemented on a DSpace DS1006 platform.

Operation of the battery-supercapacitor HESS when the system delivers 50W active power and 25VAr reactive power to the grid is illustrated in Figs. 5.9, 5.10, and 5.11. The output capacitor voltages v_{o1}, v_{o2}, and the HESS output voltage v_o are illustrate in Fig. 5.9. The operation of the active and reactive power controller is illustrates in Fig. 5.10. It can be observed that the power exchange between the HESS and the grid is achieved by changing the HESS output voltage amplitude and phase angle with respect to

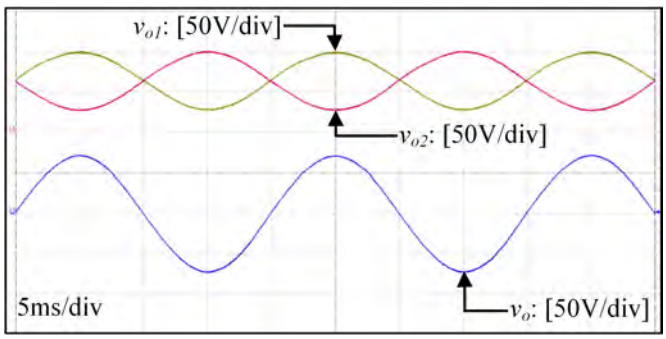

Fig. 5.9: The output capacitor voltage waveforms v_{o1} and v_{o2}, and the HESS output voltage v_o when the HESS delivers 50W active power and 25VAr reactive power to the grid

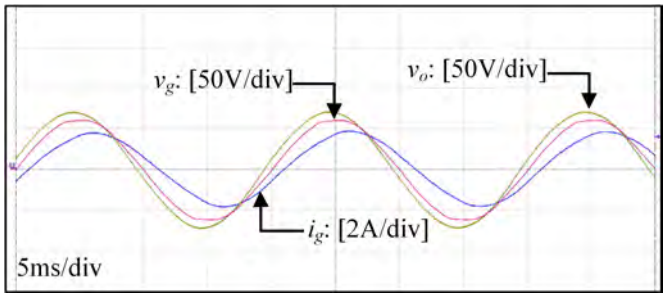

Fig. 5.10: The grid voltage v_g, the HESS output voltage v_o and the HESS output current i_g when the HESS delivers 50W active power and 25VAr reactive power to the grid

the grid voltage. The left hand side supercapacitor connected and the battery connected inductor current waveforms i_{Lsc1} and i_{Lbatt1} are illustrates in Fig. 5.11. As required, the supercapacitor supplies the required ripple current component while the battery supplies the required average current component.

Operation of the SM controlled battery-supercapacitor HESS with a step changing output power profile is illustrates in Fig. 5.12. In this experiment, a gain cross-over

Table 5.1: Hybrid energy storage system parameters

Parameter	**Value**	**Parameter**	**Value**
Power converter parameters			
V_o	60 V	$V_{DC,ref}$	60 V
L_{batt1},L_{batt2}	210 μH	L_{sc1},L_{sc2}	210 μH
C_1, C_2	60 μF	f	50 Hz
$v_{sc,max}$	28 V	$v_{sc,min}$	20 V
R_{Lsc1}, R_{Lsc2}	0.24 Ω	R_{Lbatt1}, R_{Lbatt2}	0.24 Ω
R_{Lg}	0.2		
Grid parameters			
V_g	60 V	L_g	20 mH
Sliding mode controller parameters			
$k_{sc1,a}$	2.73 $\times 10^{-4}$	$k_{sc1,b}$	8.19×10^{-5}
$k_{sc1,c}$	8.7×10^{-5}	k_{batt1}	3.78
$k_{sc1,m}$	200	$k_{batt1,m}$	0.02
f_{sw}	20 kHz		
PQ controller parameters			
$K_p(PI_P)$	2×10^{-6}	$K_p(PI_Q)$	1×10^{-5}
$K_i(PI_P)$	0.14	$K_i(PI_Q)$	4

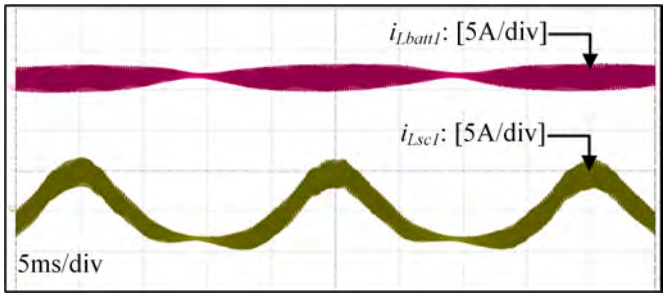

Fig. 5.11: The inductor current waveforms i_{Lbatt1} and i_{Lsc1} when the HESS delivers 50W active power and 25VAr reactive power to the grid

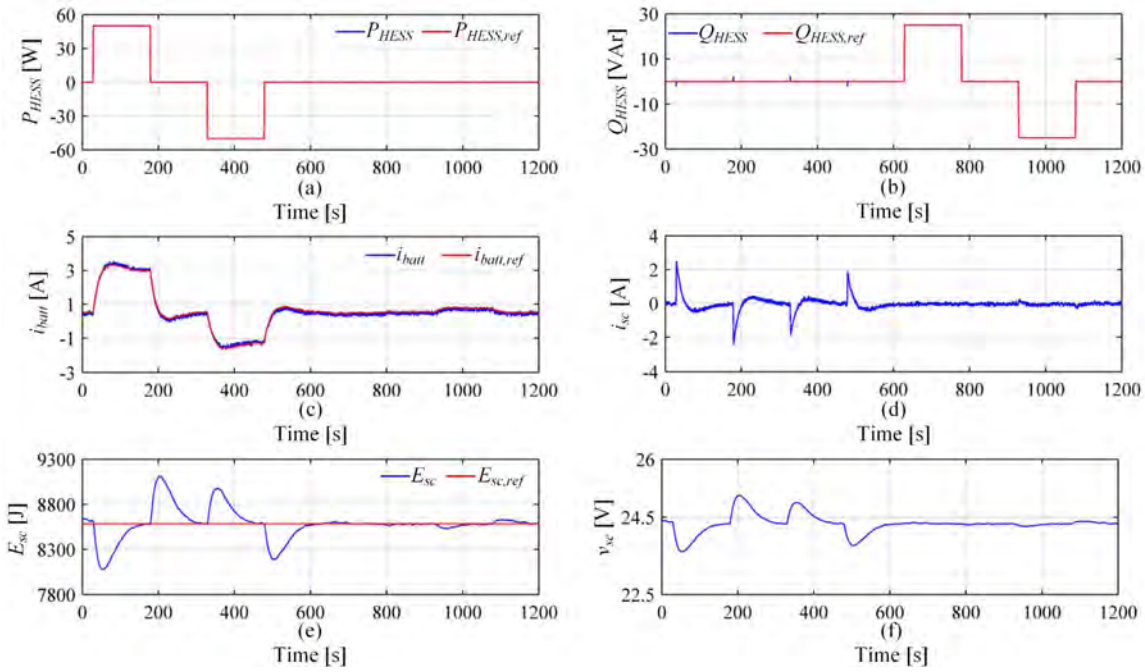

Fig. 5.12: Experimental waveforms illustrating the operation of the HESS: Supercapacitor responds to sudden power changes.

frequency of 0.1 rad^{-1} is considered to illustrate the performance of the system. The gain cross-over frequency, and hence the SCEC parameters, should be selected based on the specific application at the design stage of the HESS. In this experiment, the SCEC parameters $K_{p,Esc}$ and $K_{i,Esc}$ were selected as 0.00195 and 4.87×10^{-5} to obtain 0.1 rad^{-1} gain cross-over frequency and a 29F supercapacitor is employed. It is evident that the supercapacitor responds to the sudden power variations as shown in Fig. 5.12 (d) and hence the stored energy in the supercapacitor diverts from the reference energy level as in Fig. 5.12 (e). In Fig. 5.12 (d), the double line frequency component of the supercapacitor current is filtered out to illustrate the supercapacitor response to the sudden power changes clearly. The battery current gradually increases to provide the required DC power component and the battery supplies an additional power component to recharge the

supercapacitor back to the reference energy level as illustrates in Fig. 5.12(c) and (e).

Next, the operation of the SM controlled HESS in a PV power smoothing application as discussed in Chapter 4 is considered. A 900s HESS reference power profile as shown in Fig. 5.13 (a) is generated to emulate the HESS operation in a PV power smoothing application. The SCEC parameters are selected as $K_{p,Esc} = 3.92 \times 10^{-4}$ and $K_{i,Esc} = 1.97 \times 10^{-6}$ to obtain a 0.02 rads^{-1} gain cross-over frequency. Then, the required supercapacitor size for the considered output power profile is obtained from (5.51) as 26.3F. Hence, a commercially available 29F supercapacitor is used in the experiment. Fig. 5.13 (b) illustrates the power supplied by the battery, P_{batt} the power supplied by the supercapacitor, P_{sc} and the total power supplied by the battery and the supercapacitor, P_{tot}. As expected the supercapacitor responds to the high frequency power variations while the battery supplies the slow varying power component. Furthermore, it can be observed that the HESS is able to reduce the peak battery power as well as the number of battery charge discharge cycles. The supercapacitor energy variation is depicted in Fig. 5.13 (c) and it is controlled around the reference supercapacitor energy level. From Fig. 5.13 (d) it is evident that the selected capacitance value enables the operation of the supercapacitor within the pre-defined voltage limits. The battery and the supercapacitor current waveforms are shown in Figs. 5.13 (e) and 5.13 (f) and as required the battery supplies the slow varying current while the supercapacitor supplies the fast varying current component.

In order to observe the effect of the boost inductor ESR tolerance on the HESS output

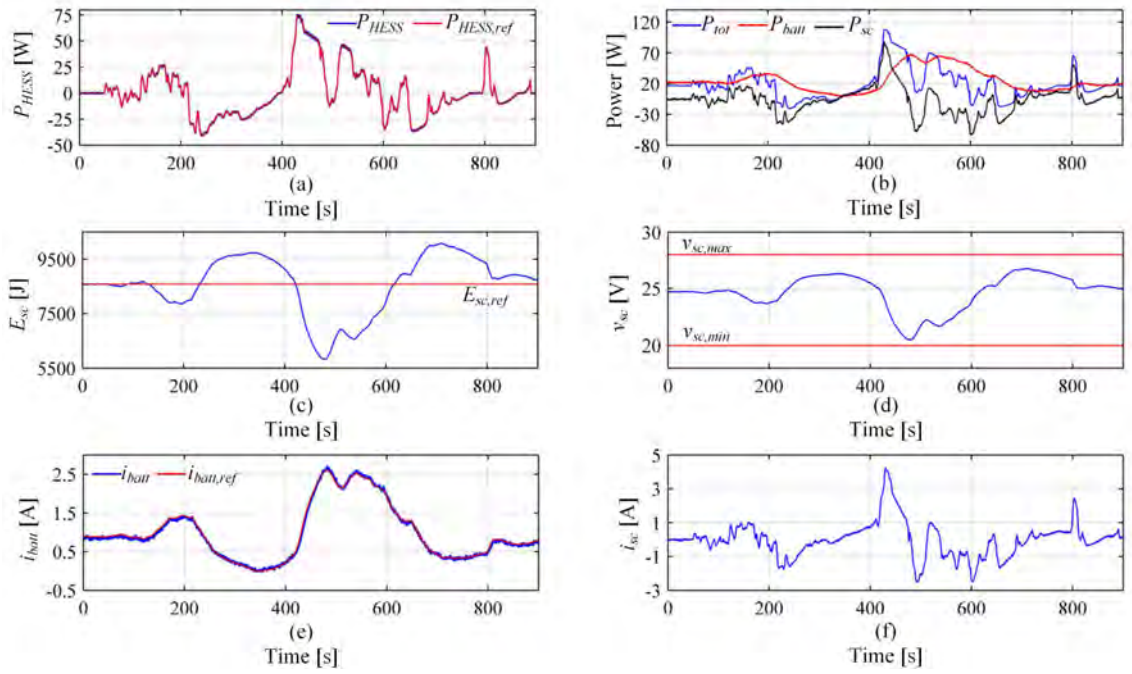

Fig. 5.13: Experimental waveforms illustrating the operation of the HESS in a PV power smoothing application.

current DC component, a 20% change in the nominal ESR value of 0.24Ω was simulated. A sample HESS output power condition of P_{HESS}=50W and Q_{HESS}=25VAr was considered and the boost inductor ESR values were selected as, $R_{Lsc1} = R_{Lbatt1} = 0.24 \times 0.8\Omega$ and $R_{Lsc2} = R_{Lbatt2} = 0.24 \times 1.2\Omega$. The SM controller was calculated using the nominal boost inductor ESR value. A DC component of 0.0814A which is 4.07% of the HESS rated output current was observed in the HESS output current with the DL control method. However, with the SM controller, the DC current component was only 0.0046A which is 0.23% of the HESS rated output current. According to the IEEE standards, it is required to limit the DC current injection to 0.5% of the rated current of the inverter [95]. This result demonstrates the advantage of the SM control method which is robust to parameters variation and therefore is unaffected by the ESR variation.

5.5 Conclusions

A fixed frequency SM controller for a boost inverter based single phase grid connected battery-supercapacitor HESS was presented in this chapter. The PWM based fixed frequency SM controller was employed to overcome high and variable frequency operation associated with the traditional SM control technique. Theoretical aspects of the SM controller design were discussed, and a SCEC based power allocation method was employed to allocate the fast power fluctuations to the supercapacitor without incorporating an additional filter. The power allocation parameter selection and the supercapacitor sizing were discussed for a given HESS application. The proposed control system for the boost inverter based HESS was experimentally verified using a laboratory prototype. The proposed controller was able to satisfy the HESS output power requirement while allocating the ripple current and fast power fluctuations to the supercapacitor. Moreover, the selected HESS power allocation parameters and the value of the supercapacitor enabled the operation of the HESS within the pre-determined supercapacitor voltage limits. Compared to the traditional DL controlled boost inverter based battery-supercapacitor HESS, the proposed SM controller was able to achieve better output capacitor reference tracking and hence reduce the risk of the DC current injection into the grid when the ESR values of the boost inductors become unequal due to the tolerances and temperature variations.

Chapter 6

A Rule-Based Controller to Mitigate DC-Side Second-Order Harmonic Current in a Single Phase Boost Inverter

In the HESS operation presented in the previous chapters, the second-order harmonic ripple current component was allocated to the supercapacitor and this leads to a supercapacitor lifetime reduction due to its internal heating. The objective of this chapter is to identify a suitable second-order harmonic ripple current reduction method for the boost inverter based battery-supercapacitor HESS. In order to simplify the analysis, only operation of a single boost inverter for a battery energy storage system is considered.

In this chapter, a rule-based control ripple current reduction method proposed in [67] for a boost inverter based battery energy storage system is presented. Operation of the existing waveform control ripple current reduction method is extensively analyzed. A key feature and advantage of the proposed controller compared to the waveform control ripple reduction method is its ability to reduce the ripple current amplitude in all four inverter output power operating quadrants without being affected by the capacitor tolerances and the equivalent series resistance (ESR) values of the inductors. Presented experimental results validate the performance of the proposed controller on a single-phase grid-connected DC/AC boost inverter based battery energy storage system (ESS).

6.1 Introduction

An interleaved boost inverter based single phase grid integrated battery-supercapacitor HESS was discussed in Chapter 3 to Chapter 5. The single-phase conversion from DC to AC using the boost inverter topology introduced a second-order harmonic ripple current at the DC side of the converter and hence the DC sources had to handle the ripple current component.

The effect of the low frequency current ripple on DC ESSs has been studied in the literature extensively. In [11], the authors reported low frequency ripple current can considerably degrade the lifetime of a lead acid battery due to internal heating. Furthermore, [13] reported a noticeable temperature increment in a Lithium Iron Phosphate (LFP) battery based community ESS, as a result of the low frequency ripple current component. In the power allocation methods discussed in Chapter 3 to Chapter 5, the second-order harmonic ripple current component was allocated to the supercapacitor as a way of extending the battery life time. However, [61] reported that a supercapacitor can also overheat when exposed to a continuous ripple current which in turn leads to deterioration of its lifetime.

A number of second-order harmonic ripple current reduction methods for the single-phase boost inverter topology have been presented in the technical literature [57, 74–78, 100] and can be classified into passive and active ripple current reduction methods. In the passive methods, a separate energy storage device is added to the converter to supply the second-order harmonic ripple current component while in the active methods, a modulation or control scheme is employed to reduce the ripple current component without incurring additional hardware. In [57,78], authors proposed a separate battery storage to compensate the second-order harmonic ripple current in a boost inverter based fuel cell ESS. However such method required additional hardware and cost and also it leads to a lifetime reduction in the battery. In the case of active methods, a waveform control method was studied in [74–77, 100] for a boost inverter based ESSs and in [74] authors reported a noticeable efficiency increase in the ESS due to the second-order harmonic ripple current reduction. However, the method has to be redesigned every time the load changes. A current feedback method for the boost-inverter waveform controller to deal with the changing load conditions was proposed in [75]. However, only the unity power factor operation was considered limiting its applicability for a boost-inverter ESS which is required to operate in all four output power quadrants. The waveform control method was extended to all possible output power conditions in [76]. In [74–77, 100], the compensation signal parameters were calculated using an ideal boost inverter model.

Hence, the effectiveness of the second-order harmonic ripple reduction was affected by the capacitance tolerance of the inverter output capacitors. In addition, the waveform control method cannot compensate for the effect of the ESR values of the inductors on the ripple. Also, the waveform control method in [74–77, 100] is not directly applicable to a grid connected boost inverter since in the grid connected boost inverter the output power control is achieved by changing the inverter output voltage amplitude and phase angle with respect to the grid voltage.

In this chapter, the waveform control ripple current reduction method is extended to the grid connected operation and the effects of the capacitor tolerances and the ESR values of the inductors on its effectiveness are analyzed. Then, a rule-based controller is proposed to reduce the second-order harmonic ripple current in the boost inverter based ESS. The main advantage of the proposed controller is that it can reduce the second-order harmonic ripple current in all four output power quadrants without being affected by the capacitor tolerances and the ESR values of the inductors. The effectiveness of the proposed controller is experimentally verified on a single-phase grid-connected DC/AC boost inverter based battery ESS prototype and it is shown that its performance is superior when compared with the waveform control method.

6.2 Second-Order Harmonic Ripple Current Analysis and Reduction Using the Waveform Control Method

6.2.1 Second-Order Harmonic Input Current Component in the Boost Inverter

The configuration of a single phase grid connected boost inverter is shown in Fig. 6.1 and the operation of the boost inverter was discussed in Chapter 2. The voltages across the output capacitors C_1 and C_2 are controlled to follow voltage references given by,

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2}\sin(\omega t + \delta) \tag{6.1}$$

and

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2}\sin(\omega t + \delta). \tag{6.2}$$

respectively. V_o, ω, and δ are the inverter output voltage amplitude, frequency and phase angle respectively. The boost inverter output current i_o is given by,

$$i_o = I_o \sin(\omega t + \alpha) \tag{6.3}$$

where α is the phase angle of the inverter output current with respect to the grid voltage. The output capacitor currents i_{C1} and i_{C2} are,

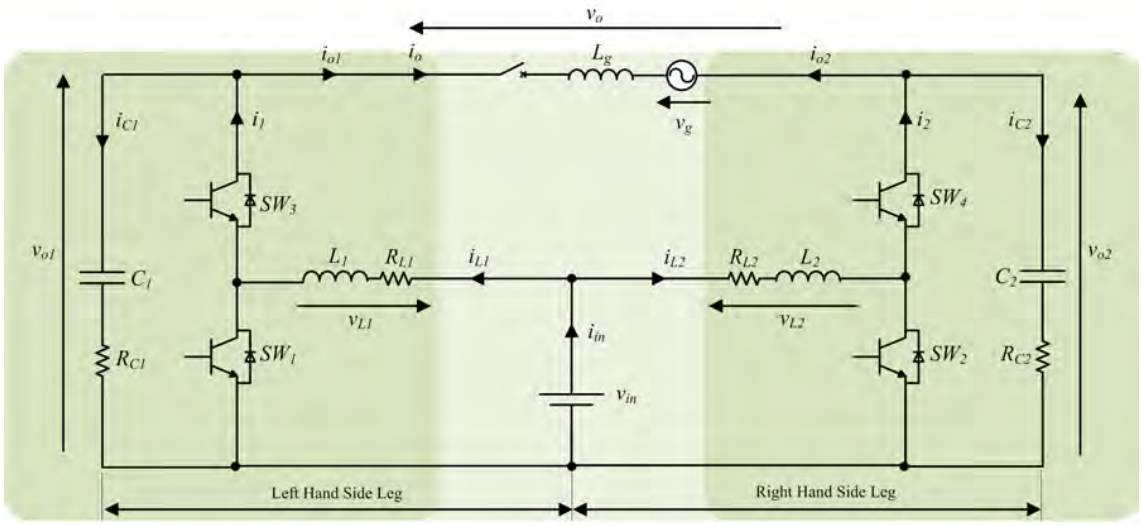

Fig. 6.1: Single phase grid connected boost inverter

$$i_{C1} = C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{6.4}$$

$$i_{C2} = -C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{6.5}$$

From (6.4) and (6.5), the capacitor current waveforms are in fundamental frequency. Using (6.1)-(6.5),

$$i_1 = I_o\sin(\omega t + \alpha) + C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{6.6}$$

Similarly, i_2 can be written as,

$$i_2 = -I_o\sin(\omega t + \alpha) - C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{6.7}$$

Then, the total input current to the boost inverter can be obtained as,

$$i_{in} = i_1\frac{v_{o1}}{v_{in}} + i_2\frac{v_{o2}}{v_{in}} \tag{6.8}$$

Then,

$$i_{in} = \frac{1}{v_{in}}\left[\frac{V_oI_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t - \theta)\right] \tag{6.9}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \frac{C\omega V_o\sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}}$$

and $C = C_1 = C_2$. A detailed analysis when $C_1 \neq C_2$ can be found in [101]. The magnitude and phase angle of the second-order harmonic ripple component depend on the

inverter output current and the phase angle, and hence depend on the inverter output power. The inductor current waveforms i_{L1} and i_{L2} can be obtained using

$$i_{L1} = i_1 \frac{v_{o1}}{v_{in}} \tag{6.10}$$

and

$$i_{L2} = i_2 \frac{v_{o2}}{v_{in}} \tag{6.11}$$

By substituting (6.1), (6.2), (6.6), and (6.7) to (6.10) and (6.11), the AC components of the inductor currents i_{L1} and i_{L2} can be obtained as

$$i_{L1,AC} = A_{\omega,n}\cos(\omega t + \lambda_{\omega,n}) + A_{2\omega,n}\cos(2\omega t + \lambda_{2\omega,n}) \tag{6.12}$$

$$i_{L2,AC} = -A_{\omega,n}\cos(\omega t + \lambda_{\omega,n}) + A_{2\omega,n}\cos(2\omega t + \lambda_{2\omega,n}) \tag{6.13}$$

where,

$$A_{\omega,n} = \frac{1}{v_{in}}\sqrt{(I_o V_{DC})^2 + \left(\frac{C\omega V_o V_{DC}}{2}\right)^2 + I_o V_{DC}^2 V_o C\omega \sin(\alpha - \delta)}$$

$$A_{2\omega,n} = \frac{V_o}{4v_{in}}\sqrt{I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega \sin(\alpha - \delta)}$$

$$\cos\lambda_{\omega,n} = \frac{I_o V_{DC}\sin\alpha + \left(\frac{C\omega V_o V_{DC}\cos\delta}{2}\right)}{\sqrt{(I_o V_{DC})^2 + \left(\frac{C\omega V_o V_{DC}}{2}\right)^2 + I_o V_{DC}^2 V_o C\omega \sin(\alpha - \delta)}}$$

$$\cos\lambda_{2\omega,n} = \frac{-I_o\cos(\alpha+\delta) + \left(\frac{C\omega V_o \sin(2\delta)}{2}\right)}{\sqrt{I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega \sin(\alpha - \delta)}}.$$

From (6.4), (6.5), (6.12) and (6.13), it is clear that the second-order harmonic current components flow only through the inductors and not through the output capacitors [74].

6.2.2 Second-Order Harmonic Input Current Ripple Reduction Using the Waveform Control Method

In [74], a waveform control method was proposed to reduce the second-order harmonic input current ripple of a boost inverter which was operated at a unity power factor. Operation of the waveform control method was extended for all possible power factor conditions in [76]. In this paper, the analysis of the waveform control method is extended to a grid connected boost inverter where the inverter output power is controlled by modifying the inverter output voltage amplitude and phase angle. Since the boost inverter is a

differential inverter, the output capacitor voltages v_{o1} and v_{o2} can be modified as in (6.14) and (6.15), without affecting the required inverter output voltage.

$$v_{o1} = V_{DC,ref} + \frac{V_o}{2}\sin(\omega t + \delta) + B\sin(2\omega t + \varphi) \tag{6.14}$$

$$v_{o2} = V_{DC,ref} - \frac{V_o}{2}\sin(\omega t + \delta) + B\sin(2\omega t + \varphi) \tag{6.15}$$

where B is the amplitude of the second-order harmonic voltage component and φ is the phase angle of the second-order harmonic voltage component with respect to the grid voltage.

Then, the output capacitor currents can be written as,

$$i_{C1} = C\omega\frac{V_o}{2}\cos(\omega t + \delta) + 2BC\omega\sin(2\omega t + \varphi) \tag{6.16}$$

$$i_{C2} = -C\omega\frac{V_o}{2}\cos(\omega t + \delta) + 2BC\omega\sin(2\omega t + \varphi) \tag{6.17}$$

The total input current with the modified output capacitor voltages can be obtained by using (6.14),(6.15), (6.16), (6.17) and (6.8) as

$$\begin{aligned} i_{in} = \frac{V_o I_o}{2v_{in}}\cos(\alpha - \delta) + \frac{V_o}{2v_{in}}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha - \delta)\right]}\cos(2\omega t - \theta) \\ + \frac{4\omega BCV_{DC}\cos(2\omega t + \varphi)}{v_{in}} + \frac{2\omega B^2 C\sin(4\omega t + 2\varphi)}{v_{in}}. \end{aligned} \tag{6.18}$$

The first term of (6.18) is the DC component of the input current which corresponds to the inverter output power. The second term is the uncompensated second-order harmonic ripple current component of the boost inverter. The second-order harmonic ripple current component due to the second-order harmonic output capacitor voltage reference component is given by the third term of the equation. It can be observed that due to the modification of the output capacitor reference voltages, a fourth-order harmonic ripple component is also present in the input current (the fourth term in (6.18)). By selecting B and φ such that,

$$\frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha - \delta)\right]}\cos(2\omega t - \theta) + 4\omega BCV_{DC}\cos(2\omega t + \varphi) = 0 \tag{6.19}$$

the second-order harmonic ripple component of the input current can be theoretically eliminated. For that, the magnitude of the two terms in (6.19) should be equal and the two terms should have 180^o phase shift. The parameters B and φ which satisfy (6.19) are given by,

$$B = \frac{V_o}{8V_{DC}\omega C}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha - \delta)\right]} \tag{6.20}$$

and

$$\cos(\varphi) = \frac{I_o \cos(\delta+\alpha) - \dfrac{C\omega V_o}{2}\sin(2\delta)}{\sqrt{\left[I_o^2 + \dfrac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega \sin(\alpha-\delta)\right]}}. \tag{6.21}$$

6.2.3 Effect of the Waveform Control Method on the Inductor Current Harmonic Content and Efficiency

With the waveform control method, the current waveforms i_1 and i_2 is given by

$$i_{C1} = I_o \sin(\omega t + \alpha) + C\omega\frac{V_o}{2}\cos(\omega t + \delta) + 2BC\omega \sin(2\omega t + \varphi) \tag{6.22}$$

$$i_{C1} = -I_o \sin(\omega t + \alpha) - C\omega\frac{V_o}{2}\cos(\omega t + \delta) + 2BC\omega \sin(2\omega t + \varphi) \tag{6.23}$$

Then, substituting (6.14), (6.15), (6.22), and (6.23) in to (6.10) and (6.11) and simplifying, the AC components of the inductor currents i_{L1} and i_{L2} can be obtained as,

$$\begin{aligned} i_{L1,AC} = {} & A_{\omega,n}\cos(\omega t + \lambda_{\omega,n}) + A_{\omega,w}\cos(\omega t + \lambda_{\omega,w}) + A_{2\omega,n}\cos(2\omega t + \lambda_{2\omega,n}) \\ & + A_{2\omega,w}\cos(2\omega t + \lambda_{2\omega,w}) + A_{3\omega,w}\cos(3\omega t + \lambda_{3\omega,w}) + A_{4\omega,w}\cos(4\omega t + \lambda_{4\omega,w}) \end{aligned} \tag{6.24}$$

$$\begin{aligned} i_{L2,AC} = {} & -A_{\omega,n}\cos(\omega t + \lambda_{\omega,n}) - A_{\omega,w}\cos(\omega t + \lambda_{\omega,w}) + A_{2\omega,n}\cos(2\omega t + \lambda_{2\omega,n}) \\ & + A_{2\omega,w}\cos(2\omega t + \lambda_{2\omega,w}) - A_{3\omega,w}\cos(3\omega t + \lambda_{3\omega,w}) + A_{4\omega,w}\cos(4\omega t + \lambda_{4\omega,w}) \end{aligned} \tag{6.25}$$

where

$$A_{\omega,w} = \frac{1}{v_{in}}\sqrt{\left(\frac{BI_o}{2}\right)^2 + \left(\frac{BC\omega V_o}{4}\right)^2 - \frac{B^2 V_o I_o C\omega \sin(\alpha-\delta)}{4}}$$

$$A_{2\omega,w} = \frac{2BC\omega V_{DC}}{v_{in}}$$

$$A_{3\omega,w} = \frac{1}{v_{in}}\sqrt{\left(\frac{BI_o}{2}\right)^2 + \left(\frac{3BC\omega V_o}{4}\right)^2 + \frac{3B^2 V_o I_o C\omega \sin(\alpha-\delta)}{4}}$$

$$A_{4\omega,w} = \frac{B^2 C\omega}{v_{in}}$$

$$\cos\lambda_{\omega,w} = \frac{\dfrac{BI_o}{2}\cos(\varphi-\alpha) - \dfrac{BV_o C\omega}{4}\sin(\varphi-\delta)}{\sqrt{\left(\dfrac{BI_o}{2}\right)^2 + \left(\dfrac{BC\omega V_o}{4}\right)^2 - \dfrac{B^2 V_o I_o C\omega \sin(\alpha-\delta)}{4}}}$$

$$\cos\lambda_{2\omega,w} = \cos\varphi$$

$$\cos\lambda_{3\omega,w} = \frac{\dfrac{3BV_o C\omega}{4}\sin(\varphi+\delta) - \dfrac{BI_o}{2}\cos(\alpha+\varphi)}{\sqrt{\left(\dfrac{BI_o}{2}\right)^2 + \left(\dfrac{3BC\omega V_o}{4}\right)^2 + \dfrac{3B^2 V_o I_o C\omega \sin(\alpha-\delta)}{4}}}$$

and

$$\cos \lambda_{4\omega,w} = \cos 2\varphi.$$

Additionally, $A_{\omega,n}$ and $A_{2\omega,n}$ are as defined in (6.12) and (6.13). In (6.24) and (6.25), the subscripts n and w denote the amplitude and phase angle components during the normal operation (without the waveform control) and the operation with the waveform control method respectively. The second-order harmonic components of the inductor currents (6.24) and (6.25) can be re-written as,

$$i_{L1,2,2\omega} = \frac{V_o}{4}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega \sin(\alpha - \delta)\right]} \cos(2\omega t - \theta) + 2\omega BCV_{DC} \cos(2\omega t + \varphi) \tag{6.26}$$

Then, by selecting B and φ as in (6.20) and (6.21), the second-order harmonic components of the inductor currents can be theoretically eliminated and will only flow through the output capacitors as evident from (6.16) and (6.17).

The frequency content of the inductor current without and with the waveform control method can be obtained from (6.12) and (6.24) using the prototype parameters given in Table 6.1. Fig. 6.2 illustrates the calculated AC components of the boost inverter inductor current using (6.12) and (6.24) when the boost inverter supplies 10W active power and 15VAr reactive power to the grid. With the waveform control, the fundamental frequency component shows a slight reduction, the second-order harmonic component is completely eliminated and the third-order and the fourth-order harmonic components are negligible. Since with the waveform control the second-order harmonic current is eliminated from the inductor and allocated to the output capacitor, the power loss in the inductor is reduced which in turn increases the converter efficiency as presented in [74, 102].

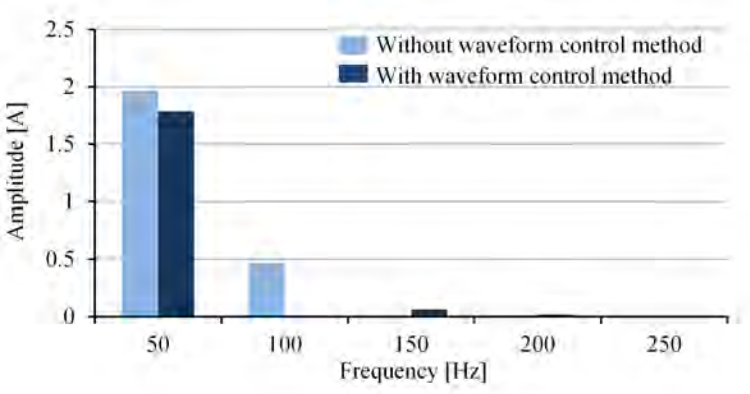

Fig. 6.2: AC components of the inductor current i_{L1}, without and with the waveform control method when delivering 10W active power and 15 VAr reactive power to the grid.

6.2.4 Selection of the Output Capacitor Capacitance C

From the analysis shown in Subsection 6.2.3 it is obvious that due to the waveform control method, the output capacitors of the boost inverter have to supply the second-order harmonic power variation as opposed to the normal boost inverter operation in which the second-order harmonic power variation is supplied by the input power source. In the following paragraphs this effect is analyzed and it is shown how it affects selection of the required output capacitor capacitance as compared with the selection of the capacitance for the normal operation.

During operation with the waveform control the maximum value of B, B_{max}, can be found from (6.20) for the maximum output current $I_{o,max}$ as,

$$B_{max} = \frac{V_o}{8V_{DC}\omega C}\sqrt{\left[(I_{o,max})^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_{o,max}C\omega\right]} \tag{6.27}$$

Then, the maximum and minimum values of the output capacitor voltages are,

$$V_{o1,max} = V_{DC} + \frac{V_o}{2} + B_{max} \tag{6.28}$$

$$V_{o1,min} = V_{DC} - \frac{V_o}{2} - B_{max} \tag{6.29}$$

In addition, V_{DC} has to satisfy the inequality

$$V_{DC} > v_{in} + \frac{V_o}{2} + B_{max} \tag{6.30}$$

From (6.28) it is clear that the higher the V_{DC} the higher the amplitude of the maximum output capacitor reference voltage $V_{o1,max}$. Since a low value of V_{DC} is preferred to reduce the gain of the boost inverter, a minimum possible value of V_{DC} , $V_{DC,min}$, which satisfies (6.30) can be obtained from (6.27) and (6.30) as,

$$V_{DC,min} = \frac{1}{2}\left[v_{in} + \frac{V_o}{2} + \sqrt{\left(v_{in} + \frac{V_o}{2}\right)^2 + \left(\frac{V_o}{2\omega C}\sqrt{\left[(I_{o,max})^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_{o,max}C\omega\right]}\right)}\right] \tag{6.31}$$

Substituting $V_{DC} = V_{DC,min}$ in (6.28), the maximum value of the output capacitor voltages, $V_{o1.max}$ is,

$$V_{o1,max} = V_{DC,min} + \frac{V_o}{2} + B_{max} \tag{6.32}$$

The relationship of $V_{DC,min}$, B_{max}, and $V_{o1,max}$ versus the output capacitance value C for $I_{o,max}$=1.5A is shown in Fig. 6.3. From Fig. 6.3, it can be observed that higher C leads to lower B_{max}, $V_{DC,min}$, and $V_{o1,max}$. Hence, the required output capacitor capacitance value $C_{req,w}$ can be found as follows. First, the maximum allowable output capacitor voltage $V_{o1,max}$ is predetermined from the input voltage v_{in} and the maximum gain of

the converter legs G_{max}, as $V_{o1,max} = v_{in} \times G_{max}$. Next, using (6.27), (6.31), and (6.32), values of B_{max}, $V_{DC,min}$, and $V_{o1,max}$ are plotted against a range of the output capacitor C values. Then, for the predetermined $V_{o1,max}$ value both the required output capacitor capacitance value $C_{req,w}$ and the required output capacitor reference voltage minimum DC shift $V_{DC,min}$ can be obtained graphically as illustrated in Fig. 6.3.

When considering the normal operation (without the waveform control method) the DC shift voltage V_{DC} has to satisfy the inequality

$$V_{DC} > v_{in} + \frac{V_o}{2} \tag{6.33}$$

Hence, the minimum possible DC shift, $V_{DC,min}$ is

$$V_{DC,min} = v_{in} + \frac{V_o}{2} \tag{6.34}$$

and the maximum output capacitor voltage, $V_{o1,max}$ is

$$V_{o1,max} = V_{DC} + \frac{V_o}{2} \tag{6.35}$$

Form (6.34) and (6.35), it is clear that $V_{DC,min}$ and $V_{o1,max}$ are independent of the output capacitor value C. Therefore, during the normal boost inverter operation, the required output capacitor value $C_{req,n}$ can be found from a selected maximum switching frequency voltage ripple in the output capacitor voltage waveform $\Delta V_{o1,max}$ which is given by

$$\Delta V_{o1,max} = \frac{I_{o,max} d_{1,max}}{f_{sw} C_{req,n}} \tag{6.36}$$

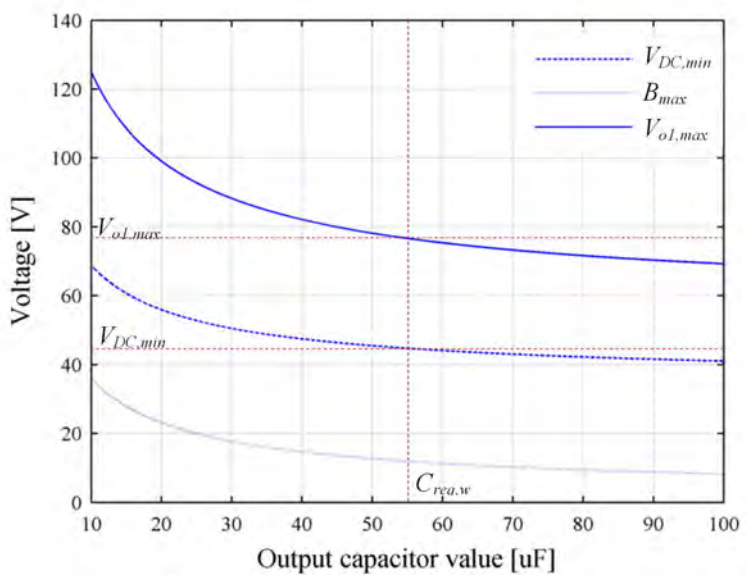

Fig. 6.3: Relationships between B_{max}, $v_{o1,max}$ and $V_{DC,min}$ versus the output capacitor C values during operation with the waveform control.

where

$$d_{1,max} = \frac{V_{o1,max} - v_{in}}{V_{o1,max}} \tag{6.37}$$

assuming a lossless conversion. From (6.36) and (6.37), the required output capacitor value $C_{req,n}$ during the normal operation is

$$C_{req,n} = \frac{I_{o,max}}{f_{sw}\Delta V_{o1,max}} \frac{V_{o1,max} - v_{in}}{V_{o1,max}}. \tag{6.38}$$

The following example illustrates selection of the required output capacitor values $C_{req,n}$ and $C_{req,w}$ for the normal operation and operation with the waveform control, respectively.

Consider a boost inverter with the input voltage v_{in}, the output voltage peak value V_o and the maximum peak output current $I_{o,max}$ equal to 12.8V, 40V, and 1.5A, respectively. Assume the switching frequency of the converter is 20kHz and the maximum gain of the boost converter leg G_{max} is 6. Then, according to (6.35) the maximum output capacitor voltage $V_{o1,max}$ for the normal operation is 52.8V which corresponds to the converter leg gain G equal to 4.125. If the required output capacitor switching frequency ripple $\Delta V_{o1,max}$ is less than 5% of the peak output voltage then the required output capacitor value $C_{req,n}$ for the normal operation can be calculated from (6.38) as 28.4 μF.

If the value of $C_{req,n}$ found for the normal operation is used with the waveform control method, then the required peak output capacitor voltage $V_{o1,max}$ can be obtained from Fig. 6.3 as 89.56V. However, to achieve this voltage, the converter leg gain G has to be equal to 7. Since this gain exceeds the maximum possible gain G_{max}, the $C_{req,n}$ value cannot be used with the waveform control method and the $C_{req,w}$ value has to be found as follows. Considering the maximum gain of the boost converter leg G_{max}=6, the maximum possible output capacitor voltage $V_{o1,max}$ is 76.8V. Then, the required output capacitor value $C_{req,w}$ to maintain the output capacitor peak voltage less than 76.8V can be obtained from Fig. 6.3 as $C_{req,w}$ = 54.6 μF. The nearest commercially available value of 60μF is then selected in the actual setup.

6.2.5 Effect of the Capacitor Tolerances and the Boost Inductor ESR Values on the Waveform Control Method Performance

In the waveform control method, (6.20) and (6.21) are used to calculate the required second-order harmonic output capacitor voltage reference signal to reduce the second-order harmonic input ripple current. However, in the derivation of (6.20) and (6.21), the ESR values of the boost inverter inductors are neglected for simplicity. Moreover, since the second-order harmonic voltage reference amplitude B and phase angle φ are functions of the capacitance of the output capacitor, the effect of the output capacitor tolerances on

the ripple reduction using the waveform control method has to be investigated. In order to analyze the effect of the ESR values of the inductors and the capacitor tolerances on the total input current the inductor currents of the boost inverter can be written as,

$$i_{L1} = \frac{i_1 v_{o1}}{v_{in} - i_{L1} R_{L1}}, i_{L2} = \frac{i_2 v_{o2}}{v_{in} - i_{L2} R_{L2}} \tag{6.39}$$

Then, the total input current can be obtained from

$$i_{in} = \frac{v_{in} - \sqrt{\left(v_{in}^2 - 4 R_L v_{o1} i_1\right)}}{2R_L} + \frac{v_{in} - \sqrt{\left(v_{in}^2 - 4 R_L v_{o2} i_2\right)}}{2R_L} \tag{6.40}$$

where $R_L = R_{L1} = R_{L2}$. Please refer Appendix A.1 for the derivation.

The effect of the ESR values of the inductors and tolerance of the capacitors on the total input current can be observed by simulating (6.40). Inverter parameters equal to the prototype parameters summarized in Table 6.1 are used in the analysis. First, the second-order harmonic output capacitor voltage reference parameters are calculated from (6.20) and (6.21) using C=60μF. Then, (6.40) is simulated for various ESR values and considering a $\pm$10% change in C. A ripple reduction factor is defined as the ratio between the ripple current amplitude without and with the waveform control method. Fig. 6.4 shows the ripple current reduction factor for various values of the inductor internal resistance and $\pm$10% change in the capacitance of the output capacitors when the inverter supplies 10W active power and 15VAr reactive power. Theoretically, a perfect ripple cancellation should result in an infinite ripple reduction factor. However, as it can be observed from Fig. 6.4, the capacitor tolerances and the inductor ESR values cause a significant performance degradation in the waveform control method because it is based on direct calculation of the second-order harmonic reference voltage parameters. Hence, a control method which is able to generate the required second-order harmonic voltage reference signal parameters without calculating them from (6.20) and (6.21) can avoid the problem.

6.3 The Proposed Rule Based Controller for Ripple Current Mitigation

A rule-based controller is proposed to mitigate the second-order harmonic input ripple current component by adjusting the output capacitor second-order harmonic voltage reference amplitude B and phase angle φ. The main advantage of the proposed controller is that it can reduce the second-order harmonic ripple current in all four output power quadrants without being affected by the capacitor tolerances and the ESR values of the inductors.

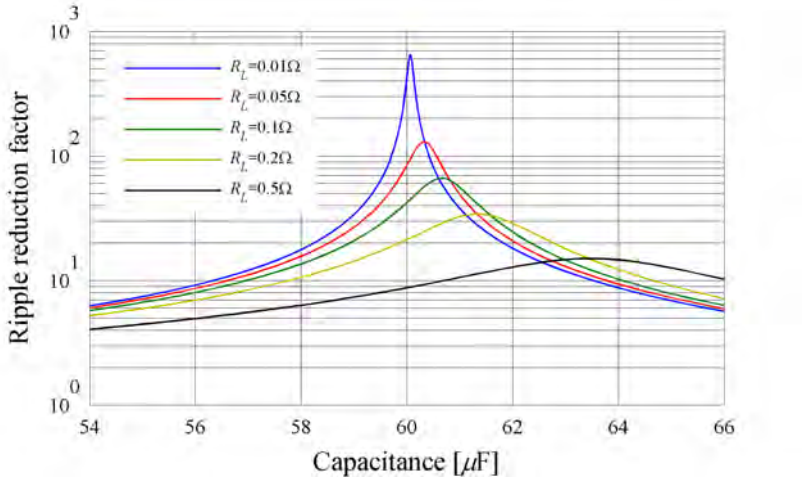

Fig. 6.4: Ripple reduction factor for various values of the inductor ESR values R_L and capacitance C of the output capacitors when the waveform control method is used (inverter supplies 10W active power and 15VAr reactive power).

Variation of the second-order harmonic ripple current amplitude as a function of B and φ is analyzed for all four operating power quadrants to verify that it contains a global minimum. The results in Fig. 6.5 illustrate that the function contains only a global minimum which corresponds to the B and φ values given by (6.20) and (6.21), respectively.

The proposed rule-based controller incorporates a perturb and observe (P&O) approach [103,104] to adjust the B and φ values. The flow chart of the proposed controller is shown in Fig. 6.6. Initially, both B and φ values are set to zero and the second-order harmonic ripple current amplitude A is measured as presented later in the section. The controller operates in two phases. In the first phase, the value of B is either increased or decreased to reduce the ripple current component and in the second phase, the value of φ is either increased or decreased to reduce the ripple current component. The transition between the phases occurs when a significant increment (ϵ) or decrement (-ϵ) of the ripple current amplitude cannot be obtained by increasing or decreasing either the value of B or φ (see Fig. 6.6).

Variable step size perturbations are used in the proposed controller algorithm in order to avoid design issues related to the fixed step size perturbations [103]. The variable step size perturbation method used for B is given by,

$$B_k = B_{k-1} + N_B A_{k-1} \tag{6.41}$$

where N_B is a scalar which is tuned at the design time of the controller and A is the measured second-order harmonic input current amplitude. Larger N_B results in faster dynamics with increased transition oscillations while smaller N_B results in slower dynamics with smaller transition oscillations. Since the controller incorporates a P&O method, an

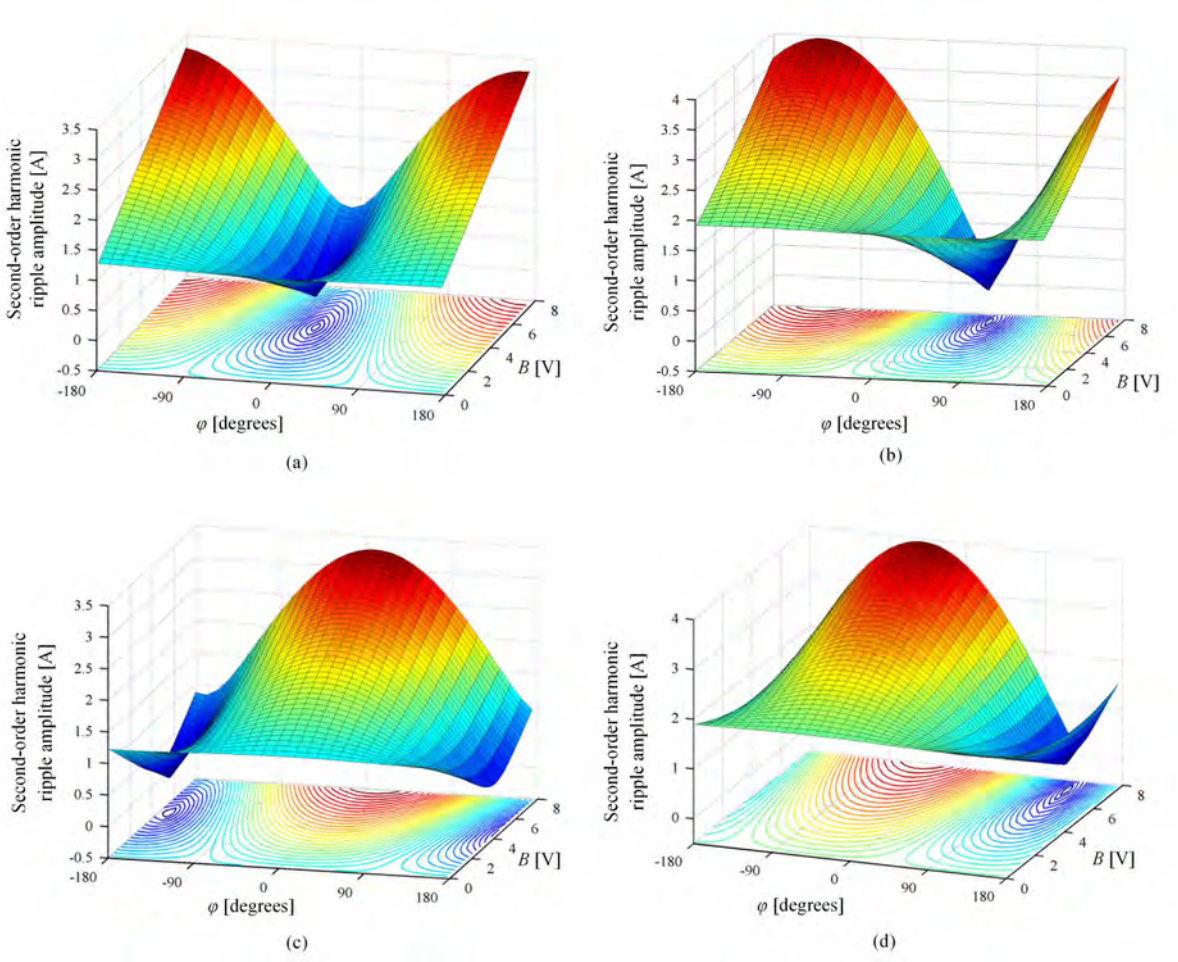

Fig. 6.5: Second-order harmonic ripple current amplitude as a function of B and φ when (a) inverter supplies 15W active power and 10VAr reactive power,(b) inverter supplies 15W active power and absorbs 10VAr reactive power, (c) inverter absorbs 15W active power and supplies 10VAr reactive power and (d) inverter absorbs 15W active power and 10VAr reactive power

increment of the second-order harmonic ripple current amplitude may occur due to the initial perturbation of B. N_B can be used to limit the initial ripple current amplitude change ΔA_{init} to a maximum allowable limit $\Delta A_{init,max}$. From (6.18), the maximum possible change of the second-order harmonic ripple current amplitude ΔA_{max} due to a step change in B can be written as,

$$\Delta A_{max} = \frac{4C\omega V_{DC}\Delta B_{max}}{v_{in}} \tag{6.42}$$

where ΔB_{max} is the maximum possible step change in B.

Hence, using (6.41) and (6.42), the value of N_B can be calculated to limit the initial step change of the ripple current amplitude ΔA_{init} due to the initial perturbation of B as,

$$N_B = \left(\frac{v_{in}}{4\omega C V_{DC}}\right)\frac{\Delta A_{init,max}}{A_{max}} \tag{6.43}$$

where $\Delta A_{init,max}$ is the maximum allowable initial step change of the ripple current

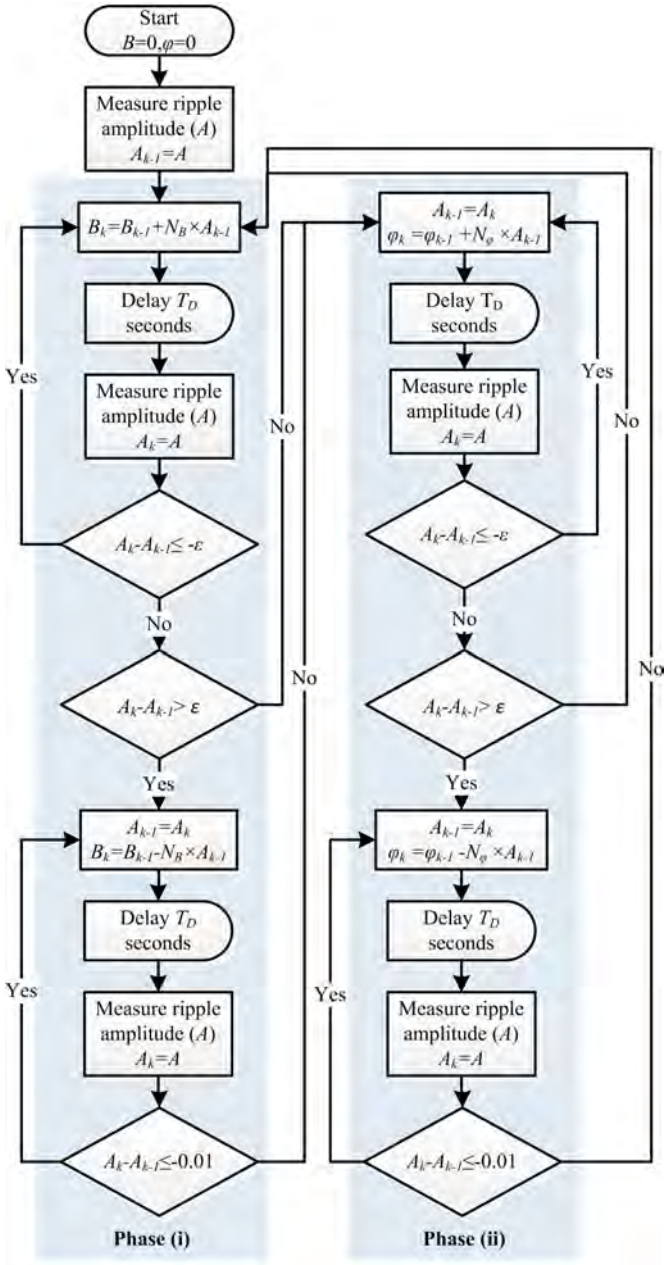

Fig. 6.6: Flow diagram of the proposed rule-based controller for the second-order harmonic ripple current reduction

amplitude and A_{max} is the maximum possible uncompensated second-order harmonic ripple current amplitude which is given by,

$$A_{max} = \frac{V_o}{2v_{in}}\sqrt{\left[(I_{o,max})^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_{o,max}C\omega\right]} \tag{6.44}$$

The variable step size perturbation method used for φ is given by,

$$\varphi_k = \varphi_{k-1} + N_\varphi A_{k-1} \tag{6.45}$$

where N_φ is a scalar which is calculated for a maximum allowable phase-angle step change

$\Delta\varphi_{max}$, by,

$$N_{\varphi} = \frac{\Delta\varphi_{max}}{A_{max}} \tag{6.46}$$

There has to be a specific time delay T_D between each perturbation and the ripple amplitude measurement instant. The value of the required time delay T_D depends on the converter response time to a step change in the voltage reference and the time required to measure the second-order harmonic ripple amplitude accurately. The faster the measurement of the second-order harmonic ripple current amplitude, the faster the dynamic performance of the controller. Hence, a Fast Fourier transformation (FFT) based amplitude measurement technique [105] is employed to ensure fast and accurate measurement. Fig. 6.7 shows the block diagram of the second-order harmonic ripple current amplitude measurement system. From (6.18), the total input current of the boost inverter with modified output capacitor reference signals consists of a DC component, a second-order harmonic component, and a fourth-order harmonic component. The total boost inverter input current in (6.18) can be re-written as,

$$i_{in} = I_{in,DC} + I_{in,2\omega}\cos(2\omega t + \gamma_{2\omega}) + I_{in,4\omega}\cos(4\omega t + \gamma_{4\omega}) \tag{6.47}$$

The following equations can be obtained after multiplying (6.47) with the reference signals, $\cos(2\omega t)$ and $\sin(2\omega t)$.

$$\begin{aligned} i_{in}\cos(2\omega t) = I_{in,DC}\cos(2\omega t) + I_{in,2\omega}\left[\frac{\cos(\gamma_{2\omega}) + \cos(4\omega t + \gamma_{2\omega})}{2}\right] \\ + I_{in,4\omega}\left[\frac{\cos(2\omega t + \gamma_{4\omega}) + \cos(6\omega t + \gamma_{4\omega})}{2}\right] \end{aligned} \tag{6.48}$$

$$\begin{aligned} i_{in}\sin(2\omega t) = I_{in,DC}\sin(2\omega t) + I_{in,2\omega}\left[\frac{\sin(\gamma_{2\omega}) + \sin(4\omega t + \gamma_{2\omega})}{2}\right] \\ + I_{in,4\omega}\left[\frac{\sin(2\omega t + \gamma_{4\omega}) + \sin(6\omega t + \gamma_{4\omega})}{2}\right] \end{aligned} \tag{6.49}$$

By averaging (6.48) and(6.49) over a period of the second-order harmonic waveform (T_{avg}),

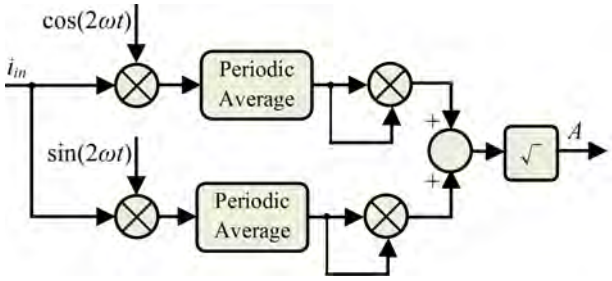

Fig. 6.7: Second order harmonic ripple current amplitude measurement technique

the following equations can be obtained.

$$\begin{aligned} i_{in}\cos(2\omega t)_{avg} &= \frac{1}{T_{avg}}\int_0^{T_{avg}} i_{in}\cos(2\omega t)dt \\ &= \frac{I_{in,2\omega}\cos(\gamma_{2\omega})}{2} \end{aligned} \tag{6.50}$$

$$\begin{aligned} i_{in}\sin(2\omega t)_{avg} &= \frac{1}{T_{avg}}\int_0^{T_{avg}} i_{in}\sin(2\omega t)dt \\ &= \frac{I_{in,2\omega}\sin(\gamma_{2\omega})}{2} \end{aligned} \tag{6.51}$$

Then, the second-order harmonic ripple current amplitude can be obtained as,

$$A = 2\sqrt{(i_{in}\cos(2\omega t)_{avg})^2 + (i_{in}\sin(2\omega t)_{avg})^2} \tag{6.52}$$

The method requires T_{avg} time to accurately measure the ripple current amplitude. Hence, for the proper operation of the rule-based controller, the delay time between the perturbations and the measurements T_D has to be selected such that,

$$T_D \geq T_{avg} \tag{6.53}$$

To avoid possible steady state oscillations, the controller should be disabled after a pre-determined number of iterations. The number of iterations can be determined based on the required ripple reduction performance, and in the experiments, the controller was disabled after four iterations.

6.4 Boost Inverter Control System

The overall block diagram of the grid-connected boost inverter with the proposed rule-based controller is shown in Fig. 6.8. The parameters of the experimental prototype are summarized in Table 6.1.

Two DL controllers are implemented to control the output capacitor voltages v_{o1} and v_{o2} as given by (6.14) and (6.15) respectively. Each DL controller has an inner current control loop and an outer voltage control loop. The block diagram of the DL controller for the left hand side boost converter leg is shown in Fig. 6.9. A proportional resonant (PR) controller with two resonant components which are tuned to 50 Hz and 100Hz is employed in the voltage control loop to achieve better sinusoidal reference following [106]. The transfer function of the PR controller is given by,

$$H_{PR}(s) = K_p + \frac{2K_{i1}\omega_{c1}s}{s^2 + 2\omega_{c1}s + \omega_1^2} + \frac{2K_{i2}\omega_{c2}s}{s^2 + 2\omega_{c2}s + \omega_2^2} \tag{6.54}$$

where K_p, K_{i1}, and K_{i2}, are gains of the PR controller. The bandwidth of the resonant components can be adjusted using ω_{c1} and ω_{c2}. The parameters ω_1 and ω_2 are selected

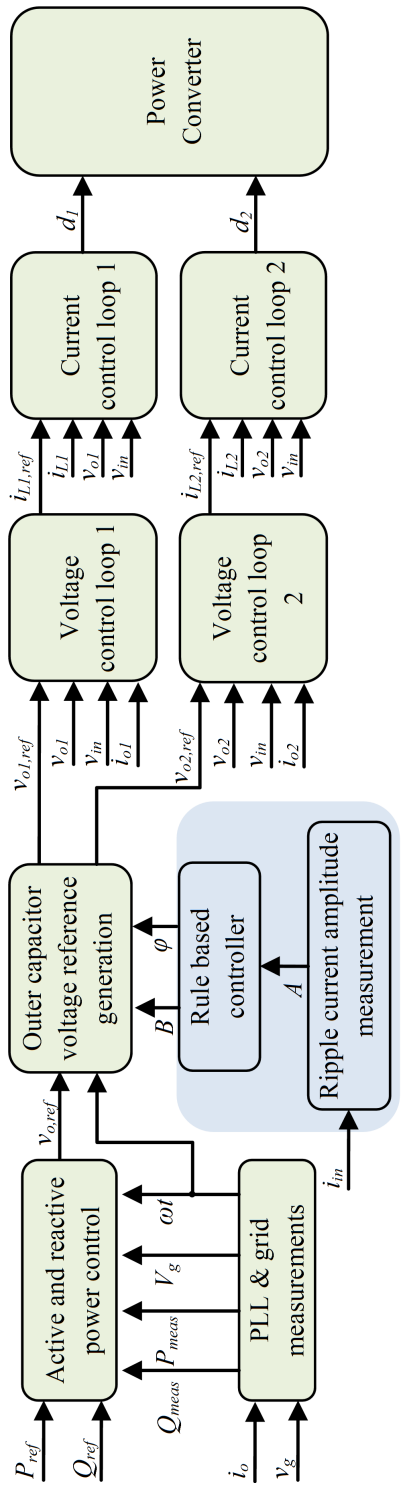

Fig. 6.8: Overall block diagram of the proposed control system

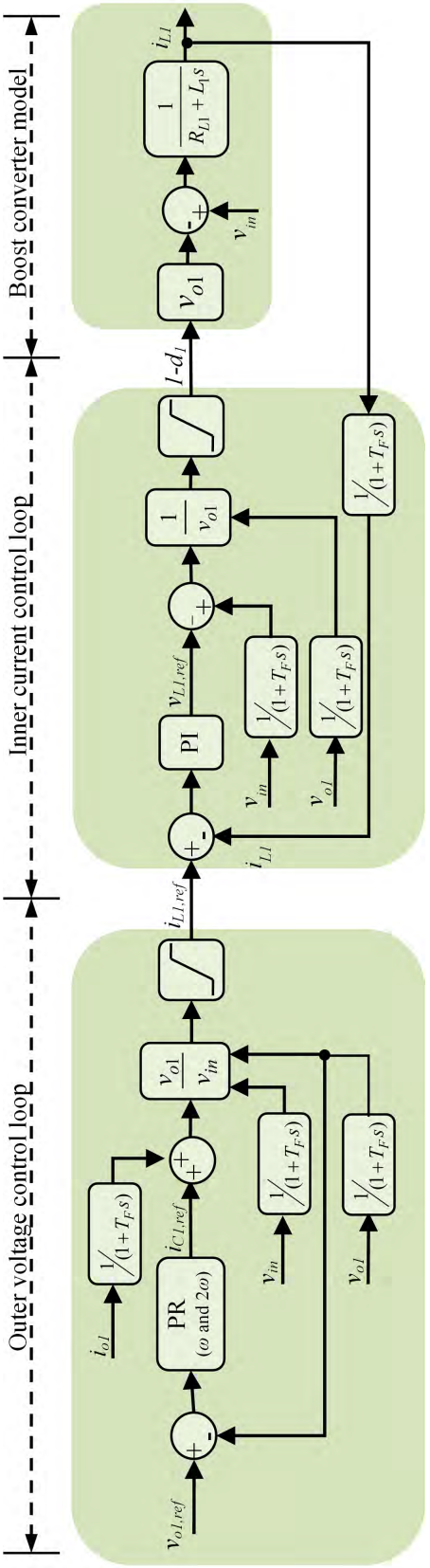

Fig. 6.9: Outer voltage control loop and inner current control loop for the left hand side boost converter leg.

Table 6.1: Experimental prototype parameters

Parameter	**Value**	**Parameter**	**Value**
Power converter parameters			
V_o	40 V	f	50 Hz
C_1, C_2	60 μF	L_1,L_2	210 μH
$I_{o,max}$	1.5 A	T_F	0.001
V_{DC}	42 V	f_{sw}	20 kHz
R_{L1}, R_{L2}	0.24 Ω		
Grid parameters			
V_g	40 V	L_g	20 mH
Voltage control loop parameters			
$K_{p,PR}$	0.1	$K_{i1,PR}$	4
$K_{i2,PR}$	6	ω_{c1}, ω_{c2}	0.5
Current control loop parameters			
$K_{p,PI}$	2.615	$K_{i,PI}$	8.44×10^{-5}
Rule based controlletr parameters			
N_B	1.1	N_φ	0.25
T_{avg}	0.01 s	T_D	0.03 s
ϵ	0.01		

as 314.2 rads^{-1} and 628.3 rads^{-1} respectively. The PI controller based inner current control loops are designed for each boost converter leg using the average continuous time model of the boost converter. The PR controllers for the outer voltage control loops are designed with 400Hz bandwidth and the PI controllers for the inner current control loops are designed with 4kHz bandwidth [55].

The maximum possible uncompensated second-order harmonic input current amplitude A_{max} can be calculated using (6.44). The scalar N_B for the rule-based controller is calculated such that the maximum initial step change of the second-order harmonic ripple component is 25% of the maximum possible uncompensated second-order harmonic input current amplitude A_{max}. The scalar N_φ for the rule-based controller is selected such that maximum possible step change of the phase angle φ is 0.75rads^{-1}. A large value for ϵ can reduce the ripple reduction performance of the controller while a very small ϵ can lead to slower dynamics. Hence ϵ was selected as 0.01 to achieve better ripple reduction with faster dynamics. All controller parameters for the experimental prototype are summarized in Table 6.1.

6.5 Experimental Results

The proposed rule-based controller for the single-phase grid-connected boost inverter was verified using an experimental prototype. A 6.4 Ah, 12.8 V $LiFePO_4$ battery from K2 Energy was used as the input power source. Fig. 6.10 shows the operation of the grid-connected boost inverter without and with the proposed ripple current reduction method. The inverter is controlled to deliver 10W active power and 15VAr reactive power to the grid. Figs. 6.10(a) and 6.10(b) show the waveforms of the output capacitor voltages and the inverter output voltage, without and with the rule-based control respectively. As expected, the output voltage waveform is the same despite the difference in the output capacitor voltage waveforms. Figs. 6.10(c) and 6.10(d) depict the inverter output voltage, grid voltage and the output current waveforms. Both the active and reactive power supplied to the grid are controlled by changing the amplitude and phase angle of the inverter output voltage with respect to the grid voltage. The inductor current waveforms and the total input current waveforms of the boost inverter without and with the rule-base control are shown in the Figs. 6.10(e) and 6.10(f), respectively. Significant reduction in the DC-side current ripple component can be observed after applying the rule-based controller compared to the conventional operation of the boost inverter.

The frequency spectrum characteristics of the boost inverter input current are shown in Figs. 6.10(g) and 6.10(h) for both cases. The second-order harmonic component amplitude with conventional operation is 1.174A while the second-order harmonic current component amplitude with the rule-based controller is reduced to 0.156A achieving close to 7.5 times reduction in the second order harmonic ripple current amplitude. The fourth-order harmonic current component with the proposed controller is 32mA while it is 11mA with the conventional operation. The increment in the fourth-order harmonic current component is as expected due to modification in the output capacitor reference voltages. However, the effect of the increment in the fourth-order harmonic current component is negligible compared to the reduction in the second order harmonic input current component.

Dynamic performance of the rule-based controller is shown in Fig. 6.11. The controller is enabled at the time 1s. First the value of B is adjusted to reduce the second-order harmonic ripple current amplitude followed by a phase angle φ adjustment. After several iterations, significant ripple current reduction is achieved. To avoid steady-state oscillations, the controller is disabled after four cycles.

Performance of the proposed controller for a step change in the output active and reactive power is shown in Fig. 6.12. The rule-based controller is reactivated each time a

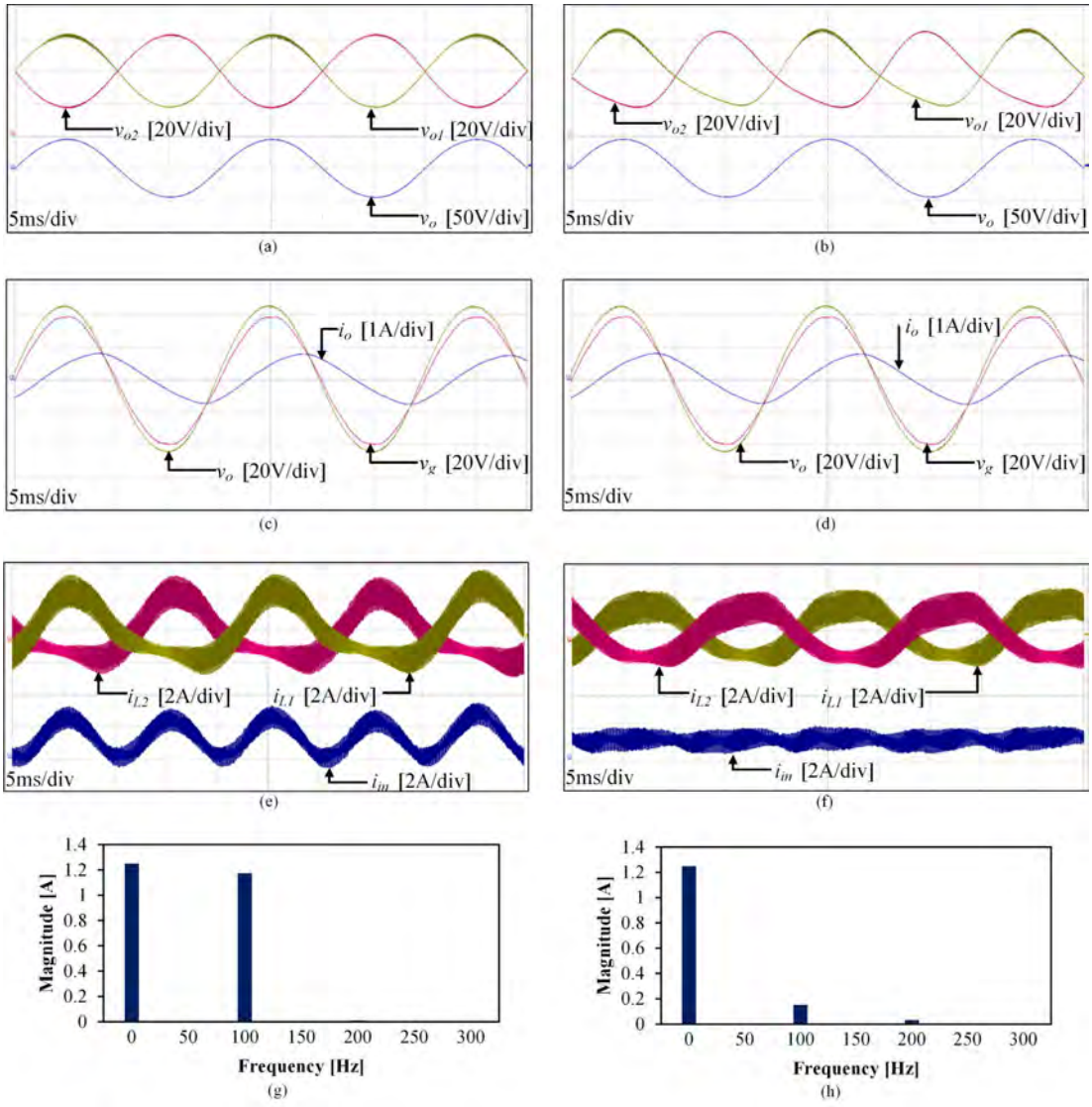

Fig. 6.10: Experimental results illustrating operation of the battery storage system when delivering 15VAr reactive power and 10W active power. (a) Output capacitor voltage waveforms and inverter output voltage without the rule-based controller, (b) Output capacitor voltage waveforms and inverter output voltage with the rule-based controller, (c) Inverter output voltage, grid voltage and inverter output current without the rule-based controller, (d) Inverter output voltage, grid voltage and inverter output current with the rule-based controller, (e) Inductor currents and total input current of the boost inverter without the rule-based controller, (f) Inductor currents and total input current of the boost inverter with the rule-based controller, (g) Frequency characteristics of the input current without the rule-based controller and (h) Frequency characteristics of the input current with the rule-based controller.

change in the reference active or reactive power P_{ref}, Q_{ref} occurs. Since it takes about 2 seconds to perform the P&O process this time interval limits how frequently the change in the reference active or reactive power can occur. Hence, the method is not suitable for PV power applications.

To emulate the effect of the capacitor tolerances on the input current ripple reduction,

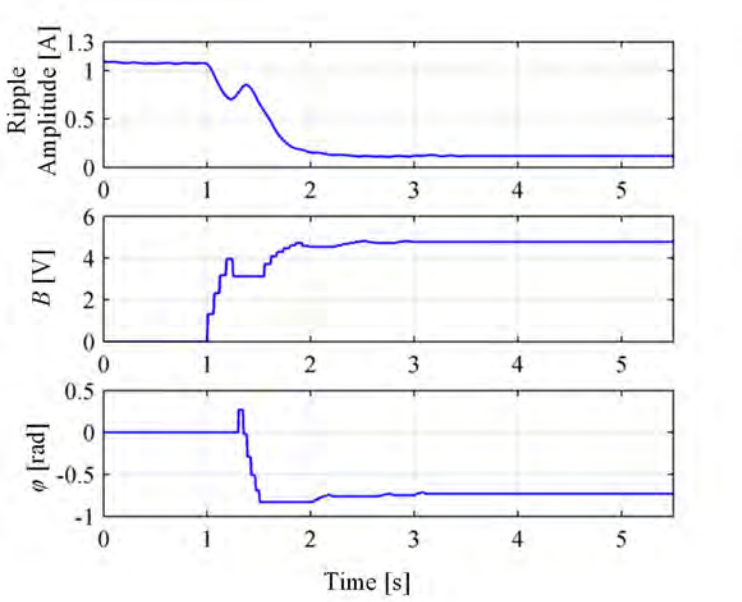

Fig. 6.11: Experimental results illustrating operation of the proposed rule-based controller when the battery storage system supplies 10W active power and 15 VAr reactive power

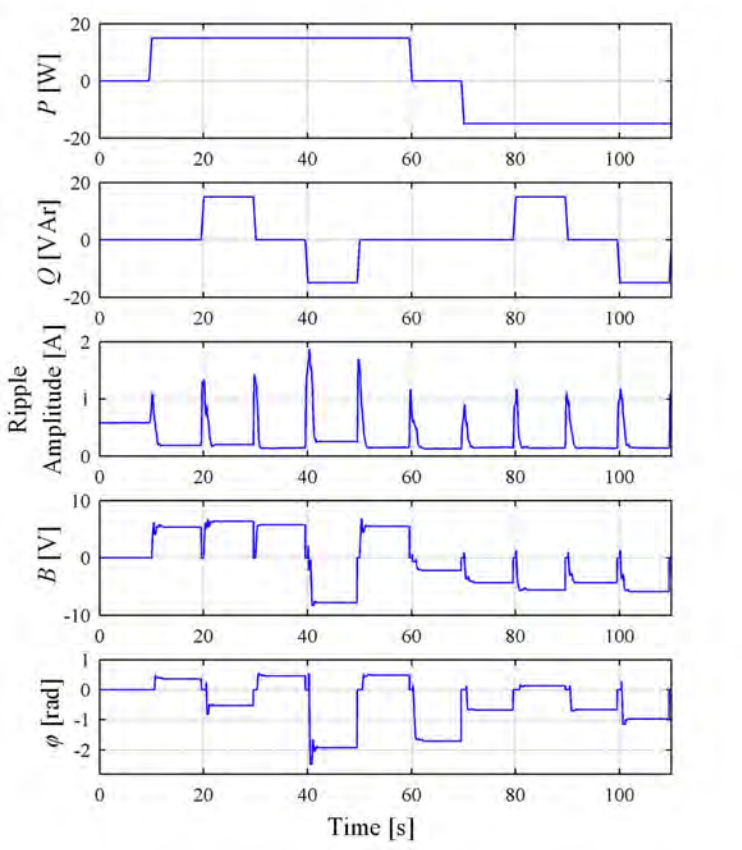

Fig. 6.12: Operation of the rule-based controller with step-changing inverter output power

the capacitance value ($C = C_1 = C_2$) used for the second-order harmonic voltage reference parameter calculation was changed by $\pm 10\%$ from the nominal capacitor value 60μF.

Fig. 6.13 illustrates the effect of the change in the capacitance value on the second-order harmonic ripple current reduction when the waveform control method is used. For the considered output power operating point (10W active power and 15VAr reactive power), a -10% change in capacitance does not leads to a significant change in the ripple reduction. However, a +10% change in the capacitance value results in considerable reduction in the waveform controller performance.

Since the boost inverter second-order harmonic input current amplitude and phase angle vary with the inverter output power, the operation of the proposed controller was tested in all possible output power operating quadrants. The boost inverter input current ripple reductions obtained using the waveform control method and the proposed rule-based control method are compared for all possible output power conditions in Fig. 6.14 and

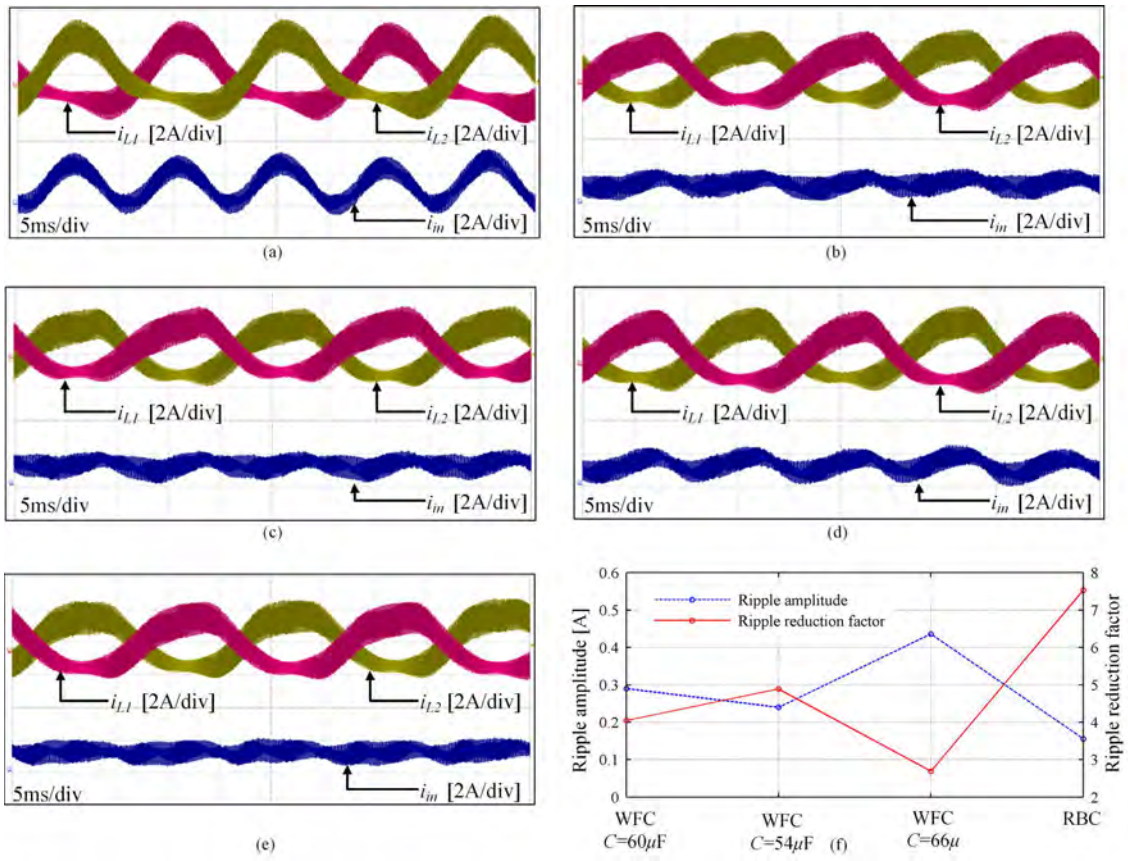

Fig. 6.13: Experimental results illustrating the effect of capacitor tolerances on the ripple current reduction when the waveform control method is used (a) Inductor currents and total input current of the boost inverter without any ripple current reduction method, (b) Inductor currents and total input current of the boost inverter with the waveform control (WFC) method and C=60μF, (c) Inductor currents and total input current of the boost inverter with the waveform control method and C=54μF, (d) Inductor currents and total input current of the boost inverter with the waveform control method and C=66μF, (e) Inductor currents and total input current of the boost inverter with the rule-based controller (RBC), (f) Comparison of the ripple amplitude and ripple reduction factor for cases (b) to (e).

summarized in Table 6.2. It can be observed that the proposed rule-based controller is able to reduce the ripple current at least six times in all conditions while the waveform control method fails to achieve significant ripple current reduction at some of the output power conditions. Percentage improvement in the ripple reduction R_{imp} when using the rule-based controller as compared with the waveform control method is also illustrated in Fig. 6.14.

$$R_{imp} = \frac{R_{RBC} - R_{WFC}}{R_{WFC}} \times 100\% \tag{6.55}$$

where, R_{RBC} and R_{WFC} are the ripple reduction factors obtained from the rule-based control method and the waveform control method respectively.

6.6 Conclusions

Due to the single phase operation of the boost inverter based battery-supercapacitor HESS, a second order harmonic ripple component exists at the DC side of the converter and the ripple component was allocated to the supercapacitor as a way of increasing the battery lifetime. However, such ripple current component increases the internal heating and losses in the supercapacitor and degrades its lifetime. Hence, it is vital to identify a suitable second-order harmonic ripple current reduction method for the boost inverter based battery-supercapacitor HESS. In order to identify a ripple reduction method, the operation of a single boost inverter based ESS was considered in this chapter.

First, the existing waveform control ripple current reduction method was extended to the grid connected boost inverter operation and the effects of the capacitor tolerances

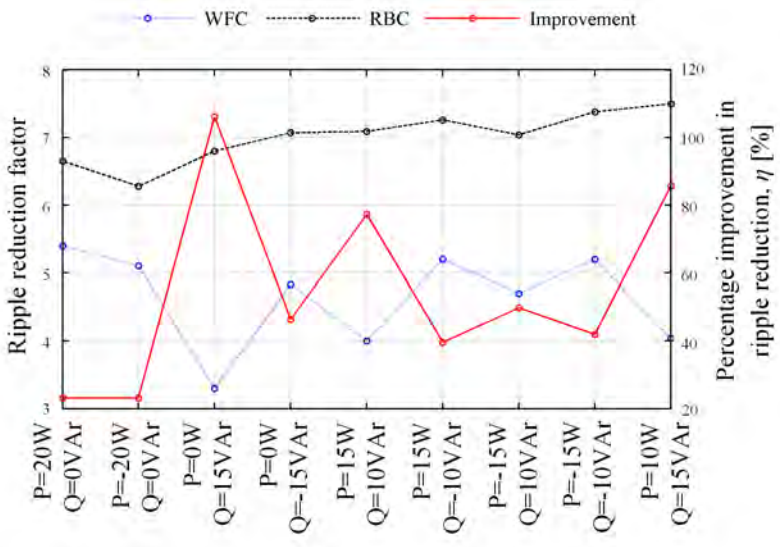

Fig. 6.14: Comparison of the ripple current reduction using the waveform control method (WFC) and the rule-based controller (RBC)

Table 6.2: Second-order harmonic ripple current mitigation for various output power conditions

Active power [W]	Reactive power [VAr]	Ripple amplitude without any compensation method [A]	Ripple amplitude reduction factor with RBC method	Ripple amplitude reduction factor with WFC method
20	0	1.954	6.65	5.40
-20	0	1.067	6.28	5.10
0	15	0.605	6.80	3.30
0	-15	1.343	7.07	4.80
15	10	1.454	7.09	4.00
15	-10	1.843	7.26	5.20
-15	10	0.936	7.04	4.70
-15	-10	1.114	7.38	5.90
10	15	1.174	7.50	4.04

and ESR of the inductors on its effectiveness were analyzed. It was illustrated that the capacitance tolerance and the inductor ESR values affect the performance of the waveform control method due to the direct calculation of the compensation signals. Then, a rule-based controller was proposed to mitigate the second-order harmonic ripple current in the boost inverter. The main advantage of the proposed controller was that it could reduce the second-order harmonic ripple current in all four output power quadrants without being affected by the capacitor tolerances and ESR values of the inductors. The proposed rule-based controller was validated experimentally and confirmed that the controller can achieve better ripple current reduction as compared to the waveform control approach without its performance being affected by the capacitor tolerances and the ESR values.

Chapter 7

An Input Current Feedback Method to Mitigate the DC-Side Low Frequency Ripple Current in a Single-Phase Boost Inverter

Due to the single phase operation of the boost inverter topology, a second-order harmonic ripple component can be observed at the DC side of the boost inverter based energy storage systems (ESSs). A novel current feedback ripple reduction method proposed in [68] is presented in this chapter. The proposed method modifies the boost inverter output capacitor reference voltages using an input current feedback signal. Compared to the existing waveform control ripple current reduction method, the performance of the proposed current feedback ripple reduction method does not get affected by the output capacitor tolerances and equivalent series resistance (ESR) of the boost inductors. Furthermore, compared to the rule-based control method presented in Chapter 6, the current feedback method demonstrates a superior ripple current reduction and dynamic performance in all output power quadrants and hence it is most suitable for the boost inverter based energy storage system. The performance of the proposed current feedback ripple reduction method is verified experimentally.

Later in the chapter, the proposed current feedback ripple reduction method is applied to the interleaved boost inverter based battery-supercapacitor HESS and its effectiveness in mitigating the second-order harmonic ripple component in the supercapacitor current is demonstrated [69]. The proposed HESS is the only single phase battery-supercapacitor HESS presented in literature which is able to mitigate the second-order harmonic ripple component in the supercapacitor current as well as able to reduce the switching frequency

ripple component in both the battery and the supercapacitor currents while allocating the fast power fluctuations to the supercapacitor.

7.1 Introduction

A boost inverter based battery-supercapacitor HESS was presented in Chapter 3 to Chapter 5. In all the HESS power allocation methods, the second order harmonic current component present at the DC side of the converter due to the single phase grid integration was allocated to the supercapacitor. However, such continuous ripple current component can increase the internal temperature of the supercapacitor and hence deteriorate its lifetime [61]. Hence, it is vital to identify a suitable second-order harmonic ripple current reduction method for the boost inverter based battery-supercapacitor HESS.

Chapter 6 extensively analyzed the operation of an existing waveform control method for the boost inverter and demonstrated that the capacitance tolerances and ESR of the inductors affect the performance of the waveform control method. A rule-based controller which generates the required output capacitor reference voltages for the waveform control ripple current reduction method was proposed in Chapter 6 [67]. The rule-based controller eliminated possible inaccuracies occurred in the traditional waveform control method due to the capacitor tolerances and inductor ESR values and was able to achieve better performance.

The rule-based control method employed a perturb and observe (P&O) approach to generate the required output capacitor reference voltages and the controller required about 2 seconds to perform the P&O process. The time required for the P&O operation limited how frequently the reference active or reactive power can change which is not desirable in the battery-supercapacitor HESS since the HESS should be able to operate under variable output power conditions.

A current feedback ripple reduction method proposed in [68] is presented in this chapter. First, the ripple current reduction in a single boost inverter is considered. Effectiveness of the proposed method is theoretically analyzed. In the proposed method, the output capacitor voltage reference signals are modified using the DC side current feedback signal as opposed to the complex calculations required in the waveform control method. Hence, performance of the proposed method is not affected by the capacitance tolerances of the output capacitors. Moreover, the proposed method is able to reduce the second-order harmonic ripple current at the DC side of the boost inverter without increasing other frequency harmonic components. Compared to the rule-based control ripple reduction method, the current feedback method is able to

achieve superior second-order harmonic ripple current reduction as well as better dynamic performance. The method is experimentally verified using a single-phase grid connected battery ESS prototype. Later in the chapter, the current feedback method is applied to the boost inverter based battery-supercapacitor HESS [69]. Effectiveness of the current feedback method on the supercapacitor current second-order harmonic ripple reduction is demonstrated experimentally.

7.2 Current Feedback Ripple Current Reduction Method

The configuration of a single phase grid connected boost inverter is shown in Fig. 7.1 and the operation of the boost inverter was discussed in Chapter 2. The voltages across the output capacitors C_1 and C_2 are controlled to follow voltage references given by,

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2}\sin(\omega t + \delta) \tag{7.1}$$

and

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2}\sin(\omega t + \delta). \tag{7.2}$$

respectively. V_o, ω, and δ are the inverter output voltage amplitude, frequency, and phase angle respectively. The boost inverter output current i_o is given by,

$$i_o = I_o \sin(\omega t + \alpha) \tag{7.3}$$

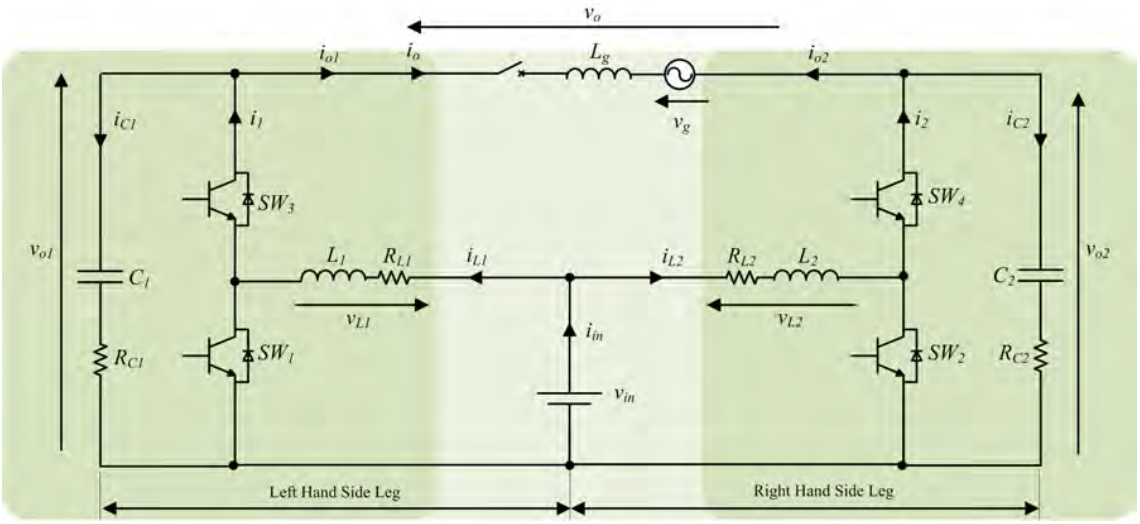

Fig. 7.1: Single phase grid connected boost inverter

where α is the phase angle of the inverter output current with respect to the grid voltage. The total input current to the boost inverter is given by

$$i_{in} = \frac{1}{v_{in}} \left[\frac{V_o I_o}{2} \cos(\alpha - \delta) + \frac{V_o}{2} \sqrt{\left[I_o^2 + \frac{C^2 \omega^2 V_o^2}{4} + V_o I_o C \omega \sin(\alpha - \delta) \right]} \cos(2\omega t - \theta) \right] \tag{7.4}$$

where

$$\cos\theta = \frac{-I_o \cos(\alpha + \delta) + \frac{C\omega V_o \sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2 \omega^2 V_o^2}{4} + V_o I_o C \omega \sin(\alpha - \delta) \right]}}$$

and $C = C_1 = C_2$. Please refer Appendix A.1 for the derivation. Then, the boost inverter input current can be re-written as,

$$i_{in} = i_{in,DC} + i_{in,AC} \tag{7.5}$$

where $i_{in,DC}$ and $i_{in,AC}$ are the DC and AC components of the total input current respectively.

The output capacitor voltage references $v_{o1,ref}$ and $v_{o2,ref}$ given by (7.1) and (7.2) can be modified as (7.6) and (7.7), without affecting the inverter differential output voltage.

$$v_{o1,ref} = V_{DC,ref} + \frac{V_o}{2} \sin(\omega t + \delta) - K i_{in.AC} \tag{7.6}$$

$$v_{o2,ref} = V_{DC,ref} - \frac{V_o}{2} \sin(\omega t + \delta) - K i_{in.AC} \tag{7.7}$$

where K is a feedback gain value. Then,

$$i_1 = I_o \sin(\omega t + \alpha) + C\omega \frac{V_o}{2} \cos(\omega t + \delta) - CK \frac{di_{in,AC}}{dt} \tag{7.8}$$

and

$$i_2 = -I_o \sin(\omega t + \alpha) - C\omega \frac{V_o}{2} \cos(\omega t + \delta) - CK \frac{di_{in,AC}}{dt} \tag{7.9}$$

Using (7.6), (7.7), (7.8), and (7.9), a differential equation for the input current AC component $i_{in,AC}$ can be obtained as

$$\frac{di_{in,AC}}{dt} = \frac{v_{in}}{(2V_{DC}CK - 2CK^2 i_{in,AC})} (i_{in,AC0} - i_{in,AC}) \tag{7.10}$$

where

$$i_{in,AC0} = \frac{V_o}{2v_{in}} \sqrt{\left[I_o^2 + \frac{C^2 \omega^2 V_o^2}{4} + V_o I_o C \omega \sin(\alpha - \delta) \right]} \cos(2\omega t - \theta) \tag{7.11}$$

corresponds to the AC component of the input current i_{in} given in (7.4) for the unmodified output capacitor reference voltages (7.1) and (7.2). Please refer Appendix A.1 for the derivation.

Before finding an analytical solution, first, a numerical solution of the differential equation (7.10) is found using Matlab for a sample case of inverter supplying 15W active power and 10VAr reactive power to the grid and considering experimental prototype parameters summarized in Table 7.1. Fig. 7.2(a) illustrates the second-order harmonic component amplitude ($m_{2\omega}$) and the fourth-order harmonic component amplitude ($m_{4\omega}$) of the obtained numerical solution for various values of the feedback gain K. From Fig. 7.2(a) it is evident that the higher the value of the feedback gain K the more significant is the reduction in the second-order as well as the fourth-order harmonic components of the input current. A change in $m_{2\omega}$ for a unit change in K, ($\Delta m_{2\omega}$) is shown in Fig. 7.2(b). As K becomes larger, the change in $m_{2\omega}$ becomes smaller. Using this result, the required minimum value for K can be found such that,

$$|\Delta m_{2\omega}| \leq |\Delta m_{2\omega,\max}| \tag{7.12}$$

where $\Delta m_{2\omega,\max}$ is a pre-determined value of the maximum allowed change in $m_{2\omega}$ for a unit change in K for all possible output power conditions. Then, for the selected maximum change in the second-order harmonic ripple amplitude for a unit change in K, $\Delta m_{2\omega,\max}$, the bounds on K are given by,

$$0 < K \leq [K|(\Delta m_{2\omega,\max} \geq |\Delta m_{2\omega}|)]\,. \tag{7.13}$$

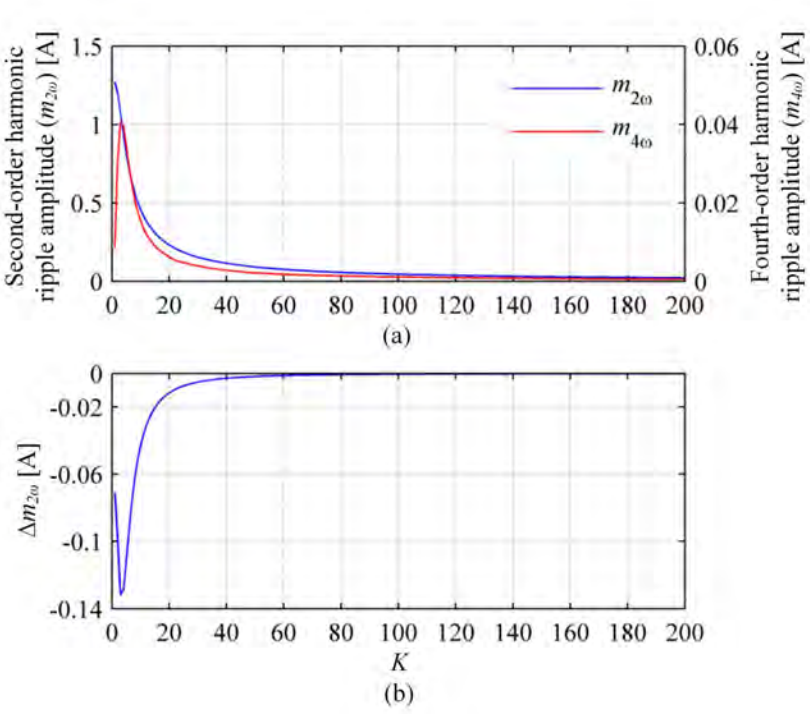

Fig. 7.2: Numerical solution of the variation of the input current with K, (a) the second and the fourth-order harmonic current ripple amplitude, (b) change in the second-order harmonic ripple amplitude for a unit change in K.

Now, to obtain an analytical solution of the second-order harmonic input current amplitude $m_{2\omega}$, it is assumed that the steady state input current AC component with the modified output capacitor voltage references is

$$i_{in,AC} = m_{2\omega}\cos(2\omega t + \theta_{2\omega}) + m_{4\omega}cos(4\omega t + \theta_{4\omega}) \tag{7.14}$$

The input current AC component differential equation (7.10) can be re-written as

$$2V_{DC}CK\frac{di_{in,AC}}{dt} - 2CK^2 i_{in,AC}\frac{di_{in,AC}}{dt} + v_{in}i_{in,AC} = v_{in}i_{in,AC0} \tag{7.15}$$

After substituting (7.14) into (7.15) and simplifying, (7.16) is obtained.

$$\begin{aligned} -4V_{DC}CK\omega m_{2\omega}\sin(2\omega t + \theta_{2\omega}) + 2CK^2\omega m_{2\omega}m_{4\omega}\sin(2\omega t + \theta_{4\omega} - \theta_{2\omega}) \\ + v_{in}m_{2\omega}\cos(2\omega t + \theta_{2\omega}) = v_{in}i_{in,AC0}. \end{aligned} \tag{7.16}$$

Considering that the product $m_{2\omega}m_{4\omega} \approx 0$, since $m_{2\omega}$ and $m_{4\omega}$ are very small when K is high, the magnitude of the second-order harmonic component in (7.16) can be found as

$$m_{2\omega} = \frac{v_{in}|i_{in,AC0}|}{\sqrt{(-4V_{DC}CK\omega)^2 + v_{in}^2}} \tag{7.17}$$

Fig. 7.3(a) compares the obtained analytical solution (7.17) with the numerical solution found using Matlab when the inverter delivers 15W, 10VAr to the grid. The error between the numerical and the analytical solution ($m_{2\omega,numerical} - m_{2\omega,analytical}$) is shown in Fig. 7.3(b) and proves the validity of (7.17) for higher values of K.

For further evaluation of the proposed method, a ripple reduction factor R is defined as the ratio of $m_{2\omega}$ before and after application the current feedback method. The ripple reduction factor R can be derived from (7.17) as

$$R = \frac{\sqrt{(4V_{DC}CK\omega)^2 + v_{in}^2}}{v_{in}} \tag{7.18}$$

To ensure proper operation of the boost inverter the DC shift of the output capacitor voltage V_{DC} has to meet condition

$$V_{DC} \geq v_{in} + \frac{V_o}{2} + \max(Ki_{in,AC}) \tag{7.19}$$

According to the numerical solution shown in Fig. 7.2(a), the second-order harmonic ripple component is the dominant component in the input current compared to the fourth-order harmonic component. Hence, (7.19) can be re-written as,

$$V_{DC} \geq v_{in} + \frac{V_o}{2} + \max(Km_{2\omega}) \tag{7.20}$$

Then, using (7.17) and assuming large K, (7.20) can be approximated as,

$$V_{DC} \geq v_{in} + \frac{V_o}{2} + \frac{v_{in}\max(|i_{in,AC0}|)}{4V_{DC}C\omega} \tag{7.21}$$

where

$$\max(|i_{in,AC0}|) = \frac{V_o}{2v_{in}}\sqrt{\left[I_{o,max}^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_{o,max}C\omega\right]}. \tag{7.22}$$

Then, the minimum required DC voltage shift V_{DC} for the output capacitor reference voltages can be calculated from,

$$V_{DC} \geq V_{DC,\min} \tag{7.23}$$

where

$$V_{DC,\min} = \frac{2C\omega(V_o + 2v_{in}) + \sqrt{[2C\omega(V_o + 2v_{in})]^2 + 16C\omega v_{in}\max(|i_{in,AC0}|)}}{8C\omega}. \tag{7.24}$$

Then, the maximum output capacitor voltage $V_{o1,\max}$ when $V_{DC} = V_{DC,\min}$ is,

$$V_{o1,\max} = V_{DC,\min} + \frac{V_o}{2} + \frac{v_{in}\max(|i_{in,AC0}|)}{4V_{DC,\min}C\omega} \tag{7.25}$$

The relationship between the $V_{DC,\min}$ and $V_{o1,\max}$ versus the output capacitor value C for the experimental prototype parameters given in Table 7.1 is illustrated in Fig. 7.4. The required output capacitor value $C_{req,i}$ can be found as explained in Chapter 6 [67]. First, the maximum allowable output capacitor voltage is obtained using the input voltage v_{in} and the maximum gain of the converter legs $G_{\max}$, as $V_{o1,\max} = v_{in}G_{\max}$. Then, the required output capacitor value $C_{req,i}$ and the minimum DC voltage shift corresponding to $V_{o1,\max}$ can be found from Fig. 7.4. A detailed comparison of the output capacitor

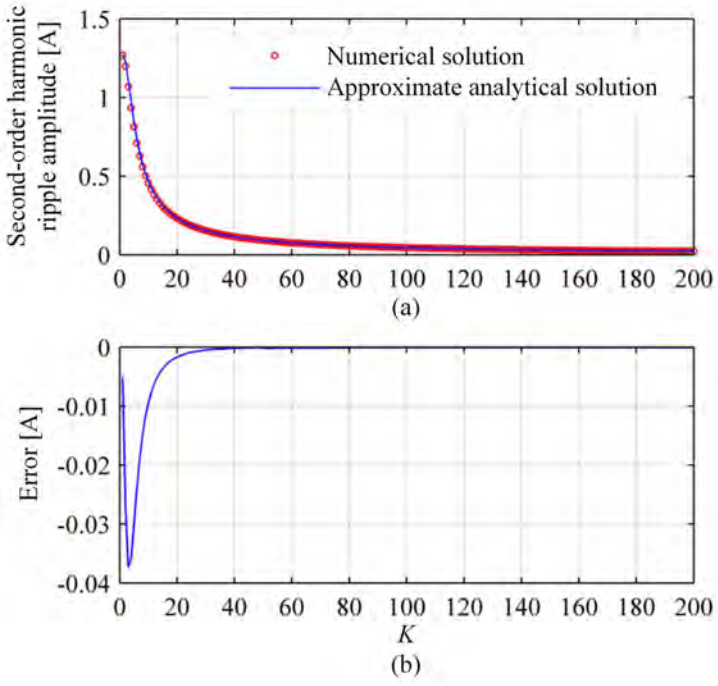

Fig. 7.3: Comparison of the numerical and approximated analytical solution, (a) the second-order harmonic current ripple amplitude, (b) error between the numerical and analytical solution.

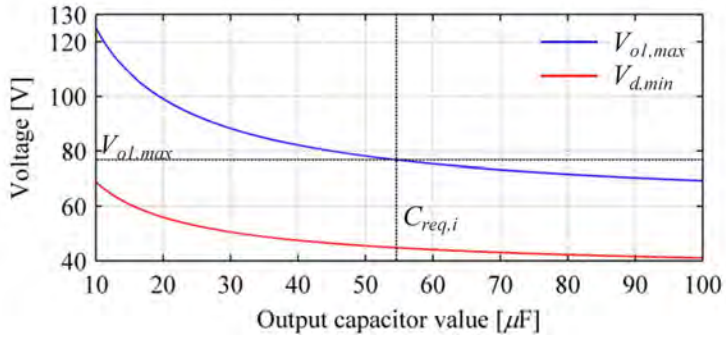

Fig. 7.4: Illustration of the effect of (a) the output capacitor tolerance and (b) the input voltage variation on the ripple reduction method performance when P=15W and Q=10VAr

requirement for the boost inverter operation without and with an output capacitor voltage modified ripple reduction method can be found in Chapter 6 [67].

7.3 Boost Inverter Control System with the Current Feedback Method

The overall block diagram of the grid-connected boost inverter with the proposed ripple current reduction method is shown in Fig. 7.5. A set of band-pass filters are employed to obtain the AC component of the input current with minimum phase distortion and to block any DC component of the input current in the feedback path.

The maximum gain of the boost converter leg is taken as 6 and hence $V_{o1,\max}$ equals to 76.8V. Then, the required output capacitor value for the operation of the boost inverter with the current feedback method is obtained from Fig. 7.4 as 54.6 μF. The nearest commercially available value of 60 μF was selected for the experimental setup.

The minimum required feedback gains K to satisfy (7.12) for $\Delta m_{2\omega,\max} = 0.001$ A are calculated for each output power condition. The calculated feedback gains are illustrated in Fig. 7.6. Then, the value of K=100 is selected to satisfy (7.12) for all output power conditions. To verify the validity of the approximated analytical solution for the selected K, the error between the numerical solution and the analytical solution for all output power conditions and K=100 is illustrated in Fig. 7.7. It is evident that the error is negligible.

A double loop (DL) control method is used to control the boost converter legs as presented in Chapter 3. The power allocation is achieved using a high pass filter and a SCVC based power allocation method as explained in Chapter 3. The active and reactive power flow between the boost inverter and the grid is achieved by controlling the inverter output voltage amplitude and phase angle with respect to the grid voltage.

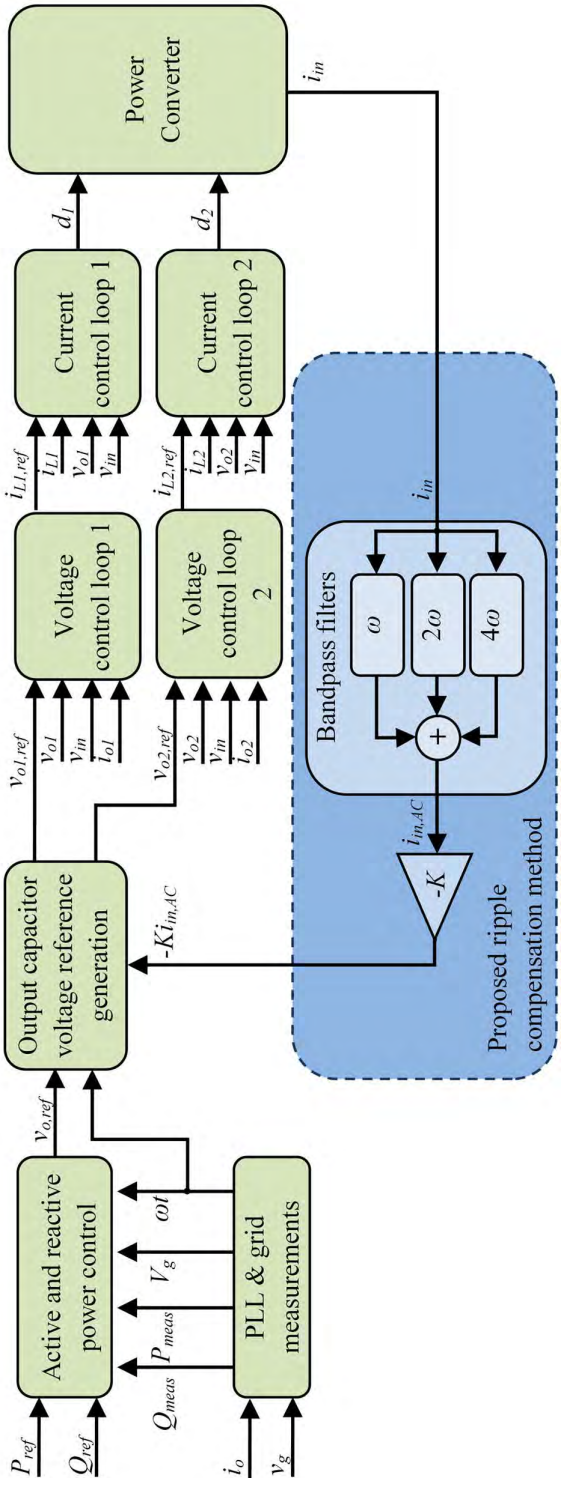

Fig. 7.5: Overall block diagram of the control system

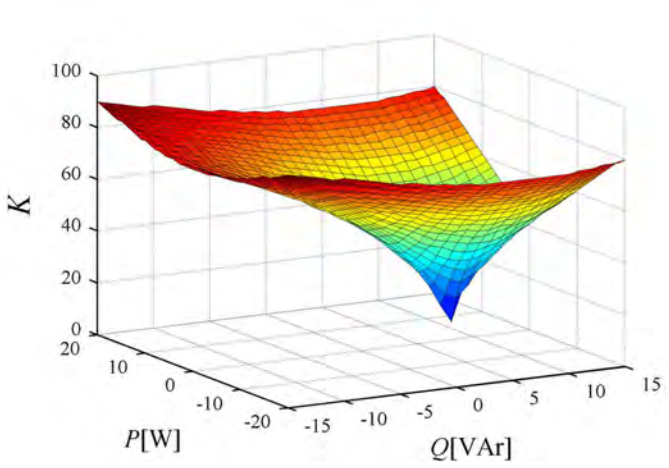

Fig. 7.6: Illustration of the required feedback gains K to satisfy (7.12) for each output power condition.

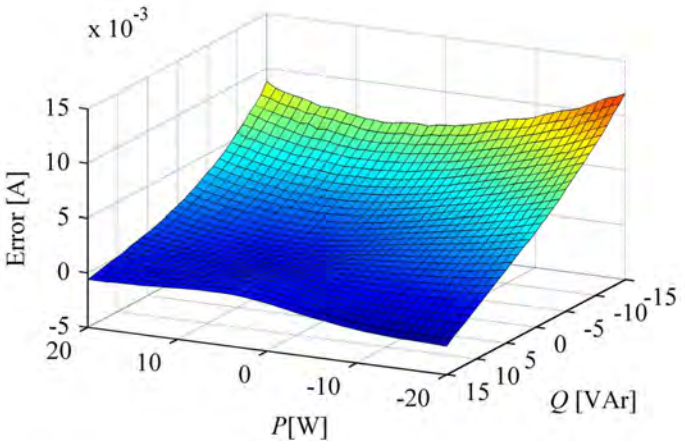

Fig. 7.7: Error between the numerical solution and the analytical solution for all output power conditions and K=100.

7.4 Experimental Results

The proposed current ripple reduction method for a grid connected boost inverter was verified using an experimental prototype and the parameters of the experimental prototype are summarized in Table 7.1. A 6.4Ah, 12.8V $LiFePO_4$ battery from K2 Energy and a 16V, 58F Maxwell supercapacitor module are used in the prototype.

Fig. 7.8 illustrates operation of the single-phase grid connected boost inverter with and without the proposed second-order harmonic ripple reduction method when delivering 15W active and 10VAr reactive power to the grid. The output capacitor voltage waveforms and the inverter output voltage are shown in Figs. 7.8(a) and 7.8(b) without and with the proposed method respectively. The inverter output voltage remains unchanged despite the modification of the output capacitor voltages. The operation of the active and reactive power controller is illustrated in Figs. 7.8(c) and 7.8(d). Figs. 7.8(e) and 7.8(f) depict the

Table 7.1: Experimental prototype parameters

Parameter	**Value**	**Parameter**	**Value**
Power converter parameters			
V_o	40 V	f	50 Hz
C_1, C_2	60 μF	L_1,L_2	210 μH
$I_{o,max}$	1 A	T_F	0.001
$V_{DC,ref}$	42 V	f_{sw}	20 kHz
R_{L1}, R_{L2}	0.24 Ω		
Grid parameters			
V_g	40 V	L_g	20 mH
Voltage control loop parameters			
$K_{p,PR}$	0.1	$K_{i1,PR}$	4
$K_{i2,PR}$	6	ω_{c1}, ω_{c2}	0.5
Current control loop parameters			
$K_{p,PI}$	2.615	$K_{i,PI}$	8.44×10^{-5}

inductor current waveforms of the boost converter legs and the total input current to the boost inverter without and with the proposed ripple current reduction method respectively. The inductor current waveforms modified due to the changes in the output capacitor voltage waveforms and a significant reduction of the input current ripple component can be observed.

The frequency spectrum characteristics of the boost inverter DC side current with and without the proposed ripple current reduction method are compared in Figs. 7.8(g) and 7.8(h). The second-order harmonic ripple amplitude is reduced from 1.482A to 0.0588A, achieving approximately 25 times second-order harmonic ripple current reduction. In addition, the proposed method reduced the first-order harmonic current component amplitude from 0.085A to 0.036A and the fourth-order harmonic current component amplitude from 0.037A to 0.004A. The frequency spectrum characteristics illustrate the ability of the proposed system to mitigate the second-order harmonic ripple component of the boost inverter input current without increasing other harmonic current components.

Dynamic performance of the proposed ripple current reduction method is shown in Fig. 7.9. At t=2s, 15W active power and 10VAr reactive power reference step change was applied. Without the proposed method, the second-order harmonic ripple amplitude reaches 1.482A due to output power step change. However, with the proposed system, the maximum second-order harmonic ripple amplitude during the transient time is 0.172A

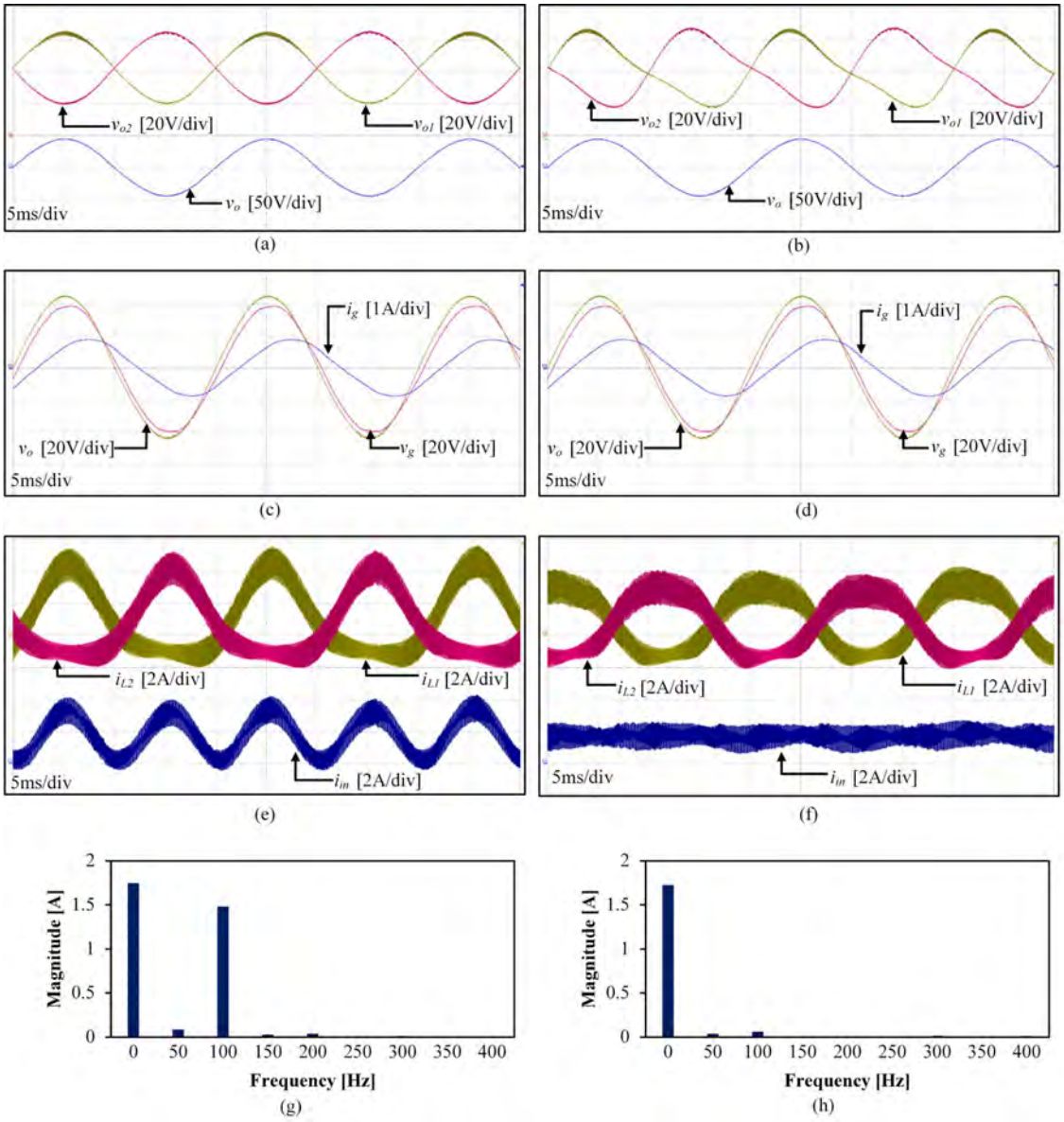

Fig. 7.8: Experimental results illustrating operation of the battery storage system when delivering 15W active power and 10VAr reactive power. (a) Output capacitor voltage waveforms and inverter output voltage without the proposed controller, (b) Output capacitor voltage waveforms and inverter output voltage with the proposed controller, (c) Inverter output voltage, grid voltage and inverter output current without the proposed controller, (d) Inverter output voltage, grid voltage and inverter output current with the proposed controller, (e) Inductor currents and total input current of the boost inverter without the proposed controller, (f) Inductor currents and total input current of the boost inverter with the proposed controller, (g) Frequency characteristics of the input current without the proposed controller and (h) Frequency characteristics of the input current with the proposed controller.

and reduces to 0.0588A in the steady state. This validates the ability of the proposed method to reduce the second-order harmonic current component even during the active and reactive power transients.

The boost inverter input current ripple reduction achieved using the proposed current

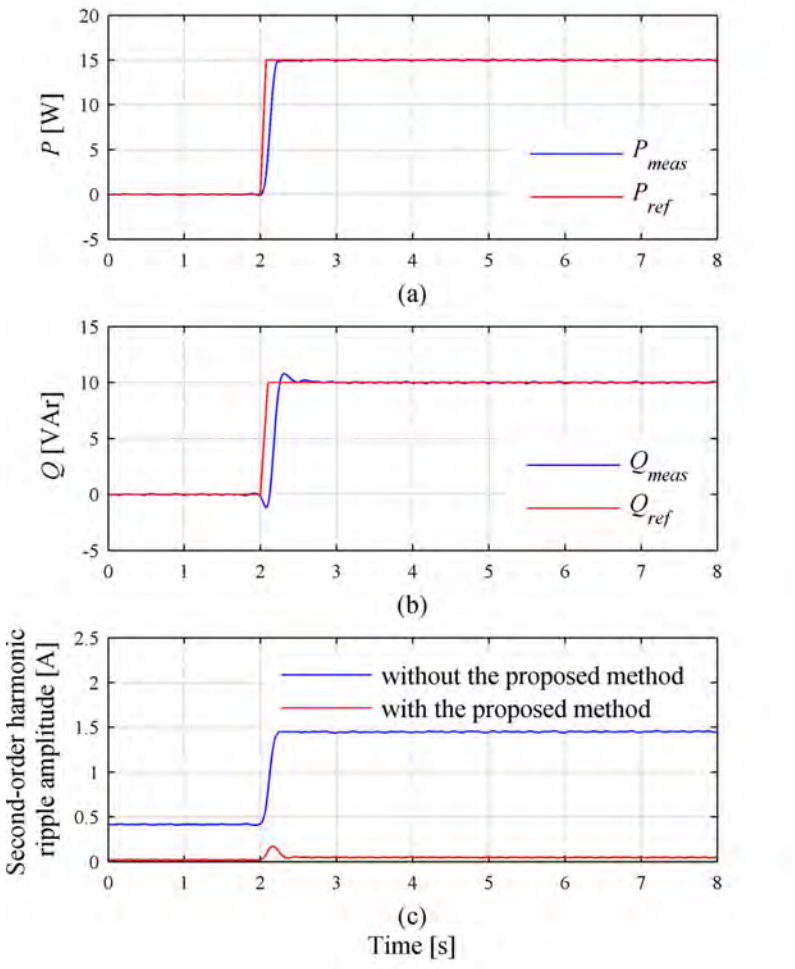

Fig. 7.9: Experimental results illustrating transient operation of the proposed control system in response to 15W and 10VAr power step change, (a) Inverter output active power, (b) inverter output reactive power (c) second-order harmonic ripple amplitude with and without the proposed method.

feedback method is compared with the waveform control method [74] and the rule-based control method [67] for all the output power conditions in Fig. 7.10. In order to have a fair comparison, the same experimental setup and control parameters as in [67] were used. It can be observed that the proposed current feedback method is able to reduce the second-order harmonic ripple current more than twenty times for all output power conditions.

The change in the second-order harmonic ripple current amplitude $|\Delta m_{2\omega}|$ for a unit change in K is illustrated for each output power condition in Fig. 7.11. The result validates that the selection of the feedback gain K=100 results in the change in the second-order harmonic ripple current amplitude $|\Delta m_{2\omega}| < 0.001$ for all output power conditions.

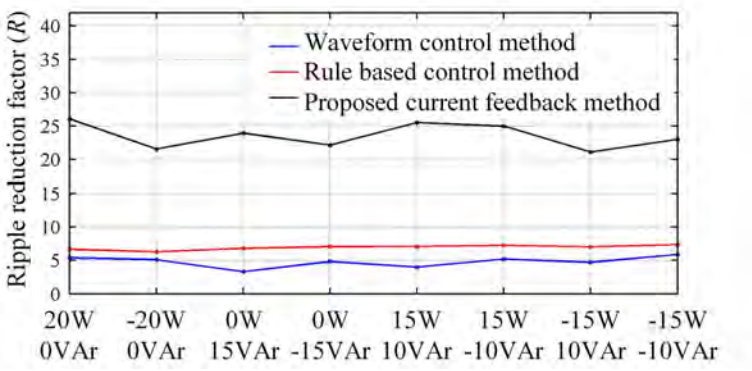

Fig. 7.10: Comparison of the ripple current reduction using the waveform control method, the rule-based control method and the proposed current feedback method (K=100).

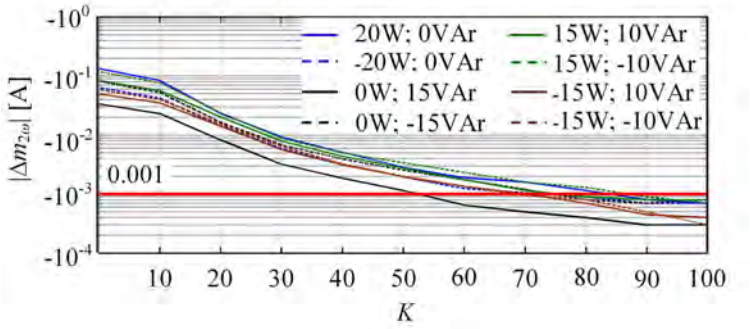

Fig. 7.11: Experimental results illustrating change in the second-order harmonic ripple current amplitude $\Delta m_{2\omega}$ for a unit change in K for all output power conditions.

7.5 Battery-Supercapacitor HESS with Reduced Low Frequency Input Current Ripple

The current feedback ripple reduction method is able to reduce the second-order harmonic ripple component at the DC side of the boost inverter. Compared to the existing ripple current reduction methods for the boost inverter, the current feedback method achieved significant ripple current reduction without increasing other harmonic components. Furthermore, the current feedback method is able to achieve a significant ripple current reduction even in the output power transients.

In this section, the current feedback ripple reduction method is applied to the boost inverter based battery-supercapacitor HESS presented in Chapter 3 to reduce the second-order harmonic ripple current component in the supercapacitor current [69].

7.5.1 Second-order Harmonic Ripple Component in the Supercapacitor Current

The configuration of the boost inverter based grid connected battery-supercapacitor HESS is illustrated in Fig. 7.12.

The instantaneous output power from the left hand side boost converter legs can be written as,

$$P_{o1} + P_{C1} = (i_{o1} + i_{C1})v_{o1}. \tag{7.26}$$

Similarly,

$$P_{o2} + P_{C2} = (i_{o2} + i_{C2})v_{o2}. \tag{7.27}$$

Then, assuming a lossless power conversion,

$$P_{in,HESS} = P_{o1} + P_{o2} + P_{C1} + P_{C2}. \tag{7.28}$$

where $P_{in,HESS}$ is the total input power to the HESS. Then,

$$P_{in,HESS} = \left[\frac{V_o I_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha-\delta)\right]}\cos(2\omega t-\theta)\right] \tag{7.29}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \frac{C\omega V_o\sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha-\delta)\right]}}$$

From (7.29), the HESS total input power contains a DC component which corresponds to the HESS output power and a second-order harmonic power component. According to the power allocation strategy, the second-order harmonic power component is allocated to the supercapacitor.

7.5.2 Current Feedback Method for the HESS

The supercapacitor current of the battery-supercapacitor HESS can be written as,

$$i_{sc} = i_{sc,DC} + i_{sc,AC} \tag{7.30}$$

where $i_{sc,DC}$ and $i_{sc,AC}$ are the DC and AC components of the supercapacitor current. The output capacitor reference voltages of the HESS can be modified as,

$$v_{o1,ref} = V_{DC,ref} + \frac{V_{o,ref}}{2} - Ki_{sc,AC} \tag{7.31}$$

$$v_{o2,ref} = V_{DC,ref} - \frac{V_{o,ref}}{2} - Ki_{sc,AC} \tag{7.32}$$

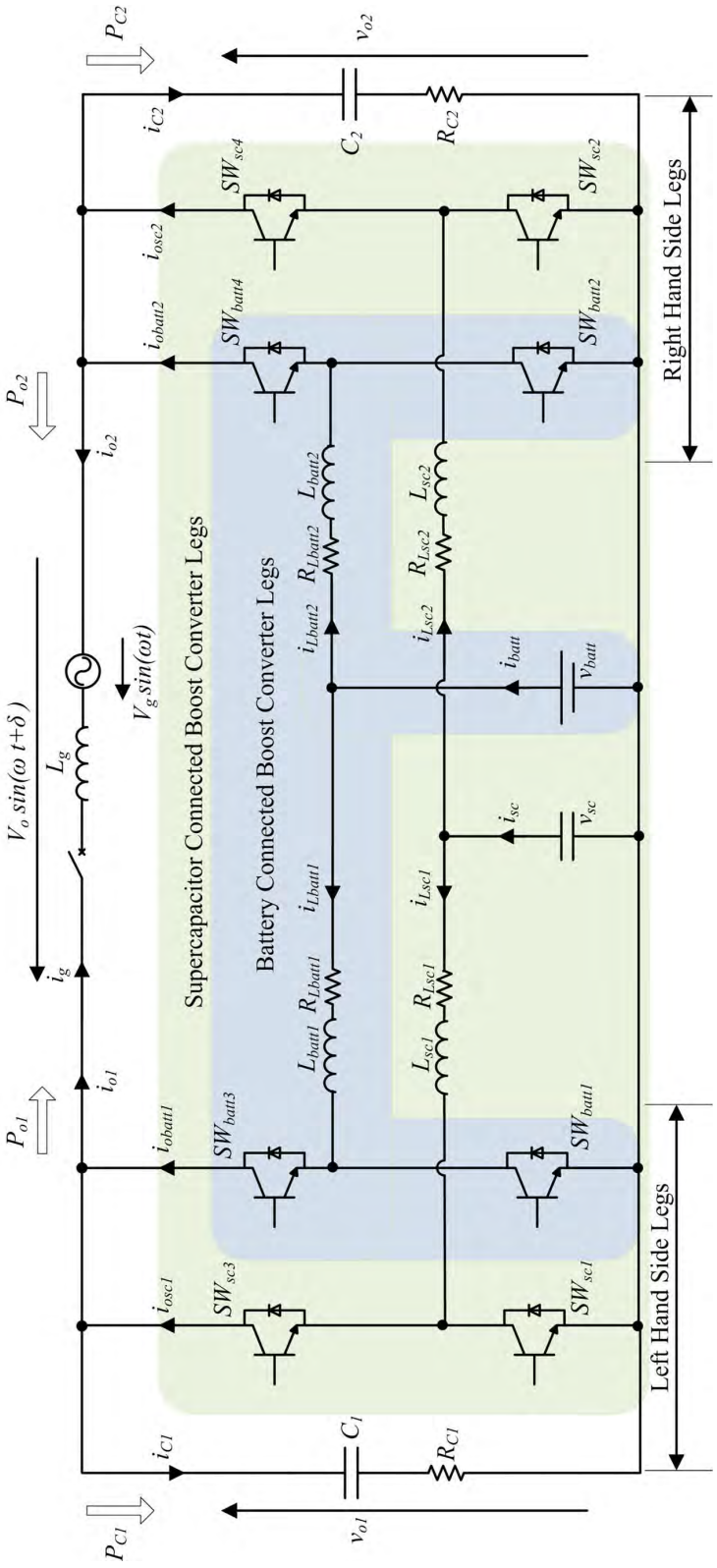

Fig. 7.12: Single-phase grid-connected battery-supercapacitor hybrid energy storage system

where K is the feedback gain. Then, the total instantaneous input power supplied by the HESS can be obtained as,

$$P_{in,HESS} = v_{batt}i_{batt} + v_{sc}i_{sc,DC} + v_{sc}i_{sc,AC} = \frac{V_o I_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha-\delta)\right]}\cos(2\omega t-\theta) - 2CKV_{DC}\frac{di_{sc,AC}}{dt} + 2CK^2 i_{sc,AC}\frac{di_{sc,AC}}{dt} \quad (7.33)$$

Considering the AC component of (7.33), a differential equation for the supercapacitor current AC component can be obtained as,

$$\frac{di_{sc,AC}}{dt} = \frac{v_{sc}}{(2V_{DC}CK - 2CK^2 i_{sc,AC})}(i_{sc,AC0} - i_{sc,AC}) \quad (7.34)$$

where

$$i_{sc,AC0} = \frac{V_o}{2v_{sc}}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha-\delta)\right]}\cos(2\omega t-\theta) \quad (7.35)$$

is the AC component of the supercapacitor current with the unmodified output capacitor reference voltages.

First, a numerical solution for (7.34) is obtained using Matlab differential equation solver when the HESS is supplying 15W active power and 10VAr reactive power to the grid as a sample case. For all the calculations, prototype parameters presented in Chapter 3 are used. The second-order harmonic amplitude ($m_{2\omega}$) and the fourth-order harmonic amplitude ($m_{4\omega}$) of the obtained numerical solution for various values of K at steady state ($v_{sc} = v_{sc,ref}$) are illustrated in Fig. 7.13(a). It can be observed that a higher feedback gain K leads to a significant reduction in both the second-order and the fourth-order harmonic components in the supercapacitor current. Fig. 7.13(b) illustrates the change in $m_{2\omega}$ for a unit change in K and it can be observed that as K increases, the change in $m_{2\omega}$ becomes smaller. Then the required minimum value for the feedback gain K can be calculated such that,

$$|\Delta m_{2\omega}| \leq \Delta m_{2\omega,max} \quad (7.36)$$

where $\Delta m_{2\omega,max}$ is the maximum allowed change in $m_{2\omega}$ for a unit change in K for all HESS output power conditions.

As presented in Section 7.2, an analytical solution for the supercapacitor current second-order harmonic component can be obtained as,

$$m_{2\omega} = \frac{v_{sc}|i_{sc,AC0}|}{\sqrt{(-4V_{DC}CK\omega)^2 + v_{sc}^2}} \quad (7.37)$$

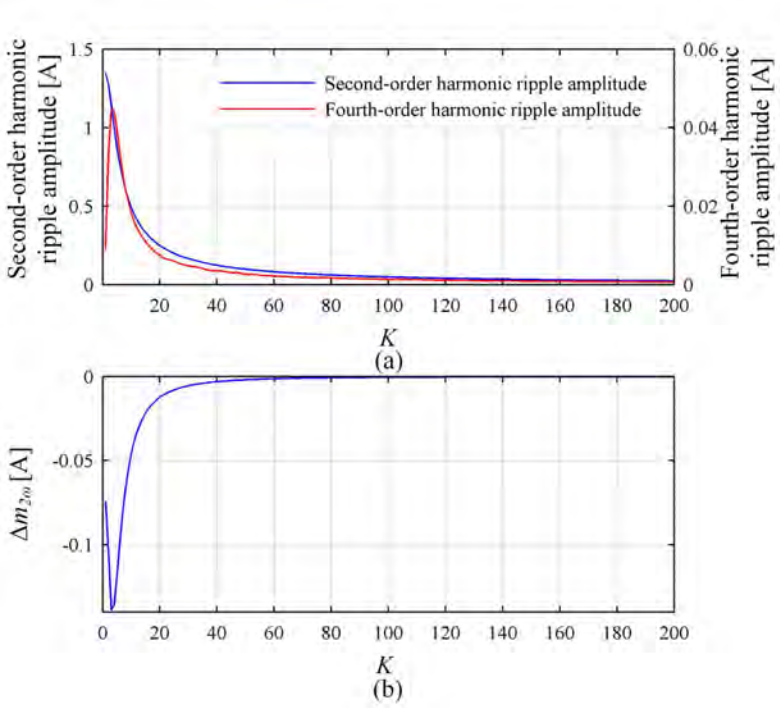

Fig. 7.13: Variation of the supercapacitor current numerical solution with K, (a) the second and the fourth-order harmonic current ripple amplitudes, (b) change in the second-order harmonic ripple amplitude for a unit change in K.

7.5.3 Experimental Results

A 6.4Ah, 12.8V, 81.92Wh $LiFePO_4$ battery from K2 Energy and a 16V, 58F, 7424J Maxwell supercapacitor module are used in the experimental prototype. The HESS control system is implemented on a DSpace DS1006 system using Matlab Simulink. Fig. 7.14 illustrates the overall block diagram of the single-phase grid connected HESS with the ripple current reduction method. The same double loop control system with the filter based power allocation method presented in Chapter 3 is used in the experiments.

To obtain the AC component of the supercapacitor current with minimum phase distortion and to block any DC component flowing in to the feedback path, a set of band-pass filters are used. For each output power condition, the minimum required feedback gain is calculated to satisfy (7.36) when $\Delta m_{2\omega,max} = 0.001$ A, and illustrated in Fig. 7.15. Then K is selected as 100 to satisfy (7.36) for all output power conditions.

A DL controller is used to control the boost inverter as explained in Chapter 3 and the same controller and converter parameters as in Chapter 3 are considered.

Fig. 7.16 depicts the steady state operation of the HESS without and with the current feedback ripple reduction method when delivering 15W and 10VAr power to the grid. Figs. 7.16(a) and 7.16(b) show the output capacitor voltage waveforms and the HESS output voltage waveforms without and with the ripple reduction method respectively.

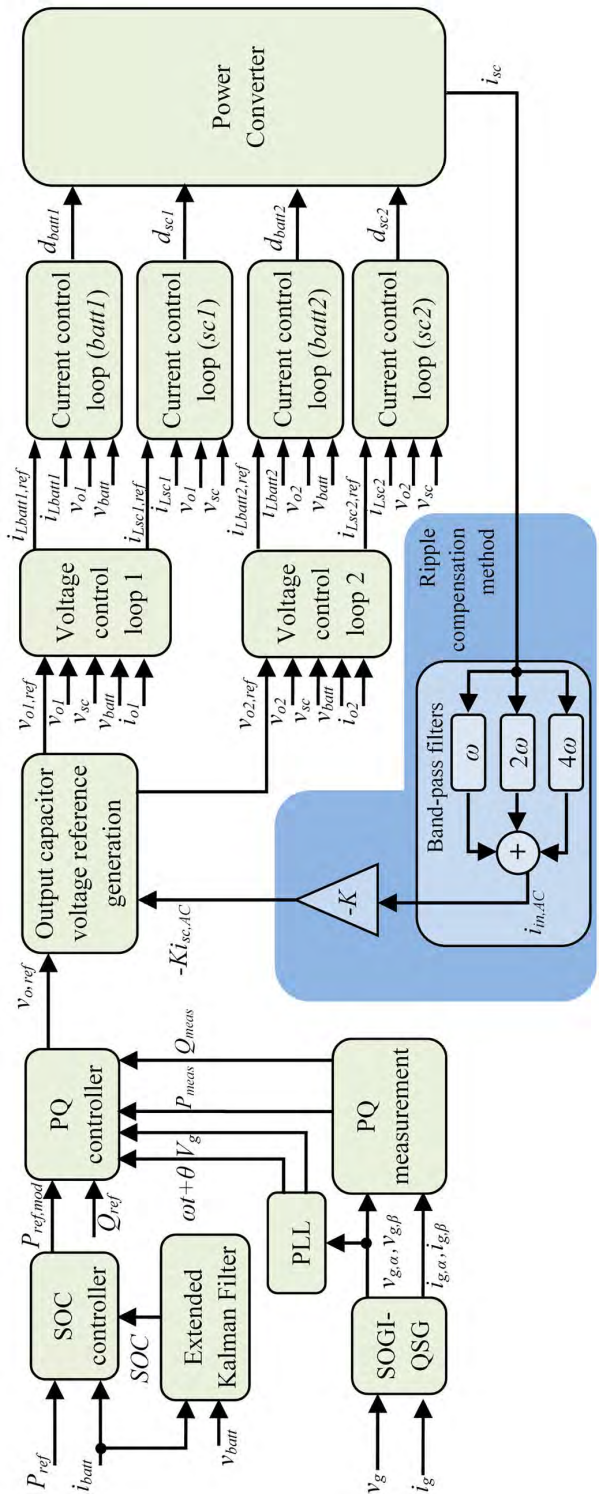

Fig. 7.14: Overall block diagram of the control system

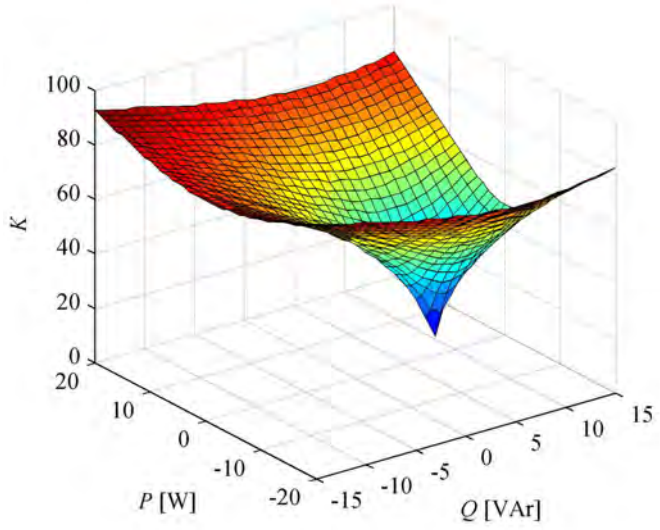

Fig. 7.15: Illustration of the required feedback gains K to satisfy (7.36) for each output power condition.

The battery current and the supercapacitor current without the ripple reduction method are illustrated in Fig. 7.16(c), and it can be observed that the battery supplies the required average current while the supercapacitor supplies the second-order harmonic current component.

The battery and the supercapacitor current waveforms with the ripple reduction method are shown in Fig. 7.16(d) and a significant reduction in the supercapacitor current ripple component can be observed.

The frequency spectrums of the supercapacitor current without and with the ripple reduction method are shown in Figs. 7.16(e) and 7.16(f), respectively. The second-order harmonic ripple amplitude is reduced from 1.656A to 0.061A which corresponds to approximately 27 times ripple reduction. Moreover, the fourth-order harmonic ripple component of the supercapacitor is reduced from 0.102A to 0.043A.

Operation of the HESS with the ripple current reduction method for a step changing output power profile is illustrated in Fig. 7.17. It can be observed that the supercapacitor responds to sudden power changes and the battery current gradually increases to supply the required average power output. The battery current settles down to supply the required average current ones the supercapacitor is recharged to the reference voltage. Fig. 7.17 compares the second-order harmonic ripple amplitude without the ripple reduction method ($m_{2\omega,n}$) and with the ripple reduction method ($m_{2\omega,CFB}$). Significant supercapacitor current second-order harmonic ripple reduction can be observed in all output power conditions.

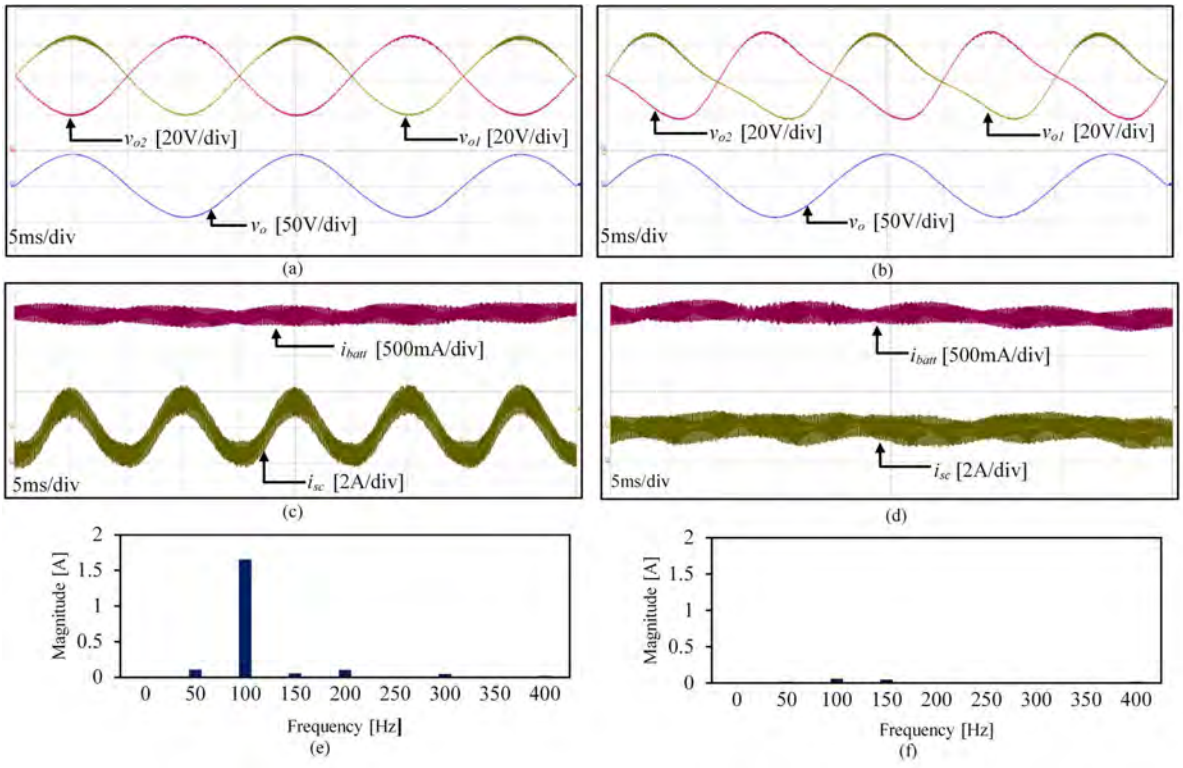

Fig. 7.16: Experimental waveforms of the HESS when delivering 15W active power and 10VAr reactive power. (a) Output capacitor voltage and inverter output voltage without the ripple reduction method, (b) output capacitor voltage and inverter output voltage with the ripple reduction method, (c) battery and supercapacitor currents without the ripple reduction method, (d) battery and supercapacitor currents with the ripple reduction method, (e) frequency characteristics of the supercapacitor current without the ripple reduction method and (f) frequency characteristics of the supercapacitor current with the ripple reduction method.

7.6 Conclusions

Due to the direct DC/AC power conversion, a second-order harmonic ripple current component appears in the DC side of the boost inverter based battery-supercapacitor HESS and the second-order harmonic current component was allocated to the supercapacitor as a way of extending the battery lifetime. However, the continuous ripple current component adversely affects the lifetime of the supercapacitor due to internal heating. Hence, it is vital to identify a suitable second-order harmonic ripple current reduction method, which can be applicable to the boost inverter based HESS.

The performance of the existing waveform control ripple reduction method was affected by the capacitor tolerances and the ESR of the boost inductors and a rule-based controller was proposed in Chapter 6 to overcome the issues associated with the existing waveform control ripple reduction method. Even though, the rule-based controller achieved better performances compared to the waveform control method, the rule-based controller required

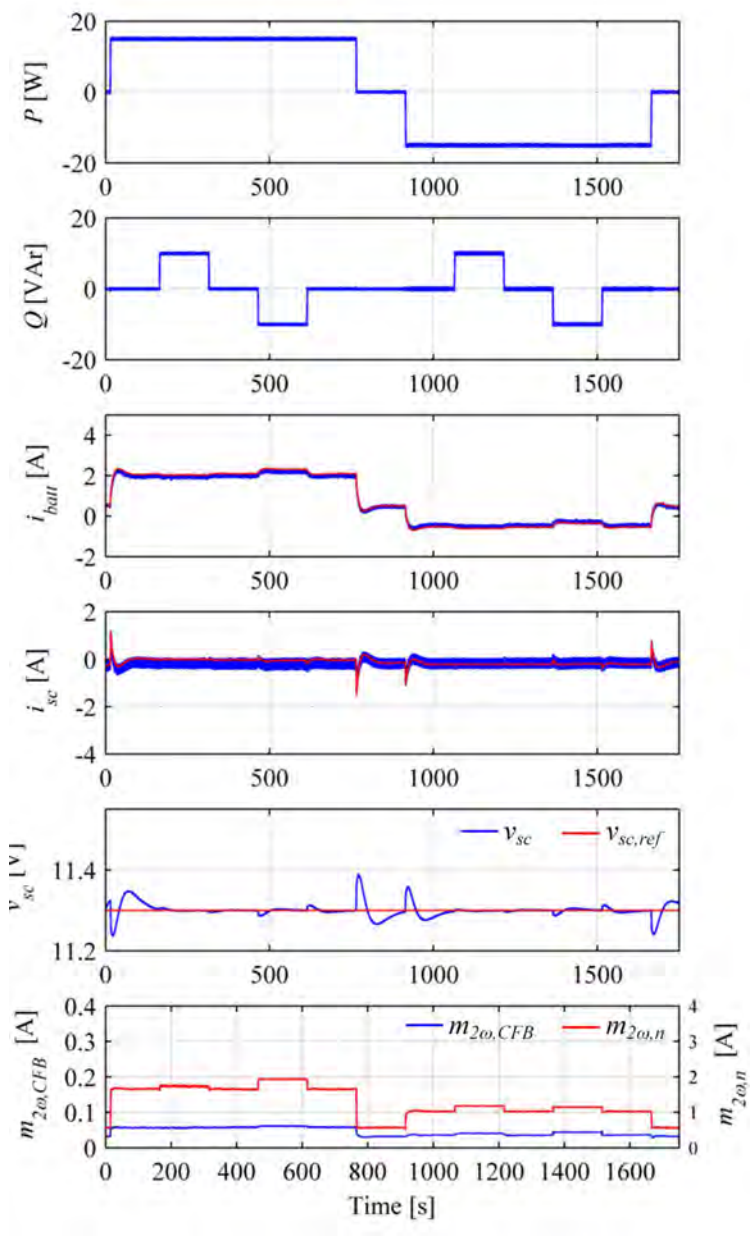

Fig. 7.17: Operation of the HESS with the current feedback ripple reduction method for a step changing output power profile.

about 2 seconds to perform the P&O process. This limits how frequently the change in the reference active or reactive power can occur and hence it limits the applicability of the rule-based controller for the boost inverter based battery-supercapacitor HESS.

A novel current feedback ripple reduction method was proposed in this chapter, The compensation signals were generated using the AC component of the boost inverter input current and the method achieved superior ripple reduction performance over the other methods. Furthermore, the current feedback method was able to mitigate the second-order harmonic ripple component of the boost inverter input current even in the output power

transients. The performance of the proposed current feedback method was validated using an experimental boost inverter prototype.

Later, the proposed current feedback ripple reduction method was applied to the boost inverter based battery-supercapacitor HESS. The boost inverter based HESS with the current feedback method was able to significantly reduce the second-order harmonic component of the supercapacitor current while operating as a conventional HESS where the fast power fluctuations were allocated to the supercapacitor. Operation of the proposed battery-supercapacitor HESS with reduced low frequency input current ripple was verified using experimental results.

The proposed boost inverter based HESS is the only single-phase direct grid connected battery-supercapacitor HESS where the second-order harmonic ripple current components as well as the switching frequency ripple current components of both the battery and the supercapacitor are mitigated. The ripple component reduction of the DC source currents reduces the internal heating and increases the lifetime of the DC sources.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The key objective of the research was to study and develop a single phase direct grid integrated battery-supercapacitor HESS. The boost inverter topology was identified as a suitable power converter configuration for the direct grid connected battery-supercapacitor HESS due to its ability to provide both the boosting and inversion functions in a single power processing stage.

Chapter 2 discussed the operation of the boost inverter topology which was used to design the single phase grid connected battery-supercapacitor HESS in this research. The switching frequency ripple component of the boost inverter DC side current was analyzed with the conventional in-phase PWM operation. Then, a phase shifted interleaved operation for the boost inverter topology was proposed and its effectiveness in reducing the switching frequency ripple component of the boost inverter DC side current was illustrated. Furthermore, a boost inverter component selection method for the interleaved boost inverter was also presented.

Chapter 3 presented the proposed interleaved boost inverter based single phase grid connected battery-supercapacitor HESS. A SCVC and a high-pass filter based power allocation method was employed to allocate the high frequency power variations and the second-order harmonic input current component to the supercapacitor. A DL control strategy was employed to control the power converter structure. A battery SOC controller with an extended Kalman filter based battery SOC estimator was developed. Experimental results were used to validate the operation of the proposed interleaved boost inverter based battery-supercapacitor HESS. The proposed boost inverter based HESS was able to allocate the fast power fluctuations and the second-order harmonic ripple current component to the supercapacitor while the battery supplied the steady power requirement.

The supercapacitor voltage was maintained around a reference voltage level to reduce the risk of supercapacitor over-charging and over-discharging. The battery SOC obtained using an extended Kalman filter was maintained within a safe SOC operating region. The interleaved operation was able to significantly reduce the switching frequency ripple component of both the battery and the supercapacitor currents. The proposed HESS was the first experimentally verified single phase direct-grid integrated battery-supercapacitor HESS. Furthermore, the proposed HESS was the only HESS designed to reduce the switching frequency ripple component of both the battery and the supercapacitor currents.

Chapter 4 analyzed the power allocation between the battery and the supercapacitor for a supercapacitor SOC controlled filter based battery-supercapacitor HESS. A SCEC and a filter based power allocation method was proposed to circumvent the challenges associated with the non-linearity of the SCVC and a filter based HESS power allocation method discussed in Chapter 3. Furthermore, a power allocation parameter selection method, an energy storage element sizing method and the dynamic behavior of the HESS power allocation method for a supercapacitor energy controlled filter based HESS were analyzed for a given HESS application. Experimental results were presented to illustrate the operation of the HESS and the validity of the selected power allocation parameters. The selected supercapacitor size enabled the operation of the HESS within the maximum and the minimum supercapacitor voltage limits.

Chapter 5 presented a novel fixed frequency SM controller for the boost inverter based battery-supercapacitor HESS. The PWM based fixed frequency SM controller was employed to overcome high and variable frequency operation associated with the traditional SM control technique. Theoretical aspects of the SM controller design were discussed and a SCEC based power allocation method was proposed to allocate the fast power fluctuations to the supercapacitor without incorporating an additional filter. The power allocation parameter selection and the supercapacitor sizing were discussed for a given HESS application. The proposed control system for the boost inverter based HESS was experimentally verified using a laboratory prototype. The proposed controller was able to satisfy the HESS output power requirement while allocating the ripple current and fast power fluctuations to the supercapacitor. Moreover, the selected HESS power allocation parameters and the value of the supercapacitor enabled the operation of the HESS within the pre-determined supercapacitor voltage limits. Compared to the traditional DL controlled boost inverter based battery-supercapacitor HESS, the proposed SM controller was able to achieve better output capacitor reference tracking and hence reduce the risk of the DC current injection into the grid when the ESR values of the boost inductors become unequal due to the tolerances and temperature variations.

In the boost inverter based battery-supercapacitor HESS presented in Chapter 3 to Chapter 5, the second-order harmonic ripple current component at the DC side of the converter was allocated to the supercapacitor as a way of extending the lifetime of the battery. However, such continuous ripple current will adversely affect the lifetime of the supercapacitor due to internal heating.

Chapter 6 and Chapter 7 were focused on identifying a suitable second-order harmonic ripple reduction method for the boost inverter based battery-supercapacitor HESS.

Chapter 6 extensively studied the operation of the existing waveform control ripple reduction method for the boost inverter and illustrated that the performance of the waveform control method can be affected by the output capacitor tolerances and ESR values of the boost inductors. Hence, a novel rule-based controller was proposed to overcome the limitations of the waveform control method. The performance of the rule-based controller was experimentally verified and unlike the waveform control method, the performance of the rule-based controller was not affected by the output capacitor tolerances and ESR values of the boost inductors. However, the rule-based controller required about 2 seconds to reduce the ripple current component once a change in the active or reactive power occurred. Hence, it is not applicable if the boost inverter based battery-supercapacitor HESS is required to operate under variable output power conditions.

A novel current feedback ripple reduction method was proposed for the boost inverter topology in Chapter 7. The compensation signals for the output capacitor reference voltages were generated using an input current feedback signal. The experimental results illustrated a superior second-order harmonic ripple current reduction compared to the waveform control method as well as to the rule-based control method. Furthermore, the proposed current feedback ripple reduction method was able to achieve a significant ripple current reduction even during the output power transients and hence it is applicable to the boost inverter based battery-supercapacitor HESS operating under variable output power conditions. Then, the proposed current feedback ripple reduction method was applied to the boost inverter based HESS and the experimental results illustrated a significant second-order harmonic ripple component reduction in the supercapacitor current.

The proposed battery-supercapacitor HESS was the first experimentally verified single phase direct grid integrated HESS. Furthermore, the proposed HESS was the only single phase battery-supercapacitor HESS which is able to reduce both the second-order harmonic ripple component and the switching frequency ripple component of both the battery and the supercapacitor currents. The proposed SCEC and filter based power allocation method enabled precise sizing of the energy storage elements and also

selection of the power allocation parameters. The HESS was able to allocate the fast power fluctuations to the supercapacitor while operating within the battery and the supercapacitor SOC limits. The proposed fixed frequency SM controller was able to achieve better output capacitor reference tracking and hence reduced the risk of the DC current injection into the grid. Furthermore, the proposed SM controlled HESS was the first experimentally verified SM controlled battery-supercapacitor HESS presented in the literature.

8.2 Future Work

Possible extensions to the research can be summarized as follows.

1. *Identify the applicability of advanced power allocation methods to the HESS*: The applicability of the advanced power allocation methods such as wavelet transform methods, fuzzy logic and neural network can be studied. A suitable power allocation parameter selection method and energy storage element sizing method have to be developed for the new power allocation methods.

2. *Development of a three-phase direct grid connected battery-supercapacitor HESS*: Three-phase boost inverter topology can be used to implement a direct three-phase grid integrated battery-supercapacitor HESS. The power allocation method design, power allocation parameter selection and energy storage element sizing can be studied for three-phase ESS applications.

3. *Development of a control system to handle grid faults and abnormalities*: The energy storage system has to be disconnected from the grid during grid faults and abnormalities while supporting critical loads. A control system can be studied to ensure a smooth transition between two operating modes.

A.1 Appendix 1

A.1.1 Derivation of equation (4.8)

Using Fig. A.1.1, following equation can be written.

$$P_{sc} = P_{tot} \times \left(\frac{as}{1+as}\right) - 2P_{charge} \tag{A.1.1}$$

Additionally,

$$2P_{charge} = E_{sc,ref} - \left(E_{sc,init} - \frac{P_{sc}}{s}\right) \times 2K_p, Esc \tag{A.1.2}$$

Using (A.1.1) and (A.1.2),

$$P_{sc} = P_{tot}\left(\frac{as}{1+as}\right) - 2K_{p,Esc}\left[E_{sc,ref} - \left(E_sc, init - \frac{P_sc}{s}\right)\right] \tag{A.1.3}$$

The equation can be rearranged as,

$$P_{sc} = \frac{as^2}{as^2 + (1+2aK_{p,Esc})s + 2K_{p,Esc}} P_{tot} - \frac{2K_{p,Esc}s}{(s+2K_{p,Esc})}(E_{sc,ref} - E_{sc,init}) \tag{A.1.4}$$

Since $P_{tot} = \frac{1}{\eta} P_{HESS}$,

$$P_{sc} = \frac{as^2}{as^2 + (1+2aK_{p,Esc})s + 2K_{p,Esc}} \frac{1}{\eta} P_{HESS} - \frac{2K_{p,Esc}s}{(s+2K_{p,Esc})}(E_{sc,ref} - E_{sc,init}) \tag{A.1.5}$$

A.1.2 Derivation of equation (5.15)

The sliding surface for the left hand side supercapacitor connected boost converter leg, S_{sc1} is given by,

$$S_{sc1} = K_{sc1,a}(v_{o1} - v_{o1,ref}) + K_{sc1,b}\int (v_{o1} - v_{o1,ref})dt + K_{sc1,c} i_{Lsc1} \tag{A.1.6}$$

The equivalent control input for the SM controller is obtained by solving,

$$\frac{dS_{sc1}}{dt} = 0 \tag{A.1.7}$$

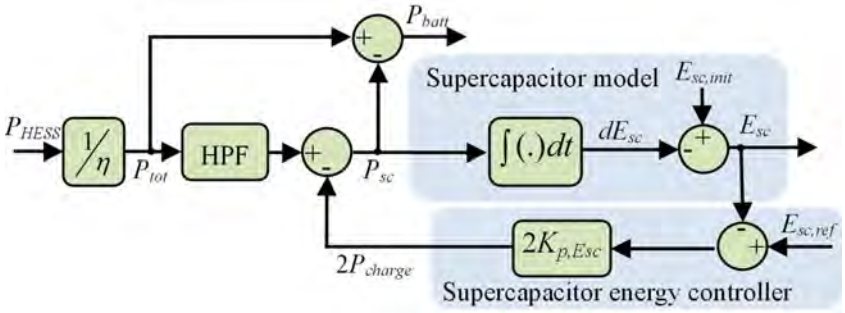

Fig. A.1.1: Simplified block diagram of the HESS power allocation with the SCEC.

Using (A.1.6),

$$K_{sc1,a}\frac{dv_{o1}}{dt} + K_{sc1,b}\left(v_{o1} - v_{o1,ref}\right) + K_{sc1,c}\frac{di_{Lsc1}}{dt} = 0 \tag{A.1.8}$$

Substituting (5.5) and (5.6) in to (A.1.8),

$$K_{sc1,a}\left(\frac{i_{obatt1} - i_{o1} + (1-u_{sc1})i_{Lsc1}}{C_1}\right) + K_{sc1,b}\left(v_{o1} - v_{o1,ref}\right) + K_{sc1,c}\left(\frac{v_{sc} - i_{Lsc1}R_{Lsc1} - (1-u_{sc1})v_{o1}}{L_{sc1}}\right) = 0 \tag{A.1.9}$$

The $(1-u_{sc1})$ value which satisfies (A.1.9) is the equivalent control input $\bar{u}_{sc1,eq}$. Using (A.1.9), the equivalent control input can be obtained as,

$$\bar{u}_{sc1,eq} = \frac{k_{sc1,a}(i_{obatt1} - i_{o1}) + k_{sc1,b}(v_{o1} - v_{o1,ref}) + k_{sc1,c}(v_{sc} - i_{Lsc1}R_{Lsc1})}{k_{sc1,c}v_{o1} - k_{sc1,a}i_{Lsc1}} \tag{A.1.10}$$

where,

$$\begin{cases} k_{sc1,a} = K_{sc1,a}L_{sc1} \\ k_{sc1,b} = K_{sc1,b}L_{sc1}C_1 \\ k_{sc1,c} = K_{sc1,c}C_1 \end{cases}$$

A.1.3 Derivation of equation (5.26)

The sliding surface for the left hand side battery connected boost converter leg, S_{batt1} is given by,

$$S_{batt1} = (i_{Lbatt1} - i_{Lbatt1,ref}) + K_{batt1}\int (i_{Lbatt1} - i_{Lbatt1,ref})dt \tag{A.1.11}$$

The equivalent control input for the SM controller is obtained by solving,

$$\frac{dS_{batt1}}{dt} = 0 \tag{A.1.12}$$

Using (A.1.11),

$$\frac{di_{Lbatt1}}{dt} + K_{batt1}\left(i_{Lbatt1} - i_{Lbatt1,ref}\right) = 0 \tag{A.1.13}$$

Substituting (5.20) in to (A.1.12),

$$\frac{v_{batt} - i_{Lbatt1}R_{Lbatt1} - (1-u_{batt1})\,v_{o1}}{L_batt1} + K_{batt1}\left(i_{Lbatt1} - i_{Lbatt1,ref}\right) = 0 \tag{A.1.14}$$

The $(1-u_{batt1})$ value which satisfies (A.1.14) is the equivalent control input $\bar{u}_{batt1,eq}$. Using (A.1.14), the equivalent control input can be obtained as,

$$\bar{u}_{batt,eq} = \frac{v_{batt} - i_{Lbatt1}R_{Lbatt1} + k_{batt1}(i_{Lbatt1} - i_{Lbatt1,ref})}{v_{o1}} \tag{A.1.15}$$

where

$$k_{batt1} = K_{batt1}L_{batt1}$$

A.1.4 Derivation of equation (5.39)

Using Fig. A.1.2, following equation can be written.

$$\left[-\left(-\frac{(P_{tot}-P_{batt})}{s}+E_{sc,init}\right)+E_{sc,ref}\right]\left(\frac{K_{p,Esc}s+K_{i,Esc}}{s}\right)2v_{batt}=P_{batt} \quad \text{(A.1.16)}$$

Then, (A.1.16) can be re-arranged as

$$P_{batt}=\left(\frac{(2v_{batt}K_{p,Esc})\,s+(2v_{batt}K_{i,Esc})}{s^2+(2v_{batt}K_{p,Esc})\,s+(2v_{batt}K_{i,Esc})}\right)P_{tot} + \left(\frac{(2v_{batt}K_{p,Esc})\,s^2+(2v_{batt}K_{i,Esc})\,s}{s^2+(2v_{batt}K_{p,Esc})\,s+(2v_{batt}K_{i,Esc})}\right)(E_{sc,ref}-E_{sc,init}) \quad \text{(A.1.17)}$$

A.1.5 Derivation of equation (6.40)

Using the boost inverter model, the inductor currents i_{L1} can be written as

$$i_{L1}=\frac{i_1 v_{o1}}{v_{in}-i_{L1}R_{L1}} \quad \text{(A.1.18)}$$

Using (A.1.18) a quadratic equation for i_{L1} can be obtained as

$$R_{L1}i_{L1}^2-v_{in}i_{L1}+v_{o1}i_1=0 \quad \text{(A.1.19)}$$

Then, a solution for i_{L1} is given by

$$i_{L1}=\frac{v_{in}-\sqrt{\left(v_{in}^2-4R_L v_{o1}i_1\right)}}{2R_{L1}} \quad \text{(A.1.20)}$$

Similarly, i_{L2} can be found as

$$i_{L2}=\frac{v_{in}-\sqrt{\left(v_{in}^2-4R_L v_{o2}i_2\right)}}{2R_{L2}} \quad \text{(A.1.21)}$$

Since $i_{in}=i_{L1}+i_{L2}$, the total input current can be obtained as

$$i_{in}=\frac{v_{in}-\sqrt{\left(v_{in}^2-4R_L v_{o1}i_1\right)}}{2R_L}+\frac{v_{in}-\sqrt{\left(v_{in}^2-4R_L v_{o2}i_2\right)}}{2R_L} \quad \text{(A.1.22)}$$

where $R_L=R_{L1}=R_{L2}$.

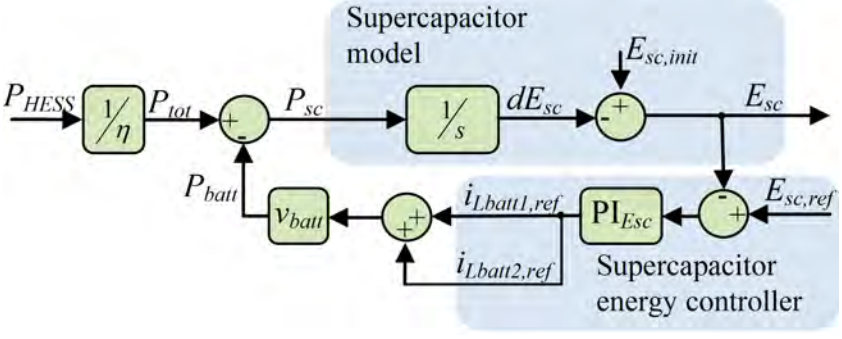

Fig. A.1.2: Simplified block diagram of the HESS power allocation.

A.1.6 Derivation of equation (7.4)

The output capacitor current waveforms i_{C1} and i_{C2} can be written as

$$i_{C1} = C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.23}$$

$$i_{C2} = -C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.24}$$

Then,

$$i_1 = I_o\sin(\omega t + \alpha) + C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.25}$$

Similarly, i_2 can be written as,

$$i_2 = -I_o\sin(\omega t + \alpha) - C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.26}$$

Then, the total input current to the boost inverter can be obtained as,

$$i_{in} = i_1\frac{v_{o1}}{v_{in}} + i_2\frac{v_{o2}}{v_{in}} \tag{A.1.27}$$

Substituting (A.1.25),(A.1.26), (7.1), and (7.2) into (A.1.27),

$$i_{in} = \frac{1}{v_{in}}\left[\frac{V_oI_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t - \theta)\right] \tag{A.1.28}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \frac{C\omega V_o\sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}}$$

and $C = C_1 = C_2$.

A.1.7 Derivation of equation (7.10) and (7.11)

The total input current of the boost inverter can be obtained by

$$i_{in} = i_1\frac{v_{o1}}{v_{in}} + i_2\frac{v_{o2}}{v_{in}} \tag{A.1.29}$$

Substituting (7.6), (7.7), (7.8), and (7.9) in to (A.1.29) and simplifying, the input current can be written as

$$i_{in} = \frac{1}{v_{in}}\left[\frac{V_oI_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t - \theta)\right]$$
$$\frac{1}{v_{in}}\left[-2CKV_{DC}\frac{di_{in,AC}}{dt} + 2CK^2i_{in_AC}\frac{di_{in,AC}}{dt}\right] \tag{A.1.30}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \dfrac{C\omega V_o \sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \dfrac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega\sin(\alpha-\delta)\right]}}$$

It can be observed that the input current waveform contains a DC component and an AC component. Hence $i_{in} = i_{in,AC} + i_{in,DC}$. Considering the AC component of (A.1.30) and simplifying

$$\frac{di_{in,AC}}{dt} = \frac{v_{in}}{(2V_{DC}CK - 2CK^2 i_{in,AC})}(i_{in,AC0} - i_{in,AC}) \tag{A.1.31}$$

where

$$i_{in,AC0} = \frac{V_o}{2v_{in}}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t - \theta) \tag{A.1.32}$$

A.1.8 Derivation of equation (7.24)

Form (7.21),

$$V_{DC} \geq v_{in} + \frac{V_o}{2} + \frac{v_{in}\max(|i_{in,AC0}|)}{4V_{DC}C\omega} \tag{A.1.33}$$

where

$$\max(|i_{in,AC0}|) = \frac{V_o}{2v_{in}}\sqrt{\left[I_{o,max}^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_{o,max}C\omega\right]}. \tag{A.1.34}$$

Then,

$$4V_{DC}^2C\omega \geq 4V_{DC}C\omega\left(v_{in} + \frac{V_o}{2}\right) + v_{in}\max(|i_{in,AC0}|) \tag{A.1.35}$$

$$4V_{DC}^2C\omega - 2C\omega V_{DC}\left(V_o + 2v_{in}\right) - v_{in}\max(|i_{in,AC0}|) \geq 0 \tag{A.1.36}$$

Then the minimum positive value which satisfies (A.1.36) is given by

$$V_{DC,\min} = \frac{2C\omega(V_o+2v_{in}) + \sqrt{[2C\omega(V_o+2v_{in})]^2 + 16C\omega v_{in}\max(|i_{in,AC0}|)}}{8C\omega}. \tag{A.1.37}$$

A.1.9 Derivation of equation (7.29)

The output capacitor current waveforms i_{C1} and i_{C2} can be written as

$$i_{C1} = C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.38}$$

$$i_{C2} = -C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.39}$$

Then,

$$i_1 = I_o\sin(\omega t + \alpha) + C_1\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.40}$$

Similarly, i_2 can be written as,

$$i_2 = -I_o\sin(\omega t + \alpha) - C_2\omega\frac{V_o}{2}\cos(\omega t + \delta) \tag{A.1.41}$$

From (7.28)

$$P_{in,HESS} = P_{o1} + P_{o2} + P_{C1} + P_{C2}. \tag{A.1.42}$$

Hence

$$P_{in,HESS} = v_{o1}i_{o1} + v_{o2}i_{o2} + i_{C1}v_{o1} + i_{C2}v_{o2}. \tag{A.1.43}$$

$$P_{in,HESS} = v_{o1}\left(i_{o1} + i_{C1}\right) + v_{o2}\left(i_{o2} + i_{C2}\right) \tag{A.1.44}$$

Substituting (A.1.40),(A.1.41), (7.1), and (7.2) into (A.1.44),

$$P_{in,HESS} = \left[\frac{V_o I_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t-\theta)\right] \tag{A.1.45}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \frac{C\omega V_o\sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}}$$

and $C = C_1 = C_2$.

A.1.10 Derivation of equation (7.33), (7.34), and (7.35)

The total input power of the HESS can be obtained by

$$P_{in,HESS} = v_{o1}\left(i_{o1} + i_{C1}\right) + v_{o2}\left(i_{o2} + i_{C2}\right) \tag{A.1.46}$$

With the ripple reduction method,

$$i_1 = I_o\sin(\omega t+\alpha) + C\omega\frac{V_o}{2}\cos(\omega t+\delta) - CK\frac{di_{sc,AC}}{dt} \tag{A.1.47}$$

and

$$i_2 = -I_o\sin(\omega t+\alpha) - C\omega\frac{V_o}{2}\cos(\omega t+\delta) - CK\frac{di_{sc,AC}}{dt} \tag{A.1.48}$$

Substituting (A.1.47), (A.1.48), (7.31), and (7.32) in to (A.1.46) and simplifying, the input current can be written as

$$P_{in,HESS} = \left[\frac{V_oI_o}{2}\cos(\alpha-\delta) + \frac{V_o}{2}\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}\cos(2\omega t-\theta)\right] \left[-2CKV_{DC}\frac{di_{sc,AC}}{dt} + 2CK^2i_{sc_AC}\frac{di_{sc,AC}}{dt}\right] \tag{A.1.49}$$

where

$$\cos\theta = \frac{-I_o\cos(\alpha+\delta) + \frac{C\omega V_o\sin(2\delta)}{2}}{\sqrt{\left[I_o^2 + \frac{C^2\omega^2V_o^2}{4} + V_oI_oC\omega\sin(\alpha-\delta)\right]}}$$

It can be observed that the input power contains a DC component and an AC component. Hence, $P_{in,HESS} = P_{in,HESS,AC} + P_{in,HESS,DC}$. Since the AC component of the input power is allocated to the supercapacitor, the AC component of the HESS input power corresponds to the AC component of the power supplied by the supercapacitor.

Considering the AC component of (A.1.49) and simplifying

$$\frac{di_{sc,AC}}{dt} = \frac{v_{in}}{(2V_{DC}CK - 2CK^2 i_{in,AC})}(i_{in,AC0} - i_{in,AC}) \tag{A.1.50}$$

where

$$i_{sc,AC0} = \frac{V_o}{2v_{in}}\sqrt{\left[I_o^2 + \frac{C^2\omega^2 V_o^2}{4} + V_o I_o C\omega \sin(\alpha - \delta)\right]}\cos(2\omega t - \theta) \tag{A.1.51}$$

A.2 Appendix 2

A.2.1 Simulink Models used for DSpace controller implementation

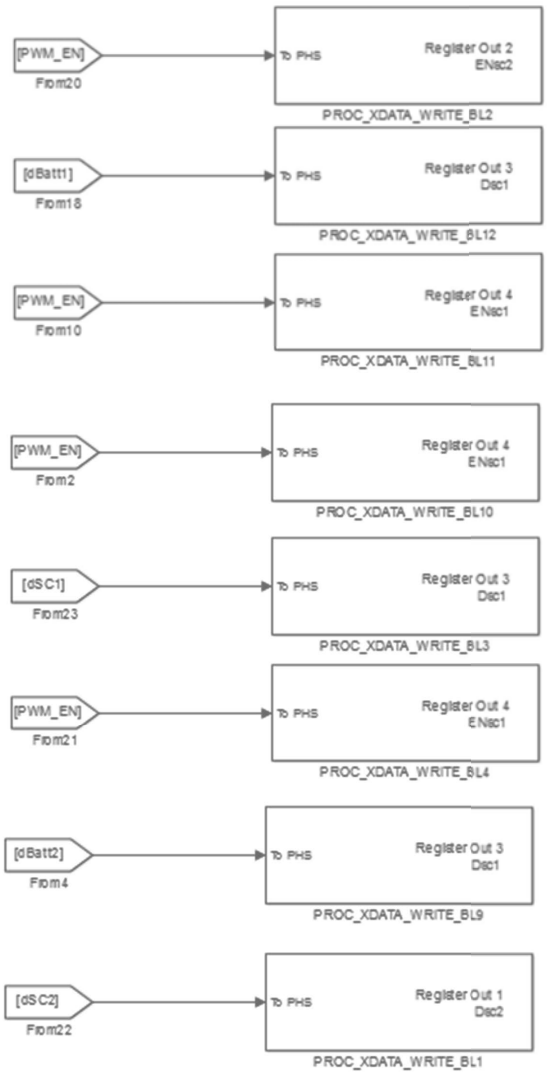

Fig. A.2.1: Simulink blocks: Duty ratio signal output to DSpace system

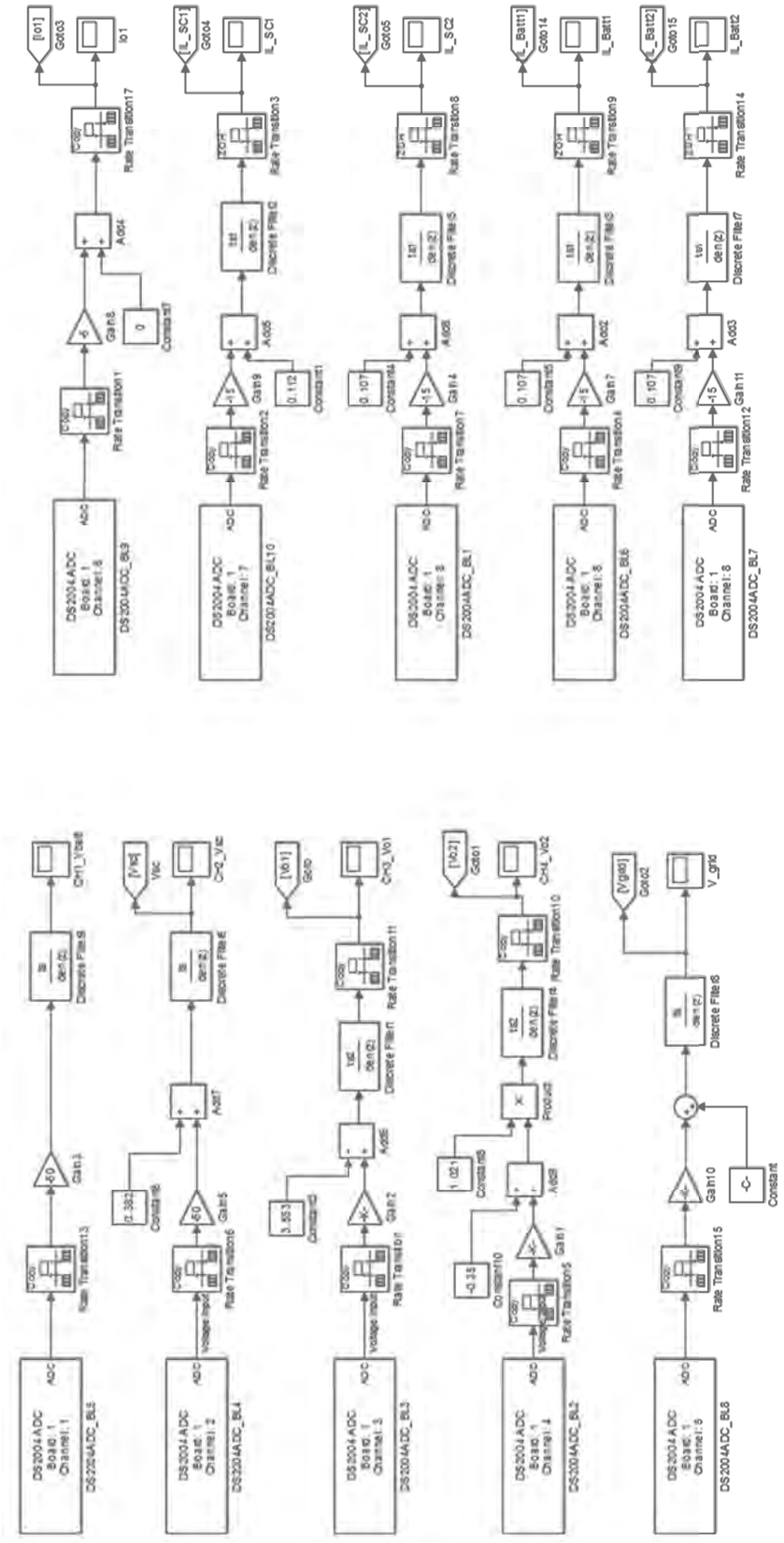

Fig. A.2.2: Simulink blocks: Voltage and current inputs through DSpace analog to digital converter

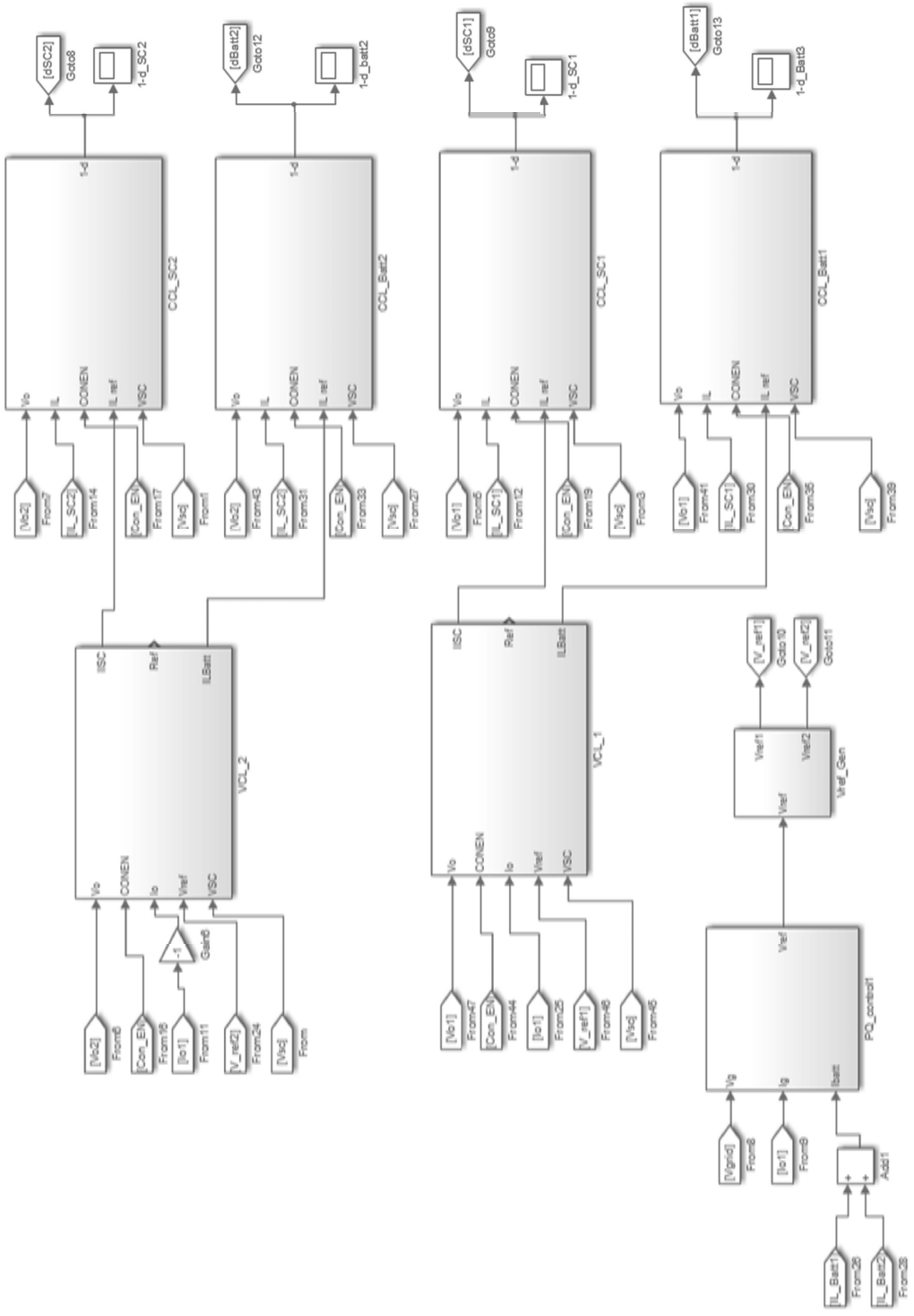

Fig. A.2.3: Simulink blocks: Active and reactive power controller and double loop control system

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