Role of surfaces and dopants in quantum devices and nanowire transistors

Author:
Damon Carrad

Supervisor:
A/Prof Adam Micolich

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

UNSW
AUSTRALIA

School of Physics
Faculty of Science

December 2015

PLEASE TYPE

THE UNIVERSITY OF NEW SOUTH WALES
Thesis/Dissertation Sheet

Surname or Family name: **Carrad**

First name: **Damon** Other name/s: **James**

Abbreviation for degree as given in the University calendar: **PhD**

School: **School of Physics** Faculty: **Faculty of Science**

Title: Role of surfaces and dopants in quantum devices and nanowire transistors

Abstract 350 words maximum: (PLEASE TYPE)

Miniaturisation of electronic devices has driven development of high speed, high density processors and memory elements. This process has required extensive optimisation of semiconductor materials and interfaces as the random nature of doping increasingly affects device performance and the influence of non-ideal surfaces and interfaces need to be counteracted. As Moore's law for silicon may soon reach its limit, there is a desire to harness electrically efficient III-V semiconductor materials in an economically viable way. There is also a desire to utilise new functionalities brought by quantum mechanics, thermoelectrics and organic materials.

This thesis explores the role of p-type AlGaAs/GaAs heterostructures, self-assembled semiconductor nanowires and organic polymer electrolytes in this broad research programme. My research investigated the impact of background potentials generated by doping and surface states for quantum devices. I developed new wrap-gating techniques for InAs semiconductor nanowires towards economically viable arrays of III-V transistors on silicon substrates. This involved both conventional metal/oxide wrap-gates as well as nanoscale patterning of polymer electrolyte films to both improve the compatibility of organics with nanostructures and seek new functionalities for nanowire transistors. I then used polymer electrolytes to both act as an external dopant, and set the background potential for nanowire thermoelectrics. I also developed proof-of-principle complementary n- and p-type proton-to-electron transducers.

Throughout, I highlight the importance of dopants and surfaces. I show how these non-ideal aspects of semiconductor devices affect performance and attempt to find solutions where possible by, e.g., using sulfur-based surface passivation solutions or polymer electrolytes as an external dopant. Using these examples I illustrate that the drive to develop new technologies leads to new physics on both ends. Imperfections in research devices lead to new understanding of material physics, and once these are overcome, the new functionalities embodied by the devices can be used to study new aspects of nature.

FOR OFFICE USE ONLY Date of completion of requirements for Award:

THIS SHEET IS TO BE GLUED TO THE INSIDE FRONT COVER OF THE THESIS

Abstract

Miniaturisation of electronic devices has driven development of high speed, high density processors and memory elements. This process has required extensive optimisation of semiconductor materials and interfaces as the random nature of doping increasingly affects device performance and the influence of non-ideal surfaces and interfaces need to be counteracted. As Moore's law for silicon may soon reach its limit, there is a desire to harness electrically efficient III-V semiconductor materials in an economically viable way. There is also a desire to utilise new functionalities brought by quantum mechanics, thermoelectrics and organic materials.

This thesis explores the role of *p*-type AlGaAs/GaAs heterostructures, self-assembled semiconductor nanowires and organic polymer electrolytes in this broad research programme. My research investigated the impact of background potentials generated by doping and surface states for quantum devices. I developed new wrap-gating techniques for InAs semiconductor nanowires towards economically viable arrays of III-V transistors on silicon substrates. This involved both conventional metal/oxide wrap-gates as well as nanoscale patterning of polymer electrolyte films to both improve the compatibility of organics with nanostructures and seek new functionalities for nanowire transistors. I then used polymer electrolytes to both act as an external dopant, and set the background potential for nanowire thermoelectrics. I also developed proof-of-principle complementary *n*- and *p*-type proton-to-electron transducers.

Throughout, I highlight the importance of dopants and surfaces. I show how these non-ideal aspects of semiconductor devices affect performance and attempt to find solutions where possible by, e.g. using sulfur-based surface passivation solutions or polymer electrolytes as an external dopant. Using these examples I illustrate that the drive to develop new technologies leads to new physics on both ends. Imperfections in research devices lead to new understanding of material physics, and once these are overcome, the new functionalities embodied by the devices can be used to study new aspects of nature.

ORIGINALITY STATEMENT

'I hereby declare that this submission is my own work and to the best of my knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at UNSW or any other educational institution, except where due acknowledgement is made in the thesis. Any contribution made to the research by others, with whom I have worked at UNSW or elsewhere, is explicitly acknowledged in the thesis. I also declare that the intellectual content of this thesis is the product of my own work, except to the extent that assistance from others in the project's design and conception or in style, presentation and linguistic expression is acknowledged.'

Signed .....

Date 17/12/2015

Acknowledgements

The results in this thesis would not have been possible without the work of so many people. It's been a privilege to work with passionate scientists with a strong desire to collaborate, help and contribute.

First and foremost a huge debt of gratitude is owed to Adam Micolich. He has been an amazing supervisor, and has consistently gone above and beyond in ensuring that we have been able to produce the best science we possibly could. None of this thesis would have been possible without his vision and support. I am also hugely grateful for the opportunities to travel around Australia and the world to collect data and present at conferences. It has also been a pleasure to have someone as a supervisor who is just a straight up good guy, with a faultlessly excellent taste in beer.

Secondly, I must thank Adam Burke, who was my partner in crime for the vast majority of research that went into this thesis. He taught me everything about device fabrication and electrical measurements, and his patience and skill in explaining everything made the whole process smooth and easy. I couldn't have asked for a better person to work with, and I really hope we do more together throughout our careers.

I would also like to thank the other members Nanoelectronics Group members, Jan Gluschke, Rifat Ullah and Roman Lyttleton. Each contributed a lot to this thesis, either directly with fabrication and experiments or indirectly with helping to run a good lab. Massive thanks also to Jan for proof-reading this thesis. I'd also like to thank Jack Cochrane for the excellent job he does in maintaining everything in the labs, and sincerely hope he's able to keep doing so for a while yet.

Thanks are also due to my collaborators and co-authors. First of all, to Peter Reece for being my co-supervisor, doing/helping with the PL measurements and having some good discussions about them with me, and for always sharing a joke. Thanks also to Oleh Klochan, Andrew See and Alex Hamilton from the QED group for helping out with the dilution fridge and the many other helpful discussions over the years, along with Karina, Sarah, Daisy, LaReine, Ashwin, Roy and Jason. I must extend a massive amount of appreciation to Bernard Mostert and Paul Meredith at the University of Queensland for hosting me twice, and to Bernard in particular for working with me non-stop to collect (and understand!)

so much good data. I am really grateful for the experience. I also thank Heiner Linke and Sofia Fahlvik Svensson for bringing us a really interesting experiment to work on, and to Martin Leijnse for providing the great insight into the meaning of the results. Thanks also to Heiner for hosting me in Lund, Sweden, along with Sofia, Kristian and Gustav, and to Mercy, Cassie, Jan and all the other Lund folk for making it an enjoyable stay. I also must acknowledge Kristian, Gustav and Sofia as well as Hannah Joyce, Hark Hoe Tan and Chennupati Jagadish from ANU for supplying us with the nanowires our devices were based on. Thanks also are extended to Andreas Wieck and his group for growing and supplying the AlGaAs/GaAs wafers. I thank Helen Rutlidge and Bill Bin Gong for performing the ICPMS and XPS contained in this thesis, and Tim Bray and Craig Johnson for assistance with the PL. Finally, I'd like to extend appreciation to the ANFF staff, past and present, for all the assistance in the cleanrooms.

I would also like to thank the Australian Nanotechnology Network for funding some of my travels and everything that they do to contribute to the community in Australia, including putting on excellent conferences and providing opportunities to young researchers. I also thank the Graduate Research School at UNSW for the funding that enabled me to visit Lund and Austin.

More personally, I would like to thank Pat McMillan. The experience in third year lab was a very important step into the research world and contributed a huge amount to my philosophy on how to do science, how to understand science, and also how to teach it. I will also be eternally grateful to Anthony Mills, without whom I never would have done physics in the first place.

I'd like to also thank Tim, Tim, Alex, Alex, Chidge, Ana, Kellie, Ahmad and everyone else in my undergrad cohort for helping me stick with it by somehow making uni fun. Thanks in particular to Ana for tipping me off about this LaTeX template and being a cool housemate. And thanks also to all my friends and everyone in the musical sphere (esp. Shelby, a strong component of both) for keeping me sane and making Sydney a worthwhile place to throw away money on rent.

I have an endless amount of gratitude and thanks for my parents and sister for their constant support in every way and providing an example that I know I'm lucky to have, and to dad for proofing this thesis too.

And finally, I need to express something that goes beyond ‘thanks’ and gratitude to Leila for simply being my love and all that brings to me, and for the life we are building together.

Publications arising from this work

Refereed Journal Publications

1. D. J. Carrad, A. M. Burke, P. J. Reece, R. W. Lyttleton, D. E. J. Waddington, A. Rai, D. Reuter, A. D.Wieck & A. P. Micolich. 'The effect of $(NH_4)_2S_x$ passivation on the (311)A GaAs surface and its use in AlGaAs/GaAs heterostructure devices.' *Journal of Physics: Condensed Matter* **25**, p. 325304 (2013)

   My contribution: I worked closely with Dr Adam Burke on the fabrication and measurement of the electrical devices. I prepared samples for the photoluminescence and X-ray photoelectron spectroscopy and performed some of the photoluminescence measurements. I analysed the data and wrote the paper with A/Prof Adam Micolich. This paper is discussed in Chapter 3.

2. D. J. Carrad, A. M. Burke, O. Klochan, A. M. See, A. R. Hamilton, A. Rai, D. Reuter, A. D. Wieck & A. P. Micolich. 'Determining the stability and activation energy of Si acceptors in AlGaAs using quantum interference in an open hole quantum dot.' *Physical Review B* **89**, p. 155313 (2014)

   My contribution: I fabricated and measured the electrical properties of the etched open hole quantum dot with Dr Adam Burke. I analysed the data and wrote the paper with A/Prof Adam Micolich. This paper is discussed in Chapter 3.

3. D. J. Carrad, A. M. Burke, R. W. Lyttleton, H. J. Joyce, H. H. Tan, C. Jagadish, K. Storm, H. Linke, L. Samuelson & A. P. Micolich. 'Electron-Beam Patterning of Polymer Electrolyte Films To Make Multiple Nanoscale Gates for Nanowire Transistors.' *Nano Letters* **14**, pp. 94–100 (2014)

   My contribution: I developed the electron-beam patterning process, fabricated devices and conducted electrical measurements with the help of Dr Adam Burke and Roman Lyttleton. I analysed the data and wrote the paper with A/Prof Micolich. This paper is discussed in Chapter 4.

4. A. M. Burke, D. J. Carrad, J. G. Gluschke, K. Storm, S. Fahlvik Svensson, H. Linke, L. Samuelson & A. P. Micolich. 'InAs Nanowire Transistors with Multiple, Independent Wrap-Gate Segments.' *Nano Letters* **15**, pp. 2836–2843 (2015)

   My contribution: I assisted Dr Adam Burke and A/Prof Adam Micolich in developing the process for fabricating multiple-wrap gated devices. I also assisted with electrical measurements and development of the logic programs used to evaluate wrap-gate electrical balance. This paper is discussed in Chapter 4.

5. S. Fahlvik Svensson, A. M. Burke, D. J. Carrad, M. Leijnse, H. Linke & A. P. Micolich. 'Using Polymer Electrolyte Gates to set-and-freeze Threshold Voltage and Local Potential in Nanowire-based Devices and Thermoelectrics.' *Advanced Functional Materials* **25**, pp. 255–262 (2015)

   My contribution: This work was highly collaborative. I worked with Sofia Fahlvik Svensson to fabricate the device. Sofia, Dr Adam Burke and myself worked together to obtain the electrical measurements. All authors contributed to the interpretation of the data. Sofia, A/Prof Adam Micolich and myself wrote the paper. This paper is discussed in Chapter 5.

6. D. J. Carrad, A. B. Mostert, A. R. Ullah, A. M. Burke, H. J. Joyce, H. H. Tan, C. Jagadish, P. Meredith & A. P. Micolich. 'n- and p-type proton-to-electron transducers based on III-V nanowires' *Manuscript in preparation*

   My contribution: I fabricated devices with help from Rifat Ullah and Dr Adam Burke. I worked closely with Dr Bernard Mostert to obtain the electrical measurements. I am in the process of writing this paper with Bernard and A/Prof Adam Micolich. This paper is discussed in Chapter 6.

Refereed Conference Proceedings

1. D. Carrad, A. Burke, S. Fahlvik Svensson, R. Lyttleton, H. Joyce, H. H. Tan, C. Jagadish, K. Storm, L. Samuelson, H. Linke & A. Micolich. 'Nanoscale polymer electrolytes: Fabrication and applications using nanowire transistors.' In: *2014 Conference on Optoelectronic and Microelectronic Materials Devices (COMMAD)*, pp. 286–289 (2014)

   This presentation was based on the results collected for publications 3 and 6 above.

Contents

Abbreviations

2DEG	**2**-**d**imensional **e**lectron **g**as
2DHG	**2**-**d**imensional **h**ole **g**as
AFM	**A**tomic **f**orce **m**icroscope/microscopy
ALD	**A**tomic **l**ayer **d**eposition
CB	**C**onduction **b**and
CMOS	**C**omplementary **m**etal-**o**xide-**s**emiconductor
DSO	**D**igital **s**ignal **o**scilloscope
EBL	**E**lectron **b**eam **l**ithography
EDL	**E**lectric **d**ouble **l**ayer
FET	**F**ield-**e**ffect **t**ransistor
HEMT	**H**igh **e**lectron **m**obility **t**ransistor
HHMT	**H**igh **h**ole **m**obility **t**ransistor
LIA	**L**ock-**i**n **a**mplifier
MCF	**M**agneto**c**onductance **f**luctuations
MOSFET	**M**etal-**o**xide-**s**emiconductor **f**ield-**e**ffect **t**ransistor
NMP	**N**-**m**ethyl-2-**p**yrrolidone
NW	**N**ano**w**ire
NWFET	**N**ano**w**ire **f**ield-**e**ffect **t**ransistor
PE	**P**olymer **e**lectrolyte
PEO	**P**oly(**e**thylene **o**xide)
PL	**P**hoto**l**uminescence
PMMA	**P**oly(**m**ethyl **m**eth**a**crylate)
QD	**Q**uantum **d**ot

QPC	**Q**uantum **p**oint **c**ontact
SDBS	**S**ource-**d**rain **b**ias **s**pectroscopy
SEM	**S**canning **e**lectron **m**icroscope
SMU	**S**ource **m**easure **u**nit
VB	**V**alence **B**and
XPS	**X**-ray **p**hotoelectron **s**pectroscopy

Physical Constants

Boltzmann constant	k_B	=	1.381×10^{-23} J/K, 8.617×10^{-5} eV/K
Conductance quantum	G_Q	=	$\frac{2e^2}{h}$
Electron charge	e	=	1.602×10^{-19} C
Permittivity of free space	ϵ_0	=	$8.854 \times 10^{-12} \frac{s^4 A^2}{m^3 kg}$
Planck constant	h	=	6.626×10^{-34} m^2kg/s
Speed of Light	c	=	$2.997\ 924\ 58 \times 10^8$ ms^{-S} (exact)

Symbols

B	Magnetic field	tesla [T]
C	Capacitance	farads [F]
C_{dot}	Quantum dot capacitance	farads [F]
C_G	Gate capacitance	farads [F]
$D_S(E)$	Density of states at the surface	number of states per square centimetre per eV [cm^{-2} eV^{-1}]
ΔE_a	Quantum dot addition energy	electron volts [eV]
E_A, E_D, E_T	Acceptor/donor/trap depth	electron volts [eV]
E_C, E_V	Conduction, Valence band energy	electron volts [eV]
E_F	Fermi energy	electron volts [eV]
$E_g = E_C - E_V$	Band-gap energy	electron volts [eV]
f	electrical frequency	hertz [Hz]
I_d	drain current	ampere [A]
I_G	gate leakage current	ampere [A]
I_{on}, I_{off}	transistor on/off current	ampere [A]
G	conductance	siemens [S]
ℓ	mean free path	metres [m]
n, p	electron/hole concentration	number per cubic centimetre (3D) or square centimetre (2D) [cm^{-3}] or [cm^{-2}]
P	pressure	mbar
q	charge	coulombs [C]
R	resistance	ohms [Ω]

S	Seebeck coefficient	volts per kelvin [V/K]
SS	subthreshold swing	millivolts per decade [mV/dec]
T	temperature	kelvin [K]
V_G or V_g	gate voltage	volts [V]
$V_{in}, V_{out}, V_{supply}$	circuit input/output/supply voltage	volts [V]
V_{sd}	source-drain voltage	volts [V]
V_{th}	threshold voltage	volts [V]
V_T	thermovoltage	volts [V]
V_{PE}	voltage at the PE/NW interface	volts [V]
V_{po}	pinch-off voltage	volts [V]
ϵ_r	dielectric constant/ relative permittivity	unitless
κ	thermal conductivity	watts per metre kelvin [W/(m·K)]
λ_F	Fermi wavelength	nanometre [nm]
μ	charge carrier mobility	centimetre squared per volt second [cm^2/Vs]
ν	optical frequency	hertz [Hz]
ϱ	nanowire radius	nanometre [nm]
σ	conductivity	siemens per centimetre [S/cm]
τ	time constant	Seconds [s]

Chapter 1

Introduction and background

1.1 Introduction and chapter outline

The simple concept of the field-effect transistor has had a profound impact on scientific and industrial progress over the last half century through the proliferation of novel devices based on it.[1–9] The underlying field-effect principle is that the flow of electrons through a semiconductor is controlled electrostatically by a gate electrode. From the initial deployment of transistors in amplifiers and then on into switching in computers, the idea of electric fields controlling charge carrier density and tailoring the underlying band-structure has led to the engineering and control of quantum systems,[5–7] and the interfacing of manufactured electronics with biological systems.[10,11] In the meantime, the drive for more efficient technology has driven the size of devices to decrease well beyond many predicted physical limits, with Moore's law driving the exponential decrease in transistor size for five decades. Despite this, there is growing concern that the 7 nm long transistors in development at Intel are finally exposing the limits of silicon as the basis for transistors in integrated circuits. To increase energy efficiency further we need to seek out materials with better performance than silicon, or devices with increased functionality.[4,12]

At the level of fundamental research, substituting new materials and expanding functionality is seldom trivial. The discovery of non-ideal materials properties raises scientific questions that must be solved to fully exploit the new potential advantages. In particular, two chief problems arising as a result of reduction in device size involve dopant impurities and the proximity of the surface to the channel. Size reduction entails a decreasing number of dopant impurities within devices, meaning that non-homogeneous distributions and/or fluctuations in occupation increasingly affect the dynamics of the channel.[13–15] Countering this has involved efforts towards understanding dopant properties and developing strategies to altogether remove dopant impurities.[16–20] Secondly, the increase in surface/volume ratio with size reduction means surfaces increasingly affect device performance.[4,21] The disruption of the ordered crystal structure at surfaces and material interfaces makes them notoriously problematic, with roughness and long-lived charge traps causing mobility reduction and device instability,[4,22–26] along with issues obtaining ideal electrical behaviour of semiconductor/metal interfaces.[27] Once the problems are solved and new functionalities are realised, these devices can be turned back around to study nature, either by embodying a unique system or providing a different way of probing external systems.

My thesis covers this broad spectrum. At one end, we investigated the use of III-V semiconductor materials as the basis for novel transistor devices, including semiconductor nanowires,[28–31] and high-mobility planar heterostructure devices.[32,33] We studied non-ideal behaviours in these systems, including surface/interface charge traps and doping impurities and attempted to develop solutions for them. We also employed new techniques to observe and study these effects. In terms of adding functionality to devices, we explored the manufacture of hybrid organic/inorganic transistors, featuring semiconductor nanowire channels with polymer electrolyte gate dielectrics. This involved characterising the performance advantages of using polymer electrolyte dielectrics, and used them as the basis of an 'external doping' technique to provide a base-line charge carrier density without the need for dopant impurities. The dielectrics could generate quantum systems and also enhance their study at low temperatures in nanowire devices. In addition, we

evaluated the thermoelectric properties of these devices, where the ultimate functional goal is conversion of waste heat into electrical energy, or efficiently cooling devices to cryogenic temperatures. Finally, the organic gate allowed us to develop complementary n- and p-type proton-to-electron transducers. These could be used to convert the proton signals typically seen in biological systems into electronic signals that can be read out by conventional electronics.

Chapter 1 gives the background behind my results. I start with the principles of operation of the field-effect transistor (FET), which forms the basis for almost all of the devices studied in this thesis. I then discuss the quantum physics of low-dimensional electron systems and how they can be addressed and controlled through field-effect methods. I discuss novel alternative methods for fabricating transistor elements including self-assembled semiconductor nanowires and polymer electrolyte gates. I also outline the non-ideal behaviours in research level devices that we seek to optimise, and explore the concept of biological interfacing.

Chapter 2 outlines the experimental procedures used in this thesis. This includes device fabrication and electrical measurement techniques at room temperature and low temperature, $T \leq 4.2$ K.

Chapter 3 presents results on the cause of instability in p-type GaAs/AlGaAs heterostructures. High electron mobility n-type GaAs/AlGaAs heterostructures have formed the basis for a wealth of low dimensional quantum systems, but making the same kind of systems with holes in p-type heterostructures has been inhibited by gate instability. We explored the effect of surface states and dopant impurity charge migration on the operation of devices made from these structures. We attempted passivation of the (311)-oriented surface used for p-type heterostructures, and found why typical treatments were not as effective as for the more common (100)-oriented surface. We also fabricated a hole quantum dot in this material and used the unique signature of conductance fluctuations in response to an external magnetic field to capture a 'fingerprint' of changes in dopant impurity distributions.

Chapter 4 focusses on novel techniques for gating self-assembled semiconductor nanowires. The results centre on gates that wrap around the nanowire to give the best control. We fabricated devices with multiple gates, using both traditional metal/oxide structures as well as polymer electrolyte gate dielectrics. In the latter case we developed a method to nanoscale pattern poly(ethylene oxide)-based polymer electrolytes and showed this organic/inorganic combination enhanced the functionality of both materials systems.

Chapter 5 explores the use of polymer electrolyte gates to enhance quantum systems in nanowires. The polymer electrolyte gates were used to 'set and freeze' the base-line charge density and the background potential for electrons traversing the nanowire at $T \leq 4.2$ K. To help probe this system we used thermoelectric measurements, which can give additional information to complement traditional conductance measurements. In doing so we also showed that polymer electrolytes could play a vital role in thermoelectric cooling applications that require a specific charge density be set.

Chapter 6 explores the use nanoscale poly(ethylene oxide) dielectrics to facilitate proof-of-principle measurements for integrating nanowires with nano-biology. We discovered that these dielectrics supported proton transport and characterised the proton dynamics as a function of hydration level using nanowire transistors. This revealed a relatively high conductivity for protons in poly(ethylene oxide). The importance is that signalling in many biological systems occurs *via* proton transport rather than electron transport. As a result, interfacing manufactured electronics with the biological world requires transduction of these proton signals into electrical signals. Using n-InAs and p-GaAs nanowire channels, we fabricated complementary nanowire transistors gated by the field-effect arising from local proton concentration. The result was that a change in current caused by proton concentration fluctuations could be read out electronically. Pairing n-InAs and p-GaAs nanowires devices in functional circuits may open the possibility for size appropriate amplifiers of biological signals on chips compatible with Si-based microelectronics.

Chapter 7 rounds out my thesis by summarising the key results and suggesting future directions. Using the examples from this thesis I show that the scientific study of device physics sits neatly between the motivations of understanding constituent material properties and the desire to generate novel devices that facilitate new understandings of physical systems from quantum to biological.

1.2 The field-effect transistor

The field-effect transistor (FET) consists of a semiconductor channel, usually doped n- or p-type, and three metal electrodes (see Fig. 1.1(a)). Device behaviour is determined by the different effect that voltages on these electrodes have on the bands and Fermi level within the semiconductor. The source and drain are electrically connected to the channel. Ideally the contacts are 'ohmic' – i.e. obey Ohm's law $V = RI$ – with a low resistance such that the source/drain voltage V_{sd} drops mostly across the semiconductor channel (Fig. 1.1(b)). The contact between metals and semiconductors typically results in a potential barrier known as a Schottky barrier. This can be overcome by including a dopant in the contact metal and diffusing it into the semiconductor to form a thin, highly doped layer below the contact. The gate electrode is electrically insulated from the semiconductor; when an oxide layer is used, these devices are known as metal-oxide-semiconductor FETs (MOSFETs). Applying a voltage V_G to the gate capacitively depletes or induces charge carriers in the conduction channel. In energetic terms, V_G and the associated electric field alter the energy of the conduction and valence bands with respect to the Fermi level E_F, illustrated in Fig. 1.1(c). To pass a current I_d through the channel, V_{sd} is applied between source and drain to drive the device out of equilibrium, as in Fig. 1.1(d). In this way, the combination of V_{sd} and V_G determines the potential landscape for electrons/holes traversing the semiconductor channel, e.g. Fig. 1.1(e) illustrates how the gate is used to generate a potential barrier that stops the flow of current.

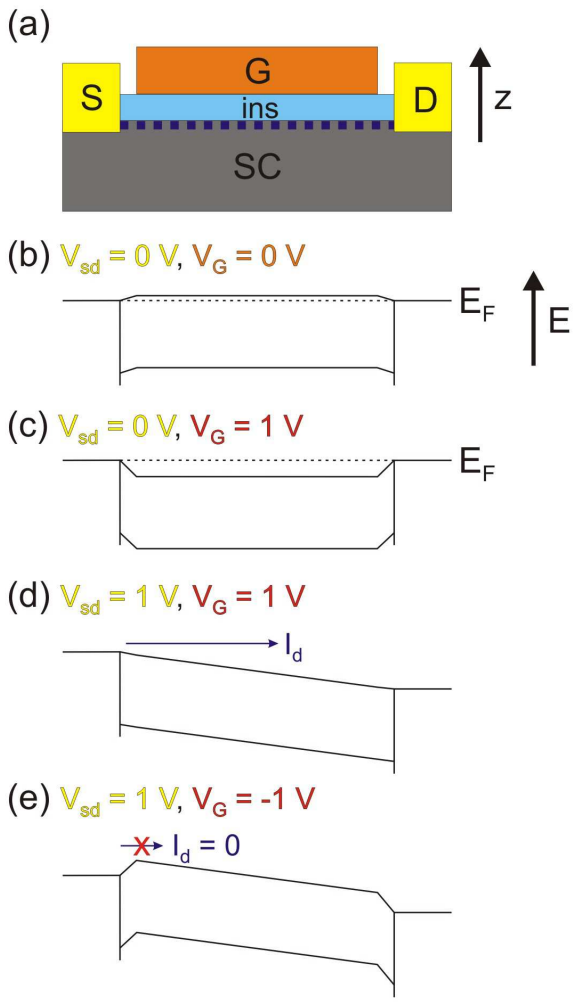

FIGURE 1.1: (a) Schematic of a field-effect transistor featuring metallic source (S), drain (D) and gate (G) electrodes along with the semiconductor channel (SC) and gate insulator (ins). The conduction channel is illustrated with the purple dotted line. (b) Band diagram of the device in (a) for $V_{sd} = V_G = 0$ V. The source and drain have formed ohmic contacts with the semiconductor as the conduction band is aligned with the Fermi level E_F at S and D. (c) Positive applied V_G moves the position of the bands relative to E_F, increasing electron density. (d) An applied V_{sd} allows current I_d to flow through the device. (e) I_d is turned off by a negative V_G, as it causes a potential barrier for electrons.

Figure 1.2 shows the idealised I_d response to V_G applied to n- and p-type transistors at different V_{sd}. These plots are known as 'transfer characteristics'. More positive/negative V_G increases/depletes the electron/hole density, increasing/decreasing channel conduction; the device is said to be 'on'. Supplying a larger V_{sd} results in increased I_d for each V_G. Reversing the V_G direction depletes carriers.

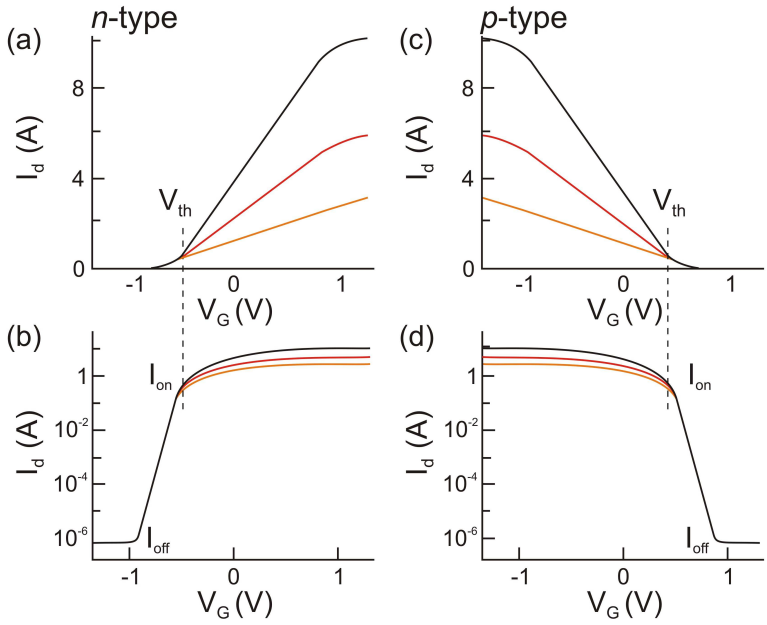

FIGURE 1.2: Transfer characteristics for n- and p-type transistors (a/b and c/d respectively) with linear and log I_d axes (top and bottom). The black, red and orange traces represent decreasing, constant V_{sd}. Below V_{th}, I_d drops exponentially from I_{on} to I_{off}.

At the threshold voltage V_{th} the band diagram looks like Fig. 1.1(e), where a potential barrier blocks transport. Here, V_{sd} has no effect on I_d as the barrier height depends only on V_G. The current through the device goes to zero exponentially with V_G, turning off the device. The exponential turn-off in the subthreshold region can be seen more easily on a log-linear plot (Figs 1.2(b/d)), where $\log(I_d)$ vs. V_G has a linear slope. The inverse subthreshold slope is called the subthreshold swing $SS \equiv \frac{\partial V_G}{\partial log(I_d)}$, given in mV of V_G per decade change of I_d, i.e. mV/dec. It is an important metric as it quantifies the V_G swing required to turn the device off; a low SS is vital for low power applications. The value is determined by material parameters and energy considerations, and is thermodynamically limited to around 60 mV/dec at room temperature.[1] A good transistor combines a low SS with a high on/off ratio, $\frac{I_{on}}{I_{off}}$. This results in orders of magnitude changes in device resistance within a 1 V range of V_G. The next section discusses the importance of these features for switching and amplification.

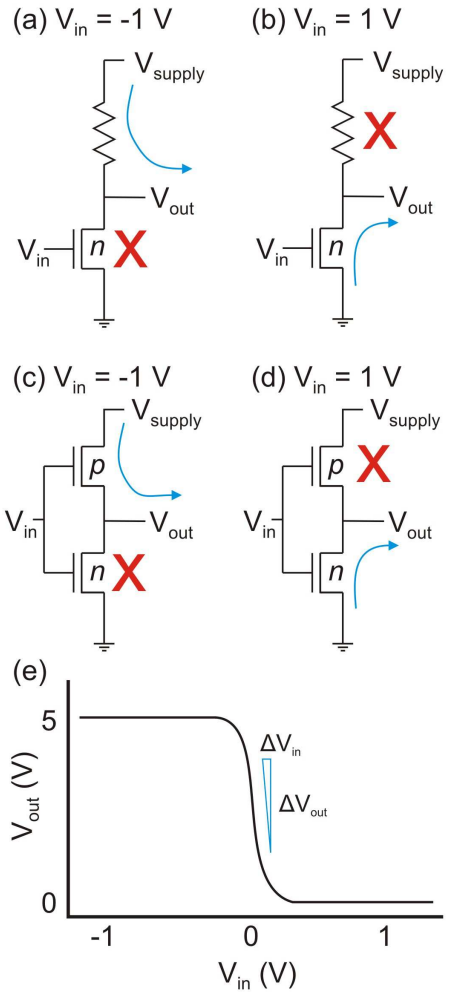

FIGURE 1.3: (a/b) An nMOS inverter circuit with n-type transistor and series resistor. (a) For $V_{in} = -1$ V, the transistor is off, and $V_{out} = V_{supply}$. (b) For $V_{in} = 1$ V, the transistor is on, making $V_{out} = 0$ V. (c/d) a CMOS inverter with p- and n-type transistors. The V_{in} swing between -1 and 1 V takes the p-type/n-type devices from off/on to on/off, respectively. (e) V_{out} vs. V_{in} for a well matched CMOS inverter. The steep slope around $V_{in} = 0$ V facilitates small signal amplification with high gain $\Delta V_{out}/\Delta V_{in}$.

1.2.1 Basic applications: switching and amplification

Two examples of an inverter are shown in Fig. 1.3. This is the most basic circuit for transistor switching and amplification. In the first example (Figs 1.3(a/b)), a resistor is placed in series with the n-transistor channel, and $V_{supply} = 5$ V is applied across the resistor and channel. A signal V_{in} is applied to the gate, and the response V_{out} is read out between the resistor and transistor source. Typical transistor ON and OFF resistances R_T are in the kΩ and GΩ ranges, respectively.

The resistor value R_R is chosen to be between the ON and OFF resistances, e.g., $R_R = 1$ MΩ. For $V_{in} = -1$ V, the transistor is off, and since $R_R \ll R_T$ by orders of magnitude, the V_{out} is linked to the $V_{supply} = 5$ V. When the input is reversed to $V_{in} = 1$ V, $R_R \gg R_T$; this essentially grounds $V_{out} = 0$ V through the open transistor channel. In this way, switching V_{in} between two voltages switches V_{out} also. In addition, the 2 V signal (from -1 to $+1$ V) at V_{in} is amplified to a 5 V signal at V_{out}. The fact that a high V_{in} gave a low V_{out} and vice versa is the origin of the term 'inverter'.

Inverter performance is improved by using complementary n-type and p-type MOSFETs in the configuration of Figs 1.3(c/d). This is the cornerstone of the complementary MOS (CMOS) platform that is the basis for computer processor technology. A CMOS inverter simply replaces the resistor from the circuit in Figs 1.3(a/b) with a p-type transistor, and V_{in} is applied to both gates simultaneously. Here, $V_{in} = -1$ V turns the p-transistor on and the n-transistor off, giving $V_{out} = 5$ V. Similarly, $V_{in} = 1$ V turns the p-transistor off and the n-transistor on, giving $V_{out} = 0$ V. High amplification gain is achieved by applying small signals around the point where V_{in} swings V_{out} between V_{supply} and ground. Figure 1.3(e) shows that at this point very small changes in V_{in} result in large changes in V_{out}; the origin of the voltage gain.

The switching action of inverters also gives a practical realisation of the NOT logic operation, since high voltages (logic state 1) on the input map to low voltages (logic state 0) on the output and vice versa. CMOS is used in computer processor technology due to its low power consumption: when $V_{in} = \pm$ 1 V, one or the other of the transistor channels is closed and no current flows through the circuit. This means power is only consumed very briefly during switching events.[2] More complex CMOS configurations yield practical realisations of logic operations such as AND and OR. However, demonstration of an inverter is typically at the edge of fundamental research as it serves as a proof-of-principle for a new potential CMOS platform. Scaling up the platform and optimising integrated circuits is mostly an engineering problem from that point onwards.

1.3 Non-ideal properties of real devices

The band structure of solid state materials arises from the regularity of atomic placement in a crystal lattice: the overlapping atomic orbitals hybridise to form energy bands that span the entire crystal.[34] While modern growth techniques such as molecular beam epitaxy have allowed manufacture of near perfect crystals with atomic precision,[35] the majority of materials contain imperfections and impurities. Indeed, the doping of semiconductors entails intentionally introducing impurities. Further, the crystal structure necessarily breaks down dramatically at the surface, or at interfaces with other materials.[34] Below I will briefly discuss how these defects can be understood as localised perturbations against the backdrop of the non-localised bands, and how the down-sizing of devices places increased importance on the distribution of dopant atoms and the effects of surfaces.

1.3.1 Doping and bulk impurities

The most familiar microscopic modification to a band structure arises from doping impurities. A comparatively low concentration of atoms with one more or less proton than that of the host crystal is introduced.[34] Figure 1.4 illustrates how the atomic orbitals of the dopant atoms do not overlap like those of the host crystal. Hence they do not form a continuous band; rather their energy levels remain localised at the physical location of each dopant. For higher proton number Z, the attraction to the nucleus is stronger, giving more tightly bound atomic energy levels. This means that for, e.g., P in Si (Z = 29 and 28 respectively), isolated energy levels containing an electron sit just below the conduction band. If the difference in energy between the dopant level and conduction band is small compared to the thermal energy k_BT, the electrons will populate the conduction band and leave behind ionised dopant impurities. Similarly, the energy levels of Al are shifted slightly higher than Si, providing a localised empty energy state above the valence band. This traps electrons and leaves a non-localised hole in the valence band.

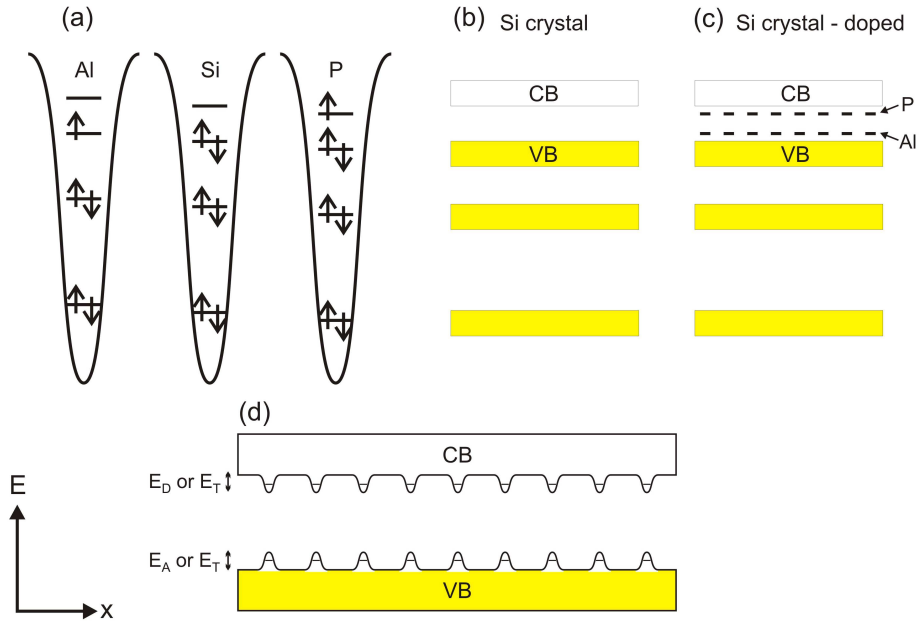

FIGURE 1.4: (a) Energy spectrum for isolated aluminium, silicon and phosphorous atoms. Increasing Z results in an additional electron (represented by spin arrows), and also generates a stronger attractive force, pulling energy levels down. (b) Hybridisation of discrete atomic orbitals leads to the formation of bands. In semiconductors, the bands are occupied until the top of the valence band (VB), leaving and empty conduction band (CB). A small density of Al or P impurities in the Si crystal act as if they are isolated atoms with discrete energy levels. (d) Impurity incorporation modifies the bands to add potential wells for electrons in the CB and holes in the VB. The wells can act as charge traps if the donor/acceptor/trap depth exceeds thermal energy, $E_D, E_A, E_T > k_B T$.

The incorporation of unintentional impurities is conceptually no different; the result is localised discrete energy levels dispersed throughout the crystal. Both unintentional and intentional impurities can possess undesirable features that contribute negatively to device performance. Since they provide potential wells just below/above the conduction/valence bands (Fig. 1.4(d)), impurities can act as electron/hole traps if the well depth E_T is large compared to $k_B T$. Here, a free electron trapped in the deep well is unable to escape due to insufficient thermal energy. If the trap depth $E_T \sim k_B T$, the charge state of the impurity may fluctuate between positive (unoccupied) and neutral (occupied) as electrons enter and leave the trap spontaneously. In larger devices the effect of many impurities rapidly switching charge state may be averaged out and not affect operation. By contrast, nm-scale devices often exist on the scale of the potential generated by the

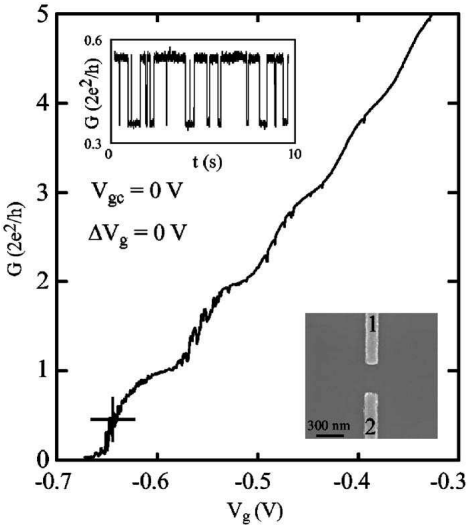

FIGURE 1.5: Data from an experiment by Pioro-Ladrière *et al.*[15] The main figure shows conductance $G = \frac{I_d}{V_{sd}}$ vs. gate voltage V_g for the device shown in the lower inset. The device consists of split surface gates that generate a 1D quantum system in an underlying AlGaAs/GaAs heterostructure as described in Section 1.4.2. The data is noisy due to a two-level switching behaviour arising as a result of changing occupation of nearby Si dopant impurities. Upper inset: The two-level switching is clearly seen if the device is held at constant $V_g \sim -0.64$ V, marked with a cross in the main figure.

impurity.[13,14,36] Such devices can be greatly affected if this potential switches between charge states. For instance, the current through a sensitive quantum device in Fig. 1.5 switches between two states as a nearby single impurity charges and discharges.[15,37] The importance of impurity configuration in setting a background potential for quantum devices is only now being fully appreciated; I will discuss this in Section 1.4.4 and present results from a device where background impurities dominate device behaviour in Chapter 3.

1.3.2 Surface states and interface states

The most dramatic rupture of the crystal structure comes at the surface. The ordered lattice structure is abruptly terminated, leaving surface atoms with unsatisfied dangling bonds, as in Fig. 1.6(a).[2,21,34,39] The dangling bonds seek to form surface bonds with each other as in Fig. 1.6(b), or capture oxygen atoms from the atmosphere and form a thin, amorphous oxide layer. Each of these surface bonds

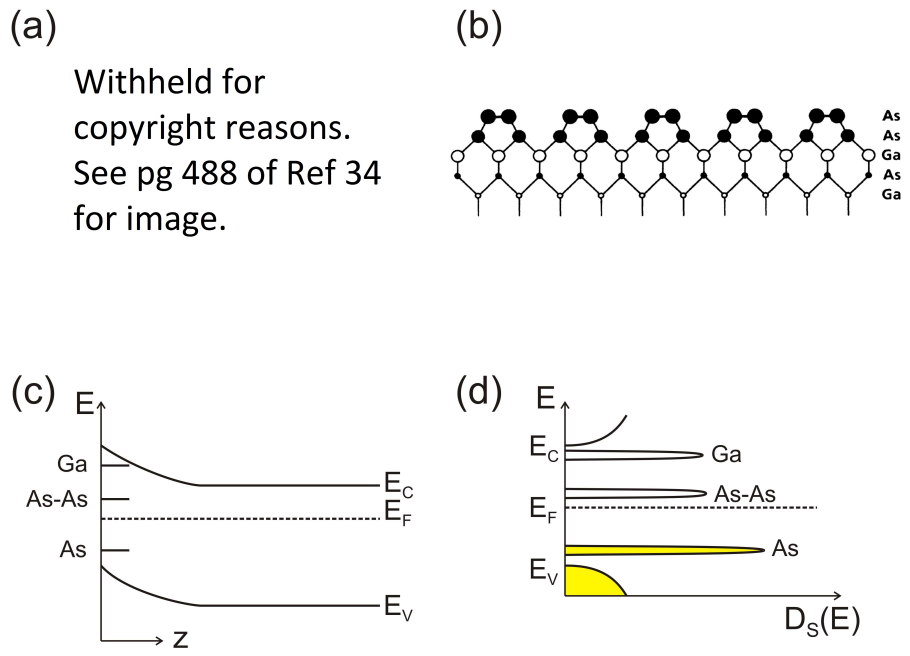

FIGURE 1.6: (a) The underlying order of a crystal is disrupted at the surface, leaving surface atoms with unsatisfied dangling bonds. (b) One possible reconstruction the (100) GaAs surface may take in order to satisfy dangling bonds, according to Ref. 38. The surface of semiconductors exposed to air consists of an amorphous layer of oxides. (c) Band diagram near the (100) surface of n-type GaAs. The Ga-dangling, As-dangling and As-As dimer bonds generate surface states that pin E_F mid-gap, but the doping level requires E_F to sit closer to E_C in the bulk. This generates a surface barrier that makes it difficult to inject carriers. (d) Density of states at the surface $D_{SS}(E)$ illustrating the source of E_F pinning. The high density of surface states compared to conduction and valence band states means surface state occupation/density determines the Fermi level position. Note this diagram only applies at the semiconductor surface due to the localised nature of the surface states. Images in (a) and (b) from Refs 34 and 38.

are different to the bulk lattice bonds, and as such their associated electron energy states do not necessarily correspond to energies within the bulk bands. If the energies exist in the bulk band gap, these so called 'surface states' act as deep trapping sites localised at the surface.[21,39] Taking GaAs as an example, Fig. 1.6(c) shows that a clean (100) surface in vacuum consists of: Ga-dangling bonds associated with empty surface states; filled As- dangling bonds associated with filled states; and in some cases, As-As dimers associated with empty mid-gap surface states.[21,40–43] The surface states with energies in the band gap act as deep charge traps. By comparison, InAs has a smaller band-gap (0.345 eV vs. 1.42 eV for GaAs) and so the highest density of surface states is in the conduction band.[40] In

reality this surface state spectrum is modified following exposure to air due to the growth of an amorphous native oxide layer.[44,45]

A high density of surface states presents numerous problems when depositing metal onto a semiconductor to act as source/drain contacts or gates. The problems arise from Fermi level position being determined by the occupation of these surface states, rather than the occupation in the bulk energy bands (see Fig. 1.6(d)). This pins the Fermi level of any metal deposited on the surface with limited dependence on metal composition and semiconductor doping concentration.[27,46,47] For GaAs, the Fermi level is pinned mid-gap, making it difficult to inject carriers into the conduction or valence band. For InAs, the Fermi level pinning in the conduction band means that electrons are always injected directly into the conduction band.[48] Both situations are far from the ideal whereby the interface Schottky barrier can be tuned by metal composition and semiconductor doping.[2]

If the surface states are deep, long-lived traps (i.e. $E_T > k_B T$) with a high density, they can cause instability and hysteresis when gating transistors. This is outlined in Fig. 1.7 for an n-type channel. A negative voltage on the gate may cause positive charge to be trapped in the surface states at the expense of depleting the channel underneath. This reduces the ability of the gate to deplete the channel, and in extreme cases may result in regions where I_d is not affected by V_G at all, as all of the energy goes into populating surface states. If a sweep to depletion is stopped, I_d will rise over time as the charge traps continue to be filled with positive charge that compensates the gate voltage. Once all the charge traps are filled, the Fermi level can be controlled again and depletion can continue. As the gate is swept towards zero, the charge traps will depopulate, but depopulate slowly. This means that initially the gate has good control over the channel, and I_d rises quickly, following a higher path than it did on the sweep to depletion. This produces the clockwise hysteresis loop for electron devices in Fig. 1.7. The characteristics for hole devices is the mirror image, since depletion occurs for positive voltages. This produces an anti-clockwise hysteresis loop that will be important in discussion of instability in p-type quantum devices in Sec. 1.4.5 and Chapter 3.

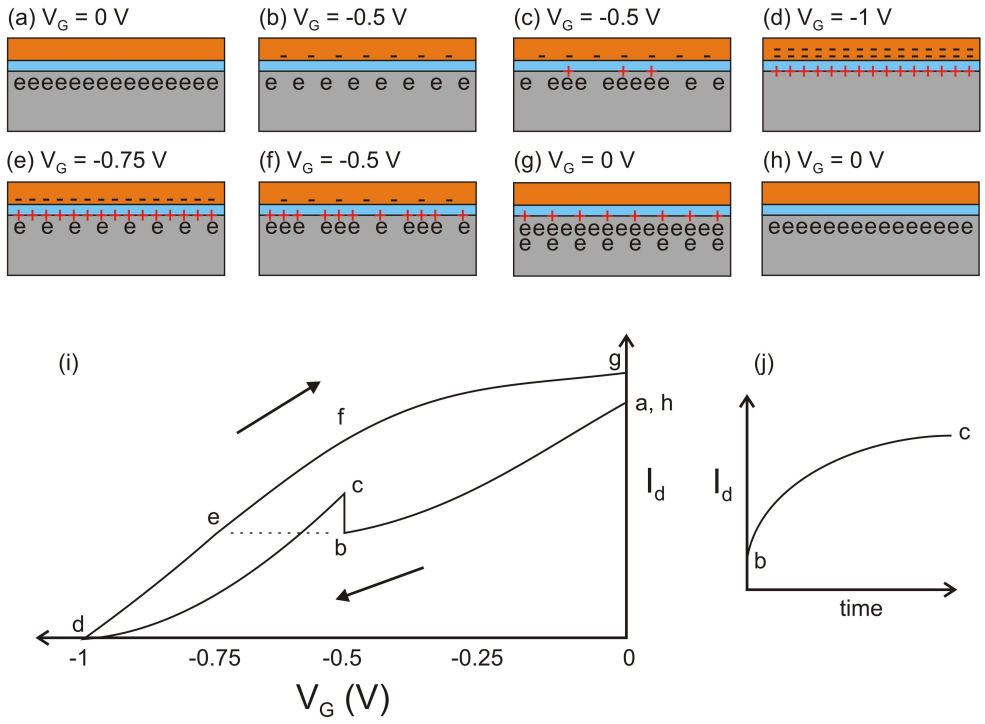

FIGURE 1.7: (a-h) Illustration of surface state charge trapping in a MOSFET with metal gate (orange), insulator (blue) and semiconductor channel (grey).(i/j) Electrical characteristics corresponding to how each situation in (a-h) generates hysteresis and instability in device characteristics. (a) Electrons, e, in the semiconductor channel carry current I_d. (b) Increasing V_G applies negative charge to the gate (-), depleting the channel of electrons. (c) Holding $V_G = -0.5$ V causes trapping of positive charges at the semiconductor/oxide interface (+), leading to the re-accumulation of electrons. (d) The channel is fully depleted at $V_G = -1$ V, but depletion may have required filling of all surface states. (e) As $V_G \to 0$ V, the surface states de-trap slowly. As such, the electron density for $V_G = -0.75$ V on this sweep is the same as it was for $V_G = -0.5$ on the sweep towards $V_G = 1$ V. (f) Similarly, the electron density for $V_G = -0.5$ V on this sweep is higher than it was for $V_G = -0.5$ on the sweep towards $V_G = 1$ V. (g) Not all surface states have de-trapped at $V_G = 0$ V, giving a higher current than in (a). (h) With time, surface states may de-trap, returning the device to the state it was at (a). (i) Hysteretic I_d vs. V_G traces for the sweeps to and from $V_G = -1$ V. Points corresponding to figures (a-h) are indicated. The dashed line shows that I_d is the same at points b and e. (j) I_d increases over time from points b to c as surface traps fill slowly, compensating the gate voltage at constant $V_G = -0.5$ V.

1.3.2.1 Surface state passivation

The success of Si-based transistors has much to do with the fact that the bonds between Si and its native oxide SiO_2 result in a low density of band-gap surface

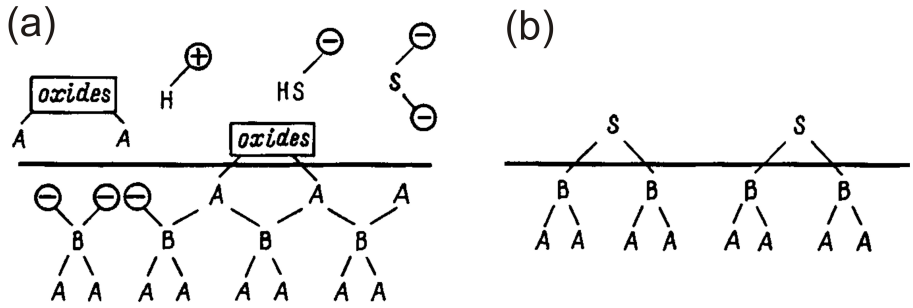

FIGURE 1.8: Chemical passivation for III-V semiconductors. A and B represent group-III and group-V elements, respectively. (a) The alkali solution etches the surface oxide layer. (b) Sulfur atoms form surface bonds, ideally with energy states outside the band gap. Adapted from Ref. 44.

states.[4,39,40,49] Unfortunately no such oxide is known for III-V's semiconductors. As a result, III-V surfaces and interfaces with gate oxides typically possess a high density of electrically active surface states in the band gap, which impede electrical and optical device performance.[4,40,44,49] Removing this impediment involves changing the bonding state of the surface/interface atoms with the aim of moving the surface states out of the band gap and into the conduction band, where they do not act as charge traps.[21] A favoured technique is the application of chemical passivation treatments. Passivation treatments act in two steps; first, they strip the natural oxide and secondly, they introduce an adsorbate atom which bonds in such a way that the associated surface states are non-band gap states (see Fig. 1.8).[21,44,50] A variety of treatments exist from both liquid and gas phases, with their suitability for different semiconductor surfaces dependent on adsorbate species as well as the chemical environment of the solution and semiconductor surface.[21,51,52]

One of the first passivation treatments for the (100) GaAs surface used spun-on $Na_2S{\cdot}9H_2O$.[53] This opened up a wealth of sulfur-based passivation solutions for this surface.[21] Aqueous and solvent-based ammonium sulfide solutions with or without extra sulfur loading – i.e. $(NH_4)_2S$ or $(NH_4)_2S_x$ – quickly emerged as the preferred solution due to the more effective native oxide removal.[44,50–52,54] These solutions were found to reduce the density of band gap states[41,43] and the associated surface Fermi level pinning[55] through the formation of Ga-S and As-S

bonds at the exclusion of Ga-O/As-O bonds.[56–59] Annealing the sample to $T = 300 - 360°\text{C}$ after treatment was found to improve the passivation in some cases by transferring S atoms from As-S to Ga-S bonds.[41,60,61] References 44 and 21 provide excellent overviews of the passivation process, including the etching of oxides by the alkali solution and the surface adsorption of sulfur atoms. I will discuss the importance of Ga-S and As-S bonding for passivation in more detail in light of my results in Chapter 3.

One limitation of sulfur-based passivation is the low stability of Ga-S and As-S bonds when exposed to air; over a period as short as 30 mins, the sulfur desorbs, allowing a re-adsorption of O which returns the surface to its original state.[57] However, the passivated surface remains intact for many metal- and oxide-deposition techniques, and once covered the surface is protected from the environment and will not re-oxidise.[40,41,62] This ensures $(NH_4)_2S_x$ is viable where the passivated surface can be quickly covered, such as in this thesis (Chapter 2 gives complete details).

1.4 Quantum physics of low-dimensional systems

The past few decades have seen the solid state realisation of many of the idealised quantum systems studied in undergraduate courses.[5,35,63] A combination of materials choice and selectively patterned surface gates can be used to modify the band structure. Quantum systems arise when the bands form potential wells that confine electrons/holes to regions on the order of the de Broglie wavelength at the Fermi energy (simply called the Fermi wavelength λ_F). Within these wells, electrons/holes occupy discrete energy levels known as sub-bands. The robustness of these systems depends on two conditions:[5,35,63] first, the electrons/holes should not be scattered by, e.g., ionised impurities or phonons. This requires a high carrier mobility to ensure a long mean free path ℓ between scattering events. Secondly, the sub-band spacing must be larger than the thermal energy k_BT to prevent

thermal smearing from making the sub-bands indistinct and returning the system to classical behaviour. For this reason, most devices require low temperatures, typically $T \lesssim 4$ K. At these temperatures phonons are strongly suppressed and impurity scattering dominates mobility. By harnessing high mobility materials and cryogenic measurement techniques, 2D, 1D and 0D systems of various forms have been realised in the solid state using a combination of band engineering and selective field-effect depletion. The breadth of available systems combined with the precision of control and read-out of particle dynamics *via* the field-effect and associated electrical measurement techniques makes nanoscale electronic devices a powerful tool for testing the theoretical predictions of quantum mechanics.[5,35,64,65] There is also a strong drive to harness their power for future devices, e.g., in quantum computing applications.[66,67]

1.4.1 2D systems; two dimensional electron/hole gas

A two dimensional electron/hole system (also known as 2D electron/hole gas, 2DEG/2DHG) can be generated at the junction between two materials with different band-gaps.[5,35] The junction can be a semiconductor heterostructure or a semiconductor/insulator interface (see Fig. 1.9). Application of an electric field from, e.g., a gate on the opposite side of the higher band-gap material induces electrons or holes in the lower band-gap material. The charge carriers are unable to overcome the potential barrier at the interface, which confines them to a two-dimensional sheet in the z-direction that extends in the x- and y-directions. To maximise the charge carrier mobility, the best choice is a lattice matched semiconductor heterostructure.[5] Electron mobility is much reduced for 2DEGs induced at semiconductor/insulator interfaces due to the interface/surface impurities outlined in Section 1.3.2.[35] Heterostructures can provide significantly less interface defects, but only if the two materials have matched inter-atomic spacing. Attempting to grow a heterostructure with different lattice constants results in significant strain, leading to defects at the interface, and even macro-scale fractures.[1,35,69] Thankfully, alloying of III-V compounds, e.g. $Al_xGa_{1-x}As$, $Ga_xIn_{1-x}As$, can be

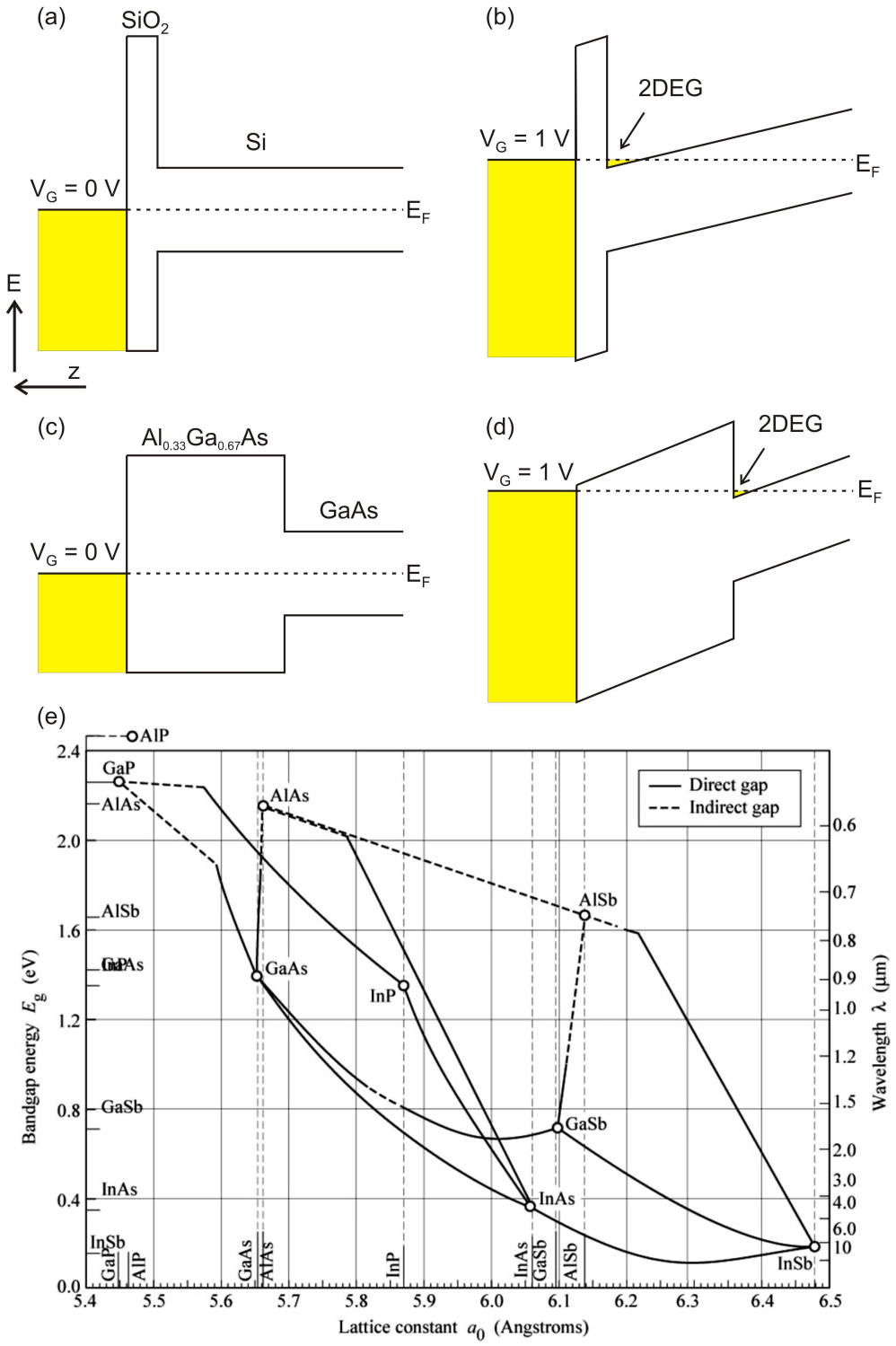

FIGURE 1.9: (a) SiO_2/Si and (c) $Al_{0.33}Ga_{0.67}As$ interfaces are used to induce 2D electron gases (2DEGs) *via* application of positive V_G (b, d). The 2DEG occupies a triangular well on a scale comparable to λ_F, confining electrons in the z-direction. (e) Band gap vs. lattice constant for III-V materials. Lines between pure compounds indicate the continuous variation of both parameters with alloying. $Al_xGa_{1-x}As$ is a popular choice due to the lattice matching across all alloys. Fig. (e) from Ref. 68.

used to vary both lattice constant and band gap. As Fig. 1.9(e) shows, there are a few materials combinations with the same lattice constant but different band gaps. The most well developed platform for quantum devices is GaAs with an $Al_xGa_{1-x}As$ alloy barrier. Drawing lines of constant lattice spacing in Fig. 1.9(e) reveal other possible combinations of fixed alloys, e.g., $InP/Ga_{0.47}In_{0.53}As$ is used for high speed electronic devices.[35] However, the $GaAs/Al_xGa_{1-x}As$ system provides much greater tunability as varying the alloy fraction x enables a continuous increase in band gap energy from 1.42 eV (GaAs) to 2.17 eV (AlAs) with a lattice mismatch of less than 0.15%.[35,70] Alloy fraction $x = 0.33$ is widely chosen as a trade-off between obtaining a sufficiently high barrier while minimising lattice strain. The devices in this thesis utilise a $Al_{0.33}Ga_{0.67}As$ layer, which I will refer to as AlGaAs for brevity.

1.4.1.1 High electron/hole mobility transistors

Figure 1.9(d) illustrates a problematic aspect of electrostatically inducing the 2DEG or 2DHG; it requires a large gate voltage to turn the device on, and risks current leaking over the AlGaAs barrier into the device. This is overcome with a band engineering technique called 'modulation doping', where the AlGaAs layer is doped.[71] Rather than occupying the AlGaAs layer, the electrons or holes diffuse into the GaAs layer where the interface potential prevents them from returning to the AlGaAs. The AlGaAs is left with positively/negatively charged donor/acceptor atoms, which attract the electrons/holes back towards the interface. The combination of the attractive dopant potential and the interface barrier potential generates confinement in the z-direction at $V_G = 0$ V (see Fig. 1.10).

The power of modulation doping lies in the fact that the dopant impurities and charge carriers are spatially separated. Ensuring the ionised dopant atoms are not directly in the path of electrons/holes maintains a high mobility[71] and leads to mean free paths of many microns at low $T \sim 4$ K.[5] The high mean free path

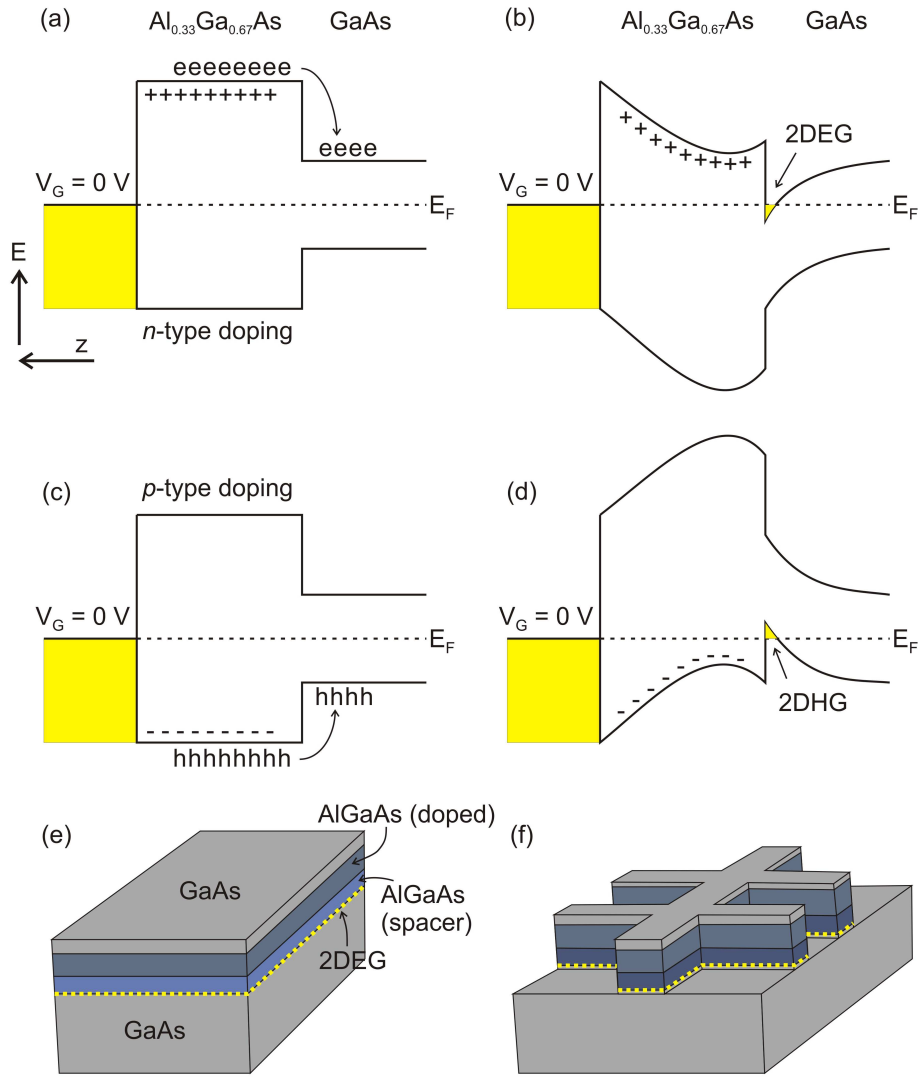

FIGURE 1.10: Modulation doping for (a/b) electrons and (c/d) holes. Electrons/holes diffuse from the doped AlGaAs layer into the GaAs layer. The electrons/holes leave positive/negatively charged dopant impurities in the AlGaAs layer. The combination of the attractive dopant potential and AlGaAs potential barrier traps electrons/holes in a triangular well at the interface. (e) An undoped spacer layer increases mobility and GaAs cap prevents AlGaAs oxidisation. (f) This wafer is selectively etched into a Hall bar mesa, with contact arms that are ultimately connected to voltage sources and probes (full details in Chapter 2).

and existence of the 2DEG without applied bias has seen modulation doped AlGaAs/GaAs heterostructures find extensive use as the basis for a wealth of low-dimensional systems discussed below. Mobility is enhanced further by the addition of an undoped AlGaAs spacer layer between the GaAs and doped AlGaAs layers.[72]

Choosing the spacer depth involves a trade-off between mobility and carrier density; the latter is reduced as the dopants are further away from the 2DEG/2DHG. A thin GaAs cap is added at the surface as AlGaAs oxidises strongly in air. The complete wafer is shown in Fig. 1.10(e).

Constructing devices from this wafer entails the addition of low resistance ohmic contacts to the 2DEG/2DHG and surface gate(s) to modulate carrier density. First, the 2DEG/2DHG is restricted to a controlled region in the x- and y-directions by etching a 'mesa' structure like that in Fig. 1.10(f); confinement in the x- and y-directions is much larger than λ_F so the system is still two dimensional. The mesa typically features multiple arms, each with an ohmic contact that connects the circuitry to the 2DEG/2DHG with a fixed resistance. The multiple arms are used to perform 4-point and Hall voltage measurements, hence the structure is known as a 'Hall bar'. The gates can be deposited directly onto the GaAs since the combination of the surface barrier and AlGaAs layer is sufficient to insulate the 2DEG/2DHG from the gate for low voltage applications.[5,73] A gate that uniformly covers a section of the channel can be used to modulate the carrier density as in a transistor. The transistor-like behaviour of this high mobility system leads to the names high electron mobility transistor (HEMT) and high hole mobility transistor (HHMT).[72] The excellent characteristics of HEMTs encouraged development towards high-speed microwave applications.[72,73] In fundamental research, the interest lies in selectively patterning nanoscale gates on the surface and using the field-effect to provide additional confinement in the x- and/or y-directions. Doing so enables the engineering and manipulation of one- and zero-dimensional quantum systems.

1.4.2 1D systems; quantum wires and quantum point contacts

Generating one dimensional systems from two-dimensional systems such as 2DEGs entails generating additional confinement perpendicular to the direction of transport. This can be accomplished *via*, e.g., split surface gates that selectively deplete

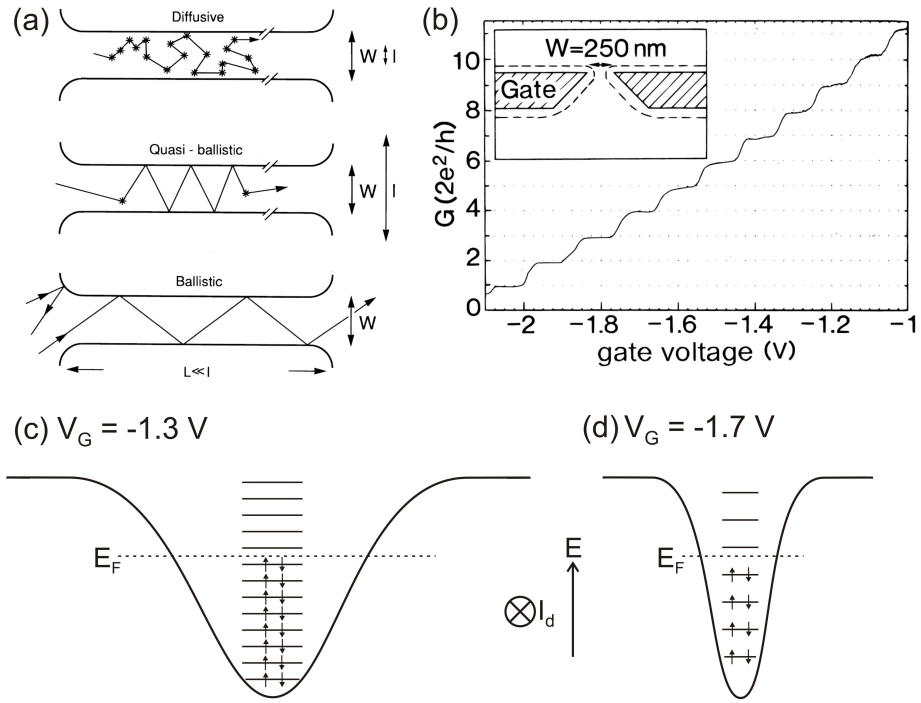

FIGURE 1.11: (a) 1D constriction with diffusive, quasi-ballistic and ballistic transport. Diffusive transport involves many scattering events and occurs when the length L and width W of the constriction are larger than the mean free path ℓ. Ballistic transport occurs when $\ell > W, L$ and carriers pass through the constriction without scattering. Electrons undergoing quasi-ballistic transport ($\ell > W, l < L$) will scatter only a few times, which can be viewed as a reduced transmission probability T_i (see text). (b) Split surface gates apply a 1D confining potential (dashed lines) to an underlying 2DEG. Ballistic transport through this potential results in conductance G quantised in units of $2e^2/h$. (c) Conduction band potential in the direction of current flow for $V_G = -1.3$ V applied to the side gates in (b). Each electron carries $I_d = (e^2/h)V_{sd}$. (d) More negative V_G squeezes the confining potential, increasing the sub-band spacing. the sub-bands depopulate as they pass through E_F. (a/b) from Ref. 5

an underlying 2DEG. The conductance $G \equiv I_d/V_{sd}$ and behaviour of electrons in 1D systems is dependent on the underlying transport regime; the three basic regimes are illustrated in Fig. 1.11(a). Diffusive transport occurs when device dimensions exceed the electron mean free path. Here, scattering from, e.g., dopant impurities dominates G according to classical electron transport theory. If no scattering occurs as electrons pass through this constriction they are said to undertake ballistic transport. In the ballistic regime, the conductance of the device is determined by the confining potential.[74,75] Operation of this device, known as a quantum point contact (QPC), is illustrated in Figs 1.11(b-d). The electric

field from the two gates establishes a confining potential that leads to electrons traversing the constriction through 1D sub-bands, analogous to the modes of a wave-guide.[5] Increasing the voltage on the two electrodes increases the extent of the electric field, further increasing confinement. As the constriction narrows, the 1D sub-band spacing increases, which depletes the sub-bands of electrons as they are pushed up through the Fermi level. Depopulation of the 1D sub-bands occurs in steps, resulting in a quantised conductance $G = i\frac{2e^2}{h}$, where i denotes the i^{th} sub-band. This expression arises as each sub-band contributes a current of $I_d = \frac{2e^2}{h}V_{sd}$ to conduction. More generally, $G = \frac{2e^2}{h}\sum T_i$ where T_i is the transmission probability, between 0 and 1, for the i^{th} sub-band through the QPC. This accounts for quasi-ballistic transport through the constriction, which consists of ballistic motion between very few scattering centres.[5] Systems with a 1D confining potential are known more generally as quantum wires, irrespective of the transport regime. Quasi-ballistic and diffusive 1D transport are of relevance for self-assembled semiconductor nanowires discussed in Sec. 1.5.4.

1.4.3 0D systems; quantum dots and billiards

Confinement in all three directions produces a quasi-zero dimensional system, usually referred to as a quantum dot. A common realisation of a quantum dot consists of an 'island' isolated from the source and drain leads by potential barriers. Electron transport through the system proceeds by tunnelling through the source barrier into discrete energy levels within the dot, and then subsequent tunnelling through the drain barrier. Two distinct effects contribute to the electrical behaviour of quantum dots. These are energy quantisation due to confinement and charge quantisation of the electron.[63,77,78] The former is analogous to the discrete energy levels that arise in square or parabolic potential wells and in atoms. Electrons within quantum dots behave somewhat like electrons in atoms in that they occupy degenerate 0D energy levels.[64,76] The second effect is known as Coulomb blockade, whereby the repulsive charge of electrons on the dot prevents subsequent electrons from tunnelling through the source barrier into the dot. Coulomb

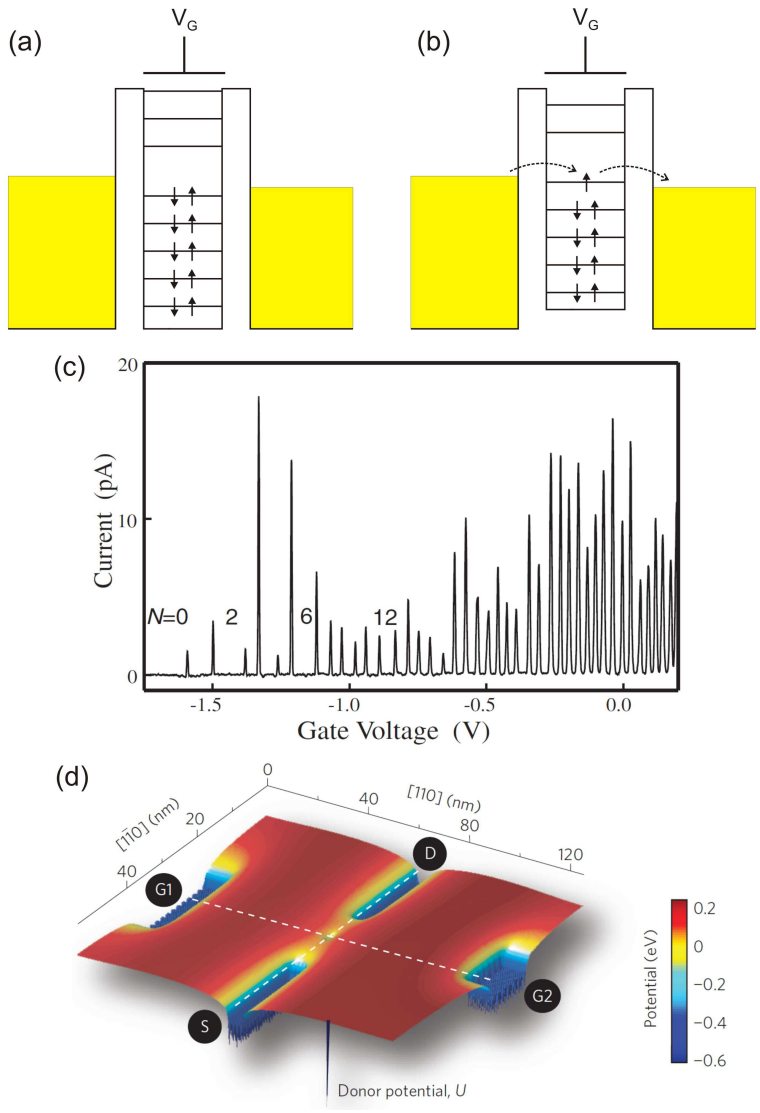

FIGURE 1.12: (a) Conduction band profile for a quantum dot with confinement in all three directions. (b) Transport takes place only when V_G is adjusted such that a discrete energy level is between the source and drain potentials. (c) A continuous sweep of V_G adds one electron at a time to the dot. The current resonances correspond to the situation in (b), and $I_d = 0$ for the situation in (a). (d) Two dimensional potential plot for a device where a single phosphorous donor in Si acts as a quantum dot. Electrons tunnel through the barriers from source (S) into the potential well and out to the drain (D), while gates G1 and G2 are used to modify occupation. Data in (c) from Ref. 76, image in (d) from Ref. 6

blockade is a capacitive charging effect, and thus the energy required to overcome blockade is e^2/C_{dot} where C_{dot} is the capacitance of the dot. The dot geometry determines the relative energy scales for the two effects. For quantum dots defined in epitaxial GaAs heterostructures, the capacative charging energy associated with

Coulomb blockade is often an order of magnitude *larger* than the separation of the energy levels associated with confinement.[63,76–78]

Figure 1.12(a) shows the spectrum of a quantum dot confined between two barriers that separate it from the source and drain on either side. The spectrum consists two contributions.[63,76,77] The first is the confinement in all three directions produces discrete, degenerate energy levels. The degeneracy arises from both spin, and symmetry effects that depend on the dot geometry. Secondly, the much larger energy separation near the source/drain potentials, above the highest occupied level, is due to Coulomb blockade. For the electron to have sufficient energy to tunnel into the dot, an empty dot energy state must be below the source potential. This can be accomplished by lowering the energy on the dot by varying V_G on a nearby gate electrode. Increasingly positive V_G leads to the situation in Fig. 1.12(b), where the lowest unoccupied level is brought between the source and drain potentials. Transport now occurs through the system *via* sequential tunnelling on to the dot from the source and off the dot into the drain, resulting in current through the device. Continuing the sweep to more positive V_G brings the energy level to below the drain potential where electrons now have insufficient energy to tunnel out. This traps a single additional electron within the dot and returns the current flow to zero. Continuing this process adds electrons to the dot one by one.[79] Figure 1.12(c) shows that this process can be sensed as a current at the drain, which exhibits sharp resonances when electrons pass through the QD (situation in b) and is zero otherwise (situation in a).[76]

The electrical properties of quantum dots are almost entirely characterised by the energy required to add the next electron. If the next available energy state is in the same degenerate 0D energy level, the addition energy is simply the capacitive energy required to overcome Coulomb blockade, $\Delta E_a = \frac{e^2}{C_{dot}}$. If the 0D degenerate energy level is filled, the next electron must occupy a higher energy level. The addition energy is then $\Delta E_a = \frac{e^2}{C_{dot}} + \Delta E_{0D}$, where ΔE_{0D} is the spacing between adjacent 0D levels. This explains the different spacing between the peaks for added electron number $N = 2, 6, 12$ in Fig. 1.12(c); a larger peak separation occurred when the added electron must start to fill the next 0D energy level.[76]

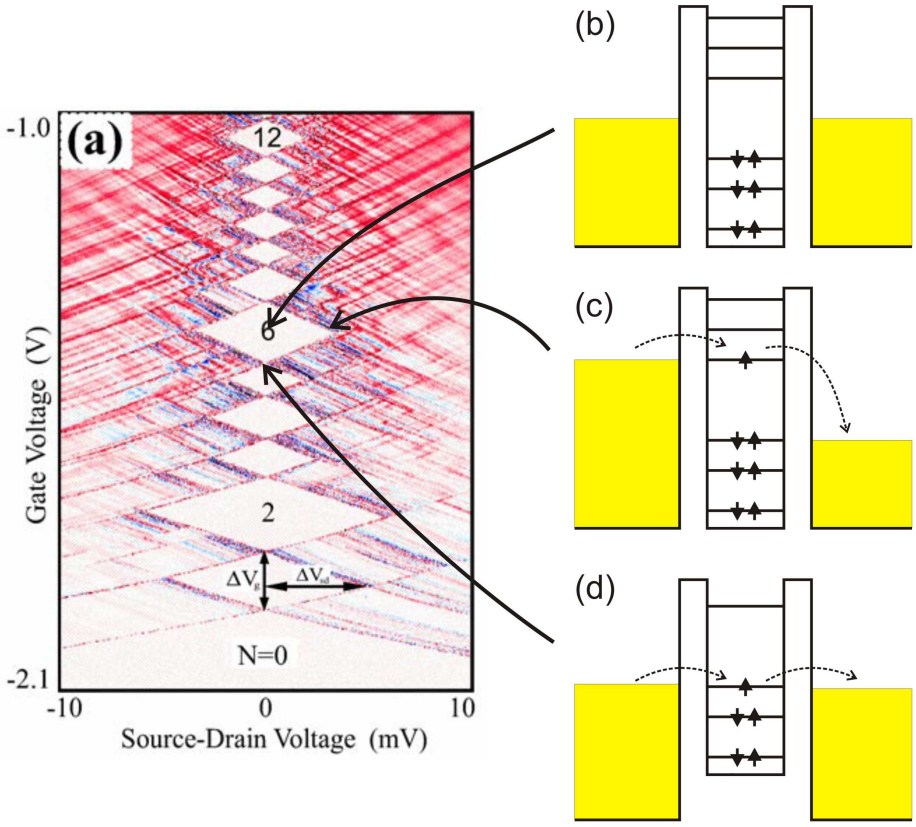

FIGURE 1.13: (a) Source-drain bias spectroscopy data. Differential conductance $\frac{\partial I_d}{\partial V_{sd}}$ is shown in colour; white corresponds to $\frac{\partial I_d}{\partial V_{sd}} = 0$, red to positive $\frac{\partial I_d}{\partial V_{sd}}$ and blue to negative $\frac{\partial I_d}{\partial V_{sd}}$. (b) In the central diamonds, no current passes through the dot and N electrons are on the dot. (c) At the left/right diamond vertices the source/drain potentials line up with two adjacent energy levels. Current flows for all higher V_{sd}. $e\Delta V_{sd}$ corresponds to the energy required to add an electron to the dot. (d) At the top/bottom vertices of each diamond, $V_{sd} \sim 0$ V, and is aligned with a dot energy level, allowing current to pass. A cut through the data at $V_{sd} \sim 0$ V produces the data in Fig. 1.12(c). Data in (a) from Ref. 76

The degeneracy of the 0D levels depends on geometry. A large degeneracy can be observed above the third 0D energy level for this device. After $N = 12$, adding electrons consisted of simply overcoming Coulomb blockade.

Source-drain bias spectroscopy (SDBS) provides a powerful technique for mapping dot energetics, outlined in Fig. 1.13.[80] It consists of applying a variable DC bias V_{sd}^{dc} to split the source/drain potentials, while also varying V_G. Varying both V_{sd}^{dc} and V_G and constructing a 3-dimensional plot with I_d on the z-axis produces a series of diamonds, where transport is forbidden (permitted) inside (outside) the

diamonds.[76] The transport regimes arise in the following way. In the middle of the diamonds there is no energy level between the source and drain potentials and transport does not occur (Fig. 1.13(b)). Increasing source-drain bias splits the source/drain potentials. Transport occurs when this supplies sufficient energy for electrons to overcome the addition energy, i.e., $e\Delta V_{sd}^{dc} = \Delta E_a$, where ΔV_{sd}^{dc} is the V_{sd}^{dc} between the centre and corner of the diamond, indicated in Fig. 1.13(a). For higher V_{sd}^{dc}, transport is always possible as there is always at least one level between the source and drain potentials (colour regions in Fig. 1.13(a)). Again, modulating V_G increases/decreases the dot energy levels with respect to the source and drain potentials (Fig. 1.13(d)). Taking a cut of I_d vs V_G along $V_{sd} \sim 0$ reproduces the Coulomb resonances in Fig. 1.12(c). The diamond pattern arises because larger V_{sd}^{dc} increases the V_G window where transport occurs. The coloured stripes outside the diamonds highlights a complex series of sharp transitions related to the excitation spectra of the dot. This is because the source/drain potential is greater than the Coulomb blockade energy and is thus resonant with the higher-level 0D states.[76] The power of SDBS is that it facilitates an almost complete characterisation of the ground state energetics of the dot. Charging energy ΔE_a, dot capacitance C_{dot} and gate capacitance C_G are all obtained from the size of the diamonds, and from these the dot's physical size can also be calculated. This is done for a quantum dot embedded in a semiconductor nanowire in Chapter 5.

Quantum dots of this type are sometimes thought of as 'artificial atoms', due to their similarity to many atomistic features.[64,76] The ability to precisely address and control single electrons in an atom-like system gives researchers an opportunity to explore the spin properties of single electrons and the exotic behaviours resulting from interactions in a way that is not possible with isolated atoms.[64,76] Additionally, the spin of single electrons confined in a quantum dot is a prime candidate for a viable, scalable quantum bit (qubit).[66,67] Addressing single spins relies on first breaking the spin degeneracy in a magnetic field. This has driven strong interest in materials with a high g-factor, such that two-level systems can be generated at low fields.[81]

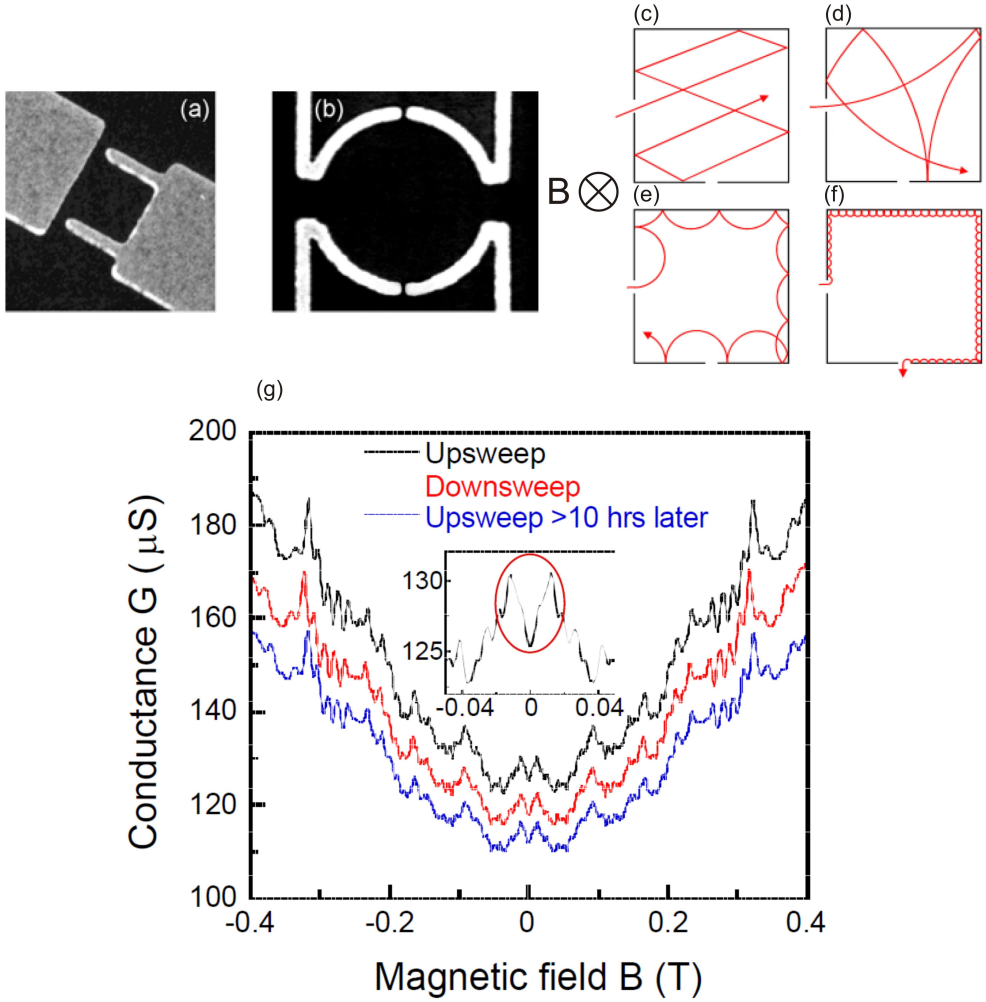

FIGURE 1.14: (a/b) Scanning electron micrographs of surface gates that define a 1×1 μm square billiard and 1 μm diameter circular billiard on the underlying 2DEG, with entrance/exit QPCs. (c) Electron trajectories consist of ballistic paths between scattering events at the billiard walls. (d/e) The paths are curved under the influence of a magnetic field B perpendicular to the transport plane. (f) For high B, electrons undergo edge transport, consisting of skipping orbits along the billiard walls. (g) Magnetoconductance fluctuations (MCF) provide a unique fingerprint of the interference between possible electron paths through the dot. The fluctuations are reproducible for $>$ 10 hours when the sample is kept at low temperatures (the vertical offset was introduced for clarity). Figures adapted from Ref. 82.

A second type of quasi-0D system is known as an open quantum dot, or billiard. Here, the dot is strongly coupled to the reservoir, usually by two QPCs at the entrance and exit that are set to $G \geqslant 2e^2/h$ (Figs 1.14(a/b)).[65,83] Most billiards could also be considered a quasi-2D system, since x- and y-confinement typically exceeds λ_F, but is below the mean free path length. Additionally, since QPCs

at these settings do not constitute tunnelling barriers, Coulomb blockade is not observed. Rather, the interest in billiards is on the trajectory of electrons in the billiard and quantum interference effects. The entrance QPC diffracts electrons, setting up multiple paths that interfere at the exit QPC.[65,82,83] In the ballistic case, the paths are determined by the billiard geometry as transport consists of electrons scattering off the billiard walls. The result of this interference determines the conductance G of the device. The paths can be altered by curving them with a magnetic field B which generates fluctuations in $G(B)$ (Fig. 1.14). These magnetoconductance fluctuations (MCF) are clearly not random, or noise, since $G(B) = G(-B)$ and they are reproducible for consecutive traces.[65,82,83] As such MCF provide a 'magneto-fingerprint' of the trajectories taken through the billiard.[84] Chaotic behaviour is observed with some geometries as the trajectories are very sensitive to the initial conditions.[65,82] Associated fractal behaviour has also been observed, where order on the large scale is repeated on smaller scales.[82]

1.4.4 Remote ionised impurities and quantum transport

The key assumption underlying ballistic transport studies in AlGaAs/GaAs heterostructures is that the remote ionised dopant impurities in the AlGaAs layer do not adversely impact electron trajectories. With dopants out of the way, electrons could be assumed to proceed in straight lines between confining potential walls, or the remaining large-angle scattering centres such as the inevitable unintentional impurity. This picture is only partially true. In reality, the 'tails' of the dopant potentials still cross the 2DEG, causing a random background potential on a scale smaller than the mean free path, as in Fig. 1.15.[85] The high mobility $\sim 10^6$ cm^2/Vs typically achieved is due to the fact that the tails cause small-angle scattering, not large-angle scattering (c.f. Fig. 1.15(a)).[86,87] Large-angle scatterers make a much larger contribution to mobility degradation since by definition they knock electrons away from the drift direction. Nevertheless, small-angle scattering must take place between large-angle scattering events in 2DEGs, knocking electrons from their straight line trajectories (Figs 1.15(d/e)).

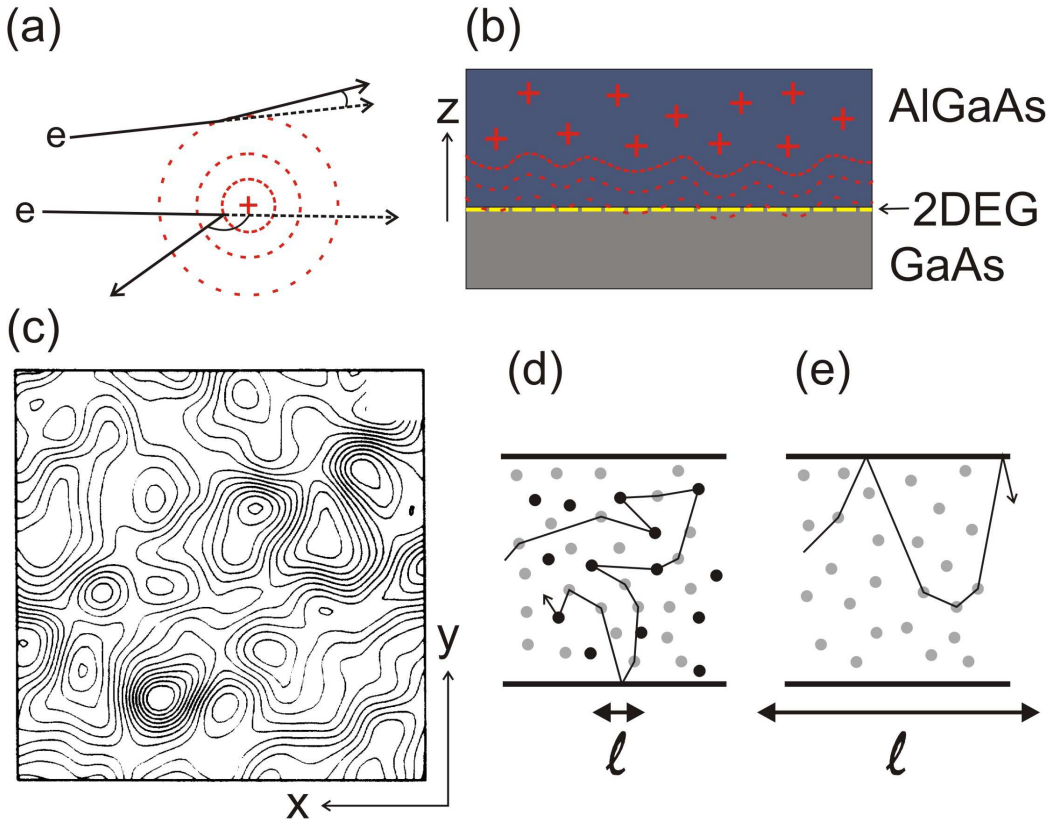

FIGURE 1.15: (a) Scattering from an ionised impurity potential. Red dashed lines represent potential contours, while solid black lines represent the electron trajectory and dashed black lines represent the path without scattering. Large-angle scattering from head on collisions impedes mobility more than small-angle scattering from glancing collisions. (b) The random placement of ionised impurities in the AlGaAs layer generates a random background potential which crosses the 2DEG. (c) Calculated non-uniform background impurity potential at the 2DEG for a 0.5 μm^2 section (from Ref. 85). (d/e) Electron trajectory is altered by both large-angle and small-angle scattering sites (black/grey dots) for diffusive transport. (e) In the ballistic limit where device dimensions are less than the mean free path ℓ, electrons still undergo small-angle scattering.

The question is, how does small-angle scattering affect the quantum transport studies mentioned above? Fortunately, the influence is likely to be negligible for many systems. In particular, transport through QPCs is not affected by *forward* scattering as this just causes the electrons to scatter between sub-bands; it doesn't change the number of occupied sub-bands.[5] However, probing the paths electrons take after leaving a QPC has shown that paths of electrons in a 2DEG *are* sensitive to small-angle scattering.[88,89] This is likely to strongly impact MCF in open quantum dots/billiards, as they are entirely dependent on electron trajectories.

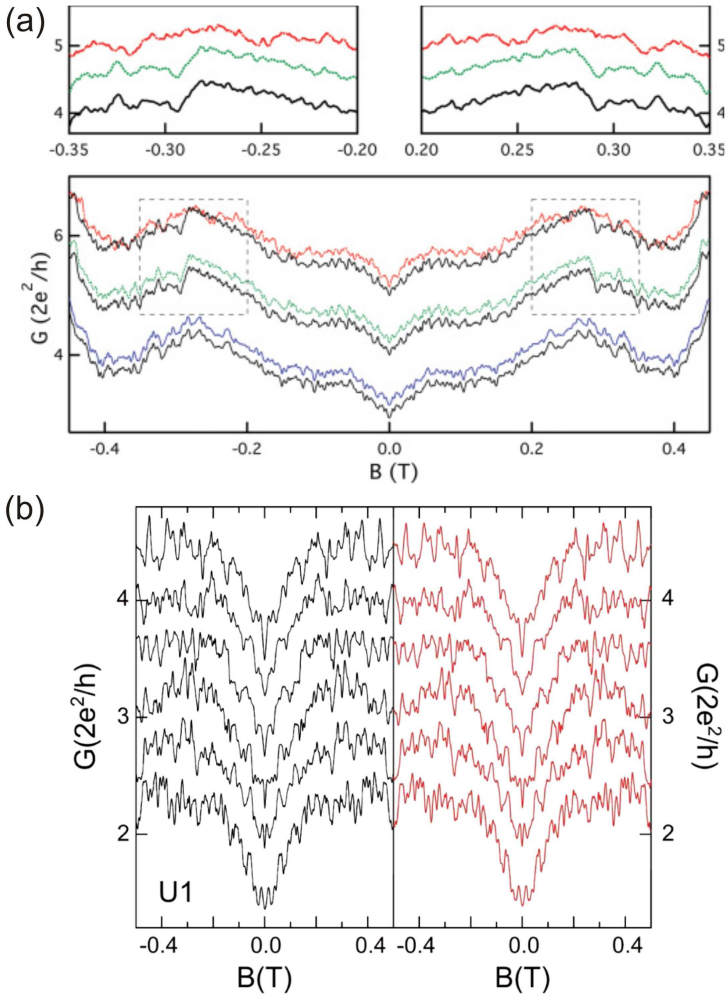

FIGURE 1.16: (a) MCF in a billiard populated by modulation doping. Traces taken before (black) and after cycling to $T_i = 240$ mK (blue), 115 K (green), and 300 K (red). MCF are robust unless k_BT exceeds the donor trap depth. Traces offset vertically for clarity (from Ref. 91). (b) MCF for a billiard populated electrostatically, without modulation doping, before (left/black) and after (right/red) cycling the device to $T_i = 300$ mK. Each trace is at a different top-gate voltage V_G. This demonstrates that removing the dopants results in robust MCF at a range of electron densities. From Ref. 90.

The impact of remote ionised impurities was considered initially, but thought to not adversely impact the essential physics.[65] Since then, a compelling body of evidence has steadily built for the notion that impurity distribution *does* play a large part in determining MCF in billiards (for a review, see Ref. 84). Definitive confirmation of the importance of small-angle scattering in billiards has come recently in two related works, which I turn to now.[90,91]

It is a well known, but rarely acknowledged fact that while MCF traces are reproducible while the device is held at low T in the cryostat, the MCF are not reproducible upon thermally cycling the device to room temperature and then cooling back down.[65] This suggests that something changes in the device that causes changes in the scattering potential. To probe the source of this change, Scannell *et al.*[91] measured initial trace $G_1(B)$ at 230 mK, held the device at intermediate temperature between $T_i = 230$ mK and 300 K for 30 minutes before cooling to $T = 230$ mK and measuring final trace $G_2(B)$. They then examined the correlation between traces $G_1(B)$ and $G_2(B)$ using an autocorrelation function that measured the difference between traces $G_1(B) - G_2(B)$ and normalised it to values between 0 (no correlation) and 1 (complete correlation).[92] The key results are shown in Fig. 1.16(a); for low $T_i \leqslant 115$ K, $G_1(B)$ and $G_2(B)$ were found to be identical. Around $T = 165$ K, traces began to significantly decorrelate, and correlation was destroyed above $T = 200$ K. This is precisely the point where Si donors in the AlGaAs layer are known to de-trap.[93,94] The conclusion is that thermal cycling to $T_i \geqslant 150$ K caused the charge configuration in the dopant layer to change, and the subsequent background potential to change. The related change in MCF gives strong evidence that small-angle scattering from remote impurities impacts the magnetofingerprint of the billiard. A follow-up work[90] performed the same experiment but for a device without modulation doping. The MCF in this device were robust to thermal cycling all the way up to room temperature (see Fig. 1.16(b)), further confirming dopants play a major role in determining electron paths through the dot. Turning this result around, the decorrelation of MCF in billiards has the potential to provide information on changes in remote ionised impurity configuration. In Chapter 3 I use the MCF of a hole billiard to probe dopant dynamics in p-type AlGaAs/GaAs heterostructures, in an effort to understand instability in these wafers.

1.4.5 Instability in p-type GaAs/AlGaAs heterostructures

Almost all of the studies mentioned above involved electron devices. This is not for a lack of interest in holes; on the contrary, holes in GaAs possess a number of interesting features. For example, their reduced spin-decoherence times compared to electrons makes them of great interest for quantum computation applications.[95–98] The presence of strong spin-orbit interactions also gives holes in GaAs a spin-$\frac{3}{2}$ nature which leads to geometrical anisotropies in spin-splitting,[99,100] and lends insight into other novel quantum phenomena.[101–103] Wafer growth is not the limiting factor either; although it was predicted to be non-trivial to grow p-type AlGaAs/-GaAs heterostructures,[104] it is now routinely done. In fact, the amphoteric nature of Si in AlGaAs facilitates the side-by-side growth of nominally identical p-type and n-type heterostructures. Si settles on Ga sites for (100)-oriented growth, and on As sites for (311)A-oriented growth, leaving the former n-doped and the latter p-doped.[105] This means that simply placing (100)-oriented and (311)A-oriented wafers side-by-side in the growth chamber gives matched n- and p-modulation doped structures.[24,105] C-doping has also been utilised as an alternative method for crystal growth on lower-index planes (e.g. (100) and (110)).[106–108]

The limiting factor for p-type heterostructures has been device instability under gating. In electron devices, using gates to confine electrons to quantum systems as discussed above is in general very robust. The devices operate without hysteresis, allowing very reliable measurements across long time periods. By contrast, gates on p-type heterostructures are plagued with instability and hysteresis for both Si- and C-doping. Some one- and zero-dimensional systems have been realised by using alternative etching or oxidation[106,109] techniques, or by working within the limits provided by gate instability.[108,110] However, data from these devices was generally more noisy and prone to drift than that from electron devices (see Fig. 1.17). That this is some of the best data from the literature highlights the significant problems faced in constructing hole quantum systems from modulation doped AlGaAs/GaAs heterostructures.

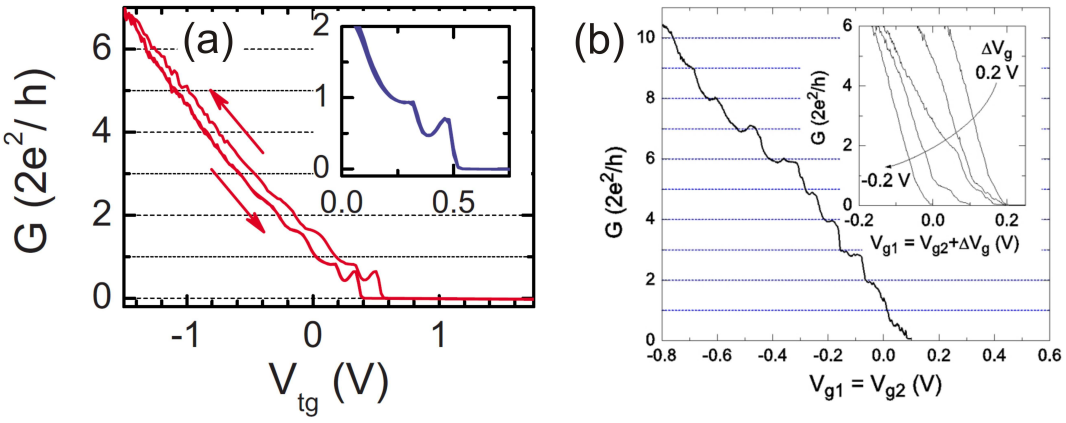

FIGURE 1.17: (a) Data from a hole QPC generated by two side gates at $T = 100$ mK (Ref. 108). The occupation is varied *via* a voltage applied to a separate top-gate, V_{tg}. Conductance steps are poorly defined and the device suffers hysteresis. Inset: Hystersis is reduced with a reduced operating range. (b) Data from a hole QPC defined by local anodic oxidation, with V_g applied simultaneously to two split gates, $V_{g1} = V_{g2}$ at $T = 50$ mK. It is not clear if hysteresis was present, however there is more noise than would be expected from an electron device. From Ref. 109.

The data in Fig. 1.18(a) gives an indication of the magnitude of the problem. This device consisted of a Si-doped p-type AlGaAs/GaAs heterostructure with a top gate covering the entire Hall bar area to modulate the 2DHG density.[24] Sweeping the device to positive voltages saw the device go through a region where the gate was ineffective, before depletion could be completed. If the gate was stopped, the device would relax towards higher I_d. The sweep toward $V_G = 0$ V saw I_d running at higher values. Similar results have been seen by other groups. The relaxation of I_d in particular destroys the hope for maintaining stable quantum systems, as the gates cannot provide a uniform, consistent, stable confining potential.

Prior work by our group suggested that both dopant impurities and surface states play a role in the instability of p-type heterostructures.[24] The work in Burke *et al.*[24] was originally spurred by suggestions that charge carriers leaking into the heterostructure from the gates was the cause of the hysteresis.[106,108] The best check for this hypothesis is to fabricate devices with an insulating layer between the GaAs cap and the gate. Doing so did not fix the hysteresis; Fig. 1.18(b) shows that insulating the gates in fact worsened the hysteresis.[24] The fact that a surface modification produced such a clear change strongly suggests a contribution from

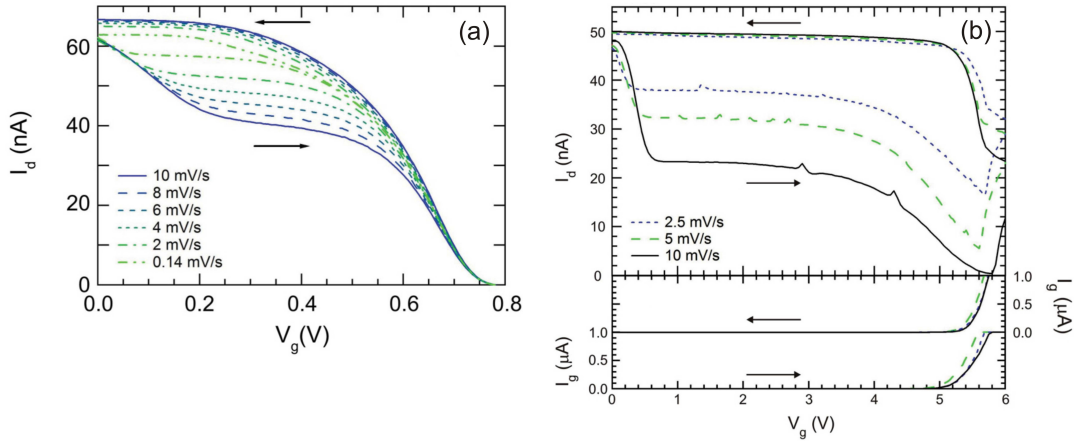

FIGURE 1.18: I_d vs V_g for HHMTs with (a) uninsulated and (b) insulated surface gates at $T = 4.2$ K. The hysteresis direction and sweep rate dependence is consistent with charge trapping/migration between the gate and 2DHG. The degraded performance in (b) is likely due to the high density of surface states at the GaAs/Al_2O_3 interface. The device could not be completely depleted before current I_g leaked from the gate into the 2DHG. (c) Optical micrograph of a HHMT with uninsulated gates. Data in (a/b) from Ref. 24.

surface states. Long-lived charge traps between the 2DHG and the gate would explain the data in Fig. 1.18 (c.f. discussion in Sec. 1.3.2). Building on this, I applied surface passivation solutions underneath the (uninsulated) gates. The focus was on the widely used sulfur-based solutions that have proven effective for (100)-oriented GaAs surfaces. While this did cause nominal changes to device behaviour, there was only one device where hysteresis was appreciably reduced.[24] This called into question the efficacy of sulfur-based solutions for (311)A GaAs surfaces. In Chapter 3 I present a focussed study of the electrical behaviour of HHMTs treated with sulfur passivation solutions prior to gate deposition. I also used photoluminesence and XPS as independent characterisation tools to examine the chemistry and physics of the passivation solutions.

As part of the work in Burke *et al.*[24] we considered other potential explanations for the hysteresis. In particular, instability in the doping layer could lead to instability of the 2DHG if the distribution of ionised impurities is affected by the gate potential. The stability of *n*-type Si dopants in AlGaAs is in part due to incorporation of deep traps known as DX centres. These arise from lattice distortions caused when the Si dopant settles on the Ga site. The form of the potential of

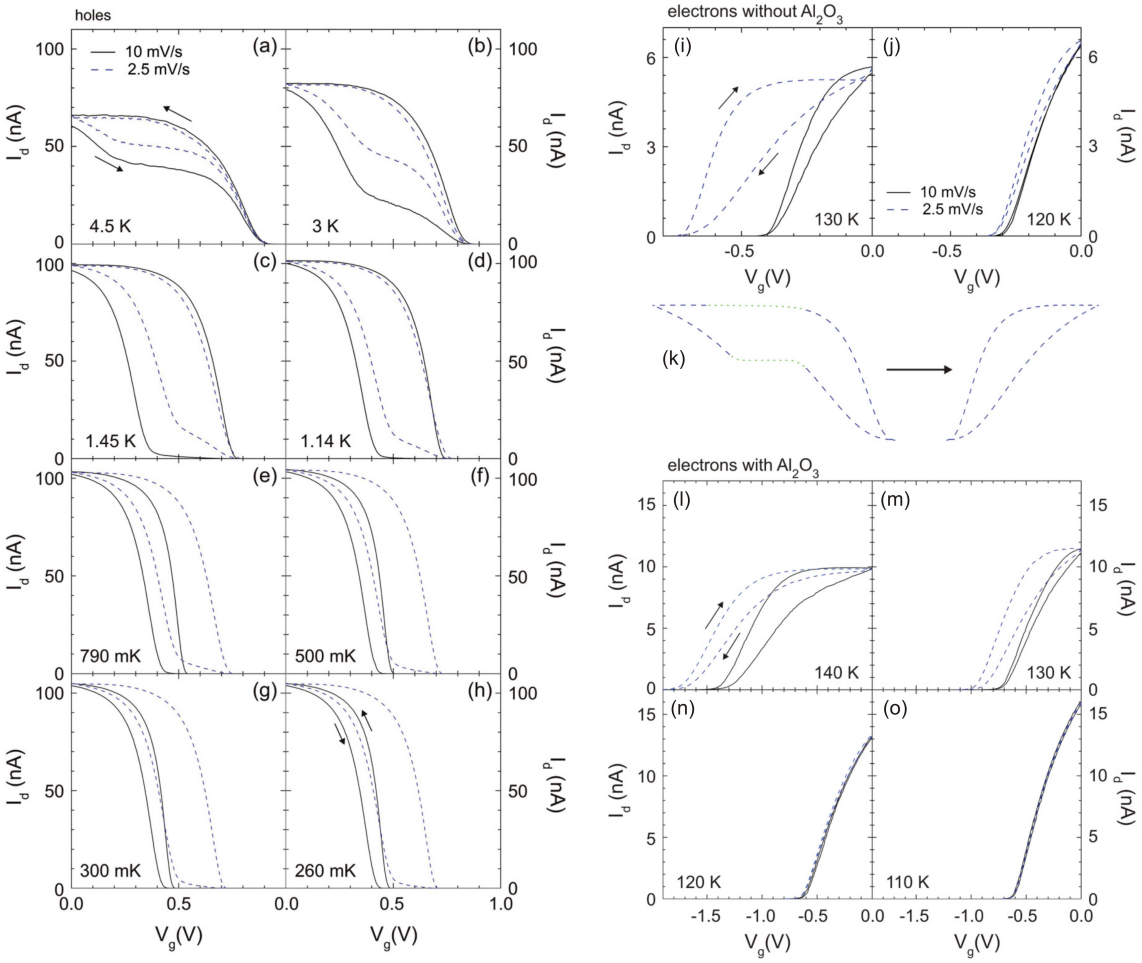

FIGURE 1.19: Temperature dependence for hole (left) and electron (right) modulation doped AlGaAs/GaAs heterostructure transistors. (a-h) Hysteresis is reduced for hole devices as temperature drops from $T = 4.5$ K to 260 mK. (i/j) Hysteresis was introduced by measuring electron devices at $T > 130$ K, where the gate causes charge migration between dopant sites in the AlGaAs layer. (k) The electron data looks similar to the hole data, except for the plateaus at intermediate V_g. These may be due to surface state differences between the (311)A and (100) surfaces, while the remaining hysteresis arises from charge migration in the dopant layer. The gates on uninsulated electron devices leaked above $T = 130$ K. (l-o) Electron devices with insulated gates allowed measurement up to $T = 140$ K to confirm the effect. From Ref. 24.

DX centres is unusual in that it features a barrier to electron trapping.[93,111,112] This barrier, combined with the depth $E_T = 250$ meV makes it very unlikely that electrons will migrate between trapping sites at $T \leqslant 4.2$ K. By contrast, little is known about Si-acceptors in AlGaAs; previous evidence suggests they form shallow potential wells without a trapping barrier.[113] In this case, the acceptors may

be active even at $T = 4.2$ K and trapped holes may be able to migrate by hopping between acceptor sites in response to an external potential. Since hopping is thermally activated, the hysteresis should have a temperature dependence. We performed temperature dependent studies of both p-type and n-type heterostructure devices to test whether dopant migration contributed to hysteresis, shown in Fig. 1.19. In the n-type devices, we saw hysteresis emerge for $T \geqslant 130$ K, where DX centres are known to begin to de-trap charge,[91,93,94,114] similar to results from semiconductor billiards in Sec. 1.4.4. Note that the apparent activation temperature in this experiment was $\sim 20 - 30$ K lower than for the billiards, because the gate potential constitutes a strong perturbation that causes charge migration between dopant sites. By contrast, the billiard experiments relied on temperature-induced spontaneous re-organisation alone. Returning to Fig. 1.19, the form and temperature dependence of the hysteresis in n-type devices above $T = 130$ K mirrored that of p-type devices below $T = 1$ K. This suggests strongly that the shallow acceptor traps are active at low temperatures and contribute to the hysteresis.[24] In Chapter 3 I present data related to MCF in a hole billiard fabricated from the p-AlGaAs/GaAs wafer. I follow the methodology of Scannell *et al.*[91] to estimate the potential well depth E_A for Si acceptors in $Al_{0.33}Ga_{0.67}As$, using a measured activation temperature ~ 2 K. I also show that the gate altered the charge configuration in the dopant layer even at $T = 40$ mK, well below the activation temperature.

1.5 Self-assembled semiconductor nanowires

1.5.1 Motivation

Si-based microelectronics has been a hugely successful technology platform in the manufacture of integrated circuits, solar cells and LEDs. The wide use of Si comes down to two factors: Firstly, the natural oxide, SiO_2, produces a very clean interface with Si that features a low defect density and the lack of a comparable oxide for III-V semiconductors has hampered device development in this area (as

discussed in Sec. 1.3.2).[4,39,40,49] Secondly, Si is relatively low cost and plentiful in supply compared to III-Vs, making it more economically viable.[49] However, Si has properties that restrict the capacity for devices with increased energy efficiency: its low electron/hole mobility imposes restrictions on transistor switching speed and I_{on} and its indirect band gap limits efficient use in opto-electronic applications such as LEDs and solar cells. Instead there is a strong desire to use III-Vs, which generally feature higher electron/hole mobilities and band gap tunability through alloying.[4,49] Although many prototype devices have been made, there is an economic hurdle for commercial use of III-Vs. The fabrication of integrated circuits proceeds from selectively etching Si wafers to create islands that form the basis for individual transistor channels. The relatively thick underlying wafer acts as a physical support for the overlayed devices. It is simply not economically viable to grow mm-thick wafers of e.g. GaAs and then utilise only the top 10-100 nm of material for device fabrication.[3] A compromise would be to grow a mm-thick Si wafer and then thin layers of III-V's on top, but this can only be done directly if the III-V material has the same lattice constant as Si, limiting the choice of materials according to Fig. 1.9(e). Two solutions to this problem are the growth of buffer layers that make the transition between the Si and chosen III-V lattice constants either gradually to prevent dislocations[12] or *via* intentionally introduce dislocations,[115] and wafer-bonding techniques that use van der Waals forces to join separately grown wafers.[116,117] However, self-assembled nanowires facilitate crystalline III-V material growth directly on Si substrates. This has opened up other possibilities for device applications and quantum system exploration.

1.5.2 Growth principles and advantages

Self-assembled semiconductor nanowires were first realised using particle-assisted, vapour-liquid-solid techniques,[119–123] such as metal-organic chemical vapour deposition (MOCVD). To grow nanowires by MOCVD, Au nano-particles are spread across a substrate surface (Fig. 1.20(a)); they act as a catalyst for nanowire growth. The substrates are placed in a high temperature growth chamber ($T \sim$

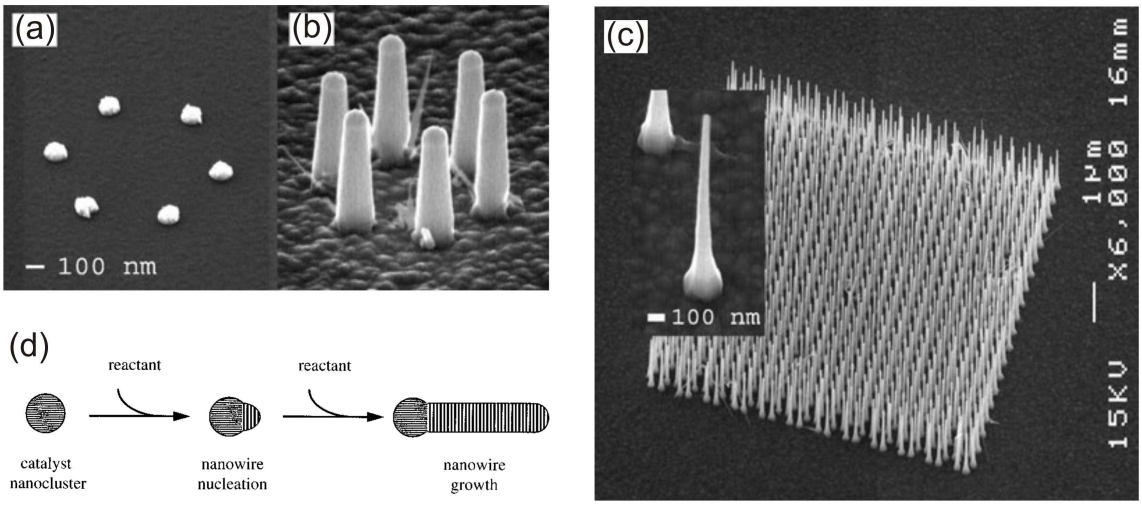

FIGURE 1.20: Scanning electron micrographs of (a) 100 nm diameter Au particles prior to nanowire growth, (b) as-grown nanowires from the particles in (a) and (c) a larger array of nanowires. From Ref. 118 (d) Nanowires grow preferentially underneath the catalyst, after an initial nucleation process. From Ref. 119

$500 - 700°C$) and exposed to a flow of precursor gas. For InAs, the gases are trimethylindium and arsine, which facilitate atomic In and As incorporation into the liquid Au droplet. This essentially forms a tiny melt, where In and As crystallise into InAs beneath the droplet (Fig. 1.20(d)).[124] Progressively more InAs material grows under the Au particle, ultimately forming a nanowire where the size of the Au particle determines the nanowire diameter – typically 20 - 200 nm – and the growth time determines the length – typically 100 nm - 20 μm. The Au particles can be patterned before nanowire growth to facilitate high density arrays (e.g. Fig. 1.20(b/c)).[118] An number of methods have since been developed to grow very high quality nanowire arrays using, e.g., molecular beam epitaxy without the need for catalyst particles.[125,126]

The biggest advantage of the self-assembly process is that the very high aspect ratio means the III-V material is not constrained to a substrate and can tolerate a high strain relaxation without defects.[127,128] As such, III-V crystals can be grown directly on Si substrates with minimal use of expensive materials.[129–131] The high strain relaxation also significantly reduces lattice matching constraints

on the nanowire itself, which has facilitated growth of a large range of defect-free heterostructure combinations not possible for planar structures, e.g. Si/Ge, GaAs/InAs. This can be done in both the radial[132] and axial[133] directions, or even a combination of the two[134] to facilitate new device functionality. This has opened up a wealth of possibilities for band-engineering that has been exploited for quantum system generation, novel transistor devices and optoelectronic devices.[124,135] In particular, nanowire solar cells and LEDs are already being considered for commercially viable technologies.[136–138]

1.5.3 Nanowire FETs

The geometry of nanowires offers a particular advantage towards FET development; they can be used as the basis for a 'gate-all-around', or 'wrap-gated' transistor. A gate that wraps around the transistor channel can apply the electric field symmetrically from all sides, in contrast to uni-directional planar devices. This helps to maintain a low SS and I_{off} in short channel devices.[4] Wrap-gated nanowire FETs (NWFETs) were first realised with as-grown nanowires standing vertically on the growth substrate, as in Figs 1.21(a/b).[23,139,140] Optimisation of this structure for InAs nanowires has lead to switching operation at frequencies well into the GHz range.[141,142] While the vertical configuration is the choice for efforts towards industrial deployment, it is time consuming to contact and study individual nanowires in this way. For fundamental research purposes, it is actually more more convenient to break the nanowires off the growth substrate and deposit them horizontally on a secondary substrate.

One immediate advantage to using the horizontal/lateral orientation is that the substrate itself can be used as a global gate, without the need for a wrap-gate.[144] Typically the substrate is highly doped Si, insulated from the nanowire by a SiO_2 layer, and V_G is applied directly to the substrate (Fig. 1.21(c)). The simple fabrication makes substrate gating a popular choice for fundamental research, whether it be a simple materials characterisation or probing embedded quantum dots. In many cases a substrate gate can be sufficient, but in general it is not an ideal

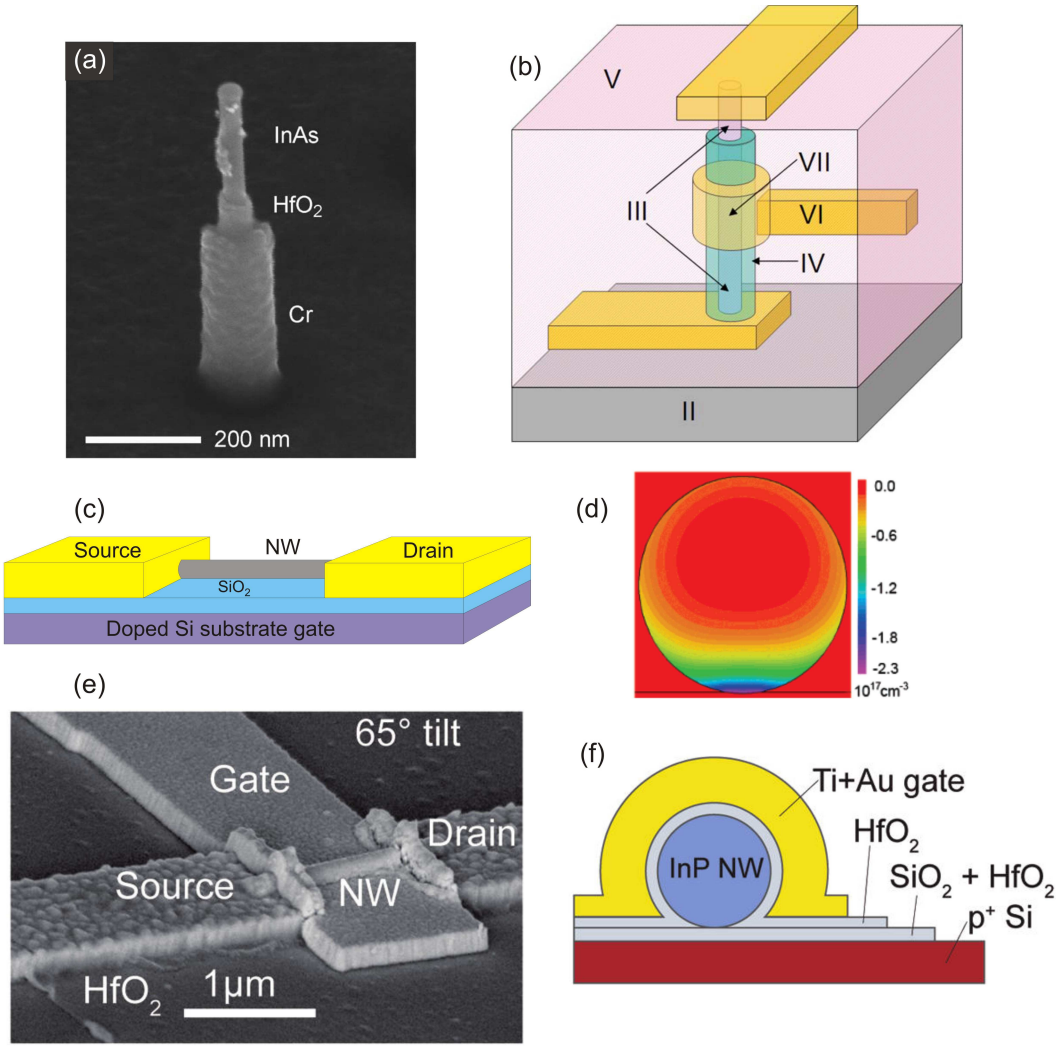

FIGURE 1.21: (a) Scanning electron micrograph of vertical InAs nanowire with Cr wrap-gate insulated by HfO_2. (b) Schematic of completed vertical wrap-gate nanowire transistor with: II; Si substrate, III; ohmic contact to source/drain, IV; HfO_2 layer, V; polymer filling layer to facilitate deposition of top contact, and VI; Cr wrap gate. (c) Schematic of substrate gated lateral NWFET. (d) Cross-section of non-uniform electron density (colour scale) in a substrate gated NWFET. (d) Scanning electron micrograph and (e) schematic cross-section of an omega gated lateral NWFET. (a/b) from Ref. 23, (d) from Ref. 143, (e/f) from Ref. 19.

strategy. First, there is no local control over individual nanowires on the same substrate, let alone the possibility of multiple gates on the same nanowire. This is essential to increase transistor density and generate and manipulate quantum systems with high precision.[135,145] Secondly, the low dielectric constant of SiO_2, combined with the fact that it is usually 100 nm thick to insure against breakdown, means large voltages $\sim$ 10 V or more are required to fully deplete the

nanowire.[22,30,145,146] The accompanying large subthreshold swings of $SS \sim 1$V/dec are clearly not optimal for efficient, low power operation. Thirdly, gating a device with radial symmetry from only one side invariably introduces a non-symmetrical potential and therefore non-symmetrical depletion/enhancement of charge carriers.[143] Figure 1.21(d) shows that the charge carriers are pushed against the rough, unevenly charged nanowire surface on one side, reducing mobility and presenting a non-uniform system.

Local gating can be achieved by back gates patterned prior to nanowire deposition, or post-deposition patterned 'omega' gates on top of the nanowire (Figs 1.21(e/f)). Omega gates give much improved gating – in some cases with subthreshold swings approaching the thermal limit[19,147] – and the local patternability of both back- and omega-gates has facilitated quantum system engineering.[148,149] However, the fact that both approaches still yield a non-uniform radial potential highlights a desire for lateral wrap-gating. Despite this, realising lateral wrap-gated nanowires proved elusive as it was not clear how to easily fabricate a wrap-gate in this orientation.[145] I will discuss this in more depth in Chapter 2, but the eventual fabrication required an innovative use of chemical etchants in work by Kristian Storm and others from Lund University, Sweden collaborating with my supervisor Adam Micolich.[145] Stepping this up to multiple lateral wrap-gates entailed a non-trivial re-think of the entire fabrication process, which I worked on during my research for this thesis. In doing so, we demonstrated the first laterally-oriented nanowire FETs with multiple wrap-gates.[29] We also showed that laterally-oriented devices with multiple wrap-gates may have scalability advantages over vertical structures because once the initial step is made from one to two gates, adding more doesn't entail additional fabrication steps. This means it takes the same time to fabricate two, three or four wrap-gates. By contrast, each gate added to a vertical NWFET entails a repetition of fabrication steps, which adds a time and yield cost. This is discussed in detail in Chapter 4.

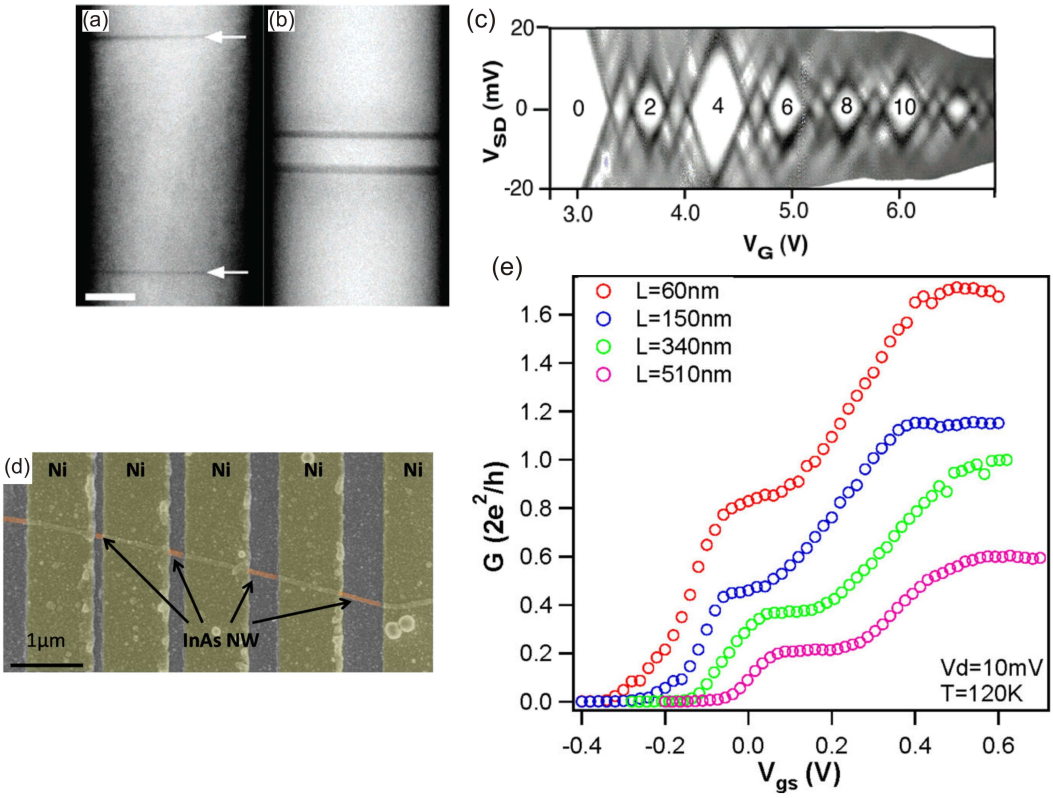

FIGURE 1.22: (a/b) Dark-field scanning transmission electron microscopy image along the axis of an InAs nanowire with $\sim 3-4$ nm thick InP heterostructure barriers (dark regions). The barriers define InAs quantum dots of 100 nm and 20 nm length. The scale bar depicts 20 nm. (c) Source-drain bias spectroscopy data for a 10 nm dot with V_G applied to the substrate gate. From Ref. 150. (d) InAs nanowire with multiple ohmic contacts defining different channel lengths. (e) Quasi-ballistic transport for different lengths defined in the device in (d). A small amount of scattering events disrupt ballistic transport, reducing the transmission co-efficient and leading to steps $G < 2e^2/h$. The step height increases as the channel length approaches the mean free path length. From Ref. 151.

1.5.4 Quantum systems in nanowires

The radial confinement of nanowires and the ability to grow heterostructure barriers resulted in the very swift realisation of embedded quantum dots based on, e.g., InP barriers in an InAs nanowire. This included single-electron transistors, few-electron quantum dots and double dots with signatures observable up to $T = 60$ K.[150,152,153] The ability to easily define dots in materials like InAs and InSb makes nanowires of great interest in addressing electron spins for quantum

computing applications due to the comparatively large effective g-factor g^* of electrons in these materials. The effective g-factor is the constant of proportionality for the magnitude of spin-splitting in a magnetic field of otherwise degenerate energy states.[63] Addressing individual spins with high accuracy at low B is aided considerably by materials by a large g-factor, e.g., $g^* = -14.7$ for bulk InAs. Additionally, the g-factor can be tuned with quantum dot size[154] and occupation level.[81,155] This opens up the possibility for multiple individually addressable dots on the same nanowire by selecting different g-factors. For quantum dots in InSb nanowires, g-factors of up to 70 have been observed.[81]

By contrast, ballistic 1D transport in nanowires has been elusive despite the natural radial confinement on the order of $20 - 100$ nm. Initial indications suggested a Coulomb staircase superimposed on a disordered background,[156] with recent measurements showing this background could be partially overcome by suppressing backscattering *via* an applied magnetic field.[157] Similarly, there exists evidence for diffusive,[158,159] and quasi-ballistic 1D sub-bands[151,160] – i.e. carriers undergo scattering events – that with high quality growth, surface passivation and very short channel length ~ 60 nm can approach the ballistic limit.[151] These results in Fig. 1.22 are also promising in that sub-band splitting can be observed at relatively high temperatures $T \sim 120$ K. Nevertheless, manipulation of a truly robust ballistic 1D system has not been convincingly achieved in nanowires to date. The continued drive towards 1D ballistic transport in nanowires is due to some interesting potential applications in which nanowires are predicted to play a pivotal role. One example is the search for Majorana fermions, particles that are their own anti-particle. They are predicted to arise in a very specific solid-state system that consists of a superconducting contact to one half of a nanowire with underlying 1D transport.[161,162] A second example, there is a long-standing prediction that the figure-of-merit for thermoelectric power conversion should be significantly enhanced by 1D transport in nanowires;[163,164] this latter application is relevant for this thesis and I will discuss this further in the section below.

The problem for ballistic transport in nanowires is that the surface necessarily defines the radial confinement. Since the surface states provide a non-uniform background potential, the confinement is not uniform along the channel length. This non-uniform potential is superimposed on any additional gate potential, meaning the potential is nothing like the ideal smooth, uniform barrier that steadily confines charge carriers. In addition, the electron mobility in nanowires is typically less than 10^4 cm^2/Vs, and mean free paths are expected to be 200 nm or less.[151,157,165] Compare this situation to QPCs in GaAs/AlGaAs heterostructures, where the well defined surface gates can provide a very uniform confining potential to a system with a mobility of $\sim 10^6$ cm^2/Vs and mean free paths over 10 μm. Observing true 1D ballistic transport in single crystal nanowires is likely to require fabrication of gates with lengths $\leqslant$ 200 nm that are located in a region where the surface potential is uniform. A possible alternative is modulation doped nanowires, with a GaAs core and doped AlGaAs shell.[147,166] This would ideally provide the high electron mobility and background potential required for ballistic 1D transport.

1.5.5 Thermoelectrics and nanowires

The direct conversion of heat to electricity and vice versa *via* the Seebeck and Peltier effects has long held interest for applications such as generating electricity from waste heat or solid-state cooling.[167–169] The basic principle is that a thermal gradient ΔT causes charge carrier diffusion from hot to cold, which establishes an open circuit voltage called the thermovoltage V_T.[1] The Seebeck coefficient $S \equiv -V_T/\Delta T$, also known as thermopower, links these two essential properties to quantify the magnitude of the thermoelectric effect. In metals S is only tens of millivolts per Kelvin as diffusion quickly cancels out the carrier imbalance that defines V_T.[169] However, insulators are not an effective solution either since extracting usable power from the device requires that a current flows. In fact, optimising thermoelectric efficiency is a balancing act governed by the thermoelectric figure

[1] I have used V_T for thermovoltage rather than the more commonly used V_{th} to avoid confusion with threshold voltage.

of merit $ZT = S^2\sigma T/\kappa$, where σ is the charge carrier conductivity, T the average temperature of the sample and κ the thermal conductivity.[170] The thermal conductivity of solids consists of phonon and charge carrier (electron/hole) contribution $\kappa = \kappa_{ph} + \kappa_{eh}$. The balancing act arises because S, σ and κ are almost always interlinked. S and σ both need to be high to extract power from the device, but as illustrated by the comparison between metals and insulators, S and σ are mostly inversely proportional to each other. Similarly, κ should be low such that the thermal gradient ΔT is not equalised across the material. However, a high carrier conductivity σ tends to result in a high carrier thermal conductivity κ_{eh} by the Wiedemann–Franz law, $\frac{\kappa}{\sigma} = LT$, where L is the Lorenz number (a constant). The difficulty in maximising ZT in bulk materials generally results in $ZT < 1$ at room temperature. Values of 3 of more are considered to be necessary for a thermoelectric material to provide efficient conversion in practical applications.[169]

At the fundamental research level, nano-structures, and in particular nanowires have been a strong focus in obtaining a useful $ZT > 3$. This is for two reasons: Firstly, heat flow is disrupted by the proximity of the rough surface, giving a much reduced κ that is largely independent of S and σ.[172] Secondly, 1D quantum confinement is predicted to result in increased $S^2\sigma$ for nanowires based on tellurides and III-V semiconductors.[163,164] This relies on operating the device just below the lowest sub-band, where transport only takes place from the hot to cold reservoir.[163,173] Despite this promise and a handful of results indicating small enhancements,[159,174] significant ZT enhancement *via* 1D confinement in nanowires has been frustrated by surface disorder prohibiting clear observation of 1D ballistic transport. Additionally, the requirements of very thin nanowires with diameters < 10 nm[163,164] and careful Fermi level control[163,171,173] are rarely addressed properly.

However, recent work by Wu *et al.*[171] has highlighted that the precise restrictions of the 1D regime are not necessarily required to achieve significant $S^2\sigma$ enhancement. In fact, this work uses the disordered nanowire surface as an advantage,[171] as the disorder potential essentially consists of a number of barriers along the nanowire channel.[175] This means that electron transport can be thought of as a mixture of propogating modes coupled to quantum dot-like states. This was shown recently

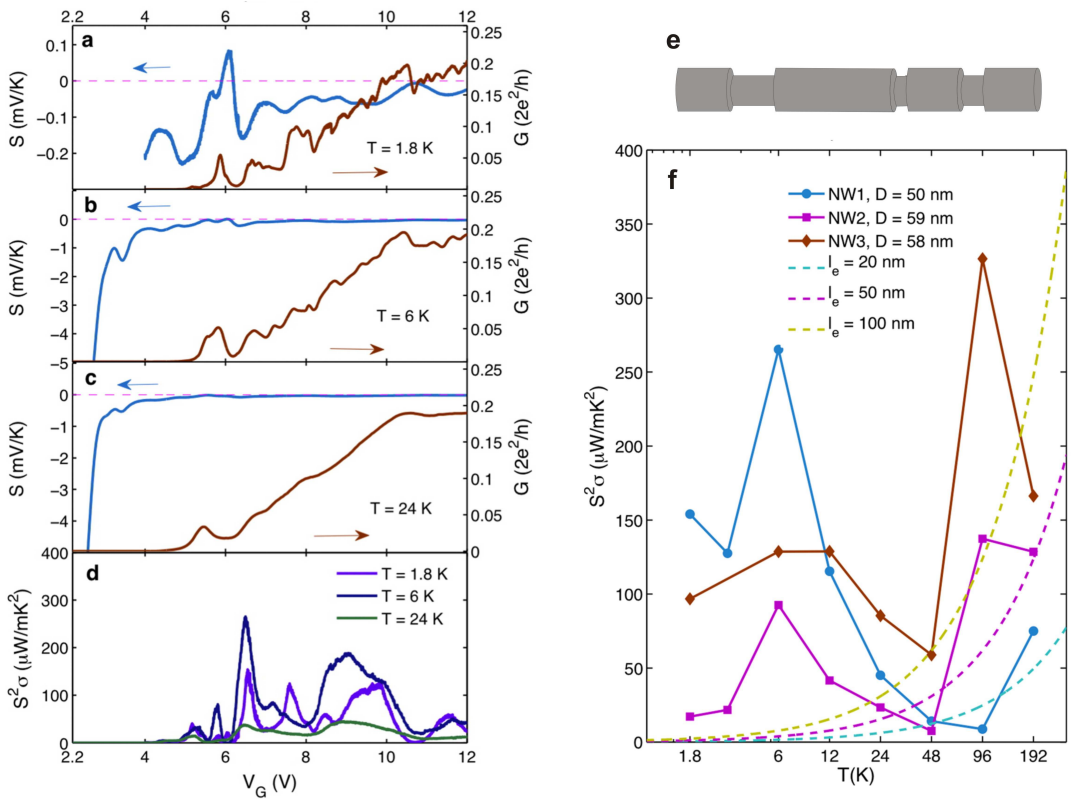

FIGURE 1.23: (a/b/c) Seebeck coefficient S and conductance G vs V_G for a substrate-gated InAs nanowire at $T = 1.8, 6, 24$ K. The fluctuations in G are quantum interference effects due to the coupling of disorder defined quantum dot states with propagating modes. The oscillations in S are also suggestive of quantum dot signatures, since they approximate $\frac{\partial G}{\partial V_G}$ and undergo sign changes. (d) The oscillations in S and G produce peaks in $S^2\sigma$ over a wide V_G range. (e) Representation of the radial confinement potential for nanowires at low temperature. (f) Peak value of $S^2\sigma$ for three different nanowire devices at different T (dots) compared to $S^2\sigma$ for bulk InAs (dashed lines). $S^2\sigma$ is enhanced in nanowires for $T \leqslant 24$ K. Adapted from Ref. 171.

both experimentally[171] and theoretically[176–178] to enhance $S^2\sigma$ at $T < 20$ K. Figure 1.23 shows the advantage is that the enhancement occurs over a wider range of carrier concentration. This relaxes the strict requirements on Fermi level positioning demanded in the 1D case and broadens the scope for practical applications where careful positioning of the Fermi level in large device arrays is not typically feasible.[171,173] Although, some optimisation will be required to exploit this effect at higher temperatures.

Beyond seeking materials with high thermoelectric efficiency, thermovoltage measurements hold interest as an electrical characterisation tool. Since V_T is related

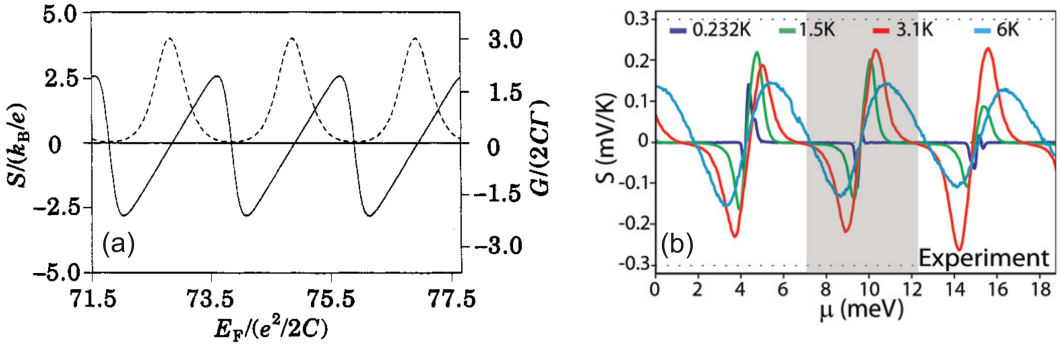

FIGURE 1.24: (a) Seebeck coefficient $S = V_T/\Delta T$ in the sequential tunnelling regime (solid trace/left axis) and conductance G (dashed trace, right axis) as a gate voltage sweeps quantum dot states through the Fermi level. The G resonances correspond to allowed transport through the discrete dot energy levels. V_T and S follow the energy of the closest dot level. From Ref. 179. (b) Experimental data of S vs gate potential μ V_G at average temperature $T = 0.232, 1.5, 3.1$ and 6 K. Reducing temperature drives S (and therefore V_T) towards a derivative-like lineshape. From Ref. 180.

to the average energy of carriers in a quantum system it can contains more information than conductance G.[179,181–184] For sequential tunnelling in quantum dots at $V_{sd} \sim 0$, the thermovoltage dependence on plunger gate voltage follows the rise of the closest dot level, $V_T(V_G) \sim \mu_N - \mu_S$. Here, μ_S and μ_N are the chemical potentials of the source contact and the dot level with energy closest to μ_S, respectively. This produces a sawtooth function that crosses $V_T = 0$ when the dot/contact levels align, and switches sharply back to negative V_T halfway between I_d resonances (see Fig. 1.24(a)). V_T also can contain fine structure, carrying information about the excitation spectrum of the dot that is absent from a simple G measurement.[179,181,182] When higher order tunnelling processes start to dominate transport, V_T makes a smooth transition towards a derivative-like lineshape $V_T \sim \frac{1}{G}\frac{\partial G}{\partial V_G}$, shown in Fig. 1.24(b).[180,183,185] Employing quantum dots or QPCs can also facilitate accurate measurement of the electron temperature, which is often distinct from the lattice temperature at low T.[186–188] In classical/diffusive systems, V_T can be used to distinguish between carrier types[189] and estimate carrier mobility and concentration.[190,191] This is particularly important for nanostructures where methods such as the Hall effect are problematic.[192]

In Chapter 5, I present results that use an organic polymer electrolyte gate dielectric to set base-line carrier density and modulate the disorder potential in an InAs nanowire for low T measurements. I show this can increase the influence of quantum dot-like states. This suggests this could be a viable method for both setting an optimal disorder potential and carrier concentration for thermoelectrics. I also use complementary G and V_T measurements to show that V_T carries extra information about multiple quantum dot systems.

1.6 Organic electronics and ionic transport

An exciting new direction in electronics research involves the use of organic materials. They offer a wealth of new functionalities not readily facilitated by inorganic materials such as Si and III-V semiconductors. In particular, organic devices can be deployed on flexible substrates for displays, lighting and plastic electronics.[11] Many of the materials feature novel, easily scalable fabrication methods such as inkjet printing.[193] In addition to electron/hole transport, many biological materials facilitate ionic transport. Ion transport has long been of interest for, e.g., Li-ion batteries, but is also relevant to biological applications.[9–11,194] Using ions in an electrolyte to facilitate gating of organic transistors and inorganic nanostructures is gaining attention where traditional metal/oxide methods are incompatible, or where the organic route provides additional functionalities.[8] Liquid electrolytes were first used at Bell labs to demonstrate Fermi level control in semiconductors[195] and continue to be employed in some specialised situations. However, polymer electrolytes in the solid or gel phase are most popular as they are more easily contained within device architecture.

1.6.1 Polymer electrolytes

A polymer electrolyte (PE) consists of mobile ionic species – often derived from a salt such as $LiClO_4$ – hosted in a polymer backbone, such as poly(ethylene oxide)

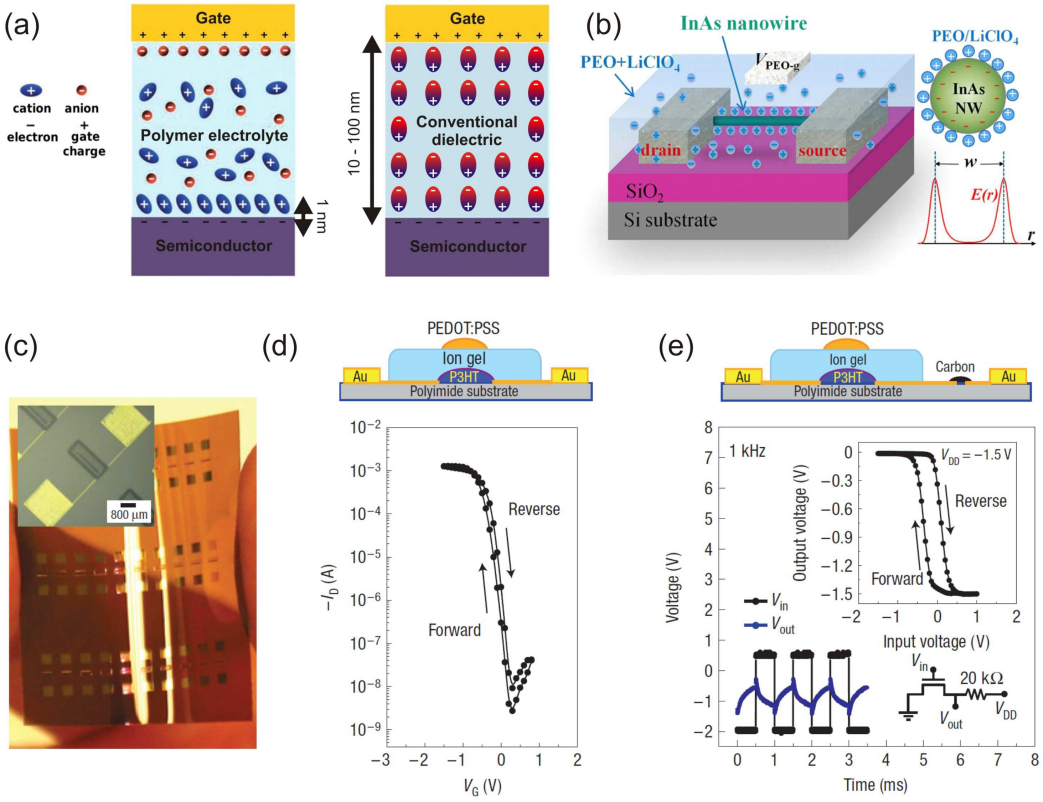

FIGURE 1.25: (a) Operation of a polymer electrolyte gate dielectric. Positive charge on the gate drives ionic motion to establish an electric double layer 1 nm away from the semiconductor channel. This contrasts with a conventional dielectric where the gate voltage is dropped over 10 - 100 nm by dipole alignment. Adapted from Ref. 8. (b) Ionic motion provides a radially symmetric potential to nanowires, facilitating wrap-gating. The PE layer covers the source/drain and entire substrate due to previous patterning resolution restrictions. From Ref. 196. (c) Flexible array of organic transistors. (d) The channel is an organic semiconductor P3HT, with an ion gel gate dielectric which facilitates a operating range $\Delta V_G < 2$ V. (d) An inverter based on the transistor in (c) with a carbon resistor load. Switching occurs at 1 kHz, but fidelity is low. From Ref. 197.

(PEO).[8,198] Figure 1.25(a) shows how polymer electrolytes are operated as high capacitance gate dielectrics. Application of V_G to the gate electrode causes dissociated Li^+ and ClO_4^- ions to move through the polymer *via* chain relaxation.[199–202] This results in electric double layers (EDL) at the channel/PE and PE/electrode interfaces. EDL formation ideally transfers the gate charge to approximately 1 nm away from the semiconductor channel, meaning V_G essentially drops across a 1 nm thick dielectric.[203] At this distance, the dielectric constant of an EDL becomes independent of the host material, and takes a value $\epsilon_r \sim 10 - 20$. The high ϵ_r

and low dielectric thickness produces a large capacitance and strong electric field which facilitates very effective gating.[8]

These features made polymer electrolytes favourable dielectrics for organic transistors. Organic surfaces typically have a high oxide content which produced non-ideal surface/interface effects when in contact with oxide dielectrics, similar to the issues seen in III-V semiconductors (recall Sec. 1.3.2). The solution processability of polymer electrolytes also improved their compatibility with organic channels.[8] Using PEs made it possible to reduce the V_G operating range to 1 or 2 V, down from the tens of volts required using other architectures (see Figs 1.25(c/d)).[197,204,205] PEs were also used to induce very high carrier densities to dramatically improve device conductivity.[203,206–208] In some cases this was assisted by the anions passing into the organic transistor channel and doping it; an additional functionality not possible with inorganic materials. Incorporating the salt-based solid electrolytes in industrial devices was hampered by the slow switching speed.[8] This arises due to the fact that EDL formation takes a finite time, limited by the ionic conductivity. The relatively rigid chains in, e.g., PEO at room temperature results in a low ionic conductivity and slow switching speeds.[201,202] The desire to increase switching speed led to exploration of ion gel gate dielectrics,[197,209–211] which consist of ionic liquids such as 1-ethyl-3-methyl imidazolium bis(trifluoromethane sulfonyl)imide gelated by polymerisation of, e.g., polymethyl methacrylate (PMMA) or block co-polymers.[212–214] Ionic liquids on their own have a very high conductivity, and gelating them with $< 10\%$ polymer ensures orders of magnitude higher conductivity at room temperature compared to salt-doped PEO, facilitating faster switching speeds (Fig. 1.25(e)).[8,215] However, the low viscosity of ion gels means they are not suited to all applications.

The benefits brought by ionic transport have seen polymer electrolytes applied to nanostructures such as carbon nanotubes[216–218] and semiconductor nanowires.[196,219] Here, PEs also bring the advantage that ions will follow the surface profile of the channel. This provides a simple way to achieve a uniform potential in unusual geometries. In particular, they open a novel route for wrap-gating nanowires (see Fig. 1.25(b)).[196,219] In my research I furthered the use of polymer electrolytes with

nano-materials by demonstrating nanoscale patterning of a PE for the first time. Most previous devices using nanostructures have used the polymer electrolyte as a continuous thin film that covers the entire substrate, and therefore globally gates all devices on the chip. While inkjet printing,[193,197] photolithography[211] and injection into microfluidic channels[217] have been used to pattern PEs, all of these techniques had resolutions > 1 μm. Broadening the scope for using PEs with nanomaterials requires nanoscale patterning to enable local control of individual devices and the possibility of multiple gates on the same device. Eliminating PE overlap of the source/drain contacts is also important to reduce parasitic behaviours.[8] In Chapter 4 I present a technique to pattern the $LiClO_4$/PEO polymer electrolyte on the nanoscale using electron beam lithography. I used this to fabricate devices with multiple gates on the same nanowire. Fabrication of NWFETs with multiple polymer electrolyte gates required even less steps than the fabrication for metal/oxide wrap-gates. Additionally, the basic performance parameters, e.g., subthreshold slope were comparable. In Chapter 5 we used the PE gate as an external doping strategy for low temperature $T < 4$ K measurements of an InAs nanowire. In addition to setting the base-line carrier density we found that the PE gate could strongly alter the background potential and generate quantum-dot like systems.

1.6.2 Proton transport and biological applications

One area that organic electronic devices have found great application in is interfacing with biological systems. Biological signalling occurs *via* ions and protons, rather than the electronic signals of manufactured electronics. Interfacing with these systems requires transduction of ionic/protonic signals into electronic ones that can be read out *via* conventional electronics.[9–11,194] Proton signals in particular are central to a number of important biological processes.[220] In solid state organic materials with high water content, water molecules can form proton wires where H^+ hops between H_2O sites in response to an external field, by the Grotthuss mechanism. In other materials they proceed by chain relaxation, as

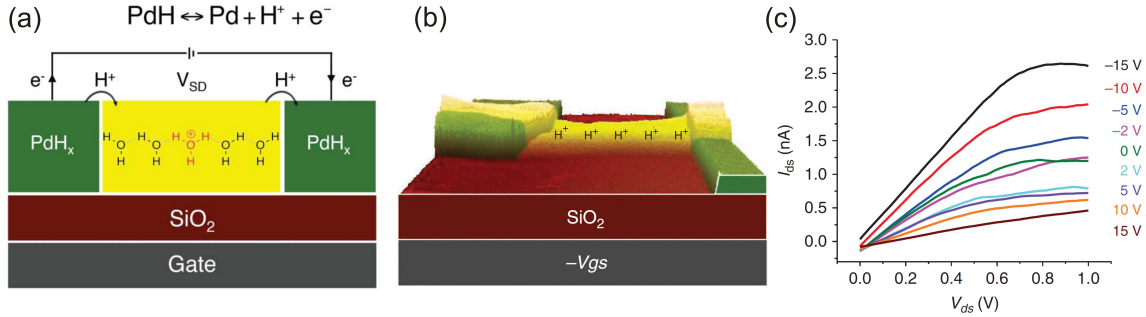

FIGURE 1.26: (a) Schematic of a protonic field-effect transistor. PdH_x contacts inject and collect H^+ ions, which hop along hydrogen bonded water chains that act as proton wires. (b) Combined AFM/schematic of a proton transistor with maleic–chitosan proton channel. The backgate modulates the H^+ concentration in the channel. (c) More negative V_G (colour) causes a higher proton current I_d. Adapted from Refs. 220 and 223.

for Li^+ in PEO.[11] In terms of sensing proton currents, direct proton-to-electron and electron-to-proton transduction can be facilitated by PdH_x in contact with the proton conductor.[220–222] Figure 1.26(a) shows that applying a bias to an external circuit causes a chemical reaction at the injection contact, such that $PdH_x \rightarrow Pd + H^+ + e^-$, with the proton injected into the channel and the electron entering the external circuit. The reverse occurs at the collecting contact, and a proton current is detected.

An interesting expansion of this idea is a proton-channel field-effect transistor (Figs 1.26(b/c)). It consists of a proton conducting maleic–chitosan channel between two PdH_x contacts and a doped Si substrate gate that is used to electrostatically deplete or accumulate protons in the channel.[220] A complementary device has been constructed using OH^- as 'proton holes', and the junction between the two materials behaves like a $p-n$ junction.[223] In a similar vein, *npn* and *pnp* ionic bipolar junction transistors based on the organic semiconductor PEDOT:PSS and electrolyte interfaces have been fabricated.[224,225] These devices are aimed at selective drug delivery more than ion-to-electron transduction.

A more general method for ion/proton-to-electron transduction involves using FETs with electron/hole channels that are sensitive to changes in the ionic environment. This can occur in a couple of ways; the ions may cause a chemical

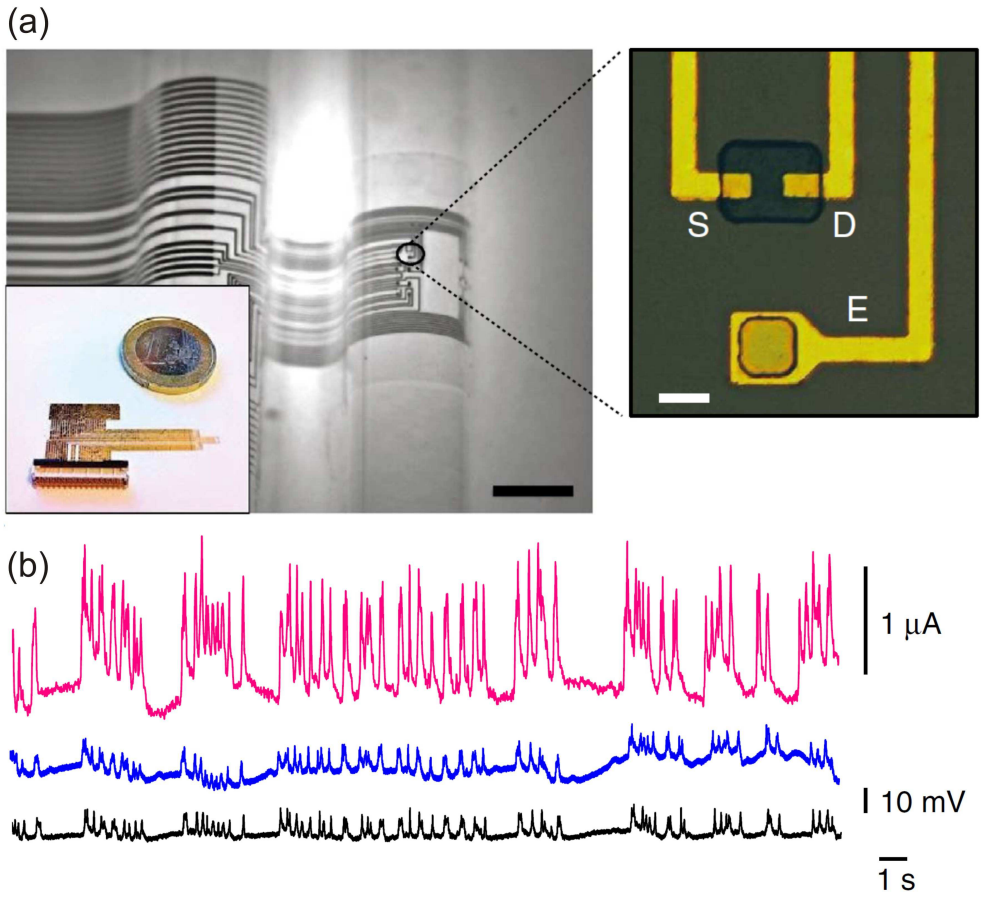

FIGURE 1.27: (a) Organic transistor channel (between source and drain S and D) and metal electrode G used to sense neuron signals. (b) Current through the channel (pink) and potential at two nearby electrodes (blue and black) responds to neuron signals in a rat brain. Signals have been normalised to the noise level, illustrating the better signal-to-noise ratio of the organic transistor. From Ref. 226.

interaction at the surface that alters the surface charge state, changing the current in the channel. These ion sensitive FETs (ISFETs) are used to detect pH changes in solution.[227,228] Sensing may also occur by simple field-effect, without a chemical reaction. These devices essentially operate like the polymer electrolyte gated transistors; a signal causes polarisation of ions within an electrolyte dielectric, gating the channel.[194] Alternatively, the biological sample may be placed directly on top of the channel. An exciting strand of this research involves engaging with neuron firings; Fig. 1.27 shows data from an organic transistor placed directly on a rat brain. The spikes correspond to neural signal events. Transistors

offer a much higher signal-to-noise ratio than more commonly used metal electrodes due to their inherent ability to amplify small signals.[226] In this particular device the ions permeate the semiconductor channel and dope it. It is also possible to turn this around and eject ions from the channel. These pass through a polymer electrolyte to trigger the neuron.[229] Such devices could form a platform for stimulating and detecting neural responses on chip.

A number of steps are needed to establish viable proton to electron transducer circuits. Amplification of the biological signals at the source is of great interest; this would have increased signal-to-noise compared with amplification using external circuitry. Complementary *n*- and *p*-type transducers coupled to the signal would provide the most effective amplification. *p*-type organic transducers with high-fidelity kHz operation have been made,[230,231] but manufacturing complementary *n*-type devices with the same performance is difficult. Additionally, switching speed may ultimately be limited by the low electron/hole mobility $\mu_{eh} < 1$ cm^2/Vs of the organic transistor channels.[11] This has seen renewed interest in using nanowires: the large surface/volume ratio offers scope for enhanced signal output,[194,228] and their size is suited for the accurate detection of biological events.[227,232] In Chapter 6 I present results suggesting that nanoscale patterned PEO supports proton transport with an unusually high conductivity. I use devices featuring PEO dielectrics without salt doping to simultaneously explore the properties of proton conduction in PEO and use them as a proof-of-principle for III-V nanowires as effective ion/proton-to-electron transducers with both *n*-InAs and *p*-GaAs channels.

1.7 Summary

This chapter outlined the physics and previous research underpinning the results presented in this thesis. Included was a description of the field-effect transistor and how the field-effect in general is a powerful tool for generating and probing various

systems, e.g., low-dimensional quantum systems and biological materials. Evaluating emergent technologies in a research usually requires overcoming materials complications. Surface states and dopants play a central role to the operation of both *p*-AlGaAs/GaAs heterostructure devices and nanowires. Both cause gate instability and hysteresis and can influence the properties of quantum systems. The goal is to mitigate their influence, work within the provided limits, or think about how they could be used to provide additional functionality. Examples of each are demonstrated throughout Chapters 3 - 6. In the next chapter I present the device fabrication methods and measurement techniques used during my research.

Chapter 2

Methods

2.1 Fabrication and micro-/nano-lithography background

Fabrication of the micro-/nanoscale devices in this thesis was enabled by lithography processes that use thin, patternable polymeric films known as 'resists'. The lithography proceeds by defining micro-/nanoscale windows in the resist layer to allow access to the substrate in only these defined regions. Subsequent deposition of thin layers of material (e.g. metals and oxides) or chemical etches are then only applied to the substrate in these windows. The resist are patterned by exposing selected areas of the resist to high energy photons (photolithography) or electrons (electron beam lithography), which causes either the scission or crosslinking polymer chains, depending on the resist properties. The exposed areas become either more or less soluble in particular 'developer' solutions. The behaviour of polymer chains under irradiation determines the tone of the resist:

- Positive-tone resist: polymer chain scission occurs under irradiation, increasing the solubility of the exposed regions.

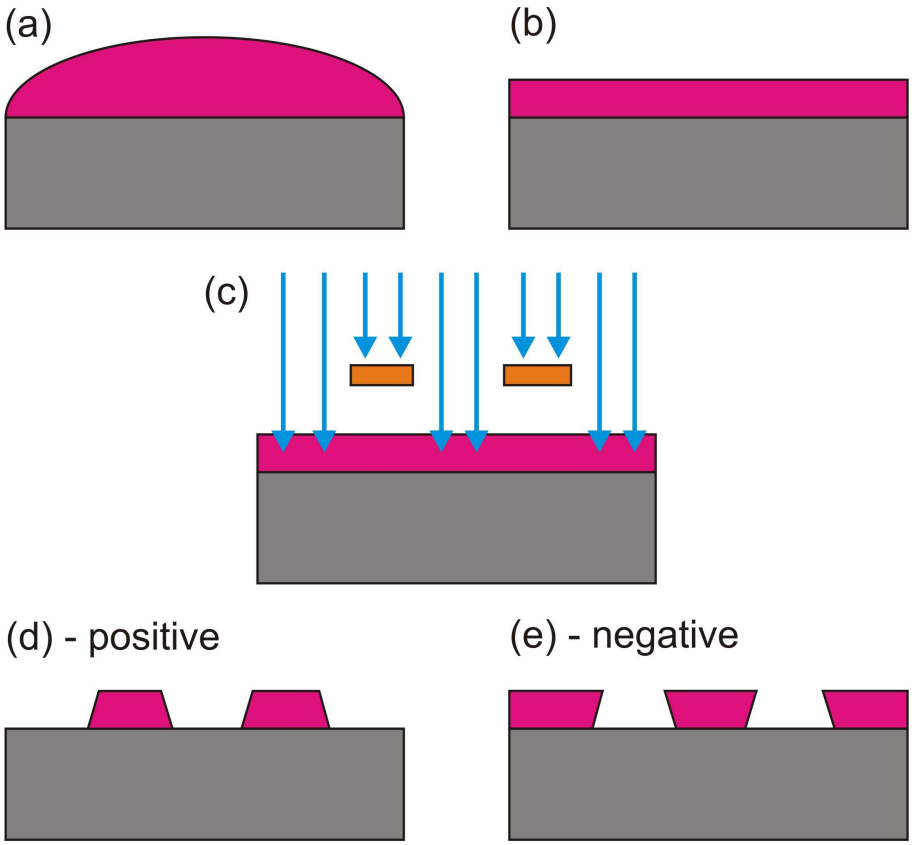

FIGURE 2.1: Photolithography process. (a) Polymeric resist (pink) is deposited onto substrate (grey). (b) Spinning and baking results in a thin film with thickness $\sim 1 - 2$ μm. (c) Sample is exposed to UV light through a chrome-on-glass mask (orange). (d) UV irradiation breaks polymer chains in a positive resist. Exposed regions are removed in developer solution, transferring the mask image to the resist layer. (e) UV irradiation cross-links polymer chains in a negative resist. Exposed regions remain after development, transferring the negative image of the mask.

- Negative-tone resist: polymer chains are cross-linked under irradiation, strengthening these regions against dissolution.

The developer is chosen such that it dissolves the regions with the weakest chains; the exposed (unexposed) regions for positive (negative) resist. This creates the windows in the resist layer through which the selective lithography takes place *via* etching or materials deposition.

2.1.1 Photolithography

Photolithography utilises resists that are sensitive to UV radiation. Selectivity is usually provided by a pre-patterned chrome-on-glass mask, where the chrome sections block the underlying resist from UV exposure. The resists used in this thesis were MicroChem S1813 (positive tone)[233] and AZ nLOF2020 (negative tone),[234] which both consist of a polymer blend dissolved in a solvent to facilitate spin-casting. Figure 2.1 illustrates the photolithography process, which followed the steps:

1. A drop of the resist was spin-cast onto the sample substrate to form a thin film. S1813 was spun at 5000 rpm for 60 s, and AZ nLOF2020 was spun at 10000 rpm for 60 s.

2. The sample was baked on a hotplate at 110°C for 60 s to evaporate the solvent. The final resist thickness was $\sim 1 - 2$ μm.[233,234]

3. The sample was exposed to UV radiation with power density 10 mW/cm^2 through a chrome-on-glass mask. Mask alignment and UV exposure was performed using a Quintel Q4000 with exposure times of 6.5 s for S1813 and 4 s for nLOF2020.

4. A post-exposure hotplate bake at 110°C for 60 s was conducted for AZ nLOF2020 only. This strengthened the unexposed regions of this resist.

5. Development was performed in solutions of 2.38% tetramethylammonium hydroxide (TMAH) in H_2O for 60 s. The process was terminated with a H_2O rinse and the sample was dried with a flow of N_2 gas.

For the positive-tone S1813 resist, the remaining resist is in the pattern of the mask used (Fig. 2.1(d)). For the negative-tone nLOF2020 resist, the removed regions take the pattern of the mask (Fig. 2.1(e)). Note that for any given chrome-on-glass mask, the negative of that mask can be also be created. This means that a nominally identical pattern can be obtained in both resist tones. That is, the

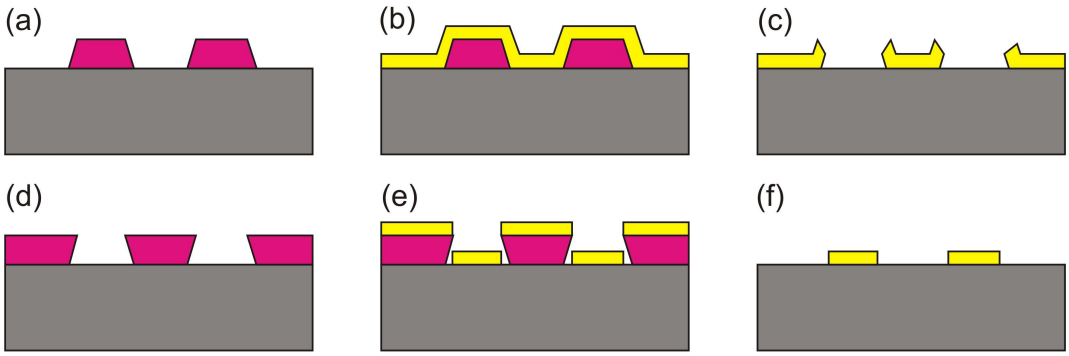

FIGURE 2.2: Metal deposition on a sample featuring (a-c) positive photo-resist with sloped side-walls and (d-f) negative photo-resist with undercut side-walls. (b) Metal deposition on positive resist results in a continuous film at the pattern edges. (c) Lift-off tears the metal, producing poorly defined edges. (e) The undercut profile of negative resist means that (e) the metal is discontinuous at the pattern edges. (f) This results in clean edges on a well defined metal pattern after lift-off.

same pattern is obtained in a negative resist as a positive resist if the negative mask pattern is also used.

The type of resist used depends on practical considerations, since the pattern itself does not determine the resist type. The most common consideration is the differing side-wall profile between the tone types (see Figs 2.1(d/e)). This arises because the UV radiation intensity is greater at the resist surface than at the resist/sample interface.[235] The profile is a particularly vital consideration in the deposition of metal films, pictured in Fig. 2.2. In this process, a $30-200$ nm thick metal layer is deposited uniformly across the sample, adhering to the substrate surfaced only in the resist windows. Completing the metal pattern entails a step known as 'lift-off', where the resist is dissolved by immersion in a solvent such as acetone or N-methyl-2-pyrrolidone (NMP). This removes the resist layer and the metal regions not in contact with the substrate. For lift-off to be effective, the solvent must be able to access the resist layer underneath the metal through discontinuous sections of the metal layer. The undercut profile of the negative-tone resist results in discontinuities of the metal layer at the edges of the resist windows (Fig. 2.2(e)), and therefore facilitates effective lift-off (Fig. 2.2(f)). Conversely, the continuous metal layer over the positive resist prevents the solvent from accessing

the resist layer (Fig. 2.2(b)). This means that lift-off is either completely prevented, or metal tearing at the edges of the pattern occurs (Fig. 2.2(c)). As such, negative photo-resists are commonly used for metal deposition, although strategies do exist to make positive resists compatible with lift-off by, e.g., soaking the resist in chlorobenzene prior to development. The chlorobenzene hardens only the very top layer of the resist and thereby generates an undercut profile.

A second consideration is that the mask usually needs to be aligned to pre-existing features on the sample. This is more easily done if the chrome pattern covers a minimal area on the mask and therefore facilitates a less restricted view of the sample. In applications that have no preferred side-wall profile, e.g., chemical etching, the choice of mask pattern and resist tone is usually guided by the ease of alignment.

The minimum feature size for photolithographically defined patterns is typically $\sim$ 1 μm, limited by the UV radiation wavelength, i.e., hundreds of nanometers, and properties of the resist. Electron beam lithography is used for features requiring a smaller pattern size.

2.1.2 Electron beam lithography

Electron beam lithography (EBL) uses the highly focussed electron beam of a scanning electron microscope (SEM) to selectively modify the crosslinking of chains in the resist at the nanoscale. With some optimisation, patterns smaller than 10 nm can be made in the resist.[237] EBL in this thesis was primarily done using the positive-tone resist poly(methyl methacrylate) (PMMA), with molecular weight MW = 950 k, dissolved in anisole. The anisole content is used to increase the viscosity and modify the film thickness vs. spin speed relationship. Thicknesses of 150 and 300 nm are expected for the MicroChem PMMA-A3 and PMMA-A5 films at the spin speeds used here.[236] PMMA-A3 was used generate the etch pattern for the hole billiard used in Chapter 3, and PMMA-A5 was used for the fabrication of nanowire FETs in Chapters 4, 5 and 6. The EBL process was:

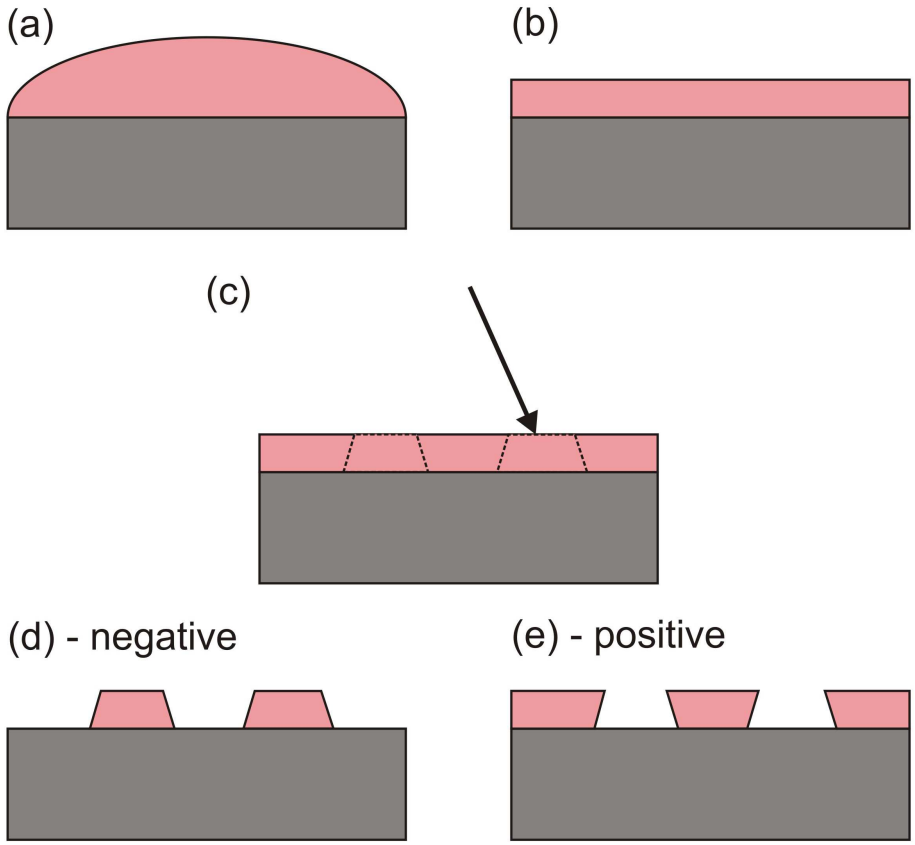

FIGURE 2.3: Electron beam lithography (EBL) process. Resist is (a) deposited and (b) spun onto the substrate to form a film $\sim 50 - 300$ nm thick.[236] (c) The electron beam of an SEM traces out the desired exposure pattern. The proximity effect exposes the underside of the resist outside the region defined by the beam. This results in (d) sloping side-walls for negative-tone resists and (e) an undercut profile for positive-tone resists.

1. The PMMA resist was spun on at 5000 rpm for 60 s.

2. A 3 min/5 min bake at 180°C was used to evaporate the anisole for PMMA-A3/A5, respectively.

3. The desired pattern was exposed using either an FEI Sirion (hole billiard) or Raith 150-Two (NWFETs). For PMMA-A3, an accelerating voltage of 30 kV and electron area dose of $300 - 400$ μC/cm^2 was used depending on feature size. PMMA-A5 was exposed with a 20 kV accelerating voltage and dose of $260 - 520$ μC/cm^2.

4. The pattern was developed by immersion in a 1:3 mix of methyl-isobutyl-ketone:isopropanol for 60 s. The sample was rinsed in isopropanol and dried under an N_2 flow.

There are some notable differences between EBL and photolithography. In EBL, a pattern generator deflects the electron beam directly to the regions of the resist to be exposed rather than using a pre-patterned mask as in photolithography. Typically the EBL exposure is done with the sample in a constant position relative to the SEM aperture, and the beam is deflected to trace out the specified pattern. This means that sections of the pattern are exposed consecutively, rather than concurrently. As a result, exposing larger pattern areas requires a longer time to complete. This contrasts with mask-based processes like photolithography, where the single exposure step takes the same time no matter the pattern size.

A second difference between EBL and photolithography is the resulting side-wall profiles. in EBL, the side-wall profiles arise from the proximity effect, which occurs as follows: primary electrons from the SEM beam penetrate well into the substrate, where backscattering and secondary electron generation causes electrons to be fired back into the underside of the resist.[238] This results in the resist close to the substrate being exposed outside of the areas scanned by the electron beam. Therefore, development produces sloped side-walls for negative-tone EBL resists, and an undercut profile for positive-tone resists like PMMA (Figs 2.3(d/e)). The proximity effect poses a difficulty in the optimisation of many negative-tone EBL resists as it can generate significant pattern broadening. An example of this is discussed in detail in Chapter 4 as part of the results on optimising the resolution of EBL patterned polymer electrolyte thin films.

2.2 *p*-AlGaAs/GaAs device fabrication

The *p*-AlGaAs/GaAs HHMTs in this thesis were fabricated on high quality custom wafers grown using molecular beam epitaxy by Ashish Rai and Dirk Reuter

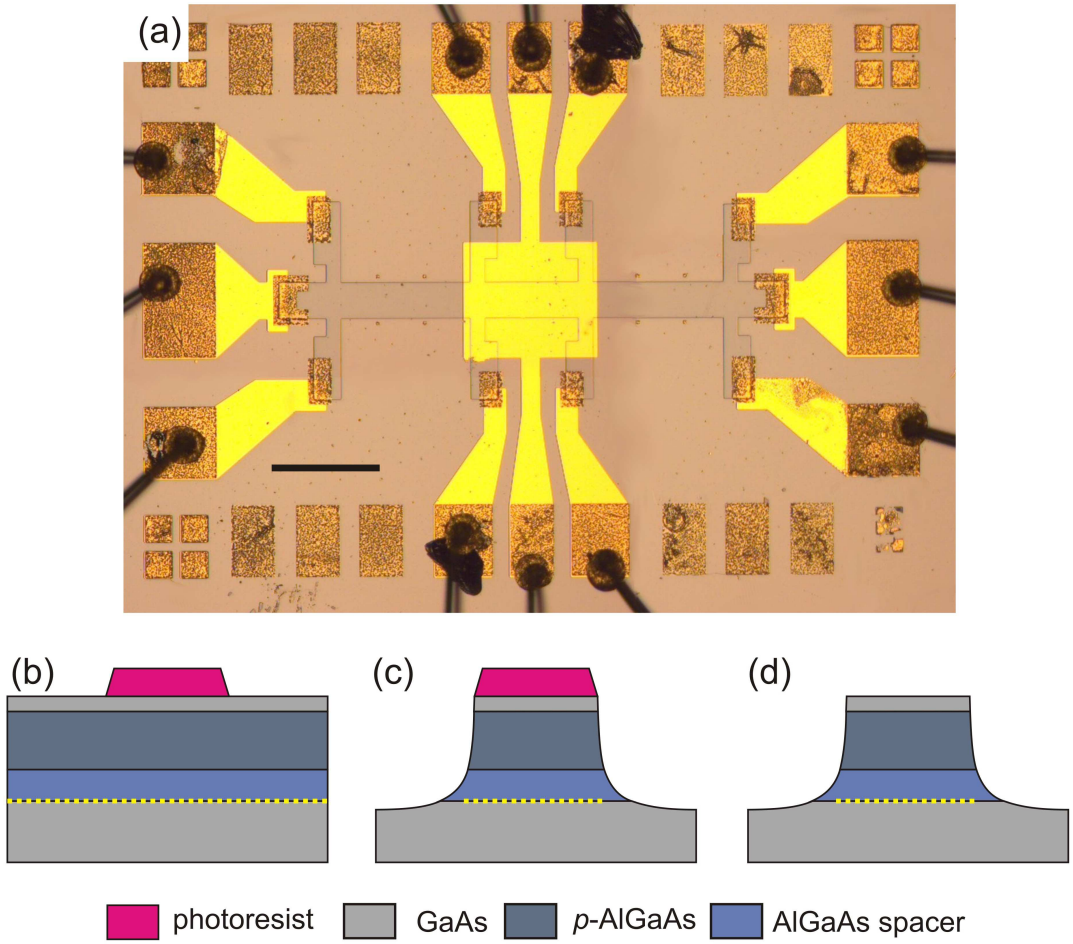

FIGURE 2.4: (a) Optical micrograph of a completed HHMT and (b-d) process used to define the the Hall bar mesa. (a) The HHMT features a central Hall bar mesa (grey outline), AuBe ohmic contacts (grainy gold) on each of the Hall bar arms, and Ti/Au gate (bright yellow square) in the middle of the Hall bar. The AuBe bond pads surrounding the device were defined and deposited as part of the ohmic contact pattern. The Au wires used to connect the device to the chip package can be seen around the outer edge of the image. The interconnects between bond pads and ohmic contacts were deposited with the Ti/Au gate. (b) Cross-section of the heterostructure, including the 2DHG (yellow dotted line) at the AlGaAs/GaAs interface. Positive-tone S1813 was patterned in the shape of the Hall bar on the heterostructure surface. (c) A HF-based solution was used to etch the unprotected heterostructure regions to a depth 10 nm below the 2DHG. (d) The resist was removed using acetone.

in Andreas Wieck's group at Ruhr-Universität Bochum, Germany. Both *n*-type and *p*-type wafers were grown simultaneously on (100)- and (311)A-oriented semi-insulating GaAs substrates supplied by AXT. Epitaxial growth began with 50 nm of undoped GaAs followed by a twenty-period superlattice, where each period consisted of 2 nm GaAs and 2 nm AlAs. The superlattice was included to trap

impurities at these interfaces and thereby reduce the background impurity density close to the 2DEG/2DHG. The active region was then grown, which was a 650 nm undoped GaAs buffer layer, a 35 nm undoped AlGaAs spacer layer, a 80 nm Si-doped AlGaAs layer with Si density $N_{Si} = 3.5 \times 10^{16}$ cm^{-3} and a 5 nm undoped GaAs cap. The Si-dopants settle on Ga sites as a n-type dopant for (100)-oriented growth and As sites as a p-type dopant for (311)A-oriented growth,[105] and provide the electrons/holes for the 2DEG/2DHG that resides at the interface between the AlGaAs spacer and GaAs buffer. All devices in this thesis were fabricated from the p-type (311)A-oriented wafer. The n-type wafer was used without additional device fabrication as part of the surface passivation characterisation in Chapter 3. The hole density and mobility in the 2DHG were measured to be $p = 1.63 \times 10^{11}$ cm^{-2} and $\mu = 1.03 \times 10^{6}$ cm^2/Vs at 4.2 K using the Hall effect.

A completed HHMT is shown in Fig. 2.4(a). The first step in device fabrication was to create a Hall bar mesa that defined the bounds of the 2DEG in the x- and y-directions. This was accomplished using photolithography and wet etching as illustrated in Figs 2.4(b-d). First, positive-tone S1813 resist was patterned into the shape of a Hall bar at the heterostructure surface. The regions of the heterostructure not covered by resist were then etched away by immersion for 37 s in a 2:1:20 solution of buffered HF:H_2O_2:H_2O, where the buffered HF was 7:1 NH_4F:HF. This etch proceeds as the H_2O_2 oxidises the AlGaAs or GaAs material and these oxides are etched away by the HF acid. The heterostructure was etched to a depth of 130 nm, which was 10 nm below the 2DHG. The resist was removed by soaking the device in acetone for 10 mins at room temperature. An isopropanol rinse was used to remove any residual acetone and the sample was dried with N_2 gas.

Ohmic contacts were then added to each arm of the Hall bar to facilitate electrical contact with the 2DHG according to the process shown in Figs 2.5(a-c). Windows at the end of each arm were patterned in negative-tone nLOF-2020 resist, which had the desired undercut side-wall profile. After development, the sample underwent an 'ashing' step, with the purpose of removing any residual resist in the defined windows. Depositing metal onto the surface when there is residual

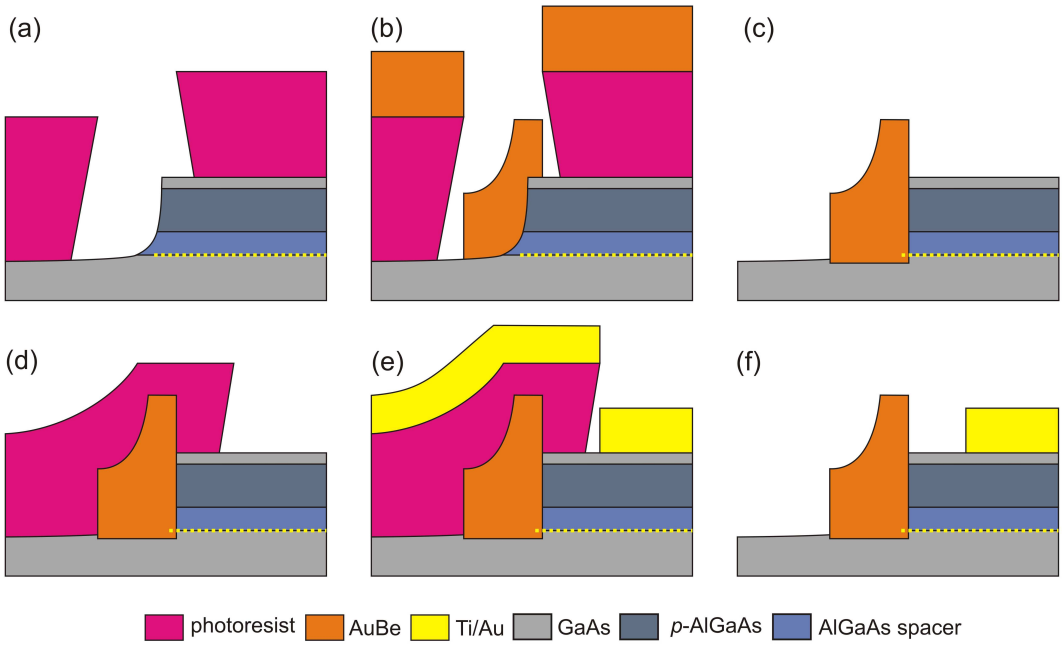

FIGURE 2.5: Cross-section of half of the Hall bar showing the contact metal deposition process. (a) Openings in negative-tone nLOF-2020 were made on each arm of the Hall bar prior to (b) AuBe deposition. (c) Lift-off removed unwanted metal, and annealing caused diffusion of the AuBe into the semiconductor and facilitated electrical contact to the 2DHG. (d) Negative-tone nLOF-2020 was again used to define the pattern for deposition of (d) Ti/Au gates. (e) The device was completed by lift-off in acetone.

resist can result in poor surface adhesion of the metal and high contact resistance. As such, the top few nanometers of resist layer were stripped by a short 30 s etch in an O_2 plasma. This was done using a Denton plasma asher with an O_2 pressure of 340 mTorr and incident power of 50 W. The 150 nm thick 99:1 AuBe ohmic contacts were then deposited by thermal evaporation under high vacuum $\sim 10^{-6}$ mbar. The source material was placed in a tungsten or molybdenum 'boat' facing the sample. The boat was resistively heated by applying a current $\sim 5-6$ A. The source metal first melts and then evaporates, which causes the metal atoms to travel ballistically through the vacuum and solidifying on the sample. Lift-off was performed by soaking the sample in acetone for 10 mins at room temperature before rinsing with isopropanol and drying with N_2.

The as-deposited AuBe forms a Schottky barrier with the underlying GaAs, since the high density of surface states pin the metal Fermi level in the middle of the GaAs band gap (recall Fig. 1.6 in Sec. 1.3.2).[27,46,47] The most common way to

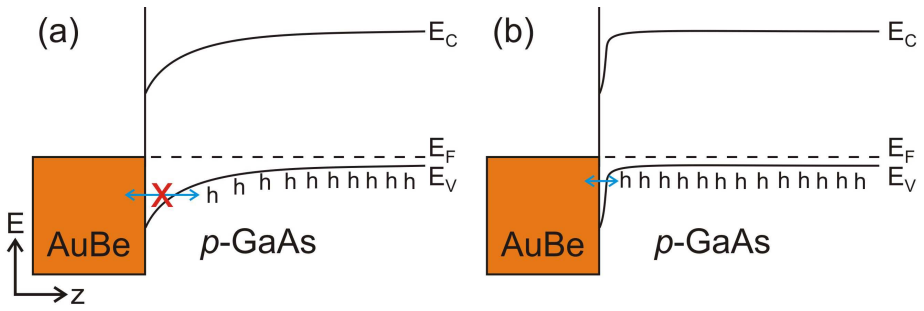

FIGURE 2.6: AuBe interface with uniformly doped p-GaAs (a) before and (b) after thermal annealing, illustrating the the general physics behind ohmic contact formation. (a) The as-deposited metal Fermi level is pinned mid-gap by GaAs surface states, which generates a Schottky barrier that suppresses charge transport across the interface. (b) Annealing causes Be diffusion into the GaAs sub-surface layer, highly doping this region and reducing the Schottky barrier width. The resultant tunnelling transport facilitates linear, low resistance electrical contact between the metal and semiconductor.

overcome the Schottky barrier and obtain linear $I-V$ characteristics is to cause the contact metal and dopant to diffuse into the GaAs via rapid thermal annealing. (Fig. 2.5(c)) For these devices, the contacts were annealed at 490°C for 90 s in a 5% H_2/N_2 atmosphere. The rapid diffusion of Be in GaAs[239] causes the Be to diffuse further than the Au and degenerately dope a thin layer of the GaAs in the vicinity of the metal contact. This does not affect the surface pinning; rather it causes the Schottky barrier to narrow as the high level of doping brings the valence band close to the Fermi level. This is shown in Fig. 2.6. The reduced barrier thickness enhances tunnelling transport through the barrier to the point where electrons/holes can pass between the metal and semiconductor with a low resistance. Ultimately this process results in linear, ohmic contacts.

The final fabrication step was the addition of a gate to modulate current flow in the 2DHG (Figs 2.5(d-f)). The photolithography process was similar to that used for the ohmic contacts. The pattern was defined in a nLOF-2020 resist, and plasma ashing post-development ensured that all resist was removed from the patterned windows. Thermal evaporation was again used to deposit a 15 nm Ti adhesion layer and a 85 nm Au layer. Lift-off was performed using a 10 min acetone soak, isopropanol rinse and N_2 dry. Finished devices were affixed to an LCC20 chip package using a small drop of PMMA or conductive silver paint (Fig. 2.7). The

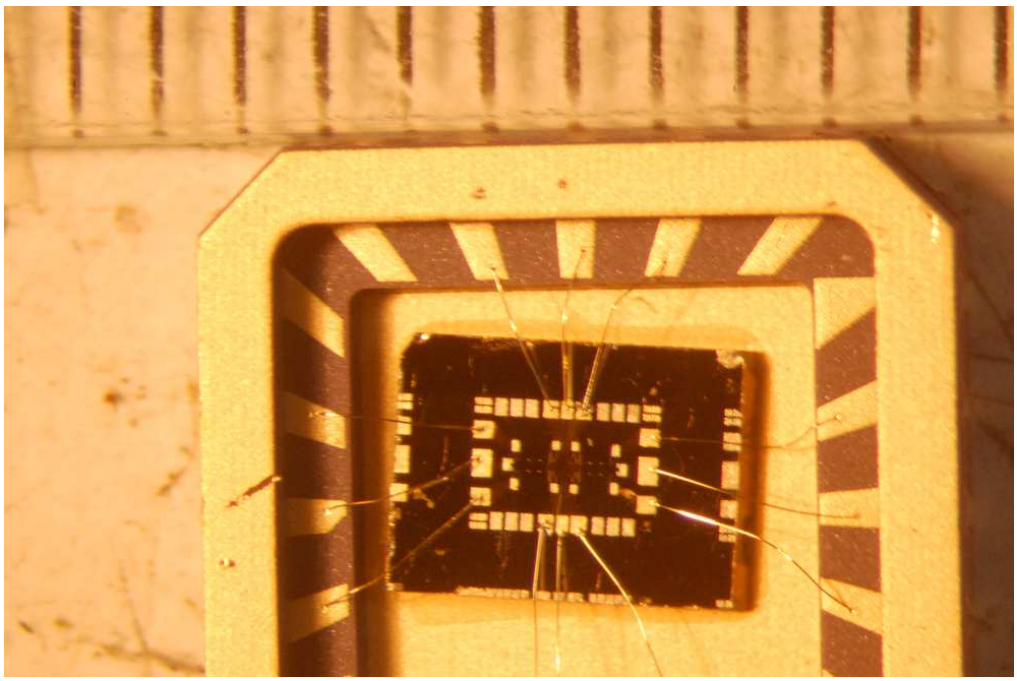

FIGURE 2.7: Finished HHMT bonded in an LCC20 chip package. The Au wire connects the bond pads on the device to the LCC20 pins. The ruler at the top of the image has 1 mm graduations.

LCC20 package features 20 pins that were connected to bond pads on the device by a thin Au wire using a Kulicke & Soffa Au ball bonder. The standardised LCC20 packages fit into the sockets on the measurement systems outlined below, and thereby facilitate interfacing the micro-scale device structures with electrical measurement equipment.

The above process was used to fabricate standard HHMTs. I undertook several variations on this throughout my research. Notably, I fabricated an etched hole billiard with an over-all top gate. Fabrication of this device involved EBL and wet etching to define the billiard trenches prior to deposition of a top-gate that was insulated from the device by a polyimide layer. The specifics of this fabrication will be discussed in Chapter 3. I also applied surface sulfur treatments prior to gate deposition on selected HHMTs; I discuss this now.

2.2.1 Sulfur passivation

The success of $(NH_4)_2S_x$ solutions in passivating low-index GaAs surfaces was outlined in Sec. 1.3.2.1. Effective passivation is achieved in two steps: first, the amorphous surface oxide is removed and secondly, adsorbed S atoms covalently satisfy all dangling bonds such that no electronic states are present in the surface band-gap.[21,44] We investigated applying these treatments to HHMTs in an attempt to mitigate the gate hysteresis and instability in these devices.[24,32] An important consideration in incorporating this treatment to the HHMT fabrication process is that the S-bonded GaAs surface has a low stability in air. Exposure to light and oxygen for approximately half an hour breaks the Ga-S and As-S bonds, and subsequent oxygen adsorption returns the surface to an oxide-covered, unpassivated state.[44,57] As such, we needed to apply the treatment immediately prior to gate deposition, after development and ashing of the gate photo-pattern. After gate deposition, the metal layer is expected to protect the surface from re-oxidisation.[41,62]

We initially considered both aqueous and alcoholic $(NH_4)_2S_x$ solutions as potential passivation treatments.[44] However, I show in Chapter 3 that alcoholic solutions were incompatible with our processing since alcoholic solvents tend to dissolve photoresist. The remainder of the work focussed on aqueous treatments, which left the photoresist intact. All treatments were based on a stock solution, which was was prepared by dissolving 2.4 g of elemental S in 25 mL of 20% $(NH_4)_2S$ in H_2O using a magnetic stirrer at room temperature in the dark for at least 12 hours. Two treatments were applied:

- Strong treatment: 10 min immersion in ~ 3 mL of the stock solution.
- Weak treatment: 2 min immersion in a 0.5% dilution of the stock solution in H_2O.

Both treatments were performed under illumination with the solution at $T = 40°C$.[44,62] These conditions enhance S-bonding and assist in the removal of excess

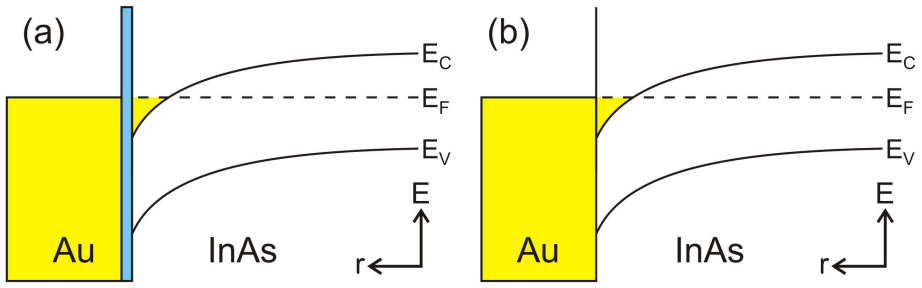

FIGURE 2.8: Radial band diagram for Au metal deposited on InAs nanowire surfaces (a) without sulfur passivation and (b) with sulfur passivation. (a) The native amorphous oxide (blue) increases the contact resistance as it provides an injection barrier. (b) Sulfur passivation removes this barrier and prevents re-oxidisation prior to metal deposition, facilitating low resistance ohmic contact formation.

electrons from the surface.[44] Treated samples were rinsed with H_2O and transferred to the evaporator as quickly as practicable. The evaporator typically achieved a vacuum of < 1 mTorr in under 5 minutes. Gate deposition and device packaging then proceeded as described above.

The sulfur passivation treatment was also applied to InAs nanowires, but with a markedly different purpose. The InAs surface states pin the surface Fermi in the conduction band,[48] in strong contrast to the GaAs surface states that pin the Fermi level mid-gap. For InAs, this aligns the Fermi level of deposited metals directly with the conduction band and facilitates direct injection of electrons. However, the presence of a thin native oxide presents an injection barrier, which increases the contact resistance (Fig. 2.8(a)). Sulfur passivation of InAs nanowires serves to remove the native oxide and re-pin the Fermi level at a slightly different energy within the conduction band (Fig. 2.8(b)). The mono-layer of S atoms preserves this oxide-free surface for long enough to perform metal deposition, which enables the formation of low resistance ohmic contacts.[240]

In this section I describe the fabrication of substrate-gated and wrap-gated NWFETs. These processes form the basis of the advanced gating techniques developed as part of my research. The fabrication processes we developed for multiple wrap-gated NWFETs and polymer electrolyte gated FETs are described in Chapter 4. Nanowire growth was done at Lund University, Sweden, the Australian National

University (ANU), and the Niels Bohr Institute, University of Copenhagen, Denmark. The ANU nanowires were pure wurtzite InAs nanowires, 50 nm in diameter and $3-6$ μm in length, grown using metal-organic chemical vapour deposition. These were used for the polymer electrolyte gated NWFETs in Chapters 4 and 6. Lund University supplied two separate batches of InAs nanowires grown by chemical beam epitaxy. The first had diameter 90 nm and length 3 μm. These were coated with 12.5 nm Al_2O_3 using atomic layer deposition, 16.5 nm of W and 11.5 nm of Au deposited *via* dc sputtering, and a final 12.5 nm Al_2O_3 layer deposited using atomic layer deposition. This batch was used for fabrication of multiple wrap-gated devices in Chapter 4. The second batch consisted of InAs nanowires which were 50 nm in diameter and 3 μm in length. One of these nanowires was used for the device in Chapter 5. The University of Copenhagen supplied Be-doped p-GaAs nanowires grown using molecular beam epitaxy, with acceptor concentration $N_A = 1\times10^{18}$ cm^{-3}, diameter 100 nm and length $5-10$ μm. These were used in for complementary PE-gated NWFETs in Chapter 6.

2.3 NWFET fabrication

2.3.1 Substrate-gated NWFETs

The first step in NWFET fabrication was transferring the as-grown nanowires from the growth substrate to the measurement substrate (Fig. 2.9(a)). This was accomplished using the corner of a clean-room tissue. Lightly tapping the tissue corner on the growth substrate collected the nanowires as they were broken from the substrate. Subsequently tapping the tissue corner on the measurement substrate randomly deposited the nanowires on this surface.

The measurement substrate was based on a degenerately doped n^+-Si wafer which functioned as a global back-gate. The n^+-Si was insulated from the nanowires by a 100 nm thermally grown SiO_2 layer and a 10 nm HfO_2 layer deposited by atomic layer deposition. The latter was included as the slow etch rate of HfO_2 protected

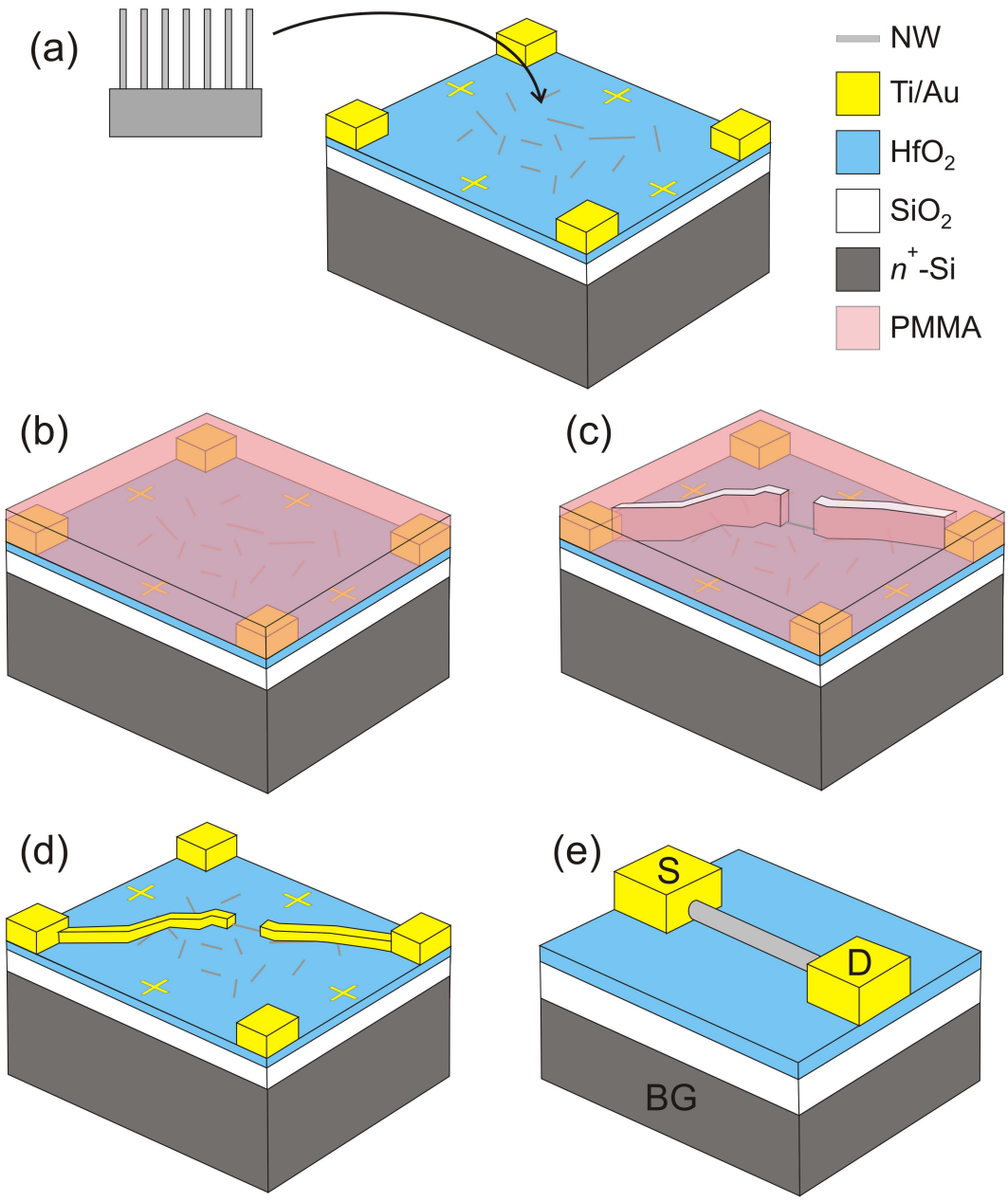

FIGURE 2.9: Fabrication process for substrate-gated nanowire FETs. (a) As-grown nanowires are transferred from the growth substrate to the measurement substrate. The measurement substrate consisted of degenerately doped n^{+}-Si which was used as a global back-gate, insulated by 100 nm of SiO_2 and 10 nm of HfO_2. Substrates were pre-patterned with a series of 100 μm $\times$100 μm write-fields. The alignment crosses were at each side and the Ti/Au interconnects at each corner. (b) The sample was covered in PMMA-A5 for EBL processing. The beam was deflected according to the desired pattern within each write-field. (c) Development removed the exposed regions. (d) Metal deposition and lift-off finalised the process. (e) Close-up of the contacted NWFET featuring source (S), drain (D) and back-gate (BG).

the SiO_2 layer from the acid etches used in wrap-gate fabrication (see next section, 2.3.2). The substrates were patterned with Ti/Au alignment crosses and interconnects prior to nanowire deposition in order to facilitate accurate pattern alignment and high through-put processing, shown in Fig. 2.9(a). The interconnects extend beyond the region shown in Fig. 2.9 and run out to bond-pads that ultimately enable electrical connection in a similar fashion to the HHMT devices. The alignment crosses were patterned to utilise the high precision alignment afforded by the Raith 150-Two EBL tool. These pre-patterned features divided the substrate into sets of 24 adjacent 100 μm $\times$100 μm 'write-fields'. In EBL, the write-field size defines the the maximal area over which the beam may be deflected to expose a pattern in the resist. Writing outside this area entails first moving the stage such that the SEM aperture is centred over a different section of the sample. Scanning the beam over the new area then constitutes writing in a separate write-field. Chips were typically processed with multiple sets of the 24 adjacent write-field patterns to enable concurrently applying an identical fabrication process to up to 72 NWFETs.

The EBL process for NWFETs was:

1. After nanowire deposition, PMMA-A5 was spun onto the substrate according to the process in Sec. 2.1.2.

2. An optical micrograph was taken of each write-field, and custom patterns were generated to link the source/drain of a single nanowire in each write-field to the Ti/Au interconnects.

3. The substrate was placed on a movable sample stage in the Raith 150-Two.

4. 'Global' sample alignment was performed, which consisted of recording the substrate position and orientation in the EBL software. Subsequent positioning was done relative to this global alignment step.

5. With the beam off, the stage was moved such that the SEM aperture was immediately above the centre of the first write-field.

6. The beam was turned on and scanned over each of the four alignment crosses. These images are displayed to the user, who places a cursor at the centre of each cross within the EBL software. This precisely specifies the position/alignment of the current write-field.

7. The beam was deflected within the 100 μm^2 write-field to expose the contact pattern in the PMMA layer.

8. The beam was then turned off, and the stage was moved to the next write-field.

9. Steps 6 - 8 were repeated until all patterns had been exposed in each write-field.

10. The sample was removed from the EBL tool and the resist was developed in 1:3 methyl isobutyl ketone:isopropanol for 60 s, rinsed with isopropanol and dried with N_2.

After development, the sample was ashed in O_2 plasma for 30 s to remove residual resist. The nanowire contacts then underwent the weak sulfur treatment outlined in the previous section immediately prior to contact deposition. The ohmic contacts were either Ti/Au or Ni/Au deposited by thermal evaporation; specific layer composition and thickness are given for each presented device. Lift-off was accomplished by soaking in NMP at 80°C for 6 to 18 hours. Samples were rinsed in acetone and isopropanol and dried with N_2 gas. The finished chips were divided into smaller sections using a diamond scriber. Each smaller piece was affixed to an LCC20 chip package using conductive silver paint, and selected devices were contacted using the Au ball bonder. One of the pins on the LCC20 was bonded directly to the bottom of the package. This facilitated electrical contact to the n^+-Si substrate *via* the conductive silver paint.

This process was used the basis for polymer electrolyte-gated NWFETs, with the full details given in Chapter 4. I also studied polymer electrolyte-gated NWFETs with *p*-GaAs channels. In these devices, at 200 nm thick AuBe layer was used for the ohmic contacts rather than Ni/Au. The nanowires underwent a 30 s etch

of 20% HCl in H_2O to remove the native oxide prior to metal deposition. After deposition and lift-off, the contacts were annealed at 300°C for 30 s to facilitate ohmic contact formation.

2.3.2 Wrap-gated NWFETs

The fabrication procedure for lateral wrap-gated NWFETs shown in Fig. 2.10 was developed by Storm *et al.*[145] In this method, the wrap-gate layers were coated onto the as-grown nanowires in the vertical orientation. The nanowires were then transferred to the measurement substrate and wrap-gate segments are selectively etched in this lateral orientation. The coatings consisted of a 12 nm insulating Al_2O_3 layer deposited by atomic layer deposition (ALD), the metal wrap gate, which was 16.5 nm of W and 11.5 nm of Au deposited by dc sputtering, and an outer 12 nm Al_2O_3 layer. The outer Al_2O_3 layer was deposited solely to facilitate nanowire transfer; metal-coated nanowires do not adhere to the cleanroom tissue. Fabrication of wrap-gated NWFETs then proceeds as follows:

1. Nanowires were transferred to the measurement substrate, as for substrate-gated NWFETs (Fig. 2.10(c)).

2. EBL was used to open windows in the PMMA resist at both ends of the nanowire (Fig. 2.10(d)). This pattern ultimately defined the source/drain leads, and therefore the windows extend to the pre-patterned interconnects.

3. A series of etches were used to selectively remove the outer oxide and wrap-gate coatings in the source/drain contact regions. An important aspect of this step was that the etches work along the nanowire length from the resist windows and remove portions of the coating layers that were covered by resist (Fig. 2.10(e)). This is central to the success of the fabrication process; if the etches only removed material in the resist windows, depositing the ohmic contacts into these windows would cause them to electrically short directly to the wrap-gate. An additional advantage of the etch working underneath the resist is that it allows the gate length to be set by the etch time. Longer

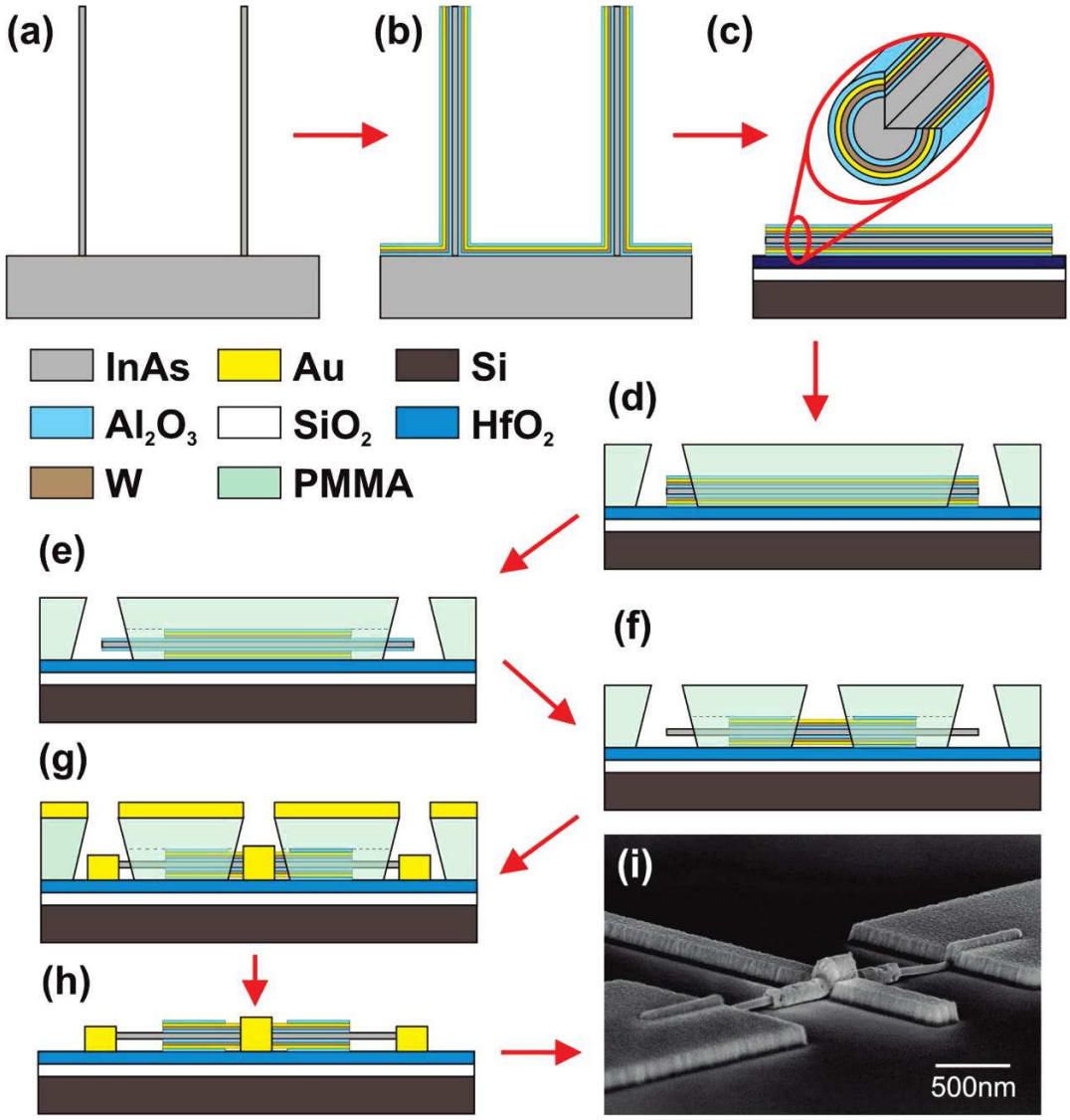

FIGURE 2.10: Fabrication for lateral wrap-gated NWFETs. (a/b/c) As-grown nanowires are coated with the wrap-gate material in the vertical orientation before being transferred to the measurement substrate. The layers are shown in the inset to (c), and are an inner Al_2O_3 insulator, the W and Au wrap-gate, and an outer Al_2O_3 layer to enable nanowire transfer in (c). (d) EBL is used to define the source/drain contact regions. (e) A series of chemical etches remove the outer oxide and wrap-gate metal in the contact regions. The etches undercut the resist, with the wrap-gate length determined by the dilution and etch time of the Au etch. (f) A window is opened in the resist for the gate contact. A second HF etch removes the outer oxide at the gate contact and the inner oxide at the source/drain contacts. (g) The Ni/Au contacts are deposited, and (h) lift-off completes the device. (i) Scanning electron micrograph of completed device. Figure from Ref. 145.

etch times remove more gate material, and result in shorter gate lengths. The etches were:

(a) A 30 s etch in 1:7 buffered HF:H_2O to remove the Al_2O_3 layer. The need to remove an oxide with an acid etch explains the choice of oxide in the wrap-gate coating and on the measurement substrate. HfO_2 has a much slower etch rate in HF solutions than Al_2O_3 and SiO_2. Therefore HfO_2 was used as a protective layer for the measurement substrate, as only a minimal amount is removed during the 30 s required to completely remove the Al_2O_3 wrap-gate insulator.

(b) A KI/I_2 etch to remove the Au layer. The composition and time of this etch determines the gate length. All etch solutions were based on a stock solution of 4 g KI and 1 g I_2 dissolved in 80 mL of H_2O. Storm *et al.*[145] used dilutions from 20% stock to 1% stock in H_2O. The highly diluted etches provided the slowest etch rate and therefore the most accurate gate length control. Typical etch times were 60 s to 240 s.

(c) A solution of 31% H_2O_2 in H_2O at $T = 40°C$ was used to etch away the W layer.

4. A second EBL step on the same resist opened a window for deposition of the gate contact.

5. The outer oxide in this window and inner oxide at the source/drain were etched using the buffered HF solution (Fig. 2.10(f)).

6. The source/drain regions of the NW were passivated with the weak $(NH_4)_2S_x$ treatment immediately before loading the device into the thermal evaporator.

7. 25 nm Ni and 75 nm Au are deposited to contact the device at the source, drain and gate (Fig. 2.10(g)). Liftoff in NMP completes the device, shown in Fig. 2.10(h/i).

A particular advantage of this fabrication procedure is that it uses only one resist layer. This ensured that the nanowire remained in the same position throughout

processing, which is vital to accurately complete high-precision nanofabrication. The concern was that using two separate resists for gate definition and contact deposition would cause the nanowire to shift position during lift-off or subsequent processing.

A major disadvantage of the single-resist approach is that it cannot be used to fabricate devices with multiple wrap-gates. This is because the final step involves depositing metal wherever a region of the resist has been opened. For example, a natural place to start with a single-resist approach would be to open the resist in the middle of the nanowire at the same time as the source/drain contact etch regions are defined at Step 2. The middle of the wrap-gate would then be etched away along with the wrap-gate portions at the source and drain in Step 3, splitting the gate into two segments. However, metal would ultimately be deposited into the resist opening at Step 7, directly onto the nanowire. This is incompatible with a number of key potential applications where a small spacing between adjacent wrap-gates would be desirable. An unnecessary ohmic contact between the gates severely limits the spacing between segments and radically increases the chance of the ohmic contacts shorting directly to the gates. A small wrap-gate separation is highly desirable for down-scaling applications. It would also be beneficial for, e.g., a quantum dot defined using three wrap-gate segments. In the latter, the potential on the two outer wrap-gates would define the tunnelling barriers and the central gate could be used as a plunger gate to probe the dot energetics. Here, having ohmic contacts within the quantum dot is highly undesirable, especially for InAs nanowire devices where the invasive ohmic contacts themselves can constitute a significant potential barrier.[30,241] Developing a general method for the fabircation of multiple wrap-gated NWFETs with only a source and drain at either end of the wire entailed using a two-resist process. I present the process we developed in Chapter 4, which was used to realise devices with up to four independent wrap-gate segments with separations of down to 200 nm.

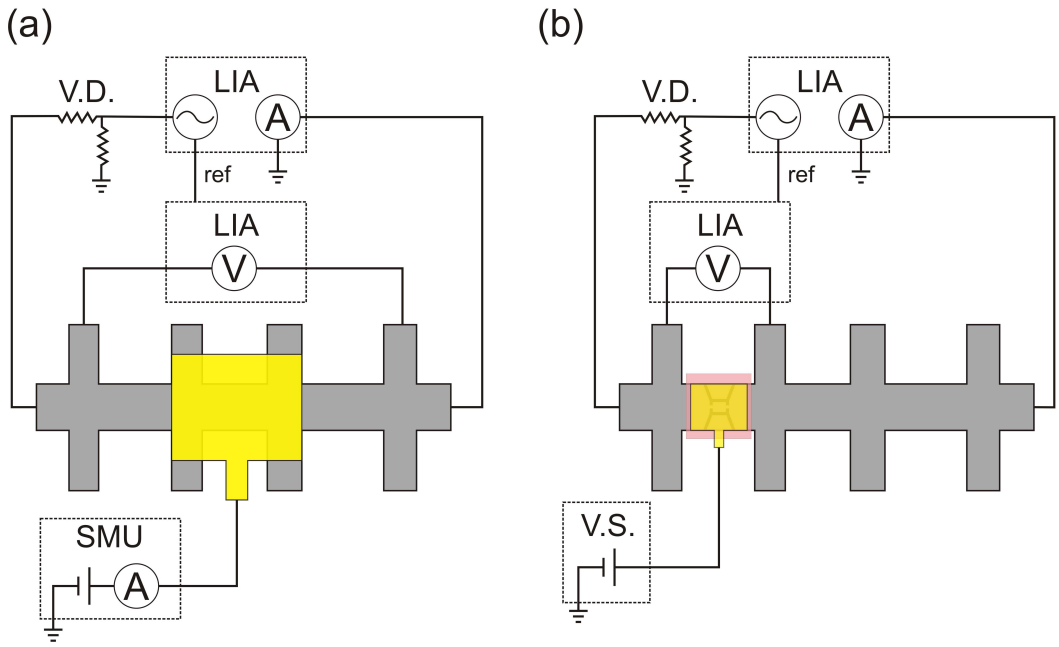

FIGURE 2.11: Electrical circuits used for (a) HHMTs and (b) the etched hole billiard in Chapter 3. The Hall bar is shown in grey, the Ti/Au gates in gold. The polyimide layer in (b) is shown in pink, with the etched billiard depicted underneath the gate and polyimide. Two lock-in amplifiers (LIA) were used to facilitate phase-sensitive detection in a four-terminal configuration. The upper LIA sourced ac excitation V_{sd}^{ac} and measured I_d while the lower was used to measure four-terminal voltage V_{4T}. A reference signal (ref) was provided for the second LIA to phase-lock to the V_{sd}^{ac} signal. A passive voltage divider (V.D.) was used to reduce V_{sd}^{ac} to 100 μV. For HHMTs, a Keithley K2400 source-measure unit (SMU) was used to supply V_G and simultaneously measure gate leakage currents I_G. A Yokogawa 7651 voltage supply (V.G.) was used to source V_G to the gate of the hole billiard due to the superior signal-to-noise ratio.

2.4 Experimental methods and measurement systems

2.4.1 Electrical characterisation

The purpose of electrical measurements throughout this thesis was to examine the influence of the gate potential on conductance through a semiconductor channel of some form. All electrical set-ups and experiments therefore proceeded along the same basic lines. A constant voltage V_{sd} was applied to the source contact, and the gate voltage V_G was used to modulate the current I_d through the channel, as

measured at the drain. In the interests of maximising the signal-to-noise ratio, a lock-in amplifier was used to source V_{sd} and sense I_d where possible, enabling phase sensitive detection. A lock-in amplifier sources a sinusoidal ac excitation V_{sd}^{ac} at known frequency ω_0 and measures the root-mean-square value of a separate input signal V_{in}. In general the input signal is also a voltage, but most lock-in amplifiers contain a current pre-amplifying stage to convert a current signal to a voltage signal if this is desired. The phase sensitive detection occurs when the input ac signal is multiplied by the output excitation, and this signal is sent through a low-pass filter. This process returns a dc value $\frac{1}{2}V_{sd}^{rms}V_{in}^{rms}$ when the input signal frequency is exactly the output frequency ω_0; otherwise it returns the dc value of zero.[242] In general, the input signal will consist of the desired I_d signal generated by V_{sd}^{ac}, plus noise in the form of sinusoidal components at other frequencies. The phase sensitive detector in a lock-in amplifier 'selects' only the component at the correct frequency, and rejects any components arising from noise. This enables a very high signal-to-noise ratio. In addition, the fact that the lock-in amplifier returns the root-mean-square I_d^{rms} means the measurement is directly comparable to a dc measurement.[242]

The circuit diagrams used for measurements on *p*-AlGaAs/GaAs heterostructure devices are shown in Fig. 2.11. An SR830 lock-in amplifier (LIA) was used to source V_{sd}^{ac} and measure I_d at either end of the Hall bar. A passive voltage divider (V.D.) was used to reduce the 1 V ac output of the LIA to 100 μV at the device source contact. The LIA served as the virtual ground for the device at the drain. Note that this means the 2DHG was grounded, with the ac excitation V_{sd}^{ac} oscillating about zero. A four-terminal configuration was used to accurately measure the channel resistance/conductance. This was accomplished using a second LIA (EG&G 5210) that measured the voltage drop V_{4T} between the two outer arms of the Hall bar. A reference signal at the excitation frequency was sent to the second lock-in to facilitate phase sensitive detection of V_{4T}. Measuring the four-terminal voltage drop V_{4T} and resistance $R = V_{4T}/I_d$ excludes the non-zero resistances of the ohmic contacts and the instrument cables, and gives an accurate measurement of the resistance of the channel itself.[243] This was particularly vital in the case of the

hole billiard (Fig. 2.11(b)), which required accurate measurement of conductance G. Finally, the gate voltage V_G was modulated by either a Keithley K2400 source-measure unit (SMU) or Yokogawa 7651 voltage supply (V.S.). The SMU sources a voltage V_G and measures the current to ground I_G. Ideally $I_G = 0$ as the gate should be floating, however a high applied V_G can cause charge to 'leak' over the Schottky barrier at the surface, and through the heterostructure into the grounded 2DHG. Gate leakage currents also arise for devices with an insulating layer if V_G exceeds the breakdown voltage of the insulator (see Fig. 1.18 in Sec. 1.4.5). The K2400 features a built-in current limiting feature to prevent further increments in V_G if a user defined I_G is reached, typically $1 - 10$ nA. This prevents potential damage to the device caused by large leakage currents. The K2400 was used for all measurements of HHMT devices in Chapter 3. The Yokogawa voltage source was used in measurements of the hole billiard due to the superior signal-to-noise ratio compared to the K2400 SMU. However, the SMU was used prior to collecting the measurements given in this thesis to check that $I_G < 0.5$ nA throughout the V_G measurement range.

The electrical circuits used to measure NWFETs in Chapters 4 and 6 are presented in Fig. 2.12. For the multiple wrap-gated NWFETs and polymer electrolyte-gated NWFETs presented in Chapter 4, an SR830 LIA was again used to source V_{sd}^{ac} and measure I_d. The SR830 also houses four voltage sources which were used to supply V_G to each of the gates on the multiple wrap-gate devices (Fig. 2.12(a)). This was done so that nominally identical voltage sources were used for each gate. For polymer electrolyte-gated NWFETs, a low-noise Yokogawa GS210 voltage source was used to supply V_G (Fig. 2.12(b)). Measurements in Chapter 6 were conducted at the University of Queensland. For these experiments, a Keithley K2450 was used to supply a V_{sd}^{dc}. This SMU also houses a high accuracy current module that was used to measure I_d at the drain. As mentioned above, the rms values obtained from LIA measurements are directly comparable to those obtained from dc measurements. A Keithley K2400 was used to supply V_G and measure $I_d < 0.1$ nA (Fig. 2.12(c)). We also explored the transient response of the PE-gated NWFET to square pulse train applied to V_G using the set-up shown in Fig. 2.12(d).

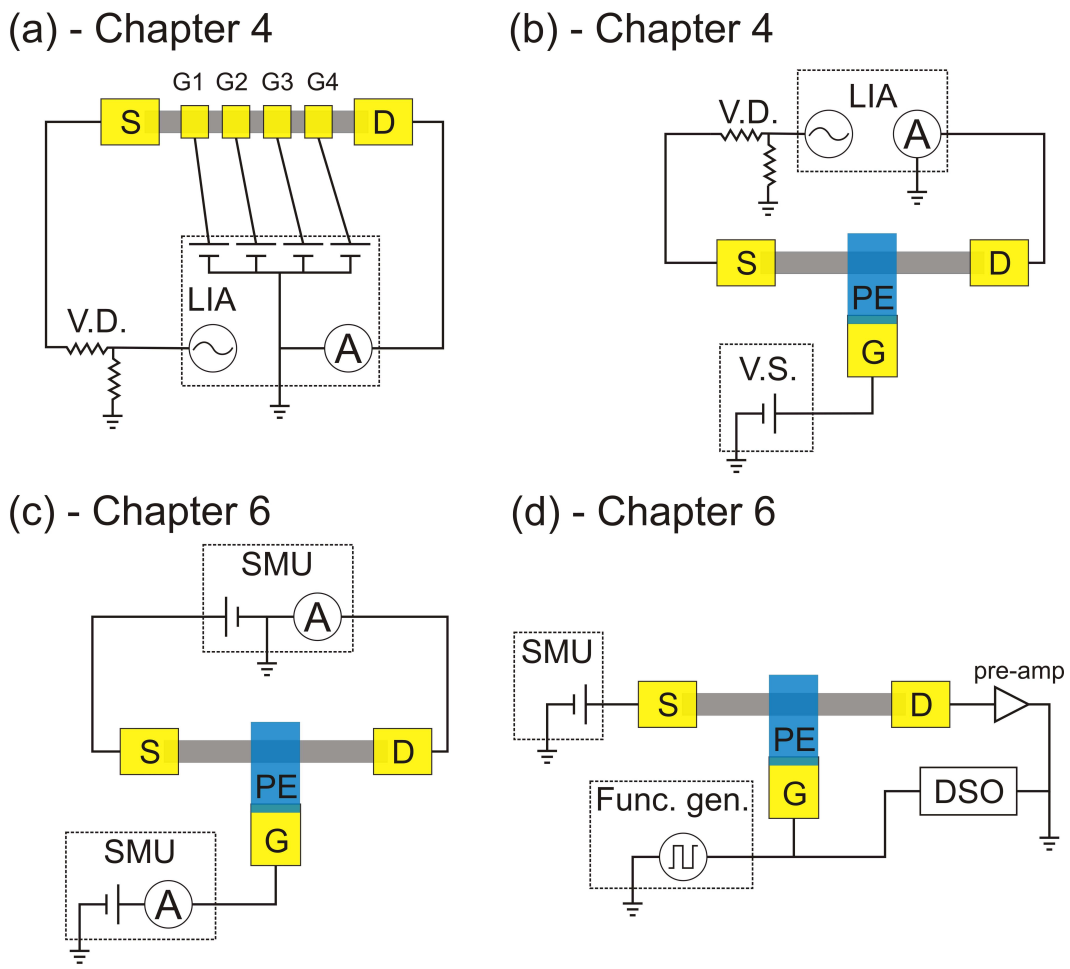

FIGURE 2.12: Electrical circuits used to measure NWFETs in (a/b) Chapter 4 and (c/d) Chapter 6. (a) For NWFETs with multiple metal/oxide wrap-gates, an SR830 provided V_{sd}^{ac} and measured I_d. The SR830 contains four voltage sources, which were used to supply V_G to each of the wrap-gates. (b) For NWFETs with patterned polymer electrolyte gate dielectrics, a Yokogawa GS210 voltage source (V.S.) was used to supply V_G. An SR830 was used to provide V_{sd}^{ac} and measure I_d. (c) For humidity dependent measurements at the University of Queensland, two separate modules within a Keithley K2450 SMU were used to source V_{sd}^{dc} and measure I_d. A K2400 SMU sourced V_G. (d) In a separate configuration, an HP33120A function generator (func. gen.) supplied a series of voltage pulses to V_G. The resulting I_d was converted to a voltage using a Femto DLPCA200 current pre-amplifier (pre-amp) and measuring using an Agilent DSO-X 3024A digital signal oscilloscope (DSO). The K2450 was used to supply V_{sd}^{dc}.

The pulse train was supplied by a H.P. 33120A function generator. A low-noise Femto DLPCA200 current pre-amplifier converted the I_d signal to a voltage signal with a gain of $10^5 - 10^7$ V/A, and this was measured by an Agilent DSO-X 3024A digital signal oscilloscope (DSO). The DSO also directly monitored the V_G pulses. Four-terminal measurements were not done on NWFETs as the morphology of the nanowires and the invasive, low resistance contacts means the contacts are either difficult to fabricate[192] or prevent a true four-terminal measurement due to challenges in correctly measuring the voltage of one dimensional modes.[156,244] In any case, the low contact resistance means that the 2-terminal and 4-terminal resistances of InAs nanowires differ by only $\sim$ 5%.[135,245] The circuits used to measure I_d and thermovoltage due to quantum dot-like states in InAs nanowires built on the set-ups used in Chapter 4. They are presented in the relevant section of Chapter 5.

2.4.2 Cryogen dewar and dipstick

Many of the devices in this thesis were studied at low temperature to observe quantum effects, and/or to reduce noise and gate instability. A very simple and effective way to cool a sample is to immerse it in a cryogenic liquid. The most commonly used cryogens are liquid N_2 (boiling point $T = 77$ K) and liquid ^{4}He (boiling point $T = 4.2$ K). The cryogens were kept in double walled, vacuum shielded dewars to minimise thermal contact with the surrounding lab. The packaged samples were loaded into a socket on the end of the 'dipstick' pictured in Fig. 2.13. The pins on the socket connected to the pins on the LCC20 package. Electrical wires from each pin ran up through the dipstick to a break-out box with BNC connections. BNC cables were then connected between the break-out box and instruments.

The dipstick/dewar set-up could be used to measure devices in a continuous temperature range between the cryogen temperature and room temperature, inclusively. For measurement at $T = 77$ K or 4.2 K, the dipstick was lowered into

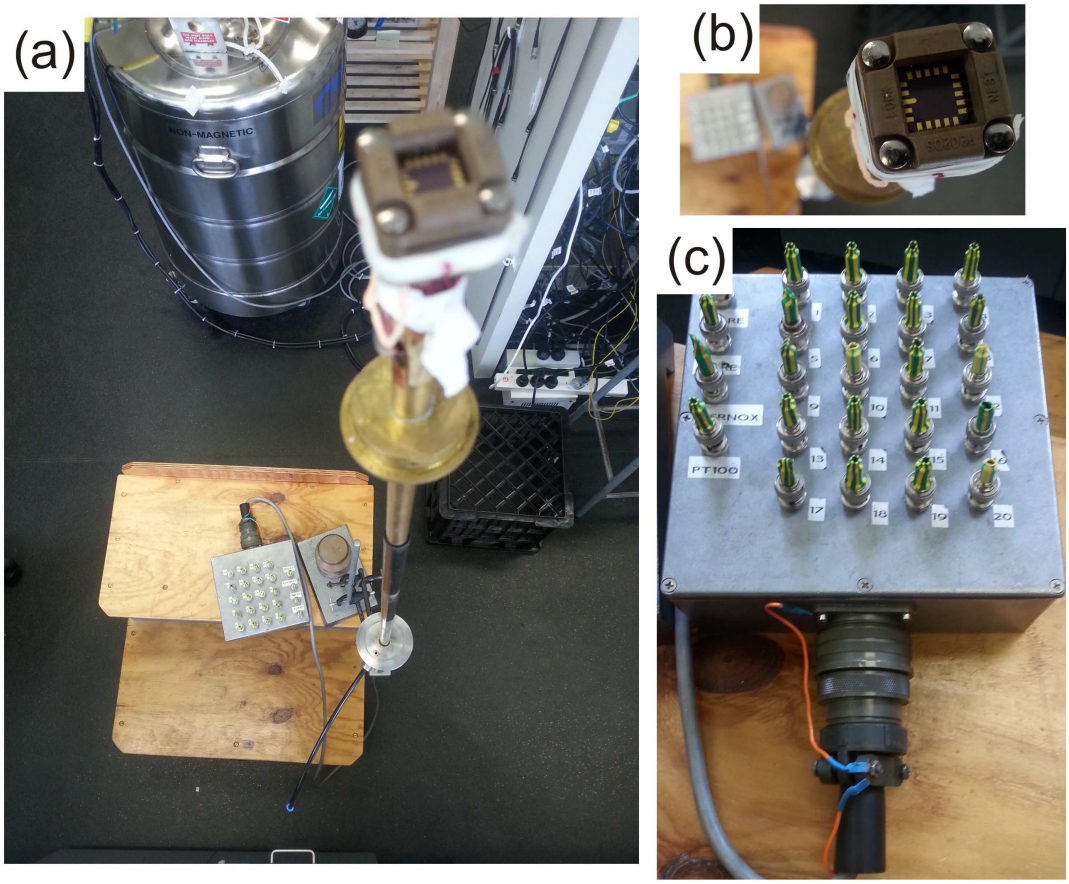

FIGURE 2.13: Photographs of the cryogen dewar and dipstick. (a) The dipstick features a socket to hold the LCC20 chip packages, which is electrically connected to the break-out box. The dipstick was inserted into the silver-coloured dewar in the background to obtain measurement temperatures down to 4.2 K. (b) Close-up of the underside of an LCC20 chip package contained within the dipstick socket. (c) Close-up of the break-out box, with 20 connectors corresponding to the 20 pins on the LCC20 packages.

the dewar until the sample was immersed in the cryogen. Stratification of the atmosphere above the liquid produces a vertical temperature gradient between the liquid and the top of the dewar. Therefore, fixing the sample position above the liquid facilitated measurement at temperatures 4.2 K $< T <$ 300 K. The dipstick was also used outside the dewar in ambient to conduct the room temperature measurements of polymer electrolyte-gated NWFETs presented in Chapter 4.

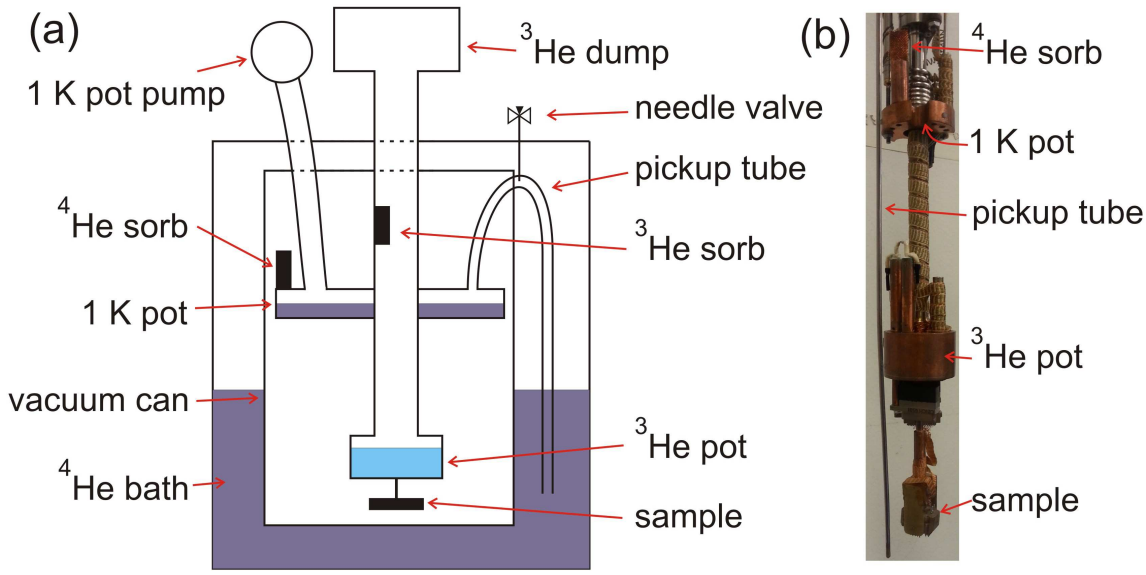

FIGURE 2.14: (a) Schematic of the Heliox ^{3}He cryostat. The system is contained within a vacuum can with a small amount of ^{4}He exchange gas. The cryostat is lowered into a ^{4}He bath, which brings the system to 4.2 K and causes the exchange gas to be absorbed by the ^{4}He sorb. Liquid ^{4}He is admitted to the 1 K pot by controlling the needle valve. Pumping on the evaporated liquid cools the 1 K pot to $T \sim 1.5$ K. The 1 K pot is in thermal contact with the closed ^{3}He system, which condenses ^{3}He into the ^{3}He pot. Absorption of evaporated gas by the ^{3}He sorb effectively pumps on the ^{3}He and cools the pot to base temperature $T_B = 275$ mK. The sample is kept in thermal contact with the ^{3}He pot. (b) Image of the lower section of the Heliox, showing the ^{4}He sorb wrapped in copper mesh, 1 K pot, pick-up tube, ^{3}He pot and sample socket.

2.4.3 Heliox ^{3}He cryostat

Temperatures $T < 4.2\ K$ can be obtained *via* evaporative cooling techniques. The principle is that the latent heat involved in evaporation of a liquid necessarily cools the remaining liquid. The cooling power is determined by the evaporation rate, which can be enhanced by pumping out the evaporated gas. By pumping on ^{4}He it is possible to cool the liquid to $T = 1.2 - 1.5$ K. Lower temperatures $T \sim 230$ mK can be obtained by using ^{3}He, which has a faster evaporation rate than ^{4}He, and thereby increased cooling power.[246]

The Heliox cryostat utilises three stages of immersion in a liquid ^{4}He bath and both ^{4}He and ^{3}He evaporative cooling to obtain $T \sim 275$ mK.[246,247] A schematic of the equipment is given in Fig. 2.14. The closed ^{3}He section consists of a pot where

the liquid will eventually settle and a dump where the gaseous ^{3}He is contained at room temperature. Having this section of the system tightly closed off facilitates simple operation and entails low risk of leaking expensive ^{3}He. It does mean, however, that pumping is not done using a typical mechanical pump. Rather, the behaviour of the ^{3}He is mediated by a charcoal 'sorb' mounted between the ^{3}He pot and dump, which absorbs ^{3}He gas for $T < 10$ K. In this way the sorb effectively acts as a miniature, automatic pump. The pumped ^{4}He aspect of the Heliox surrounds the '1 K pot'. A thin vacuum shielded pick-up tube runs from the 1 K pot into the ^{4}He bath to draw liquid ^{4}He into the 1 K pot. The flow is regulated by a needle valve. A pumping line runs out of the cryostat and is connected to a rotary pump, which is used to pump the 1 K pot to vacuum < 1 mbar before loading the cryostat. The entire cryostat is contained within a vacuum sealed can. A small amount, ~ 1 cm^3, of ^{4}He exchange gas is admitted into the vacuum can to facilitate the initial cooling to 4.2 K. The sample is mounted in thermal contact with the ^{3}He pot.[246,247]

Cooling the Heliox to base temperature $T_B \sim 275$ mK follows these four steps:[247]

1. Cooling to $T = 4.2$ K: The cryostat is loaded into the liquid ^{4}He dewar and immersed in the bath. The exchange gas in the vacuum can brings the cryostat into thermal equilibrium with the bath, at $T = 4.2$ K. A second charcoal sorb was included within the vacuum can – but outside the other cryostat components – to absorb the exchange gas as the cryostat cools. This restores vacuum between the cryostat and ^{4}He, which is desirable as the following steps cool the cryostat below 4.2 K. Thermal contact with the liquid ^{4}He bath from this point on would constitute an unwanted heat source.

2. Cooling the 1 K pot: A small amount of liquid ^{4}He is drawn into the 1 K pot *via* the pick-up tube. Pumping on the 1 K pot while drawing in liquid ^{4}He cools the 1 K pot to $T \sim 1.5$ K.

3. Condensing ^{3}He: The 1 K pot is in thermal contact with the central section of the closed ^{3}He portion of the cryostat. This causes condensation of ^{3}He

into the pot, since 1.5 K is less than the ^{3}He boiling point of 3.2 K. The ^{3}He sorb is heated to $T = 30$ K to ensure that all ^{3}He is released, and ultimately condenses into the pot.

4. Cooling to base temperature $T_B \sim 275$ mK: To cool the ^{3}He from 1.5 K, the sorb heater is turned off. The sorb slowly cools to $T \sim 2$ K and begins to absorb ^{3}He. This essentially pumps on the ^{3}He and cools the pot to base temperature $T_B \sim 275$ mK.

The Heliox holds base temperature for approximately 48 hours, limited by the finite supply of ^{3}He. As the ^{3}He evaporates and is absorbed, the thermal mass of the remaining liquid is slowly reduced and the ^{3}He pot temperature rises. Cooling the ^{3}He pot back to T_B requires repeating Steps 4 and 5 to expel all ^{3}He from the sorb, condense the gas into liquid and then cool the system to base temperature.

It is possible to obtain stable intermediate temperatures between 275 mK and 4.2 K by working in two distinct regimes, depending on whether the desired temperature is higher or lower than the temperature of the 1 K pot. Temperatures up to 1.5 K can be achieved by heating the charcoal ^{3}He sorb to moderate temperatures $<$ 10 K. Heating reduces the pumping efficiency of the sorb, and therefore the cooling power of the evaporation process. The advantage of this method over directly heating the ^{3}He pot is that the latter accelerates evaporation and significantly reduces the available measurement time at T_B.[246,247] To obtain $T > 1.5$ K, the charcoal sorb is first heated to 20 K to release some of the ^{3}He gas and bring the ^{3}He pot into thermal equilibrium with the 1 K pot at $T = 1.5$ K. Heat is then applied directly to the ^{3}He pot until the required temperature is reached.[246,247] ^{3}He evaporation in this regime is less of a concern as heating the sorb releases excess ^{3}He gas which is condensed when the sorb heater is turned off after measuring.

The Heliox cryostat was used to collect the results on quantum dot-system in InAs nanowires presented in Chapter 5.

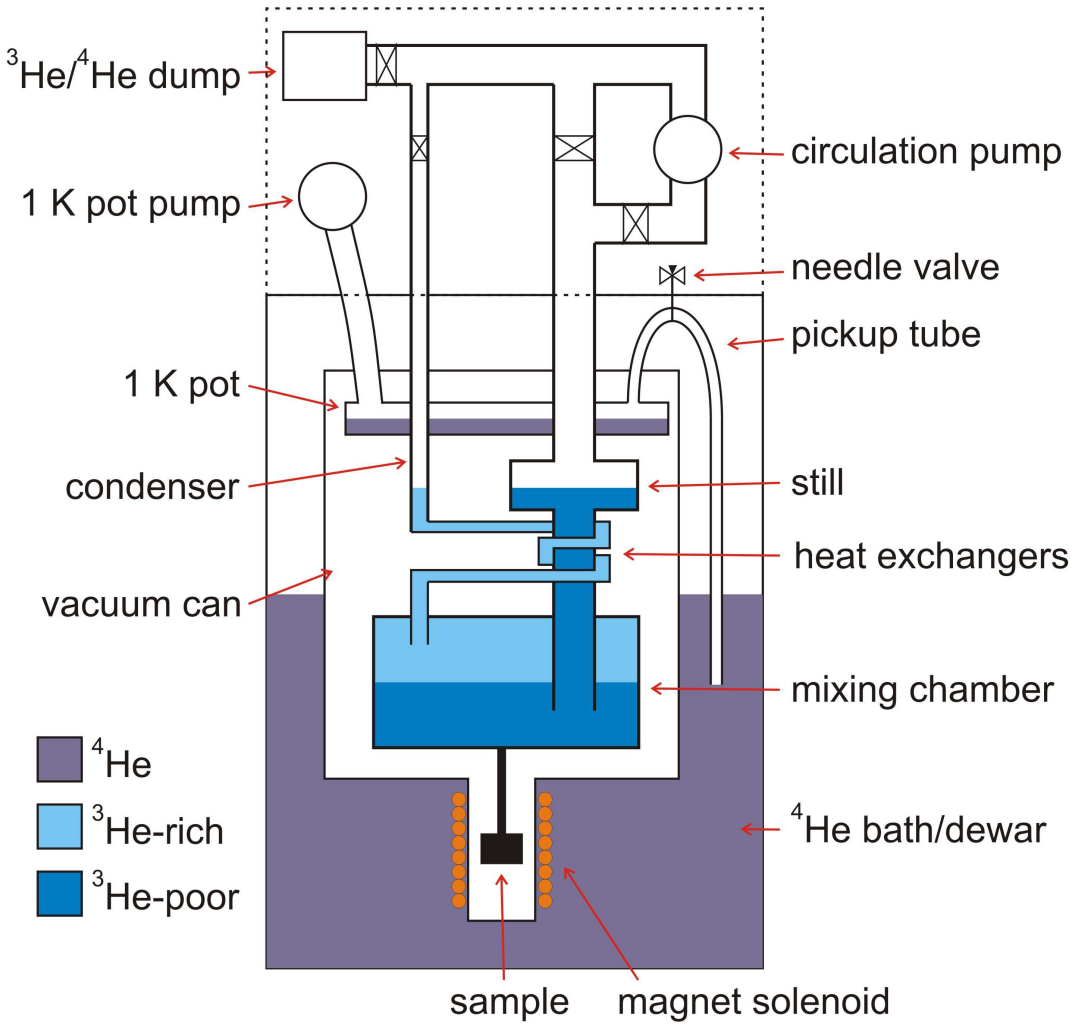

FIGURE 2.15: Diagram of Kelvinox K100 dilution refrigerator at base temperature, $T_B = 40$ mK. The dilution unit is contained within a vacuum can secured in a dewar with ^{4}He bath. The bath initially cools the unit to 4.2 K and supplies ^{4}He to the 1 K pot *via* the pick-up tube. Pumping the 1 K pot cools it to $T \sim 1.2$ K. The boundary of the phase separated ^{3}He/^{4}He mixture is in the middle of the mixing chamber. The still draws only on the ^{3}He-poor phase. The circulation pump extracts evaporated ^{3}He and feeds it back to the condenser, where the gas is re-condensed by the 1 K pot (see Fig. 2.16 for more detail). The condenser tubes are wrapped around the pipes below the still to act as a heat exchanger; this cools the re-condensed gas to the temperature of the mixing chamber. The sample is secured to the mixing chamber on a post that fits within the bore of a superconducting solenoid magnet. The magnet is held within the ^{4}He bath. The gaseous ^{3}He/^{4}He mixture is stored in the dump when not in use. The dump is part of a room temperature gas handling system, contained within the dashed lines.

2.4.4 Kelvinox K100 dilution refrigerator

Obtaining even lower measurement temperatures requires more complex cooling methods. One such method relies on drawing ^{3}He across a phase boundary between two different dilutions of a ^{3}He/^{4}He mixture. The operating principle is as follows. Below a critical temperature, liquid ^{3}He/^{4}He mixtures separate into two phases with different dilutions; a ^{3}He-rich and ^{3}He-poor phase. The comparatively light ^{3}He-rich phase floats on the heavier ^{3}He-poor phase. ^{3}He atoms can be induced to cross the phase boundary in a process called mixing. Transferring ^{3}He across the phase boundary requires energy, in the form of latent heat. This can be understood by analogy to evaporative cooling. The transfer of ^{3}He from the ^{3}He-rich phase to the ^{3}He-poor phase is similar to the phase transition as atoms evaporate from a liquid; the latent heat required to facilitate the phase transition necessarily cools the ^{3}He/^{4}He mixture.

Dilution refrigerators enable the realisation of this powerful cooling process.[82,248] A diagram of the K100 used in this thesis is shown in Fig. 2.15. The dilution unit contains the mixing chamber, which is connected on one side by condenser lines, and on the other side by a chamber called the still. The sample is mounted in thermal contact with mixing chamber, and is positioned inside the bore of a superconducting solenoid, capable of delivering magnetic fields up to $B = \pm 10$ T. The solenoid is secured in the surrounding ^{4}He bath. Initial cooling occurs in the same manner as the Heliox. The unit is contained within a vacuum can that features a small amount of exchange gas and a charcoal sorb. The exchange gas cools the dilution unit to 4.2 K when brought into thermal contact with the ^{4}He bath. The sorb automatically adsorbs the exchange gas while this occurs, thermally isolating the dilution unit for $T < 4.2$ K. The ^{3}He/^{4}He mixture is condensed *via* thermal contact with a 1 K pot. A pick-up tube feeds ^{4}He into the 1 K pot and pumping on the ^{4}He in the pot cools it to $T \sim 1.2$ K. The room temperature gas-handling system directs the gaseous ^{3}He/^{4}He mixture flow through the system. Briefly, the valves are initially set to direct the ^{3}He/^{4}He from the dump into the dilution unit for condensing. The configuration is then

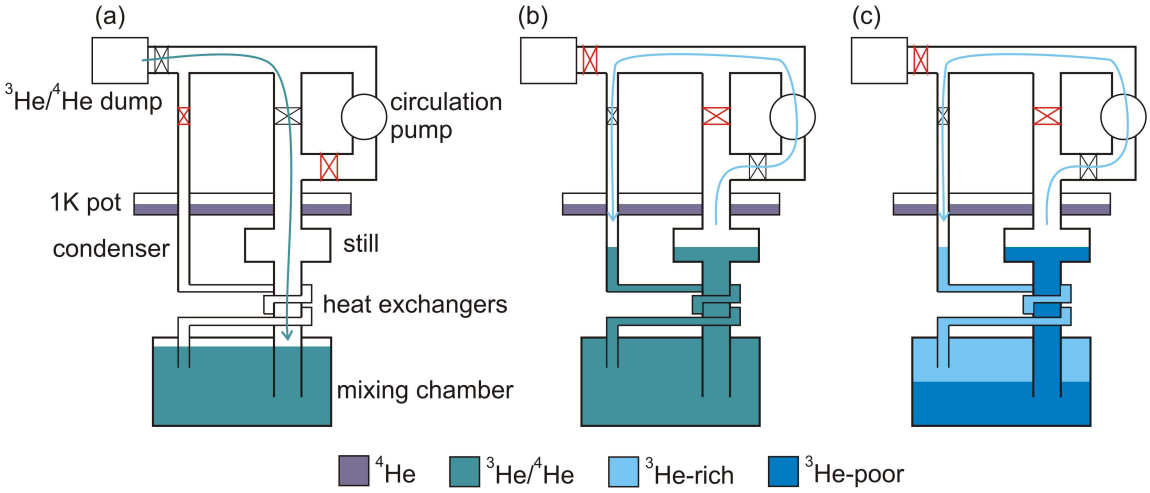

FIGURE 2.16: Cooling process for the K100 dilution refrigerator. Open (closed) valves are represented in black (red) and the arrows indicate the direction of gas flow. (a) The 1 K pot temperature is set to ~ 1.2 K and ^{3}He/^{4}He gas flow is directed into the mixing chamber on the still side. Thermal contact with the 1 K pot condenses the mixture. (b) After condensation, the mixture $T \sim 1.2$ K. The dump is sealed, and gas is directed from the still to the condenser through the circulation pump. Pumping on the still reduces the mixture temperature through evaporative cooling. ^{3}He is preferentially evaporated due to the superfluid state of the heavier ^{4}He atoms. (c) Below the critical temperature $T_C = 870$ mK, phase separation occurs. The circulation pump draws ^{3}He from the still, which causes ^{3}He in the mixing chamber to cross the phase boundary, cooling the mixing chamber to base temperature $T_B = 40$ mK.

switched to circulate the mixture and cool the system to base temperature. In detail, reaching base temperature in the dilution refrigerator is achieved with the following steps, following Fig. 2.16:

1. Condensing the mixture: The 1 K pot temperature is set to $T = 1.2$ K by adjusting the needle valve and pumping on the ^{4}He. The initial condensing process is actually done *via* the still. The larger pipes on this side make the process faster and ensure that any contaminants, e.g., oxygen and nitrogen, do not solidify in the thin condenser tubes and cause a blockage. Figure 2.16(a) shows the valves are set to flow ^{3}He/^{4}He gas through the still. Thermal contact with the 1 K pot condenses the mixture into the mixing chamber.

2. Circulation: Once all the mixture has been condensed into the mixing chamber, the ^{3}He/^{4}He dump valve is closed, and the gas system set up to circulate the mixture (Fig. 2.16(b)). A rotary pump is used to extract evaporated He from the still, reducing the temperature of the mixture by evaporative cooling. As the temperature is reduced, the faster evaporation rate of ^{3}He compared with ^{4}He means that gas flow consists almost entirely of ^{3}He. This occurs because the heavier, bosonic ^{4}He atoms condense into a strongly interacting superfluid that resists evaporation. Meanwhile, the weaker interactions between the lighter ^{3}He fermions means they continue to undergo evaporation. The ^{4}He component can essentially be considered a static and inert background for the movement of ^{3}He.[82,248] The evaporated ^{3}He is fed through liquid N_2 and liquid ^{4}He traps to solidify and remove contaminants before the gas is returned to the condenser pipes. Once in the condenser lines, thermal contact with the 1 K pot condenses the ^{3}He into the mixing chamber. The condenser tubes are wrapped around the pipe below the still. This acts as a heat exchanger to ensure that the temperature of the re-condensed ^{3}He quickly comes to equilibrium with the liquid already in the mixing chamber.

3. Phase separation: The process of evaporation and circulation cools the mixture to below the critical temperature for phase separation, $T_C = 870$ mK. The component size and mixture volume are matched to meet three conditions: First, the phase boundary occurs in the mixing chamber. Secondly, the still draws on only the ^{3}He-poor phase. Thirdly, the condenser returns liquid directly into the ^{3}He-rich phase (Fig. 2.16(c)). The continuing circulation process evaporates ^{3}He at the still and consequently draws ^{3}He across the phase boundary in the mixing chamber. This occurs because the ^{3}He-poor phase has a minimum ^{3}He concentration, even at 0 K.[82,248] As a result, any ^{3}He evaporated from the ^{3}He-poor phase at the still must be replaced from the ^{3}He-rich phase at the mixing chamber. The subsequent ^{3}He transfer across the phase boundary cools the mixing chamber to $T_B = 40$ mK.

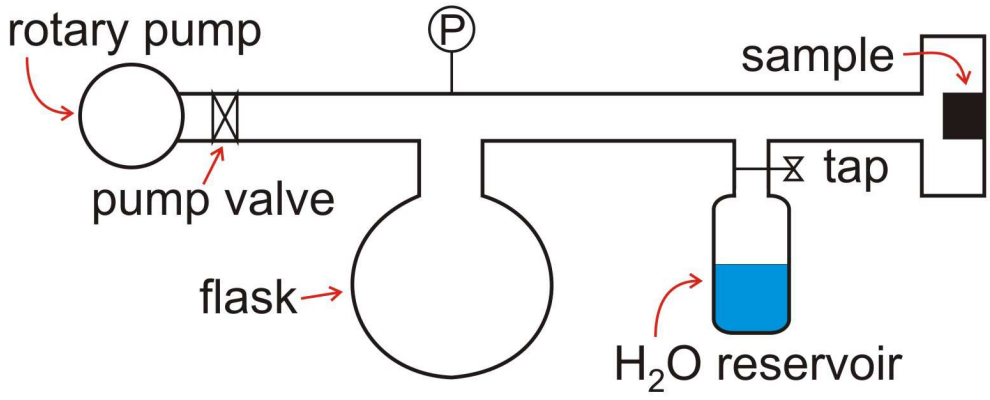

FIGURE 2.17: Hydration dependent measurement chamber schematic. The rotary pump evacuated the chamber and was then isolated by the pump valve. H_2O vapour was admitted to the chamber from the reservoir *via* the bleed valve, which hydrated the sample. The flask increased the chamber volume to ensure that the pressure P read on the gauge matched that at the sample location.

The circulation and cooling process continues indefinitely once the mixing chamber reaches base temperature, assuming there are no unintentional heat loads on the mixing chamber or 1 K pot. This is a highly favourable aspect compared to, e.g., the Heliox, as it facilitates continuous measurement at base temperature for as long as the system is stable. The indefinite circulation process also means that higher temperatures can be obtained by directly heating the mixture chamber. However, this is limited to $T \sim 900$ mK due to the critical temperature of the phase separation. Above this temperature, the system becomes very unstable, meaning the next viable measurement temperature is at $T = 4.2$ K, in thermal equilibrium with the ^{4}He bath.

The Kelvinox K100 was used to collect data from the hole billiard, presented in Chapter 3.

2.4.5 Hydration dependent measurement chamber

Chapter 6 presents results on hydration-dependent transport properties of polymer electrolyte-gated NWFETs. These measurements were obtained in a hydration controlled measurement chamber housed at the University of Queensland, Brisbane. A schematic of the equipment is shown in Fig. 2.17. The sample

was mounted inside a vacuum chamber connected to a H_2O reservoir by a bleed valve. The deionised Millipore H_2O was degassed prior to measurements by three freeze-pump-thaw cycles.[249–251] This procedure operates as follows: pumping on the reservoir while the H_2O is frozen removes gas in the reservoir. Thawing the H_2O releases any gas, e.g., N_2, O_2, previously contained in the liquid. The H_2O is then re-frozen to facilitate pumping out this gas. The procedure was repeated until the gas was removed from the H_2O, and the reservoir was left at vacuum.

To take measurements, the chamber was evacuated overnight using a rotary pump. Once the chamber was at vacuum, the pump valve was closed. Water vapour was then admitted from the H_2O reservoir by opening the bleed valve. The water vapour pressure was monitored on the pressure gauge, and the bleed valve closed when the desired pressure was reached. Electrical measurements were then performed at constant water vapour pressure. In this way the device hydration was increased in discrete steps until the saturation vapour pressure was reached, $P_{sat} = 24$ mbar at $T = 20°$C. The large round bottom flask increased the chamber volume to ensure a uniform atmosphere. A small chamber volume raises the probability of non-uniformities in atmospheric pressure. Increasing the chamber volume ensured the pressure at the gauge was equal to the pressure at the sample.[249]

2.4.6 Photoluminescence and X-ray photoelectron spectroscopy

In Chapter 3 I explore the efficacy of $(NH_4)_2S_x$ treatments in passivating (311)A GaAs surfaces. In addition to measuring the electrical properties of treated HHMTs, I characterised the treated surfaces using photoluminescence (PL) and X-ray photoelectron spectroscopy (XPS). PL and XPS are two of the most commonly used methods to evaluate the efficacy of passivation treatments[44,53,252] and examine the surface chemistry.[56–58,253]

XPS uses the photoelectric effect to determine the binding energy E_B of inner shell electrons.[254] The underlying physics is depicted in Fig. 2.18. X-rays incident on

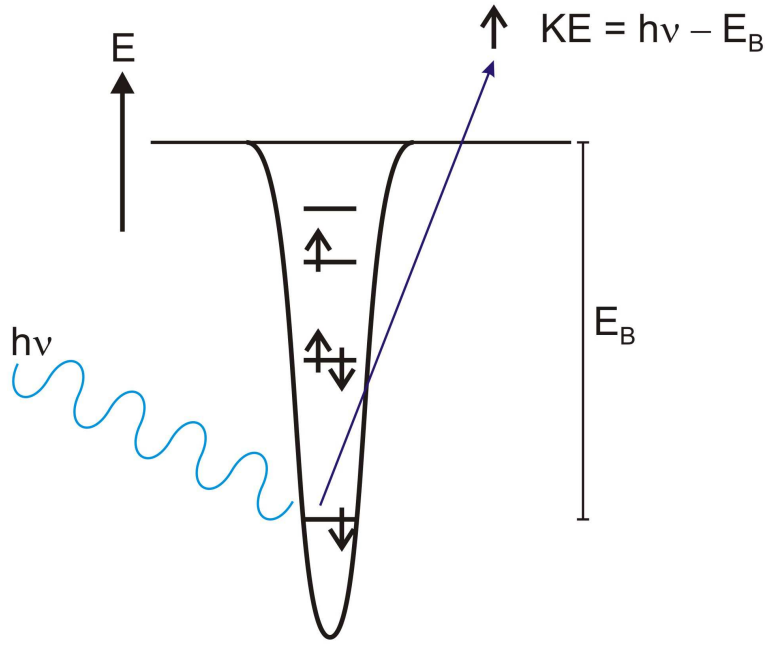

FIGURE 2.18: X-ray photoelectron spectroscopy is enabled by the photoelectric effect. Incident X-rays with known energy $h\nu$ eject inner shell electrons. Measurement of the ejected electrons' kinetic energy $KE = h\nu - E_B$ allows the binding energy E_B to be determined

the sample eject inner shell electrons by absorbing the photon. The electron first expends energy to overcome the binding energy of the atomic potential, and any excess energy manifests as kinetic energy. The binding energy E_B can be inferred by measuring the kinetic energy KE of emitted electrons, using:

$$E_B = h\nu - KE \tag{2.1}$$

where the incident X-ray energy $h\nu$ is accurately known.

The use of XPS as a chemical analysis technique centres on the fact that different chemical bonds shift the electron binding energy relative to the binding energy in the isolated atom.[254] In the context of sulfur passivation of the GaAs surface, it is possible to distinguish between the binding energies of electrons emanating from, e.g., As-O bonded species and As-S bonded species. I used XPS in Chapter 3 to ensure that $(NH_4)_2S_x$ treatment removed the surface oxides and generated a sulfur bonded monolayer. This process has been well established for (100) GaAs.[56–58,253]

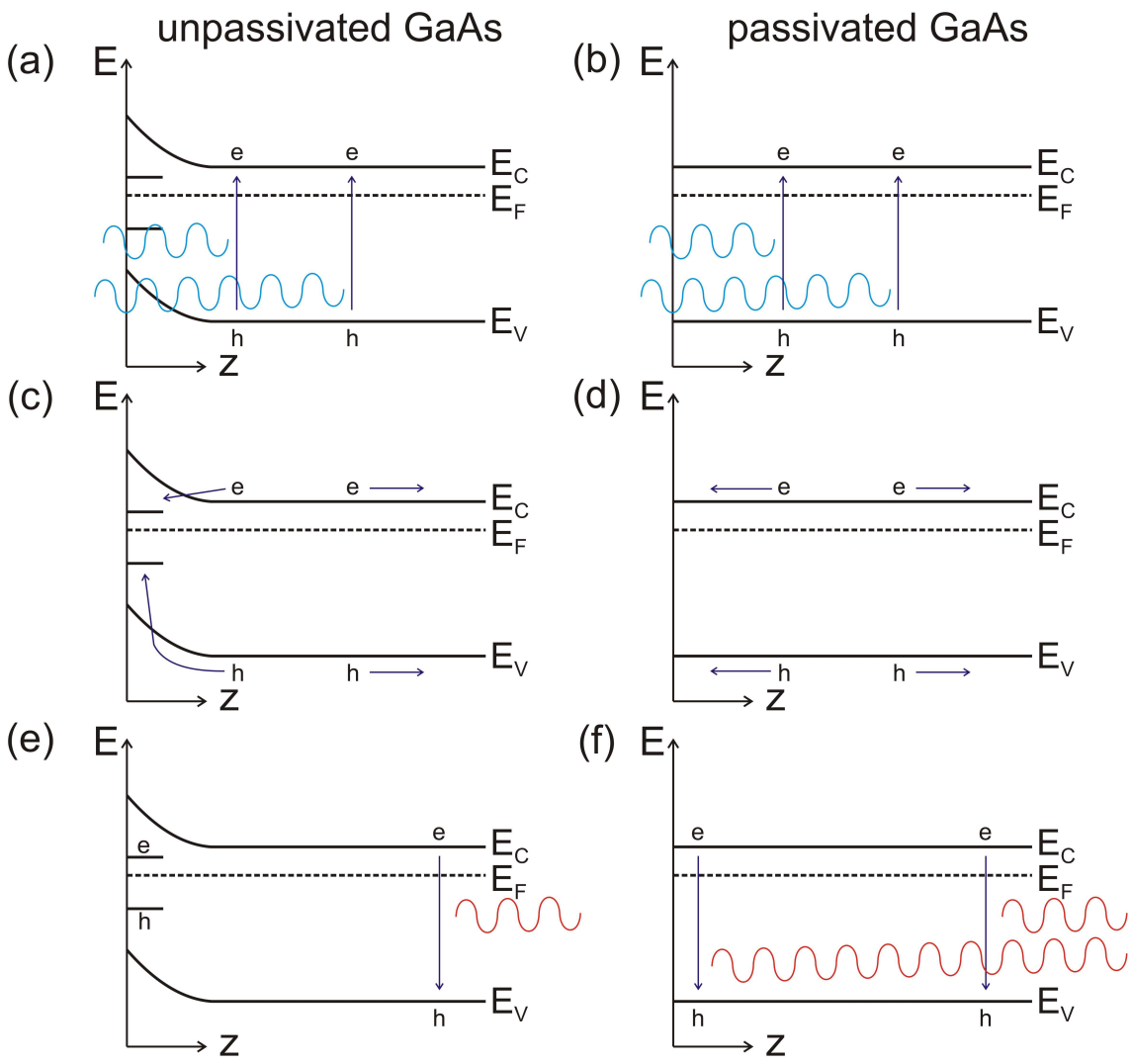

FIGURE 2.19: Photoluminescence of (a/c/e) a bare GaAs surface with a high surface state density and (b/d/e) a passivated GaAs with low surface state density. (a/b) A laser is used to generate electron-hole pairs. (c/d) The electrons/holes diffuse randomly in the sample and may become trapped in surface states. (e/f) Electron/hole recombination emits photons at the band gap energy $h\nu = E_C - E_V$. (e) The recombination life-time of charges trapped in surface states is much longer than that of electron/hole pairs in the continuous bands. (f) This leads to a higher PL intensity for surfaces free of band-gap states.

XPS was performed by Dr Bill Bin Gong at the Mark Wainwright Analytical Center at UNSW. Measurements were done using a ThermoScientific ESCALAB250Xi system with a monochromated Al Kα X-ray source ($h\nu$ = 1486.68 eV at 164 W power). The penetration depth of XPS is such that only the top $1 - 10$ nm of the material is probed. Binding energies were measured in reference to the C(1s) binding energy at 285.0 eV, and the expected uncertainty in all measurements

was ±0.1 eV. The measured binding energy peaks were fitted using the Advantage software package, based on the expected binding energy of electrons arising from each particular chemical species.

Photoluminescence (PL) was used to compare the relative surface state density of treated and untreated samples. The process is illustrated in Fig. 2.19. A laser is used to excite electron/hole pairs across the GaAs band gap. After diffusing for a short time, the pairs may recombine, or become trapped in surface states. Pair recombination emits luminescence consisting of photons with energy at the GaAs band-gap energy, $E_g = 1.42$ eV. The luminescence intensity is directly proportional to the number of radiative recombination events at the band edges. Charges trapped in surface states do not contribute to this signal. As such, a sample with a low surface state density will have a high PL intensity compared to a sample with a high surface state density.[44,53,252]

It is worth noting that an increased PL intensity can also arise if the treatment modifies the surface state spectrum such that the surface band-bending increases. This presents as a surface barrier that inhibits tunnelling into the surface states. The consequence is that PL intensity may increase without a corresponding decrease in overall surface state density. As such it is important to conduct secondary experiments to corroborate PL findings. In this thesis, I show that results obtained from PL were consistent with the electrical performance of HHMTs. PL experiments were performed using the 488 nm line of an Ar ion (Coherent Innova 70). Luminescence was detected using a CCD camera coupled to a Spex 270M grating spectrometer with spectral resolution of 3 nm.

2.5 Summary

This Chapter outlined the fabrication and experimental techniques utilised in this thesis. This included photolithography and electron-beam lithography based strategies for generating micro- and nano-scale patterns *via*, e.g., metal deposition and selective etching. I then described how these techniques were applied

to the specific GaAs/AlGaAs heterostructure devices and nanowire transistors investigated in this thesis. I also discussed the electrical measurement techniques employed to evaluate the field-effect related behaviour of these devices – including phase-sensitive detection of signals using lock-in amplifiers and four-terminal methods for accurately measuring sample resistance – and how these were applied to each device. Finally, I outlined the operation of each measurement system used, from room temperature down to $T = 40$ mK, and explained the principles behind photoluminescence and X-ray photoelectron spectroscopy, which were used to characterise sulfur-treated GaAs surfaces. The following chapters present the experimental results collected during the course of my research.

Chapter 3

Results: The impact of surfaces and dopants on instability in p-type AlGaAs/GaAs heterostructures

Section 1.4 outlined how the AlGaAs/GaAs materials system has facilitated the realisation and study of a wealth of quantum phenomena including one dimensional ballistic transport and artificial atoms. There is a great interest in studying the corresponding hole systems, but doing so has been severely hampered by the instability of hole devices manufactured from both Si-doped and C-doped p-AlGaAs/GaAs modulation doped wafers[24,107–110,255] as outlined in Sec. 1.4.5. During my honours year I contributed to a study which suggested that both charge trapping in (311)A surface states and charge migration between acceptor impurities in the AlGaAs layer contribute to gate hysteresis and instability in these wafers.[24] Our subsequent interest was in exploring the properties of both the (311)A GaAs surface and p-type Si dopants in AlGaAs. The aim was to more closely understand the underlying physics behind mechanisms causing gate instability and hysteresis, and potentially help to enable successful fabrication of stable devices based on p-type

modulation doped AlGaAs/GaAs heterostructures. For the surface aspect, we explored the use of $(NH_4)_2S_x$ treatments that have had extensive use as surface passivation for (100) GaAs.[32] As discussed in Sec. 1.3.2, sulfur passivation strips the native oxide and covalently satisfies both Ga- and As-related dangling bonds to result in a surface free of band-gap states.[21,41,43,44,55] To study dopant dynamics we fabricated an etched hole billiard in the hysteretic wafer, and studied changes in magnetoconductance fluctuations (MCF) induced in response to applied V_G and thermal cycling.[33] MCF in billiards is a phase-sensitive phenomenon arising from interference of electron/hole trajectories between entrance and exit.[82,83] The MCF are determined by both device geometry and background disorder potential; as such they can be used to provide a 'fingerprint' for the charge configuration of remote ionised dopants in the AlGaAs layer (see Secs 1.4.3 and 1.4.4).[84,90,91] I present results from both of these studies in this chapter.

3.1 Efficacy of $(NH_4)_2S_x$ solutions on the (311)A GaAs surface

3.1.1 Experiment and sample outline

The best case scenario towards improving (311)A AlGaAs/GaAs heterostructure performance would be gaining device stability through a simple surface treatment that provides effective surface state passivation. This was not necessarily going to be straightforward; despite significant work on lower index planes such as (100), (110) and (111) due to their importance for industrial device development, passivation of the (311)A GaAs surface has received little to no attention. Nevertheless, the success of $(NH_4)_2S_x$ solutions for (100) GaAs made these a natural choice in our attempt to reduce the (311)A GaAs surface state density. Additionally, dipping the sample in a solution prior to gate deposition constitutes simpler fabrication compared to, e.g., gas deposition[256] or specialised oxide deposition.[257] Applying $(NH_4)_2S_x$ to a new surface gave me the opportunity to explore the efficacy of the

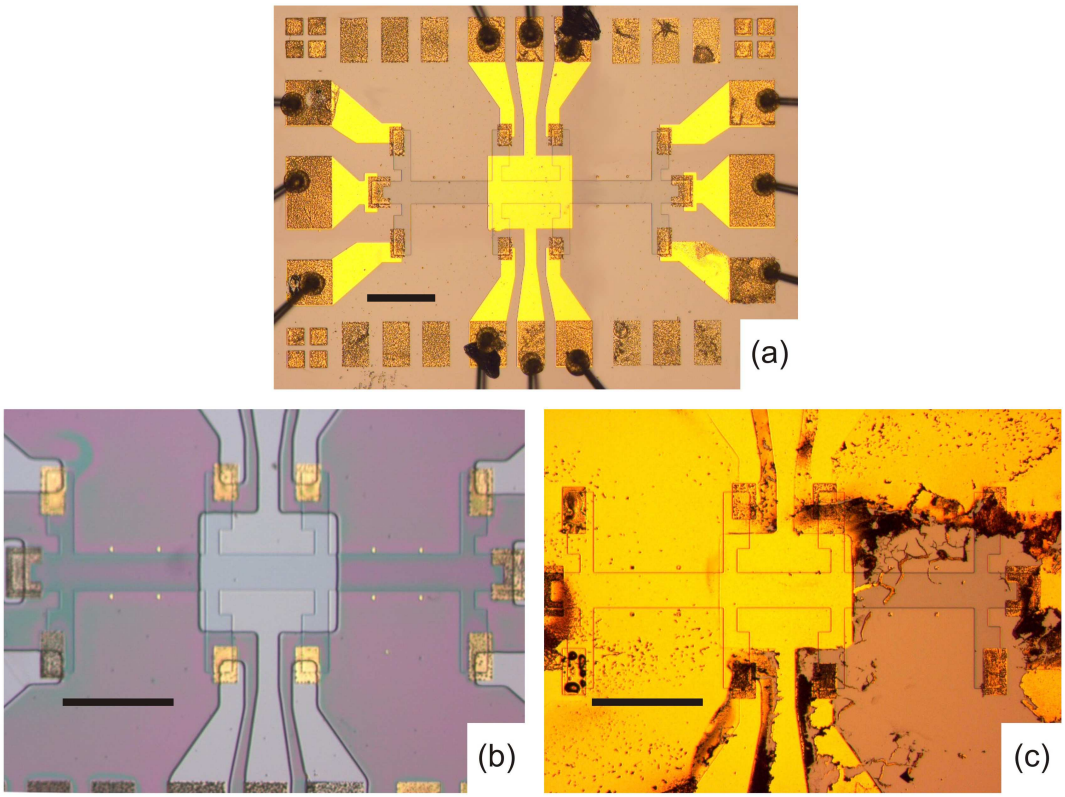

FIGURE 3.1: Optical micrographs of HHMTs at various stages. (a) Completed HHMT featuring Hall bar (light brown outline) contacted with AuBe Ohmic contacts (grainy gold) and a Ti/Au gate (central yellow square). (b) HHMT with gate pattern defined in photoresist layer (purple) prior to passivation and metallisation. (c) HHMT after treatment with alcoholic $(NH_4)_2S_x$ solution and subsequent metallisation. The alcoholic solution dissolved much of the photoresist, leaving unwanted metal over large regions of the device. Scale bars represent 300 μm.

treatment. In addition to measuring the electronic properties of treated AlGaAs/-GaAs devices, we characterised the effect of $(NH_4)_2S_x$ treatments using X-ray photoelectron spectroscopy (XPS) and photoluminescence (PL).

The devices used for electrical characterisation were HHMTs fabricated from (311)A-oriented *p*-AlGaAs/GaAs heterostructures, with an overall top gate that modulated the 2DHG density (see Fig. 3.1(a)). Heterostructure layer depths, doping levels and fabrication methods were outlined in Sec. 2.2. We used XPS to confirm that the $(NH_4)_2S_x$ treatment stripped the native oxide layer and produced Ga-S and As-S bonds at the (311)A and (100) surfaces. This was done using samples from the (311)A-oriented *p*-AlGaAs/GaAs and the matched (100)

n-AlGaAs/GaAs heterostructure grown alongside it. XPS probes only the top 5 nm of the sample, and thus interacted only with the GaAs capping layer. Finally, we utilised PL as a secondary tool to evaluate the passivation efficacy of $(NH_4)_2S_x$. An effective surface passivation reduces the number of non-radiative recombination pathways, increasing PL intensity.[252] The laser penetration depth of $\sim$ 80 nm meant that the heterostructures could not be used here; I show in Sec. 3.1.4 below that band bending in the underlying structure caused recombination to take place well away from the surface. As a result electron/hole recombination and PL signal were not limited by surface effects for modulation doped heterostructures. Therefore we used bulk (100) and (311)A wafers with no underlying heterostructure. These wafers were similar to those used as the basis for the epitaxial heterostructure growth.

Two treatments were prepared as outlined in Sec. 2.2.1 based on the $(NH_4)_2S_x$ stock solution. The 'weak' treatment consisted of a 2 min dip in a 0.5% dilution of the stock solution in H_2O. The 'strong' treatment involved immersion in the stock solution for 10 mins. The weak treatment was used on most devices due to concerns about the ability of $(NH_4)_2S_x$ to etch GaAs. Etching the thin 5 nm GaAs cap on the heterostructure wafer would risk exposing the AlGaAs layer, which strongly oxidises if exposed to air. A 30 s dip in 31% HCl:H_2O prior to sulfur treatment was used to ensure the surface was de-oxidised. We restricted our attention to aqueous $(NH_4)_2S_x$ treatments due to compatibility issues with photoresist. To limit the exposure to light and oxygen, the gate pattern was defined in the photoresist layer prior to treatment (see Fig. 3.1(b)). This enabled the devices to be loaded into the metal evaporator and under vacuum of $<$ 1 mTorr in less than 5 minutes. Alcoholic solutions based on, e.g., isopropanol and 2-methyl-2-propanol have been suggested as more effective in some circumstances.[21,44] We found that immersion in these solutions dissolved significant portions of the photoresist during the 2 minute weak treatment; often the resist was removed entirely. Figure 3.1(c) shows that attempting metal evaporation after treatment in a 2% mixture of the stock solution in isopropanol prior to gate deposition resulted in unwanted metal covering large regions of the device.

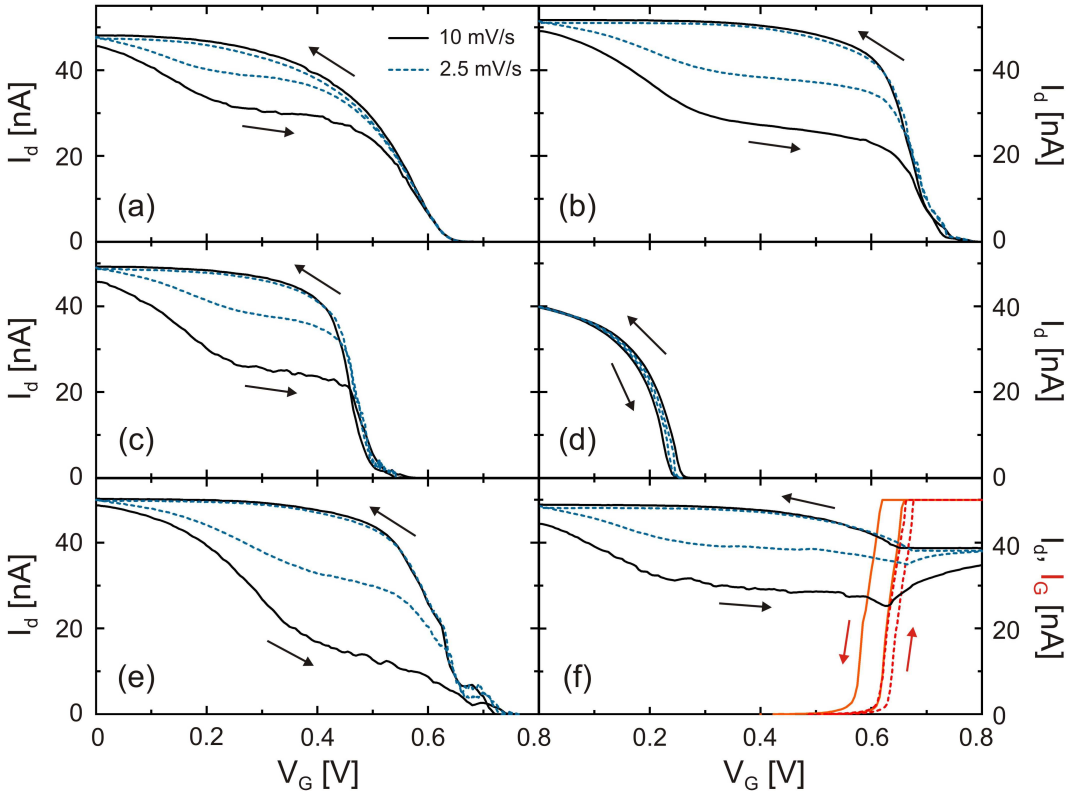

FIGURE 3.2: I_d vs V_G for devices with (a) no treatment, (b,c,d) weak treatment, (e) strong treatment and (f) strong treatment plus annealing at 360°C prior to gate deposition. The gate was incremented at 10 mV/s (black solid line) and 2.5 mV/s (blue dashed line). The device in (f) exhibited gate leakage with current I_G (red solid and dashed lines) above $V_G = 0.61$ V.

3.1.2 Performance of $(NH_4)_2S_x$ treated heterostructure devices

The I_d vs V_G characteristic for an untreated p-AlGaAs/GaAs device at $T = 4.2$ K is shown in Fig. 3.2(a). An ac excitation $V_{sd} = 100$ μV at 73 Hz was applied to the source and I_d detected at the drain by a lock-in amplifier. V_G was supplied by a Keithley K2400 source measure unit, which simultaneously monitored gate leakage current I_G. The anti-clockwise, rate-dependent hysteresis loop is consistent with trapping of charge in long lived surface states and charge migration amongst dopants in the AlGaAs layer.[24] The data can be compared with Fig. 1.7, albeit with a reversed hysteresis direction due to the reversal of the sign of the charge carriers. A striking feature of the data in Fig. 3.2(a) is the I_d plateau at intermediate V_G

on sweeps towards depletion. Comparison of these devices with n-AlGaAs/GaAs HEMTs at $T \geqslant 120$ K in Ref. 24 led us to conclude that the I_d plateau was due to the gate induced filling of a high density of surface states.[24] This is supported by the results to follow. During this plateau, the I_d dependence on V_G is reduced significantly as the electric field causes charge to be trapped in surface states at the expense of causing depletion of holes in the 2DHG. Depletion resumed only once all the surface states were filled, allowing the device to reach pinch-off, i.e., where $I_d = 0$. The plateau length and pinch-off voltage V_{po} therefore provide a measure of relative surface state density between devices; a longer plateau and higher V_{po} implies a higher surface state density. One example of this was shown in Fig. 1.18 of Sec. 1.4.5, where adding an Al_2O_3 insulating layer between the gate and semiconductor increased the plateau length to $3 - 4$ V, consistent with increased Ga-O and As-O bonding and other interface defects.[40,258]

To investigate the effectiveness and reliability of $(NH_4)_2S_x$ treatments on (311)A GaAs, the weak treatment was applied to five separate devices. Electrical characteristics from three of these devices are shown in Figs 3.2(b/c/d). There is significant variability in device characteristics, especially I_d plateau length and V_{po}. The latter varied between $V_{po} = 0.25$ to 0.8 V across the five measured devices, despite each undergoing a nominally identical surface treatment prior to gate deposition. The I_d vs V_G characteristics of the two other devices we measured, but have not shown here, most resemble the device in Fig. 3.2(b). This same variability is not seen in devices with no sulfur treatment; the characteristics all strongly resemble those in Fig. 3.2(a). This suggests that the treatment altered (311)A GaAs surface states, and supports the designation of the I_d plateau as arising from surface states. However, $(NH_4)_2S_x$ treatments clearly produced a highly variable effect on mid-gap surface state density. The longer I_d plateau and higher V_{po} for the device in Fig. 3.2(b) suggests an *increase* in surface state density. By contrast, the I_d plateau length – and therefore surface state density – was reduced for the device in Fig. 3.2(c) and eliminated entirely for the device in Fig. 3.2(d). The dramatic reduction in hysteresis for this latter device unfortunately was an isolated occurrence; although the data was repeatable for the same

device on separate cool downs, the low hysteresis was not reproducible for any other subsequently fabricated device. Additionally, it is not clear that the data obtained from this device was a result of complete surface state elimination. It could be that the surface state spectrum was shifted away from the Fermi level at $V_G = 0$ V. This could have facilitated pinch-off at lower V_G, before the Fermi level reached the highest surface state density. The two devices in Figs 3.2(b/c) also underwent increased depletion before the onset of the I_d plateau compared to the untreated device in Fig. 3.2(a). The device in Fig. 3.2(d) may simply represent an extreme variation of this behaviour.

A possible concern about the devices in Figs 3.2(b-d) is that the weak treatment was insufficient to provide complete passivation. To test this, the strong treatment was applied to the device in Fig. 3.2(e). This treatment modified the form of the hysteresis, facilitating increased depletion at low V_G and weakening the I_d plateau. However, V_{po} was not significantly altered. This is indicative of a change in the surface state distribution rather than an appreciable reduction in the overall density. A further issue is that instability increased at low I_d around pinch-off. The QPCs and quantum dots outlined in Sec. 1.4 all operate in this region, e.g., quantum dots operating down to the last electron typically have I_d in the nA to pA range. The introduction of noise/instability at low I_d would make any treatment incompatible with low dimensional electrostatic confinement.

One commonly used method to further alter the surface state distribution is post-passivation annealing.[44] The differing energetics and stability of Ga-related and As-related bonds means that annealing the treated (100) GaAs suface to over 350°C transfers sulfur atoms from As-S bonds to Ga-S bonds.[59–61] This can be beneficial or detrimental, depending on the relative importance of these bonds for a particular application. To ascertain the effect this has on the (311)A-oriented devices, we annealed one device to 360°C for 10 mins in Ar after treatment with the strong solution. Annealing at this temperature would not be possible with the photoresist already on the surface; the resist would either strongly adhere to the surface or undergo pyrolysis. As such we performed treatment and annealing prior to photoprocessing. Gate definition and metallisation was conducted as

soon as possible afterwards, ensuring the device was kept in the dark as much as possible. I showed in Ref. 32 that the passivation effect can be preserved on (100) surfaces throughout the photoprocessing process by minimising exposure to illumination. Doing so is not ideal, hence our earlier desire to limit treatments to those compatible with photoprocessing. The data in Fig. 3.2(f) suggests that annealing was detrimental to device performance, especially in the re-emergence of a prominent I_d plateau compared to Fig. 3.2(e). Significant gate leakage occurred for $V_G > 0.61$ V, possibly due to additional diffusion of Be from the ohmic contacts shorting to the gate. The fast diffusion of Be in GaAs is well established,[239] and although the temperature of this anneal was lower than that used to form ohmic contacts, the 10 minute annealing time was much longer. These results point to importance of As-S bonding in the partial passivation observed for the other (311)A devices.

The device characteristics in Fig. 3.2 show that the $(NH_4)_2S_x$ treatment modifies the surface properties of the (311)A GaAs surface. However, it did not provide effective passivation and the resulting device behaviour was highly variable. We turned to XPS and PL on both (100) and (311)A GaAs surfaces to ensure that our treatment was correctly formulated and reproduced literature results. PL was also used to provide a secondary evaluation of the effectiveness of the solution in terms of reducing (311)A GaAs surface state density.

3.1.3 XPS of $(NH_4)_2S_x$ treated surfaces

XPS was performed on four different samples: an untreated reference sample from each of the (100) and (311)A heterostructure wafers, and one sample each from the (100) and (311)A wafers that underwent the weak treatment. The samples were kept in the dark for the $\sim$ 10 mins prior to being loaded into the XPS chamber and placed under vacuum. XPS and peak fitting was conduced by Dr Bill Bin Gong at the Mark Wainwright Analytical Centre, UNSW. The As($2p_{3/2}$), Ga($2p_{3/2}$) and S(2p) core level spectra are most relevant for GaAs S-passivation, and data from each of the four devices are shown in Fig. 3.3.

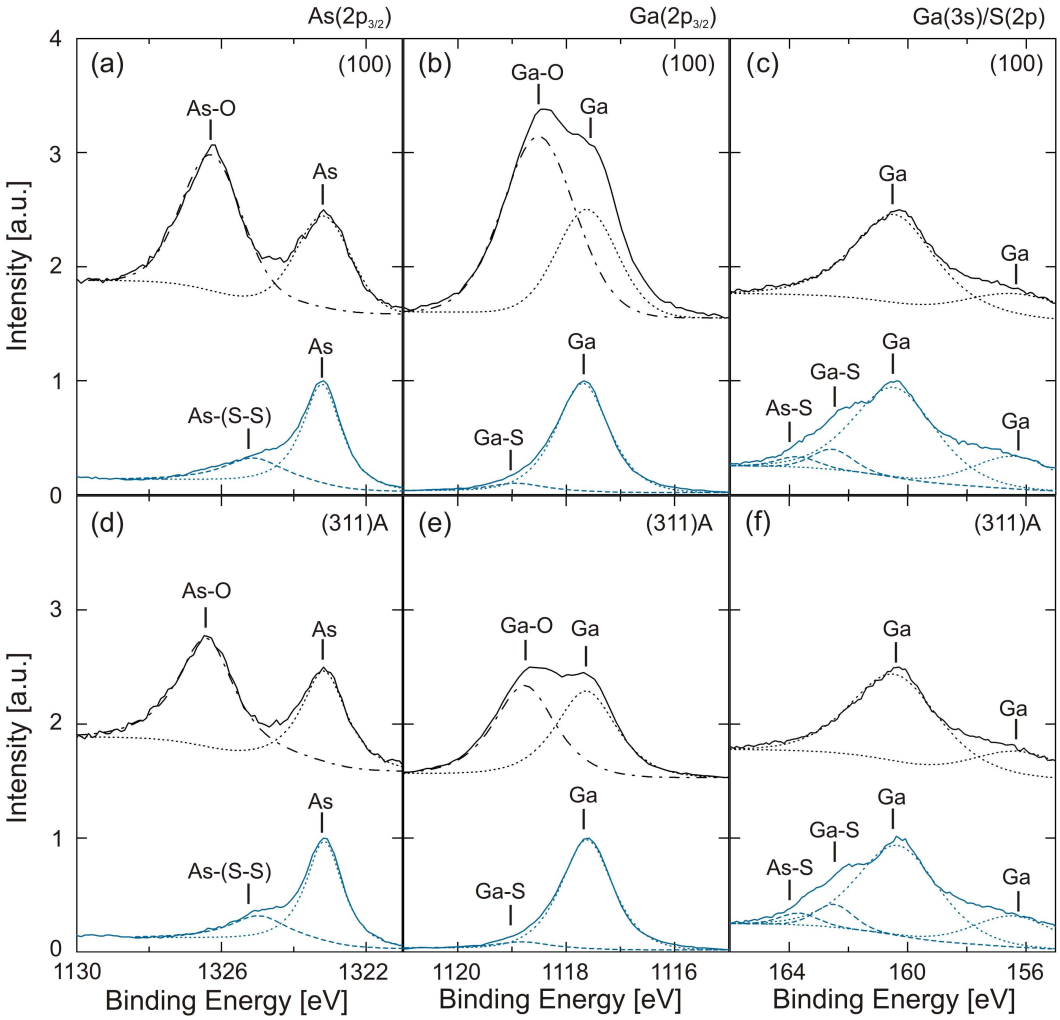

FIGURE 3.3: X-ray photoelectron spectra for (a/b/c) (100) oriented and (d/e/f) (311)A oriented GaAs surfaces without (black) and with (blue) weak $(NH_4)_2S_x$ treatment. Solid lines represent the measured XPS signal. Dashed and dotted lines are fits to the marked peaks, assigned according to the expected bond binding energy. Each signal was normalised to the relevant Ga/As peak, and the black traces were offset vertically by 1.5 for clarity. $(NH_4)_2S_x$ treatment stripped the surface oxide and resulted in Ga-S and As-S bonding for both (100) and (311)A surfaces.

Looking first at the As($2p_{3/2}$) in Figs 3.3(a/d), both untreated samples show clear peaks related to GaAs and As_2O_3 at 1323.2 eV and 1326.3 eV, respectively. The latter peak was eliminated in the treated samples and replaced by a peak at 1324.5 eV that is commonly associated with As-(S-S), i.e., the formation of disulfide bridges bonded to surface As.[57] The As-(S-S) peak intensity was the same for both (100) and (311)A GaAs. Similarly, the untreated surfaces in Fig. 3.3 show

$Ga(2p_{3/2})$ peaks related to GaAs and Ga_2O_3 at 1117.4 eV and 1118.5 eV, respectively. The peak height for Ga_2O_3 on the (311)A surface was twice as small as that for (100). This likely reflects the different valency of Ga surface atoms on the two surfaces;[105,259,260] (100) Ga surface atoms are divalent and hence bind twice as much oxygen as the monovalent Ga atoms at the (311)A surface. After treatment, the Ga-O peaks were removed. A small peak at higher binding energy, $\sim$ 1119 eV emerged. Due to the low intensity it is not clear whether this can be conclusively assigned to Ga-S bonds.[253] It may have arisen from a residual Ga-O component also. Finally, the Ga(3s) spectra is not sensitive to oxygen bonding, and thus only shows two GaAs related bonds for untreated samples (Figs 3.3(c/f)). The interest in this binding energy range is that the S(2p) spectra overlap the Ga(3s) spectra. The spectra of treated samples includes Ga-S and As-S related bonds, with a similar peak intensity on both treated (100) and (311)A GaAs.[253,261] The As-S signal is possibly related to the disulfide bridges seen in the $As(2p_{3/2})$ spectra.[261]

The XPS results show that the weak $(NH_4)_2S_x$ treatment provided the expected result for (100) GaAs surface chemistry; the oxide layer was removed and replaced by Ga-S and As-S bonds. The similarity of results for (311)A strongly supports the notion that de-oxidisation and sulfidisation occurs equivalently for (311)A also. However, the ineffective passivation observed from device performance in Fig. 3.2 suggests that the treatment does not result in a low density of band-gap surface states for the (311)A surfaces. To provide independent evidence for this, I turn now to photoluminescence studies.

3.1.4 Photoluminescence of $(NH_4)_2S_x$ treated wafers

Figures 3.4(a/b) show PL spectra for (100) and (311)A GaAs wafers after receiving the weak $(NH_4)_2S_x$ treatment. The signal arises from band-to-band recombination, with the peak intensity occurring at the room temperature GaAs band gap energy $E_g = 1.42$ eV $= \frac{hce}{873 \text{ nm}}$. The peak intensity for each of the (100) and (311)A samples was normalised to the peak height obtained from an untreated reference sample from the same wafer. The raw, un-normalised data from these reference

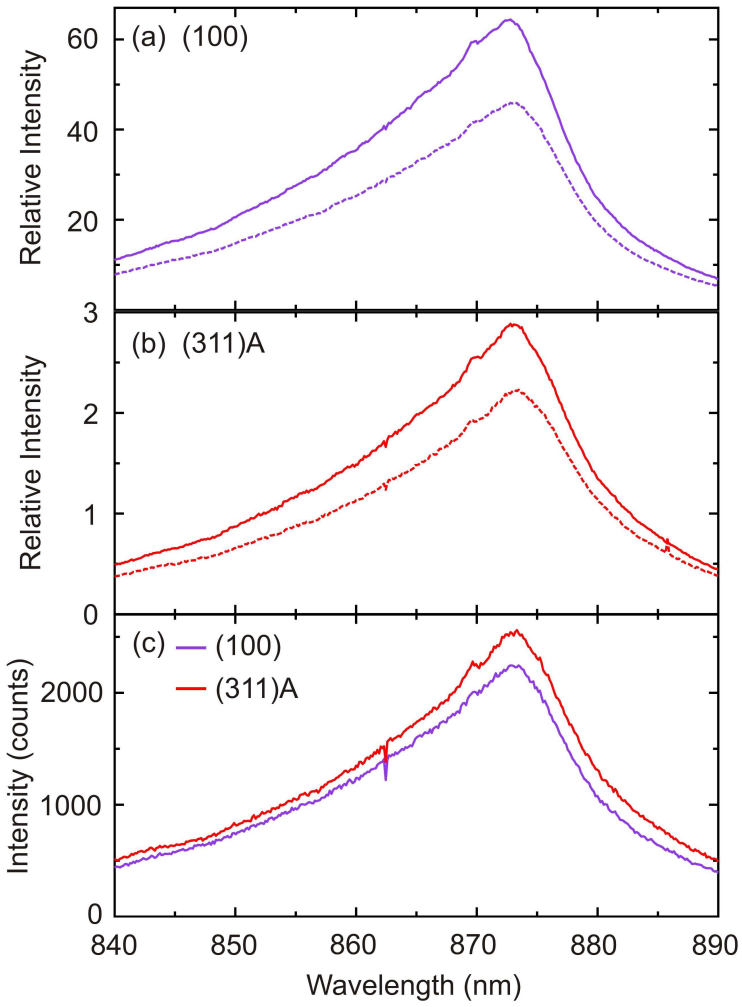

FIGURE 3.4: (a/b) Photoluminescence spectra from two different samples for each of the (100) and (311)A surfaces after receiving the weak $(NH_4)_2S_x$ treatment. (c) PL spectra for the untreated (100)/(311)A reference samples (purple/red line respectively). Peak intensity of each sample in (a/b) was normalised to the associated reference sample with the same orientation. The intensity in (c) from the reference samples is given in raw counts detected by the CCD camera. The $40-60\times$ increase in PL peak intensity for treated (100) GaAs is indicative of surface state passivation and the associated reduction in non-radiative recombination pathways. The comparatively small increase for (311)A GaAs suggests $(NH_4)_2S_x$ does not effectively passivate this surface.

samples in shown in Fig. 3.4(c). The PL peak intensity for $(NH_4)_2S_x$ treated (100) GaAs surfaces was increased $40-60\times$ compared to the untreated reference sample. The enhanced PL signal arises from the reduction of non-radiative recombination pathways due to effective surface state passivation.[44,53,252] By contrast, the same treatment produced only a $2-3\times$ increase in PL intensity for (311)A GaAs surfaces. Such a small PL intensity increase suggests the band-gap surface

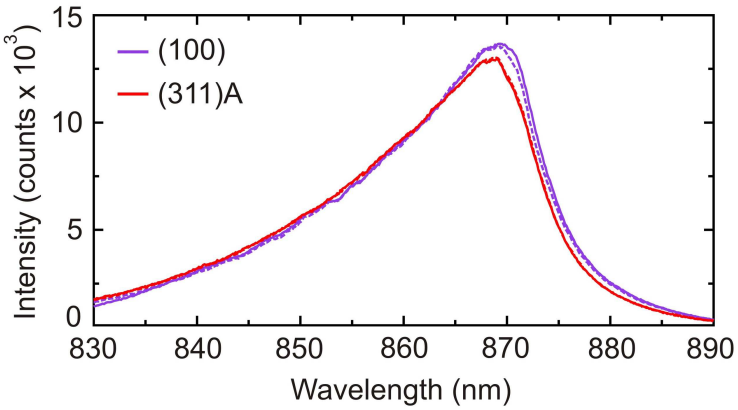

FIGURE 3.5: Photoluminescence spectra for treated/untreated (100) (purple solid/dashed lines) and treated/untreated (311)A (red solid/dashed lines) AlGaAs/GaAs heterostructures. $(NH_4)_2S_x$ treatment did not alter the PL signal as recombination was not limited by the surface in these samples (see text).

state density was not appreciably reduced by $(NH_4)_2S_x$ treatment and subsequent sulfidisation. This corroborates the conclusions drawn from the gate-dependent electrical measurement of devices presented in Sec. 3.1.2.

The shift from electrical/XPS measurements to PL measurements entailed a change of wafer. Initial PL measurements were conducted with pieces from a matched pair of (100) oriented *n*-type and (311)A oriented *p*-type heterostructure wafers used for the devices in Sec. 3.1.2 and Ref. 24. As shown in Fig. 3.5, no PL enhancement was observed for either $(NH_4)_2S_x$ treated wafer. To explain this, consider that the laser penetration depth in GaAs/AlGaAs is approximately 80 nm at a wavelength $\lambda = 488$ nm. This excitation would have generated electron/hole pairs well into the bulk of the modulation doped wafer. The band bending of the heterostructure may then have provided an effective barrier for surface recombination. In this case, no recombination would have taken place *via* surface states for even the untreated samples, and surface state reduction would have no appreciable affect on PL intensity. Another possible alternative for the lack of PL intensity increase could be that the high density of impurities in the AlGaAs doping layer dominates non-radiative recombination. However, this is a less likely scenario as significant PL gain has previously been observed for bulk samples with similar doping density $N_{Si} \sim 10^{16}$ cm^{-3}.[43,44,252] In any case, the PL signal of modulation

doped wafers was not sensitive to changes in surface state distribution. Accurately probing comparative surface dynamics between the (100) and (311)A surfaces by PL necessitates only that other properties of the wafer are roughly the same. This justifies the use of the bulk materials in this case.

3.1.5 Possible causes of ineffective passivation

The above results show that $(NH_4)_2S_x$ alters the bare (311)A GaAs surface by removing the oxide layer and generated Ga-S and As-S bonds, as for (100) GaAs. However, it did not produce a similarly substantial increase in PL intensity and no reliable improvement in the performance of *p*-AlGaAs/GaAs HHMTs. This was characterised by sweep-rate dependent hysteresis and an I_d plateau where the filling of surface states suppressed hole depletion and changed the pinch-off voltage V_{po}. The changing length and slope of the I_d plateau and the corresponding shifts in V_{po} pointed to a modification of the surface state distribution, but no consistent reduction in the overall density. It is apparent that $(NH_4)_2S_x$ does not passivate the (311)A surface in the same way as it does for (100) GaAs, and results in surface states with energies that fall within the band gap.

We postulate that the nature of (311)A GaAs surface bonds can explain the ineffective passivation of this surface. Given the scarcity of previous work on the (311)A surface, we turn to the known properties of lower index planes. Higher Miller index planes can be considered linear combinations of lower-index Miller planes; specifically, the bare (311)A GaAs surface consists of (111)A-like single dangling bonds for Ga and (100)-like double dangling bonds for As.[105] I now use previous work on (111)A and (100) sulfidisation to provide possible explanations for our data.

Looking first at Ga bonding, the success of sulfur passivation for (100) arises in part from the Ga-S-Ga bridge bonds covalently satisfying the Ga double-dangling bonds at this surface.[21,44,59,60,262,263] By contrast, surface Ga atoms only have a single dangling bond as three of the four Ga bonds are satisfied by sub-surface Ga-As

bonding.[264] Adsorbed S atoms either bond directly on top of Ga surface atoms, or directly substitute at the Ga site.[264–267] Calculations suggest that both situations do not covalently satisfy S bonds; this leaves S-related dangling bonds and associated band gap surface states.[264] This is supported by experimental evidence for ineffective passivation of (111)A GaAs.[267] The similar Ga-S bonding state for (311)A is likely to have contributed to the ineffective passivation observed here.

Turning to As, XPS results in Fig. 3.3 showed that As-S bonds on (311)A mirror those on the (100) surface, as expected. The stability of As-related bonds is reduced compared to Ga-S bonds. While initial H_2O rinsing removes excess elemental As-As dimers and the associated band gap surface states,[261,268,269] prolonged water exposure breaks the weak As-S bonds and leads to a re-accumulation of surface As and As-O bonds.[253,261] The As-related surface states are below the surface Fermi level for (100) GaAs.[40] If the situation is similar for (311)A, a positive bias applied to the gate in Fig. 3.2 sweeps the surface Fermi level through these states. The variable I_d plateau length and V_{po} may well indicate this instability and unreliablilty of As-S bond formation, since a process as simple as natural variation of rinse time could have contributed to the difference between device characteristics. Similarly, post-treatment annealing to 360°C is likely to have broken As-S bonds[59–61] and lead to the re-emergence of limited low V_G depletion and the I_d plateau in Fig. 3.2(f). The combination of poor As-S bond strength combined with the likely unsatisfied Ga-S dangling bonds explains the insufficient and variable passivation of the (311)A GaAs surface.

The question then is: Is there a solution that can facilitate effective passivation of (311)A GaAs surfaces? The difficulty is that both single and double dangling bonds need to be satisfied. One possibility for satisfying the Ga-dangling bonds is a monovalent adsorbate such as Cl; positive results have been obtained on the (111)A GaAs surface.[270] Producing a solution that incorporated both S and Cl, e.g., S_2Cl_2[271,272] may hold interest as a general approach to passivating (311)A GaAs. In terms of this thesis, investigating alternative passivation solutions was unlikely to completely remove instability and hysteresis in modulation doped devices, due to

charge mobility in the dopant layer.[24] I turn to this influence now, using quantum interference effects in a hole quantum billiard.

3.2 Using magnetoconductance fluctuations to detect changes in dopant configuration

3.2.1 Background, sample and methods

Recent work highlighted in Sec. 1.4.4 has illustrated the impact of small-angle scattering on 'ballistic' transport in modulation doped heterostructures.[84,90,91] The tails of the potential generated by ionised dopant impurities in the AlGaAs layer was shown to cause deviations of electrons even as they travel between large-angle scattering sites.[84,88–91] The sensitivity of magnetoconductance fluctuations (MCF) in semiconductor billiards to electron trajectory and phase means that they are altered by changes in the background potential due to dopants in the AlGaAs layer. The strongest evidence for this was obtained by comparing $G(B)$ traces before and after thermally cycling billiards fabricated from modulation doped heterostructures. MCF became non-reproducible for thermally cycling to temperatures $T \geqslant 165$ K.[91] This matches the activation temperature for deep donor trapping sites known as DX centres[93,94,112] and gives strong evidence that the decorrelation of MCF traces occurs as a result of spontaneous reorganisation of the donor occupation distribution. This random process changed the form of the background disorder potential crossing the 2DEG and – at least in part – determined a different $G(B)$ signature *via* small-angle scattering of electrons.[84,90,91]

The sensitivity of MCF to small-angle scattering by dopant impurities opens up its use as a characterisation technique to detect changes in dopant configuration. As mentioned in relation to Fig. 1.19 in Sec. 1.4.5, comparison of the temperature dependence of electron and hole devices suggested that charge migration amongst dopant sites in response to V_G contributed to the hysteresis of modulation doped p-type AlGaAs/GaAs heterostructures.[24] In this section, I present results from a

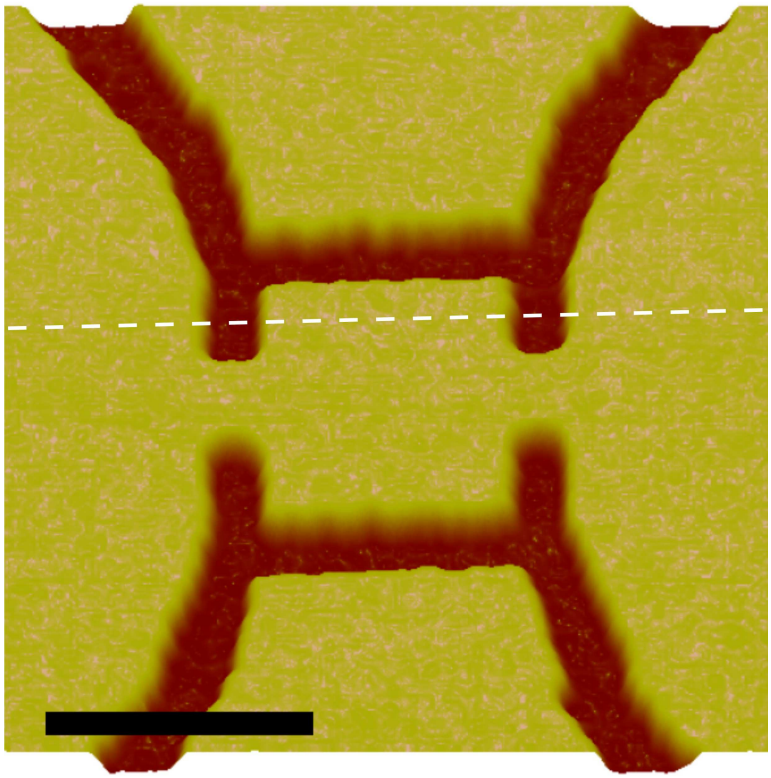

FIGURE 3.6: Atomic force micrograph of the etched square hole billiard prior to polyimide and gate deposition. The 120 nm deep trenches (red regions) define the billiard and entrance/exit QPCs that connected the billiard to the 2DHG. Lateral etching resulted in a billiard size slightly smaller than the 1 μm^2 pattern defined by EBL. The white dashed line shows the cut through the billiard used for the cross-sections in Figs 3.9 and 3.11 below. The scale bar represents 1 μm.

hole billiard fabricated using the hysteretic wafer. We measured MCF changes in response to applied V_G in a billiard made from this wafer as a way of confirming and characterising the dopant layer contribution to device instability. Fabrication of the Hall bar and ohmic contacts proceeded as per Sec. 2.2. We etched trenches in the AlGaAs layer to define the billiard rather than define it electrostatically due to gate instability presenting difficulties in confining the 2DHG.[24,106,108–110] The pattern was defined by EBL using PMMA-A3 and wet etching with a 1:8:259 H_2SO_4:H_2O_2:H_2O solution to a trench depth of 120 nm. The resulting billiard is shown in Fig. 3.6. The EBL pattern defined a 1 μm $\times$1 μm square with QPCs at the entrance and exit. Lateral etching resulted in slightly smaller billiard dimensions. The distance between billiard walls was much smaller than the mean free

path, estimated to be $\ell = 6.8$ μm. The billiard was covered in a 140 nm thick polyimide layer to prevent gate leakage from the trenches into the 2DHG. Polyimide acts as a negative photoresist and was therefore patterned directly. Polyimide has previously been used as a gate insulator for highly stable ambipolar GaAs/AlGaAs heterostructure devices.[273,274] The thin film was spun on at 6000 rpm for 60 s and baked at 65°C for 90 s. The regions that were intended to remain after developement were exposed to UV radiation at 10 mW/cm^2 for 70 s. Development in a dedicated developer removed the surrounding polyimide. The sample was then hard baked in a furnace at 250°C for 60 mins to render the remaining polyimide insoluble in alcoholic solvents. The top-gate pattern was then defined using photolithography, and 20/80 nm layers of Ti/Au were deposited by thermal evaporation.

Conductance G was measured using the 4-terminal techniques outlined in Sec. 2.4.1 using two lock-in amplifiers measuring I_d and V_{4T} on either side of the billiard in response to an ac excitation of $V_{sd}^{ac} = 100$ μV at 13 Hz. V_G was supplied by a Keithley K2400 SMU, which was also used to monitor gate leakage I_G. The leakage current remained below $I_G < 0.5$ nA throughout the experiment. A magnetic field $|B| \leqslant 10$ T was supplied by a superconducting solenoid and applied perpendicular to the 2DHG. The experiment was performed in the Kelvinox K100 dilution refrigerator outlined in Sec. 2.4.4, with a mixing chamber base temperature $T_B = 40$ mK. Heating the mixing chamber allowed continuous temperature variation up to $T = 900$ mK, with measurements also possible at thermal equilbrium with the ^{4}He bath, $T = 4.2$ K. We used a dilution refrigerator rather than the ^{3}He cryostat used by Scannell *et al.*[91] as lower temperatures $T < 100$ mK were required to observe hole MCF. This is because the higher hole effective mass generates stronger carrier-carrier interactions that reduce the phase coherence time compared to electrons.[275]

The majority of this experiment deals with differences in MCF for successive $G(B)$ traces. Often clearly different features will be apparent in the raw data. However, quantifying the magnitude of changes is necessary to draw conclusions about trends in the data. I now briefly outline the methods used in the following experiments.

Subtracting successive $G(B)$ traces is the simplest way to obtain the B-dependent difference in G, i.e.

$$\delta G(B) = G_2(B) - G_1(B) \tag{3.1}$$

Ideally $\delta G(B) = 0$ for all B where $G_2(B)$ and $G_1(B)$ were identical. In practice, differences in $G(B = 0)$ were hard to avoid, since device instability meant that G would sometimes drift very slightly even at constant V_G. As a result, $\delta G(B)$ would develop a constant offset. To deal with this, we defined the difference function $\Delta(B)$

$$\Delta(B) = \delta G(B) \; - \; \langle \delta G(B) \rangle \tag{3.2}$$

where the subtraction of the average difference $\langle \delta G \rangle$ accounts for any offset. The function $\Delta(B)$ is zero for all B if two $G(B)$ traces are identical, and develops oscillations around 0 when differences in the MCF emerge. These oscillations are larger for greater MCF differences and this can be quantified by the root-mean-square conductance difference:

$$RMS_\Delta = \langle \Delta(B)^2 \rangle^{\frac{1}{2}} \tag{3.3}$$

The RMS_Δ will be used to quantify the degree of MCF difference between traces. This can be normalised to a number between 0 (no correlation) and 1 (complete correlation) following Scannell *et al.*[91] using the autocorrelation function F:

$$F = \sqrt{1 - \frac{\Delta(B)^2}{N}} \tag{3.4}$$

where N is a normalisation function, equal to the average $\Delta(B)^2$ of completely de-correlated traces.[91,92] N was obtained by randomly generating 100 different $G(B)$ traces and taking the average of the conductance difference $N = \langle (G_x(B) - G_y(B))^2 \rangle$. Each of the random traces $G_x(B)$ and $G_y(B)$ were constrained to have the same minima and maxima as the measured traces $G_1(B)$, $G_2(B)$. Thus F automatically takes a value between 0 and 1. Since MCF are dependent on density, we compared only traces where the conductance at zero-magnetic field $G(B = 0)$ matched to within a very small value, $0.05 \times 2e^2/h$. Analysis was performed only

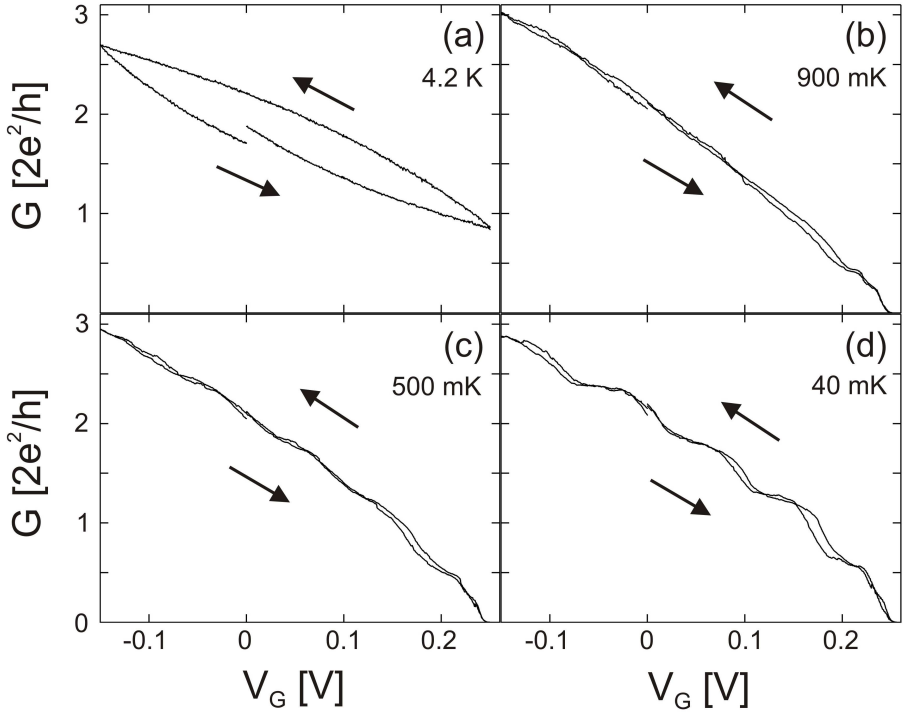

FIGURE 3.7: G modulation for V_G applied to the top gate covering the billiard at decreasing T. V_G was incremented at 1 mV/s. Hysteresis in (a) is consistent with that in Fig. 3.1.2 and reduces with decreasing T because the lower thermal energy suppresses charge hopping between acceptor sites. Conductance steps at $T = 40$ mK arise due to the entrance/exit QPCs.

for $|B| < 0.07$ T, where the cyclotron radius was larger than the billiard diameter. Fluctuations in $G(B)$ at higher B are due to tighter skipping orbits along the billiard walls, not MCF (see Fig. 1.14(d) in Sec. 1.4.3).

3.2.2 Gate characterisation

We first characterised the G dependence on V_G at $B = 0$ T for different temperatures, shown in Fig. 3.7. The hysteresis observed at $T = 4.2$ K is consistent with that shown in Fig. 3.2. The magnitude of the hysteresis decreases as the temperature is lowered because k_BT becomes smaller relative to the trap depth, but the hysteresis is still present at $T = 40$ mK. The conductance steps at $T = 40$ mK are due to the QPCs at the entrance/exit of the billiard. The non-additivity of QPCs in series with separation less than the mean free path is known to produce steps that do not align with integer values of the conductance quantum $G_Q = 2e^2/h$.[276,277]

The persistence of hysteresis at low T means that these characteristics provide only a guide to device behaviour. Throughout the experiment the characteristics in Fig. 3.7(d) were displaced horizontally in response to shifts and drifts in G at constant V_G – this is explored in the next section. A consequence of the non-monotonic $G(V_G)$ relationship is that moving away from and returning to the same V_G results in different $G(B = 0) \equiv G_0$. The need to compare traces with similar G_0 meant that traces were taken at whichever V_G gave the desired G_0. Typically this was on a conductance plateau, e.g., $G_0 = 1.8\ G_Q$ where the G_0 dependence on V_G is weak. Here, small differences in V_G settings would result in minimal variation between G_0 values.

3.2.3 Temporal stability of MCF at constant V_G

The presence of hysteresis indicates that charge in the dopant layer may still be active at $T = 40$ mK. We examined the temporal stability of MCF at constant V_G with two objectives. Firstly, to ensure that stability was maintained during the ~ 20 min $G(B)$ traces and that $G(B)$ provided a reliable 'fingerprint' of the background disorder potential. The second objective was to observe any changes in the background potential. Depending on the relationship between trap depth and thermal energy, these changes may have two sources. The first is from spontaneous reorganisation due to random thermal fluctuations, and the second is charge migration driven by a static V_G. To collect this data, $G(B)$ was measured at times $t = 0, 8$ and 15 hours with constant V_G. The traces taken at $t = 8$ and 15 hours were compared with the trace at $t = 0$ to look for changes in MCF. These changes could also be clearly identified using the conductance difference $\Delta(B)$ with $\delta G(B) = G(B, t) - G(B, 0)$ where $t = 8, 15$ hours.

Figures 3.8(a/b) show this experiment for two $V_G = -58.5$ mV and -156 mV, which were set to give $G_0 = 1.8\ G_Q$ and $2.5\ G_Q$, respectively. Each MCF trace was symmetrical, $G(B) = G(-B)$, showing that at these V_G, the disorder potential did not evolve appreciably during each trace. Further, the MCF at $V_G = -58.5$ mV

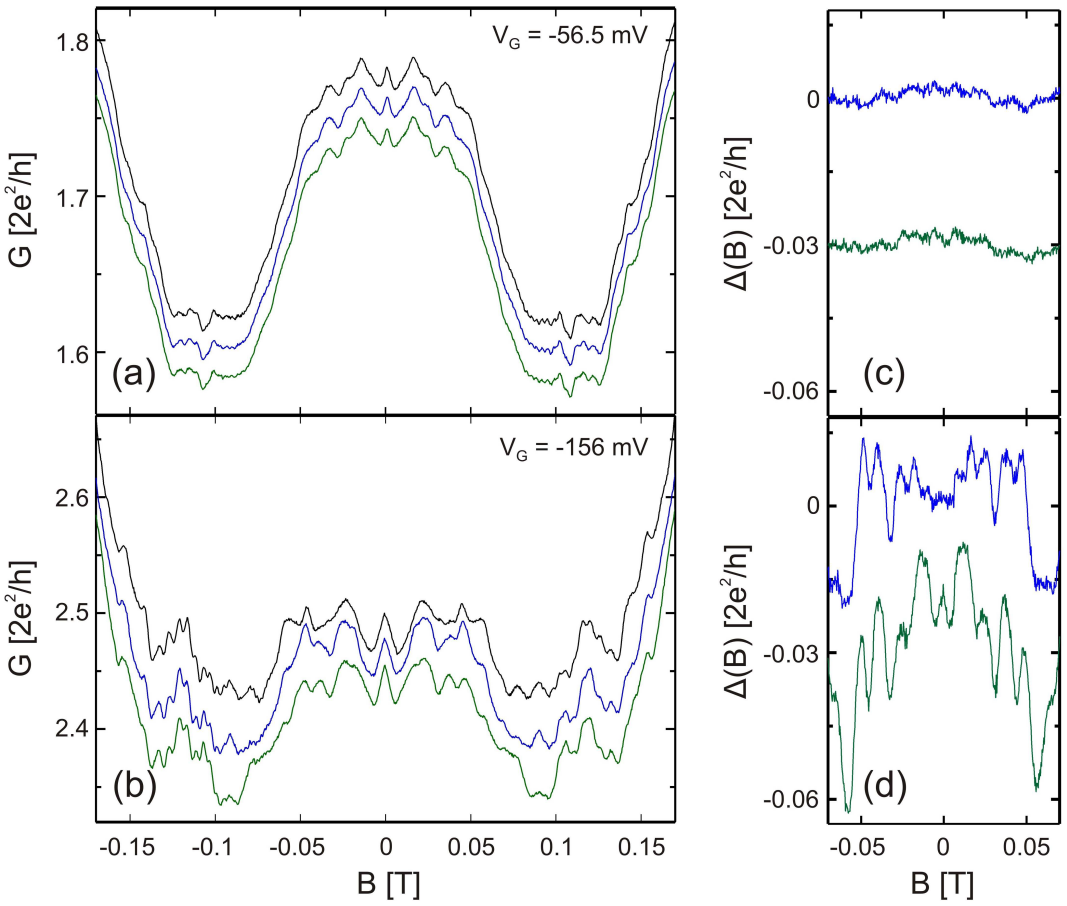

FIGURE 3.8: (a/b) $G(B)$ at constant $V_G = -58.5$ mV and -156 mV, with G_0 set to (a) 1.8 G_Q and (b) 2.5 G_Q at time $t = 0, 8$ and 15 hours (black, blue, green traces respectively). Traces were offset vertically for clarity by 0, 0 and -0.02 G_Q in (a) and 0, -0.04 G_Q and -0.07 G_Q in (b), from top to bottom. The inconsistent offsets were due to random jumps and drifts in G at constant V_G due to the commonly observed gate instability of p-AlGaAs/GaAs devices. (c/d) Conductance difference $\Delta(B) = \delta G(B) - \langle \delta G(B) \rangle$ corresponding to data in (a/b) for $\delta G(B) = G(B,t) - G(B,0)$ with $t = 8$ hours (blue traces) and 15 hours (green traces). The green traces were offset vertically by -0.03 G_Q. $\Delta(B) \sim 0$ for $G_0 = 1.8$ G_Q, $V_G = -58.5$ mV but develops increasing fluctuations over time for $G_0 = 2.5$ G_Q, $V_G = -156$ mV as more negative V_G drives charge migration between Si-acceptor sites in the AlGaAs layer.

did not evolve over the 15 hour period; the three traces in Fig. 3.8(a) were practically identical. This suggests that the system was stable at $V_G = -58.5$ mV on a long time scale. There were no spontaneous reorganisation events in the dot vicinity, and the configuration was not changed by V_G. Conversely, changes emerged between the three traces at the more negative gate voltage, $V_G = -156$ mV in Fig. 3.8(b), indicative of a temporal evolution of the underlying disorder potential.

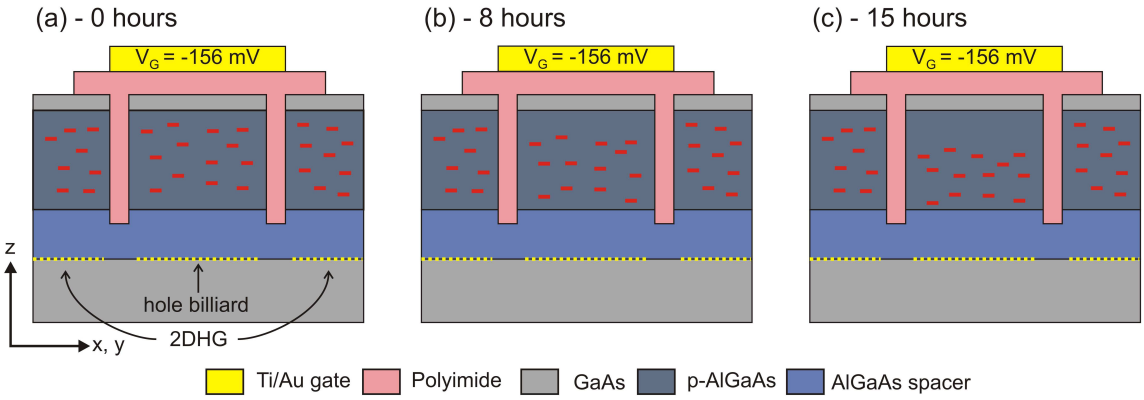

FIGURE 3.9: (a/b/c) Cross-section of the hole billiard along the white dashed line in Fig. 3.6 at $t = 0, 8$ and 15 hours. The billiard was defined by etching the heterostructure, which caused selective depletion of the 2DHG in the x, y plane. (a) At $t = 0$ hours negatively charged impurity sites were randomly located. (b/c) Negative V_G caused a slow migration of holes towards the gate, leading to a higher density of negative impurities closer to the billiard. The configuration was driven further from the initial configuration over longer times. This was sensed as MCF changes in Figs 3.8(b/d).

The different behaviour at different V_G is clearly demonstrated in the respective $\Delta(B)$ vs B plots shown in Figs 3.8(c/d). The conductance difference $\Delta(B)$ was close to zero for all B at $V_G = -58.5$ mV (Fig. 3.8(c)), confirming that negligible changes in MCF occurred even after 15 hours at this gate voltage. For $V_G = -156$ mV in Fig. 3.8(d) however, $\Delta(B)$ developed oscillations around 0. The increasing magnitude of $\Delta(B)$ oscillations shows that the MCF had changed more after 15 hours than they had after 8 hours. This is consistent with a continual evolution of the background potential over time as it was driven further away from the initial state at $t = 0$.

The MCF evolution in Figs 3.8(b/d) must be due to an underlying change in disorder potential since neither the hole density or billiard geometry changed during this time.[84,90,91] The likely cause of this behaviour is that V_G drives charge hopping between acceptor sites in the AlGaAs layer. This process is illustrated in Fig. 3.9. Charge migration occurs because the equilibrium impurity charge distribution at each V_G is not the equilibrium distribution at $V_G = 0$; more negative V_G means that a higher positive charge density towards the gate is a more favourable configuration. As such, negative V_G will drive hopping of holes between impurity sites

towards this new equilibrium configuration, leaving a high density of negatively charged ionised impurities in proximity to the 2DHG. More positive V_G will cause migration in the opposite direction. This process will be slow for thermal energy similar to or less than the acceptor trap depth, $k_BT \lesssim E_A$, and contributes to the hysteresis in I_d vs V_G. By reducing the available thermal energy further at $T = 40$ mK the time scale for the migration was dramatically increased, i.e., 8 to 15 hours. This slow migration towards a new equilibrium configuration was sensed by the MCF changes in Figs 3.8(b/d).

Related to this, the question may be asked: What about other small-angle scattering centres? In particular, could surface states be responsible for the observed MCF changes? We suggest that in the modulation doped sample used here, the much higher density of acceptor impurities separated from the 2DHG by $\sim 40 - 120$ nm are extremely likely to dominate the background potential and small-angle scattering effects, compared to surface state charges located 120 nm away from the 2DHG. While small-angle scattering from surface charges has been suggested to occur for shallow 2DEGs in heterostructures *without* modulation doping, it was shown to be strongly suppressed for 2DEG depths of > 100 nm.[25,26] This highlights the importance of the proximity of the scattering centres to the 2DEG/2DHG. The two major differences between this work and that of Mak *et al.*[25] and Wang *et al.*[26] is that the 2DHG is 120 nm below the surface in the sample here, with a high density of ionised dopants in the modulation doped layer. As such, charge in the dopant layer is likely to dominate the background potential in this device. A separate argument towards this is that (100) surface states are also active in n-AlGaAs/GaAs heterostructures, but are comparatively shallow traps with different trapping time scales.[24] The time scales meant that surface charges did not produce hysteresis, and instead caused non-linearities in I_d vs V_G (see Ref. 24, in particular the discussion relating to Figure 3 of that paper). If true, these surface charges were active in the modulation doped electron billiards used in Scannell *et al.*[91], See *et al.*[90] and all other billiard studies.[65,82,83] Yet gate-induced MCF changes were not observed, likely due to the domination of small-angle scattering by charges in the modulation doping layer. I will therefore assume hereafter

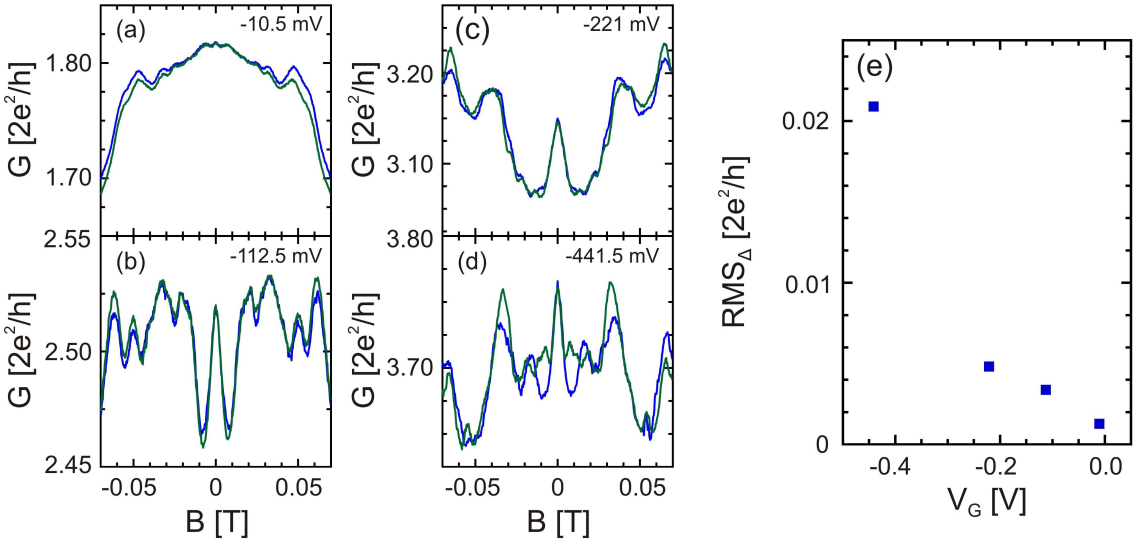

FIGURE 3.10: (a-d) $G(B,t)$ for $t = 0$ and 1 hr (blue and green traces respectively) at $V_G = -10.5, -112.5, -221$ and -441.5 mV. The green traces were offset vertically by (a) 0.015 G_Q, (b) 0, (c) 0.015 G_Q and (d) 0.05 G_Q to align G_0 to facilitate easy identification of changes in $G(B)$. Greater differences between traces are apparent at more negative V_G. (e) Root-mean-square conductance difference $RMS_\Delta = \langle \Delta(B)^2 \rangle^{\frac{1}{2}}$ between the two traces in each panel plotted against V_G. Higher V_G caused greater de-correlation between $G(B)$ traces due to increased charge migration between Si-acceptor sites in the AlGaAs layer.

that MCF changes arose due to changes in the charge configuration amongst Si-acceptors in the AlGaAs layer.

3.2.4 Evolution of MCF with gate modulation

The data in Fig. 3.8 showed larger conductance differences at the more negative gate voltage. This suggests that the stronger electric field drove more pronounced charge migration. To confirm this effect, we took pairs of $G(B)$ traces one hour apart at increasingly negative V_G, shown in Figs 3.10(a-d). The traces at higher V_G are noticeably altered after 1 hour. The RMS_Δ for each $\Delta(B)$ between the two traces at constant V_G is plotted in Fig. 3.10(e). RMS_Δ increased with more negative V_G, supporting the notion that an increasing electric field strength drives charge in the dopant layer further from its initial configuration over time.

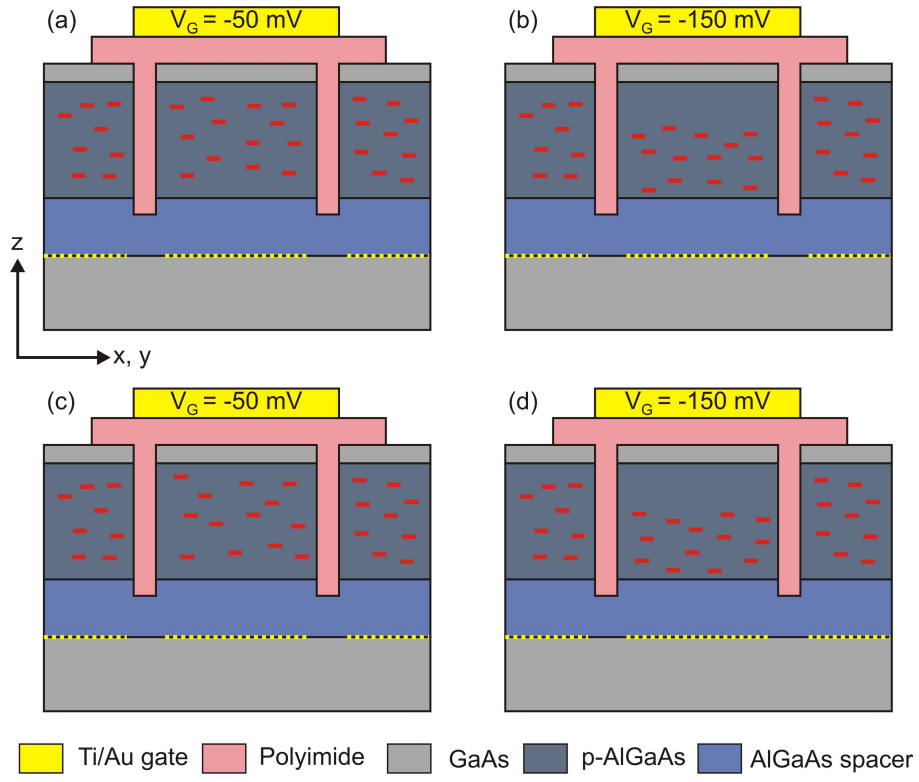

FIGURE 3.11: Device cross-sections along the cut in Fig. 3.6 illustrating a possible scenario for the effect of gate sweeps on the charge configuration in the dopant layer. From (a) to (b), V_G was swept to more negative V_G and then from (b) to (c) it was swept back to the original value. This perturbed the charge distribution in the dopant layer. Upon returning to the original V_G in (c), the density distribution was similar to that in (a), however the charges were not returned to their exact initial configuration. This scenario is likely to occur if there are a large number of trap sites compared to the number of holes. The process would also occur for an experiment starting at (b), sweeping to more positive V_G in (c) and returning to the more negative V_G in (d).

The data in Figs 3.8 and 3.10 show that V_G drives a change in the underlying disorder potential, and that this change was detected by the MCF in the hole billiard. An interesting question is whether particular impurity charge configurations are repeatable. For example, consider collecting MCF for $G_0 = 1.8\ G_Q$, then sweeping V_G away from this initial value to induce charge migration amongst impurities. If V_G is returned to where $G_0 = 1.8\ G_Q$ and a final MCF trace is collected, will the initial and final $G(B)$ traces match? Or is the impurity configuration such that charges are highly unlikely to be returned to the initial state, causing a de-correlation of MCF traces? The latter scenario for this experiment is shown in Fig. 3.11. It would occur if the number of charges is small compared

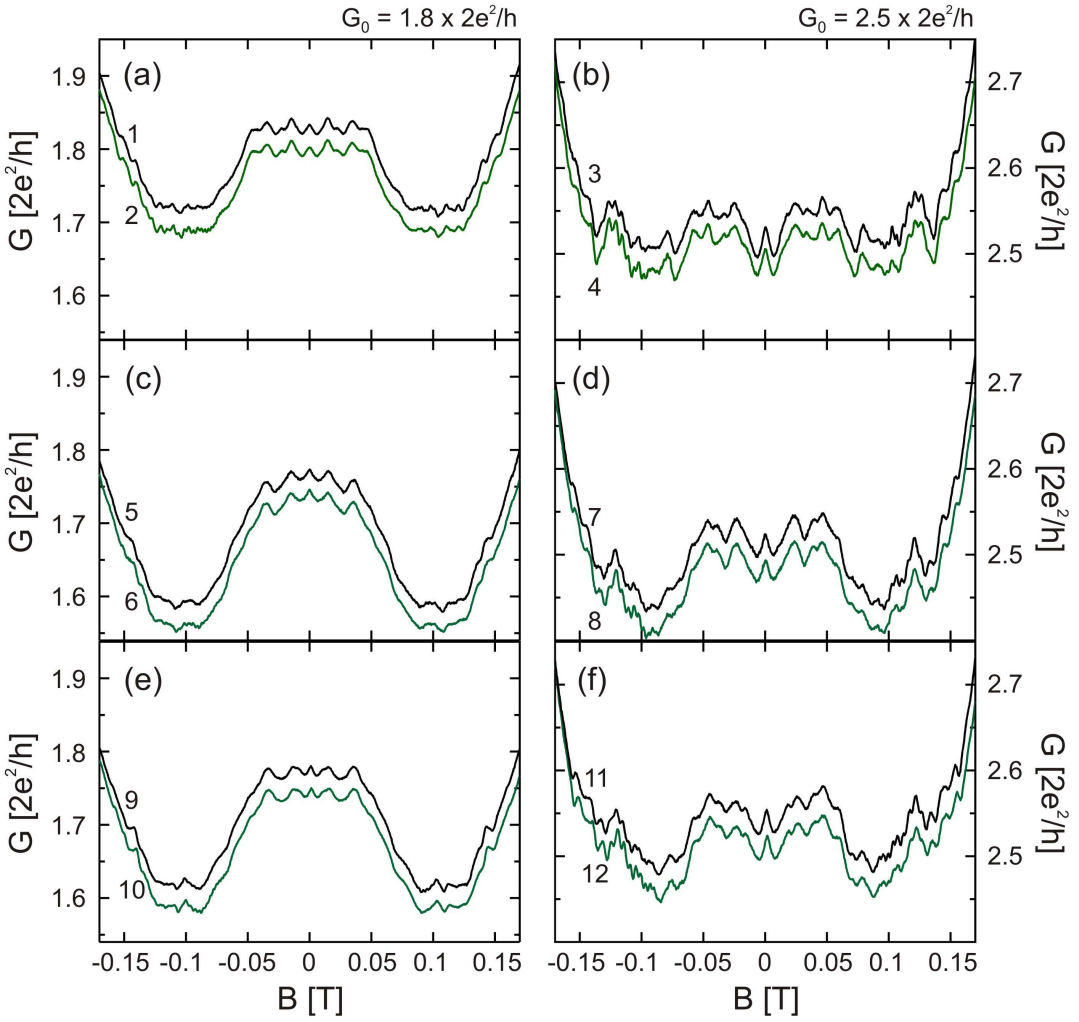

FIGURE 3.12: $G(B,t)$ at $t = 0$ hours (black traces) and 1 hour (green traces) for V_G such that G_0 was set to (a/c/e) 1.8 G_Q and (b/d/f) 2.5 G_Q. After collecting the green trace in each panel, V_G was cycled to the higher or lower setting in the next panel following the order of the numbers 1 - 12. Cycling V_G produced more marked changes in $G(B)$ between panels compared to the temporal evolution observed within panels.

to the number of impurity sites where the charges may be located.

Data from this V_G cycling experiment are shown in Fig. 3.12. It proceeded as follows:

i. V_G was set to give $G_0 = 1.8\ G_Q$.

ii. Two $G(B)$ traces were obtained, one hour apart. This was to check for the degree of temporal evolution during the experiment.

iii. V_G was set to give $G_0 = 2.5\ G_Q$.

iv. Two $G(B)$ traces were obtained, one hour apart, at this more negative V_G.

These steps were repeated three times to produce the data in Fig. 3.12. The numbers $1 - 12$ indicate the order that the traces were collected. The traces in the left-hand (right-hand) column were obtained at Step ii (iv) of each iteration. Therefore comparing $G(B)$ differences in the left-hand (right-hand) column allowed us to evaluate the effect of cycling to more (less) negative V_G.

Looking first at the temporal evolution, the black and green traces within each panel were very similar to each other. This shows that MCF did not markedly evolve within each one hour period at Steps ii and iv, similar to the low V_G data in Fig. 3.10. By comparison, strong differences emerged when comparing traces between different panels in the same column. That is, the MCF were appreciably altered between the black traces (a) and (c) and (e) in the left-hand column, and between the black traces in (b) and (d) and (f) in the right-hand column. This suggests that charges were unlikely to return to the same configuration once V_G has caused a perturbation of the charge impurity distribution. This is consistent with there being a high density of trap sites in the p-AlGaAs layer compared to the hole density. Figure 3.12 also suggests that disturbing the charge configuration by V_G cycling caused a greater de-correlation than the background temporal evolution. The latter is not surprising as V_G cycling is likely to represent a stronger perturbation than a constant V_G.

3.2.5 Thermal cycling and Si-acceptor activation energy

The data presented so far shows that the charge configuration in the AlGaAs layer does not spontaneously re-organise at $T = 40$ mK, but it can be driven out of equilibrium by the application of an external electric field. This suggests a metastable state at $T = 40$ mK, with $k_B T \lesssim E_A$. By increasing $k_B T > E_A$, it is possible to induce spontaneous reorganisation of charge trap occupation in

the dopant layer and determine the activation energy for dopant impurities. The following method was used by Scannell *et al.*[91]

1. Measure initial $G_1(B)$ at base temperature T_B
2. Raise device T to some intermediate temperature T_i and hold there for 30 mins before returning to T_B
3. Measure a second $G_2(B)$ trace and compare $G_1(B)$ and $G_2(B)$ using the autocorrelation function F (Equation 3.4)[91,92]

Scannell *et al.*[91] found significant decorrelation, $F \leqslant 0.5$, for $T_i \geqslant 165$ K in n-type AlGaAs/GaAs billiards, corresponding to the activation energy of DX centres in n-type AlGaAs.[93] The accuracy of this technique was facilitated by the particular Heliox ^{3}He cryostat used in Ref. 91, which featured continuous temperature variation between base temperature $T_B = 240$ mK and room temperature. The suppression of MCF in GaAs hole billiards above $T = 100$ mK[275] necessitated using the dilution refrigerator, which has a reduced range of controllable intermediate temperatures $T_i = 40-900$ mK and 4.2 K. Fortunately, we expected the activation temperture to be less than 4.2 K from the temperature-dependent gate characteristics in Fig. 3.7. This meant the thermal cycling experiment could be done, although it was slightly more difficult in practice. Temperatures $T_i \leqslant 900$ mK were obtainable by carefully heating the mixing chamber, with a constant $V_G = 0$. However, obtaining $T_i = 4.2$ K required completely extracting the ^{3}He/^{4}He mixture to bring the sample into equilibrium with the ^{4}He bath, and then re-condensing the mixture to obtain $T_B = 40$ mK. The significant change in device properties due to this thermal cycle necessitated taking measurements at $V_G = -156$ mV and -270 mV before and after cycling.

Figure 3.13 shows $G(B)$ before and after thermal cycling to $T_i = 300$ mK, 500 mK, 700 mK, 900 mK and 4.2 K. The before and after cycling traces at $T_i = 300$ mK exhibit no clear differences. Small changes between traces emerged at higher T_i; some examples are indicated by the arrows. Nevertheless, the two before and after traces were still largely the same up to $T_i = 900$ mK. Conversely, thermal cycling to

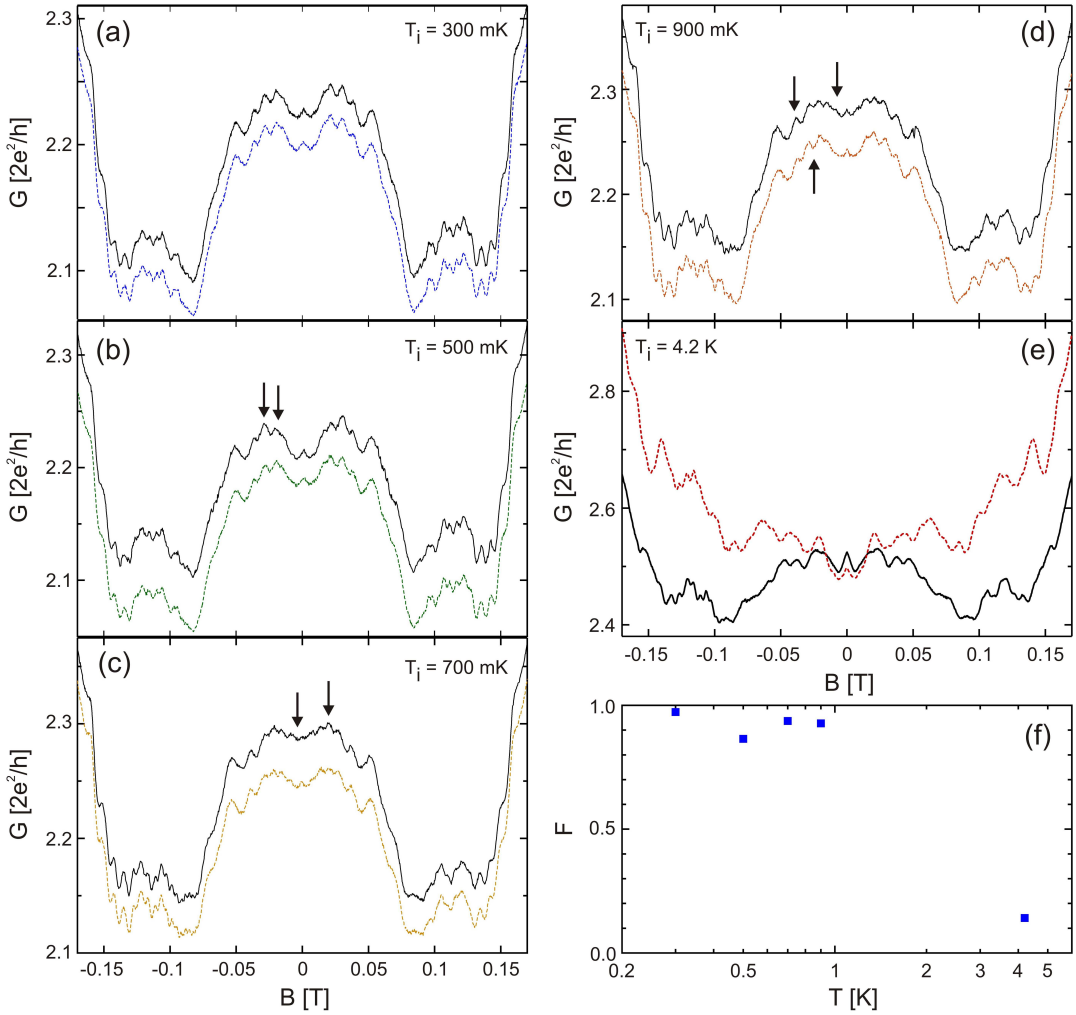

FIGURE 3.13: (a-e) $G(B)$ at $T = 40$ mK before (black traces) and after (coloured traces) thermal cycling to intermediate temperatures T_i of (a) 300 mK, (b) 500 mK, (c) 700 mK, (d) 900 mK and (e) 4.2 K. T_i was held for 30 mins in (a-d), and data was collected with $V_G = 0$. Obtaining the data in (e) was more involved, as per the main text. Changes in MCF between traces for $T_i \leqslant 900$ mK are highlighted by the arrows. The $G(B)$ traces obtained before and after $T_i = 4.2$ K have low correlation. (f) Autocorrelation function F vs T_i for the data in Figs (a-e). De-correlation occurred in the range $T_i = 0.9 - 4.2$ K.

$T_i = 4.2$ K produced almost complete de-correlation of the before and after $G(B)$ traces. This interpretation was borne out by the autocorrelation function F values in Fig. 3.13(f). Cycling to $T_i \leqslant 900$ mK caused only small spontaneous changes in charge configuration, and the corresponding autocorrelation values were high, $F = 0.9 - 1$. The $T_i = 4.2$ K thermal cycle gave an autocorrelation value $F = 0.14$. This indicates that significant de-correlation occurs in the T_i range $0.9 - 4.2$ K. Activation of DX centres in n-type billiards with trap depth ~ 250 meV[93] caused

$F \leqslant 0.5$ for $T_i \geqslant 165$ K. From Fig. 3.13(f), F fell below 0.5 in the range $T_i = 0.9 - 4.2$ K. The activation energy for Si-acceptors in AlGaAs is $40 - 180 \times$ smaller than for DX centres. This gives an acceptor depth of $E_A = 1.4 - 6.25$ meV. Given the extra time and gate sweeps involved in obtaining the 4.2 K data, it is likely that this F value was artificially reduced. In this case we expect E_A to be towards higher end of this range, $E_A = 3 - 6$ meV.

There is little literature available on p-AlGaAs with which to compare this result. One work places Si-acceptor depth in AlGaAs around 60 meV,[113] which is consistent with the known Si-acceptor depth in GaAs of $E_A = 34.8$ meV,[278] This is an order of magnitude larger than the E_A measured here. The shallow traps causing the behaviour in Fig. 3.13 may therefore not be the hydrogenic Si-acceptor. One alternative may be the Si-X defect[279] which is present in p-GaAs at very high doping densities $N_A \sim 10^{16}$ cm^{-3} and is expected to have low activation energy compared to the hydrogenic Si-acceptor.[280] However, little is known about p-$Al_{0.33}Ga_{0.67}As$ and so conclusively assigning the source of the shallow level will require further work. Note that the bandstructure precludes the measured activation energy having arisen from the shallow hydrogenic Si-donor, despite a coincidentally similar small trap depth $E_D \sim 6 - 20$ meV.[281] Looking at the p-type modulation doped bandstructure in Fig. 1.10(d) (Sec 1.4.1), donor levels will be positioned just below the conduction band. This places them well above the Fermi level and means they are not populated with electrons. If electrons did somehow populate and hop between hydrogenic donor sites, they would follow the band bending and lose energy by leaving the AlGaAs layer on either side. There the electrons would re-combine with holes in the 2DHG or pass into the gate. Thus the Si-donor cannot explain the observed data.

3.3 Discussion

In this Chapter I presented results from two investigations into the causes of gate hysteresis and instability in p-AlGaAs/GaAs heterostructures. We explored the

use of $(NH_4)_2S_x$ surface treatments on (311)A GaAs,[32] and postulated that the ineffective surface state passivation arose from the the need to satisfy both single- and double-dangling bonds. The variable results likely arose from the low stability of As-S bonds. We then used MCF in a hole billiard to detect changes in charge distribution amongst acceptor impurities in the AlGaAs layer.[33] These changes could be induced by using an external electric field to drive charge migration, or thermal cycling to cause spontaneous reorganisation. Thermal cycling was also used to estimate the activation energy of Si-acceptor traps $E_A \sim 3-6$ meV from the corresponding $T_i = 2-4.2$ K data. These experiments illustrate the potential for MCF as a diagnostic tool to sense background potential fluctuations towards optimisation of doping and impurity incorporation.[33,282] Looking at these results in the context of (311)A *p*-AlGaAs/GaAs heterostructure-based quantum device development, they provide further evidence for the role of both surface states and dopants in gate instability at low T. The changes in I_d vs V_G induced by the $(NH_4)_2S_x$ solution – particularly in I_d plateau length and V_{po} – provide strong evidence for the role of surface states. Similarly, the small-angle scattering from impurities observed using MCF in a billiard highlights the impact of charge migration between acceptor sites.

The data in Fig. 3.13 showed that the activation temperature for Si-acceptors was $2-4.2$ K. In Ref. 24 we suggested that surface states froze out around $1-2$ K based on the reduced prominence of the I_d plateau in HHMTs (see Fig. 1.19 in Sec. 1.4.5 or Fig. 6 in Ref. 24). A second explanation for the temperature dependent behaviour of HHMTs is that charge migration in the dopant layer froze out at 2 K. This would have facilitated enhanced low V_G depletion and potentially allowed pinch-off to occur before the onset of the I_d plateau, i.e., before the surface Fermi level reached the highest density of surface states. This may have resulted in an apparent reduction in I_d plateau with reduced T in Fig. 1.19, rather than an actual reduction in surface state electrical activity. Obtaining further information and teasing apart the potentially coincidental energetics would likely require additional wafer growth and experiments capable of probing only surface states. Of particular interest would be mapping out the (311)A surface

state density spectrum using, e.g., deep level transient spectroscopy (DLTS)[43] or C-V measurements.[39,41] Also of interest would be corroboration of the estimated activation energy for charge traps in p-$Al_{0.33}Ga_{0.66}As$ *via*, e.g., low T PL or DLTS.

From a practical perspective, obtaining stable, noise-free hole quantum devices will require addressing both the contributions from the surface and the dopant layer. Indeed, the most stable control of hole quantum systems has come from wafers where both dopants and surface states are negated. This is accomplished by inducing the 2DHG using a degenerately doped cap as a gate.[103,283–287] The cap can be selectively etched to generate sets of independent gates that induce and/or confine the 2DHG. The stability arises as these 'induced' devices abandon both modulation doping and the need for a metal/semiconductor interface. Here, the surface states are above the gate, not between the gate and the 2DHG. This means slow charge trapping in response to V_G either does not occur or cannot influence the 2DHG as it is effectively screened by the gate. The difficulty for induced devices is that the gate must overlap the ohmic contacts in order to ensure the 2DHG connects to the ohmics. The application of a large voltage between the closely separated gates and ohmics limits the measurement range and device yield. Gate feature size is also limited as surface Fermi level pinning generates depletion regions at the feature edges that reduces conductivity.[25] Relatively stable low-dimensional hole systems have also been induced using metal gates on (100)-oriented heterostructures without doping.[98,273,274] This suggests that doping is therefore the biggest road-block for (100)-oriented modulation doped p-heterostructures.[108] The best solution may be to find a suitably stable p-type doping scheme for (100)-oriented growth. The stability of n-type devices is likely to be due to the deep DX centres trapping any free electrons in the AlGaAs layer at $T \leq 165$ K. As previously suggested in Ref. 24, this encourages the intentional introduction of deep traps that could mirror the role of DX centres.

Chapter 4

Results: Advanced gating methods for nanowire transistors

4.1 Gating nanowires using multiple metal/oxide wrap-gates

The pursuit of greater electrostatic control over electron transport in nanostructures has pointed to using transistors where the gate wraps concentrically around the channel. Moving from traditional planar structures towards structures where the gate is folded or wrapped around the channel is a major motivation in transistor development for high speed logic applications,[3,4,12,288,289] and offers improved control over quantum systems.[290] The morphology of self-assembled semiconductor nanowires makes them excellent candidates to develop wrap-gate technology.[3] Additionally, the cost- and materials-effective synthesis of III-V nanowires compared to planar growth has driven considerable interest in the development of III-V wrap-gated nanowires towards efficient deployment in transistor systems.[3,4,12,135] Strong electrostatic control has also facilitated concepts such as 'external doping', where a base-line charge carrier density is set by a gate voltage rather than doping. This has been used to, for example, fabricate a tunable $p-n$ junction in an InP

nanowire,[20] and lock-in charge configurations for quantum measurements at low T.[30] The latter is the subject of Chapter 5 in this thesis. Aside from the new functionality of improved tunability, excluding dopant atoms holds the potential for a range of nanoscale devices. This may consist of, e.g., reducing large-angle scattering to improve mobility, similar to modulation doped[71,72] or electrostatically induced[16,17,283,284] structures. At an even smaller scale, random placement of dopants can cause a large variability in behaviour for device sizes $\lesssim 50$ nm.[13,14,36] Using devices where transport is induced solely by strong electric fields supplied by effective gating could address some of these issues.

Returning to nanowires specifically, development will need to go beyond simply the performance advantages brought by III-V materials for nanowire technologies to provide a truly viable alternative to planar Si technology.[12] Scalability is a major factor due to the desire to fit an increasing number of transistors in the same chip area. Nanowires also offer potential advantages here in the form of 3D architectures, where multiple layers of transistors facilitate a greater number of transistors in the same substrate surface area.[3,291] One simple way of achieving this is multiple wrap-gates on vertical structures; this opens the potential for two, three, four etc transistors in the substrate area previously occupied by a single transistor. Additionally, multiple gates on the same transistor opens routes towards simpler logic functionality. For example, the AND operation can be realised with a single two-gate device,[292] rather than the four separate transistors required in CMOS. Devices with more than two gates are also interesting for novel logic processes.[293] While fabrication of a vertical Si nanowire transistor with two wrap-gates has been demonstrated[292] there is a significant time cost in the fabrication, as each individual wrap-gate must be defined consecutively. This entails repeating a large number of processing steps for each gate with a significant time and yield cost.

An alternative 3D architecture would be multiple layers of *lateral* nanowire transistors, each with multiple wrap-gates.[29] The lateral orientation is also favourable for fundamental studies of both basic materials properties and quantum phenomena, as outlined in Sec. 1.5.3. One example of the latter would be using a device with three wrap-gates to define and probe highly tunable quantum dot systems

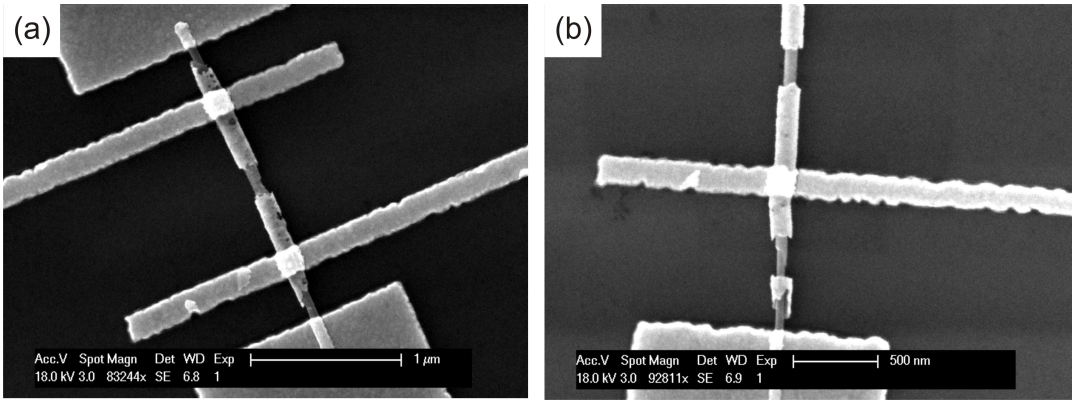

FIGURE 4.1: Scanning electron micrographs of double wrap-gated NWFETs fabricated by first depositing the source, drain and gate contacts. This process resulted in (a) gradual bends (b) sharp kinks in the nanowires. Images courtesy of Adam Micolich.

in nanowires. Here, the two outer gates would be used to define tunnel barriers surrounding a central plunger gate. The first step in any of these programmes naturally is a realisation of a single lateral nanowire transistor with multiple wrap-gates. I contributed to the development of a fabrication method for such devices during my research.[29] We developed a method where the same number of fabrication steps were used for devices with a number of gates $N \geqslant 2$.[29] The fact that the number of processing steps does not increase with the number of gates provides a significant scaling advantage over the vertical orientation.

4.1.1 Fabrication process

The main challenge in realising multiple-gate nanowire transistors was in making the initial step from a single gate to two gates. As explained in Sec. 2.3.2, an important aspect of fabrication for single wrap-gated NWFETs developed by Storm *et al.*[145] is that a single resist layer was used for the entire process. However, a single-resist approach to fabricating multiple wrap-gates would necessarily result in ohmic contacts between each gate. This would severely limit a number of applications. As such, we focussed on the development of a more general method that used two separate resist layers. The devices were based on 70 nm diameter InAs nanowires pre-coated with a 12 nm insulating Al_2O_3 layer, a 16.5 nm W layer

and 11.5 nm Au layer that acted as the wrap-gate, and an outer 12 nm Al_2O_3 layer to facilitate nanowire transfer as described in Sec. 2.3.

The first fabrication method we investigated was to use the first resist to define the source, drain and gate contacts. The process was similar to that presented for single wrap-gates in Sec. 2.3.2. A second resist was then used to define the multiple gate segments. The process was:

1. Define the source/drain contact regions in the first resist *via* EBL.
2. Etch away the outer oxide, Au and W in the source/drain region.
3. Expose the regions for multiple gate contacts in the same resist layer *via* EBL.
4. Etch the outer oxide in the gate contact region and inner oxide in source/drain region.
5. Deposit source, drain and gate contacts. So far this process is identical to single wrap-gates, but with multiple gate contacts to what is at this point still a single wrap-gate.
6. Lift-off resist and spin second resist.
7. Define etch regions to separate gate segments *via* EBL.
8. Etch away outer oxide, Au and W layers.
9. Lift-off second resist for completed device.

Depositing the contacts using the first resist ensured that the nanowire remained fixed in the same position during lift-off at Step 6, and during subsequent gate definition. Using this method we realised NWFETs with multiple wrap-gates, as shown in Fig. 4.1. However, performing subsequent fabrication with contact metal deposited appeared detrimental to nanowire quality. The nanowires in Figs. 4.1(a) and (b) sustained a gradual bend and sharper kinks, respectively. This may have arisen from the forces applied during metal lift-off or resist spinning if unrestrained

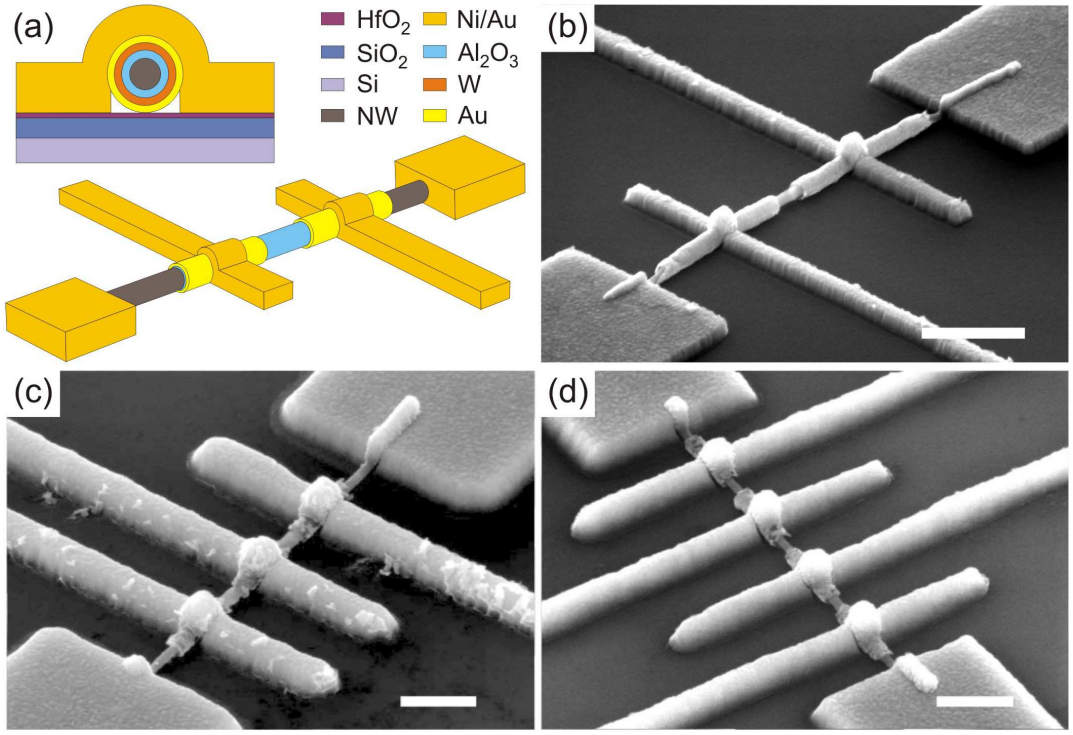

FIGURE 4.2: (a) Schematic and (inset) cross-section of wrap-gated NWFET with two independent segments. The cross-section shows the inner Al_2O_3, W and Au wrap-gate layers along with the Ni/Au gate contact. The underlying substrate consisted of highly doped Si that was used as a back-gate, insulated from the NWFET by 100/10 nm layers of SiO_2/HfO_2. (b/c/d) Scanning electron micrographs of double, triple and four wrap-gated NWFETs. Fabrication of each device entailed the same number of processing steps. SEM images courtesy of Adam Burke.

sections of the nanowire moved when the restrained sections underneath the contacts could not.

In the interests of minimising nanowire damage, we moved to an alternative method. This second process had the additional advantage of less processing steps; it only required two EBL sessions, rather than the three used in the previous method. The process was:

1. Etch away outer Al_2O_3 layer on all nanowires immediately after transfer, before spinning the first resist.

2. Use the first resist to define source/drain contacts as well as etch regions to separate wrap-gate segments *via* EBL.

3. Etch Au and W layers.
4. Lift-off first resist and spin second resist.
5. Define source, drain and gate contacts *via* EBL.
6. Deposit contact metal.
7. Lift-off second resist for completed device.

Examples of NWFETs with 2, 3 and 4 wrap-gates in series produced using this method are shown in Fig. 4.2. The success of the fabrication relied on the unrestrained nanowires maintaining their position through lift-off and secondary resist spinning in Step 4, as no contacts were deposited using the first resist. Fortunately this held for $\sim 90\%$ of nanowires, enough to facilitate the proof-of-principle experiments we conducted. The scalability power of this method is that the total number of fabrication steps did not depend on the number of wrap gates. Defining and contacting additional wrap-gates only required changing the EBL patterns in Steps 2 and 5.

As in fabrication for single wrap-gated devices, Au, W and Al_2O_3 removal was accomplished using KI/I_2, H_2O_2 and HF etches, respectively (see detail in Sec. 2.3.2). The outer Al_2O_3 layer was removed prior to resist spinning at Step 1 rather than immediately prior to gate metal etches at Step 3 since it was only required to facilitate nanowire transfer. We found that etching the Al_2O_3 at Step 3 resulted in less accurate gate definition. The source/drain contacts were passivated by immersion in the weak $(NH_4)_2S_x$ solution at 40°C for 2 minutes.[240] The contacts consisted of 45/205 nm of Ni/Au deposited in the Lesker thermal evaporator. The thick contacts were required to obtain continuous metal coverage over the wrap-gated segments of the nanowire, which were ~ 170 nm in diameter. The total 420 nm thickness of the contacts plus the nanowire was greater than a single PMMA layer, ~ 300 nm. Thus, we used a double-layer of PMMA for the second resist spun at Step 4. This was accomplished by consecutively spinning and baking two layers of PMMA A5, for a total thickness of ~ 600 nm. EBL was performed using the Raith 150-Two EBL system with a 20 kV accelerating voltage and 20 μm aperture.

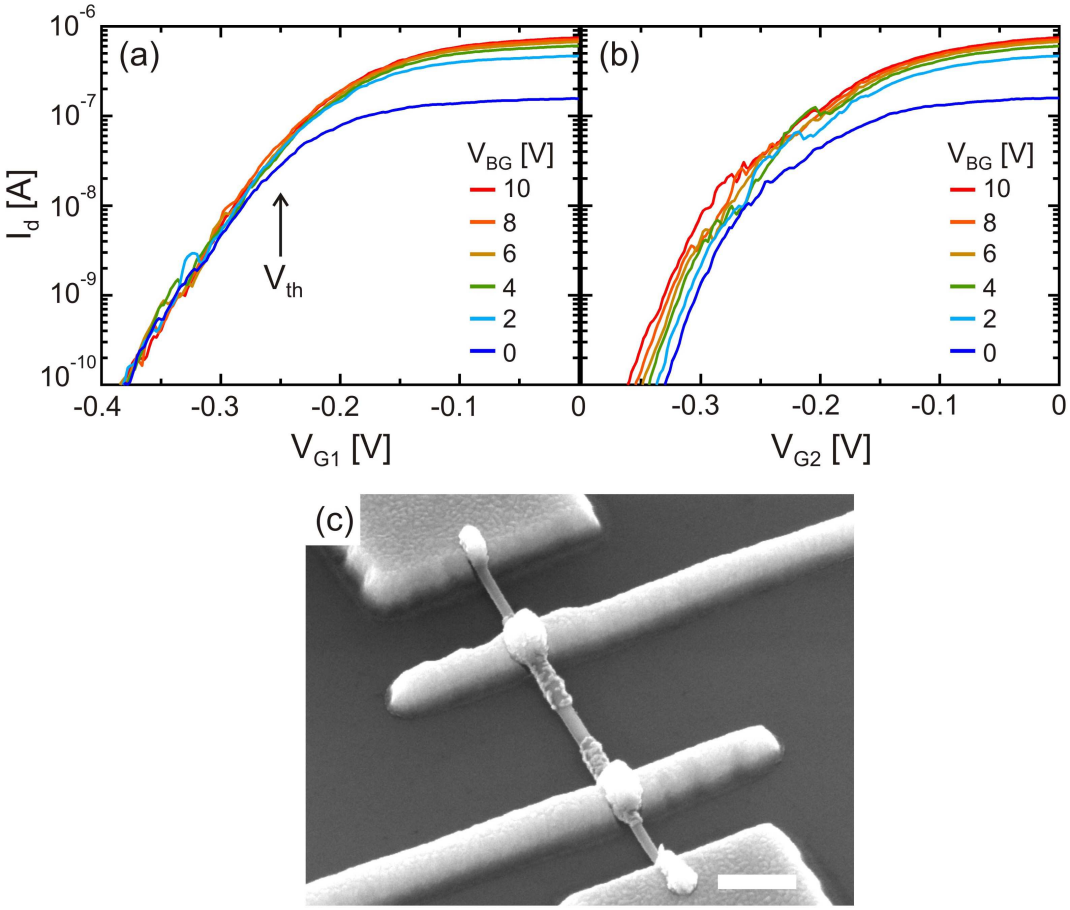

FIGURE 4.3: (a/b) Electrical characteristics and (c) scanning electron micrograph of a double wrap-gated NWFET. (a) I_d vs V_{G1} at varying V_{BG}. The electrical properties of G1 were independent of V_{BG} below threshold voltage $V_{th} \sim -0.25$ V due to the wrap-gate providing effective screening of the nanowire from the back-gate potential. This suggests that the W layer of this gate was intact. (b) I_d vsV_{G2} at varying V_{BG}. The V_{BG} dependence of I_d vs V_{G2} indicates insufficient screening, likely due to holes in the W layer. SEM image courtesy of Adam Burke.

4.1.2 Electrical characterisation of the two-gate device

We evaluated the electrical performance of the gates by focussing on the transfer characteristics in the subthreshold region, where the gate exercises the strongest control over the channel. Ideally, I_d vs V_G in the subthreshold region depends only on temperature and the materials properties of the gate insulator and semiconductor.[1,2] A SR830 lock-in amplifier supplied an ac excitation $V_{sd} = 30$ μV at 73 Hz to the source and measured the resulting I_d at the drain. A Keithley K2400 SMU was used to check that each gate did not exhibit significant leakage currents

within the operating range. For measurements, gate voltage V_{GN} was applied to gate number $N = 1, 2, 3, 4$ by the voltage supplies included in the SR830, with RCR filters used on each output to reduce high frequency noise. V_{GN} was incremented at 4 mV/s. A back gate voltage V_{BG} was supplied to the n^+-Si substrate using a Keithley K2400 SMU. Measurements were performed in liquid nitrogen at $T = 77$ K using the cryogenic dewar and dipstick outlined in Sec. 2.4.2. This was to freeze-out charge traps at the NW/Al_2O_3 interface and thereby reduce drift and hysteresis that arises at room temperature.[22,23,28]

The I_d vs V_{G1}/V_{G2} transfer characteristics are shown in Fig. 4.3(a/b) for G1 and G2 of the device in Fig. 4.3(c) at varying V_{BG}. In this measurement, G2 was grounded while G1 was swept, and vice versa. Both gates turn off the NWFET within a 0.4 V range, with subthreshold swings of $SS = 40$ and 30 mV/dec and threshold voltages $V_{th} = -0.247$ and -0.236 V, for G1 and G2 respectively. Scaling the subthreshold swing to room temperature gives expected values of $SS(T = 300\text{ K}) = 117$ and 168 mV/dec. Typically, room temperature subthreshold swings of $100 - 750$ mV/dec are observed for InAs wrap-gated NWFETs with a Al_2O_3 dielectric.[22,23,139,140,145,294,295] This places the device in Fig. 4.13 amongst the better performing NWFETs. The comparatively good performance of this device may be partially due to the fact that charge trapping in surface states will have degraded the subthreshold properties of NWFETs measured at room temperature in these previous works.[1,2,12,48]

Looking closely at the SEM in Fig. 4.3(c) reveals various imperfections in the gates. In particular, there are large patches of unintentionally removed material. This was most likely due to small quantities of etchant attacking the Au layer by wicking between the resist and device. The uneven nature of the patches can be explained by the large grain size of sputtered Au films resulting in large voids between grains.[145] Such imperfections are normal in nanofabrication as a result of small changes in materials and reagents between fabrication batches. In particular, recall the much more continuous gates fabricated using a nominally identical process shown in Fig. 4.2. For device applications, the most important aspect is the extent to which these imperfections affect the electrical performance.

The major concern with devices like that in Fig. 4.3 is that the integrity and electrical quality of the gates was compromised. Practically, material removal was only likely to affect device performance if the W layer was also compromised; an intact W layer would provide a strong radial confinement potential irrespective of the properties of the Au layer. Since this was not easily determined from SEM images, we used a simple electrical method of testing the extent of W removal, which I explain now.

The technique we used relies on the capacity of the wrap-gate to screen external electric fields. Significant W removal would noticeably decrease screening capabilities as external electric fields penetrate directly to the nanowire through holes in the metal. To test the screening, we used V_{BG} to apply an external electric field in parallel to the wrap-gate and observe how this affected the subthreshold region when sweeping V_{GN}. In an ideal device, current in the subthreshold region depends only on the potential barrier generated by the gate voltage (see Sec. 1.2).[1,2,145] This ideal behaviour was seen for G1, where I_d vs V_{G1} fell on the same path below V_{th}, i.e. $V_{G1} < -0.25$ V (Fig. 4.3(a)). A back-gate dependence of I_d vs V_{G1} emerged above V_{th} due to positive V_{BG} inducing a higher carrier concentration in the regions of the nanowire not covered by the wrap-gate. This was noted by Storm *et al.*[145] for single wrap-gate NWFETs also. By contrast, I_d vs V_{G2} shows that G2 performance was influenced by V_{BG} even in the subthreshold region. This suggests that G2 did not effectively screen the nanowire channel from the back-gate potential due to holes in the wrap-gate extending into the W layer.

This simple electrical technique allowed us to determine the suitability of a particular device for applications without recourse to more time consuming imaging methods. Additionally, many of the most probing imaging methods, e.g., transmission electron microscopy, are destructive and cannot be used on devices intended for electrical measurement. This means information is only gained about devices that can never be used anyway. It is also worth noting that G1 of the device in Fig. 4.3 exhibited ideal behaviour despite the poor appearance compared to, e.g., the devices in Fig. 4.2 and in Storm *et al.*[19] This illustrates that effectively

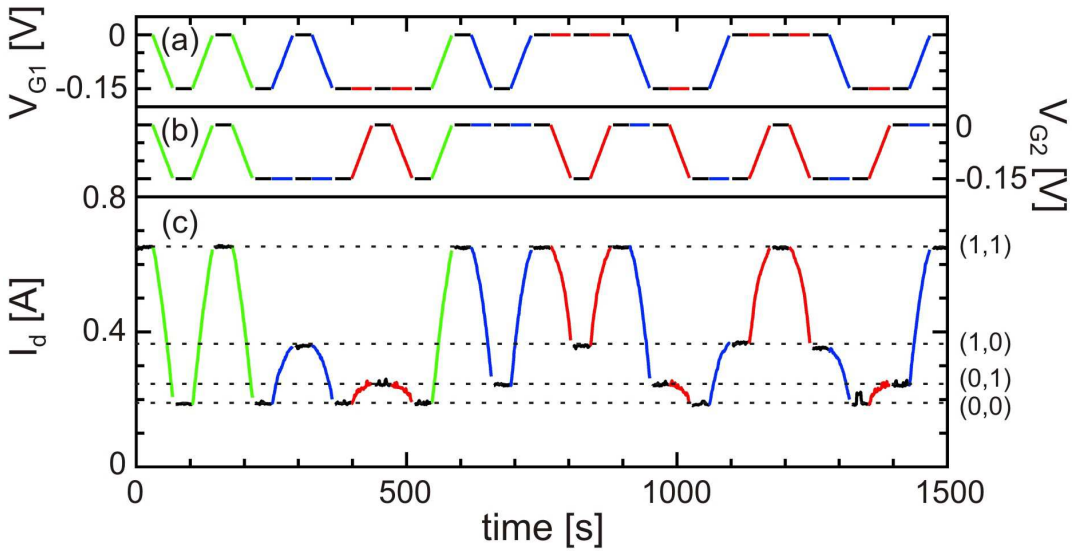

FIGURE 4.4: (a) V_{G1} and (b) V_{G2} vs time as they were swept between 0 V (logical 1) and −0.15 V (logical 0). Green traces represent where G1 and G2 were swept together, blue traces where G1 was swept with G2 fixed, and red traces where G2 was swept with G1 fixed. The black traces are 30 s wait times to establish device stability. The program switched each two-input logic state between every other logic state. (c) I_d output in response to the program in (a/b). I_d took four distinct values corresponding to each input logic state.

utilising devices rests on ascertaining the actual device performance rather than relying on appearance alone.

We then evaluated the independence and electrical balance between gates. Fabricating gates that reproducibly apply the same potential is important for logic applications or the generation of quantum systems. We investigated this by treating the NWFET as a logic system, using the two gates as inputs and reading I_d as the output. The power of this was that we could set well defined V_{GN} inputs and predict the I_d outputs. Deviations in the measured I_d from the expected output states could then be traced back to imbalance at the inputs. For instance, take the simplest case of a single gate FET switching between two pre-defined V_G values. The high V_G is notated as logical 1 and the lower V_G as logical 0. Switching between these two values should consistently generate only two I_d values: a high I_d for logical input 1, and a low I_d for logical input 0. Stepping this up to two independent gates generates four logical input states: (1,1), (1,0), (0,1) and (0,0). The expected I_d output behaviour is four constant values that correspond to the

four input states in the following way: Applying (1,1) at the input will generate the highest I_d output; applying (0,0) and the input generates a low I_d output; applying inputs (1,0) and (0,1) generates an I_d output somewhere in between the highest and lowest I_d. A stable device should return to these four I_d output values no matter the order of operation.

To test this on the device pictured in Fig. 4.3(c) we formulated a program that swept the gates separately or together between $V_{GN} = 0$ V (logical 1) and $V_{GN} = -0.15$ V (logical 0) such that each of the four logical states switched to each of the other logical states at least once. Figures 4.4(a/b) follows the action of V_{G1} and V_{G2} inputs over time as the program ran. The green traces correspond to when the gates were swept together and the blue (red) traces show when G1 (G2) was swept with G2 (G1) constant. A 30 s wait time at constant V_{GN} was used between sweeps to examine device stability. The output I_d took four distinct values corresponding to the four input states during each 30 s wait time (Fig. 4.4(c)). These four I_d values did not depend on the order of operations, indicating excellent device stability and gate independence.

In terms of electrical balance, G1 in this device had a stronger coupling to the nanowire channel than G2. This is apparent by comparing the blue and red traces (G1/G2 only sweeps, respectively) in the range $t = 200 - 500$ s. Going from (0,0) to (1,0) by sweeping V_{G1} generated a greater change at the output than sweeping V_{G2} to go from (0,0) to (0,1). Related behaviour was observed in the range $t = 600 - 900$ s, where the transition from (1,1) to (0,1) using V_{G1} entailed a larger I_d change than that generated by the (1,1) to (1,0) transition using V_{G2}. Some imbalance was observed in the basic transfer characteristics in Fig. 4.3, however the logical operations here make this imbalance much clearer. An imbalance in this device is not unexpected given the noticeable damage to G2 visible in Fig. 4.3(c).

The interest in two-gate devices for logic applications is the embodiment of logical AND.[292] This functionality occurs when the input logical 0 is set to a $V_{GN} < V_{th}$. In the subthreshold region, V_{GN} generates a potential barrier that blocks

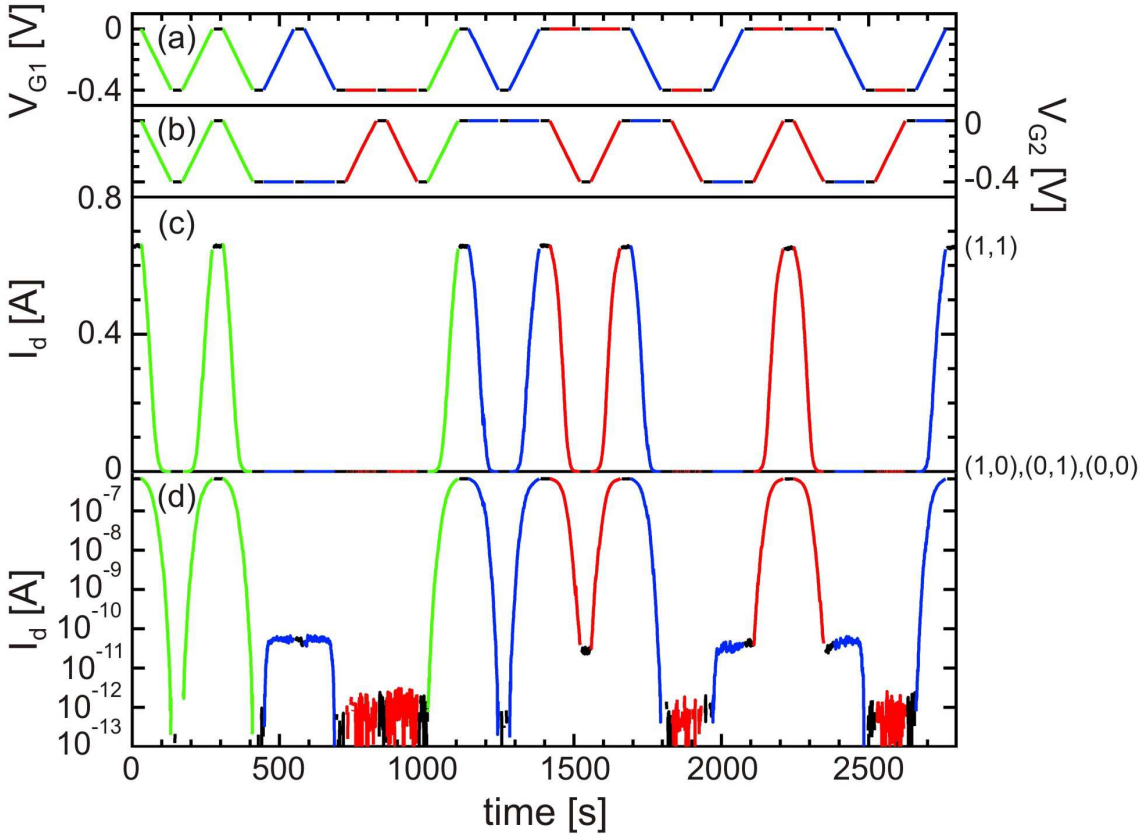

FIGURE 4.5: (a) V_{G1} and (b) V_{G2} executing the same program as Fig. 4.4, but logical 0 was set to -0.4 V. (c) Sweeping V_{G1} or V_{G2} is sufficient to obtain $I_d \sim 0$, i.e., for logic inputs (1,0), (0,1) and (0,0). The device embodies the AND operation as I_d flows only when both G1 and G2 are above threshold, at input logic state (1,1). (d) I_d data in (c) plotted on a $\log_{10}$ scale reveals that gate imbalance affected device performance. Nevertheless, I_d was reduced by a factor of $10^{-4} - 10^{-7}$, which enabled AND operation.

I_d, independent of the voltage on the other gate. This means that logical inputs (1,0), (0,1) and (0,0) all cause $I_d \sim 0$ at the output. Non-zero I_d is obtained only when both gates are above threshold, i.e., the input is (1,1). Figs 4.5(a/b) show the logic program applied to the same device, but with input logical 0 set to $V_{GN} = -0.4$ V, which was below $V_{th} = -0.25$ V. The input logical 1 was again set to $V_{GN} = 0$ V. Fig. 4.5(c) shows that the I_d output was zero for all inputs aside from when $V_{G1} = V_{G2} = 0$ V. That is, logical state (1,1) on the inputs generated 1 at the output, while (1,0), (0,1), (0,0) at the inputs all generated logical 0 at the output, effectively embodying the AND operation. Table 4.1 shows the truth table for AND, and the values used to embody the operation using the double wrap-gated NWFET. The program previously used in Fig. 4.4 generated a four

level output I_d – rather than the two output AND – because the logical 0 of $V_{GN} = -0.15$ V set there was well above V_{th}.

TABLE 4.1: (left) Truth table for logical AND. (right) Device inputs/outputs from Fig. 4.5.

AND			Device input		Device output
Input 1	Input 2	Output	V_{G1} [V]	V_{G2} [V]	I_d [A]
1	1	1	0	0	6.5×10^{-7}
1	0	0	0	-0.4	$\sim 10^{-10}$
0	1	0	-0.4	0	$\sim 10^{-12}$
0	0	0	-0.4	-0.4	$\sim 10^{-13}$

To examine the effect of gate imbalance on AND realisation, I_d was plotted on a $\log_{10}$ scale in Fig. 4.5(d). Similarly to the data in Fig. 4.4, the stronger coupling of G1 caused the (1,0) state to generate a higher output than the (0,1) state. However, I_d in both states was 10^4 to 10^7 times lower than the I_d when (1,1) was applied to the input, which lead to an effective $I_d = 0$ in Fig. 4.5(c). This reinforces the point that even devices with a poor appearance often have adequate electrical performance. The advantage of the multiple gate approach to AND realisation is that it requires only a single transistor with two gates. In CMOS technology, AND requires two n-type and two p-type transistors. Note that the device could likely be operated much faster than the slower sweeps conducted here; vertical InAs wrap-gated transistors with GHz operation have been demonstrated, by undertaking optimisation of various parasitic effects.[141,142,296] The slow sweep rate was used here to accurately capture the steady state device properties.

4.1.3 Electrical characterisation of the four-gate device

As mentioned previously, the multiple wrap-gate fabrication process facilitated realisation of NWFETs with four gates using the same number of processing steps as for NWFETs with two gates. Figure 4.6 shows the transfer characteristics for each gate of the four-gate device in Fig. 4.2(d). There was a high degree of similarity in the electrical properties of each gate, with average subthreshold swing $SS = 34 \pm 9$ mV/dec and median threshold voltage $V_{th} = -0.46 \pm 0.04$ V. The

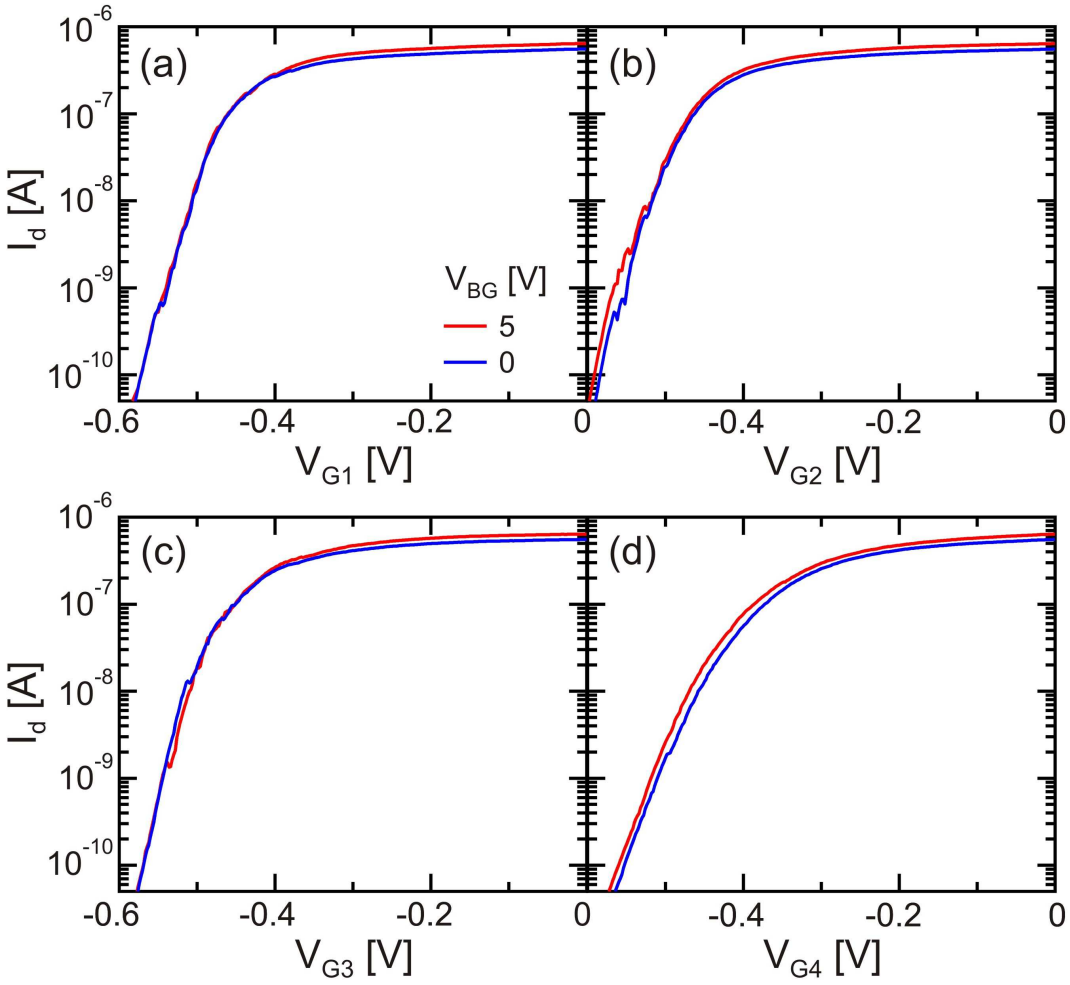

FIGURE 4.6: I_d through the four wrap-gated NWFET in response to (a) V_{G1}, (b) V_{G2}, (c) V_{G3} or (d) V_{G4} at $V_{BG} = 0$ V (blue traces) or 5 V (red traces). The comparative lack of dependence on V_{BG} and strong similarity between the characteristics of each gate are indicative of a high quality device.

V_{BG} dependence of wrap-gate sweeps was much reduced compared to the two-gate device studied in Fig. 4.3, indicating excellent screening and therefore a high degree of material integrity. The comparative lack of V_{BG} dependence above threshold is likely due to the additional gate coverage. This would increase the associated screening and reduce V_{BG} influence over electron density in the nanowire. The effective screening in this device illustrates the capacity to fabricate high quality gates with lengths $\sim$ 400 nm and separations of 200 nm using our fabrication process.

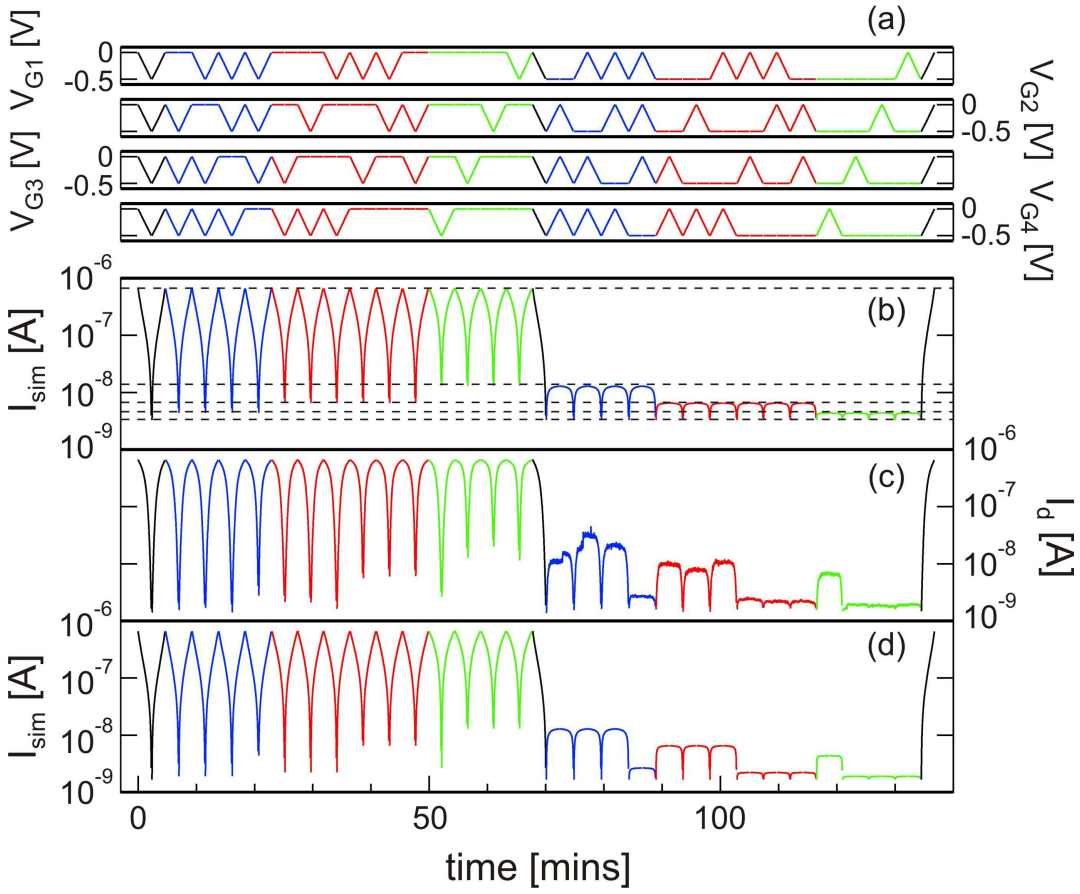

FIGURE 4.7: (a) Logic program applied to V_{GN}, $N = 1 - 4$ for the four-gate NWFET with logical input 1 set to $V_{GN} = 0$ V and logical input 0 set to $V_{GN} = -0.5$ V. The program switched from/to logic input (1,1,1,1) to/from all other input logic states outlined in Table 4.2, then from/to (0,0,0,0) to/from all other logic states. Black, blue, red and green traces correspond to one, two, three or four gates swept, respectively. All other gates were held constant. (b) Simulated current I_{sim} for an ideal device with equal gate-nanowire coupling for all gates. The 18 input logic states result in 5 ouput logic states. (c) Measured I_d for the four-gate device in Fig. 4.2(d). The device deviates from expected behaviour due to different coupling of G4. (d) I_{sim} taking into account the different G4 gate coupling (see text).

Evaluating the temporal stability and gate balance of this device was more complex than for the device with two wrap-gates. The logic programs in Figs. 4.4 and 4.5 consisted of switching each of the four logic states between every other logic state. This becomes impractical when dealing with four independent gates; four inputs generate a total of 18 possible input logic states. This means a prohibitively large number of sweeps would be needed to map out the four-gate device in the same way as the two-gate device. Instead, we focussed on the essential details to illuminate

gate imbalance. First, we considered ideal device behaviour, where the nanowire-gate coupling is identical for each gate. In this case, changing G1 from logical 0 to logical 1 would result in the same I_d output as changing G2, G3 or G4 from logical 0 to logical 1. That is, four gates with identical coupling to the nanowire should generate the same output for the input permutations (1,1,1,0), (1,1,0,1), (1,0,1,1) and (0,1,1,1). Considering the remaining logical input states reveals that 5 output states arise from the 18 possible input states in an ideal four-gate device. These are summarised in Table 4.2.

TABLE 4.2: Input and outputs for the four-gate device where the gates couple equally to the channel. Ordered from highest to lowest I_d output

Input logic states	Output logic state
$(1,1,1,1)$	5
$(1,1,1,0), (1,1,0,1), (1,0,1,1), (0,1,1,1)$	4
$(1,1,0,0), (1,0,0,1), (0,0,1,1), (0,1,1,0), (1,0,1,0), (0,1,0,1)$	3
$(1,0,0,0), (0,1,0,0), (0,0,1,0), (0,0,0,1)$	2
$(0,0,0,0)$	1

Recognising gate imbalance thus consisted of simply evaluating the degeneracy of I_d output states. Fig. 4.7(a) shows the protocol we used. We started with all gates at $V_{GN} = 0$ V, i.e., logic input state (1,1,1,1), output 5. We then swept all gates to $V_{GN} = -0.5$ V and back to establish logic state (0,0,0,0), output 1. We then systematically ran through each permutation of each of the logic output states 2, 3 and 4. This entailed sweeping a different number of gates depending on the initial and final logic states. The blue traces correspond to three gates being swept with one held constant, red traces correspond to two gates being swept with two held constant, green traces correspond to individual gates being swept with the other three held constant, and the black traces correspond to all four gates swept between (1,1,1,1) and (0,0,0,0).

Before looking at the device result, we needed to understand ideal device behaviour. We did this by simulating the current output I_{sim} of an ideal four-gate device, shown in Fig. 4.7(b). The simulation used a simple model of the nanowire resistance, $R = R_0 + \Sigma R_N(V_{GN})$, where R_0 is the nanowire resistance when all gates were set to 0 V, and $R_N(V_{GN})$ was the gate voltage-dependent resistance of

the nanowire segment beneath each gate, $N = 1 - 4$. For the data in Fig. 4.7(b), each function $R_N(V_{GN})$ was an identical linear function of V_{GN} to simulate equal gate-nanowire coupling. As expected, the I_{sim} output was driven between the five logic states outlined in Table 4.2. These output states $5 - 1$ (top to bottom) are highlighted with the dashed lines.

The measured response from the actual device is given in Fig. 4.7(c). The I_d output did not consist of five clearly defined output states. This immediately indicates the presence of gate imbalance. The major deviations from ideal behaviour arose from G4. This is most apparent in traces that involved only altering V_{G4}; these are the first set of green traces in each series. Sweeping V_{G4} alone caused a greater deviation from either the (1,1,1,1) state or (0,0,0,0) state than when any of the other gates were swept alone. A related effect was observed when three gates were swept simultaneously (blue traces). The last set in each blue series shows that when V_{G4} was *not* swept, the resulting change in current was smaller than the other three sets when V_{G4} *was* swept. This suggests that the function $R_4(V_{G4})$ differs from $R_N(V_{GN})$ for $N = 1, 2, 3$. To show this clearly, the simulation was repeated with $R_1(V_{G1}) = R_2(V_{G2}) = R_3(V_{G3}) = 0.984 \times R_4(V_{G4})$, and the resulting simulated I_{sim} plotted in Fig. 4.7(d). This simulation matched actual device performance more closely, suggesting the gate coupling for G4 deviated from the coupling for G1, G2 and G3 by a simple scaling factor 0.984. Firstly this indicates that G1, G2 and G3 were all very well matched gates, and that G4 differed only slightly. This positive result suggests that even better results could be obtained with some optimisation of the fabrication process.[23,296] The technique used here also illustrates the potential to compensate for gate imbalance. The different coupling of G4 could be accounted for by applying the evaluated scaling factor to the relevant gate voltages sourced in subsequent experiments/applications.

4.1.4 Multiple transistors on the same nanowire

The fabrication platform we developed also enabled realisation of two independent wrap-gate transistors on the same nanowire. This device is shown in Fig. 4.8(a).

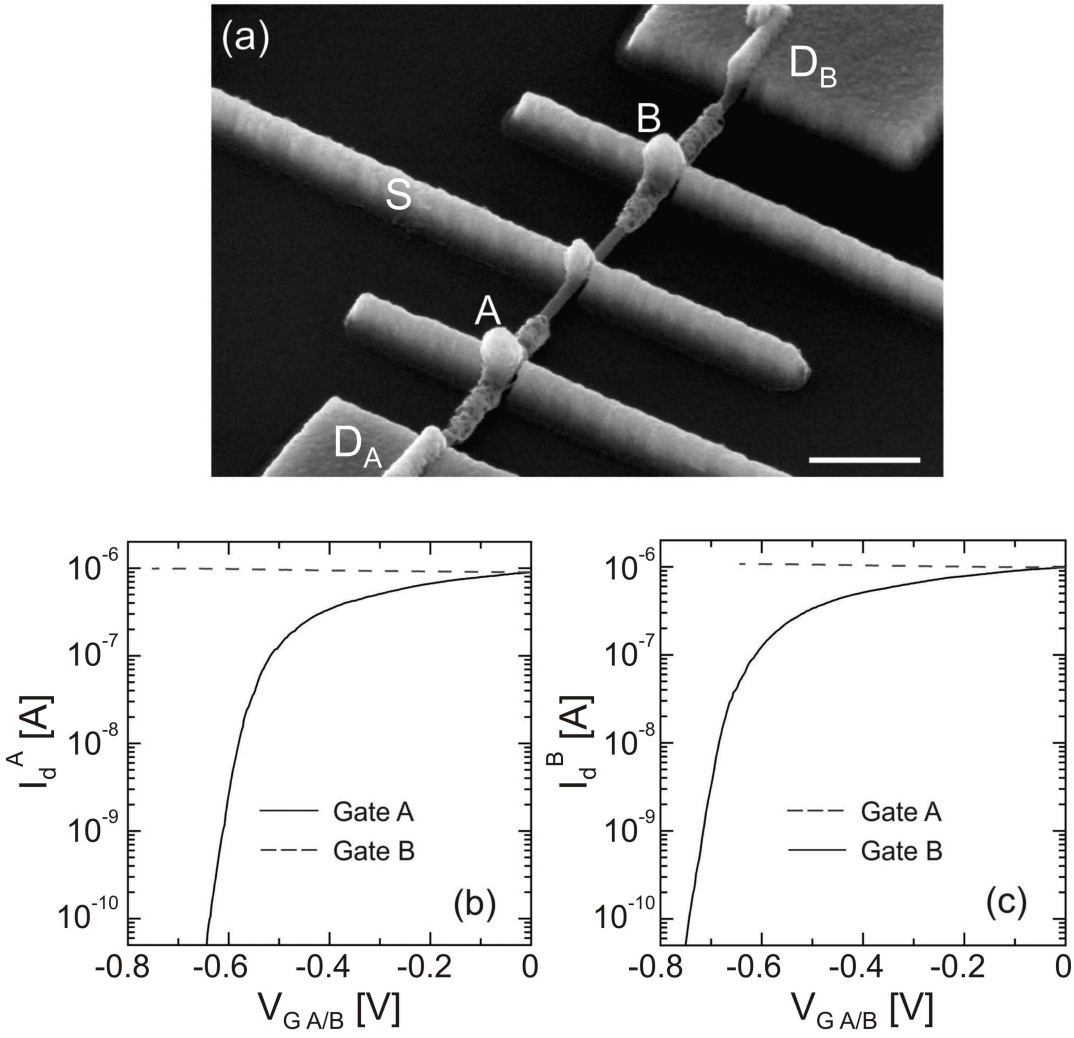

FIGURE 4.8: (a) Scanning electron micrograph of two transistors A and B on the same nanowire with common source contact S and respective drain contacts D_A and D_B. (b) I_d^A for transistor A and (c) I_d^B for transistor B measured at the drain contact of each transistor in response to applied V_{GA} or V_{GB} with $V_{BG} = 0$ V. Solid traces in each frame represents the current response from sweeping the gate of that particular transistor. Dashed traces show the current obtained when sweeping the gate of the other transistor.

Fabrication differed from previous devices only by the inclusion of a common source contact in the middle of the nanowire. This contact was defined alongside the two drain and gate contacts during the second EBL step. The electrical data in Fig. 4.8(b/c) demonstrates independent operation of the two transistors A and B with V_{sd} applied to the common source. I_d^A and I_d^B were measured at their respective drain contacts using two lock-in amplifiers coupled to the V_{sd} reference signal. This facilitated simultaneous measurement of I_d^A and I_d^B in response to

applied V_{GA} or V_{GB}. Only one gate G_A or G_B was swept while the other gate was held at 0 V.

The transfer characteristics of each transistor – solid lines in Fig. 4.8(b/c)) – were very similar to that seen in multiple wrap-gate devices above. The transistors also match each other well, with identical subthreshold swings and a difference in V_{th} of only ~ 0.15 V. The dashed lines show the I_d response in each transistor when the gate of the other transistor was swept to deplete that side of the device. In both devices, I_d rose as the other device was depleted. This was not because the gate was directly influencing the opposing channel. Rather, it is because the two transistors passed current to separate grounded drain contacts in a parallel circuit. Since there is a constant V_{sd} applied to the source, reducing I_d^A by application of V_{GA} necessarily caused more current to flow to ground through Transistor B, and vice versa.

4.1.5 Summary

Multiple wrap-gate NWFETs offer a versatile route to many novel devices and functionalities.[29] The devices can implement two-input AND logic on a single transistor as opposed to the four required by CMOS. The simple fabrication method facilitated three and four wrap-gated devices with the same number of processing steps as two wrap-gates. This contrasts with vertical wrap-gated nanowires where the number of steps scales with the number of gates.[292] Gate control and balance was already satisfactory for most applications, although work could be done in improving the oxide/nanowire interface[23,296] and the quality of sputtered Au. The latter may reduce the extent of gate material removal seen in Fig. 4.3(c). Nevertheless, even devices with poor appearance often provided suitable electrical performance. We presented a method to characterise the performance of potentially damaged gates using screening of an external potential, and a second method to evaluate the electrical balance between gates and compensate for this in future experiments. From here, the multi-gate devices could be utilised for strong electric field control in the generation and manipulation of quantum systems, as well as

novel many-input logic systems.[293] Finally, we demonstrated two transistors with a common source on the same nanowire using the same process, which could also be used to facilitate device scaling in 3D architectures.[3,291] The multiple wrap-gates could be combined with more complex heterostructure nanowire growth to produce devices with unique functionality that further enhances scalability. For example, similar structures – albeit without wrap-gates – have been fabricated to realise inverters on single nanowires.[297] The stronger confinement and versatility supplied by our multiple wrap-gate fabrication technique has the potential to enhance nanowire development in virtually any electrical application.

4.2 Gating nanowires using nanoscale patterned polymer electrolytes

As outlined in Sec. 1.6.1, polymer electrolyte (PE) dielectrics offer an interesting alternative to metal/oxide gates to generate strong electric fields.[8] The strong gating arises from the fact that the mobile ions in the polymer matrix are driven to ~ 1 nm away from the semiconductor channel.[8,203] The mobile ions offer a particular advantage to nanomaterials such as nanowires, as the ions follow the surface morphology of the semiconductor material. When used to gate nanowires, the ions are expected to wrap concentrically around the nanowire. As such, PEs provide an organic, spin cast route to wrap-gating.[28,31,196,219] Furthering the use of PEs with nanomaterials requires patterning them on the nanoscale to facilitate individual device contact and control. This would also open up the possibility of using multiple independent PE gates on the same nanowire. Patterning the PE is desirable in general as it eliminates overlap with the source and drain contact, which reduces parasitic capacitance, leakage currents and contact erosion.[8] Patterning *via* photolithography,[211] ink-jet printing[193,197] and injection into microfluidic channels[217] has enhanced the use of PE electrolytes in microelectronics. However, the resolution of these methods is insufficient to fit the PE between source/drain contacts on a nanowire, which typically have a 200 nm $-$ 3 μm separation. In this Section I

present a nanoscale patterning method using electron beam lithography for a polymer electrolyte consisting of poly(ethylene oxide) (PEO) doped with $LiClO_4$.[28,31] We applied the nanoscale PEs as gate dielectrics in InAs nanowire transistors and obtained electrical performance comparable to metal/oxide wrap-gate transistors. We also demonstrated two independent gates on a single nanowire using patterned PE dielectrics, which exhibited excellent electrical balance.

4.2.1 Electron beam patterning of PEO/$LiClO_4$

Electron beam lithography (EBL) operates by high energy electrons selectively causing the scission or cross-linking of chains in a polymeric resist layer. This alters the solubility of the patterned regions when immersed in developer solutions and causes either the patterned regions to be removed, or the surrounding resist to be removed (see Sec. 2.1.2). PEO – a common polymer backbone for many PEs – functions as a negative-tone EBL resist,[298] where the patterned area remains after development. The polymer chains in PEO are cross-linked on exposure to high energy electrons, making the exposed regions comparatively insoluble in a range of developers including methanol, tetrahydrofuran and H_2O.[298] PEO has not found extensive application as a resist outside niche biological applications,[299,300] despite the ability to pattern PEO features with dimensions below $\sim$ 200 nm.[299–302] Further, EBL patterning of a salt-doped PE has not previously been investigated. Expanding EBL patterning to salt doped PEO required addressing the concern that the added ions may capture incident electrons, which could potentially prevent cross-linking. This may inhibit pattern formation and/or lower the ionic conductivity, which would be detrimental for device performance. There is some research to suggest EBL should at least not be detrimental to device performance; unpatterned PE films used in battery applications have seen a conductivity enhancement after irradiation with high energy electrons.[303,304]

My initial work towards realising PE-gated NWFETs was to evaluate the viability of EBL patterning and optimise the process. Thin films were produced using the following method.[196,204,217] First, PEO (MW 100 k) and $LiClO_4 \cdot 3H_2O$ with

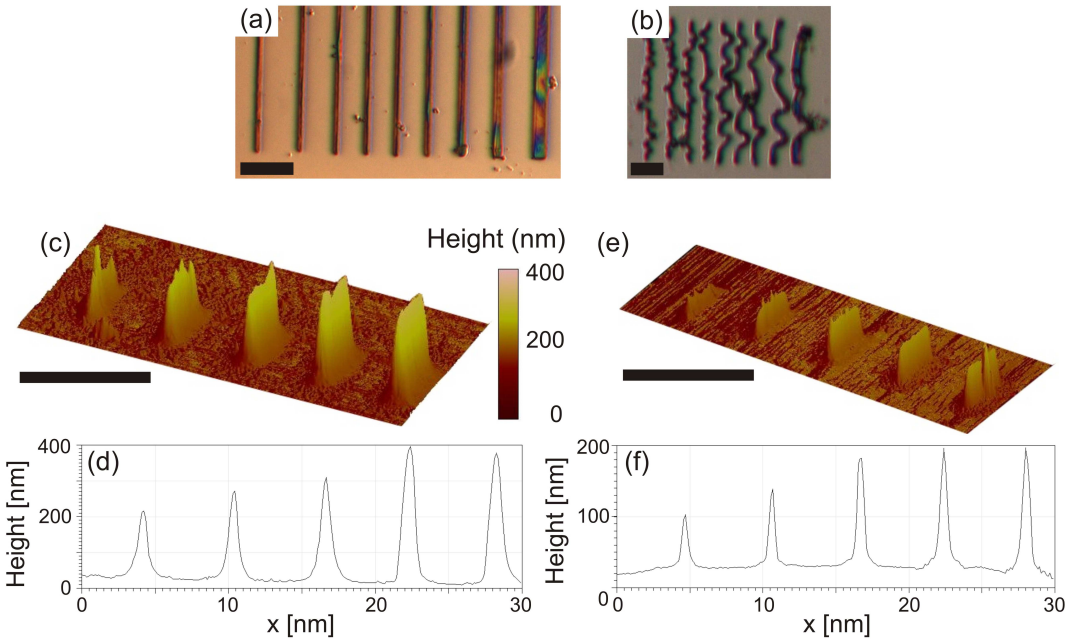

FIGURE 4.9: (a/b) Optical micrographs of 50 μm long patterned PEO/$LiClO_4$ strips with $w_d = 50, 100, 200, 300, 400, 500, 750, 1000$ and 2000 nm from left to right, with doses (a) 400 $\mu C/cm^2$ and (b) 100 $\mu C/cm^2$. The high dose in (a) resulted in w_m saturation for $w_d < 500$ nm. The pattern distortions in (b) were sometimes observed when low doses were used. (c/e) 3D rendered atomic force micrographs and (d/f) cross-sections of 4 μm long PEO/$LiClO_4$ strips with $w_d = 100$ nm patterned using doses of $50, 100, 200, 300$ and 400 $\mu C/cm^2$ from left to right. The polymer:salt ratios were 10:1 in (c/d) and 2.4:1 in (d/f). Reducing dose at constant w_d decreased w_m and feature height.

polymer:salt ratios 10:1, 8:1 or 2.4:1 were dissolved in methanol by sonication for $10 - 15$ minutes. The mixture was left standing overnight to precipitate out any large undissolved particulates. The supernatant was spun onto the sample at 4000 rpm for 60 s and the sample was baked at 90°C on a hot-plate for 30 minutes to evaporate the remaining solvent. Preliminary patterning tests were done using the Sirion SEM/EBL tool, with a 5 kV accelerating voltage and typical beam currents $\sim$ 20 pA. Development consisted of a 25 s rinse in H_2O to remove the unexposed regions of the film, and the sample was dried with N_2 gas.

Figure 4.9 shows optical microscope and atomic force microscope (AFM) images of patterned PEO/$LiClO_4$ films on Si substrates. These patterns provided initial confirmation that this PE could be patterned by EBL. They were then used to gauge the resolution limits for the PE strips that were ultimately used on the

NWFETs. The biggest limit to resolution for negative-tone EBL resists is the proximity effect, whereby secondary electron emission at high accelerating voltages and doses causes cross-linking outside the intended regions. The resultant pattern broadening meant that two line-widths were important for EBL-defined PEO strips. The first is the line-width w_d defined by the EBL pattern, and the second is the measured PEO line-width, w_m. We took w_m as the full-width at half maximum as measured by AFM. Having already chosen a low accelerating voltage, 5 kV, to reduce the proximity effect,[238] we turned to optimising dose within other constraints of the materials system.

Figure 4.9(a) shows one example of how dose dominates pattern definition for a 10:1 PEO/$LiClO_4$ film. The pattern traced by the electron beam was a series of lines of differing $w_d = 100 - 2000$ nm, but the resulting w_m saturated for $w_d \leqslant 500$ nm when a dose of 400 μC/cm^2 was used. Since w_d no longer uniquely determined w_m, further reducing w_m entailed setting a constant line-width 100 nm and reducing the dose to various values from 400 to 50 μC/cm^2. The resulting pattern is shown in Fig. 4.9(c/d), with the obtained $w_m = 1.2$ μm $-$ 820 nm from right to left.

Two materials limitations prevented further dose reduction. Firstly, the feature height on this sample also fell from 350 nm to 150 nm with decreasing dose. This aspect was somewhat variable, with heights < 100 nm sometimes observed at doses of 100 μC/cm^2. It was important that feature height did not fall further than this to ensure the PEO continuously covered the nanowire. Secondly, low doses < 100 μC/cm^2 provided insufficient cross-linking to generate suitable surface adhesion. This occasionally resulted in unrestrained swelling for some sections of the PEO/$LiClO_4$ during development. The result was pattern distortions like those shown in Fig. 4.9(b). Pattern distortions frequently occurred for patterns with defined widths $w_d < 100$ nm also. These results pointed towards using $w_d =$ 100 nm and a dose of 100 μC/cm^2 for the 10:1 PEO/$LiClO_4$ films. When applying these patterns to NWFETs on the n^+-Si/SiO_2/HfO_2 substrates, we found that w_m was further reduced to values as low as ~ 600 nm. This suggested a reduced interaction volume and proximity effect, which has been previously observed for

bilayer dielectrics.[305] Further reduction in line widths are likely to be possible if smaller feature heights are viable for a particular device architecture.[301,302]

The final aspect of patterning was the influence of increased salt content. The height and w_m for features patterned with 8:1 PEO/$LiClO_4$ films were similar to that for the 10:1 films. However, the increased salt content for the 2.4:1 films resulted in a reduction of feature dimensions, as seen in Fig. 4.9(e/f). This suggests that some electron capture did occur at the expense of cross-linking. The dose needed to be increased by a factor of 8 to obtain the same feature size from 2.4:1 films as for 10:1 films. The concern still was that electron capture may adversely affect device performance through neutralising Li^+ ions. As with the multiple wrap-gate NWFETs, the best way to evaluate electrical properties was with electrical methods from incorporating the PE into NWFETs. The PE line widths $w_m \sim 600 - 800$ nm were sufficient to fit strips of the dielectric between the contacts of our $3 - 6$ μm long nanowires.

4.2.2 Single PE-gated nanowire transistors

A schematic and AFM image of a NWFET featuring a nanoscale patterned PEO/$LiClO_4$ dielectric are shown in Fig. 4.10(a/b). The fabrication method proceeded as follows:

1. As-grown InAs nanowires were deposited onto the measurement substrate.
2. Source, drain and gate contacts were defined in PMMA by EBL.
3. The contact metal was 25/75 nm Ni/Au deposited by thermal evaporation. Lift-off in NMP removed all unwanted metal.
4. PEO/$LiClO_4$ thin films were prepared and spun as outlined above.
5. Strips were patterned in the PE film to link the gate electrodes and NW using the Raith150-Two. The strips were defined with $w_d = 100$ nm and dose of 100 μC/cm^2.

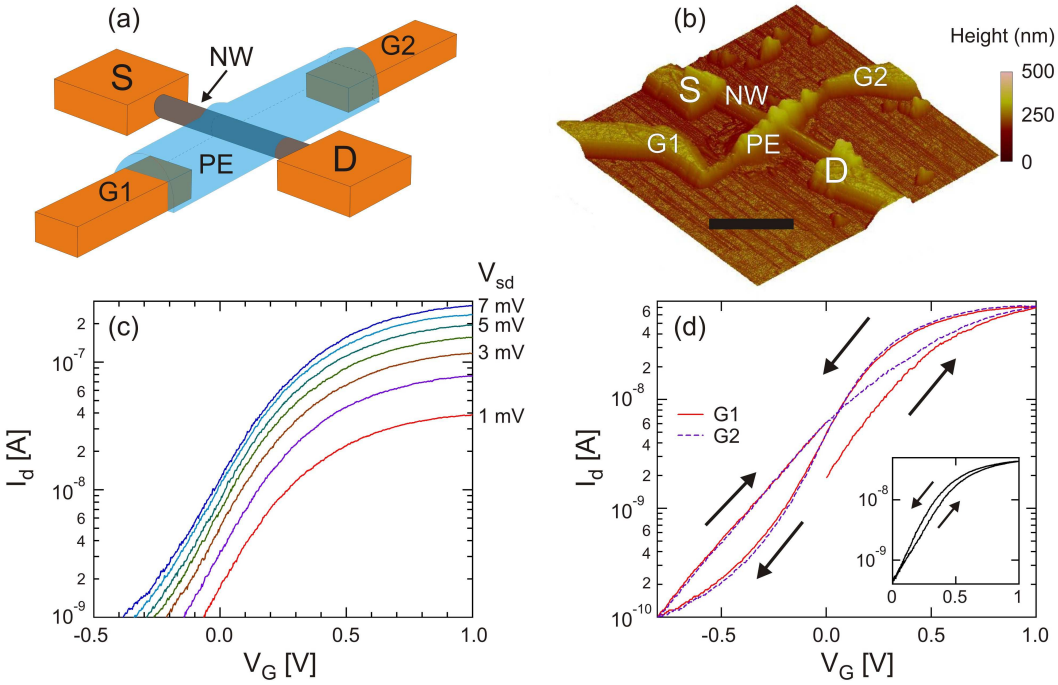

FIGURE 4.10: (a) Schematic and (b) atomic force micrograph of a NWFET featuring a nanoscale patterned PE gate dielectric, showing Ni/Au source (S), drain and gate contacts (G1 and G2). The polymer electrolyte (PE) spans the gap between the gate electrodes and the nanowire. (c) I_d vs V_{G1} at increasing V_{sd} for a PE-gated NWFET. The low subthreshold swing is indicative of effective gating and compares well with metal/oxide wrap-gated NWFETs. (d) Hysteresis for a device with $s_{G1} = 1$ μm and $s_{G2} = 4$ μm. The two time-limited behaviours of surface state trapping and EDL formation generate a complex figure-of-eight loop shape when devices were swept to the full off state. Despite the factor of 4 difference s_{G1} and s_{G2}, the electrical characteristics of G1 and G2 were almost identical apart from the 'virgin' behaviour of the initial trace. This is because properties of the EDL do not depend on the thickness of the dielectric (see Fig. 4.11 below). (Inset) Restricting V_G sweep range avoided the figure-of-eight hysteresis loop.

6. Devices were completed by development of the PE films in H_2O for 25 s.

It is worth noting the low number of fabrication steps compared to metal-oxide wrap-gate fabrication. This process does not rely on a series of specialised etches, and devices are completed simply by developing the PE resist. This makes the above process a powerful method for achieving strong, local electrostatic gating of NWFETs with high yield.

The device in Figs 4.10(a/b) featured two gate electrodes, G1 and G2, connected by a single PE dielectric. The two separate gate electrodes were used to test the

dependence of device properties on electrode/NW separation s_{GN}. The G1/NW separation on all devices with a single PE dielectric was held constant at $s_{G1} = 1$ μm, while s_{G2} was varied from $1-4$ μm. Devices were again studied using the SR830 to supply ac excitation V_{sd} at 73 Hz at the source and detect I_d at the drain. Gates were tested to ensure there were negligible leakage currents in the measurement range using a Keithley K2400 SMU, and low-noise Yokogawa GS210 voltage sources were used to increment V_{G1} or V_{G2} at 5 mV/s for data collection. Each gate was swept separately with the opposite electrode grounded. This was a matter of convenience; floating the opposing gate electrode had no influence on device performance. All experiments on PE-gated NWFETs in this section were conducted at room temperature in ambient.

Figure 4.10(c) shows the transfer characteristics I_d vs V_{G1} for a device featuring a PEO/$LiClO_4$ dielectric with 10:1 polymer:salt ratio at increasing $V_{sd} = 1-7$ mV. In this figure the gate was swept towards negative V_{G1}. The strong electrostatic gating supplied by the PE dielectric turned off I_d within a 1.5 V range, aided by the low $SS = 271$ mV/dec. Twelve devices featuring dielectrics with 10:1 salt ratio were studied, which gave an average $SS = 307 \pm 33$ mV/dec and $V_{th} = 0.16 \pm 0.06$ V at $V_{sd} = 2$ mV across the 22 working gates. The average SS compares very favourably to previously studied InAs NWFETs; room temperature SS for metal/oxide wrap-gates is typically $100-750$ mV/dec,[22,23,139,140,145,294,295] while the less effective substrate gates typically achieve only $SS = 1-4$ mV/dec.[22,30,145,146] The major advantage of substrate gating is simplicity of fabrication compared to metal/oxide wrap-gates. The patterned PE presented here offers an attractive compromise between the two common architectures; PEs enable strong, local gate control using simple fabrication methods.

A commonly encountered feature in most research-level FETs is gate hysteresis. These devices are no different, with an example of the hysteresis observed shown in Fig. 4.10(d). Interestingly, the hysteresis took a figure-of-eight form rather than a simple clockwise or anti-clockwise loop. This can be explained by the presence of two competing time-limited behaviours. The first contribution was likely to be charge trapping in InAs surface states,[22,23,48] similar to the effect of GaAs

surface states on *p*-AlGaAs/GaAs devices in Chapter 3. For the electron devices here, surface states should cause a clockwise hysteresis loop, as traced out in the discussion surrounding Fig. 1.7 in Sec. 1.3.2. Indeed, this is commonly observed in metal/oxide wrap-gated NWFETs.[22,23]

The second contribution to hysteresis is likely to have arisen from the limited ionic conductivity in the PE, which causes electric double layer (EDL) formation to take a finite amount of time (milliseconds to seconds).[8,203,204] In contrast to surface states, time-limited EDL formation should cause an anti-clockwise hysteresis loop. The rationale for this is as follows. Consider starting at $V_G = 0$, with a random equilibrium distribution of ions in the PE dielectric, and initial electron density n_i contributing to initial current I_{d0}. Applying negative V_G drives negative ions towards the NW channel, depleting electrons. Upon sweeping V_G back to 0 V, the ions in the PE take a finite time to reach the initial equilibrium configuration. This results in a net negative ionic charge in proximity to the channel, with a final electron density and current lower than the initial values, i.e., $n_f < n_i$ and $I_{df} < I_{di}$. This traces an anti-clockwise hysteresis loop.

The different loop directions and time scales for these two contributions likely resulted in the complex figure-of-eight pattern when the device was swept to the full 'off' state. The figure-of-eight could be negated by limiting sweep range, as demonstrated in the inset to Fig. 4.10(d). The exact parameters varied between devices, but halting the sweep towards depletion in the range $I_d = 10^{-9} - 10^{-10}$ A was usually sufficient to prevent the figure-of-eight hysteresis. The dynamics of ion transport and surface state charge trapping will be examined in detail as part of Chapter 6.

PE dielectrics possess a number of interesting features that distinguish them from conventional dielectrics. These arise from the differing nature of EDL formation *via* ion transport in PEs and direct field effects from the polarisation of molecular dipoles in conventional dielectrics (recall Fig. 1.25 in Sec. 1.6.1).[8] The NWFETs developed here facilitated demonstration of some of these effects, which also provided confirmation that the gating was due to ionic transport and EDL formation.

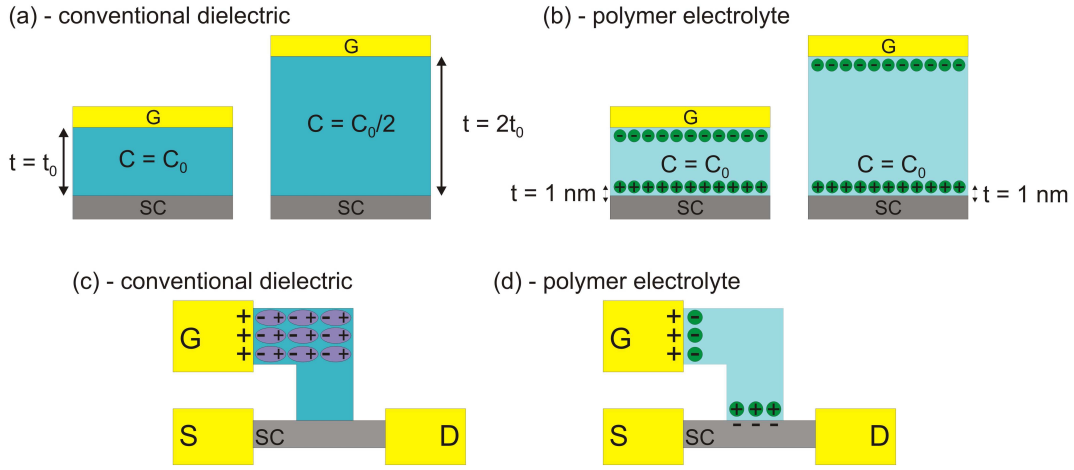

FIGURE 4.11: Comparison between conventional dielectrics and polymer electrolytes when used between a gate G and semiconductor channel, SC. (a) In a conventional dielectric, doubling the layer thickness t halves the dielectric capacitance C. (b) In a polymer electrolyte, the capacitance is a property of the EDL, since this is where the voltage drop occurs. Increasing the separation between the gate and semiconductor does not influence the dielectric capacitance. (c) Gating using a conventional dielectrics is facilitated by molecular polarisation. Gating does not occur if the gate electrode does not align with the semicondcutor channel. (d) Ion transport in polymer electrolytes facilitates very different behaviour. The positive voltage on G drives ion transport and EDL formation even for geometries where the gate electrode is offset from the channel and/or screened by the source/drain contacts.[197,205]

Investigating the interesting features was partially to allay concerns that electron capture at the EBL patterning stage caused neutralisation of ions and that any gating effect was due to direct field coupling through a PEO layer functioning as a conventional dielectric. Closely positioned metal electrodes have been shown to exert electrostatic control over nanowires,[306,307] so it was worth ruling out direct field effects as the major contribution to gate control in these devices. There are four major differences that we used to determine that the dielectrics operated as PEs.

1. Effective gating: If EBL neutralised Li^+ ions and gating occurred by direct field effect, the performance of the gates could be expected to be similar to devices with no dielectric at all.

2. $LiClO_4$ concentration: This should strongly influence device performance if EDL formation dominates the gating behaviour.

3. NW/gate separation dependence: The capacitance of conventional dielectrics scales with thickness. This means that performance is reduced for increasing NW/gate separation. By contrast, the voltage in a PE drops only across the EDL at the NW surface. This means the capacitance depends only on the properties of the EDL, which are not affected by material thickness (see Fig. 4.11(a/b)).[8,308]

4. Novel gate geometries: Conventional dielectrics work only if gate electrode is in the 'line-of-sight' of the transistor. Ion transport in PEs enable a unique 'non-local' gating effect, where the gate potential drives charge to the channel surface even if the electrode and channel are offset (see Fig. 4.11(c/d)).[197,205]

I will now demonstrate the first three features listed here using single PE-gated NWFETs, with novel gating geometries (feature 4) investigated in the next section.

Figure 4.12(a) presents I_d vs V_{G1} for representative devices featuring no PE dielectric, and PE dielectrics with polymer:salt ratios 10:1, 8:1 and 2.4:1. The gating effect for the device with no patterned PE dielectric was dramatically diminished. There was a small residual direct field effect, but this only reduced I_d by a factor of 3 in the same V_{G1} range where the dielectric with a 10:1 ratio reduced I_d by a factor of almost 10^3. As for the salt concentration, there was little difference in performance between the dielectrics with ratios 10:1 and 8:1. However, performance was reduced for the device with ratio 2.4:1. These observations were supported by the SS values across a number of devices. For 10:1, $SS = 307 \pm 33$ mV/dec (as above), 8:1 devices gave $SS = 286 \pm 45$ mV/dec and devices with 2.4:1 ratios gave $SS = 431 \pm 53$ mV/dec. These SS values are consistent with previously determined trends for ionic conductivity versus concentration for Li^+ in PEO.[202,308–310] Conductivity tends to increase with salt concentration until it peaks for ratios around 8:1. Further increases in salt concentration causes crystallisation of the host polymer.[8,202] Crystallisation impairs conductivity because ion transport takes place in amorphous regions of the material.[202,303,311]

A practical consideration was that patterning PE films for NWFETs using the low accelerating voltage was sometimes problematic. Obtaining accurate alignment

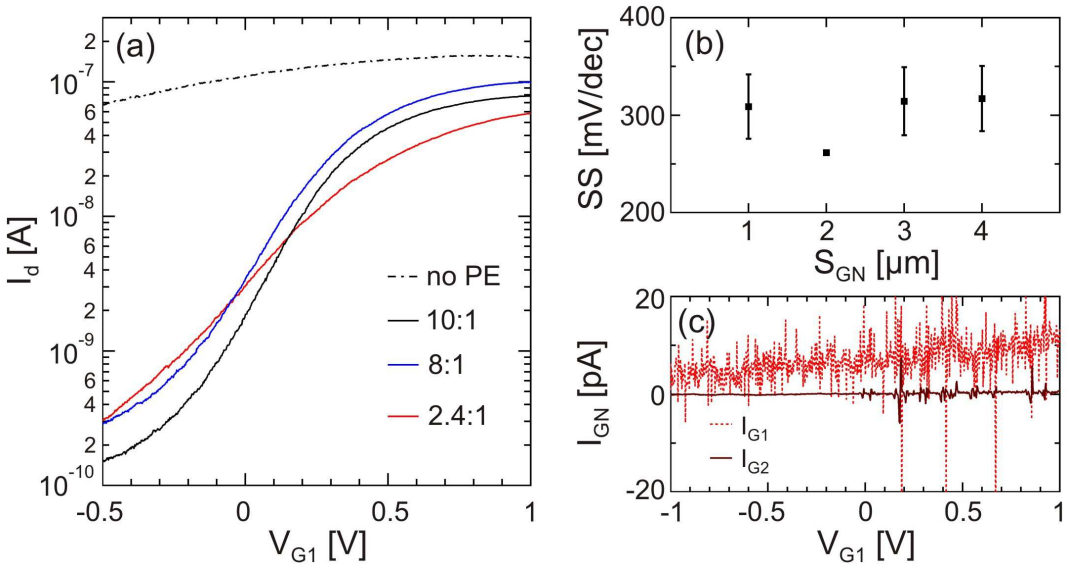

FIGURE 4.12: (a) I_d vs V_G for four NWFETs: One with no dielectric between G1 and the NW (dot dash black trace), and one each featuring PE dielectrics with polymer:salt ratios 10:1 (black solid trace), 8:1 (blue solid trace) and 2.4:1 (red solid trace). The much more effective gating offered by devices with PE dielectrics and the dependence of gate characteristics on salt concentration strongly suggests that ion transport dominates over any direct field effects. (b) Subthreshold swing SS as a function of gate/NW separation s_{GN} for devices featuring PE dielectrics with 10:1 polymer:salt ratio. Error bars represent the standard deviation of each data set. The effectiveness of the gate did not depend on s_{GN}; this is because the gate capacitance in PEs depends on properties of the EDL. The value for $s_{GN} = 2$ μm deviated from the trend and had a low associated standard deviation because only two devices with this s_{GN} worked, and they coincidentally had very similar SS. (c) Current measured at G1 (dotted trace) and G2 (solid trace) for applied voltage V_{G1}. Both I_{G1} and I_{G2} were essentially zero, as no electrical current passes through polymer electrolytes. The clean and accurate signal for I_{G2} is due to the extremely sensitive measurement capabilities of the K6517 electrometer compared to the K2400 SMU used to measure I_{G1}.

was achieved by viewing pre-patterned alignment markers underneath the resist layer prior to exposure. This relies on the electron beam penetrating the resist layer, and the backscattered electrons reaching the detector. However, the low accelerating voltage means the electron beam penetration depth and number of backscattered electrons was low. As a result, alignment marker visibility was often impaired, and sometimes the films were entirely opaque to the electron beam. This prevented accurate alignment and significantly reduced device yield. Films with 8:1 polymer:salt ratio were more susceptible to this than films with ratio 10:1,

perhaps due to the increased ion concentration. As such, most of this work focussed on dielectrics with salt concentration 10:1, which provided the best compromise between patternability and device performance.

Turning to how the gate/NW separation s_{GN} affected device performance, an isolated example was actually already given in Fig. 4.10(d). G2 for this device had $s_{G2} = 4$ μm, compared to the $s_{G1} = 1$ μm. Despite the factor of four increase in separation, the two traces were identical. Although not all devices had the same remarkable similarity between gates, on average s_{G2} did not affect device performance. This is illustrated by plotting SS against s_{GN} in Fig. 4.12(b). The lack of SS dependence despite gate/NW separations up to 4 μm clearly demonstrates that gate capacitance was not affected by the material thickness. This gives strong support to the notion that the gating effect is due to EDL formation by ionic charge transport.[8]

One feature that PEs do have in common with conventional dielectrics is that no electrical current passes through the material under gating.[8] The charge motion through the polymer consists only of ions drifting under the influence of an external electric field, and no charge passes into or out of the metal contacts. This is demonstrated in Fig. 4.12(c), where a Keithley K2400 SMU was used to apply V_{G1} and measure any leakage current I_{G1}. A Keithley K6517 electrometer was used to simultaneously measure the current I_{G2} at G2, on the opposite side of the PE dielectric. Both currents I_{G1} and I_{G2} were on the order of pA for the entire V_{G1} range, with the fluctuations arising due to noise.

4.2.3 Dual PE-gated nanowire transistors

EBL patterning of the PE opened up the possibility of NWFETs with multiple independent gates, linked to the nanowire using separate PE strips. The schematic and AFM image for one of these devices are shown in Fig. 4.13(a/b). Fabrication of this device differed from the single dielectric devices only in the EBL pattern

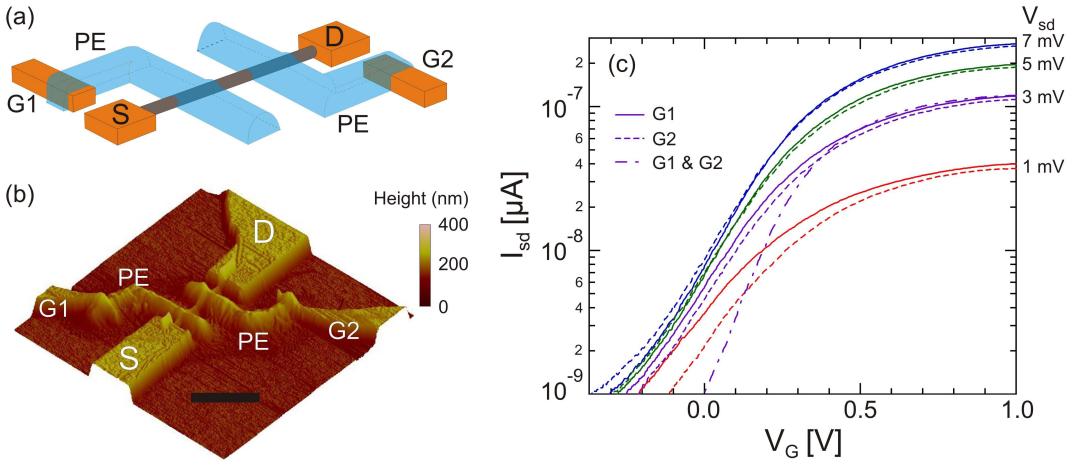

FIGURE 4.13: (a) Schematic and (b) atomic force micrograph NWFET featuring two independent nanoscale patterned PE gate dielectrics, showing Ni/Au source (S), drain and gate contacts (G1 and G2). G1 and G2 were offset to preclude direct field effects influencing the channel; gating in this device operated solely through EDL formation. (c) Transfer characteristics of a dual PE-gated NWFET with V_{G1} swept and V_{G2} grounded (solid lines), V_{G2} swept and V_{G1} grounded (dashed lines) and V_{G1} and V_{G2} swept simultaneously. The two gates are very well matched, with remarkably similar subthreshold properties. The increased depletion when both gates are swept together is indicative of independent operation.

used, with all other steps remaining the same. This device also featured a 'non-local' gating geometry, where the metal electrode was physically offset from the channel.[197,205] This geometry eliminated direct field coupling between the gate and NW, and ensured that gating occurred solely *via* ionic transport and subsequent EDL formation.

Transfer chacteristics for G1 and G2 of a dual PE-gated NWFET are shown in Fig. 4.13(c). The electrical properties closely resemble that of the single PE-gated NWFET in Fig. 4.10, supported by the similar $SS = 332$ mV/dec and 321 mV/dec at $V_{sd} = 2$ mV for G1 and G2, respectively. This strongly highlights the unique properties of PEs – despite a $s_{GN} \sim 4$ μm and a non-local geometry, SS for these devices was within experimental error of SS for single PE-gate devices with $s_{GN} = 1$ μm. This makes it clear that EDL formation is the major contribution to gating in these structures. Simultaneously sweeping both G1 and G2 improved depletion, with a resulting $SS = 192$ mV/dec (dot-dash line in Fig. 4.13(c)).

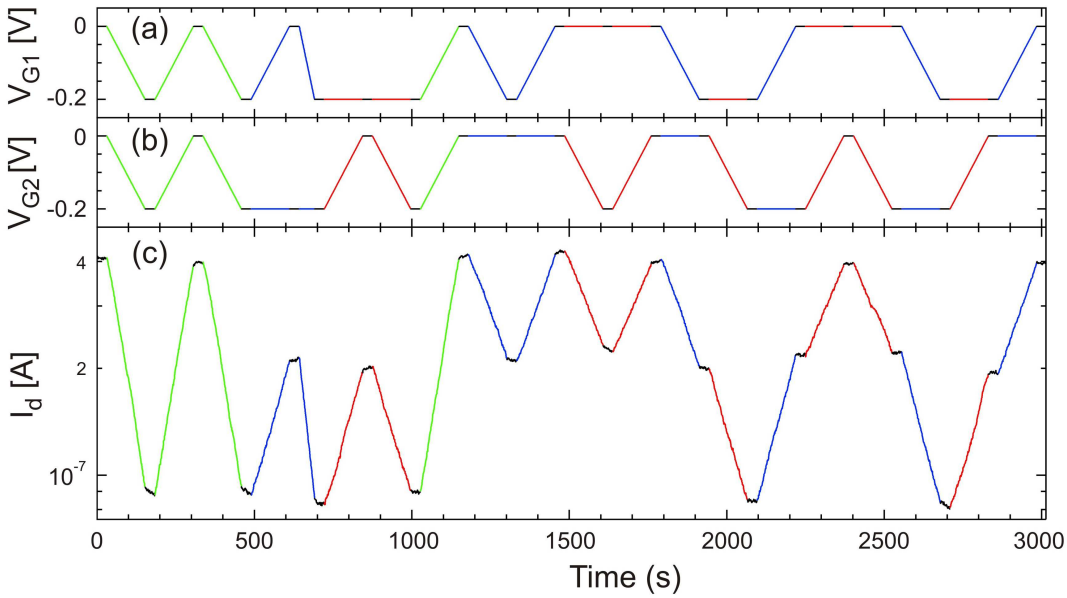

FIGURE 4.14: (a) V_{G1}, (b) V_{G2} and (c) I_d vs time with constant $V_{sd} = 42$ mV for a logic program with logical 1 set as $V_{GN} = 0$ V and logical 0 set as $V_{GN} = -0.2$ V. Gates were incremented at 2 mV/s together (green traces) or separately, with either V_{G1} swept and V_{G2} held constant (blue traces) or V_{G2} swept and V_{G1} held constant (red traces). A 30 s wait time was used between sweeps to examine the stability of I_d output states. The equality of the I_d output states for input states (1,0) and (0,1) highlights the excellent electrical balance of the gates in this device.

The data in Fig. 4.13(d) and the SS values show that G1 and G2 on this device had remarkably good electrical balance. To further illustrate the gate independence and electrical balance between the gates, we applied the two-gate logic program used previously for metal/oxide wrap-gates in Figs. 4.4 and 4.5. The resulting data for the dual PE-gated NWFET is shown in Fig. 4.14. Each gate voltage V_{GN} was swept between two pre-defined values – in this case 0 V and -0.2 V – in order to switch each input logic state between every other input logic state (Figs. 4.14(a/b)). Similarly for the metal/oxide wrap-gated device, the I_d output in Fig. 4.14(c) took distinct values corresponding to the input logic states. The long term stability of the PE-gated device was reduced compared to the wrap-gated devices; this is likely due to the increased surface state influence here, which was eliminated for wrap-gated devices by measuring at $T = 77$ K.

An impressive feature of the data in Fig. 4.14(c) is that the I_d output was equal for the (1,0) and (0,1) logic states. The degeneracy of these outputs is indicative of

identical coupling between the gate and NW for both G1 and G2. This excellent electrical balance was actually observed in the majority of dual PE-gate NWFETs, indicating a high degree of reproducibility. Reproducibility is an important topic in nanoscale devices, because small defects can have a large influence. The reproducibility of the PE-gates far exceeds that of the metal/oxide wrap gates we studied, and is likely a product of the EDL. Since the EDL consists of ions 1 nm away from the semiconductor,[8,203] only defects at the nanowire surface could influence device properties. This contrasts with the metal/oxide wrap-gates where defects in the oxide layer could also contribute to irreproducibility.[13]

4.3 Discussion

In this Chapter I presented two routes to realising strong local electrostatic control of NWFETs with multiple gates. We advanced the use of metal/oxide wrap-gates by developing a highly scalable method to produce NWFETs with 2, 3 and 4 wrap-gates in series along the channel and developed electrical techniques to characterise gate performance. Materials optimisation of these structures would likely lead to GHz operation[296] and deployment in novel logic circuits.[293] I then presented a method to nanoscale pattern the PEO/$LiClO_4$ polymer electrolyte using EBL, and fabricated NWFETs gated using two independent PE dielectrics. These devices had excellent electrical reproducibility and balance. The major limitation for polymer electrolytes in general remains switching speed. The limited ionic mobility means that switching over large gate ranges is limited to $f \sim 1 - 100$ Hz.[8] An interesting class of polymer electrolytes is ion gels,[197,212,214,312] which consist of an ionic liquid that has been gelated by a relatively small fraction of polymer (typically $< 10\%$ polymer).[214] The comparatively high ionic conductivity that results from such a high ion density facilitates much faster transistor switching.[197,210,219] Investigating the nanoscale patternability of these would be an interesting project, since both PEO[215,313,314] and PMMA[212,315] have been used in different ion gels to provide the polymer backbone. Nevertheless, the patterned PE presented here is

still an excellent choice for the characterisation of nanodevices, due to the ability to generate strong local electric fields with a simple fabrication method.

Over the next two chapters I focus on experiments that illuminate two further applications for PE-gated NWFETs, and how these relate to dopant and surface impurities in InAs nanowires. In the next chapter I present results on using a PE to 'freeze-in' charge states at cryogenic temperatures to enhance the study of quantum systems. This technique allows a range of base-line charge densities to be set in a single device for separate cool-downs, as if the same device had different doping densities for different cool-downs. This is an interesting approach for quantum systems where a low impurity density is required to, e.g., achieve high mobilities. I then present results showing how surface and background impurity charges can dominate device behaviour, and tune the background potential generated by these impurities using the PE dielectric. In Chapter 6 I show that PEO without salt doping can act as a proton-conducting polymer electrolyte, and investigate the competing dynamics of ionic transport and surface state trapping as part of an effort to evaluate the use of III-V NWFETs as proton-to-electron transducers.

Chapter 5

Results: Using polymer electrolytes for external doping and setting background disorder potential

5.1 Setting and freezing ionic potential

In this Chapter I show how patterned PE gates can be used to enhance the study of quantum devices at cryogenic temperatures. Transport of Li^+ and ClO_4^- ions in poly(ethylene oxide) is strongly temperature dependent. The polymer chain relaxations that transport ions are hindered at lower temperatures and ions are immobilised for temperatures $T \leqslant 220$ K.[208] This results in a corresponding decrease in dielectric performance, illustrated in Fig. 5.1. The subthreshold swing of this PEO/$LiClO_4$-gated NWFET steadily degraded with decreasing temperature, until at $T = 220$ K the gate characteristics resembled the device with no dielectric in Fig. 4.12(a) of Sec. 4.2.2.

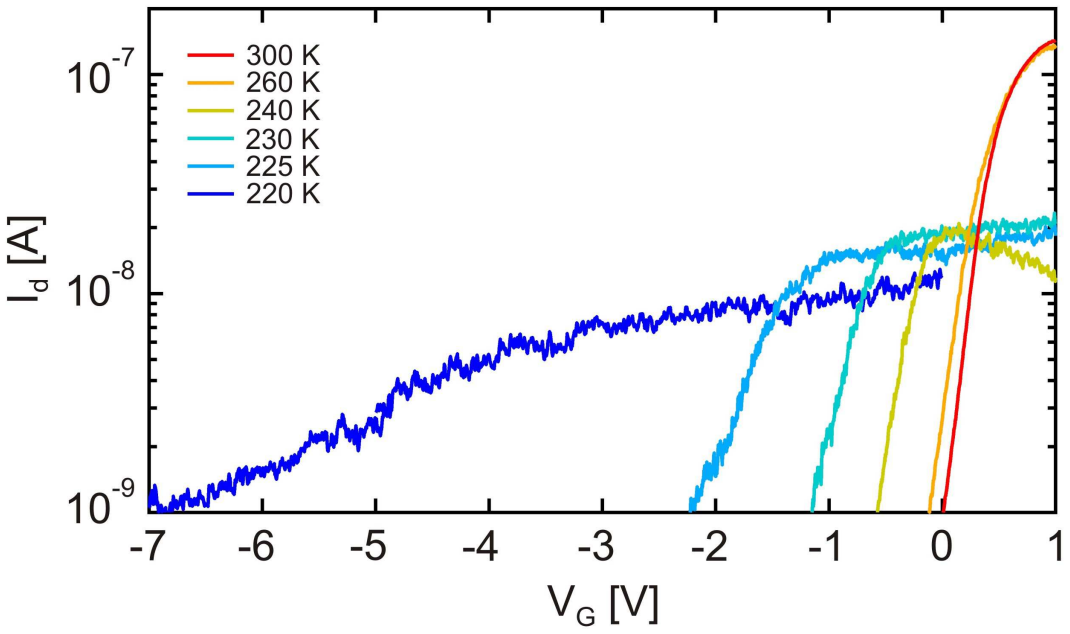

FIGURE 5.1: Current I_d through a PE-gated NWFET vs gate voltage V_G applied to the PE gate electrode with decreasing temperature $T = 300 \rightarrow 220$ K. Lower temperatures inhibit ionic motion and degrade transistor performance.

Using a 'frozen' PE gate in parallel with a second, conventional gate, e.g., a substrate/back-gate, brings added functionality to low temperature measurements in the following way. Cooling below $T = 220$ K with a non-zero V_G on the PE gate electrode sets and freezes in a particular non-equilibrium configuration of Li^+/ClO_4^- ions. That is, cooling with positive (negative) V_G fixes more Li^+ (ClO_4^-) ions close to the nanowire. Below $T = 220$ K, the ion configuration constitutes a potential V_{PE} that is independent of the voltage on the gate electrode V_G,[208] the back-gate voltage V_{BG}, or any other gate in parallel.[30,31] This means that the potential V_{PE} can be set at room temperature, frozen in place by cooling to cryogenic temperatures, and the resulting system properties probed using V_{BG}.

Figure 5.2 outlines the basics of this methodology. The device consisted of a NWFET with a PE gate and n^+-Si substrate as back gate, similar to that used in the previous chapter. Utilising a substrate/back gate becomes a more viable option at low T compared to at room temperature, since conventional metal and degenerately doped semiconductor gates are able to more effectively influence I_d with reduced T.[1,2] Fig. 5.2(a) illustrates that at $T = 300$ K, a back gate voltage

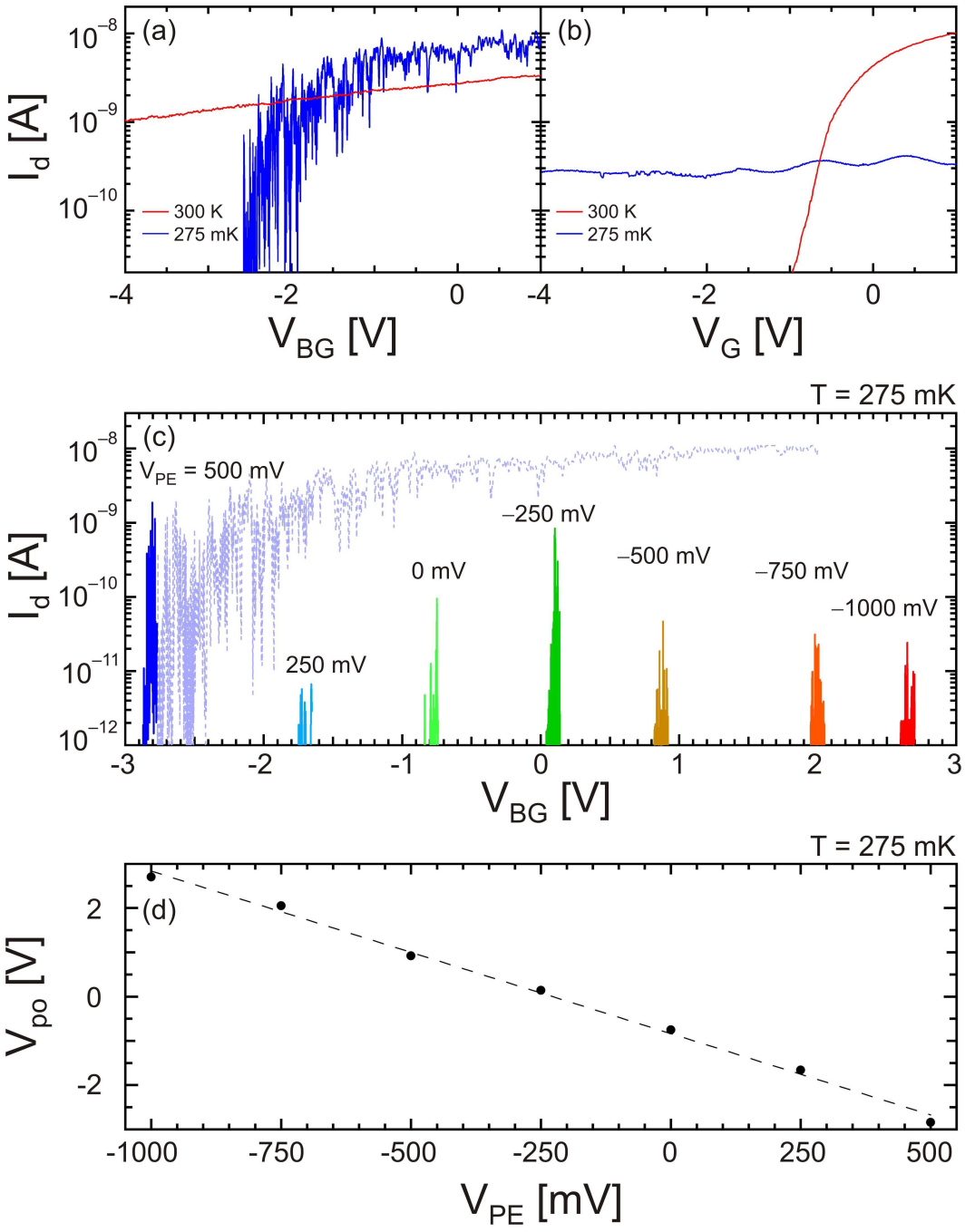

FIGURE 5.2: (a) I_d vs. V_{BG} applied to a n^+-Si backgate and (b) I_d vs. V_G applied to a gate electrode with a PE dielectric at $T = 300$ K and 275 mK. Low temperatures improved the performance of the back gate, but froze ionic motion in the PE. For the $T = 275$ mK trace in (a), we used $V_{PE} = 500$ mV to show that low-voltage operation of the back-gate was maintained even at the highest carrier density used in this work. For all other traces in (a/b) each gate was grounded when not in use. (c) I_d vs V_{BG} for the range $V_{po} \leqslant V_{BG} \leqslant V_{po}+100$ mV with different frozen in V_{PE}. The pinch-off voltage V_{po} is the V_{BG} where $I_d = 0$. Each trace was collected on a separate cooldown, with V_{PE} set at $T = 300$ K and held during cooldown. The dashed blue trace shows the full V_{BG} range; a similar tail was present for all other V_{PE}, but excluded from the figure for clarity. (d) Setting V_{PE} within a 1.5 V range at $T = 300$ K tuned V_{po} roughly linearly through a 6 V range at $T = 275$ mK. Using V_{PE} to alter the $V_{BG} = 0$ V carrier density constitutes a novel 'external doping' technique.

range -4 V $\leqslant V_{BG} \leqslant 1$ V tunes I_d by only a factor of 3 and is insufficient to pinch off the channel. By contrast, the nanowire can be pinched off within the same range at low $T = 275$ mK. I_d exhibits quantum interference effects typically observed in NWFETs and quantum dot resonance signatures near pinch-off, $I_d = 0$ A.[171,241] The latter is discussed in detail throughout this chapter. The temperature dependence of the PE performance is the reverse of the back gate (Fig. 5.2(b)). The strong gating effect at $T = 300$ K vanishes at $T = 275$ mK; the potential V_{PE} is frozen-in and independent of V_G. The weak quantum interference oscillations reflect residual direct field coupling between the gate electrode and the nanowire[306,307] across the 1 μm of PEO.

The simplest consequence of setting and freezing V_{PE} is a shift in the back gate threshold voltage and pinch-off point. This is because a positive (negative) V_{PE} increases (decreases) the electron density at zero back gate voltage $V_{BG} = 0$ V. The data in Fig. 5.2(c) demonstrates this effect, which was collected using the following methodology. The ion configuration was set by sweeping V_G at room temperature to the desired V_{PE}. This voltage was held constant while the device was cooled to $T = 275$ mK, which locked-in the base-line charge configuration in the nanowire. V_G was then swept to 0 and the voltage source was disconnected to fully demonstrate the charge freeze-in effect. Transfer characteristics were then collected by sweeping V_{BG}. Setting the next desired V_{PE} was accomplished by first warming the cryostat and device to room temperature to allow the ion configuration in the PE to be reset. The device was cooled down with this different V_{PE}, and a new set of measurements collected at $T = 275$ mK.

Setting positive voltage $V_{PE} \geqslant 0$ V accumulated electrons in the channel, and an increasingly negative V_{BG} was required to pinch off the nanowire. For negative $V_{PE} \leqslant -250$ mV the channel was already depleted at low T, requiring positive V_{BG} to accumulate electrons in the NW. In this way we could use V_{PE} to tune the back gate operating point linearly across a 6 V range (Fig. 5.2(d)). Using V_{PE} to set the $V_{BG} = 0$ V electron density can be thought of as an 'external doping' technique, since V_{PE} essentially serves the same purpose as dopant atoms. There are a number of advantages to using an external, field-effect technique over dopant

impurity atoms. Firstly, different effective doping densities can be set within the same device by simply cooling down with a different V_{PE}. Secondly, excluding dopants from the channel can be expected to increase the charge carrier mobility, as in modulation doping.[5,71,72] Thirdly, external doping may be useful in situations where doping is difficult or inappropriate. In particular, having greater control over base-line carrier density is useful for InAs nanowires, since they are typically undoped and the electron density is set by properties of the surface accumulation layer.[48]

5.2 Setting the background disorder potential

Our interest in tuning carrier density arose from the work by Heiner Linke's group at Lund University on enhancement of thermoelectric power factor $S^2\sigma$.[171] As mentioned in Sec. 1.5.5, they found that background disorder potential in nanowires leads to quantum dot-like states that couple with propagating modes to enhance the thermoelectric power factor over a large carrier density range.[171,176–178] Our aim in this project was to evaluate the suitability of polymer electrolytes for thermoelectric measurements since they offer the dual advantages of strong carrier density tuning and low thermal conductivity. The high thermal conductivity of a metal wrap-gate along the length of the nanowire may 'short-out' an applied thermal gradient. This would dramatically reduce the thermovoltage V_T, and mean the measurement was dominated by the metal gate, rather than the nanowire itself.

To study the disorder properties and thermoelectric response of PE-gated NWFETs we used the device in Fig. 5.3. It consisted of an InAs nanowire contacted with three ohmic contacts and a polymer electrolyte gate dielectric. The resistive heating strips provided a temperature gradient to generate open circuit thermovoltage V_T. The n^+-Si substrate was used as the back gate. Two different measurement set-ups were required to obtain the closed circuit electric current I_d and open circuit thermovoltage V_T, as described in Figs 5.3(b/c). Typically we performed I_d vs V_{BG} and source-drain bias spectroscopy measurements before switching to the

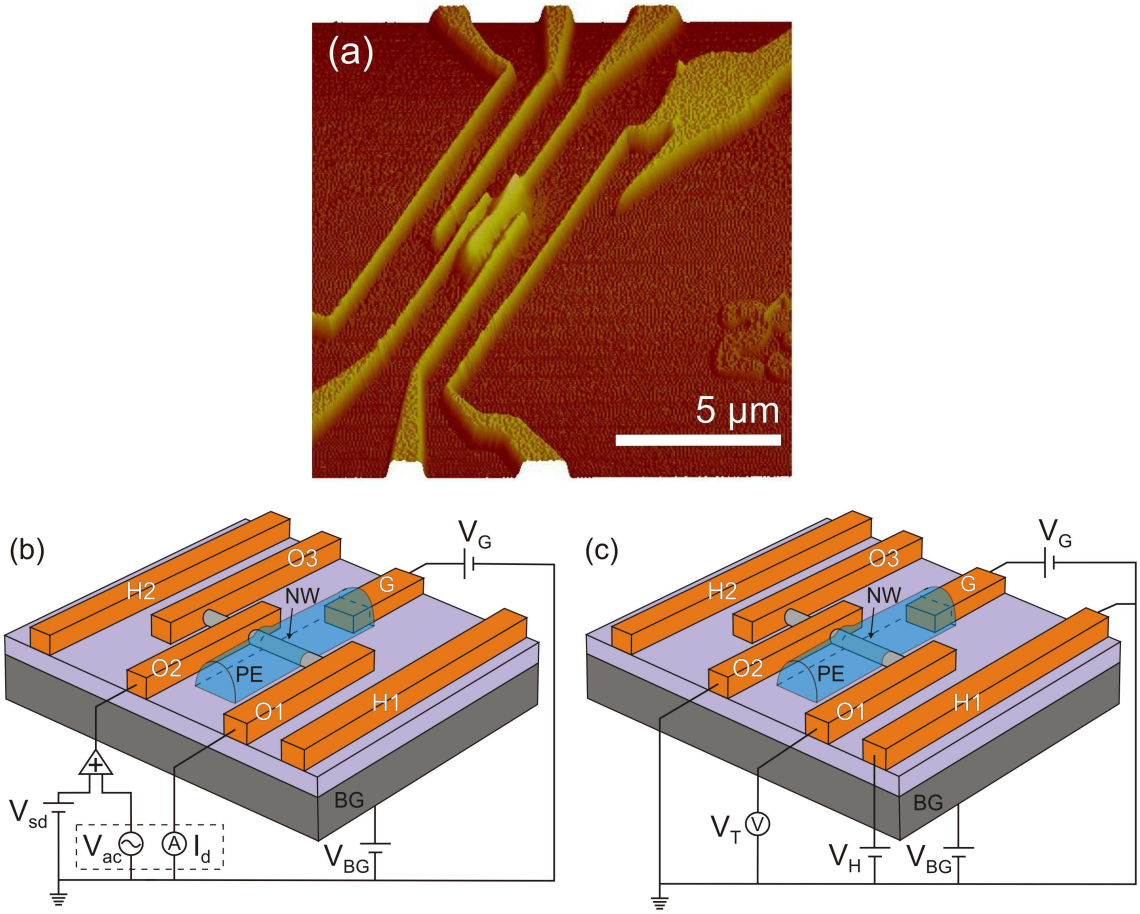

FIGURE 5.3: (a) Atomic force micrograph and (b/c) schematics of the device used in this chapter. Schematics show nanowire (NW), ohmic contacts (O1, O2, O3), heater strips (H1, H2), gate electrode (G), polymer electrolyte (PE) and n^+-Si substrate back gate (BG). (b) I_d measurement set-up. A Stanford SR830 lock-in amplifier (represented by the dashed box) sourced an ac excitation $V_{sd}^{ac} = 100$ μV at 13 Hz and measured I_d. A dc voltage V_{sd}^{dc} was supplied by a Yokogawa 7651 voltage source and added to V_{ac} for source-drain bias spectroscopy measurements using passive circuitry. (c) Open-circuit thermovoltage V_T measurement set-up. A dc voltage V_H was applied to heater strip H1, and the associated current flow generated a thermal gradient ΔT across the nanowire *via* Joule heating. The resulting open circuit thermovoltage V_T was measured between O1 and O2. V_T was amplified using a Stanford SR560 voltage preamplifier and then read out using a Keithley 2000 multimeter. In both set-ups V_G was applied to the polymer electrolyte gate at room temperature, and V_{BG} to the back gate at low T using a Keithley K2400 SMU.

V_T circuit. After V_T vs V_{BG} was obtained for each desired heating voltage V_H, a final I_d vs V_{BG} trace was taken to confirm measurement consistency. Measurements were performed in the Heliox ^{3}He cryostat described in Sec. 2.4.3. The base temperature was $T_B \sim 275$ mK throughout, and higher temperatures up to

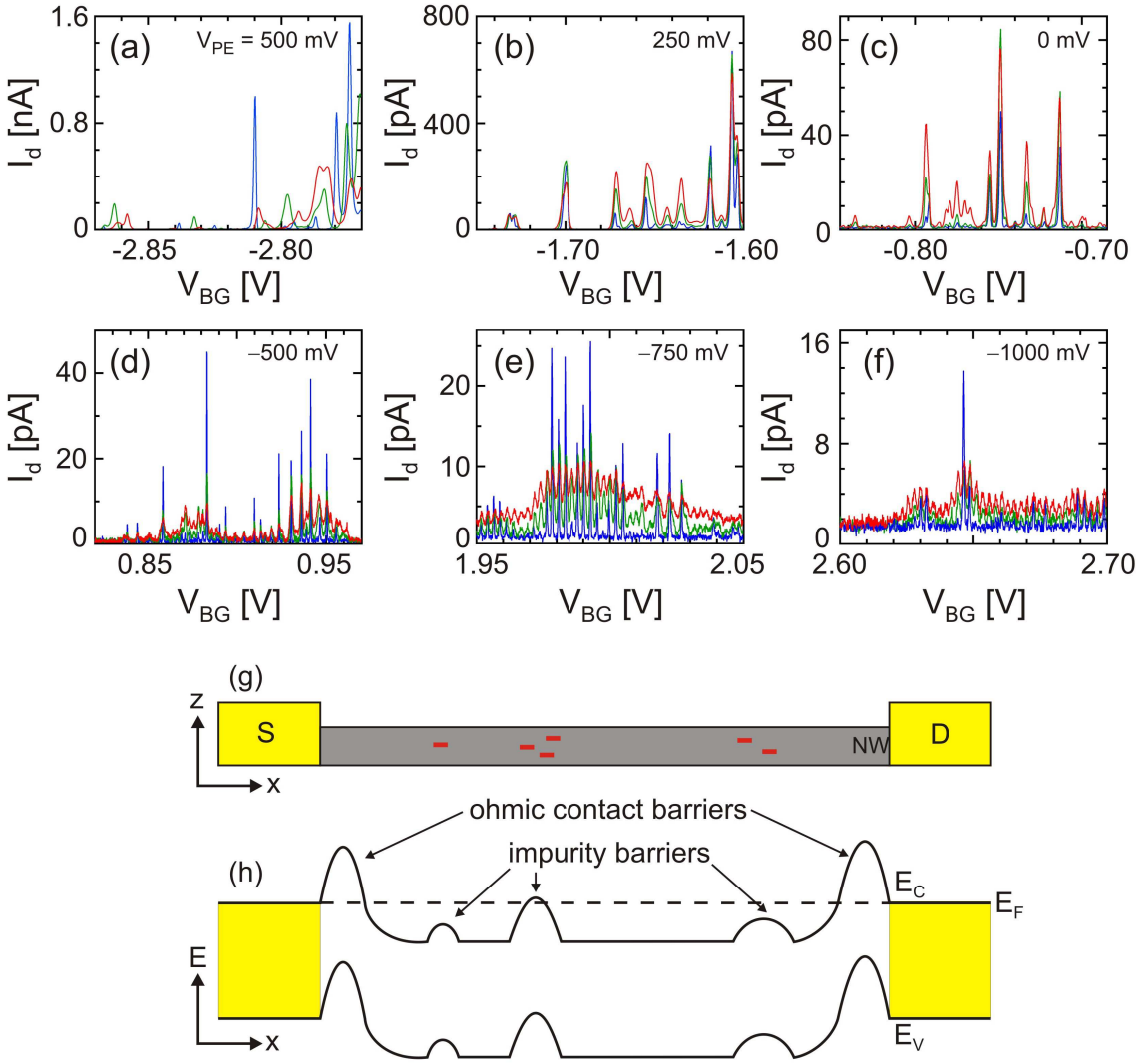

FIGURE 5.4: (a-f) I_d vs V_{BG} near pinch-off for increasingly negative V_{PE} settings with $T = 0.275, 1.5, 2.5$ K (blue, green and red traces respectively). Coulomb blockade resonances are apparent at all V_{PE}. (g) Physical schematic and (h) band diagram of a nanowire (NW) with ohmic contacts at the source (S) and drain (D). Strongly confining barriers in the vicinity of the ohmic contacts can arise from distortions of the gate potential. Weaker barriers along the nanowire length arise due to randomly placed ionised impurities, represented as red negative charges in (g).

$\sim$ 4.5 K were obtained by carefully controlling the ^{3}He pot heater and/or the amount of gas between the pot and charcoal sorb. V_H generated a thermal gradient ΔT that produced the open circuit V_T. It also locally raised the average temperature of the device, even while the cryostat maintained base temperature $T_B = 275$ mK. We determined the approximate average device temperature due to V_H by measuring I_d at each V_H and comparing the peak heights of quantum

dot I_d resonances with those measured when heating the cryostat. We found that applying $V_H = 20, 60$ and 100 mV corresponded approximately to average device temperatures $T_D = 0.7, 1.3$ and 2.0 K for the device, respectively.

Figure 5.4 shows I_d vs V_{BG} near pinch-off for six V_{PE} values between +500 and −1000 mV. Traces were taken at T = 275 mK, 1.5 K and 2.5 K obtained by heating the cryostat. I_d resonances were observed at all V_{PE}, consistent with previous observations of impurity-related transport barriers that define quantum dots along the nanowire length.[171,175,178] The most striking aspect of the data in Fig. 5.4 is that the regularity and robustness of the peaks increased with negative V_{PE}. The quantum dot signatures for $V_{PE} \geqslant 250$ mV were unstable, and often not reproducible for consecutive traces. This is apparent from Fig. 5.4(a), where the system at $V_{PE} = 500$ mV was not robust enough to produce a reproducible signal across the traces at each T. By contrast, the systems for $V_{PE} < 0$ mV were more stable; reproducible behaviour was obtained for days at a time while V_{BG} remained in the measurement range and a low T was maintained. Thermal excitation and electric fields altered the impurity distribution, and therefore the quantum dot resonances, in a similar fashion to the MCF changes observed in the hole billiard presented in Chapter 3. Changing V_{BG} by more than approx. 1 V and returning to the region of interest and/or separate cool-downs with the same V_{PE} gave similar overall peak heights and spacing, but with different specific peak positions and heights. This indicates a qualitative reproducibility of each system at set V_{PE}, but suggests the location and/or strength of the barriers can be altered by external fields and temperature changes.

With no 0D confinement introduced during nanowire synthesis or device fabrication, the question is: what is the origin of the quantum dot system? The Li^+/ClO_4^- ions are unlikely to directly provide the disorder potential; a high density of ions closely following the nanowire surface would provide a relatively uniform potential. Rather, we suggest V_{PE} accentuates the effect of pre-existing potential barriers. In nanowires, potential barriers have been observed to arise both due to the ohmic contacts at either end of the device,[241] and from charged impurities at the surface and in the bulk of the nanowire[171,175,178] (see illustration in Fig. 5.4(g/h)).

The barriers near the ohmic contacts arise as the gate potential becomes non-homogenous in the vicinity of the source/drain contacts, and produces a local electron depletion.[241] Depending on the interplay between the gate/contact potentials, the generated barriers can constitute a quantum dot with well defined confinement dimensions. By contrast, barriers generated by surface charges or ionised impurities in the bulk tend to provide weak, random confinement that changes with the location and charging state of the impurities.[171,175] Combined, Figs 5.4(g/h) show that nanowires at low T provide a highly non-uniform potential landscape for electrons. This example highlights very clearly how the behaviour of nanoscale devices can be dominated by surface and bulk impurities.

The changing nature of I_d resonances in Fig. 5.4 allows us to hypothesise the origin of each system. Increasingly negative V_{PE} produced narrower, more closely spaced peaks with maxima that decreased by over two orders of magnitude. The reduced peak height and greater regularity with more negative V_{PE} points to better defined barriers, while the reduced peak spacing is indicative of a larger dot size.[63] These features suggest the disorder at positive V_{PE} defines a series of small, weakly defined quantum dots, likely due to random impurity charges at the surface or in the bulk. At negative V_{PE}, the smaller peak spacing and reduced peak height indicate at least one large dot with well defined barriers. The most likely cause for this is barriers located at the ohmic contacts. The impurity defined barriers between the ohmic contacts then define small, weakly coupled quantum dots that contribute to the complex signatures in Figs. 5.4(d/e/f). Overall, these results show that in addition to setting a base-line carrier density, V_{PE} can be used to tune the background disorder potential for a low temperature quantum system.

We turn now to a focussed study of the system at $V_{PE} = -500$ mV, which proved the simplest system to understand. In addition to I_d measurements, we use source-drain bias spectroscopy measurements, a powerful tool for mapping quantum dot energetics (recall Sec. 1.4.3). This allowed us to examine our hypotheses regarding the source of quantum dot-like states in our device. We then looked at the thermovoltage signal. Investigating thermoelectric applications for PEs was doubly interesting since the PE could be used to tune the background potential as well as

the carrier density.[171] This is a strong example of how 'non-ideal' properties, i.e., surface charges and bulk impurities can sometimes be harnessed to generate new functionalities.

5.3 Probing the disorder potential

Figure 5.5 shows current, source-drain bias spectroscopy (SDBS) and thermovoltage data for $V_{PE} = -500$ mV. The I_d data in Fig. 5.5(a) is the same as in Fig. 5.4(d). SDBS involved the addition of two voltages at the source; an ac component $V_{sd}^{ac} = 100\ \mu$V at 13 Hz to generate the I_d signal detected at the drain using the phase sensitive detection of a lock-in amplifier, and a dc bias V_{sd}^{dc} to split the source/drain chemical potentials.[80] The experiment proceeded by stepping V_{BG} and sweeping V_{sd}^{dc}, with the resulting I_d plotted on a colour scale as a function of both V_{BG} and V_{sd}^{dc}. The purple diamonds where $I_d = 0$ are the transport-prohibited regions outlined in Sec. 1.4.3. The high I_d outside the diamonds (green to red colours) arises since a dot energy level is always between the source and drain potentials. Moving V_{BG} along the line $V_{sd}^{dc} \sim 0$ reproduces the resonances in I_d when the diamonds close. V_T was obtained in response to applied heater voltages $V_H = 20, 60, 100$ mV, which provided a small thermal gradient and also raised the average temperature of the device.

The temperature dependence of I_d peaks in Fig. 5.5(a) gives initial clues to the energetics of the system.[78,316,317] Peaks with the greatest amplitude at $T = 275$ mK became wider and shorter with increasing T, while the amplitude of suppressed peaks increased with increasing T. The former is observed in the quantum limit where the addition energy is large compared to k_BT, and transport can only take place *via* the ground state.[316] The latter behaviour is typically a product of thermally activated transport through excited states where the excited level spacing is small.[316] While both behaviours can be present in a single quantum dot where different levels have different couplings to the leads,[78,316] the observed temperature dependence in Fig. 5.5(a) is also a feature of multiple, serially coupled

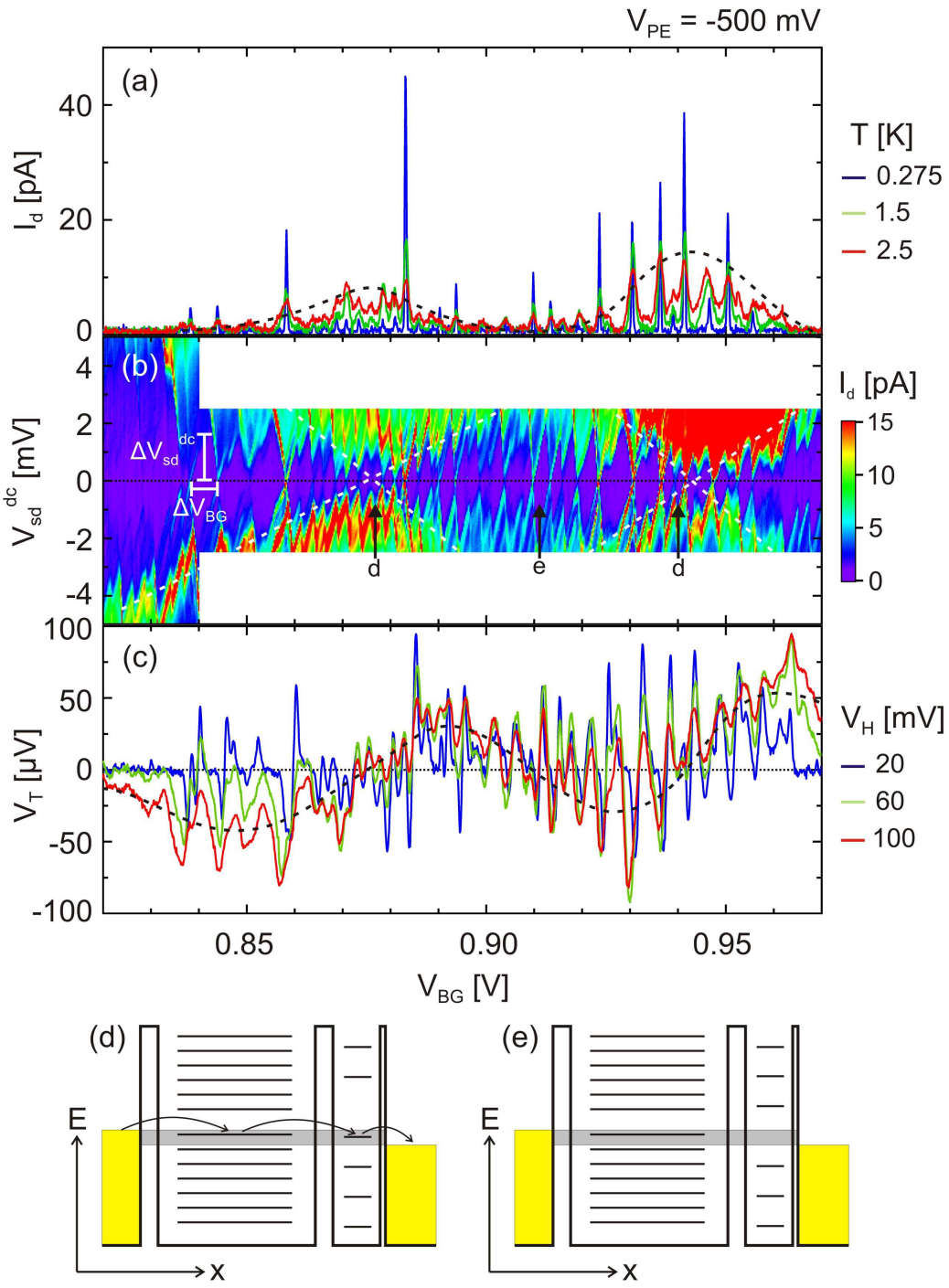

FIGURE 5.5: (a) I_d vs V_{BG} at $T = 0.275, 1.5, 2.5$ K, (b) source-drain bias spectroscopy (SDBS) and (c) thermovoltage V_T vs V_{BG} for heater voltages $V_H = 20, 60$ and 100 mV near pinch-off with $V_{PE} = -500$ mV. The temperature dependence in (a) and the double diamond structure in (b) suggests the nanowire is broken into two serially coupled quantum dots according to the explanation in the text. The background modulation of V_T at higher V_H is consistent with this explanation. The underlying I_d resonances, diamonds and V_T modulations are indicated by the dashed lines in (a/b/c). Diamond dimensions ΔV_{sd}^{dc} and ΔV_{BG} are used calculate dot charging energy, capacitance and length. (d/e) Conduction band diagram along the nanowire length x for (d) matched and (e) mismatched dot levels. Electrons traverse the system only when both dots have an energy level within the source/drain window shown in light grey. The data corresponding to the situations (d) and (e) are noted in (b).

quantum dots.[316,317] The latter seems the most likely origin for the data here, given previous evidence for disorder-defined quantum dots in InAs nanowires.[171,175]

SDBS was vital in determining the specific system defined by the background potential at $V_{PE} = -500$ mV; the data in Fig. 5.5(b) strongly suggests two serially coupled quantum dots. The most striking clue that there were two dots is the background of larger diamonds superimposed on the smaller diamonds, highlighted by the white dashed lines. The size of SDBS diamonds is proportional to the quantum dot charging energy, which is inversely proportional to dot size. Thus, a dot with large (small) physical size generated the small (large) SDBS diamonds. The observed pattern arose because transport through the entire double-dot system is possible only when energy levels from both dots are between the potential of the source and drain. This is illustrated in Figs. 5.5(d/e). When the levels of the two dots are aligned, only a small V_{sd}^{dc} is required to induce charge transport through the dot and a high I_d (Fig. 5.5(d)). If the levels are mismatched, a much higher V_{sd}^{dc} is required to induce high I_d (Fig. 5.5(e)). Looking back at the data in Fig. 5.5(b), the first case was seen at the points marked 'd'. At these V_{BG} values, the larger diamonds close, and a low V_{sd}^{dc} was sufficient to induce high I_d (red on the colour scale). The situation corresponding to Fig. 5.5(e) is marked with an 'e' in Fig. 5.5(b). At this V_{BG} setting there was a large mismatch in the dot energy levels, meaning that a significantly higher V_{sd}^{dc} was required for onset of high I_d. Between these two limits, the green and red I_d bands follow a diamond-like shape, highlighted by the white dashed lines.

Using this interpretation, we can return to Fig. 5.5(a) briefly and understand the temperature dependent data in more detail. We previously noted regions of suppressed I_d peaks that grew with increasing T, and regions of large peaks whose intensity fell with increasing T. This can be understood using the models presented in Figs. 5.5(d/e) in the following way. The regions where large peak heights were observed correspond to the situation in Fig. 5.5(d), where the energy levels are well matched. Increasing T caused the peaks to become shorter and wider, which is the expected behaviour for transport through the ground state.[316] Looking now at the suppressed peaks at $T = 275$ mK, these occurred in the region

corresponding to the situation in Fig. 5.5(e). No current could pass through the device at $V_{sd}^{dc} = 0$ because the dot levels were misaligned. However, increasing T effectively widens the V_{sd}^{dc} bias window. This facilitated temperature activated transport through the system, and produced a non-zero I_d. Similar to the SDBS data, the I_d peak height was modulated by a background signal highlighted by the black dashed line. It consisted of broad I_d peaks that align with the vertices for the large diamonds in Fig. 5.5(b). This strongly suggests that the background signal represents the resonances of the smaller quantum dot.

The SDBS data facilitated an estimation of the capacitance C_{dot}, addition energy ΔE_a, and length L of both dots. I start with the larger dot, which gave rise to the smaller diamonds. The varying size of these diamonds is due to orbital effects from the degenerate energy levels.[76] In general, the addition energy $\Delta E_a = \frac{e^2}{C_{dot}} + \Delta E_{0\mathrm{D}}$. The capacitive contribution $\frac{e^2}{C_{dot}}$ related to Coulomb blockade is always present due to the repulsive potential of electrons already in the dot. Conversely, the spacing between 0D energy levels $\Delta E_{0\mathrm{D}}$ is only included when the added electron must also start filling the next 0D level. To obtain C_{dot} we looked at smaller diamonds, which were likely to involve adding electrons at a constant 0D energy level $E_{0\mathrm{D}}$. Here, the addition energy is simply $\Delta E_a = e^2/C_{dot}$. The addition energy is related to the spacing between resonance peaks ΔV_{BG} by $\Delta E_a = \alpha e \Delta V_{BG}$ where the 'lever arm' $\alpha = C_{BG}/C_{dot}$ scales the gate-dot coupling. Obtaining a measured value of α is done using the ratio between the V_{sd}^{dc} and V_{BG} required to overcome Coulomb blockade $\alpha = \Delta V_{sd}^{dc}/\Delta V_{BG}$. This can be read directly from SDBS, illustrated in Fig. 5.5(b).[63,76,316]

Taking an average ΔV_{BG} and ΔV_{sd}^{dc} from the smallest diamonds gave $\alpha = 0.37$, $\Delta E_a = 1$ meV and $C_{dot} = 0.16$ fF. Dot length L was obtained from the coupling between the gate and the dot using $\alpha = C_{BG}/C_{dot}$ and a cylinder on a plane model $C_{BG} = \frac{2\pi\epsilon_r\epsilon_0 L}{\cosh^{-1}(1+t/\varrho)}$.[318,319] Solving for L with effective dielectric constant $\epsilon_r = 4.2$ and thickness $t = 110$ nm of the SiO_2/HfO_2 dual layer and nanowire radius $\varrho = 25$ nm gave a dot length $L \sim 600$ nm. The same was done for the smaller dot using the single diamond defined by the dashed lines in Fig. 5.5(b). For this we found $\alpha = 0.05$, $\Delta E_a = 4$ meV, $C_{dot} = 0.02$ fF and dot length $L \sim 30$ nm.

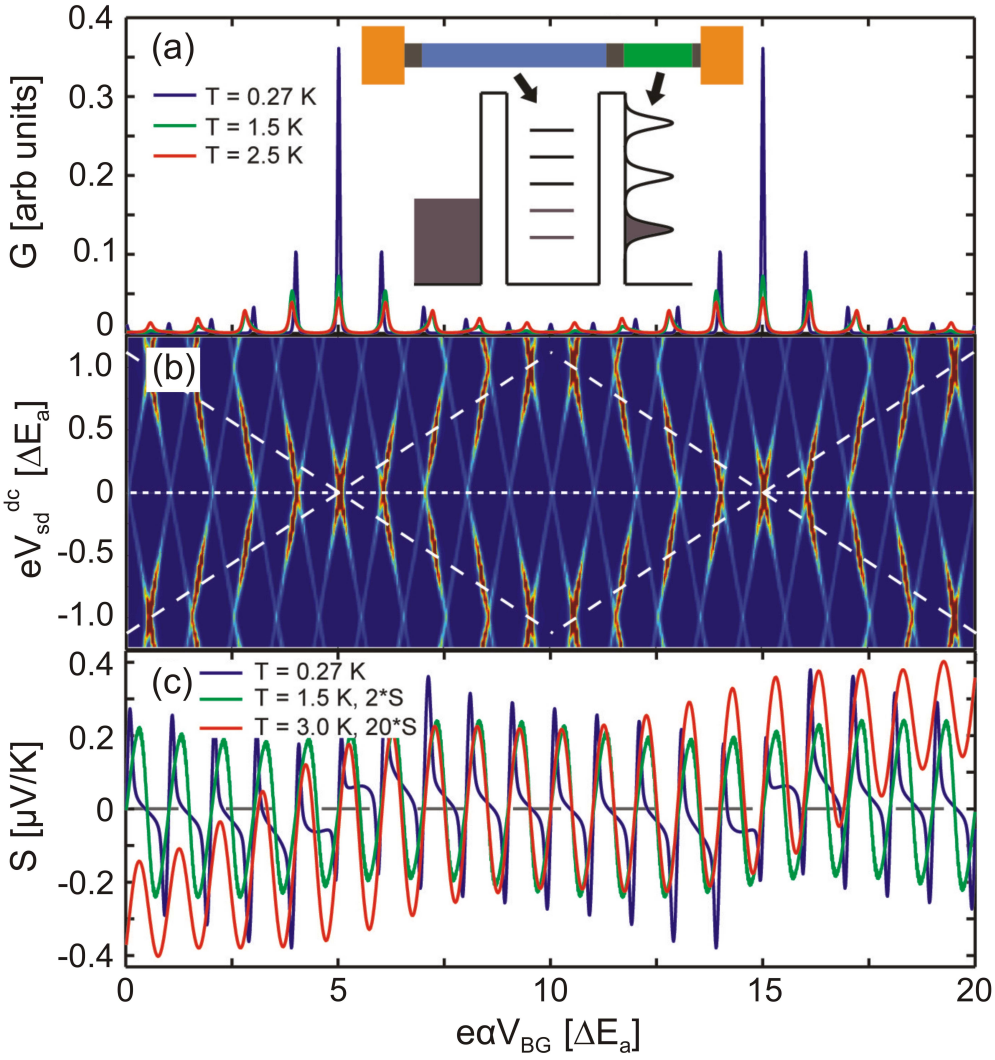

FIGURE 5.6: Theoretical simulations of (a) $G = I_d/V_{sd}^{ac}$ at $T = 0.27, 1.5$ and 2.5 K, (b) SDBS with differential conductance on the colour axis where blue (red) is low (high) $\partial I_d/\partial V_{sd}^{ac}$, and (c) Seebeck coefficient $S = -V_T/\Delta T$ at average $T = 0.27, 1.5$ and 3 K. The voltages were scaled by electron charge e and lever arm α to be in units of addition energy ΔE_a. The model consisted of a nanowire containing two serially coupled quantum dots, shown in the inset to (a). The small dot has a stronger lead coupling, which was included in the description of the lead for the purposes of the simulation. This simple model reproduced the major features of the data in Fig. 5.5. Simulations were done by Martin Leijnse.

However, there is considerable uncertainty in the values for the smaller dot due to the determination of α from the slope of the dashed lines. The uncertainty arises both from possible error in the placement of the lines and the limited measurement range where quantum dot-like states were observed.

To confirm the double-dot interpretation, theoretical simulations were carried out by Martin Leijnse (Lund University) using the Landauer-Büttiker formula to calculate the conductance G through the system. The data is shown in Fig. 5.6, with full details on the method given in Ref. 30 and the supporting information for that paper. Briefly, the model consisted of two serially coupled quantum dots of different sizes. An equal energy level spacing was used within each dot; these spacings differed between the two dots according to their differing size. The data in Fig. 5.5 also suggested that the smaller dot had a strong coupling to the adjacent lead. The rationale for this is that the effect of increased coupling to the leads is a broadening of the energy levels within the dot.[63] The broad nature of the I_d resonances associated with the small dot therefore strongly suggest a strong lead coupling for this dot. In Figs 5.5(d/e) the strong coupling was illustrated by the thin barrier between the small dot and the adjacent lead. To keep the theoretical calculation simple, the small dot was included as a modification to the drain lead. The inset of Fig. 5.6(a) shows this resulted in a drain lead consisting of broad energy levels. This encapsulates the same physics as a dot that strongly couples to the leads. The modelling reproduced all the major features outlined in the data, including the superimposed backgrounds on the I_d vs V_{BG} and SDBS data. The simulations were also used to calculate the Seebeck coefficient $S = -V_T/\Delta T$ and provide insight into our thermovoltage measurements, which I turn to now.

5.4 Understanding the thermovoltage signal

The V_T vs V_{BG} signal in Fig. 5.5(c) consists of a series of resonances produced in response to the changing energy levels within the quantum dot system.[179–181,183,185] In a quantum dot, the relative contributions of sequential tunnelling and higher order processes determines the V_T lineshape (recall Fig. 1.24). Sequential tunnelling typically dominates at higher T, producing a continuous, sawtooth dependence of V_T on V_G.[179,181] As T is lowered, higher order tunnelling processes begin to dominate, driving a transition towards a lineshape proportional to the derivative

of conductance, $V_T \sim \frac{1}{G}\frac{\partial G}{\partial V_G}$.[180,183,185] These consist of single, discrete V_T oscillations around $V_T = 0$ that correspond to the V_G position of I_d resonances. The derivative-like lineshape dominated the $V_H = 20$ mV trace in Fig. 5.5(c). It consisted of sharp oscillations, the zeros of which align with the peaks of I_d resonances in in Fig. 5.5(a). This behaviour is most clear around, e.g., $V_{BG} = 0.83 - 0.86$ V. The lineshape of the oscillations changes as increased $V_H = 60, 100$ mV raises the average device temperature. At higher V_H, V_T varies more smoothly with V_{BG} and takes on the sawtooth lineshape expected at higher T.[181,320]

A second consequence of the higher V_H and associated average T increase was that V_T developed a slowly varying vertical offset. At $V_H = 100$ mV in particular, V_T oscillations in some regions were either entirely positive or entirely negative. Rather than oscillating about $V_T = 0$, V_T oscillated approximately about the dashed line in Fig. 5.5(c). The lineshape traced by the dashed line is consistent with the V_T signal for a smaller quantum dot with strong lead coupling. The positive slope zero crossings at $V_G = 0.875$ and 0.945 V line up with the inferred I_d peaks of the smaller dot and the closing of the larger diamonds in Figs 5.5(a) and (b), respectively. The absence of a clearly defined sawtooth can be explained by the stronger lead coupling of the smaller dot washing out the signal, similar to the broad dashed I_d resonances in Fig. 5.5(a). Again, the major features of the data were reproduced in the simulations shown in Fig. 5.6(c). Importantly, the theoretical calculations assumed the same temperature gradient ΔT for all traces. This shows that the V_T behaviour was due to an increase in average temperature rather than an increased temperature gradient. In all, it is apparent that the V_T signal for serially coupled quantum dots is simply the addition of the two signals, as for the conductance and SDBS results.

5.5 Disorder potential at other V_{PE}

I now touch briefly on measurements made at two other V_{PE} settings shown in Fig. 5.7. The I_d data at various V_{PE} in Fig. 5.4 suggested that for positive V_{PE},

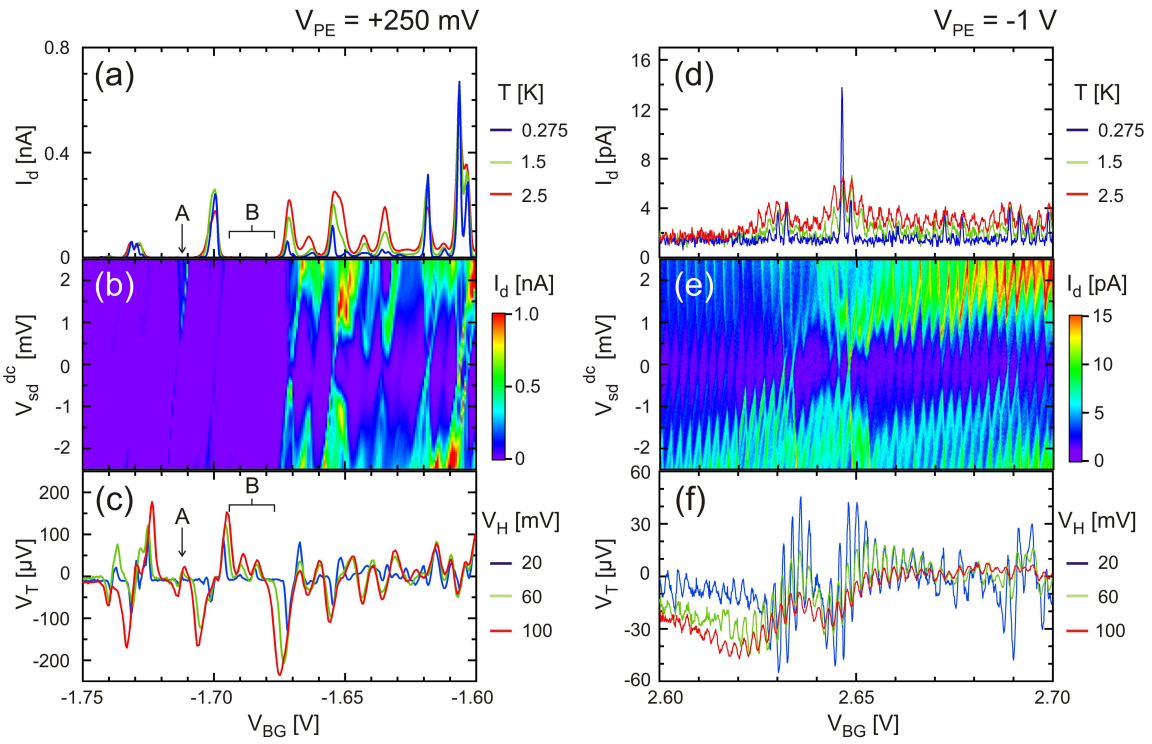

FIGURE 5.7: (a/d) I_d at $T = 0.275, 1.5, 2.5$ K, (b/e) source-drain bias spectroscopy (SDBS) and (c/f) thermovoltage V_T dependence on V_{BG} near pinch-off for (a/b/c) $V_{PE} = 250$ mV and (d/e/f) $V_{PE} = -1$ V. At positive V_{PE} the nanowire consisted of a series of weakly coupled quantum dots. The system at $V_{PE} = -1$ V was similar to that observed at $V_{PE} = -500$ mV, although it is unclear from the data how many dots were present. The markers A and B in (a) and (c) highlight where resonances in V_T did not have a corresponding clear signal in I_d or SDBS data. This encourages further work on V_T as a characterisation tool.

the nanowire was broken into a series of small, weakly defined quantum dots; likely more than two. This is supported by the SDBS and V_T data for $V_{PE} = 250$ mV. The irregularly spaced, overlapping diamonds in Fig. 5.7(b) are consistent with multiple dots in series with poorly defined barriers. Unlike the data for $V_{PE} = -500$ mV, it is not clear how many quantum dots constitute this system. Similarly, the complex V_T oscillations in Fig. 5.7(c) are likely to have arisen from the addition of signatures from multiple quantum dots.[321] The V_T temperature evolution is clearer than it was for $V_{PE} = -500$ mV, due to the increased peak spacing here. At $V_H = 20$ mV, the V_T oscillations follows the derivative of the corresponding I_d resonance in Fig. 5.7(a). With increasing V_H, the V_T lineshape in Fig. 5.7(c) evolves towards a continuous, sawtooth shape as sequential tunnelling dominates

transport.

The data in Fig. 5.7(c) also shows an interesting aspect of using V_T as a characterisation tool. At $V_H = 100$ mV, strong V_T signals emerge that do not have clearly visible corresponding I_d resonances; two examples are at $V_{BG} = -1.71$ V and -1.685 V, indicated by the letters A and B in Figs 5.7(a/c). Crucially, there is no clear signal in the SDBS data around B either. Even so, the presence of a V_T signal shows that a quantum dot level passed through the Fermi level at these V_{BG}. Ordinarily this would result in an I_d resonance. The absence of a resonance suggests that a mis-alignment of the energy levels between multiple dots prevented electrons from traversing the dot. A large V_T signal at low G often arises due to the $\frac{1}{G}$ term in the relationship $V_T \sim \frac{1}{G}\frac{\partial G}{\partial V_G}$.[189] However, it is interesting that the large V_T was prominent at higher temperatures, where the derivative-like line shape may not be applicable.[179,181] A second possibility is that the signals arose because V_T traces the evolution of dot energy level(s).[179,181,183] It is possible that this may occur even if transport was blocked due to a misalignment between consecutive dot energy levels. Unfortunately, from the available data it is only possible to speculate about the source. Nevertheless, the fact that the V_T signal remains clear even when there is no I_d signal or clear SDBS data highlights the potential for thermovoltage as a characterisation technique.[189] Here, V_T has illuminated the presence and evolution of dot energy states that would have gone undetected using only I_d and SDBS. Further work using well controlled double-dot systems would be extremely valuable to properly examine this effect.

Going to more negative V_{PE}, the system at $V_{PE} = -1$ V in Figs 5.7(d-f) resembles that seen with $V_{PE} = -500$ mV. The small diamonds and ΔV_{BG} oscillations in I_d and V_T oscillations arise from a larger dot. This is modulated by the signature of at least one smaller dot. The absence of clear larger diamonds in the SDBS data means it is likely there is more than one smaller dot, but again it is not clear how many are present. The larger dot was approximately 700 nm long, with $\Delta E_a \sim 0.75$ mV and $C_{dot} = 0.07$ fF. A similar period of ΔV_{BG} oscillation and therefore similar dot size was observed at $V_{PE} = -750$ mV also (see Fig. 5.4(e) for I_d data and Ref. 31 for SDBS and V_T). The consistency in the larger dot lengths,

and the similarity of these values to the source/drain contact separation ~ 850 nm suggests that these dots were defined by the barriers generated in the vicinity of the ohmic contacts. The smaller dots at each V_{PE} can be attributed to random surface or bulk impurities that shifted with thermal cycling or large applied V_{BG}. The disorder-induced quantum dots produced the strongest signatures when V_{BG} was swept to positive voltages. The positive back-gate potential would have induced an electron density close to the nanowire surface like that in Fig. 1.21(d). The fact that the influence of disorder was strongest when the electron density was closest to the surface supports previous suggestions that surface impurities are the dominant source of disorder in these devices.[241,322]

5.6 Discussion

In terms of thermoelectrics, there are two areas of significance for these measurements. Firstly, Fig. 5.5(c) confirms that the PE gate is compatible with thermoelectrics; the V_T signal took the expected form and had a magnitude on the same order as previous work on quantum dots in nanowires under similar heating powers.[171,180] This ensures the compatibility of PEO for applications involving tuning the disorder potential and setting base-line charge density for thermoelectric power factor enhancement. Secondly, the pronounced background signal in V_T was much clearer than the background in conductance, providing stronger evidence for the existence of a double-dot system. Thermovoltage is related to the average energy of carriers in the system, and therefore often carries more information than the conductance alone. In principle the amplitude of the Seebeck coefficient in quantum dots gives a measure of charging energy ΔE_a and capacitance C_{dot}.[179,181] Therefore it may be possible to fully characterise quantum dot systems using the Seebeck coefficient $S = -V_T/\Delta T$,[320] since C_G, and thereby dot size can be obtained from I_d resonance spacing $\Delta V_G = e/C_G$. However, higher order tunnelling effects reduce the S amplitude from the theoretical value as the lineshape moves towards the derivative-like form.[180,182,183,185] This introduces difficulties in a reliably determining S.[323] Fully developing a thermovoltage-based characterisation

technique for double quantum dots using a rigorous theoretical understanding of well controlled experimental systems would be an interesting project. Extracting dot energetics from V_T rather than SDBS would be useful for situations where driving the device out of equilibrium with a large electric field would disrupt the system energetics[306] and affect the ability to correctly probe the system. The other advantage is that V_T measurements are significantly less time consuming than SDBS measurements; collecting the data in Fig. 5.5(b) took over 10 hours, while collecting a single V_T trace with the resolution in Fig. 5.5(c) took less than 30 mins. The measurements presented here provide a solid base for expansion of thermovoltage as a measurement technique by showing that the thermovoltage remains the straightforward addition of signatures even for multiple quantum dots with different sizes and lead couplings.

More broadly, the device studied here provided an interesting case study along the thematic lines of this thesis. Firstly, we intended to examine the set-and-freeze functionality of the PE gate dielectric as means to exclude dopant atoms from quantum devices. Indeed, the data in Fig. 5.2 showed that this technique could be used to linearly tune the back-gate operating point as if the same device had different doping densities on different cool-downs. While showing this, we also collected data that illustrated the dominant role that surface and bulk impurity charges play in influencing electron transport through InAs nanowires at low temperature. These charges form a background disorder potential that contributes to nanowires presenting as a series of quantum dots states near V_{po}. The clear, robust quantum dot signatures obtained at many of the V_{PE} settings highlights the important role of impurities in nanoscale devices. Nevertheless, these 'non-ideal' features can be used to understand new physics and work towards possible thermoelectrics applications.

I now turn to quite different work involving PEO-based dielectrics, yet one where I again encountered the importance of surface states in determining device behaviour.

Chapter 6

Results: Protons in poly(ethylene oxide)

6.1 Motivation; a control experiment

Section 4.2.2 presented experiments on PEO/$LiClO_4$-gated NWFETs aimed at ensuring the strong gating effect was due to EDL formation *via* ion transport. This included measuring devices with no gate dielectric, dielectrics with differing salt concentration, devices with differing electrode/NW separation, and devices with a non-local gate architecture where direct field effects were excluded. Data from these experiments showed conclusively that ionic motion was responsible for the effective gating in these NWFETs. Data on the temperature dependence of PE gating in Fig. 5.1 supports this conclusion; device performance dropped dramatically when the ions were immobilised at $T = 220$ K. We did one more experiment not yet mentioned, which was the fabrication of NWFETs featuring patterned PEO dielectrics *without* $LiClO_4$. Fabrication of devices proceeded as usual, except for the exclusion of $LiClO_4$ when mixing the polymer electrolyte solution. The same electron beam parameters were used to pattern the dielectrics – e.g., accelerating voltage, electron dose – since the morphology/dimensions of

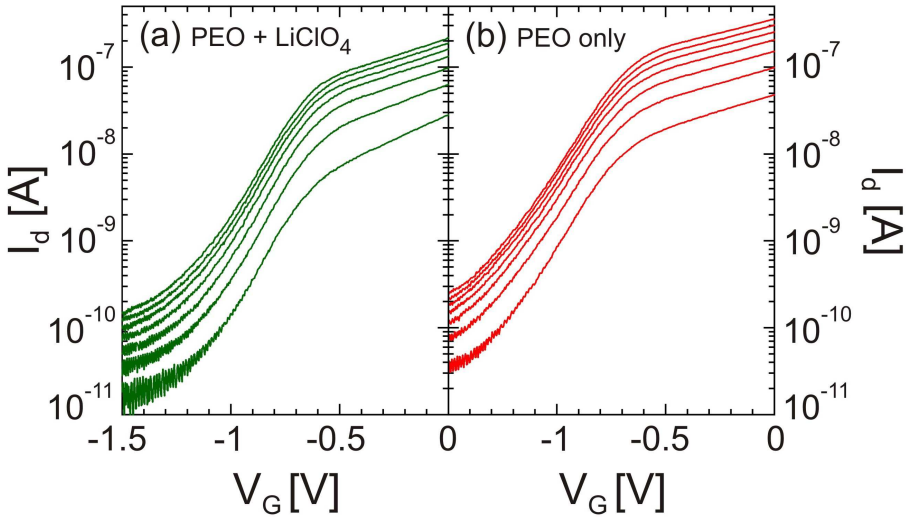

FIGURE 6.1: Transfer characteristics for InAs transistors featuring patterned PEO dielectrics (a) with and (b) without $LiClO_4$. Traces are for $V_{sd} = 1-7$ mV from bottom to top. The characteristics are almost identical; the difference in overall I_d is within device to device variation.

patterned dielectrics without Li was comparable to those with a polymer:salt ratio of 10:1. Without ions to facilitate EDL formation, device behaviour was expected to resemble that of devices without dielectrics (Fig. 4.12(a) in Sec. 4.2.2), or devices when the ionic motion was frozen out at $T = 220$ K (Fig. 5.1 in Sec. 5.1). By contrast, experiments showed that the performance of undoped PEO dielectrics was comparable to the performance of devices with $LiClO_4$. The data in Fig. 6.1 highlights this equality. The performance of both devices is almost identical, despite the dielectric of one device not containing the Li^+/ClO_4^- ions that are normally assumed to facilitate such effective gating. Analysis of 16 devices (25 working gates) across 3 separate fabrication batches featuring PEO gates without $LiClO_4$ gave an average subthreshold swing $SS = 321 \pm 50$ mV/dec at source-drain voltage $V_{sd} = 2$ mV in ambient. This is well within experimental error of the value of $SS = 307 \pm 33$ mV/dec given in Sec. 4.2.2 for devices with $LiClO_4$. Naturally, device to device variation produced some differences in e.g. SS, on/off ratio, V_{th}, hysteresis area, etc, between any two randomly chosen devices, but the average SS values show that gate performance was not hampered by removing the $LiClO_4$. Most remarkably, PEO-only dielectrics with a non-local configuration gated the NWFETs. This precluded a direct field effect and gave very strong evidence that

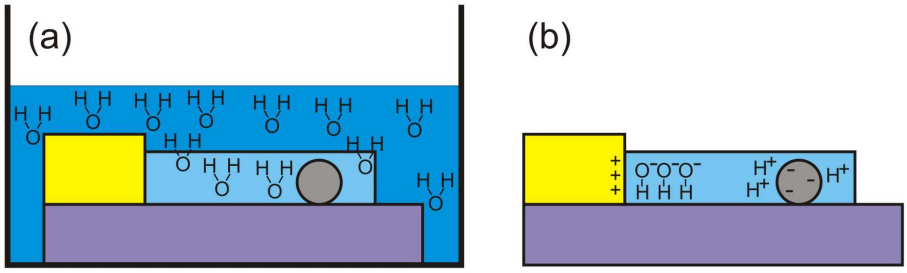

FIGURE 6.2: Illustration of process for H_2O uptake and transport in PEO films. (a) Cross-section of PEO-gated NWFET during development of patterned PEO film, with grey nanowire, light blue PEO film, gold electrode and purple substrate. The PEO film absorbs H_2O molecules.[298] A similar process is likely to occur under hydrated atmospheres. (b) Dissociation and of H_2O and subsequent H^+/OH^- ion transport under a gate bias alters the electron concentration in the nanowire.

a mobile ionic species was present in PEO films without $LiClO_4$ doping.

We postulated that H_2O uptake and subsequent H^+/OH^- transport was the most likely explanation for the data in Fig. 6.1. Patterned PEO films readily adsorb H_2O,[298] and PEO intentionally doped with H^+ exhibits proton conduction.[324–326] There is also small body of evidence for H^+ transport in undoped PEO,[309,325,327,328] with transport arising from the same polymer chain relaxation process as for polymer electrolytes.[327–329] These studies suggest native H^+ conductivity in PEO on the order of $\sigma = 10^{-10} - 10^{-9}$ S/cm.[309,325,327] This is low compared to Li^+ conductivity in PEO at room temperature, $\sigma = 10^{-7} - 10^{-6}$ S/cm.[303,309–311,330] In our case, the PEO films were exposed to H_2O during development, and could also have adsorbed H_2O directly from the atmosphere during measurement (see Fig. 6.2). The departure from previous work is that the equality of transistor characteristics here suggests an equality of ionic conductivity for PEO films with and without $LiClO_4$ doping. Through the rest of the chapter I focus on reconciling the results presented here with previous work on H^+ transport in PEO. We suggest that H_2O exposure produced PEO-based polymer electrolytes with an ionic conductivity that matches that of salt-doped PEO-based polymer electrolytes. We then used this feature to develop devices and prototype circuits featuring proton-gated NWFETs that could be used in a platform for biological interfacing.

Before undertaking this investigation there was an obvious question: Is the high conductivity of undoped PEO films due to Li contamination during processing? This was answered by measuring the Li content of representative PEO films using laser ablation inductively coupled plasma mass spectrometry (ICPMS). The ICPMS was performed by Helen Rutlidge at the Mark Wainwright Analytical Centre at UNSW. Laser ablation causes fine particles to be expelled from the surface, which are swept into the analysis chamber. A plasma ionises the particles, whose mass and concentration can be analysed by the mass spectrometer. For this measurement I fabricated two sets of representative films spun onto Si substrates. The films were unpatterned as ICPMS required larger coverage to make an accurate determination. The results gave 2580 μg/g Li for the intentionally Li-doped film and 12.6 μg/g Li for the film without PEO. The limit of detection was 1.4 μg/g. The Li concentration differed significantly; by a factor of over 200. Looking at previous literature, such a large difference means that contamination cannot explain the electrical behaviour. The ICPMS results show the undoped films have an effective PEO:$LiClO_4$ ratio of 2000:1. Even films with ratio of 100:1 have previously been observed to have four orders of magnitude lower ionic conductivity compared to films with a 10:1 ratio[309] and reducing ion concentration significantly reduces dielectric capacitance.[308] This makes it extremely unlikely that Li contamination can explain the equality of transistor characteristics in Fig. 6.1, and the results that I present throughout the rest of the Chapter.

6.2 Dependence on H_2O concentration

Our hypothesis was that H_2O adsorption essentially dopes PEO films with H^+/OH^- ions. In this case, additional H_2O adsorption should increase the ionic concentration in the PEO and improve the ionic conductivity. This in turn should result in more effective EDL formation and improved transistor action. To examine this, we studied the hydration dependence of PEO-gated NWFETs using the humidity controlled measurement chamber outlined in Sec. 2.4.5. The measurements were

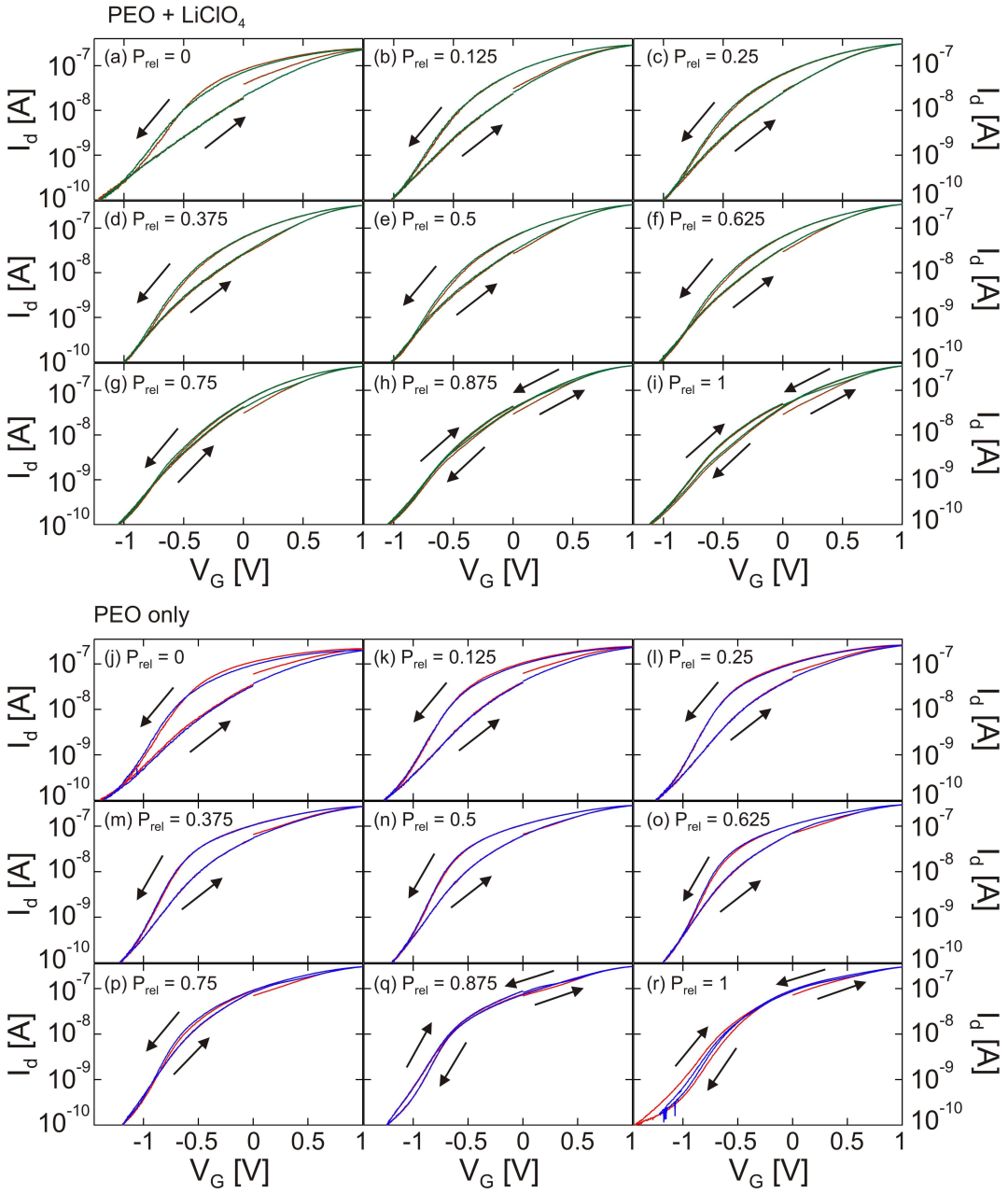

FIGURE 6.3: Hydration dependent transfer characteristics for PEO-gated InAs NWFETs (a-i) with and (j-r) without $LiClO_4$ doping. Two consecutive traces were taken at $V_{sd} = 2$ mV (green/brown for doped PEO, red/blue for undoped PEO). Water vapour pressure was increased from $P = 0$ to 24 mbar in 3 mbar increments, increasing relative vapour pressure P_{rel} from 0 to 1. Added H_2O was adsorbed into the PEO dielectric, increasing on current I_{on}, reducing hysteresis and altering the subthreshold swing SS and threshold voltage V_{th} (see text).

done at the University of Queensland by myself and Bernard Mostert, who constructed the specialised system. Each panel in Fig. 6.3 shows two consecutive I_d vs V_G traces for one device (a-i) with and (j-r) another without $LiClO_4$. Note these are not the same devices as those used for Fig. 6.1.

To obtain the data in Fig. 6.3, the following methodology was used:

1. The vacuum chamber was pumped overnight using a rotary pump prior to obtaining the data in Fig. 6.3(a/j) at $P = 0$ mbar, which we defined as $P < 0.1$ mbar on the 50 mbar gauge.

2. Water vapour was introduced by opening the bleed valve between the vacuum chamber and a reservoir containing the degassed, deionised water until the desired P was reached.

3. The PEO was allowed to fully absorb the additional water and come to equilibrium. This typically took $20 - 30$ minutes and was judged by monitoring the evolution of I_d during that time.

4. Electrical measurements in Fig. 6.3 were done with $V_{sd} = 2$ mV and V_G incremented at 5 mV/s. V_G ran from 0 V to 1 V and then towards negative voltages until I_d dropped to 0.1 nA before finally returning to $V_G = 0$ V. The arrows show the direction of each trace. The sweep was stopped at $I_d = 0.1$ nA to avoid the complex figure-of-eight hysteresis seen in PEO gated devices when swept to their full off state (see Fig. 4.10(d) in Sec. 4.2.2).

Steps 2 - 4 were repeated, incrementing P by 3 mbar each time until saturation pressure $P_{sat} = 24$ mbar was reached. The presented relative pressure values are normalised to the saturation pressure, $P_{rel} = P/P_{sat}$.

As P increases, there are clear changes in four of the transistor properties: subthreshold swing SS, the threshold voltage V_{th}, on current I_{on} and, the hysteresis loop area. To properly examine the changes in transistor performance, and the underlying trends in ionic transport I present extracted values for the four transistor parameters in Fig. 6.4. The common scales for y-axes in the left and right

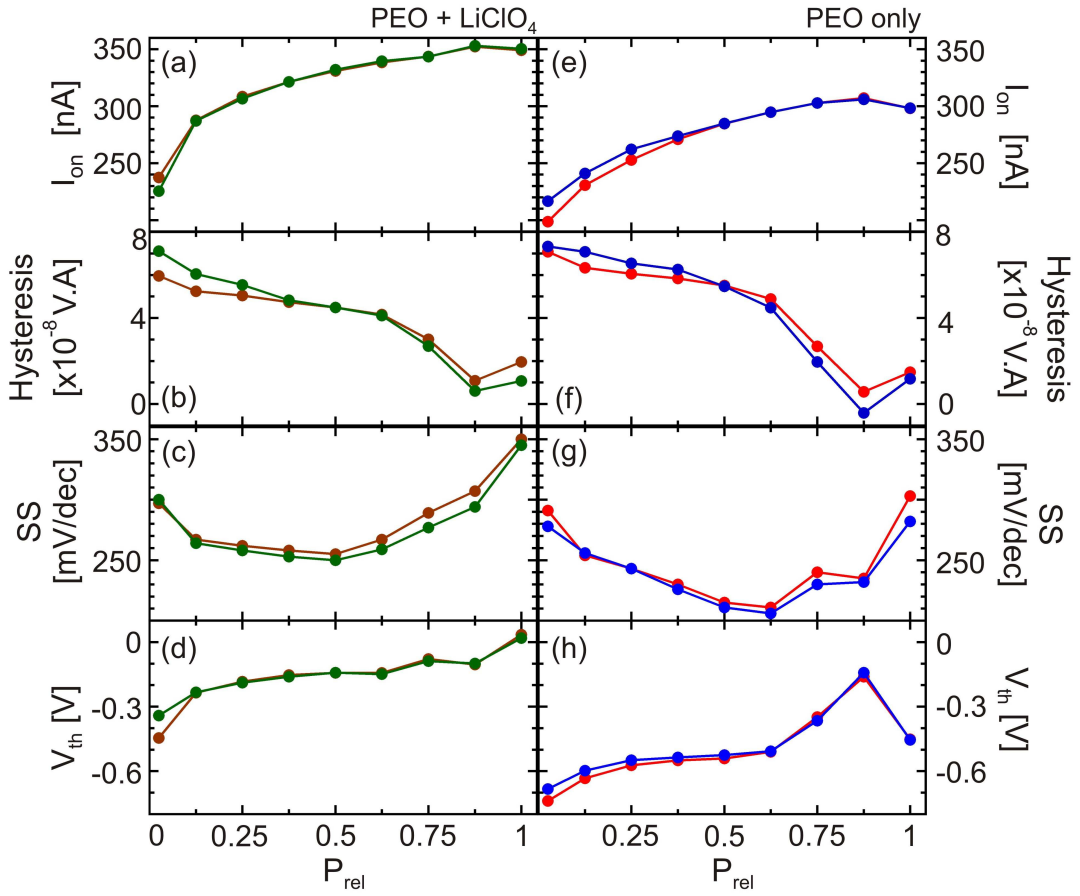

FIGURE 6.4: Extracted transistor characteristics from each of the traces in Fig. 6.3. The colour corresponds to the colour of the trace in Fig. 6.3. Increasing P_{rel} donated H^+/OH^- to PEO films, altering (a/e) on current, I_{on}, (b/f) hysteresis loop area, (c/g) subthreshold swing SS and (d/h) threshold voltage V_{th} according to discussion in the text. The data at $P_{rel} = 1$ tends to counter the trends up to that point. This is likely due to a thin layer of condensed water forming on the surface at saturation vapour pressure affecting device operation.

columns indicates that the transistor properties for both devices fall within a similar range. This confirms the equality of transistor behaviour seen in Fig. 6.3. V_{th} differed most between these two devices, reflective of a large V_{th} variation across all devices; a range of up to 0.5 V was generally observed even within fabrication batches. A relatively large V_{th} variation occurs for metal/oxide wrap gated InAs nanowires also.[145]

Looking first at $I_{on} = I_d(V_G = 1\text{ V})$ in Figs 6.4(a/e)), Sweeping V_G positive caused migration of positive ions to the NW/PEO interface, increasing the electron density within the nanowire and thereby I_d. This process is limited by the ionic

concentration since the electron density is set by the number of ions at the semiconductor/PEO interface. The increase in I_{on} with increasing P for both devices is therefore consistent with increased H^+/OH^- concentration due to water adsorption. The V_{th} response to increased hydration (Figs 6.4(d/h)) is also consistent with higher ionic concentration. V_{th} tended to less negative values at higher P_{rel} as less charge on V_G was required to produce the same H^+ density at the PEO/NW interface. This resulted in I_d turning off at lower V_G.

Similarly, the hysteresis in I_d vs V_G is an indicator of ionic mobility in the PEO (Figs 6.4(b/f)). This is because the time taken to establish the EDL is dependent on ionic mobility. The hysteresis loop area falls with increasing P_{rel}, suggesting a corresponding improvement in ionic mobility. However, using hysteresis to gain quantitative information about conductivity/mobility is problematic due to the contribution to the hysteresis from charge trapping at the InAs surface.[22,23,28,331] The charge trap dynamics depend on the chemistry of the insulator/semiconductor interface and therefore tend to vary for different insulator/semiconductor combinations. Since little is known about the InAs/PEO interface, accurate quantitative information about H^+/OH^- mobility cannot be drawn from these measurements. Nevertheless, we determined the ionic conductivity using time dependent relaxation/pulsing measurements discussed in the next section.

The SS response to PEO hydration was more complicated. For low $P_{rel} < 0.5$, SS decreased, consistent with the notion that increased ion concentration improves gate efficiency. For $P_{rel} \geqslant 0.5$, SS increased, implying less effective gating. This opposes the trends in the three other device parameters; an increase in I_{on} and decrease in V_{th} and hysteresis are all indicators of improved device performance, likely due to added H_2O. One possible cause of the increased SS is surface state occupation; high surface state charge density is a common source of SS degradation.[1,4] This could arise in two possible ways. Firstly, H_2O adsorbed on the nanowire surface may directly induce a higher surface state density. I suggest this is *not* the case for InAs devices, as this process should increase hysteresis with increasing P_{rel}; the opposite is observed. Secondly, the increased surface charge density could be induced indirectly. The increased ionic density at the NW/PEO

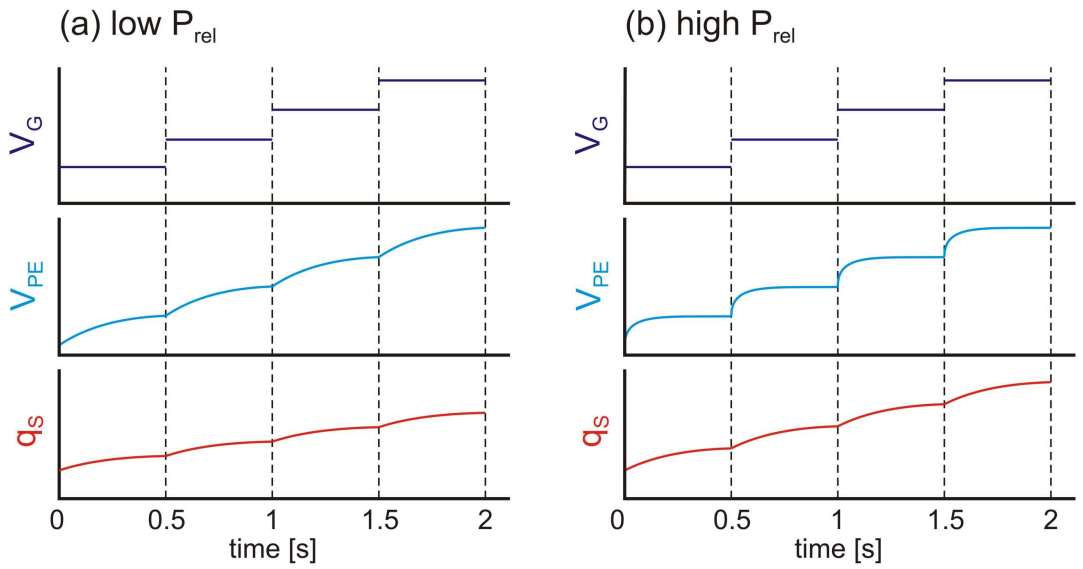

FIGURE 6.5: Illustration of how the measurement protocol affects surface charge q_S at each V_G for (a) low P_{rel} and (b) high P_{rel}. Measurements were taken every 0.5 s, before V_G was incremented by 2.5 mV. In (a), the slow ionic response limits the amount of surface charge filling. In (b), the higher ionic conductivity gives a faster V_{PE} response. This means surface states have longer to fill at a higher V_{PE}. This increases the surface charge present at each measurement point.

interface may increase the surface state occupation at each measurement point. To understand this, consider the measurement protocol outlined in Fig. 6.5. Each measurement consisted of incrementing V_G by 2.5 mV, waiting 0.5 s, then collecting I_d before incrementing V_G by another 2.5 mV. During this 0.5 s waiting time, the voltage V_{PE} at the NW/PEO interface builds up as the ions are transferred to the interface. At low P_{rel}, this occurs slowly, and takes most of the 0.5 s wait time. At high P_{rel}, V_{PE} is established quickly and is stable for most of the 0.5 s wait. Data presented in the next section confirms this. Meanwhile, the amount of charge trapped in surface states is dependent on V_{PE}; higher V_{PE} induces a higher surface charge q_S. Since surface state filling is a time limited process, holding a particular V_{PE} for a longer time also increases q_S as surface states continue to slowly fill at constant V_{PE}. In all, holding a higher V_{PE} for a longer time results in a higher q_S. Looking at the high P_{rel} case in Fig. 6.5(b), V_{PE} spends longer at higher values during each measurement cycle than in the low P_{rel} case (Fig. 6.5(a)). This means a higher surface charge will be induced at higher P_{rel}. A higher surface charge gives a higher surface state capacitance, which in turn degrades SS.[2]

This process would explain why hysteresis continued to improve for $P_{rel} > 0.5$ while SS degraded. A higher ionic conductivity reduced EDL formation time, and thereby hysteresis, but caused more charge to be trapped in surface states, thereby increasing SS.

The above discussion highlights how the differing temporal dynamics of surface states and ionic migration in these devices can generate complex behaviour for the gate sweeps. The competing dynamics of these two influences also resulted in the complex figure-of-eight hysteresis observed for PE-gated NWFETs when swept to more negative voltages (Fig. 4.10(d) in Sec. 4.2.2). The next section presents results from transient measurements which illuminate and to some extent separate the effects of surface states and ionic transport. These measurements also allowed determination of the ionic conductivity.

6.3 Transient behaviour and ionic conductivity

The dependence on P_{rel} of I_{on}, V_{th} and hysteresis loop area suggested that that ion concentration n and mobility μ improved with added water content. Thus the conductivity $\sigma = qn\mu$ should also improve. An accurate determination of σ is a vital part of understanding ion dynamics. It is also important for dielectric applications since σ determines how fast the transistor can switch between on and off states.[8] To measure σ, we turned to transient measurements. EDL formation *via* ionic motion in a PE can be modelled as a resistor and capacitor in series. The effective resistance R accounts for the resistance experienced by the ions as they set up the double-layer capacitance, C.[8,219] Applying a voltage to the gate electrode causes a time-dependent build-up of the voltage V_{PE} at the NW/PEO interface according to $V_{PE} = V_G e^{-t/\tau_{ion}}$. The time constant $\tau_{ion} = RC$ quantifies how quickly the EDL is established. In the region where I_d is linear in V_{PE}, we have $I_d(t) \sim e^{-t/\tau_{ion}}$. The RC time constant can thus be measured by applying a V_G pulse in the region $V_G > V_{th}$ and observing the I_d response in the nanowire. However, surface states will also influence the transient response, since they also

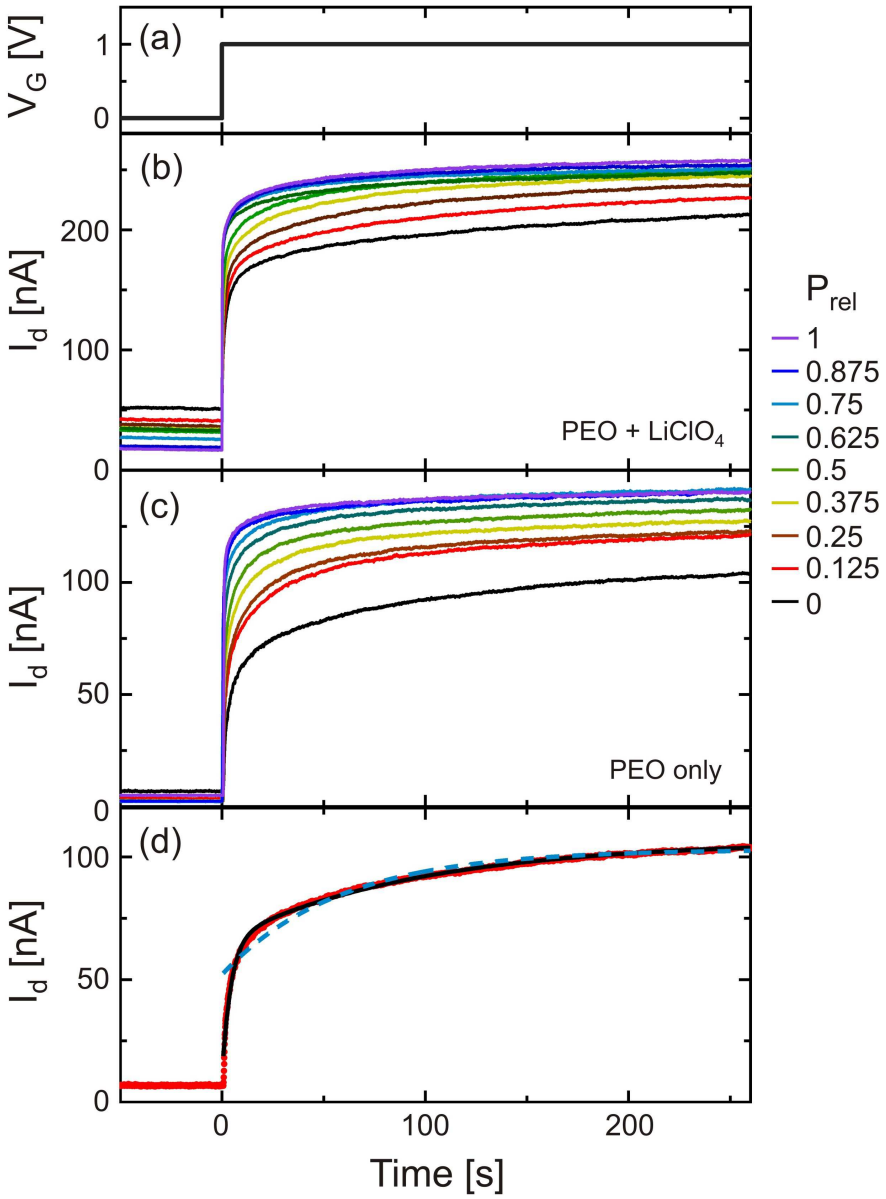

FIGURE 6.6: (a) V_G pulse to measure I_d transient response for devices (b) with and (c) without $LiClO_4$ under increasing P_{rel}. (d) Data (red dots) for the PEO only device at $P_{rel} = 0$ with best fits of $I_d(t) = I_0 + Ae^{-t/\tau_{ion}}$ (blue dotted line) and $I_d(t) = I_0 + Ae^{-t/\tau_{ion}} + Be^{-t/\tau_{SS}}$ (black solid line).

act as an RC circuit with time constant $\tau_{SS} = R_{SS}C_{SS}$[39] that can be as long as 30 mins for InAs nanowires.[331] In this case, the transient will take the form $I_d(t) = I_0 + Ae^{-t/\tau_{ion}} + Be^{-t/\tau_{SS}}$. Finally, a direct field may add some small component to the I_d transient. To eliminate this aspect only devices with a non-local geometry were used for all transient measurements. This ensured that the experiments accurately probed ion/surface dynamics.

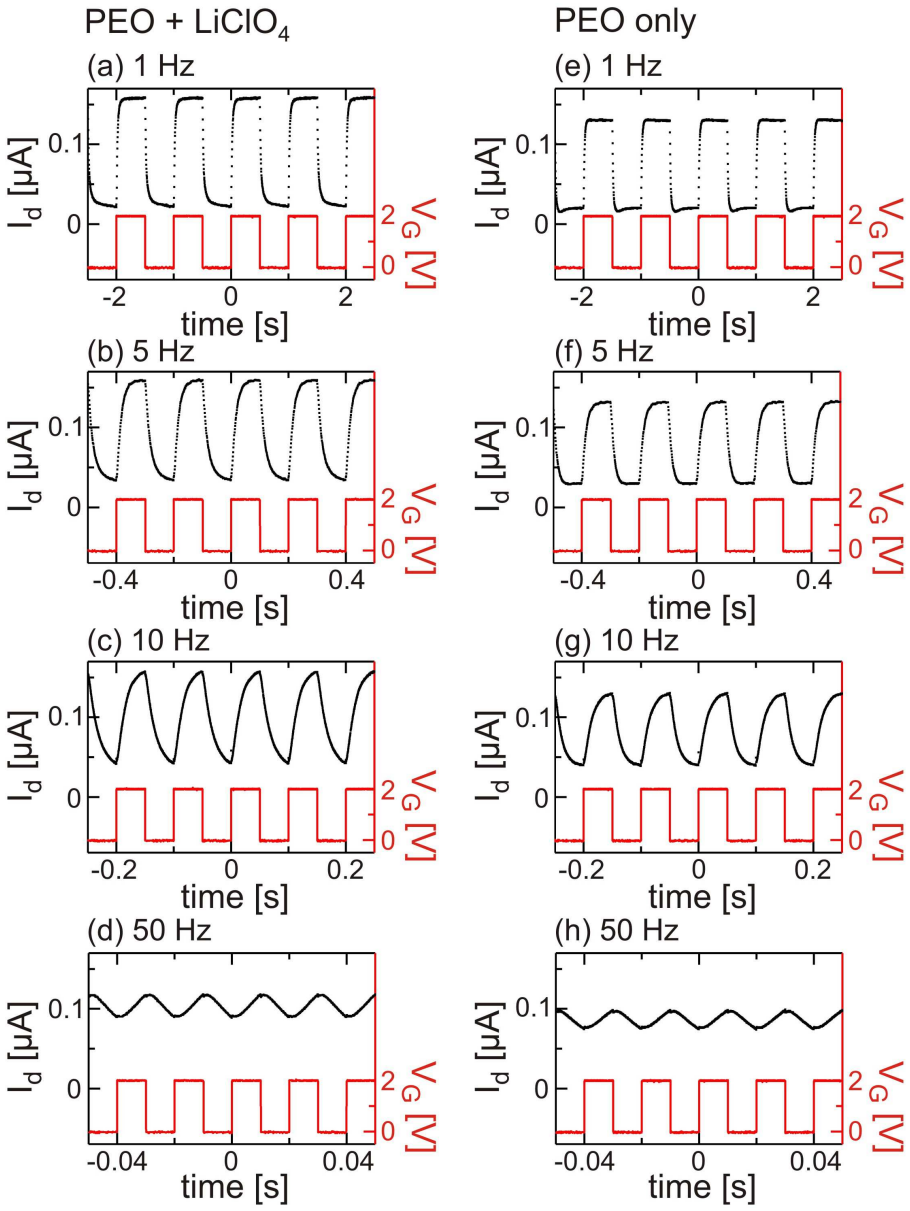

FIGURE 6.7: I_d transient response (black/left axes) to square pulse trains at different frequency f applied to V_G (red/right axes) of devices (a-d) with and (e-h) without $LiClO_4$ at $P_{rel} = 1$. Switching the gate faster than the surface state trapping time results in stable operation. For high $f > 10$ Hz the switching time exceeds the time required for complete EDL formation.

Figure 6.6 shows the result of applying a 1 V pulse to the gate electrodes of NWFETs with non-local PEO dielectrics. Figure 6.6(a) is an illustration of the applied pulse, with the I_d response for devices with and without $LiClO_4$ at each P_{rel} shown in Figs 6.6(b/c). Both devices exhibit a sharp rise in I_d followed by a longer, slow relaxation. The slow response is on the order of seconds and does not saturate even after 4 minutes, as expected if τ_{SS} is on the order of minutes.[331] As

P_{rel} increases, the overall I_d increases, consistent with the data for I_{on} in Figs 6.3 and 6.4. The initial transient response becomes notably faster with increasing P_{rel}, consistent with increased ionic conductivity. Fits were performed for each device at each P_{rel}; an example of the fitted data for the case $P_{rel} = 0$ is shown in Fig. 6.6(d). As expected, the data (red dots) does not fit a simple exponential $I_d(t) = I_0 + \mathrm{A}e^{-t/\tau_{ion}}$ (blue dotted line). The fit of $I_d(t) = I_0 + \mathrm{A}e^{-t/\tau_{ion}} + \mathrm{B}e^{-t/\tau_{SS}}$ (black solid line) follows the data more closely. This makes a strong case for the presence of two time limiting behaviours – i.e. ion migration and surface states. However close inspection reveals that the fit is not as close as one might like to reliably extract σ values. This may be due to the fact that assigning a single τ for each ionic/surface state component is not always appropriate. Surface states in particular tend to consist of numerous different traps each with different trapping time.[39] Most importantly, fitting multiple exponential terms to a single trace with this many free parameters is bound to lead to errors in the extracted values.[332,333]

To improve the accuracy of σ determination we sought to exclude the influence of surface states altogether. This was accomplished by pulsing V_G faster than the typical surface state filling time. In this way V_G would switch before the surface states had time to trap/de-trap charge. We used a function generator to apply square pulse trains to V_G at varying frequency f. I_d was amplified by a Femto current pre-amplifier and monitored on a digital signal oscilloscope (DSO). The DSO was also used to directly monitor the V_G pulse train. The results at $P_{rel} = 1$ are shown in Fig. 6.7. The I_d transient response is much improved; I_d saturates and becomes stable within 0.1 s for positive V_G pulses. The V_G pulses to zero produce a less ideal response, perhaps due to the filling of surface states with a short time constant. By increasing the switching frequency to $f = 5$ Hz, the I_d transients contain only a single exponential contribution due to ionic motion, and I_d saturates once the EDL is established. As f is increased beyond 10 Hz, the time between pulses drops below the time required for complete ion separation across the ~ 4 μm thick dielectric, cutting off the I_d response.

Linearising the data proved the best way to extract σ. The I_d response to pulses of V_G to 1 V follow the relationship $I_d(t) = I_0 + I_{sat}(1 - e^{t/\tau_{ion}})$ where $I_0 = I_d(t = 0)$

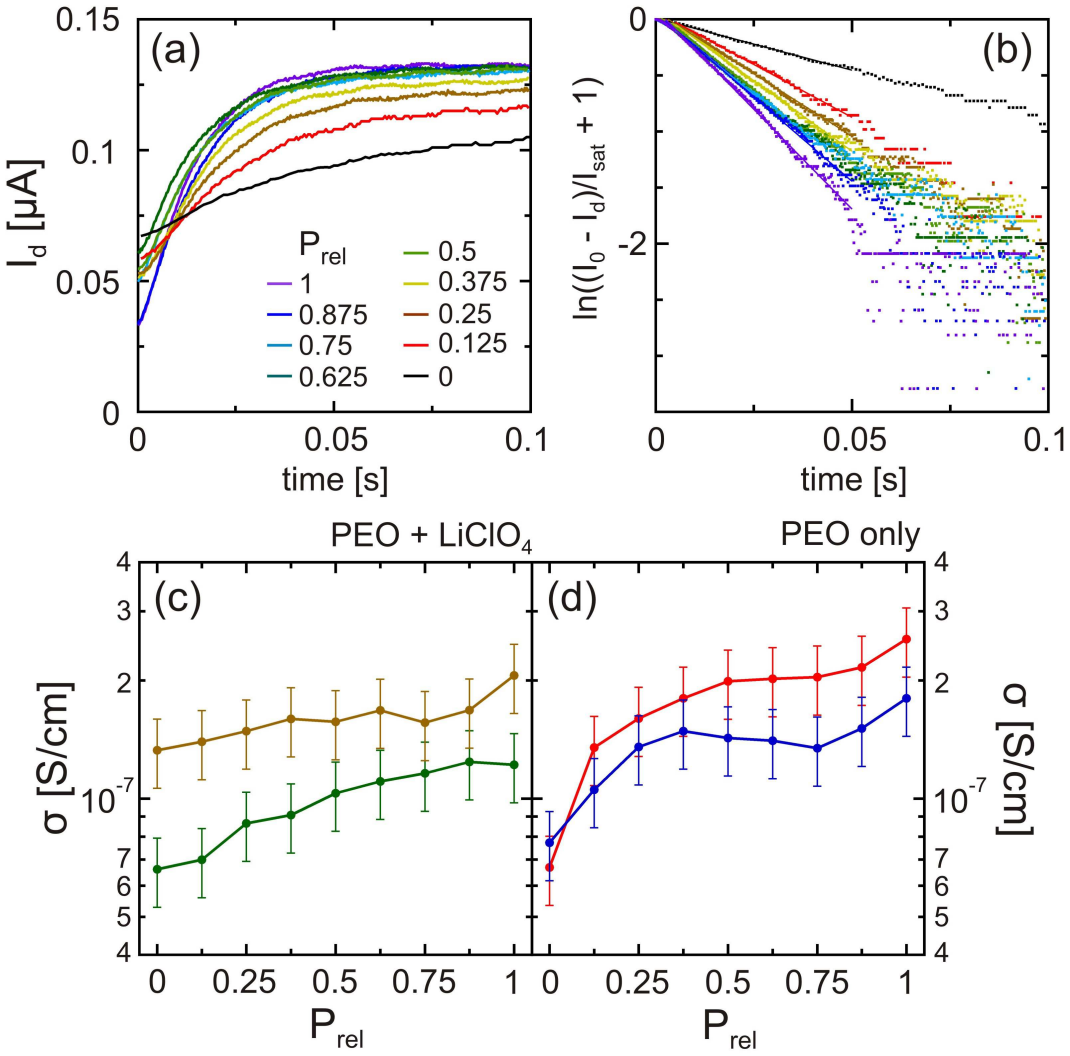

FIGURE 6.8: (a) I_d transient response from 5 Hz data for a PEO-only gated device at each P_{rel}. Transient form is close to an exponential that saturates at long t, but deviates from ideal behaviour around $t = 0$ s when the device switches. (b) Plotting the data (dots) as $\ln(\frac{I_0 - I_d}{I_{sat}} + 1)$ vs time t gives a linear trend with slope of $-1/\tau_{ion}$; a steeper slope indicates a shorter time constant. Only the regions that followed a linear trend were fitted (solid lines). (c/d) Ionic conductivity σ extracted from two devices each with and without $LiClO_4$. The error bars are largely due to uncertainty in device dimensions. The σ extracted from both sets of devices are within device-to-device variation, and match previously reported values for $LiClO_4$ doped PEO. Devices without $LiClO_4$ have a slightly stronger hydration dependence.

and I_d saturates for long t, $I_d \to I_0 + I_{sat}$ (see data in Fig. 6.8(a)). The two constants I_0 and I_{sat} were collected from the data, and linear plots of $\ln(\frac{I_0 - I_d}{I_{sat}} + 1)$ vs t were used to extract the slope $-1/\tau_{ion}$. An example is shown in Fig. 6.8(b). This method was more accurate compared to performing an exponential fit to raw

data as the curves did not always conform to an ideal exponential at the start and end of each pulse. This is likely due to non-ideal behaviour at the point where ions change direction. At long times, I_d saturation and the possible influence of surface states causes deviations from ideal behaviour. Linearising the data made it much clearer where the fit should be performed to obtain the most accurate results. Pulses at 5 Hz were used as they typically provided the best compromise between the desire to exclude surface state influence at long times, but also capture an entire I_d transient response. Once τ_{ion} was given from the linear fits, σ could be calculated by $\tau_{ion} = RC = \frac{l}{\sigma A}C$. The PEO dielectric length l and cross-sectional area A were measured with atomic force microscopy. C is the capacitance of the electrical double layer at the PEO/NW interface, given by the capacitance for concentric cylinders $C = \frac{2\pi\epsilon_r\epsilon_0 L}{ln(1+t/\varrho)}$ [196,219] where ϵ_0 is the permittivity of free space, $\epsilon_r = 10$ and $t = 1$ nm are the dielectric constant and thickness of the EDL, respectively,[8,196,203] L is the length of the nanowire covered by PEO, and ϱ the nanowire radius.

Figures 6.8(c/d) give the extracted σ as a function of P_{rel} for two devices with $LiClO_4$ doped PEO and two devices with undoped PEO dielectrics. The ionic conductivity extracted from both sets of devices is of order $\sigma = 10^{-7}$ S/cm, consistent with previously reported values for $LiClO_4$/PEO polymer electrolyte films at room temperature.[303,309–311,330] This value is much higher than previous measurements of proton conductivity in PEO, $\sigma = 10^{-9} - 10^{-10}$ S/cm.[309,325,327] The question is: What is the difference in our devices? The mobility μ for Li^+ and H^+ in PEO is likely to be very similar, since both species progress by segmental motions of polymer chains.[329] The key to the high H^+ conductivity $\sigma = qn\mu$ is therefore likely to be a high ionic concentration n. There are two aspects that could contribute to the difference between our results and previous work.[309,325,327] First, care was taken in previous work on proton conduction in PEO to actively exclude water during fabrication. Secondly, the parallel plate capacitor geometry typically used to evaluate conductivity has recently been shown to strongly inhibit water uptake in organic materials.[250,251] By contrast, the device was immersed in

H_2O to develop the pattern and the uncovered dielectrics were exposed to a hydrated atmosphere in the measurement chamber. As a result a much increased H^+/OH^- concentration can be expected compared to previous work.

As for the hydration dependence of σ, there was a general trend to higher σ with increasing P_{rel}, which was an expected consequence of water adsorption from the atmosphere. Conductivity extracted from devices without $LiClO_4$ had a slightly stronger hydration dependence than those with Li-doped dielectrics, consistent with Li^+ transport contributing to EDL formation. However, the variation in conductivity is less than an order of magnitude for each device, without a clear, consistent trend. In addition, σ is not zero at vacuum, even when the chamber had been pumped for more than 15 hours. Together these results suggest that the majority of H^+/OH^- carrier were introduced during processing and were not extracted by vacuum. H^+/OH^- incorporation could have been during thin film preparation, or at the development stage. Any additional water adsorption in the measurement chamber likely added only a little to the pre-existing H^+/OH^- concentration. The conclusion is that by simply not attempting to exclude water from fabrication it is possible to produce a PEO polymer electrolytes with the same conductivity as intentionally doped films. This may be useful in cases where the high capacitance of polymer electrolytes is required, but salt doping is undesirable.

An interesting feature of the data in Fig. 6.6 is that I_d increased as surface states filled. This is the opposite of expected behaviour according to the explanation in Sec. 1.3.2 and the data presented in Chapter 3 on AlGaAs/GaAs heterostructures. For an n-type semiconductor channel with surface traps, positive V_G should trap negative charge and compensate the gate voltage. This would give a *reduction* in I_d over time; this is not observed for these InAs surface traps. The behaviour of InAs nanowire surface traps may be due to the high density of states in the conduction band and the related surface Fermi level pinning. The latter causes a surface accumulation layer which means electron transport is expected to take place close to the surface, rather than in the bulk (see Fig. 6.9(a)).[48] The energetic and spatial proximity of surface states to the conduction channel is likely to result in fundamentally different behaviour to surface states in the band gap. For

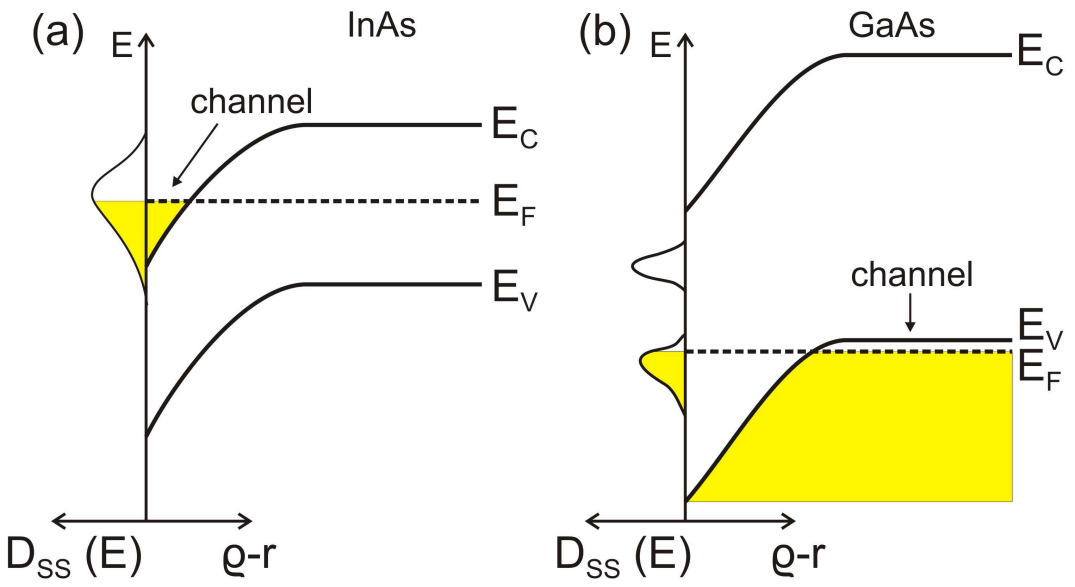

FIGURE 6.9: Surface state density $D_{SS}(E)$ and radial band diagram for (a) InAs and (b) p-doped GaAs nanowires with radius ϱ. The high density of surface states in the conduction band pins the InAs surface Fermi level in the conduction band. This makes undoped InAs nanowires n-type, with a conduction channel at the surface of the nanowire. Charge pulled into InAs surface states may further enhance to conduction. The band-gap surface states in GaAs generate a surface barrier, confining the hole conduction channel to the centre of the nanowire. Charge trapping in GaAs surface states opposes an applied gate voltage.

InAs nanowires, charge pulled into the surface states may in fact be non-localised and contribute to conduction in the surface accumulation layer. Alternatively, de-trapped charge may fall directly into the conduction band and contribute to conduction here. Either situation would result in increasing I_d for positive V_G pulses as observed.

To test this hypothesis, we turned to p-GaAs nanowires, which we expected to possess band-gap surface states and a conduction channel that extends to the centre of the nanowire, away from the surface (see Fig. 6.9(b)). In addition to testing the influence of the GaAs surface on device behaviour, utilising a different nanowire material could give an independent measurement of ionic conductivity σ. Using a p-type channel also gave us scope to investigate the potential use of III-V nanowires as proton-to-electron transducers and the opportunity to explore complementary amplification/inverting applications.

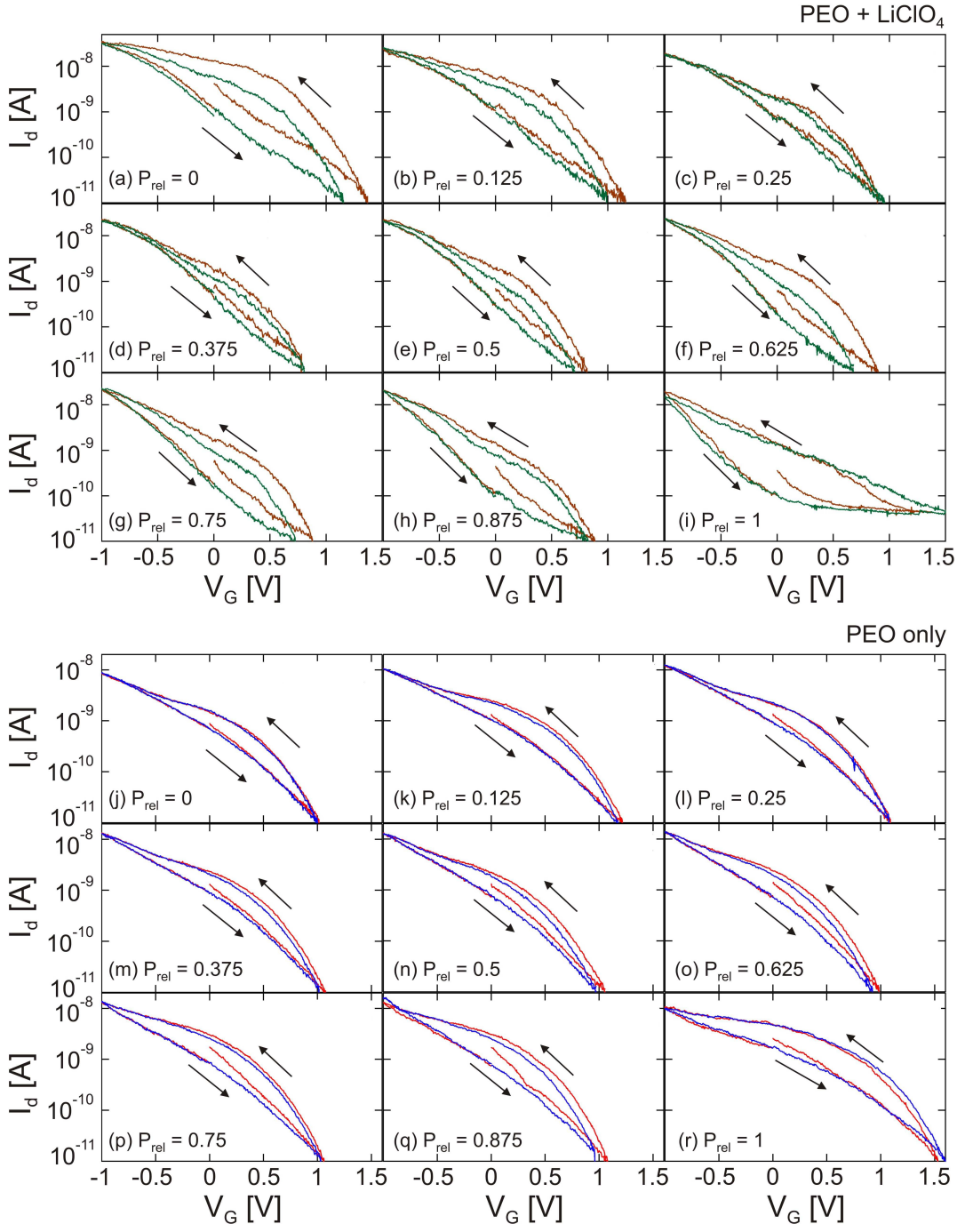

FIGURE 6.10: Hydration dependent transfer characteristics for PEO-gated p-GaAs NWFETs (a-i) with and (j-r) without $LiClO_4$ doping. Two consecutive traces were taken at $V_{sd} = 1$ V. The p-GaAs devices have similar operating range and on/off ratios to the n-InAs devices. The increasing hysteresis at high P_{rel} is likely due to an increased contribution from surface states compared to n-InAs devices.

6.4 Complementary *p*-GaAs devices

The basic performance of *p*-GaAs devices was ascertained by the transfer characteristics shown in Fig. 6.10. The *p*-GaAs devices are well matched to the *n*-InAs devices in terms of V_G operating range ~ 2 V and on/off ratio of $10^3 - 10^4$. The correspondence of these two parameters is essential for complementary switching and amplification applications. The overall current for *p*-GaAs devices is lower because techniques for ohmic contact formation to *p*-type GaAs nanowires are less mature than those for InAs nanowires. This results in high contact resistance and necessitated measuring *p*-GaAs devices with $V_{sd} = 1$ V. Rifat Ullah from our group at UNSW is currently working to improve the linearity and contact resistance of contacts to *p*-GaAs nanowires as part of his research.

The hydration dependence of the *p*-GaAs transfer characteristics was not as strong as for *n*-InAs devices. Hysteresis tended to reduce up to $P_{rel} \sim 0.75$ but rose again towards $P_{rel} = 1$. Additionally, some GaAs devices became very unstable/noisy at $P_{rel} = 1$. Similar instability was not observed for any InAs devices. The difference points to surface effects, possibly related to the formation of a condensed water layer at $P_{rel} = 1$. Water adsorption on the GaAs surface may induce a higher density of surface states that increase hysteresis and instability. Since charge trapping in band-gap surface states directly opposes charge accumulation at the semiconductor/PEO interface, a surface state component would drive larger hysteresis loops against the hysteresis-reducing effect of improved ionic conductivity. This means it was not helpful to draw conclusions from these measurements. Similarly to *n*-InAs devices, transient measurements gave a clearer picture of ion and surface dynamics.

Figure 6.11 shows the outcome of a $V_G = -1$ V pulse to the gate of a *p*-GaAs NWFET featuring PEO dielectrics with and without $LiClO_4$. V_G was pulsed negative rather than positive to induce charge carriers and operate the device in the linear I_d vs V_G region, mirroring the *n*-InAs experiments. In contrast to the InAs devices, I_d falls after the initial step, consistent with the filling of band-gap

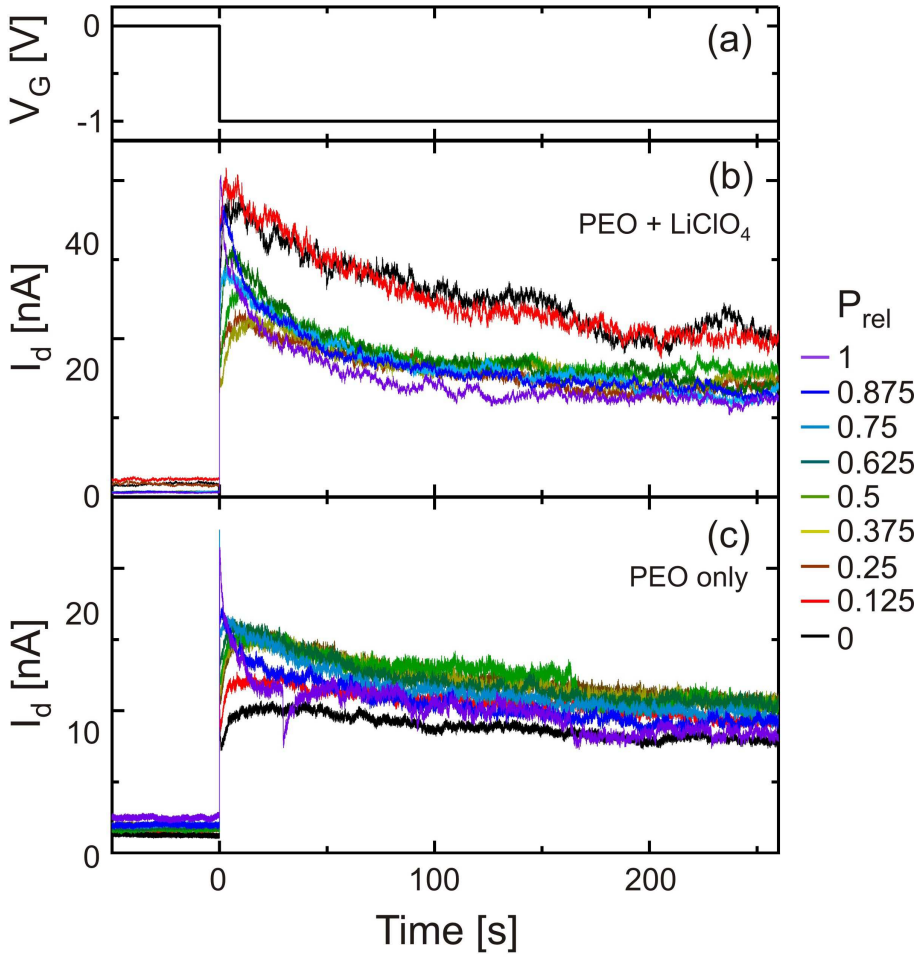

FIGURE 6.11: (a) V_G pulse to measure I_d transient response for p-GaAs devices featuring PEO gates (b) with and (c) without $LiClO_4$ under increasing P_{rel}. Filling of surface states reduces I_d over time. This component depends on P_{rel}, and very quickly suppresses I_d at high $P_{rel} = 0.875, 1$. The noise seems to arise from the devices; Fig. 6.10 also has more noise compared to Fig. 6.3.

surface states compensating the gate voltage. The GaAs surface state response is fast compared to InAs surface states, especially for higher hydrations. This supports the suspicion from the I_d vs V_G data in Fig. 6.10 that as P_{rel} approaches 1, a high density of surface states comes to dominate hysteresis. GaAs devices had much higher noise than InAs NWFETs; this was also seen in the transfer characteristics (Figs 6.3 and 6.10). The noise source was not the measurement set-up or a product of the reduced signal, since GaAs and InAs devices measured in the same I_d range show different noise magnitudes. Rather, it seems specific to GaAs devices and could be due to e.g. spontaneous trapping/de-trapping in surface states.

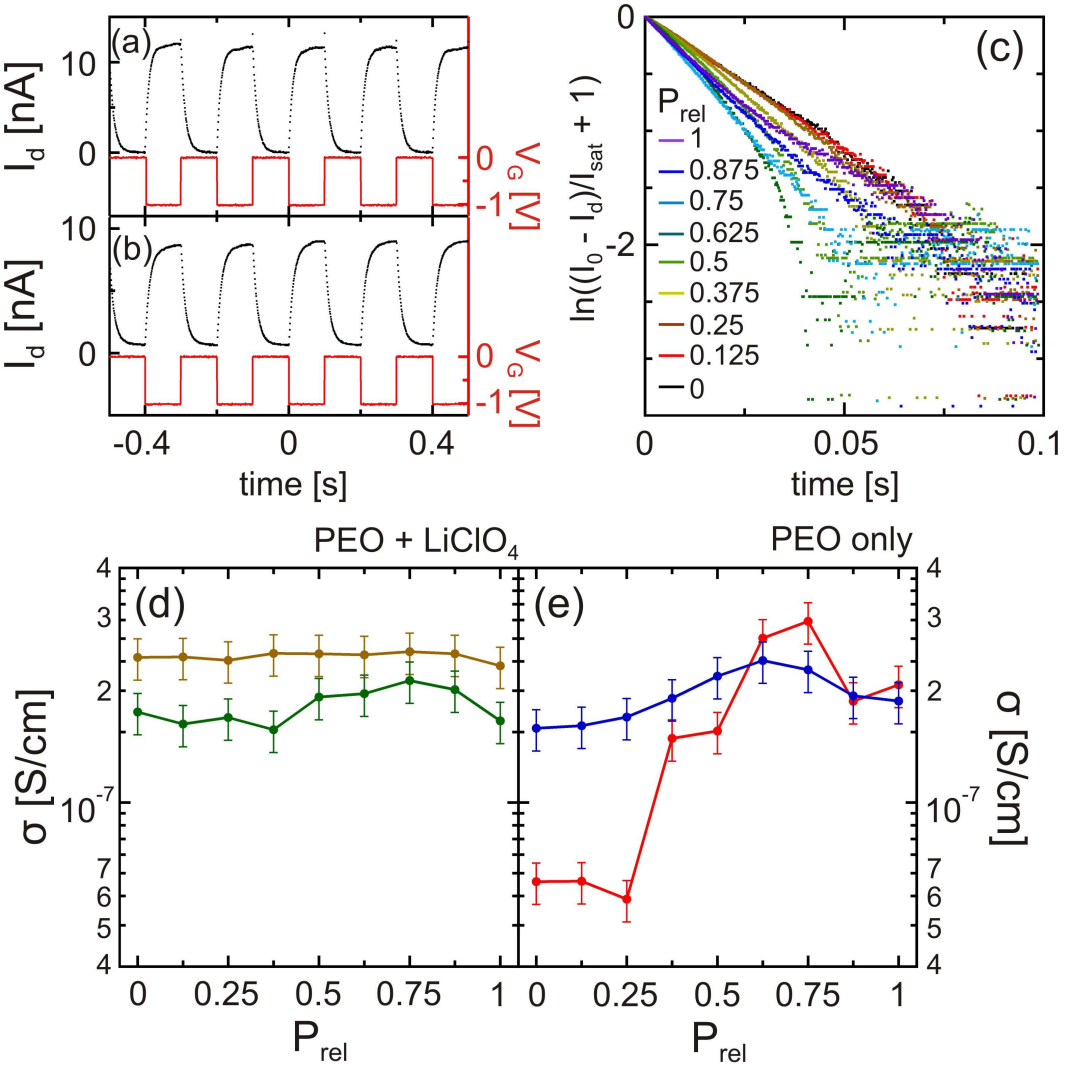

FIGURE 6.12: (a/b) I_d switching (black traces/left axes) in response to a $f = 5$ Hz square pulse train applied to V_G (red traces/right axes) for p-GaAs devices gated by PEO (a) with and (b) without $LiClO_4$ doping at $P_{rel} = 1$. Device stability and noise was greatly improved compared to Fig. 6.11. (c) 5 Hz data from device in (b) at each P_{rel} plotted as $\ln(\frac{I_0 - I_d}{I_{sat}} + 1)$ vs time. Non-linear behaviour at high P_{rel} is likely due to increased surface state influence. (d/e) Ionic conductivity σ extracted from two devices each with and without $LiClO_4$. The error bars are largely due to uncertainty in device dimensions. The extracted σ is on the same order as for n-InAs devices, however the trend is likely to be less accurate due to the stronger surface state influence.

We again applied square pulse trains in an attempt to operate faster than the surface traps; $f = 5$ Hz data is shown in Fig. 6.12(a/b) for dielectrics with and without $LiClO_4$. Stability and noise dramatically improved compared to Figs 6.10 and 6.11. The data was taken at $P_{rel} = 1$, where the greatest instability was observed. This strongly supports the notion that the noise arose due to trapping/de-trapping of

charge in GaAs surface states. Similarly to InAs devices we find that the influence of surface states on device operation can be somewhat mitigated by operating at speeds faster than the trapping/de-trapping times.

The square pulse trains facilitated a second determination of ionic conductivity σ for dielectrics both with and without $LiClO_4$ doping. However, these efforts were hampered by the comparatively fast acting surface states, especially for higher P_{rel}. Figure 6.12(c) shows linearised data from a p-GaAs NWFET featuring a PEO dielectric without $LiClO_4$. At low $P_{rel} < 0.75$, the slope increases with P_{rel} and the trends are largely linear. For $P_{rel} > 0.75$, the data deviates from linear behaviour as rapid filling of surface states suppresses the I_d transient responses. The curved response in this plot means the original data consists of more than one exponential component. Since the band-gap surface states of GaAs act in opposition to the gate voltage, this resulted in an artificial reduction in τ_{ion} and σ for high P_{rel}. This is apparent on the plots of σ vs P_{rel} in Figs 6.12(d/e), where σ is suppressed for $P_{rel} > 0.75$. However, I stress that this is a measurement artefact due to surface states, and not an accurate measurement of σ. Beyond this caveat, the extracted σ values agree with the order of magnitude obtained from InAs devices in Fig. 6.8(c/d). Again, the variation for σ extracted from devices with Li-doped dielectrics is smaller than for those with undoped dielectrics. The low dependence of σ on hydration over all prevents meaningful conclusions about ion dynamics, but supports the conclusion drawn from the n-InAs devices that the majority of the H^+/OH^- ions were introduced during processing.

6.5 Circuit/transducer applications

Underlying the above discussion is the conversion of proton signals to electron signals by PEO-gated n-InAs and p-GaAs devices. As explained in Sec. 1.6.2, proton-to-electron transducers are of great interest for biological interfacing, with a number of organic transistors showing promise towards this. Full-scale integration of biological systems with conventional electronics rests on developing

biological logic gates and signal amplifiers; ideally using complementary n- and p-type transistors. While organic transistors have the advantages of flexibility and channel permeability, they lack integrability with Si-based microelectronics and have poor electron/hole mobilities. A combined organic/inorganic approach using III-V nanowires has distinct advantages, including growth directly on Si substrates,[129–131] n- and p-type materials with high electron/hole mobilities,[22,334] dimensions that are well matched to cells and proteins,[227] and a high surface-to-volume ratio that lends scope for enhanced detection capabilities compared to thin film devices.[232] With this in mind we investigated the switching capabilities of PEO-based proton-gated n-InAs and p-GaAs NWFETs and their use in a basic inverter circuit.

For operation in a switching circuit, transistors are switched between their full on and off states; i.e. pulses are not limited to the linear I_d vs V_G ranges utilised above. Figures 6.3 and 6.10 show both n-InAs and p-GaAs devices switch between I_{on} and I_{off} in the range -1 V $< V_G <$ $+1$ V. To evaluate their performance as switches, voltage pulses between $V_G = \pm 1$ V were applied, presented in Fig. 6.13. To mimic a wet biological environment the chamber was hydrated to a greater extent than usual. This consisted of leaving the bleed valve open for $5 - 10$ mins; far longer than the $\sim 10 - 20$ s required to reach each P_{rel} in the preceding experiments. The long hydration time would have ensured condensation on the device substrate and that the PEO films were completely hydrated. The device response in Fig. 6.13 is similar to that in Figs 6.7 and 6.12, with some notable differences. First, I_d in both devices in Fig. 6.13 drops to $I_{off} \sim 0$ when turned off. Secondly, the transients do not follow a simple exponential because I_d vs V_G is no longer linear in the steady state. At $f = 1$ Hz, the p-GaAs device was very noisy and I_d in the n-InAs device fell after the initial transient, in contrast to the rise in current previously observed. Both effects can likely be attributed to water-induced band-gap surface states. This improved with switching speed, and a stable signal was obtained from both devices up to $f = 50$ Hz.

Finally, we constructed complementary circuits from n-InAs and p-GaAs PEO-gated NWFETs. Figures 6.14(a/b) contain data and the schematic for an inverter

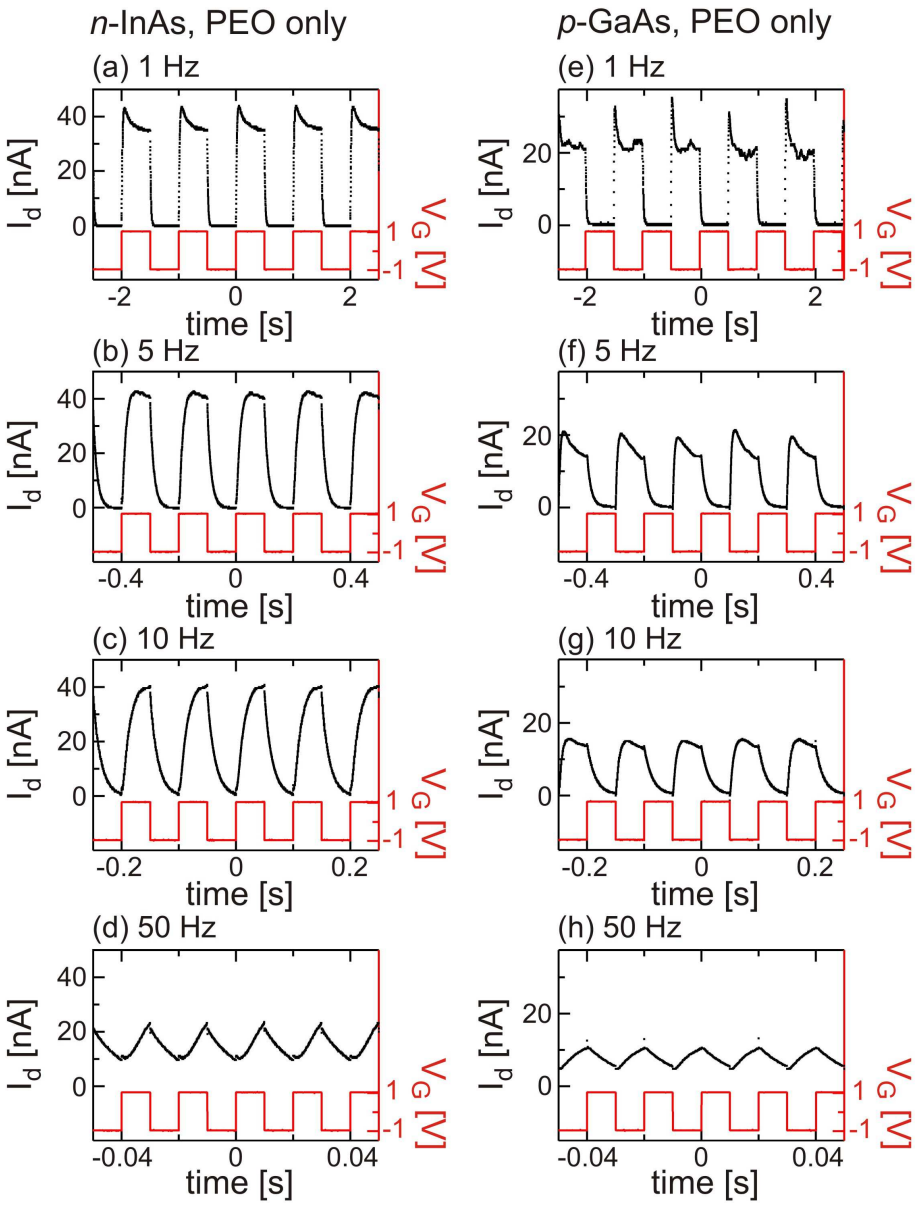

FIGURE 6.13: Square pulse trains -1 V $< V_G < +1$ V at frequency f for (a-d) n-InAs and (e-h) p-GaAs devices with PEO only dielectrics at $P_{rel} = 1$. The devices are switched on and off up to 50 Hz.

with the channels of p-GaAs and n-InAs devices connected in series. The devices were on separate chips in the same chamber at $P_{rel} = 1$, connected *via* external circuitry. Ultimately the ideal situation would be to have the devices side-by-side on the same chip linked by a common PEO gate. Here, the devices were linked *via* external circuitry as it was the most efficient option for a simple proof of principle given the significant obstacles to placing nanowires side-by-side on the same chip. It is possible to achieve lateral nanowire alignment using trenches

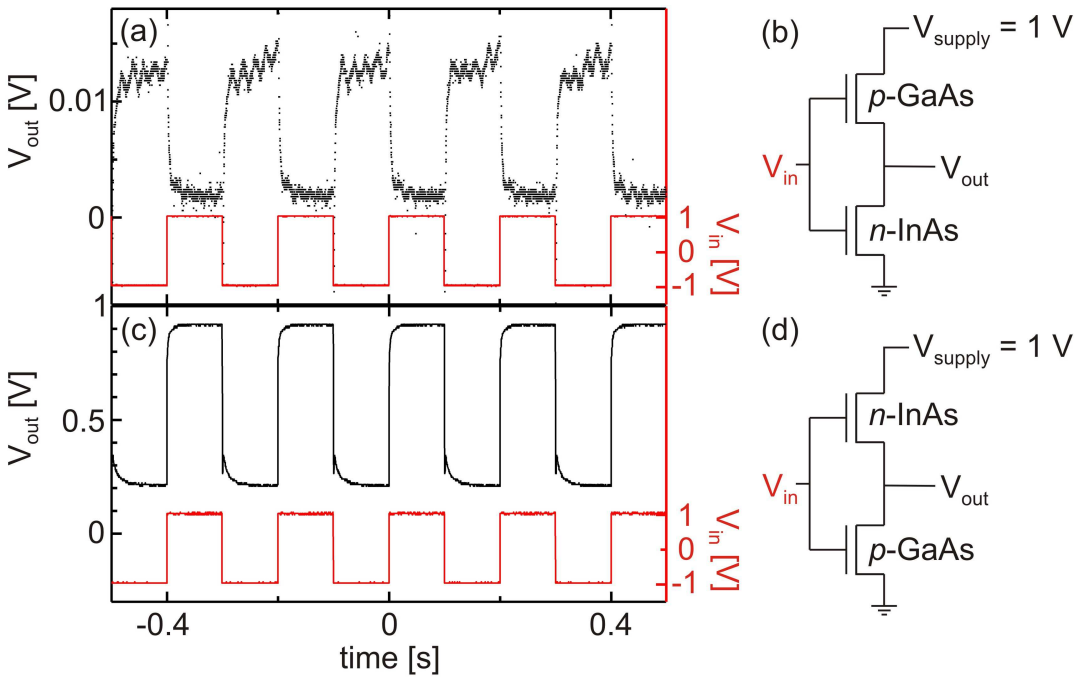

FIGURE 6.14: (a) Data and (b) schematic for an inverter circuit with complementary n-InAs and p-GaAs devices. The circuit inverts the V_{in} signal at V_{out} but gain is severely limited by the poor ohmic contacts to p-GaAs. The low signal resulted in visible 50 Hz noise at V_{out}. (c/d) The circuit was reversed and V_{supply} instead applied to the source of the n-InAs. Gain improved as V_{in} could swing V_{out} close to V_{supply}.

defined in an EBL resist, with a yield of approximately 14% of the trenches filled by a single nanowire.[335,336] Two consecutive steps of this process for the two different materials may result in the desired configuration. However, the low yield for this alignment process means that going through this process for a prototype would not be an efficient use of time. Significantly better alignment yield can be achieved by carefully depositing nanowires from solution onto a substrate with pre-patterned electrodes while a sinusoidal voltage is applied across the electrodes.[337] The time cost here would be in establishing a working system to perform this more complex alignment technique. In addition, the poor p-GaAs ohmic contacts limit the the inverter performance; optimising these prior to attempting complex device fabrication/application is the more efficient approach.

For the inverter circuit, a dc supply voltage V_{supply} was applied to the source of the p-GaAs. A square pulse train V_{in} was applied to the gate electrodes of both devices simultaneously and V_{out} was read out between the n-InAs/p-GaAs channels

by a DSO. Figure 6.14(a) shows that the circuit inverts the V_{in} signal at V_{out}; V_{in} is high when V_{out} is low and vice versa. However, the V_{out} signal is very weak, with a gain of only ~ 0.01. This is due the high p-GaAs source/drain contact resistance. Looking back at Fig. 6.10, the applied $V_{sd} = 1$ V generated current $I_{on} \sim 10^{-8}$ A and the resistance in the on state is therefore ~ 100 MΩ. The high resistance means that V_{out} can never reach the supply voltage as much of it will drop over the contacts even when the resistance of the transistor channel is low. To illustrate this, V_{supply} was instead sourced to the n-InAs device drain in Figs 6.14(c/d). This circuit displays excellent fidelity; the V_{out} signal closely resembles the square wave at V_{in}. Additionally, $V_{in} = 1$ V swung V_{out} close to the supply voltage $V_{supply} = 1$ V due to the low resistance across the n-InAs contacts. For $V_{in} = -1$ V, $V_{out} \sim 0.2$ V rather than ground due again to the high contact resistance of the p-GaAs nanowires.

In terms of the potential for applications, the data presented here highlights that III-V semiconductor nanowires could be very useful elements in biological interfacing. They can be gated by the field effect from proton/ion signals with operating range $V_G \pm 1$ V and the high electron/hole mobility means that fidelity and switching speed is only limited by the biological/organic material. Stability over long time-scales may be compromised by surface states, but operation at even $f = 1$ Hz nullified this influence as the pulse time is insufficient to allow charge trapping/detrapping.

There are some areas for improvement in future work. Most notably, the maximal switching speed remains around 50 Hz, limited by the ionic conductivity and device geometry. These devices have a non-local configuration; the gate electrode/nanowire separation is ~ 4 μm, meaning it takes a long time to establish the EDL. Device switching would occur much faster for thinner layers. One application would be sensing electrical signals from biological sources, e.g., cells/neurons. In this case the biological material would sit on top of the PEO, 100 nm away from the nanowire. Given 100 nm of PEO at a proton conductivity of 10^{-7} S/cm, one could expect a response time $\tau_{ion} \sim 0.6$ ms, and therefore switching speeds exceeding 1 kHz. An alternative would be to utilise materials with higher proton

conductivity such as maleic chitosan[220,223] or Nafion.[338] However, it is not clear whether either of these materials could be patterned at the nanoscale to fit between the nanowire source/drain contacts. Nanoscale patternability is a major advantage for PEO here.

Improving inverter gain will largely rest on developing low resistance ohmic contacts to *p*-GaAs nanowires. Unfortunately this process is not trivial for nanowires; their structure renders them susceptible to damage and destruction under annealing. This places constraints on annealing temperature and time that are absent for traditional planar structures. For example, ohmic contacts to *p*-type heterostructures with AuBe contacts required annealing to temperatures of 490°C. This temperature completely destroys GaAs nanowires. Increasing the doping in the nanowire itself gives better contact formation, but comes at the expense of gate controllability. A high $V_G > 10$ V was required to turn off more highly doped *p*-GaAs nanowires; this is clearly not optimal for low voltage operation. Juggling all these variables and finding the right compromise constitutes a significant project in itself. Also of concern is that GaAs surface states caused increased noise and instability at higher P_{rel}, although this may not affect high speed operation where switching occurs on a time-scale shorter than that of the trapping/de-trapping time. Development of *p*-GaAs nanowires is at an earlier stage compared to InAs nanowires, so a concerted optimisation programme may well resolve these issues. If not, one option is to turn to alternative, more developed nanowire materials, e.g. InP[19,144] or *p*-InAs.[339]

These problems aside, the data presented in this chapter makes a strong case for development of III-V nanowires towards a biological interfacing platform that could connect the organic, biological world with traditional inorganic microelectronics. Parallel to this, the discovery of relatively high proton conductivity in nanoscale patterned PEO films opens up the opportunity to use this dielectric as a polymer electrolyte without the need for additional salt doping.

Chapter 7

Discussion and conclusions

This thesis has centred on the impact of the simple concept of the field-effect transistor, and how devices based on it permeate a wide array of research areas. The drive for new, more efficient technologies has steered research towards III-V semiconductors,[3,4,12] quantum devices[5–7] and organic materials.[8–11] I explored each of these areas in this thesis and showed how their overlap can produce novel, exciting devices, such as NWFETs with organic gates. I also showed many of the challenges in developing these new devices towards potential applications. Issues due to dopant impurities and surface states repeatedly arise in nanoscale device development, due to the increased probability of inhomogeneous dopant distributions for smaller device sizes,[13–15] and the effective increase in surface-to-volume ratio bringing the surface closer to the channel.[4,21] Understanding the physics behind surfaces and dopants constitutes interesting science in itself, and is also vital to establishing the future utility of emergent devices and realising new functionalities.

The issues arising from surfaces and dopants were most prominent in the study of *p*-AlGaAs/GaAs heterostructure devices in Chapter 3. Despite the strong similarities to the hugely successful *n*-AlGaAs/GaAs heterostructures, a simple change in crystal orientation from (100) to (311)A brought about a significant change in

electrical behaviour. The differences in surface states and dopant impurity energetics rendered the *p*-type heterostructures prone to hysteresis and instability.[24] Examining the influence of the surface contribution highlighted the importance of the mixed valency of the (311)A GaAs surface and suggests that effective passivation for this surface may prove more difficult than for (100) GaAs surfaces.[32] Similarly, focussing on charge dynamics in the dopant layer revealed that shallow Si-acceptor traps cause instability as charges migrate between trapping sites.[33] By comparison, the stability of *n*-type devices is likely to be due – at least in part – to the deep DX centre charge traps in the AlGaAs layer. This encourages work on finding a stable *p*-type dopant species for (100)-oriented *p*-AlGaAs/GaAs heterostructures, where surface states may not contribute to hysteresis.

Nanowires are an interesting case study on the caveats of increased surface-to-volume ratio. On the one hand, their geometry makes them naturally suited to wrap-gating for the most effective electric field control.[145] The multiple wrap-gated NWFETs developed in Chapter 4 hold promise towards strongly confined quantum systems, e.g., quantum dots, and the scalability power of the fabrication technique encourages their use in dense, 3D architectures.[29] On the other hand, the increased surface-to-volume ratio means that the non-ideal III-V surface necessarily strongly influences carrier transport. This was especially true for the device in Chapter 5, where surface charge likely contributed to potential barriers that defined a series of quantum dots along the nanowire length.[30] However, these impurities, along with the background bulk impurities that also contribute, can be used to realise new functionality in the form of nanoscale thermoelectric elements. In these, the coupling between the quantum dot-like states and propagating modes enhances the thermoelectric efficiency across a wide range of gate voltages.[171] Harnessing this effect reliably and predictably will likely proceed by the study of devices with controlled potential barriers *via*, e.g., heterostructure barrier growth or multiple wrap-gates.

Surface states also causes instability for the NWFETs measured at room temperature. This included the PE-gated NWFETs studied in Chapters 4 and 6.[28] I showed that while surface states contributed significantly to hysteresis in the

steady state transfer characteristics for PE-gated NWFETs, this influence could be negated by switching the gate faster than the typical charge trapping time. The switching speed limit was then determined by the ionic conductivity in the polymer electrolyte. Improving switching speed through geometries where the gate electrode is closer to the nanowire, or exploring nanoscale patterning of ion-gels with a high ionic conductivity[197,210,219] would be the next step for future research. The results in Chapter 6 also constituted a proof-of-principle operation for III-V nanowires in complementary proton-to-electron transducer circuits.[11] Optimisation of the ohmic contacts to *p*-type nanowires will be central to the future success of such a programme, along with the switching speed gains outlined above.

Together, these results illustrate the importance of cutting edge semiconductor research, and how it simultaneously drives and responds to the cycle of development of new technologies through materials study and optimisation, and the subsequent realisation of new device functionalities. This thesis also shows how these devices are at the centre of a huge range of research programmes, from fundamental studies of quantum systems, to interfacing with biological environments. In all, it shows that non-ideal materials behaviour brings both challenges and opportunities in the advancement of our scientific knowledge and the continual quest for a more energy efficient world.

Bibliography

[1] S. M. Sze & M. K. Lee. *Semiconductor Devices, Physics and Technology*. Wiley, Hoboken, N.J, 3rd edition (2012)

[2] S. M. Sze & K. K. Ng. *Physics of Semiconductor Devices*. Wiley-Interscience, Hoboken, N.J, 3rd edition (2007)

[3] L. Wernersson, C. Thelander, E. Lind & L. Samuelson. 'III-V Nanowires – Extending a Narrowing Road.' *Proceedings of the IEEE* **98** (12), pp. 2047–2060 (2010)

[4] H. Riel, L. Wernersson, M. Hong & J. A. del Alamo. 'III–V compound semiconductor transistors—from planar to nanowire structures.' *MRS Bulletin* **39** (08), p. 668–677 (2014)

[5] C. W. J. Beenakker & H. van Houten. 'Quantum transport in semiconductor nanostructures.' *Solid State Physics* **44** (1), p. 228 (1991)

[6] M. Fuechsle, J. A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck & M. Y. Simmons. 'A single-atom transistor.' *Nature Nanotechnology* **7** (4), pp. 242–246 (2012)

[7] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. L. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith & M. A. Eriksson. 'Silicon quantum electronics.' *Reviews of Modern Physics* **85** (3), pp. 961–1019 (2013)

[8] S. H. Kim, K. Hong, W. Xie, K. H. Lee, S. Zhang, T. P. Lodge & C. D. Frisbie. 'Electrolyte-Gated Transistors for Organic and Printed Electronics.' *Advanced Materials* **25** (13), pp. 1822–1846 (2013)

[9] M. Berggren & A. Richter-Dahlfors. 'Organic Bioelectronics.' *Advanced Materials* **19** (20), pp. 3201–3213 (2007)

[10] R. M. Owens & G. G. Malliaras. 'Organic electronics at the interface with biology.' *MRS bulletin* **35** (06), p. 449–456 (2010)

[11] P. Meredith, C. J. Bettinger, M. Irimia-Vladu, A. B. Mostert & P. E. Schwenn. 'Electronic and optoelectronic materials and devices inspired by nature.' *Reports on Progress in Physics* **76** (3), p. 034501 (2013)

[12] J. A. del Alamo. 'Nanometre-scale electronics with III-V compound semiconductors.' *Nature* **479** (7373), pp. 317–323 (2011)

[13] K. Kuhn, C. Kenyon, A. Kornfeld, M. Liu, A. Maheshwari, Wei-kai Shih, S. Sivakumar, G. Taylor, P. Van Der Voorn & K. Zawadzki. 'Managing Process Variation in Intel's 45nm CMOS Technology.' *Intel Technology Journal* **12** (2), pp. 93–109 (2008)

[14] M. Pierre, R. Wacquez, X. Jehl, M. Sanquer, M. Vinet & O. Cueto. 'Single-donor ionization energies in a nanoscale CMOS channel.' *Nature Nanotechnology* **5** (2), pp. 133–137 (2010)

[15] M. Pioro-Ladrière, J. H. Davies, A. R. Long, A. S. Sachrajda, L. Gaudreau, P. Zawadzki, J. Lapointe, J. Gupta, Z. Wasilewski & S. Studenikin. 'Origin of switching noise in GaAs/$Al_xGa_{1-x}As$ lateral gated devices.' *Physical Review B* **72** (11), p. 115331 (2005)

[16] P. Solomon, C. Knoedler & S. Wright. 'A GaAs gate heterojunction FET.' *IEEE Electron Device Letters* **5** (9), pp. 379–381 (1984)

[17] K. Matsumoto, M. Ogura, T. Wada, N. Hashizume, T. Yao & Y. Hayashi. 'n^+-GaAs/undoped GaAlAs/undoped GaAs field-effect transistor.' *Electronics Letters* **20** (11), pp. 462–463 (1984)

[18] B. E. Kane, L. N. Pfeiffer, K. W. West & C. K. Harnett. 'Variable density high mobility two-dimensional electron and hole gases in a gated GaAs/$Al_xGa_{1-x}As$ heterostructure.' *Applied Physics Letters* **63** (15), pp. 2132–2134 (1993)

[19] K. Storm, G. Nylund, M. Borgström, J. Wallentin, C. Fasth, C. Thelander & L. Samuelson. 'Gate-Induced Fermi Level Tuning in InP Nanowires at Efficiency Close to the Thermal Limit.' *Nano Letters* **11** (3), pp. 1127–1130 (2011)

[20] K. Storm, G. Nylund, M. Borgström, J. Wallentin, C. Fasth, C. Thelander & L. Samuelson. 'Dual-gate induced InP nanowire diode.' *AIP Conference Proceedings* **1399** (1), pp. 279–280 (2011)

[21] M. Lebedev. 'Surface modification of III–V semiconductors: chemical processes and electronic properties.' *Progress in Surface Science* **70** (4-8), pp. 153–186 (2002)

[22] E. Lind, A. I. Persson, L. Samuelson & L. Wernersson. 'Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor.' *Nano Letters* **6** (9), pp. 1842–1846 (2006)

[23] C. Thelander, C. Rehnstedt, L. E. Froberg, E. Lind, T. Mårtensson, P. Caroff, T. Lowgren, B. J. Ohlsson, L. Samuelson & L. Wernersson. 'Development of a Vertical Wrap-Gated InAs FET.' *IEEE Transactions on Electron Devices* **55** (11), pp. 3030–3036 (2008)

[24] A. M. Burke, D. E. J. Waddington, D. J. Carrad, R. W. Lyttleton, H. H. Tan, P. J. Reece, O. Klochan, A. R. Hamilton, A. Rai, D. Reuter, A. D. Wieck & A. P. Micolich. 'Origin of gate hysteresis in *p*-type Si-doped AlGaAs/GaAs heterostructures.' *Physical Review B* **86** (16), p. 165309 (2012)

[25] W. Y. Mak, K. D. Gupta, H. E. Beere, I. Farrer, F. Sfigakis & D. A. Ritchie. 'Distinguishing impurity concentrations in GaAs and AlGaAs using very shallow undoped heterostructures.' *Applied Physics Letters* **97** (24), p. 242107 (2010)

[26] D. Q. Wang, J. C. H. Chen, O. Klochan, K. Das Gupta, D. Reuter, A. D. Wieck, D. A. Ritchie & A. R. Hamilton. 'Influence of surface states on quantum and transport lifetimes in high-quality undoped heterostructures.' *Physical Review B* **87** (19), p. 195313 (2013)

[27] J. R. Waldrop. 'Schottky-barrier height of ideal metal contacts to GaAs.' *Applied Physics Letters* **44** (10), pp. 1002–1004 (1984)

[28] D. J. Carrad, A. M. Burke, R. W. Lyttleton, H. J. Joyce, H. H. Tan, C. Jagadish, K. Storm, H. Linke, L. Samuelson & A. P. Micolich. 'Electron-Beam Patterning of Polymer Electrolyte Films To Make Multiple Nanoscale Gates for Nanowire Transistors.' *Nano Letters* **14** (1), pp. 94–100 (2014)

[29] A. M. Burke, D. J. Carrad, J. G. Gluschke, K. Storm, S. Fahlvik Svensson, H. Linke, L. Samuelson & A. P. Micolich. 'InAs Nanowire Transistors with Multiple, Independent Wrap-Gate Segments.' *Nano Letters* **15** (5), pp. 2836–2843 (2015)

[30] S. Fahlvik Svensson, A. M. Burke, D. J. Carrad, M. Leijnse, H. Linke & A. P. Micolich. 'Using Polymer Electrolyte Gates to set-and-freeze Threshold Voltage and Local Potential in Nanowire-based Devices and Thermoelectrics.' *Advanced Functional Materials* **25** (2), pp. 255–262 (2015)

[31] D. Carrad, A. Burke, S. Fahlvik Svensson, R. Lyttleton, H. Joyce, H. H. Tan, C. Jagadish, K. Storm, L. Samuelson, H. Linke & A. Micolich. 'Nanoscale polymer electrolytes: Fabrication and applications using nanowire transistors.' In: *2014 Conference on Optoelectronic and Microelectronic Materials Devices (COMMAD)*, pp. 286–289 (2014)

[32] D. J. Carrad, A. M. Burke, P. J. Reece, R. W. Lyttleton, D. E. J. Waddington, A. Rai, D. Reuter, A. D. Wieck & A. P. Micolich. 'The effect of $(NH_4)_2S_x$ passivation on the (311)A GaAs surface and its use in AlGaAs/GaAs heterostructure devices.' *Journal of Physics: Condensed Matter* **25** (32), p. 325304 (2013)

[33] D. J. Carrad, A. M. Burke, O. Klochan, A. M. See, A. R. Hamilton, A. Rai, D. Reuter, A. D. Wieck & A. P. Micolich. 'Determining the stability and activation energy of Si acceptors in AlGaAs using quantum interference in an open hole quantum dot.' *Physical Review B* **89** (15), p. 155313 (2014)

[34] C. Kittel. *Introduction to Solid State Physics*. Wiley, Hoboken, NJ, 8th ed edition (2005)

[35] J. H. Davies. *The physics of low-dimensional semiconductors: an introduction*. Cambridge University Press, Cambridge, United Kingdom (1998)

[36] A. Asenov. 'Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm MOSFETs: a statistical 3D 'atomistic' simulation study.' *Nanotechnology* **10** (2), pp. 153–158 (1999)

[37] D. H. Cobden, A. Savchenko, M. Pepper, N. K. Patel, D. A. Ritchie, J. E. F. Frost & G. A. C. Jones. 'Time-irreversible random telegraph signal due to current along a single hopping chain.' *Physical Review Letters* **69** (3), pp. 502–505 (1992)

[38] D. K. Biegelsen, R. D. Bringans, J. E. Northrup & L. Swartz. 'Surface reconstructions of GaAs (100) observed by scanning tunneling microscopy.' *Physical Review B* **41** (9), p. 5701 (1990)

[39] L. M. Terman. 'An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes.' *Solid-State Electronics* **5** (5), pp. 285–299 (1962)

[40] L. Lin & J. Robertson. 'Passivation of interfacial defects at III-V oxide interfaces.' *Journal of Vacuum Science & Technology B* **30** (4), p. 04E101 (2012)

[41] J. Fan, H. Oigawa & Y. Nannichi. 'The Effect of $(NH_4)_2S$ Treatment on the Interface Characteristics of GaAs MIS Structures.' *Japanese Journal of Applied Physics* **27** (7A), p. L1331 (1988)

[42] R. Cohen, L. Kronik, A. Vilan, A. Shanzer & D. Cahen. 'Frontier Orbital Model of Semiconductor Surface Passivation: Dicarboxylic Acids on *n*- and *p*-GaAs.' *Advanced Materials* **12** (1), pp. 33–37 (2000)

[43] D. Liu, T. Zhang, R. A. LaRue, J. S. Harris Jr & T. W. Sigmon. 'Deep level transient spectroscopy study of GaAs surface states treated with inorganic sulfides.' *Applied Physics Letters* **53** (12), pp. 1059–1061 (1988)

[44] V. N. Bessolov & M. V. Lebedev. 'Chalcogenide passivation of III–V semiconductor surfaces.' *Semiconductors* **32** (11), pp. 1141–1156 (1998)

[45] T. Ishikawa & H. Ikoma. 'X-Ray Photoelectron Spectroscopic Analysis of the Oxide of GaAs.' *Japanese Journal of Applied Physics* **31** (12R), p. 3981 (1992)

[46] W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su & I. Lindau. 'New and unified model for Schottky barrier and III–V insulator interface states formation.' *Journal of Vacuum Science & Technology* **16** (5), pp. 1422–1433 (1979)

[47] W. E. Spicer, I. Lindau, P. Skeath & C. Y. Su. 'Unified defect model and beyond.' *Journal of Vacuum Science & Technology* **17** (5), pp. 1019–1027 (1980)

[48] S. A. Dayeh. 'Electron transport in indium arsenide nanowires.' *Semiconductor Science and Technology* **25** (2), p. 024004 (2010)

[49] M. Heyns & W. Tsai. 'Ultimate Scaling of CMOS Logic Devices with Ge and III–V Materials.' *MRS Bulletin* **34** (07), p. 485–492 (2009)

[50] Y. Nannichi, J. Fan, H. Oigawa & A. Koma. 'A Model to Explain the Effective Passivation of the GaAs Surface by $(NH_4)_2S$ Treatment.' *Japanese Journal of Applied Physics* **27** (12A), p. L2367 (1988)

[51] V. N. Bessolov, A. F. Ivankov & M. V. Lebedev. 'Sulfide passivation of III–V semiconductors: The starting electronic structure of a semiconductor as a

factor in the interaction between its valence electrons and the sulfur ion.' *Journal of Vacuum Science & Technology B* **13** (3), pp. 1018–1023 (1995)

[52] V. N. Bessolov, E. V. Konenkova & M. V. Lebedev. 'Sulfidization of GaAs in alcoholic solutions: a method having an impact on efficiency and stability of passivation.' *Materials Science and Engineering: B* **44** (1), pp. 376–379 (1997)

[53] C. J. Sandroff, R. N. Nottenburg, J. Bischoff & R. Bhat. 'Dramatic enhancement in the gain of a GaAs/AlGaAs heterostructure bipolar transistor by surface chemical passivation.' *Applied Physics Letters* **51** (1), pp. 33–35 (1987)

[54] R. S. Besser & C. R. Helms. 'Comparison of surface properties of sodium sulfide and ammonium sulfide passivation of GaAs.' *Journal of Applied Physics* **65** (11), pp. 4306–4310 (1989)

[55] M. S. Carpenter, M. R. Melloch & T. E. Dungan. 'Schottky barrier formation on $(NH_4)_2S$-treated n-and p-type (100) GaAs.' *Applied Physics Letters* **53** (1), pp. 66–68 (1988)

[56] M. S. Carpenter, M. R. Melloch, B. A. Cowans, Z. Dardas & W. N. Delgass. 'Investigations of ammonium sulfide surface treatments on GaAs.' *Journal of Vacuum Science & Technology B* **7** (4), pp. 845–850 (1989)

[57] C. J. Sandroff, M. S. Hegde & C. C. Chang. 'Structure and stability of passivating arsenic sulfide phases on GaAs surfaces.' *Journal of Vacuum Science & Technology B* **7** (4), pp. 841–844 (1989)

[58] C. J. Sandroff, M. S. Hegde, L. A. Farrow, C. C. Chang & J. P. Harbison. 'Electronic passivation of GaAs surfaces through the formation of arsenic-sulfur bonds.' *Applied Physics Letters* **54** (4), pp. 362–364 (1989)

[59] H. Sugahara, M. Oshima, H. Oigawa, H. Shigekawa & Y. Nannichi. 'Synchrotron radiation photoemission analysis for $(NH_4)_2S_x$-treated GaAs.' *Journal of Applied Physics* **69** (8), pp. 4349–4353 (1991)

[60] H. Sugahara, M. Oshima, R. Klauser, H. Oigawa & Y. Nannichi. 'Bonding states of chemisorbed sulfur atoms on GaAs.' *Surface Science* **242** (1-3), pp. 335–340 (1991)

[61] C. J. Spindt, D. Liu, K. Miyano, P. L. Meissner, T. T. Chiang, T. Kendelewicz, I. Lindau & W. E. Spicer. 'Vacuum ultraviolet photoelectron spectroscopy of $(NH_4)_2S$-treated GaAs (100) surfaces.' *Applied Physics Letters* **55** (9), pp. 861–863 (1989)

[62] Y. Jeong, K. Choi, S. Jo & B. Kang. 'Effects of Sulfide Passivation on the Performance of GaAs MISFETs with Photo-CVD Grown P_3N_5 Gate Insulators.' *Japanese Journal of Applied Physics* **34** (2S), p. 1176 (1995)

[63] T. Ihn. *Semiconductor Nanostructures: Quantum states and electronic transport.* Oxford University Press, Oxford, United Kingdom (2009)

[64] M. A. Kastner. 'Artificial Atoms.' *Physics Today* **46** (1), pp. 24–31 (1993)

[65] C. M. Marcus, A. J. Rimberg, R. M. Westervelt, P. F. Hopkins & A. C. Gossard. 'Conductance fluctuations and chaotic scattering in ballistic microstructures.' *Physical Review Letters* **69** (3), pp. 506–509 (1992)

[66] D. Loss & D. P. DiVincenzo. 'Quantum computation with quantum dots.' *Physical Review A* **57** (1), pp. 120–126 (1998)

[67] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe & J. L. O'Brien. 'Quantum computers.' *Nature* **464** (7285), pp. 45–53 (2010)

[68] E. F. Schubert. 'Light Emitting Diodes Chapter 12: Visible-spectrum LEDs.' 'https://www.ecse.rpi.edu/~schubert/Light-Emitting-Diodes-dot-org/chap12/chap12.htm

[69] G. H. Olsen. 'Interfacial lattice mismatch effects in III-V compounds.' *Journal of Crystal Growth* **31**, pp. 223–239 (1975)

[70] S. Adachi. 'GaAs, AlAs, and $Al_xGa_{1-x}As$: Material parameters for use in research and device applications.' *Journal of Applied Physics* **58** (3), pp. R1–R29 (1985)

[71] R. Dingle, H. L. Störmer, A. C. Gossard & W. Wiegmann. 'Electron mobilities in modulation-doped semiconductor heterojunction superlattices.' *Applied Physics Letters* **33** (7), pp. 665–667 (1978)

[72] T. Mimura, S. Hiyamizu, T. Fujii & K. Nanbu. 'A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions.' *Japanese Journal of Applied Physics* **19** (5), p. L225 (1980)

[73] D. Delagebeaudeuf & N. T. Linh. 'Charge control of the heterojunction two-dimensional electron gas for MESFET application.' *IEEE Transactions on Electron Devices* **28** (7), pp. 790–795 (1981)

[74] B. J. van Wees, H. van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel & C. T. Foxon. 'Quantized conductance of point contacts in a two-dimensional electron gas.' *Physical Review Letters* **60** (9), pp. 848–850 (1988)

[75] D. A. Wharam, T. J. Thornton, R. Newbury, M. Pepper, H. Ahmed, J. E. F. Frost, D. G. Hasko, D. C. Peacock, D. A. Ritchie & G. A. C. Jones. 'One-dimensional transport and the quantisation of the ballistic resistance.' *Journal of Physics C: Solid State Physics* **21** (8), p. L209 (1988)

[76] L. P. Kouwenhoven, D. G. Austing & S. Tarucha. 'Few-electron quantum dots.' *Reports on Progress in Physics* **64** (6), p. 701 (2001)

[77] C. W. J. Beenakker. 'Theory of Coulomb-blockade oscillations in the conductance of a quantum dot.' *Physical Review B* **44** (4), p. 1646 (1991)

[78] Y. Meir, N. S. Wingreen & P. A. Lee. 'Transport through a strongly interacting electron system: Theory of periodic conductance oscillations.' *Physical Review Letters* **66** (23), pp. 3048–3051 (1991)

[79] U. Meirav, M. A. Kastner & S. J. Wind. 'Single-electron charging and periodic conductance resonances in GaAs nanostructures.' *Physical Review Letters* **65** (6), pp. 771–774 (1990)

[80] J. Weis, R. J. Haug, K. von Klitzing & K. Ploog. 'Competing channels in single-electron tunneling through a quantum dot.' *Physical Review Letters* **71** (24), pp. 4019–4022 (1993)

[81] H. A. Nilsson, P. Caroff, C. Thelander, M. Larsson, J. B. Wagner, L. Wernersson, L. Samuelson & H. Q. Xu. 'Giant, Level-Dependent g Factors in InSb Nanowire Quantum Dots.' *Nano Letters* **9** (9), pp. 3151–3156 (2009)

[82] A. P. Micolich. *Fractal Magneto-conductance Fluctuations in Mesoscopic Semiconductor Billiards*. PhD thesis, University of New South Wales (2000)

[83] J. P. Bird, R. Akis, D. K. Ferry, A. P. S. de Moura, Y. Lai & K. M. Indlekofer. 'Interference and interactions in open quantum dots.' *Reports on Progress in Physics* **66** (4), p. 583 (2003)

[84] A. P. Micolich, A. M. See, B. C. Scannell, C. A. Marlow, T. P. Martin, I. Pilgrim, A. R. Hamilton, H. Linke & R. P. Taylor. 'Is it the boundaries or disorder that dominates electron transport in semiconductor 'billiards'?' *Fortschritte der Physik* **61** (2-3), pp. 332–347 (2013)

[85] J. A. Nixon & J. H. Davies. 'Potential fluctuations in heterostructure devices.' *Physical Review B* **41** (11), p. 7929 (1990)

[86] P. T. Coleridge. 'Small-angle scattering in two-dimensional electron gases.' *Physical Review B* **44** (8), pp. 3793–3801 (1991)

[87] S. J. MacLeod, K. Chan, T. P. Martin, A. R. Hamilton, A. See, A. P. Micolich, M. Aagesen & P. E. Lindelof. 'Role of background impurities in the single-particle relaxation lifetime of a two-dimensional electron gas.' *Physical Review B* **80** (3), p. 035310 (2009)

[88] M. A. Topinka, B. J. LeRoy, R. M. Westervelt, S. E. J. Shaw, R. Fleischmann, E. J. Heller, K. D. Maranowski & A. C. Gossard. 'Coherent branched flow in a two-dimensional electron gas.' *Nature* **410** (6825), pp. 183–186 (2001)

[89] K. E. Aidala, R. E. Parrott, T. Kramer, E. J. Heller, R. M. Westervelt, M. P. Hanson & A. C. Gossard. 'Imaging magnetic focusing of coherent electron waves.' *Nature Physics* **3** (7), pp. 464–468 (2007)

[90] A. M. See, I. Pilgrim, B. C. Scannell, R. D. Montgomery, O. Klochan, A. M. Burke, M. Aagesen, P. E. Lindelof, I. Farrer, D. A. Ritchie, R. P. Taylor, A. R. Hamilton & A. P. Micolich. 'Impact of Small-Angle Scattering on Ballistic Transport in Quantum Dots.' *Physical Review Letters* **108** (19), p. 196807 (2012)

[91] B. C. Scannell, I. Pilgrim, A. M. See, R. D. Montgomery, P. K. Morse, M. S. Fairbanks, C. A. Marlow, H. Linke, I. Farrer, D. A. Ritchie, A. R. Hamilton, A. P. Micolich, L. Eaves & R. P. Taylor. 'Probing the sensitivity of electron wave interference to disorder-induced scattering in solid-state devices.' *Physical Review B* **85** (19), p. 195319 (2012)

[92] R. P. Taylor, A. P. Micolich, R. Newbury & T. M. Fromhold. 'Correlation analysis of self-similarity in semiconductor billiards.' *Physical Review B* **56** (20), pp. R12733–R12736 (1997)

[93] P. M. Mooney. 'Deep donor levels (DX centers) in III-V semiconductors.' *Journal of Applied Physics* **67** (3), pp. R1–R26 (1990)

[94] D. D. Carey, S. T. Stoddart, S. J. Bending, J. J. Harris & C. T. Foxon. 'Investigation of deep metastable traps in Si δ-doped GaAs/$Al_{0.33}Ga_{0.67}As$ quantum-well samples using noise spectroscopy.' *Physical Review B* **54** (4), p. 2813 (1996)

[95] D. Heiss, S. Schaeck, H. Huebl, M. Bichler, G. Abstreiter, J. J. Finley, D. V. Bulaev & D. Loss. 'Observation of extremely slow hole spin relaxation in self-assembled quantum dots.' *Physical Review B* **76** (24), p. 241306 (2007)

[96] D. V. Bulaev & D. Loss. 'Spin Relaxation and Decoherence of Holes in Quantum Dots.' *Physical Review Letters* **95** (7), p. 076805 (2005)

[97] B. D. Gerardot, D. Brunner, P. A. Dalgarno, P. Öhberg, S. Seidl, M. Kroner, K. Karrai, N. G. Stoltz, P. M. Petroff & R. J. Warburton. 'Optical pumping of a single hole spin in a quantum dot.' *Nature* **451** (7177), pp. 441–444 (2008)

[98] Z. K. Keane, M. C. Godfrey, J. C. H. Chen, S. Fricke, O. Klochan, A. M. Burke, A. P. Micolich, H. E. Beere, D. A. Ritchie, K. V. Trunov, D. Reuter, A. D. Wieck & A. R. Hamilton. 'Resistively Detected Nuclear Magnetic Resonance in n- and p-Type GaAs Quantum Point Contacts.' *Nano Letters* **11** (8), pp. 3147–3150 (2011)

[99] R. Winkler, S. J. Papadakis, E. P. De Poortere & M. Shayegan. 'Highly Anisotropic g-Factor of Two-Dimensional Hole Systems.' *Physical Review Letters* **85** (21), pp. 4574–4577 (2000)

[100] R. Winkler, E. Tutuc, S. J. Papadakis, S. Melinte, M. Shayegan, D. Wasserman & S. A. Lyon. 'Anomalous spin polarization of GaAs two-dimensional hole systems.' *Physical Review B* **72** (19), p. 195321 (2005)

[101] J. Yau, E. P. De Poortere & M. Shayegan. 'Aharonov-Bohm Oscillations with Spin: Evidence for Berry's Phase.' *Physical Review Letters* **88** (14), p. 146801 (2002)

[102] R. Danneau, O. Klochan, W. R. Clarke, L. H. Ho, A. P. Micolich, M. Y. Simmons, A. R. Hamilton, M. Pepper & D. A. Ritchie. '0.7 Structure and Zero Bias Anomaly in Ballistic Hole Quantum Wires.' *Physical Review Letters* **100** (1), p. 016403 (2008)

[103] O. Klochan, A. P. Micolich, A. R. Hamilton, K. Trunov, D. Reuter & A. D. Wieck. 'Observation of the Kondo Effect in a Spin-$\frac{3}{2}$ Hole Quantum Dot.' *Physical Review Letters* **107** (7), p. 076805 (2011)

[104] H. L. Störmer & W. Tsang. 'Two-dimensional hole gas at a semiconductor heterojunction interface.' *Applied Physics Letters* **36** (8), pp. 685–687 (1980)

[105] W. I. Wang, E. E. Mendez, T. S. Kuan & L. Esaki. 'Crystal orientation dependence of silicon doping in molecular beam epitaxial AlGaAs/GaAs heterostructures.' *Applied Physics Letters* **47** (8), pp. 826–828 (1985)

[106] B. Grbić, R. Leturcq, K. Ensslin, D. Reuter & A. D. Wieck. 'Single-hole transistor in p-type GaAs/AlGaAs heterostructures.' *Applied Physics Letters* **87** (23), p. 232108 (2005)

[107] C. Gerl, J. Bauer & W. Wegscheider. 'Growth and subband structure determination of high mobility hole gases on (001) and (110) GaAs.' *Journal of Crystal Growth* **301–302**, pp. 145–147 (2007)

[108] M. Csontos, Y. Komijani, I. Shorubalko, K. Ensslin, D. Reuter & A. D. Wieck. 'Nanostructures in p-GaAs with improved tunability.' *Applied Physics Letters* **97** (2), p. 022110 (2010)

[109] L. P. Rokhinson, D. C. Tsui, L. N. Pfeiffer & K. W. West. 'AFM local oxidation nanopatterning of a high mobility shallow 2D hole gas.' *Superlattices and Microstructures* **32** (2–3), pp. 99–102 (2002)

[110] A. J. Daneshvar, C. J. B. Ford, A. R. Hamilton, M. Y. Simmons, M. Pepper & D. A. Ritchie. 'Enhanced g-factors of a one-dimensional hole gas with quantized conductance.' *Physical Review B* **55** (20), pp. R13409–R13412 (1997)

[111] P. M. Mooney, N. S. Caswell & S. L. Wright. 'The capture barrier of the DX center in Si-doped $Al_xGa_{1-x}As$.' *Journal of Applied Physics* **62** (12), pp. 4786–4797 (1987)

[112] D. J. Chadi & K. J. Chang. 'Energetics of DX-center formation in GaAs and $Al_xGa_{1-x}As$ alloys.' *Physical Review B* **39** (14), p. 10063 (1989)

[113] N. Galbiati, E. Grilli, M. Guzzi, L. Brusaferri, L. Pavesi & M. Henini. 'Photoluminescence investigation of Si as p-type dopant in AlGaAs grown by molecular beam epitaxy on high-index planes.' *Semiconductor Science and Technology* **11** (12), p. 1830 (1996)

[114] C. Berven, M. N. Wybourne, A. Ecker & S. M. Goodnick. 'Negative differential conductance in quantum waveguides.' *Physical Review B* **50** (19), pp. 14639–14642 (1994)

[115] L. Desplanque, S. E. Kazzi, C. Coinon, S. Ziegler, B. Kunert, A. Beyer, K. Volz, W. Stolz, Y. Wang, P. Ruterana & X. Wallart. 'Monolithic integration of high electron mobility InAs-based heterostructure on exact (001) Silicon using a GaSb/GaP accommodation layer.' *Applied Physics Letters* **101** (14), p. 142111 (2012)

[116] Q. Y. Tong & U. Gösele. 'Semiconductor wafer bonding: recent developments.' *Materials Chemistry and Physics* **37** (2), pp. 101–127 (1994)

[117] A. Fontcuberta i Morral, J. M. Zahler, H. A. Atwater, S. P. Ahrenkiel & M. W. Wanlass. 'InGaAs/InP double heterostructures on InP/Si templates fabricated by wafer bonding and hydrogen-induced exfoliation.' *Applied Physics Letters* **83** (26), pp. 5413–5415 (2003)

[118] T. Mårtensson, M. Borgström, W. Seifert, B. J. Ohlsson & L. Samuelson. 'Fabrication of individually seeded nanowire arrays by vapour–liquid–solid growth.' *Nanotechnology* **14** (12), p. 1255 (2003)

[119] J. Hu, T. W. Odom & C. M. Lieber. 'Chemistry and Physics in One Dimension: Synthesis and Properties of Nanowires and Nanotubes.' *Accounts of Chemical Research* **32** (5), pp. 435–445 (1999)

[120] M. Yazawa, M. Koguchi & K. Hiruma. 'Heteroepitaxial ultrafine wire-like growth of InAs on GaAs substrates.' *Applied Physics Letters* **58** (10), pp. 1080–1082 (1991)

[121] K. Haraguchi, T. Katsuyama, K. Hiruma & K. Ogawa. 'GaAs p-n junction formed in quantum wire crystals.' *Applied Physics Letters* **60** (6), pp. 745–747 (1992)

[122] X. Duan & C. M. Lieber. 'General Synthesis of Compound Semiconductor Nanowires.' *Advanced Materials* **12** (4), pp. 298–302 (2000)

[123] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg & L. Samuelson. 'One-dimensional heterostructures in semiconductor nanowhiskers.' *Applied Physics Letters* **80** (6), pp. 1058–1060 (2002)

[124] L. Samuelson. 'Self-forming nanoscale devices.' *Materials Today* **6** (10), pp. 22 – 31 (2003)

[125] D. Spirkoska, C. Colombo, M. Heiss, G. Abstreiter & A. Fontcuberta i Morral. 'The use of molecular beam epitaxy for the synthesis of high purity III–V nanowires.' *Journal of Physics: Condensed Matter* **20** (45), p. 454225 (2008)

[126] C. Colombo, D. Spirkoska, M. Frimmer, G. Abstreiter & A. Fontcuberta i Morral. 'Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy.' *Physical Review B* **77** (15), p. 155326 (2008)

[127] E. Ertekin, P. A. Greaney, D. C. Chrzan & T. D. Sands. 'Equilibrium limits of coherency in strained nanowire heterostructures.' *Journal of Applied Physics* **97** (11), p. 114325 (2005)

[128] M. W. Larsson, J. B. Wagner, M. Wallin, P. Håkansson, L. E. Fröberg, L. Samuelson & L. R. Wallenberg. 'Strain mapping in free-standing heterostructured wurtzite InAs/InP nanowires.' *Nanotechnology* **18** (1), p. 015504 (2007)

[129] K. Tomioka, M. Yoshimura & T. Fukui. 'A III-V nanowire channel on silicon for high-performance vertical transistors.' *Nature* **488** (7410), pp. 189–192 (2012)

[130] M. Borg, H. Schmid, K. E. Moselund, G. Signorello, L. Gignac, J. Bruley, C. Breslin, P. Das Kanungo, P. Werner & H. Riel. 'Vertical III–V Nanowire Device Integration on Si(100).' *Nano Letters* **14** (4), pp. 1914–1920 (2014)

[131] H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia & H. Riel. 'Template-assisted selective epitaxy of III–V nanoscale

devices for co-planar heterogeneous integration with Si.' *Applied Physics Letters* **106** (23), p. 233101 (2015)

[132] L. J. Lauhon, M. S. Gudiksen, D. Wang & C. M. Lieber. 'Epitaxial core–shell and core–multishell nanowire heterostructures.' *Nature* **420** (6911), pp. 57–61 (2002)

[133] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg & L. Samuelson. 'One-dimensional Steeplechase for Electrons Realized.' *Nano Letters* **2** (2), pp. 87–89 (2002)

[134] A. W. Dey, J. Svensson, M. Ek, E. Lind, C. Thelander & L. Wernersson. 'Combining Axial and Radial Nanowire Heterostructures: Radial Esaki Diodes and Tunnel Field-Effect Transistors.' *Nano Letters* **13** (12), pp. 5919–5924 (2013)

[135] C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, W. Riess, B. J. Ohlsson & U. Gösele. 'Nanowire-based one-dimensional electronics.' *Materials Today* **9** (10), p. 28–35 (2006)

[136] 'Aledia website.' http://www.aledia.com

[137] 'Sol Voltaics AB website.' http://www.solvoltaics.com

[138] 'Glo AB website.' http://www.glo.se

[139] C. Rehnstedt, T. Mårtensson, C. Thelander, L. Samuelson & L. Wernersson. 'Vertical InAs Nanowire Wrap Gate Transistors on Si Substrates.' *IEEE Transactions on Electron Devices* **55** (11), pp. 3037–3041 (2008)

[140] C. Rehnstedt, C. Thelander, L. Fröberg, B. Ohlsson, L. Samuelson & L. Wernersson. 'Drive current and threshold voltage control in vertical InAs wrap-gate transistors.' *Electronics Letters* **44** (3), p. 236 (2008)

[141] M. Egard, S. Johansson, A. Johansson, K. Persson, A. W. Dey, B. M. Borg, C. Thelander, L. Wernersson & E. Lind. 'Vertical InAs Nanowire Wrap Gate Transistors with $f_t > 7$ GHz and $f_{max} > 20$ GHz.' *Nano Letters* **10** (3), pp. 809–812 (2010)

[142] S. Johansson, E. Memisevic, L. Wernersson & E. Lind. 'RF characterization of vertical InAs nanowire MOSFETs with f_t and f_{max}; above 140 GHz.' In: *26th Internation Conference on Indium Phosphide and Related Materials (IPRM)*, pp. 1–2 (2014)

[143] D. R. Khanal & J. Wu. 'Gate Coupling and Charge Distribution in Nanowire Field Effect Transistors.' *Nano Letters* **7** (9), pp. 2778–2783 (2007)

[144] X. Duan, Y. Huang, Y. Cui, J. Wang & C. M. Lieber. 'Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices.' *Nature* **409** (6816), pp. 66–69 (2001)

[145] K. Storm, G. Nylund, L. Samuelson & A. P. Micolich. 'Realizing Lateral Wrap-Gated Nanowire FETs: Controlling Gate Length with Chemistry Rather than Lithography.' *Nano Letters* **12** (1), pp. 1–6 (2012)

[146] A. R. Ullah, H. J. Joyce, A. M. Burke, J. Wong-Leung, H. H. Tan, C. Jagadish & A. P. Micolich. 'Electronic comparison of InAs wurtzite and zincblende phases using nanowire transistors.' *Physica Status Solidi – Rapid Research Letters* **7** (10), pp. 911–914 (2013)

[147] S. Morkötter, N. Jeon, D. Rudolph, B. Loitsch, D. Spirkoska, E. Hoffmann, M. Döblinger, S. Matich, J. J. Finley, L. J. Lauhon, G. Abstreiter & G. Koblmüller. 'Demonstration of Confined Electron Gas and Steep-Slope Behavior in Delta-Doped GaAs-AlGaAs Core–Shell Nanowire Transistors.' *Nano Letters* **15** (5), pp. 3295–3302 (2015)

[148] A. Pfund, I. Shorubalko, R. Leturcq & K. Ensslin. 'Top-gate defined double quantum dots in InAs nanowires.' *Applied Physics Letters* **89** (25), p. 252106 (2006)

[149] A. Fuhrer, C. Fasth & L. Samuelson. 'Single electron pumping in InAs nanowire double quantum dots.' *Applied Physics Letters* **91** (5), p. 052109 (2007)

[150] M. T. Björk, C. Thelander, A. E. Hansen, L. E. Jensen, M. W. Larsson, L. R. Wallenberg & L. Samuelson. 'Few-Electron Quantum Dots in Nanowires.' *Nano Letters* **4** (9), pp. 1621–1625 (2004)

[151] S. Chuang, Q. Gao, R. Kapadia, A. C. Ford, J. Guo & A. Javey. 'Ballistic InAs Nanowire Transistors.' *Nano Letters* **13** (2), pp. 555–558 (2013)

[152] C. Thelander, T. Mårtensson, M. T. Björk, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg & L. Samuelson. 'Single-electron transistors in heterostructure nanowires.' *Applied Physics Letters* **83** (10), p. 2052 (2003)

[153] A. Fuhrer, L. E. Fröberg, J. N. Pedersen, M. W. Larsson, A. Wacker, M. Pistol & L. Samuelson. 'Few Electron Double Quantum Dots in InAs/InP Nanowire Heterostructures.' *Nano Letters* **7** (2), pp. 243–246 (2007)

[154] M. T. Björk, A. Fuhrer, A. E. Hansen, M. W. Larsson, L. E. Fröberg & L. Samuelson. 'Tunable effective g factor in InAs nanowire quantum dots.' *Physical Review B* **72** (20), p. 201307 (2005)

[155] S. Csonka, L. Hofstetter, F. Freitag, S. Oberholzer, C. Schönenberger, T. S. Jespersen, M. Aagesen & J. Nygård. 'Giant Fluctuations and Gate Control of the g-Factor in InAs Nanowire Quantum Dots.' *Nano Letters* **8** (11), pp. 3932–3935 (2008)

[156] C. Thelander, M. T. Björk, M. W. Larsson, A. E. Hansen, L. R. Wallenberg & L. Samuelson. 'Electron transport in InAs nanowires and heterostructure nanowire devices.' *Solid State Communications* **131** (9–10), pp. 573–579 (2004)

[157] I. van Weperen, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov & L. P. Kouwenhoven. 'Quantized Conductance in an InSb Nanowire.' *Nano Letters* **13** (2), pp. 387–391 (2013)

[158] A. C. Ford, S. B. Kumar, R. Kapadia, J. Guo & A. Javey. 'Observation of Degenerate One-Dimensional Sub-Bands in Cylindrical InAs Nanowires.' *Nano Letters* **12** (3), pp. 1340–1343 (2012)

[159] Y. Tian, M. R. Sakr, J. M. Kinder, D. Liang, M. J. MacDonald, R. L. J. Qiu, H. Gao & X. P. A. Gao. 'One-Dimensional Quantum Confinement Effect Modulated Thermoelectric Properties in InAs Nanowires.' *Nano Letters* **12** (12), pp. 6492–6497 (2012)

[160] S. Abay, D. Persson, H. Nilsson, H. Q. Xu, M. Fogelström, V. Shumeiko & P. Delsing. 'Quantized Conductance and Its Correlation to the Supercurrent in a Nanowire Connected to Superconductors.' *Nano Letters* **13** (8), pp. 3614–3617 (2013)

[161] R. M. Lutchyn, J. D. Sau & S. Das Sarma. 'Majorana Fermions and a Topological Phase Transition in Semiconductor-Superconductor Heterostructures.' *Physical Review Letters* **105** (7), p. 077001 (2010)

[162] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers & L. P. Kouwenhoven. 'Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices.' *Science* **336** (6084), pp. 1003–1007 (2012)

[163] L. D. Hicks & M. S. Dresselhaus. 'Thermoelectric figure of merit of a one-dimensional conductor.' *Physical Review B* **47** (24), p. 16631 (1993)

[164] N. Mingo. 'Thermoelectric figure of merit and maximum power factor in III–V semiconductor nanowires.' *Applied Physics Letters* **84** (14), p. 2652 (2004)

[165] X. Zhou, S. A. Dayeh, D. Aplin, D. Wang & E. T. Yu. 'Direct observation of ballistic and drift carrier transport regimes in InAs nanowires.' *Applied Physics Letters* **89** (5), p. 053113 (2006)

[166] M. J. Tambe, S. K. Lim, M. J. Smith, L. F. Allard & S. Gradečak. 'Realization of defect-free epitaxial core-shell GaAs/AlGaAs nanowire heterostructures.' *Applied Physics Letters* **93** (15), p. 151917 (2008)

[167] I. Terasaki. 'Thermal Conductivity and Thermoelectric Power of Semiconductors.' In: P. Battacharya, R. Fornari & H. Kamimura (eds.), *Comprehensive Semiconductor Science and Technology*, pp. 326 – 358. Elsevier, Amsterdam, The Netherlands (2011)

[168] L. E. Bell. 'Cooling, Heating, Generating Power, and Recovering Waste Heat with Thermoelectric Systems.' *Science* **321** (5895), pp. 1457–1461 (2008)

[169] K. Nielsch, J. Bachmann, J. Kimling & H. Böttner. 'Thermoelectric Nanostructures: From Physical Model Systems towards Nanograined Composites.' *Advanced Energy Materials* **1** (5), pp. 713–731 (2011)

[170] M. S. Dresselhaus, G. Chen, M. Y. Tang, R. G. Yang, H. Lee, D. Z. Wang, Z. F. Ren, J. Fleurial & P. Gogna. 'New Directions for Low-Dimensional Thermoelectric Materials.' *Advanced Materials* **19** (8), pp. 1043–1053 (2007)

[171] P. M. Wu, J. Gooth, X. Zianni, S. F. Svensson, J. G. Gluschke, K. A. Dick, C. Thelander, K. Nielsch & H. Linke. 'Large Thermoelectric Power Factor Enhancement Observed in InAs Nanowires.' *Nano Letters* **13** (9), p. 4080–4086 (2013)

[172] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar & P. Yang. 'Enhanced thermoelectric performance of rough silicon nanowires.' *Nature* **451** (7175), pp. 163–167 (2008)

[173] N. Nakpathomkun, H. Q. Xu & H. Linke. 'Thermoelectric efficiency at maximum power in low-dimensional systems.' *Physical Review B* **82** (23), p. 235428 (2010)

[174] P. Mensch, S. Karg, V. Schmidt, B. Gotsmann, H. Schmid & H. Riel. 'One-dimensional behavior and high thermoelectric power factor in thin indium arsenide nanowires.' *Applied Physics Letters* **106** (9), p. 093101 (2015)

[175] A. C. Bleszynski, F. A. Zwanenburg, R. M. Westervelt, A. L. Roest, E. P. A. M. Bakkers & L. P. Kouwenhoven. 'Scanned Probe Imaging of Quantum Dots inside InAs Nanowires.' *Nano Letters* **7** (9), pp. 2559–2562 (2007)

[176] X. Zianni. 'Diameter-modulated nanowires as candidates for high thermoelectric energy conversion efficiency.' *Applied Physics Letters* **97** (23), p. 233106 (2010)

[177] X. Zianni. 'Efficient thermoelectric energy conversion on quasi-localized electron states in diameter modulated nanowires.' *Nanoscale Research Letters* **6** (1), p. 1–6 (2011)

[178] X. Zianni. 'Disorder-induced enhancement of the thermoelectric efficiency in diameter-modulated nanowires.' *Microelectronic Engineering* **112**, pp. 235–240 (2013)

[179] A. A. M. Staring, L. W. Molenkamp, B. W. Alphenaar, H. Van Houten, O. J. A. Buyk, M. A. A. Mabesoone, C. W. J. Beenakker & C. T. Foxon. 'Coulomb-blockade oscillations in the thermopower of a quantum dot.' *Europhysics Letters* **22** (1), p. 57 (1993)

[180] S. Fahlvik Svensson, A. I. Persson, E. A. Hoffmann, N. Nakpathomkun, H. A. Nilsson, H. Q. Xu, L. Samuelson & H. Linke. 'Lineshape of the thermopower of quantum dots.' *New Journal of Physics* **14** (3), p. 033041 (2012)

[181] C. W. J. Beenakker & A. A. M. Staring. 'Theory of the thermopower of a quantum dot.' *Physical Review B* **46** (15), p. 9667 (1992)

[182] A. S. Dzurak, C. G. Smith, C. H. W. Barnes, M. Pepper, L. Martin-Moreno, C. T. Liang, D. A. Ritchie & G. A. C. Jones. 'Thermoelectric signature of the excitation spectrum of a quantum dot.' *Physical Review B* **55** (16), p. R10197 (1997)

[183] M. Turek & K. Matveev. 'Cotunneling thermopower of single electron transistors.' *Physical Review B* **65** (11), p. 115332 (2002)

[184] R. Scheibner, H. Buhmann, D. Reuter, M. N. Kiselev & L. W. Molenkamp. 'Thermopower of a Kondo Spin-Correlated Quantum Dot.' *Physical Review Letters* **95** (17), p. 176602 (2005)

[185] B. Kubala & J. König. 'Quantum-fluctuation effects on the thermopower of a single-electron transistor.' *Physical Review B* **73** (19) (2006)

[186] E. A. Hoffmann, N. Nakpathomkun, A. I. Persson, H. Linke, H. A. Nilsson & L. Samuelson. 'Quantum-dot thermometry.' *Applied Physics Letters* **91** (25), p. 252114 (2007)

[187] E. A. Hoffmann, H. A. Nilsson, J. E. Matthews, N. Nakpathomkun, A. I. Persson, L. Samuelson & H. Linke. 'Measuring Temperature Gradients over Nanometer Length Scales.' *Nano Letters* **9** (2), pp. 779–783 (2009)

[188] N. J. Appleyard, J. T. Nicholls, M. Y. Simmons, W. R. Tribe & M. Pepper. 'Thermometer for the 2D electron gas using 1D thermopower.' *Physical Review Letters* **81** (16), p. 3491 (1998)

[189] J. G. Gluschke, M. Leijnse, B. Ganjipour, K. A. Dick, H. Linke & C. Thelander. 'Characterization of Ambipolar GaSb/InAs Core–Shell Nanowires by Thermovoltage Measurements.' *ACS Nano* **9** (7), pp. 7033–7040 (2015)

[190] V. Schmidt, P. F. J. Mensch, S. F. Karg, B. Gotsmann, P. D. Kanungo, H. Schmid & H. Riel. 'Using the Seebeck coefficient to determine charge carrier concentration, mobility, and relaxation time in InAs nanowires.' *Applied Physics Letters* **104** (1), p. 012113 (2014)

[191] S. Roddaro, D. Ercolani, M. A. Safeen, S. Suomalainen, F. Rossella, F. Giazotto, L. Sorba & F. Beltram. 'Giant Thermovoltage in Single InAs Nanowire Field-Effect Transistors.' *Nano Letters* **13** (8), pp. 3638–3642 (2013)

[192] K. Storm, F. Halvardsson, M. Heurlin, D. Lindgren, A. Gustafsson, P. M. Wu, B. Monemar & L. Samuelson. 'Spatially resolved Hall effect measurement in a single semiconductor nanowire.' *Nature Nanotechnology* **7** (11), pp. 718–722 (2012)

[193] B. de Gans, P. C. Duineveld & U. S. Schubert. 'Inkjet Printing of Polymers: State of the Art and Future Developments.' *Advanced Materials* **16** (3), pp. 203–213 (2004)

[194] J. Rivnay, R. M. Owens & G. G. Malliaras. 'The Rise of Organic Bioelectronics.' *Chemistry of Materials* **26** (1), pp. 679–685 (2014)

[195] W. H. Brattain & C. G. B. Garrett. 'Experiments on the Interface Between Germanium and an Electrolyte.' *Bell System Technical Journal* **34** (1), pp. 129 – 176 (1955)

[196] D. Liang & X. P. A. Gao. 'Strong tuning of Rashba spin–orbit interaction in single InAs nanowires.' *Nano Letters* **12** (6), pp. 3263–3267 (2012)

[197] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge & C. D. Frisbie. 'Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic.' *Nature Materials* **7** (11), pp. 900–906 (2008)

[198] D. Fenton, J. Parker & P. Wright. 'Complexes of alkali metal ions with poly(ethylene oxide).' *Polymer* **14** (11), p. 589 (1973)

[199] S. Chao & M. S. Wrighton. 'Characterization of a solid-state polyaniline-based transistor: water vapor dependent characteristics of a device employing a poly(vinyl alcohol)/phosphoric acid solid-state electrolyte.' *Journal of the American Chemical Society* **109** (22), pp. 6627–6631 (1987)

[200] S. Chao & M. S. Wrighton. 'Solid-state microelectrochemistry: electrical characteristics of a solid-state microelectrochemical transistor based on poly(3-methylthiophene).' *Journal of the American Chemical Society* **109** (7), pp. 2197–2199 (1987)

[201] P. V. Wright. 'Recent Trends in Polymer Electrolytes Based on Poly(Ethylene Oxide).' *Journal of Macromolecular Science: Part A - Chemistry* **26** (2-3), pp. 519–550 (1989)

[202] P. G. Bruce & C. A. Vincent. 'Polymer electrolytes.' *J. Chem. Soc., Faraday Trans.* **89** (17), p. 3187–3203 (1993)

[203] J. Takeya, K. Yamada, K. Hara, K. Shigeto, K. Tsukagoshi, S. Ikehata & Y. Aoyagi. 'High-density electrostatic carrier doping in organic single-crystal

transistors with polymer gel electrolyte.' *Applied Physics Letters* **88** (11), pp. 112102–112102–3 (2006)

[204] M. J. Panzer, C. R. Newman & C. D. Frisbie. 'Low-voltage operation of a pentacene field-effect transistor with a polymer electrolyte gate dielectric.' *Applied Physics Letters* **86** (10), p. 103503 (2005)

[205] M. J. Panzer & C. D. Frisbie. 'Polymer Electrolyte-Gated Organic Field-Effect Transistors: Low-Voltage, High-Current Switches for Organic Electronics and Testbeds for Probing Electrical Transport at High Charge Carrier Density.' *Journal of the American Chemical Society* **129** (20), pp. 6599–6607 (2007)

[206] M. J. Panzer & C. D. Frisbie. 'Polymer Electrolyte Gate Dielectric Reveals Finite Windows of High Conductivity in Organic Thin Film Transistors at High Charge Carrier Densities.' *Journal of the American Chemical Society* **127** (19), pp. 6960–6961 (2005)

[207] M. J. Panzer & C. D. Frisbie. 'High charge carrier densities and conductance maxima in single-crystal organic field-effect transistors with a polymer electrolyte gate dielectric.' *Applied Physics Letters* **88** (20), pp. 203504–203504–3 (2006)

[208] M. J. Panzer & C. D. Frisbie. 'High Carrier Density and Metallic Conductivity in Poly(3-hexylthiophene) Achieved by Electrostatic Charge Injection.' *Advanced Functional Materials* **16** (8), pp. 1051–1056 (2006)

[209] J. Lee, M. J. Panzer, Y. He, T. P. Lodge & C. D. Frisbie. 'Ion Gel Gated Polymer Thin-Film Transistors.' *Journal of the American Chemical Society* **129** (15), pp. 4532–4533 (2007)

[210] J. H. Cho, J. Lee, Y. He, B. S. Kim, T. P. Lodge & C. D. Frisbie. 'High-Capacitance Ion Gel Gate Dielectrics with Faster Polarization Response Times for Organic Thin Film Transistors.' *Advanced Materials* **20** (4), pp. 686–690 (2008)

[211] J. Choi, S. W. Lee, J. P. Kar, S. N. Das, J. Jeon, K. Moon, T. I. Lee, U. Jeong & J. Myoung. 'Random network transistor arrays of embedded ZnO nanorods in ion-gel gate dielectric.' *Journal of Materials Chemistry* **20** (35), pp. 7393–7397 (2010)

[212] M. A. B. H. Susan, T. Kaneko, A. Noda & M. Watanabe. 'Ion Gels Prepared by in Situ Radical Polymerization of Vinyl Monomers in an Ionic Liquid and Their Characterization as Polymer Electrolytes.' *Journal of the American Chemical Society* **127** (13), pp. 4976–4983 (2005)

[213] M. A. Klingshirn, S. K. Spear, R. Subramanian, J. D. Holbrey, J. G. Huddleston & R. D. Rogers. 'Gelation of Ionic Liquids Using a Cross-Linked Poly(Ethylene Glycol) Gel Matrix.' *Chemistry of Materials* **16** (16), pp. 3091–3097 (2004)

[214] T. P. Lodge. 'A Unique Platform for Materials Design.' *Science* **321** (5885), pp. 50–51 (2008)

[215] J. Choi, G. Cheruvally, Y. Kim, J. Kim, J. Manuel, P. Raghavan, J. Ahn, K. Kim, H. Ahn, D. S. Choi & C. E. Song. 'Poly(ethylene oxide)-based polymer electrolyte incorporating room-temperature ionic liquid for lithium batteries.' *Solid State Ionics* **178** (19–20), pp. 1235–1241 (2007)

[216] G. P. Siddons, D. Merchin, J. H. Back, J. K. Jeong & M. Shim. 'Highly Efficient Gating and Doping of Carbon Nanotubes with Polymer Electrolytes.' *Nano Letters* **4** (5), pp. 927–931 (2004)

[217] T. Ozel, A. Gaur, J. A. Rogers & M. Shim. 'Polymer Electrolyte Gating of Carbon Nanotube Network Transistors.' *Nano Letters* **5** (5), pp. 905–911 (2005)

[218] H. Shimotani, T. Kanbara, Y. Iwasa, K. Tsukagoshi, Y. Aoyagi & H. Kataura. 'Gate capacitance in electrochemical transistor of single-walled carbon nanotube.' *Applied Physics Letters* **88** (7), p. 073104 (2006)

[219] B. Nasr, D. Wang, R. Kruk, H. Rösner, H. Hahn & S. Dasgupta. 'High-Speed, Low-Voltage, and Environmentally Stable Operation of Electrochemically Gated Zinc Oxide Nanowire Field-Effect Transistors.' *Advanced Functional Materials* **23** (14), pp. 1750–1758 (2013)

[220] C. Zhong, Y. Deng, A. F. Roudsari, A. Kapetanovic, M. Anantram & M. Rolandi. 'A polysaccharide bioprotonic field-effect transistor.' *Nature Communications* **2**, p. 476 (2011)

[221] L. Glasser. 'Proton conduction and injection in solids.' *Chemical Reviews* **75** (1), pp. 21–65 (1975)

[222] H. Morgan, R. Pethig & G. T. Stevens. 'A proton-injecting technique for the measurement of hydration-dependent protonic conductivity.' *Journal of Physics E: Scientific Instruments* **19** (1), p. 80 (1986)

[223] Y. Deng, E. Josberger, J. Jin, A. F. Rousdari, B. A. Helms, C. Zhong, M. P. Anantram & M. Rolandi. 'H^+-type and OH^--type biological protonic semiconductors and complementary devices.' *Scientific Reports* **3** (2013)

[224] K. Tybrandt, K. C. Larsson, A. Richter-Dahlfors & M. Berggren. 'Ion bipolar junction transistors.' *Proceedings of the National Academy of Sciences* **107** (22), p. 9929–9932 (2010)

[225] K. Tybrandt, R. Forchheimer & M. Berggren. 'Logic gates based on ion transistors.' *Nature Communications* **3**, p. 871 (2012)

[226] D. Khodagholy, T. Doublet, P. Quilichini, M. Gurfinkel, P. Leleux, A. Ghestem, E. Ismailova, T. Hervé, S. Sanaur, C. Bernard & G. G. Malliaras. '*In vivo* recordings of brain activity using organic transistors.' *Nature Communications* **4**, p. 1575 (2013)

[227] N. Misra, J. A. Martinez, S. J. Huang, Y. Wang, P. Stroeve, C. P. Grigoropoulos & A. Noy. 'Bioelectronic silicon nanowire devices using functional membrane proteins.' *Proceedings of the National Academy of Sciences* **106** (33), p. 13780–13784 (2009)

[228] S. Upadhyay, R. Frederiksen, N. Lloret, L. D. Vico, P. Krogstrup, J. H. Jensen, K. L. Martinez & J. Nygård. 'Indium arsenide nanowire field-effect transistors for pH and biological sensing.' *Applied Physics Letters* **104** (20), p. 203504 (2014)

[229] J. Isaksson, P. Kjäll, D. Nilsson, N. Robinson, M. Berggren & A. Richter-Dahlfors. 'Electronic control of Ca^{2+} signalling in neuronal cells using an organic electronic ion pump.' *Nature Materials* **6** (9), pp. 673–679 (2007)

[230] J. Rivnay, P. Leleux, M. Sessolo, D. Khodagholy, T. Hervé, M. Fiocchi & G. G. Malliaras. 'Organic Electrochemical Transistors with Maximum Transconductance at Zero Gate Bias.' *Advanced Materials* **25** (48), pp. 7010–7014 (2013)

[231] D. Khodagholy, J. Rivnay, M. Sessolo, M. Gurfinkel, P. Leleux, L. H. Jimison, E. Stavrinidou, T. Herve, S. Sanaur, R. M. Owens & G. G. Malliaras. 'High transconductance organic electrochemical transistors.' *Nature Communications* **4**, p. 2133 (2013)

[232] K. R. Rostgaard, R. S. Frederiksen, Y. C. Liu, T. Berthing, M. H. Madsen, J. Holm, J. Nygård & K. L. Martinez. 'Vertical nanowire arrays as a versatile platform for protein detection and analysis.' *Nanoscale* **5** (21), pp. 10226–10235 (2013)

[233] 'Microposit^{TM} S1800^{TM} G2 series photoresists data sheet.' *MicroChem Corp.*

[234] 'AZ nLOF^{TM} 2000 Series i-Line Photoresists data sheet.' *Clariant Corp.*

[235] M. J. Madou. *Fundamentals of Microfabrication: The Science of Miniaturization, Second Edition*. CRC Press (2002)

[236] 'NANO^{TM} PMMA and Copolymer data sheet.' *MicroChem Corp.*

[237] V. R. Manfrinato, L. Zhang, D. Su, H. Duan, R. G. Hobbs, E. A. Stach & K. K. Berggren. 'Resolution Limits of Electron-Beam Lithography toward the Atomic Scale.' *Nano Letters* **13** (4), pp. 1555–1558 (2013)

[238] M. A. McCord & T. H. Newman. 'Low voltage, high resolution studies of electron beam resist exposure and proximity effect.' *Journal of Vacuum Science & Technology B* **10** (6), pp. 3083–3087 (1992)

[239] S. Ivanov, P. Kop'ev & N. Ledentsov. 'Interplay of beryllium segregation and diffusion in heavily doped GaAs and AlGaAs grown by molecular beam epitaxy (thermodynamic analysis).' *Journal of Crystal Growth* **108** (3-4), pp. 661–669 (1991)

[240] D. B. Suyatin, C. Thelander, M. T. Björk, I. Maximov & L. Samuelson. 'Sulfur passivation for ohmic contact formation to InAs nanowires.' *Nanotechnology* **18** (10), p. 105307 (2007)

[241] A. V. Kretinin, R. Popovitz-Biro, D. Mahalu & H. Shtrikman. 'Multimode Fabry-Pérot Conductance Oscillations in Suspended Stacking-Faults-Free InAs Nanowires.' *Nano Letters* **10** (9), pp. 3439–3445 (2010)

[242] 'About Lock-In Amplifiers.' *Stanford Research Systems*

[243] 'Four-Probe Resistivity and Hall Voltage Measurements with the Model 4200-SCS.' *Keithley Instruments, Inc.*

[244] R. de Picciotto, H. L. Stormer, L. N. Pfeiffer, K. W. Baldwin & K. W. West. 'Four-terminal resistance of a ballistic quantum wire.' *Nature* **411** (6833), pp. 51–54 (2001)

[245] S. Wirths, K. Weis, A. Winden, K. Sladek, C. Volk, S. Alagha, T. E. Weirich, M. von der Ahe, H. Hardtdegen, H. Lüth, N. Demarina, D. Grützmacher & T. Schäpers. 'Effect of Si-doping on InAs nanowire transport and morphology.' *Journal of Applied Physics* **110** (5), p. 053709 (2011)

[246] 'Heliox Sorption Pumped ^{3}He Refrigerator Systems: Principles of Operation and Control.' *Oxford Instruments* (2014)

[247] 'HelioxVL Insert Manual.' *Oxford Instruments* (2013)

[248] F. Pobell. *Matter and Methods at Low Temperatures.* Springer-Verlag, Berlin, 2nd edition (1996)

[249] A. B. Mostert, K. J. P. Davy, J. L. Ruggles, B. J. Powell, I. R. Gentle & P. Meredith. 'Gaseous Adsorption in Melanins: Hydrophilic Biomacromolecules with High Electrical Conductivities.' *Langmuir* **26** (1), pp. 412–416 (2010)

[250] A. B. Mostert, B. J. Powell, I. R. Gentle & P. Meredith. 'On the origin of electrical conductivity in the bio-electronic material melanin.' *Applied Physics Letters* **100** (9), pp. 093701–093701–3 (2012)

[251] A. B. Mostert, B. J. Powell, F. L. Pratt, G. R. Hanson, T. Sarna, I. R. Gentle & P. Meredith. 'Role of semiconductivity and ion transport in the electrical conduction of melanin.' *Proceedings of the National Academy of Sciences* **109** (23), pp. 8943–8947 (2012)

[252] B. J. Skromme, C. J. Sandroff, E. Yablonovitch & T. Gmitter. 'Effects of passivating ionic films on the photoluminescence properties of GaAs.' *Applied Physics Letters* **51** (24), pp. 2022–2024 (1987)

[253] Z. H. Lu, M. J. Graham, X. H. Feng & B. X. Yang. 'Structure of S on passivated GaAs (100).' *Applied Physics Letters* **62** (23), pp. 2932–2934 (1993)

[254] J. F. Watts. 'X-ray photoelectron spectroscopy.' *Vacuum* **45** (6–7), pp. 653–671 (1994)

[255] I. Zailer, J. E. F. Frost, C. J. B. Ford, M. Pepper, M. Y. Simmons, D. A. Ritchie, J. T. Nicholls & G. A. C. Jones. 'Phase coherence, interference, and conductance quantization in a confined two-dimensional hole gas.' *Physical Review B* **49** (7), pp. 5101–5104 (1994)

[256] S. Conrad, D. R. Mullins, Q. S. Xin & X. Y. Zhu. 'Thermal and photochemical deposition of sulfur on GaAs(100).' *Applied Surface Science* **107**, pp. 145–152 (1996)

[257] M. Passlack, M. Hong & J. P. Mannaerts. 'Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated

by insitu molecular beam epitaxy.' *Applied Physics Letters* **68** (8), pp. 1099–1101 (1996)

[258] H. Hasegawa, L. He, H. Ohno, T. Sawada, T. Haga, Y. Abe & H. Takahashi. 'Electronic and microstructural properties of disorder-induced gap states at compound semiconductor–insulator interfaces.' *Journal of Vacuum Science & Technology B* **5** (4), pp. 1097–1107 (1987)

[259] D. J. Chadi. 'Atomic and electronic structures of (111), (211), and (311) surfaces of GaAs.' *Journal of Vacuum Science & Technology B* **3** (4), pp. 1167–1169 (1985)

[260] K. Stiles & A. Kahn. 'Low energy electron diffraction study of (221) and (311) GaAs surfaces.' *Journal of Vacuum Science & Technology B* **3** (4), pp. 1089–1092 (1985)

[261] M. Sakata & H. Ikoma. 'Electrical Characteristics and Surface Chemistry of P_2S_5-Passivated GaAs.' *Japanese Journal of Applied Physics* **33** (Part 1, No. 7A), pp. 3813–3824 (1994)

[262] H. Sugahara, M. Oshima, H. Oigawa & Y. Nannichi. 'Chemistry of S/GaAs and metal/S/GaAs systems.' *Journal of Vacuum Science & Technology A* **11** (1), pp. 52–57 (1993)

[263] M. Sugiyama, S. Maeyama & M. Oshima. 'Structure of the sulfur-passivated GaAs(001) surface.' *Physical Review B* **50** (7), pp. 4905–4908 (1994)

[264] T. Ohno. 'Sulfur passivation of GaAs surfaces.' *Physical Review B* **44** (12), pp. 6306–6311 (1991)

[265] M. Sugiyama, S. Maeyama, M. Oshima, H. Oigawa, Y. Nannichi & H. Hashizume. 'Surface and interface structures of S-passivated GaAs(111) studied by soft x-ray standing waves.' *Applied Physics Letters* **60** (26), pp. 3247–3249 (1992)

[266] M. Sugiyama, S. Maeyama & M. Oshima. 'Surface-structure analysis of sulfur-passivated GaAs(111)A and GaAs(111)B by x-ray standing-wave triangulation.' *Physical Review B* **48** (15), pp. 11037–11042 (1993)

[267] B. Murphy, P. Moriarty, L. Roberts, T. Cafolla, G. Hughes, L. Koenders & P. Bailey. 'Chemical and structural studies of the interactions of molecular sulfur with the GaAs(111)A and GaAs(111)B surfaces.' *Surface Science* **317** (1-2), pp. 73–83 (1994)

[268] V. L. Berkovits, V. N. Bessolov, T. N. L'vova, E. B. Novikov, V. I. Safarov, R. V. Khasieva & B. V. Tsarenkov. 'Fermi-level movement at GaAs(001) surfaces passivated with sodium sulfide solutions.' *Journal of Applied Physics* **70** (7), pp. 3707–3711 (1991)

[269] D. Paget, A. O. Gusev & V. L. Berkovits. 'Sulfide-passivated GaAs (001). II. Electronic properties.' *Physical Review B* **53** (8), pp. 4615–4622 (1996)

[270] Z. H. Lu, F. Chatenoud, M. M. Dion, M. J. Graham, H. E. Ruda, I. Koutzarov, Q. Liu, C. E. J. Mitchell, I. G. Hill & A. B. McLean. 'Passivation of GaAs(111)A surface by Cl termination.' *Applied Physics Letters* **67** (5), pp. 670–672 (1995)

[271] Z. S. Li, W. Z. Cai, R. Z. Su, G. S. Dong, D. M. Huang, X. M. Ding, X. Y. Hou & X. Wang. 'S_2Cl_2 treatment: A new sulfur passivation method of GaAs surface.' *Applied Physics Letters* **64** (25), pp. 3425–3427 (1994)

[272] X. Cao, X. Hou, X. Chen, Z. Li, R. Su, X. Ding & X. Wang. 'Passivation of GaAs/AlGaAs heterojunction bipolar transistors by S_2Cl_2 solution.' *Applied Physics Letters* **70** (6), pp. 747–749 (1997)

[273] J. C. H. Chen, D. Q. Wang, O. Klochan, A. P. Micolich, K. D. Gupta, F. Sfigakis, D. A. Ritchie, D. Reuter, A. D. Wieck & A. R. Hamilton. 'Fabrication and characterization of ambipolar devices on an undoped AlGaAs/GaAs heterostructure.' *Applied Physics Letters* **100** (5), p. 052101 (2012)

[274] J. C. H. Chen, O. Klochan, A. P. Micolich, K. D. Gupta, F. Sfigakis, D. A. Ritchie, K. Trunov, D. Reuter, A. D. Wieck & A. R. Hamilton. 'Fabrication and characterisation of gallium arsenide ambipolar quantum point contacts.' *Applied Physics Letters* **106** (18), p. 183504 (2015)

[275] S. Faniel, B. Hackens, A. Vlad, L. Moldovan, C. Gustin, B. Habib, S. Melinte, M. Shayegan & V. Bayot. 'Dephasing time of two-dimensional holes in GaAs open quantum dots: Magnetotransport measurements.' *Physical Review B* **75** (19), p. 193310 (2007)

[276] C. W. J. Beenakker & H. van Houten. 'Magnetotransport and nonadditivity of point-contact resistances in series.' *Physical Review B* **39** (14), pp. 10445–10448 (1989)

[277] L. P. Kouwenhoven, B. J. van Wees, W. Kool, C. J. P. M. Harmans, A. A. M. Staring & C. T. Foxon. 'Transition from Ohmic to adiabatic transport in quantum point contacts in series.' *Physical Review B* **40** (11), pp. 8083–8086 (1989)

[278] R. F. Kirkman, R. A. Stradling & P. J. Lin-Chung. 'An infrared study of the shallow acceptor states in GaAs.' *Journal of Physics C: Solid State Physics* **11** (2), p. 419 (1978)

[279] R. Murray, R. C. Newman, M. J. L. Sangster, R. B. Beall, J. J. Harris, P. J. Wright, J. Wagner & M. Ramsteiner. 'The calibration of the strength of the localized vibrational modes of silicon impurities in epitaxial GaAs revealed by infrared absorption and Raman scattering.' *Journal of Applied Physics* **66** (6), pp. 2589–2596 (1989)

[280] M. J. Ashwin, M. R. Fahy, R. C. Newman, J. Wagner, D. A. Robbie, M. J. L. Sangster, I. Silier, E. Bauser, W. Braun & K. Ploog. 'A local vibrational mode investigation of *p*-type Si-doped GaAs.' *Journal of Applied Physics* **76** (12), pp. 7839–7849 (1994)

[281] N. Chand, T. Henderson, J. Klem, W. T. Masselink, R. Fischer, Y. Chang & H. Morkoĉ. 'Comprehensive analysis of Si-doped $Al_xGa_{1-x}As$ ($x = 0$ to 1): Theory and experiments.' *Physical Review B* **30** (8), p. 4481 (1984)

[282] A. M. See, A. R. Hamilton, A. P. Micolich, M. Aagesen & P. E. Lindelof. 'Using light and heat to controllably switch and reset disorder configuration in nanoscale devices.' *Physical Review B* **91** (8), p. 085417 (2015)

[283] W. R. Clarke, A. P. Micolich, A. R. Hamilton, M. Y. Simmons, K. Muraki & Y. Hirayama. 'Fabrication of induced two-dimensional hole systems on (311)A GaAs.' *Journal of Applied Physics* **99** (2), p. 023707 (2006)

[284] O. Klochan, W. R. Clarke, R. Danneau, A. P. Micolich, L. H. Ho, A. R. Hamilton, K. Muraki & Y. Hirayama. 'Ballistic transport in induced one-dimensional hole systems.' *Applied Physics Letters* **89** (9), p. 092105 (2006)

[285] O. Klochan, A. P. Micolich, L. H. Ho, A. R. Hamilton, K. Muraki & Y. Hirayama. 'The interplay between one-dimensional confinement and two-dimensional crystallographic anisotropy effects in ballistic hole quantum wires.' *New Journal of Physics* **11** (4), p. 043018 (2009)

[286] J. C. H. Chen, O. Klochan, A. P. Micolich, A. R. Hamilton, T. P. Martin, L. H. Ho, U. Zülicke, D. Reuter & A. D. Wieck. 'Observation of orientation- and k-dependent Zeeman spin-splitting in hole quantum wires on (100)-oriented AlGaAs/GaAs heterostructures.' *New Journal of Physics* **12** (3), p. 033043 (2010)

[287] O. Klochan, J. C. H. Chen, A. P. Micolich, A. R. Hamilton, K. Muraki & Y. Hirayama. 'Fabrication and characterization of an induced GaAs single hole transistor.' *Applied Physics Letters* **96** (9), p. 092103 (2010)

[288] B. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios & R. Chau. 'High performance fully-depleted tri-gate CMOS transistors.' *IEEE Electron Device Letters* **24** (4), pp. 263–265 (2003)

[289] D. Hisamoto, W. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. King, J. Bokor & C. Hu. 'FinFET-a self-aligned double-gate MOSFET scalable to 20 nm.' *IEEE Transactions on Electron Devices* **47** (12), pp. 2320–2325 (2000)

[290] H. Sellier, G. P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak & S. Biesemans. 'Transport Spectroscopy of a Single Dopant in a Gated Silicon Nanowire.' *Physical Review Letters* **97** (20), p. 206805 (2006)

[291] D. K. Ferry. 'Nanowires in Nanoelectronics.' *Science* **319** (5863), pp. 579–580 (2008)

[292] X. Li, Z. Chen, N. Shen, D. Sarkar, N. Singh, K. Banerjee, G. Lo & D. Kwong. 'Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire.' *IEEE Electron Device Letters* **32** (11), pp. 1492–1494 (2011)

[293] H. Yan, H. S. Choe, S. Nam, Y. Hu, S. Das, J. F. Klemic, J. C. Ellenbogen & C. M. Lieber. 'Programmable nanowire circuits for nanoprocessors.' *Nature* **470** (7333), pp. 240–244 (2011)

[294] L. E. Fröberg, C. Rehnstedt, C. Thelander, E. Lind, L. Wernersson & L. Samuelson. 'Heterostructure Barriers in Wrap Gated Nanowire FETs.' *IEEE Electron Device Letters* **29** (9), pp. 981–983 (2008)

[295] T. Tanaka, K. Tomioka, S. Hara, J. Motohisa, E. Sano & T. Fukui. 'Vertical Surrounding Gate Transistors Using Single InAs Nanowires Grown on Si Substrates.' *Applied Physics Express* **3** (2), p. 025003 (2010)

[296] K. Jansson, E. Lind & L. Wernersson. 'Performance Evaluation of III -V Nanowire Transistors.' *IEEE Transactions on Electron Devices* **59** (9), pp. 2375–2382 (2012)

[297] A. W. Dey, J. Svensson, B. M. Borg, M. Ek & L. Wernersson. 'Single InAs/GaSb Nanowire Low-Power CMOS Inverter.' *Nano Letters* **12** (11), pp. 5593–5597 (2012)

[298] P. Krsko, S. Sukhishvili, M. Mansfield, R. Clancy & M. Libera. 'Electron-Beam Surface-Patterned Poly(ethylene glycol) Microhydrogels.' *Langmuir* **19** (14), pp. 5618–5625 (2003)

[299] C. M. Kolodziej & H. D. Maynard. 'Electron-Beam Lithography for Patterning Biomolecules at the Micron and Nanometer Scale.' *Chemistry of Materials* **24** (5), pp. 774–780 (2012)

[300] P. Krsko, T. E. McCann, T. Thach, T. L. Laabs, H. M. Geller & M. R. Libera. 'Length-scale mediated adhesion and directed growth of neural cells by surface-patterned poly(ethylene glycol) hydrogels.' *Biomaterials* **30** (5), pp. 721–729 (2009)

[301] Y. Hong, P. Krsko & M. Libera. 'Protein Surface Patterning Using Nanoscale PEG Hydrogels.' *Langmuir* **20** (25), pp. 11123–11126 (2004)

[302] B. Brough, K. L. Christman, T. S. Wong, C. M. Kolodziej, J. G. Forbes, K. Wang, H. D. Maynard & C. Ho. 'Surface initiated actin polymerization from top-down manufactured nanopatterns.' *Soft Matter* **3** (5), pp. 541–546 (2007)

[303] R. Uchiyama, K. Kusagawa, K. Hanai, N. Imanishi, A. Hirano & Y. Takeda. 'Development of dry polymer electrolyte based on polyethylene oxide with co-bridging agent crosslinked by electron beam.' *Solid State Ionics* **180** (2-3), pp. 205–211 (2009)

[304] M. Ueno, N. Imanishi, K. Hanai, T. Kobayashi, A. Hirano, O. Yamamoto & Y. Takeda. 'Electrochemical properties of cross-linked polymer electrolyte by electron beam irradiation and application to lithium ion batteries.' *Journal of Power Sources* **196** (10), pp. 4756–4761 (2011)

[305] N. Aizaki. 'Proximity effect dependence on substrate material.' *Journal of Vacuum Science & Technology* **16** (6), pp. 1726–1733 (1979)

[306] S. Roddaro, A. Pescaglini, D. Ercolani, L. Sorba & F. Beltram. 'Manipulation of Electron Orbitals in Hard-Wall InAs/InP Nanowire Quantum Dots.' *Nano Letters* **11** (4), pp. 1695–1699 (2011)

[307] L. Romeo, S. Roddaro, A. Pitanti, D. Ercolani, L. Sorba & F. Beltram. 'Electrostatic Spin Control in InAs/InP Nanowire Quantum Dots.' *Nano Letters* **12** (9), pp. 4490–4494 (2012)

[308] X. Liu & T. Osaka. 'All-Solid-State Electric Double-Layer Capacitor with Isotropic High-Density Graphite Electrode and Polyethylene Oxide/$LiClO_4$ Polymer Electrolyte.' *Journal of The Electrochemical Society* **143** (12), pp. 3982–3986 (1996)

[309] S. K. Fullerton-Shirey & J. K. Maranas. 'Effect of $LiClO_4$ on the Structure and Mobility of PEO-based Solid Polymer Electrolytes.' *Macromolecules* **42** (6), pp. 2142–2156 (2009)

[310] C. D. Robitaille & D. Fauteux. 'Phase Diagrams and Conductivity Characterization of Some PEO-LiX Electrolytes.' *Journal of The Electrochemical Society* **133** (2), pp. 315–325 (1986)

[311] F. Croce, G. B. Appetecchi, L. Persi & B. Scrosati. 'Nanocomposite polymer electrolytes for lithium batteries.' *Nature* **394**, p. 456 (1998)

[312] Y. He, P. G. Boswell, P. Bühlmann & T. P. Lodge. 'Ion Gels by Self-Assembly of a Triblock Copolymer in an Ionic Liquid.' *The Journal of Physical Chemistry B* **111** (18), pp. 4645–4652 (2007)

[313] B. Rupp, M. Schmuck, A. Balducci, M. Winter & W. Kern. 'Polymer electrolyte for lithium batteries based on photochemically crosslinked poly(ethylene oxide) and ionic liquid.' *European Polymer Journal* **44** (9), pp. 2986–2990 (2008)

[314] J. Shin, W. A. Henderson & S. Passerini. 'PEO-based polymer electrolytes with ionic liquids and their use in lithium metal-polymer electrolyte batteries.' *Journal of The Electrochemical Society* **152** (5), pp. A978–A983 (2005)

[315] J. Lee, L. G. Kaake, J. H. Cho, X. Zhu, T. P. Lodge & C. D. Frisbie. 'Ion gel-gated polymer thin-film transistors: Operating mechanism and characterization of gate dielectric capacitance, switching speed, and stability.' *The Journal of Physical Chemistry C* **113** (20), pp. 8972–8981 (2009)

[316] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt & N. S. Wingreen. 'Electron Transport in Quantum Dots.' In: L. L. Sohn, L. P. Kouwenhoven & G. Schön (eds.), *Mesoscopic Electron Transport*. Kluwer, Boston, MA, USA (1997)

[317] I. M. Ruzin, V. Chandrasekhar, E. I. Levin & L. I. Glazman. 'Stochastic Coulomb blockade in a double-dot system.' *Physical Review B* **45** (23), pp. 13469–13478 (1992)

[318] A. C. Ford, J. C. Ho, Y. Chueh, Y. Tseng, Z. Fan, J. Guo, J. Bokor & A. Javey. 'Diameter-Dependent Electron Mobility of InAs Nanowires.' *Nano Letters* **9** (1), pp. 360–365 (2009)

[319] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan & K. C. Saraswat. 'Germanium nanowire field-effect transistors with SiO_2 and high-κ HfO_2 gate dielectrics.' *Applied Physics Letters* **83** (12), pp. 2432–2434 (2003)

[320] R. Scheibner, E. G. Novik, T. Borzenko, M. König, D. Reuter, A. D. Wieck, H. Buhmann & L. W. Molenkamp. 'Sequential and cotunneling behavior in the temperature-dependent thermopower of few-electron quantum dots.' *Physical Review B* **75** (4), p. 041301 (2007)

[321] H. Thierschmann, M. Henke, J. Knorr, L. Maier, C. Heyn, W. Hansen, H. Buhmann & L. W. Molenkamp. 'Diffusion thermopower of a serial double quantum dot.' *New Journal of Physics* **15** (12), p. 123010 (2013)

[322] K. Weis, S. Wirths, A. Winden, K. Sladek, H. Hardtdegen, H. Lüth, Detlev Grützmacher & T. Schäpers. 'Quantum dots in InAs nanowires induced by surface potential fluctuations.' *Nanotechnology* **25** (13), p. 135203 (2014)

[323] P. Mani, N. Nakpathomkun, E. A. Hoffmann & H. Linke. 'A Nanoscale Standard for the Seebeck Coefficient.' *Nano Letters* **11** (11), pp. 4679–4681 (2011)

[324] M. A. Ratner & D. F. Shriver. 'Ion transport in solvent-free polymers.' *Chemical Reviews* **88** (1), pp. 109–124 (1988)

[325] S. A. Hashmi, A. Kumar, K. K. Maurya & S. Chandra. 'Proton-conducting polymer electrolyte. I. The polyethylene oxide+NH_4ClO_4 system.' *Journal of Physics D: Applied Physics* **23** (10), p. 1307 (1990)

[326] D. M. DeLongchamp & P. T. Hammond. 'Highly ion conductive poly(ethylene oxide)-based solid polymer electrolytes from hydrogen bonding layer-by-layer assembly.' *Langmuir* **20** (13), pp. 5403–5411 (2004)

[327] A. E. Binks & A. Sharples. 'Electrical conduction in olefin oxide polymers.' *Journal of Polymer Science Part A-2: Polymer Physics* **6** (2), p. 407–420 (1968)

[328] P. Donoso, W. Gorecki, C. Berthier, F. Defendini, C. Poinsignon & M. B. Armand. 'NMR, conductivity and neutron scattering investigation of ionic dynamics in the anhydrous polymer protonic conductor $PEO(H_3PO_4)_x$.' *Solid State Ionics* **28–30, Part 2**, pp. 969–974 (1988)

[329] W. Gorecki, E. Belorizky, C. Berthier, P. Donoso & M. Armand. 'NMR investigation of $P(EO)(LiClO_4)_x$.' *Electrochimica Acta* **37** (9), pp. 1685–1687 (1992)

[330] G. Wang, L. Yang, J. Wang, H. Liu & S. Dou. 'Enhancement of Ionic Conductivity of PEO Based Polymer Electrolyte by the Addition of Nanosize Ceramic Powders.' *Journal of Nanoscience and Nanotechnology* **5** (7), pp. 1135–1140 (2005)

[331] S. Roddaro, K. Nilsson, G. Astromskas, L. Samuelson, L. Wernersson, O. Karlström & A. Wacker. 'InAs nanowire metal-oxide-semiconductor capacitors.' *Applied Physics Letters* **92** (25), p. 253509 (2008)

[332] F. Dyson. 'A meeting with Enrico Fermi.' *Nature* **427** (6972), pp. 297–297 (2004)

[333] J. Mayer, K. Khairy & J. Howard. 'Drawing an elephant with four complex parameters.' *American Journal of Physics* **78** (6), pp. 648–649 (2010)

[334] B. Ketterer, E. Uccelli & A. Fontcuberta i Morral. 'Mobility and carrier density in p-type GaAs nanowires measured by transmission Raman spectroscopy.' *Nanoscale* **4** (5), pp. 1789–1793 (2012)

[335] J. K. Lim, B. Y. Lee, M. L. Pedano, A. J. Senesi, J. Jang, W. Shim, S. Hong & C. A. Mirkin. 'Alignment Strategies for the Assembly of Nanowires with Submicron Diameters.' *Small* **6** (16), pp. 1736–1740 (2010)

[336] M. Lard, L. ten Siethoff, J. Generosi, A. Månsson & H. Linke. 'Molecular Motor Transport through Hollow Nanowires.' *Nano Letters* **14** (6), pp. 3041–3046 (2014)

[337] M. Collet, S. Salomon, N. Y. Klein, F. Seichepine, C. Vieu, L. Nicu & G. Larrieu. 'Large-Scale Assembly of Single Nanowires through Capillary-Assisted Dielectrophoresis.' *Advanced Materials* **27** (7), pp. 1268–1273 (2015)

[338] Y. Sone, P. Ekdunge & D. Simonsson. 'Proton Conductivity of Nafion 117 as Measured by a Four-Electrode AC Impedance Method.' *Journal of The Electrochemical Society* **143** (4), pp. 1254–1259 (1996)

[339] A. C. Ford, S. Chuang, J. C. Ho, Y. Chueh, Z. Fan & A. Javey. 'Patterned p-Doping of InAs Nanowires by Gas-Phase Surface Diffusion of Zn.' *Nano Letters* **10** (2), pp. 509–513 (2010)