Si-MOS Multiplexer and Depletion Mode Charge Sensor for Quantum Computation

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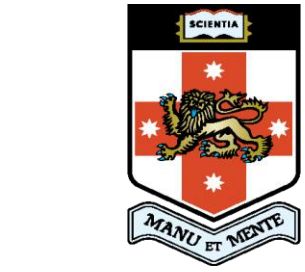

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Spin qubits based on silicon metal-oxide-semiconductor (Si-MOS) quantum dots represent a promising pathway to large-scale quantum computation. The development of these qubit devices at UNSW involves the testing of a large volume of devices in order to find those suitable to undertake detailed measurements at sub-Kelvin temperatures. Currently, only one device can be tested at a time during the preliminary screening process, which acts as a bottleneck in the development process. Another issue with these qubits is the impact of strain caused by the differential thermal expansion of the device components, which can modify the desired position of the quantum dots from their designed locations.

This thesis addresses both of the abovementioned issues and comprises two sub-projects. The first sub-project involves the development of a Si-MOS multiplexer, with the aim of improving efficiency by testing a number of devices in parallel during one screening session at 4 Kelvin. The second sub-project focuses on the development of a Si-MOS depletion-mode charge sensor which can be used as Single Electron Transistor (SET) sensor that has a reduced likelihood of forming unintentional quantum dots due to strain.

In the multiplexer study, device robustness was studied and leakages between n-type conducting leads ("n-fingers") were found on all tested samples. 74% of n-fingers had resistances in the MΩ regime due to high channel resistances of the addressing switches. SIMS analysis showed that this leakage resulted from p-type channel stop regions (between the n-fingers) that had a lower doping concentration and shallower profile than the target design. We therefore concluded that the fabrication process should employ ion implantation for making p-type channel stoppers, and redesign of the addressing switches structure.

Measurements of the depletion-mode charge sensors demonstrated that the device could be operated as an SET charge sensor, since electron charge transitions at a nearby quantum dot could be detected by this sensor through capacitive coupling. The two measured devices did not create strain-induced quantum dots, but there was not yet sufficient evidence to justify that this device architecture could significantly reduce the chance of forming these unintentional dots.

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ORIGINALITY STATEMENT

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Signed

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List of Abbreviations

AC	Alternative current
ALD	Atomic layer deposition
ANFF	Australia National Fabrication Facility
CPU	Central processing unit
CQC2T	Centre for Quantum Computation and Communication Technology
CTE	Coefficient of thermal expansion
DC	Direct current
EBL	Electron-beam lithography
ESR	Electron spin resonance
FET	Field-effect transistor
HF	Hydrofluoric acid
IPA	Isopropanol
MIBK	Methyl isobutyl ketone
PCB	Printed circuit board
PMMA	Poly methyl methacrylate
SEM	Scanning electron microscope
SET	Single electron transistor
Si-MOS	Silicon-metal-oxide-semiconductor
SIMS	Secondary ion mass spectrometry
SMU	Source measure unit
UNSW	The University of New South Wales
2DEG	Two-dimensional electron gas

Chapter 1
Introduction

In today's world, computers have become an indispensable tool due to their powerful capabilities to perform many types of tasks. Computers are not only widely used for daily tasks such as sending emails and browsing the Internet, but also for running complex modelling and simulations, processing large amounts of data and for design and rendering, to name but a few examples. Performing such complicated tasks requires very strong computational power, and as these tasks become increasingly complex, computers will be pushed beyond their limits and become ever faster.

The computational power of the digital computers we use daily is growing with the integration of more and more transistors – the basic building block of digital computers – onto a silicon chip known as the CPU. Today, these microprocessors have more than a billion transistors on a single chip. The number of transistors on a single chip has been predicted by Moore's law, which states that this number continues to double every 18 months [1]. In other words, computers will become more and more powerful by fitting more transistors on a chip, and the size of these transistors will become smaller and smaller. It is believed that by the year 2030 transistor size will reach the atomic scale, whereupon the logical next step is to build quantum computers [1].

Quantum computing is not simply a result of transistor size scaling down; it will utilise the quantum behaviours of subatomic particles to perform calculations and process certain tasks much faster than classical computers [2]. Today's digital computers work by manipulating bits in one of their two states: either 0 or 1. However, quantum computers encode information as quantum bits, or qubits, which can exist not only as 0 or 1 but also a superposition of 0 and 1 [1]. Figure 1.1 shows a graphical representation of a qubit termed the Bloch sphere. The two poles represent two classical bit states, 0 and 1, and a qubit can point to anywhere on this sphere, i.e. a superposition of the two states. This potentially allows quantum computers to store and process significantly more information than classical computers [2]. Moreover, unlike classical computers, which perform calculations in a sequential order, the superposition of qubits gives

quantum computers their inherent parallelism, so that they can simultaneously perform many calculations in parallel [1]. Hence, quantum computers are able to calculate much faster than classical computers.

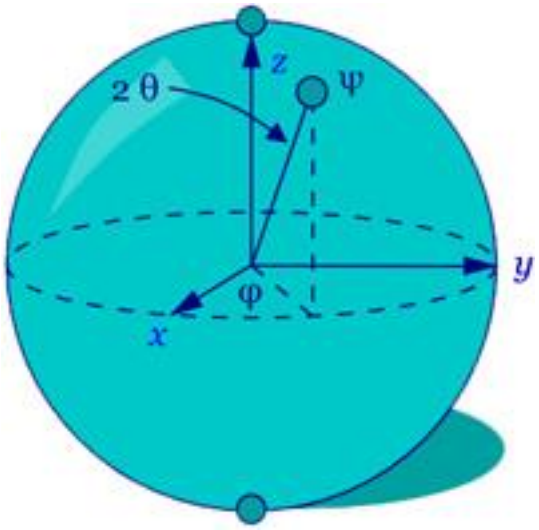


Figure 1.1: The Bloch sphere. A graphical representation of a quantum bit, or qubit.

1.1 Background

In quantum computation, qubits are usually controlled by their specific control devices depending on the different materials used. Researchers at CQC2T based at UNSW are attempting to build a quantum computer based on silicon, which is the most commonly used material in classical computers. Several research groups are working on projects from different approaches, such as precision qubit program, integrated silicon nanospintronics and quantum spin control [3], to explore the possibilities of constructing this silicon quantum computer. The precision qubit and quantum spin control programs utilise phosphorus atoms incorporated into silicon to realise qubits, while the integrated silicon nanospintronics program focuses on creating quantum dots to localise electrons which can then be manipulated as qubits. The research group which the candidate is belong to focuses on silicon quantum dot electron spin qubit manipulation.

Figure 1.2a shows an SEM image of a recent device structure that is used to control electron spin qubits [4]. It consists of four main parts, labelled as the electron reservoir, quantum dot qubit, SET and ESR line. All of these aluminium gate electrodes are fabricated on top of an isotopically purified silicon-28 substrate, using a multi-level gate-stack Si-MOS technology. The overlapping areas are insulated by the naturally grown aluminium oxide on the surface of the electrodes. The electron reservoir gate R is connected to an n-doped ohmic region, which forms a reservoir that supplies electrons to the quantum dot as qubits. Control gates G1–G4 can either be tuned to form a tunnel barrier between the reservoir and quantum dot, or used to capture and control an electron qubit. Confinement gate C creates a potential barrier at all the other dimensions (left, right and bottom in this image) at the qubit region, so that the quantum dot is confined. The SET is constructed by its top gate ST, left barrier gate LB and right barrier gate RB. The capacitive coupling between the SET island and the quantum dot enables the SET to be used as a charge sensor that monitors the quantum dot occupancy. The on-chip ESR line generates a time-varying magnetic field B_1 by passing through an AC at the ESR frequency, or I_{ESR} as labelled here, to alter the qubit orientation. All measurements are performed at the base temperature of $T \approx 50$mK in a dilution refrigerator, with a static magnetic field B_0.

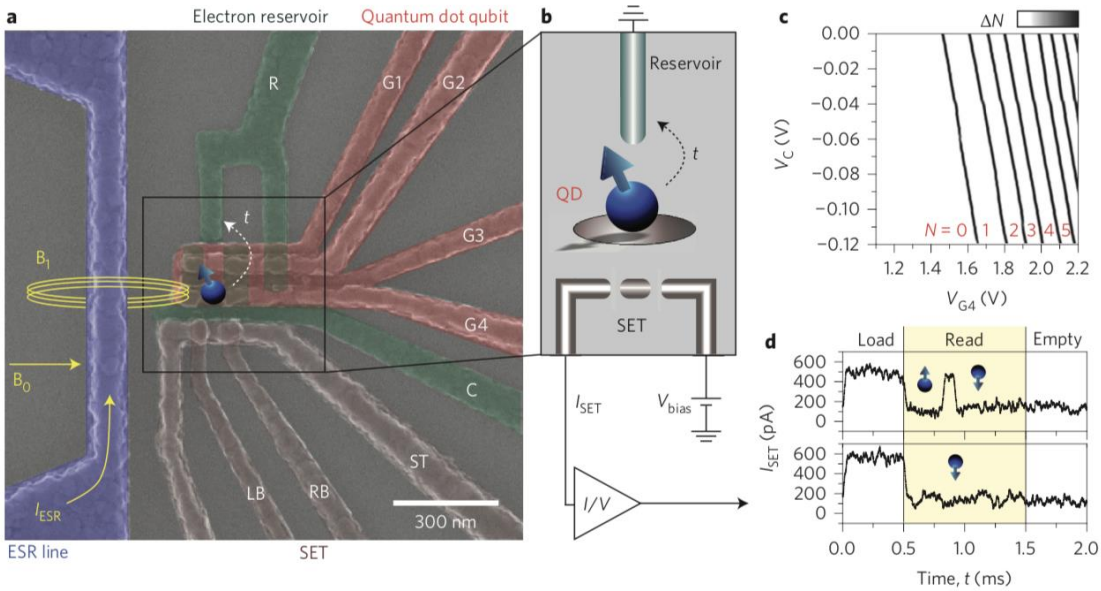


Figure 1.2: (a) SEM image of a qubit control device. Gate R acts as an electron reservoir and gate C confines the quantum dot at all dimensions except the reservoir side. Gates G1–G4 can operate as tunnel barriers or qubit control gates by appropriately biasing the gate electrodes. The

SET is used as a charge sensor to monitor the dot occupancy, and the ESR line generates a magnetic field to vary the spin qubit orientation. (b) Schematic diagram of the device. (c) Charge stability diagram showing SET readout of the quantum dot status to the last electron. (d) Single-shot spin readout measurement to determine the spin orientation from the dot. *Courtesy of Veldhorst et al., Nature Nanotechnology 9 (2014)*

The device shown here is operating in single quantum dot mode, where gate G4 is biased to control an electron qubit. Figure 1.2b shows the operation principle using a schematic diagram. An electron is able to quantum mechanically tunnel from the reservoir on the quantum dot when the dot is biased such that its energy level is lower than the reservoir Fermi-level. Figure 1.3 illustrates an explanation of this tunnelling event [5]. During the *Load* phase, the quantum dot energy level is tuned below the reservoir Fermi-level E_F so that an electron with random spin orientation can tunnel on the dot. To determine the spin orientation, we perform single-shot spin readout measurement via energy-selective tunnelling.

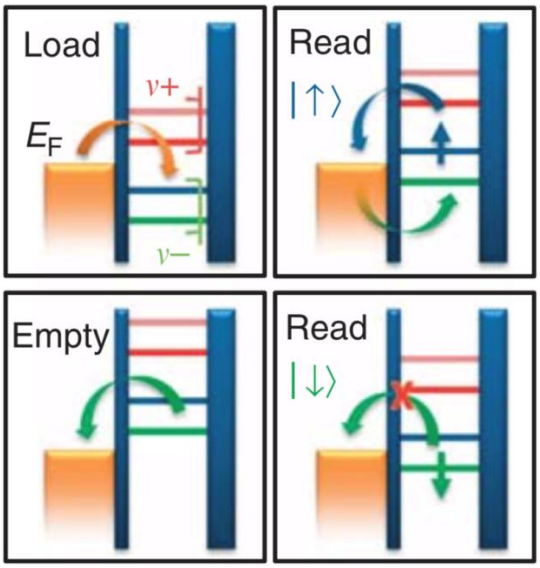


Figure 1.3: Schematic diagram showing the three-level pulsing sequence of the quantum dot. The spin orientation is determined by single-shot readout via energy-selective tunnelling. *Courtesy of Yang et al., Nature Communications 4: 2069 (2013)*

The applied static magnetic field B_0 Zeeman splits each electron energy level into two sub-levels. The higher level accommodates a spin-up electron, while the lower level is filled by a spin-down electron, and only one sub-level can be occupied by an electron at

any one time [5]. In Figure 1.3, the two sub-levels labelled blue and green are shown to be loaded/unloaded. During the *Read* phase, the dot energy level is adjusted such that the reservoir Fermi level sits between the spin-up and spin-down energy states. Therefore, if the electron in the dot is spin-up, it will tunnel off the dot while a spin-down electron tunnels on the dot simultaneously; otherwise, if it is a spin-down electron, it remains in the dot. By lifting the dot energy levels above E_F, all electrons will tunnel off the dot as in the *Empty* phase. The SET captures tunnelling events and indicates them as current peaks. This signal is fed into a transconductance amplifier for measurement clarity. The charge stability diagram in Figure 1.2c depicts how the quantum dot is plunged to the last electron, and Figure 1.2d shows a measurement result of the single-shot readout. A spin-up electron will tunnel off the dot and the SET detects this as a current peak. In contrast, no signal is detected for a spin-down electron.

These qubit devices have been extensively used in our group's experiments during recent years; however, they have certain limitations and issues in terms of the testing process and device structures. We can only test one device at a time and the SET can generate unintentional quantum dots due to its gating structure. This thesis consist of two sub-projects: (i)the Si-MOS multiplexer and; (ii)the depletion-mode charge sensor; both of which explore possibilities to resolve these issues, and concludes research findings that contribute to device improvement.

1.2 Motivation

Before starting measurements in a dilution refrigerator, each qubit device needs to pass a preliminary test called 4K dipping. This test is performed in a liquid helium dewar at T = 4K in order to characterise device behaviour at cryogenic temperature, and thus determine whether it is suitable for fridge measurement. Figure 1.5 shows a liquid helium dewar and a dip-stick with its electrical contacts layout. To carry out the test, a qubit device chip is attached and bonded up on a PCB, then the PCB is mounted at the bottom of the dip-stick. The electrical wires on the dip-stick are connected to the PCB pins and each PCB pin is individually matched to the electrical contact. Due to the

limited number of electrical contacts on the measurement setup, only one device can be tested in one cooldown session.

Figure 1.5: Liquid helium dewar and its dip-stick with electrical contact layout for 4K dipping.

Since the 4K dipping experiment is a quick test for device characterisation, and we are looking for a suitable device for fridge measurement from a large volume of devices, performing 4K dipping for one device at a time is not efficient. At the same time, we cannot alter the device structure nor the experimental setup. In this case, we propose the solution to employ a Si-MOS multiplexer to test multiple devices by selecting them individually in a single cooldown session.

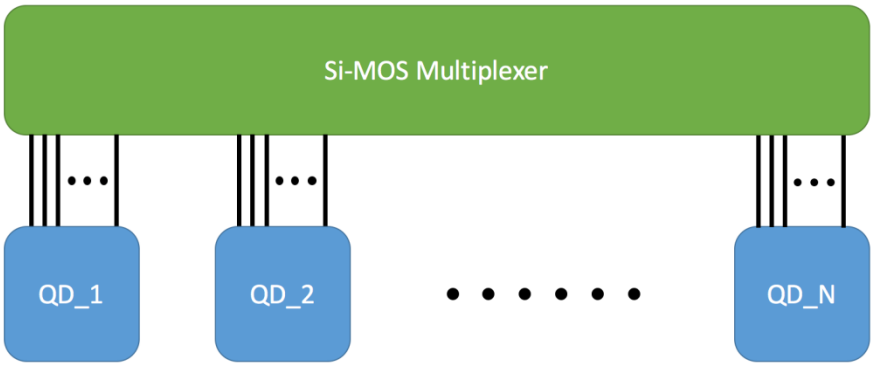


Figure 1.6: High-level schematic diagram of a Si-MOS multiplexer. The multiplexer is able to address and operate each quantum dot device individually. The number of electrical contacts fits the limitations on the measurement setup.

Figure 1.6 shows a high-level schematic diagram of a Si-MOS multiplexer. This device will allow a number of quantum dot qubit devices to be fabricated on-chip, and is able to address these qubit devices individually. It can also operate each gate electrode of a qubit device individually, while the number of electrical contacts is within the limitations of the experimental setup. The multiplexer will be compatible with current qubit devices, as they are all fabricated on the same base material – silicon. This will enable us to test devices at 4K more efficiently as multiple devices can be dipped in one session.

The depletion mode charge sensor project investigates problems associated with strain-induced quantum dots in silicon. Due to the gate design, fabrication and measurement process, it is often found that the quantum dot qubit devices described in Figure 1.2 would create unintentional quantum dots under gate electrodes randomly. One of the main causes of this issue is the strain created in the conduction band energy profile of the silicon substrate due to the different thermal expansion coefficients of the device materials. We focus on the SET readout device component of the architecture shown in Fig. 1.2 and study the strain related issues, modifying its design to seek improvements. Strain may arise from two factors: device fabrication and cryogenic operation [7]. During fabrication, growing oxides on material surfaces induces stress in the material, because thermally grown oxide expands in volume. Part of this expansion remains as compressive strain in the oxide [7]. Conversely, cooling devices to cryogenic temperature also creates strain. For silicon quantum dots, at the interface between different materials with different CTEs, the mismatch of CTEs will cause strain when devices are being cooled [7]. Figure 1.7 schematically shows thermal contraction of a Si-MOS structure with changes in the conduction band profile in silicon just below the metal/silicon interface at cryogenic temperature. Metals usually have larger CTEs than semiconductors, hence they contract more when cooled, but the semiconductor prevents metal from contracting near the interface, as shown in Figure 1.7b. This creates tensile elastic strain in the metal and compressive elastic strain in the silicon [7]. Consequently, the conduction band profile is affected and altered by these strains. Metal near the corners is more free to contract because it is further away from the interface, and this creates a high strain concentration at the corners. This raises the conduction band

beneath the corners in the silicon and forms peaks. The conduction band below the centre of the metal is lower since there is less strain. This change in conduction band profile can induce a quantum dot, which is known as a strain-induced quantum dot.

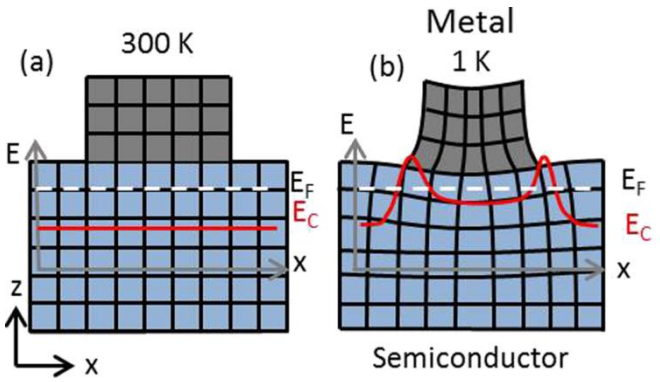


Figure 1.7: Schematic of a Si-MOS structure at: (a) room temperature and (b) cryogenic temperature. The conduction band energy profile in silicon directly below the interface is also plotted, showing peaks at the metal block corners caused by strain. *Courtesy of Thorbeck & Zimmerman, AIP Advances 5, 087107 (2015)*

The current SET design (shown in Figure 1.2a) has the top gate ST overlapping the two barrier gates LB and RB, which creates a complicated conduction band profile due to the gate-stacked architecture. It is difficult to avoid forming strain-induced quantum dots when devices are cooled to cryogenic temperature, which affects their performance. The depletion mode charge sensor project intends to verify whether we can minimise this effect by separating the ST gate and two barrier gates, while the modified device can still be operated as an SET in depletion mode. We will compare the experimental results of the original and modified devices, and justify whether the modified devices exhibit improved performance.

1.3 Thesis outline

This thesis consists of five main chapters, with the sub-sections in each chapter discussing experiments and results of different aspects.

Chapter 1 gives a brief introduction to quantum computation and recent breakthroughs of the UNSW silicon quantum dot research team. The Si-MOS multiplexer project and the depletion mode charge sensor project are also introduced with motivations.

Chapter 2 presents a literature review of several relevant research papers. The experimental methods and results presented in these papers are used as references for this thesis.

Chapter 3 discusses the Si-MOS multiplexer project, including its design, a series of tests and their relevant issues, and discussion and analysis of the results.

Chapter 4 explores the depletion mode charge sensor project in terms of device fabrication, 4K dipping and dilution refrigerator measurement.

Chapter 5 concludes all of the work presented in this thesis. Further research on these projects is also suggested in this chapter.

Chapter 2
Literature review

This chapter discusses several published articles on relevant work done by other research groups. Research activities carried out in this thesis refer to the content mentioned in the following studies. In this chapter, Al-Taie *et al.* and Puddy *et al.* are reviewed regarding the Si-MOS multiplexer project, and all other papers are used as references for the depletion mode charge sensor project.

2.1 Multiplexer for split-gate devices

Al-Taie *et al.* [8] present an on-chip multiplexing device for measuring an array of 256 split gates in a cryogenic environment. The multiplexer is fabricated on the surface of a GaAs/AlGaAs heterostructure with a layout of 16 rows by 16 columns (total of 256) of split gates integrated onto the same chip. The reason for choosing split gates as a testing device for the multiplexing scheme is that the split gate is one of the simplest quantum devices to operate. Using split gates can effectively reduce errors associated with the testing devices, while their quantum mechanical phenomena can still be observed in a cryogenic environment. Therefore, this is the best option to verify the operational yield of the multiplexer.

The aim of the multiplexing scheme is to achieve a large volume of device measurements via a cryogenic setup with limited electrical contacts in a single cooldown [8]. Due to the fact that the number of contacts available on the current cryostat setups is usually limited to 20–30 pads, it is impossible to measure a large number of devices, as devices require many contacts during one cooldown session. In order to overcome this limit, an on-chip multiplexer is developed such that devices can be individually addressed via the multiplexer. In this case, a multiplexer that required 19 contacts, including sixteen addressing gates, two contacts for the source and drain, and one contact for the control voltage was used to control and operate 256 split gates. Figure 2.1c shows an optical microscopic image of the entire device [8]. The source,

drain and control voltage are labelled S, D and V, respectively. The eight addressing gates on the source side multiplex any of the 16 rows, and the other eight addressing gates on the control voltage side select any of the 16 columns. Hence, each of the 256 split gates can be individually addressed via its corresponding row and column by correctly biasing these addressing gates. The control voltage V is passed towards the addressed split gate via the top multiplexer. A 100μV AC excitation is applied to the source to drain via a two-terminal lock-in amplifier, and the conductance of the split gate is measured. All gates were patterned by optical lithography, whereas the split gates were defined by EBL. The measurements were performed in a dilution refrigerator at the temperature of T = 1.4K.

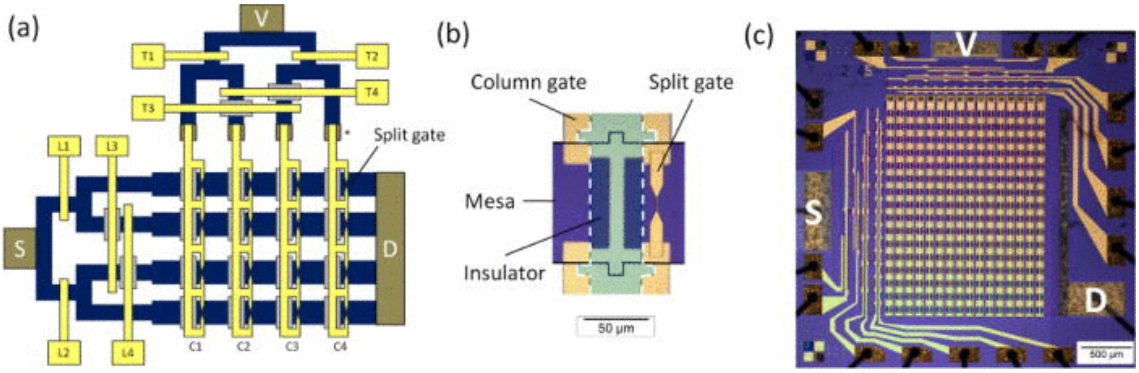


Figure 2.1: (a) Simplified schematic diagram of the device with a 4×4 layout [8]. Addressing gates L1–L4 direct an AC excitation voltage from source to drain through the selected 2DEG. Addressing gates T1–T4 direct the control voltage V to columns C1–C4. An individual split gate is then addressed and measured by multiplexing its corresponding row and column. (b) Microscopic image of a split gate [8]. The white-dotted area indicates the insulator region. (c) Microscopic image of the 256 split gate multiplexer [8]. All gates are shown in yellow. *Courtesy of Al-Taie et al., Applied Physics Letters 102, 243102 (2013)*

A three-level schematic diagram is drawn to explain the operational principle of the multiplexer, as shown in Figure 2.2 [8]. The 2DEG is defined using standard etching techniques, forming a three-level multiplexing system with eight output paths. G1 to G6 form the addressing gates, and by negatively biasing these gates, electrons below the corresponding gates are depleted and hence block the current paths. Insulators are also placed at the regions where the addressing gate voltages are bypassed, i.e. electron paths underneath these regions are not depleted, as the insulating dielectrics shift the voltage

required to deplete the 2DEG. In this diagram, gates G2, G4 and G6 are turned on, i.e. a negative voltage is applied such that only path 1 is addressed. On the first level, G2 depletes the 2DEG on the right-hand side path so that the only viable path to the second level is the left-hand side path. G4 then depletes the 2DEG at points A and C, blocking the right-hand side paths on the second level. Note that point B has an insulator placed between addressing gate G4 and the 2DEG path, preventing the depletion from occurring. Hence, the only viable path is now the further left-hand side path at level two. Similarly, G6 depletes the right-hand side 2DEG paths at level three, and finally the control voltage V is only directed through path 1. With this multiplexing structure, the control voltage V can be directed towards any path with the combination of addressing gates G1 to G6 being on or off.

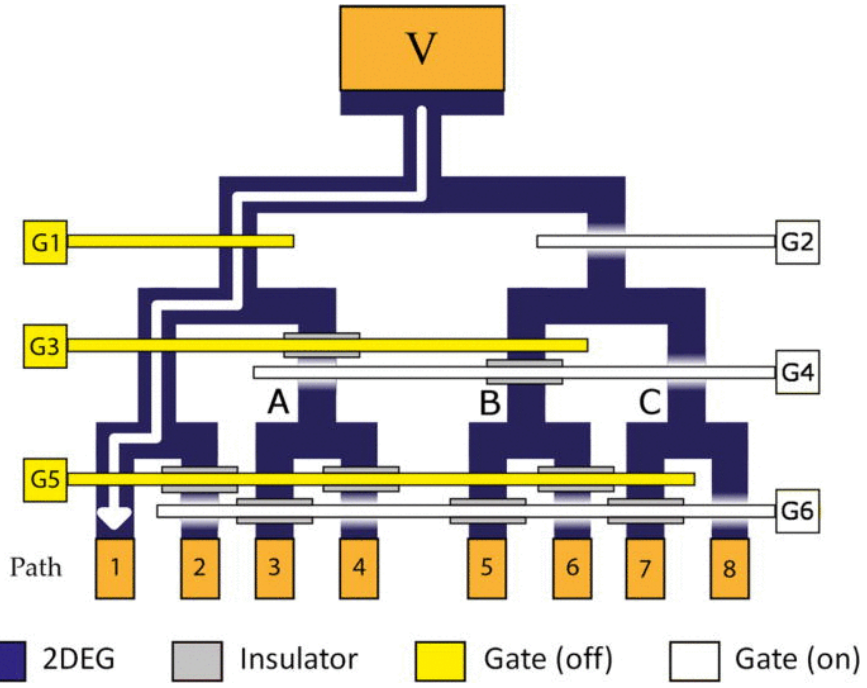


Figure 2.2: Simplified three-level schematic diagram of the multiplexer [8]. The 2DEG branches form eight output paths and direct the control voltage V to the addressed output. Addressing gates G2, G4 and G6 are turned on to deplete the 2DEG underneath so that the control voltage V is directed to path 1, as indicated by the arrow.
Courtesy of Al-Taie et al. Applied Physics Letters 102, 243102 (2013)

Figure 2.1a shows a simplified schematic diagram of the multiplexer in a 4×4 layout for illustration purposes. Addressing gates L1 to L4 select the desired row, and T1 to T4

select the desired column. Hence, each of the 16 split gates can be individually addressed. Insulators are also deposited below the column arms to prevent the 2DEG from being depleted. Figure 2.1b shows a microscopic image of a split gate. The 2DEG mesa is indicated by black lines, and the white-dotted lines outline the insulator.

The sample studied in this publication has 15 failed split gates due to damages incurred during fabrication. The fabrication yield is therefore Y_f = 94%. A quantum yield is also defined by the number of split gates for which the first and second conductance peaks are clearly seen [8]. In this experiment, the quantum yield is measured as Y_q = 86.3%. The total yield is therefore $Y_t = Y_f \times Y_q$ = 81.3%.

This paper demonstrates a multiplexing scheme that allows a large number of devices to be measured on a single chip with limited electrical contacts on the existing cryostat. Quantum phenomena on the split gates can also be measured at a high yield, which demonstrates the reliability of the multiplexer. This enables measurements with a large volume of devices to be performed during one cooldown session, which leads to a systematic study of the yield, device characteristics and statistical analysis of quantum phenomena.

2.2 Multiplexing charge-locking devices

Puddy *et al.* [9] demonstrates a modified version of the multiplexer mentioned previously in Al-Taie *et al*. Here, the previous testing devices, split gates, were used as a component to construct the addressing system of the multiplexer. Figure 2.3 shows a schematic diagram of a single-level three-way multiplexer. A 2DEG is divided into three channels with addressing gates G1 and G2 passing over the left and right channels, either directly on top of the GaAs/AlGaAs surface, or separated by an insulating dielectric. Both G1 and G2 form split gates above the central channel. The voltages required to deplete the 2DEG below the surface gates and split gates are defined as V_{surf} and V_{sg}, respectively. The split gate width is chosen such that $V_{sg} < V_{surf}$, and subsequently pinching off the 2DEG under the surface gates will have negligible effects on the 2DEG conductance under the split gates. Furthermore, the thickness of the

dielectric is set to bypass the addressing gate depletion effects on the 2DEG. The voltage combinations of G1 and G2 required to individually address each of the three channels are written in the three dashed boxes below the corresponding outputs. For example, V_{G1} = 0V opens all three paths where G1 is crossing, but $V_{G2} = V_{sg}$ pinches off the 2DEG at both the central and right channels. Hence, only the left channel is addressed in this case.

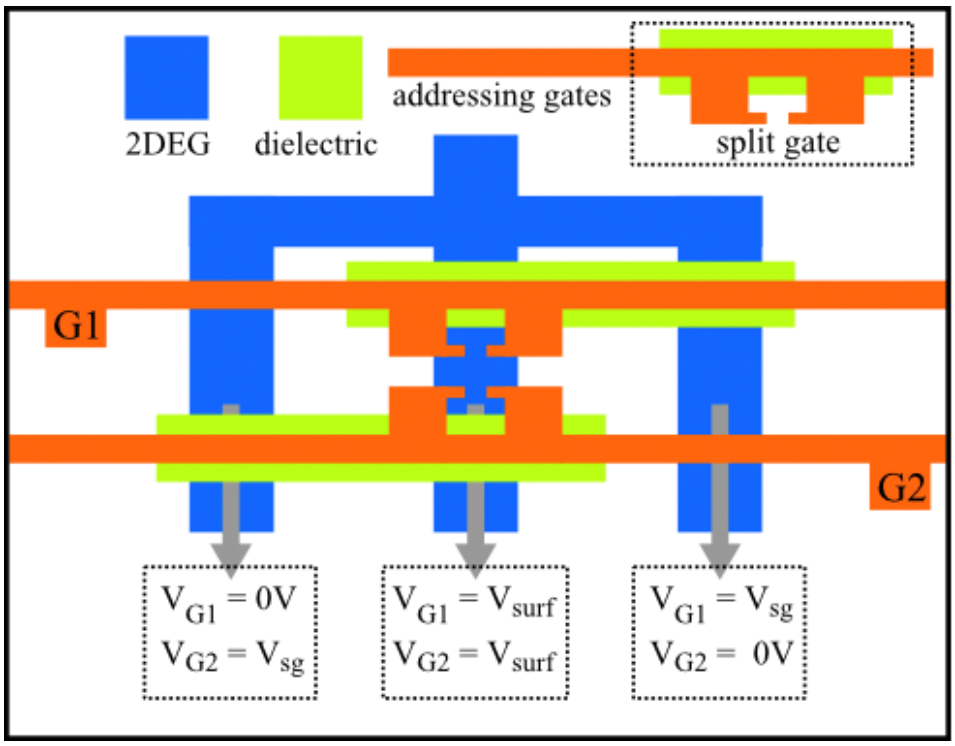


Figure 2.3: Schematic diagram of a three-way multiplexer [9]. Addressing gates G1 and G2 either pass over the 2DEG branches, or are separated by the insulating dielectrics. Both G1 and G2 form split gates above the central branch. The split gate dimension is designed such that their pinch-off voltage is lower than the surface gates' pinch-off voltage, i.e. $V_{sg} < V_{surf}$. The dielectric thickness is chosen to bypass the depletion effect of G1 and G2. The voltages required to address each of the three channels are shown in the three dashed boxes, respectively. *Courtesy of Puddy et al., arXiv: 1408.2872v2 (2014)*

A charge-locking system is described with a schematic diagram in Figure 2.4 [9]. This system consists of three 2DEG parts, labelled as ① the multiplexer 2DEG, ② the gate source 2DEG and ③ the measurement 2DEG. Each multiplexer output connects to an ohmic contact, which then connects to a surface gate defined as a locking gate, labelled

as ⓐ at the right output branch as an example. The gate source 2DEG consists of a main channel and three sub-channels, where the main channel is covered by the dielectric. The 2DEG shape under this dielectric is indicated by the dotted lines. Each sub-channel has a locking gate deposited on top and an ohmic contact connected at the end. Three surface gates then individually connect the ohmic contacts to the measurement 2DEG. The gate on the right is labelled as ⓑ for illustration purposes.

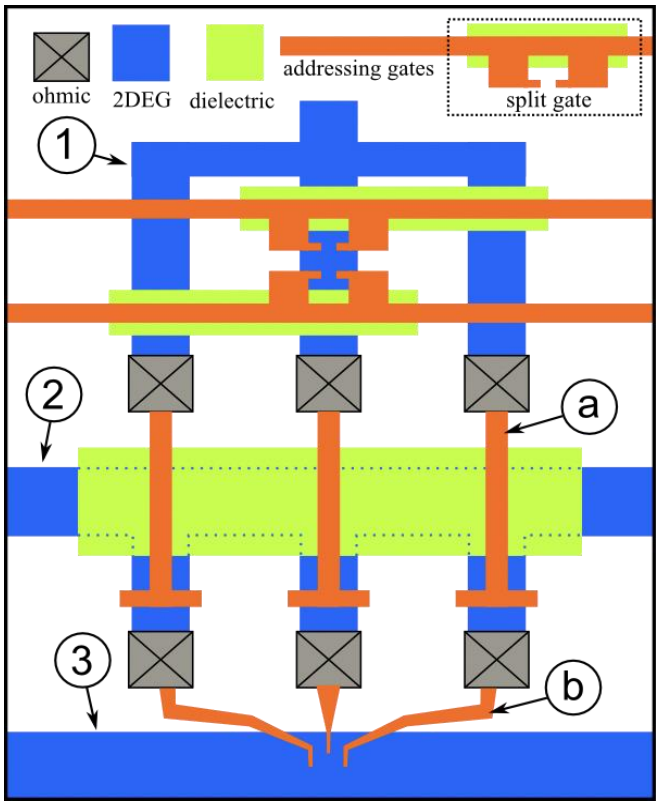


Figure 2.4: Schematic diagram of a charge-locking device with: (1) the multiplexer 2DEG, (2) the source gate 2DEG and (3) the measurement 2DEG [9]. Three locking gates, with one labelled (a), individually connect the multiplexer outputs and source gate 2DEG sub-channels, where the main channel is insulated by a dielectric layer. The measurement 2DEG is connected to the three sub-channels via the ohmic contacts and surface gates, with one labelled (b). *Courtesy of Puddy et al., arXiv: 1408.2872v2 (2014)*

The four operation stages of charge-locking are depicted in Figure 2.5 [9]. A locking voltage V_{lock} is defined, which is set well beyond the surface gate depletion voltage V_{surf}. In Figure 2.5a, the device is initialised by setting the control voltage and addressing gates to V_{lock}. This depletes the 2DEG of all three sub-channels, hence disconnecting

the gate source 2DEG and measurement 2DEG. Next, in Figure 2.5b, addressing gates are set to a voltage V_{dblock} that is well beyond the split gates' pinch-off voltage V_{sg}. This step blocks out all 2DEG paths of the multiplexer. The left path is then addressed as shown in Figure 2.5c, by setting the control voltage and the top address gate to 0V. This sets the left locking gate to 0V and reconnects the left sub-channel to the main channel. Now, only one channel is addressed and can be swept to the desired voltage via the gate source 2DEG. Finally, in Figure 2.5d the control voltage is set back to V_{lock} while maintaining the gate source voltage. This disconnects the sub-channel 2DEG and locks the charges at the measurement 2DEG side. The top addressing gate is then set back to V_{dblock} so that the operations shown in Figures 2.5b–d can be repeated to address and vary the status at any channel.

A microscopic image of a charge-locking device multiplexer is shown in Figure 2.6a [9]. This device is fabricated on a GaAs/AlGaAs substrate in a two-way mirror layout. It comprises two opposite-facing multiplexers, each with 16 outputs. However, split gates are not used to construct addressing gates here. The architecture of the multiplexers is identical to that mentioned previously in section 2.1.

The central region is shown in the SEM image in Figure 2.6b, together with the measurement setup. Two quantum dot arrays are patterned via EBL with each array containing seven dots, separated by a central gate. Only fifteen outputs from each multiplexer are used to address and control these quantum dots. The minimum separation between the control gates is approximately 20nm and the dot diameter is designed to be 300nm. The central gate also forms two measurement 2DEG channels so that the two quantum dot arrays can be independently measured via sources and drains, or S1/D1 and S2/D2, respectively. Note that the first three addressing gate levels are shared between the multiplexers to minimise contact numbers. All measurements are performed at 50mK, which is the base temperature of the dilution refrigerator.

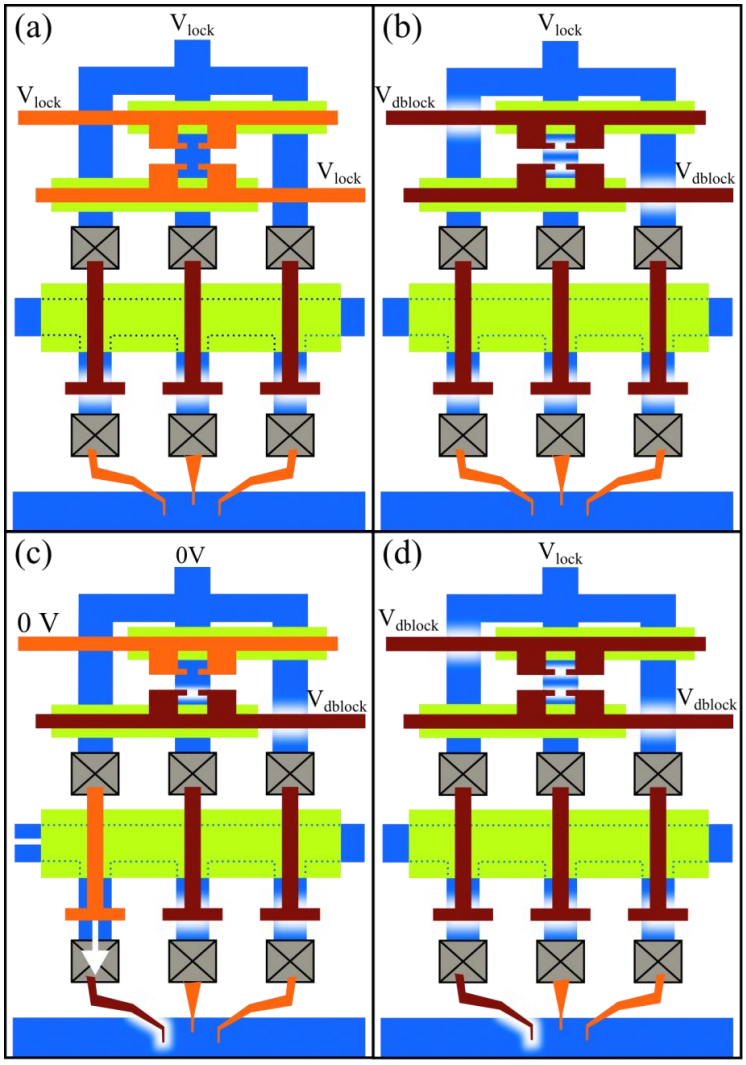


Figure 2.5: Schematic diagrams showing the four operation stages of the charge-locking device [9]. (a) Control voltage and addressing gates are set to V_{lock}, closing all sub-channels of the gate source 2DEG. (b) Addressing gates are set to V_{dblock}, closing all paths of the multiplexer. (c) The left locking gate is addressed by setting the control voltage and top address gate to 0V. The left sub-channel reconnects to the main channel of the gate source 2DEG and the voltage can be swept to a desired value. (d) The control voltage is set to V_{lock} so that the left sub-channel is blocked. Charges are locked at the measurement 2DEG and addressing gates are set back to V_{dblock}. This procedure is then repeated for the next channel.

Courtesy of Puddy et al., arXiv: 1408.2872v2 (2014)

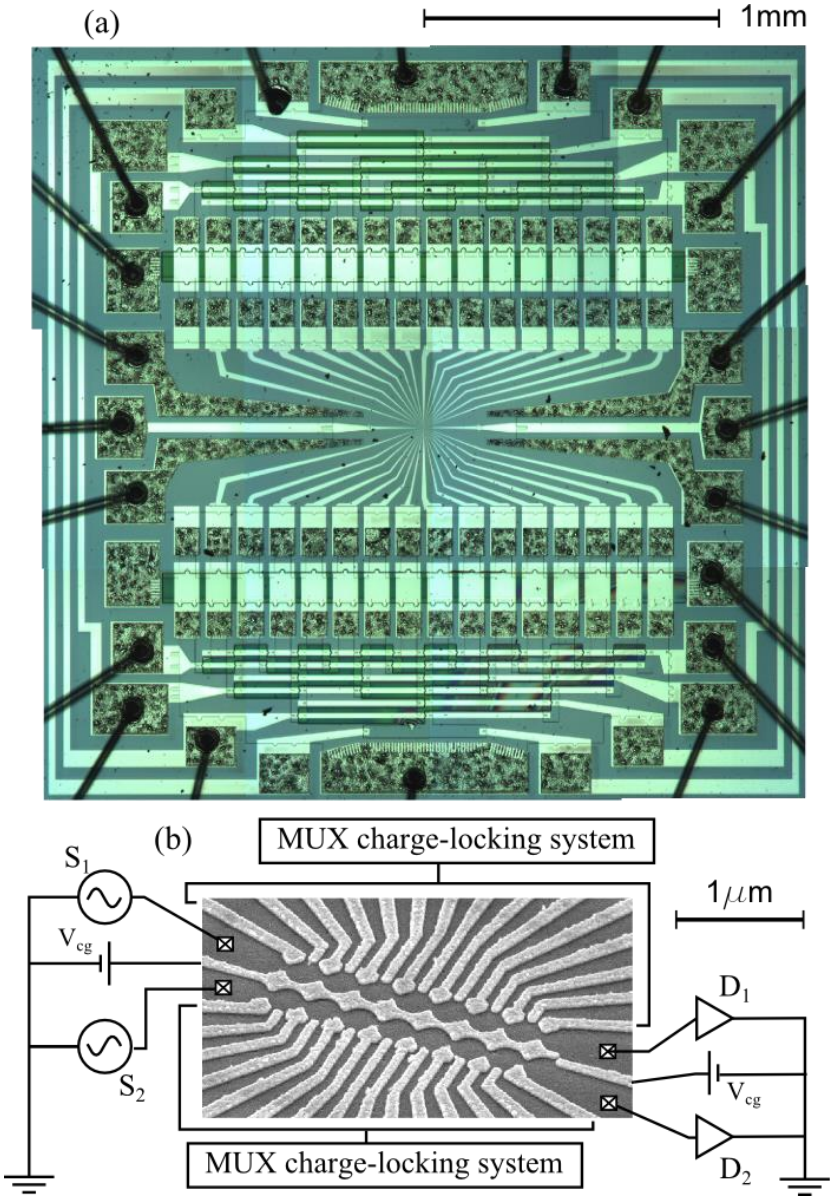


Figure 2.6: (a) Optical microscopic image of two 16-output opposite-facing multiplexers [9]. The first three addressing gate levels are shared to minimise contact numbers. (b) SEM image of the device central region and measurement setup. Two quantum dot arrays are separated by a central gate and measured via S1/D1 and S2/D2, respectively. Each multiplexer can individually address and control any of the dots within an array.

Courtesy of Puddy et al., arXiv: 1408.2872v2 (2014)

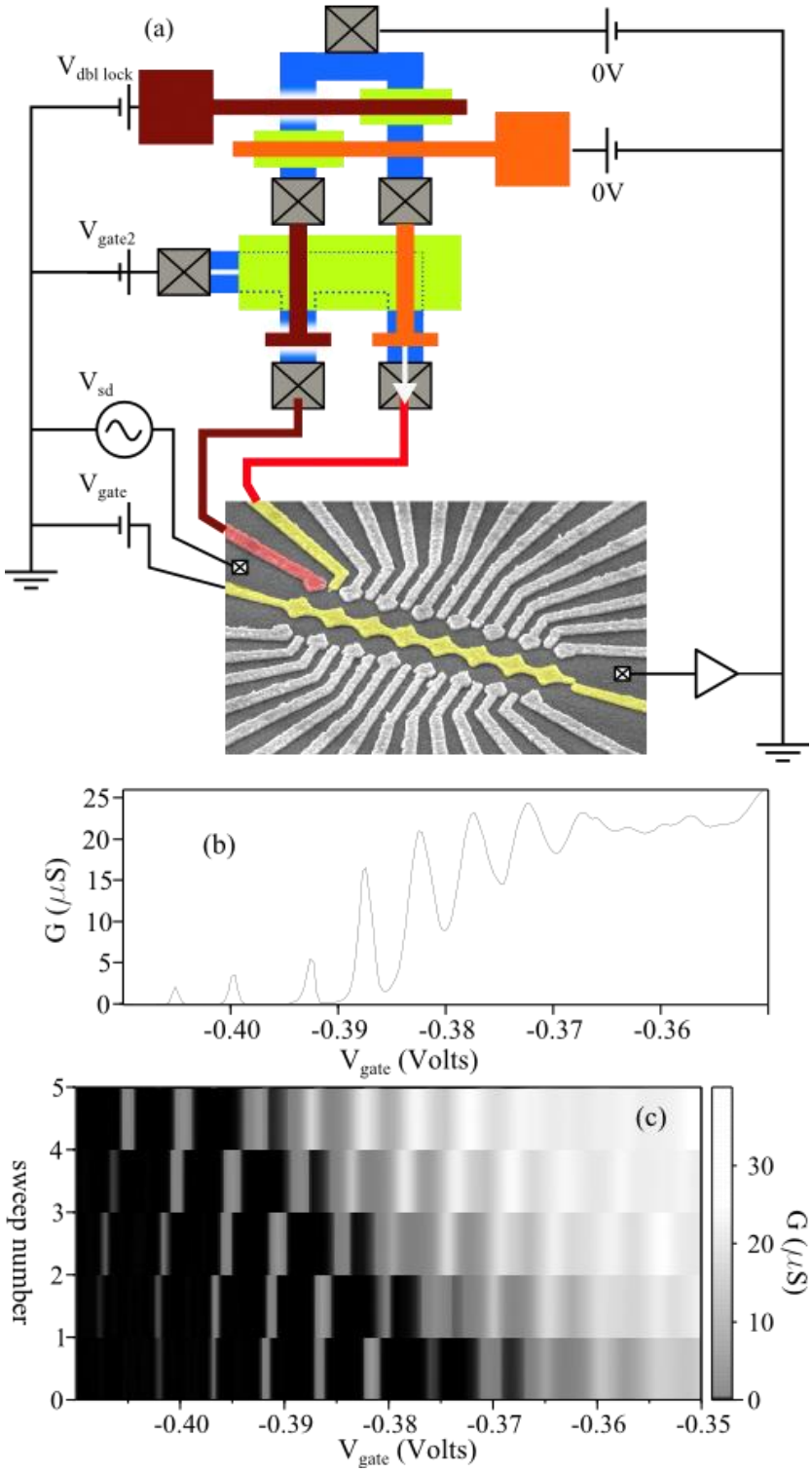


Figure 2.7: (a) Partial measurement circuit diagram. Control gate 1 is charge-locked at -0.4V and gate 2 is addressed. The central gate is held at -0.5V to isolate two measurement channels. (b) Conductance as a function of control gate 2 voltage, showing Coulomb peaks. (c) 2D greyscale plot of five measurements by sweeping control gate 2 at one-hour intervals [9]. *Courtesy of Puddy et al., arXiv: 1408.2872v2 (2014)*

During the measurement, the central gate is fixed at V_{gate} = -0.5V in order to separate the two measurement channels by depleting the 2DEG in-between. A single quantum dot is addressed following the procedure presented in Figure 2.5, and the conductance G is measured as a function of the control gate voltage V_{dg}. Figure 2.7a shows a partial circuit diagram of this measurement. Control gate 1 is charge-locked at -0.4V, forming a tunnel barrier between the source and the first quantum dot. Control gate 2 is addressed so that the second output can be swept by varying V_{gate2} and hence changing the potential at the first dot. Figure 2.7b shows the Coulomb peaks when sweeping control gate 2. This measurement is repeated five times with a one-hour interval between each sweep. A 2D greyscale plot shows the result in Figure 2.7c, which also shows a drift in the Coulomb peak voltages over time during repeated measurement.

In summary, this paper demonstrates a modified multiplexer design by implementing split gates on the addressing gates. This allows more multiplexing paths to be introduced at the same addressing level. Charge-locking devices are also fabricated on-chip and measured via the multiplexer. The charge locking mechanism demonstrates a solution for preserving and overwriting a controlled state via a multiplexing scheme. Quantum dot arrays are chosen as the charge-locking device in this experiment, and the characteristics of quantum dots are observed.

2.3 Gate-defined silicon quantum dots

Angus *et al.* [10] reports experiments on two devices with quantum dots created by tuneable electrostatic potential barriers and a narrow-channel FET in silicon. Unlike the GaAs quantum dots mentioned in the previous section, which are defined by the depletion of 2DEG, silicon quantum dots are formed by accumulating 2DEG under gate electrodes. In this paper, high-resistivity near-intrinsic silicon was used as the substrate for fabrication. Ohmic contact regions were defined via phosphorus diffusion. A 5nm SiO_2 gate oxide was grown on the Si surface via thermal oxidation. Two aluminium barrier gates were fabricated using EBL, thermal evaporation and lift-off, forming the first layer of the device. These gates were partially oxidised in an oxygen plasma for 3 minutes at around 150°C so that an ultra-thin aluminium oxide was formed on the

surface. The top gate was aligned to the barrier gates during the second EBL stage, again followed by thermal evaporation and lift-off. The top gate was insulated to the barrier gates by the aluminium oxide, forming the second layer of the device. The final process was forming gas annealing at 400˚C for 15 minutes, which reduced the interface trap density. An SEM image and cross-section of the device is shown in Figures 2.8a and 2.8b, respectively. The barrier gates are normally 30nm wide, separated by a distance *d* of about 40nm. The widths of the two devices reported in this paper are 60nm and 100nm.

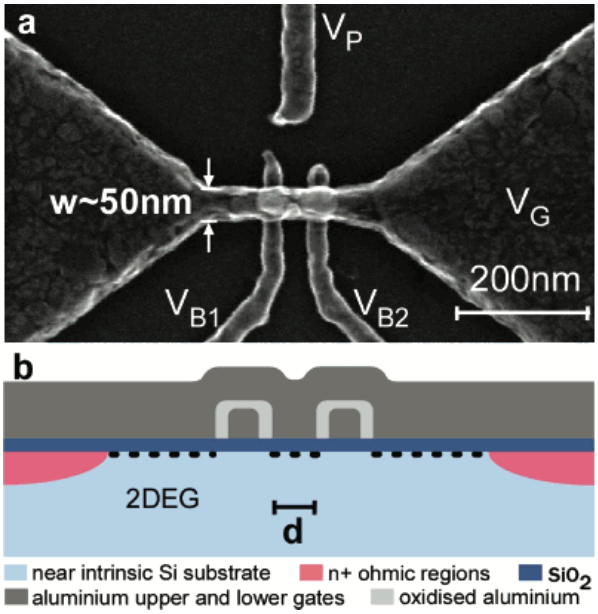


Figure 2.8: (a) SEM image of the device. The top gate V_G overlaps the two barrier gates V_{B1} and V_{B2}. Gate V_P is not used in this experiment. (b) Cross-section illustrating a 2DEG accumulated under the top gate and locally depleted by the barrier gates at the Si/SiO_2 interface [10]. *Courtesy of Angus et al., Nano Letters Vol.7, No.7, 2051-2055 (2007)*

Electrical transport measurements were performed in a dilution refrigerator at the base temperature of ~100mK. Two-terminal conductance and differential conductance through these dots were measured using low-frequency lock-in techniques at zero magnetic field. Figure 2.9 shows the global turn-on and barriers' pinch-off device characteristics. To measure the turn-on, a voltage was applied to all three gates simultaneously and thus induced a 2DEG channel between the source and drain ohmics. This characteristic is shown in Figure 2.9a with two curves representing the results of an annealed and unannealed device, respectively. Clearly, the annealed device gives a

lower threshold voltage and higher conductance, which confirms that a forming gas anneal is essential. Figure 2.9b shows the pinch-off characteristic of both barriers separately. Only one barrier was measured at a time, with the top gate and the other barrier held well above the threshold voltage in order to isolate the barrier effects. These results show that both barriers have a very sharp pinch-off effect, which can be tuned from highly transparent to fully opaque.

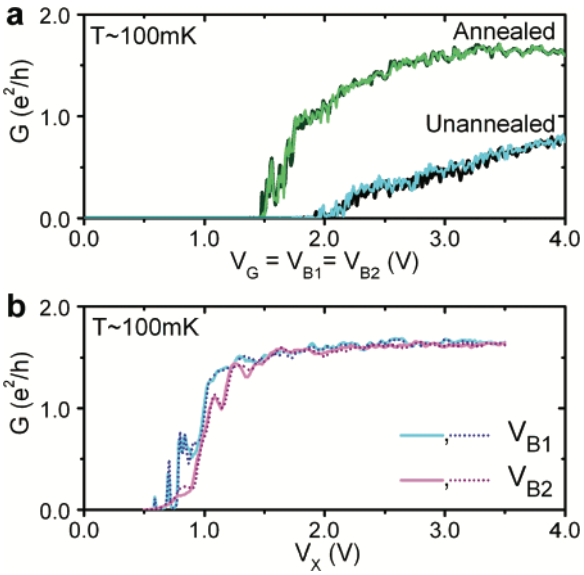


Figure 2.9: (a) Global turn-on characteristics for an annealed and unannealed device, showing that the annealed device gives a lower threshold voltage and a higher conductance. (b) Pinch-off characteristics of both barriers measured independently while top gate and the other barrier were held well above the threshold voltage. Both barriers have sharp pinch-off effects [10].
Courtesy of Angus et al., Nano Letters Vol.7, No.7, 2051-2055 (2007)

The combined effects of the top gate and both barriers on the source-drain conductance are illustrated in Figure 2.10. Figure 2.10a shows the Coulomb oscillation of the quantum dot with a 50 μV lock-in AC excitation applied to the source/drain and the barriers biased at V_{B1} = 0.43 and V_{B2} = 0.37. Figure 2.10b illustrates the relationship of the top gate and the barriers. The current is zero when the top gate is below its threshold value or when the barriers are opaque. At non-zero current regions, a Coulomb blockade with constant period is observed over a large biasing range. Figure 2.10c shows a magnified region of the small box in Figure 2.10b, which shows that a single quantum dot can be formed by the highly tuneable barriers over a wide range of biases. Oscillations shown here correspond to the electron occupancy at that region.

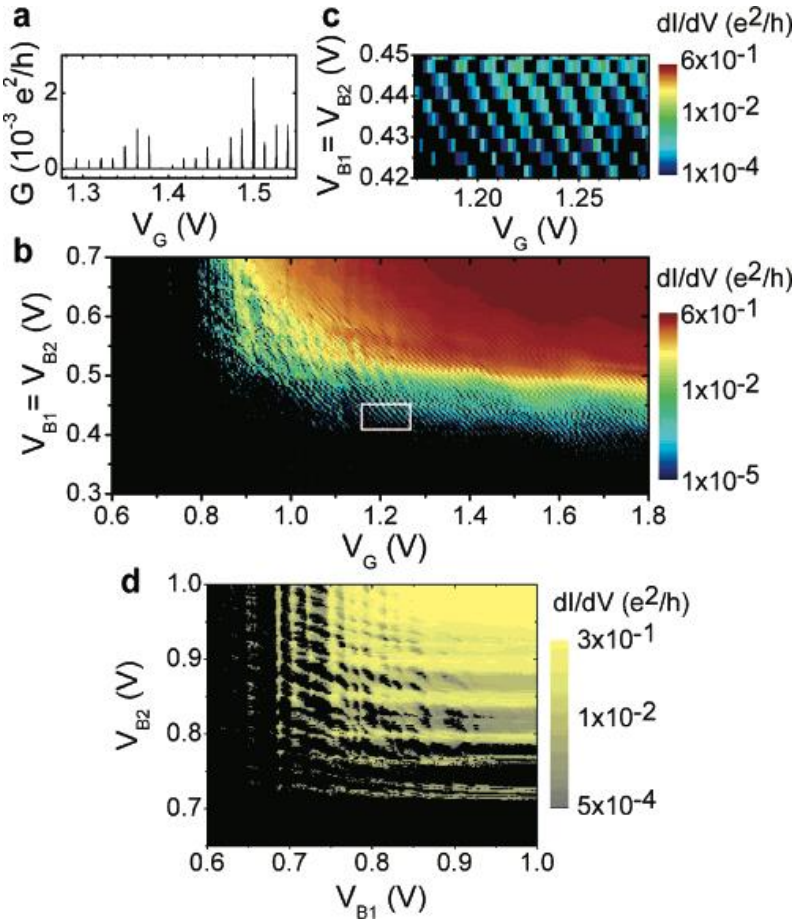


Figure 2.10: (a) Coulomb oscillations measured by AC biasing the source/drain and sweeping the top gate, where the barriers are tuned to V_{B1} = 0.43 and V_{B2} = 0.37 [10]. (b) Differential conductance as a function of the top gate and the barrier gates. (c) Enlarged region of the small box in (b). The slope of these lines indicates the dot dependency of all gates. (d) Differential conductance as a function of both barrier gates, measured at V_G = 1.3V.
Courtesy of Angus et al., Nano Letters Vol.7, No.7, 2051-2055 (2007)

Figure 2.10d shows the quantum dot dependency of each barrier measured at V_G = 1.3V. Diagonal lines in the plot indicate that Coulomb blockade is equally coupled to each barrier due to the centrally located dot. Vertical lines and horizontal lines at other regions show that the dot is strongly coupled to B1 and B2, respectively.

Coulomb diamonds are also probed by measuring the conductance as a function of an applied DC bias to the source/drain and the top gate voltage, as shown in Figure 2.11. Measurement results for sample 1 with a dot area of 30nm × 105nm, and sample 2 with a dot area of 35nm × 65nm, are plotted in Figures 2.11a and 2.11b, respectively. Constant Coulomb blockade periods are observed in both figures, further confirming

that a single quantum dot is centrally defined. Sample 1 gives a charging energy of 2.5meV, where sample 2 has a charging energy of 2–4meV. This verifies that a smaller dot size would provide a larger charging energy. Figure 2.11c shows that the total capacitance of the dot and top gate is approximately linearly dependent. This capacitance increases as the dot size increases.

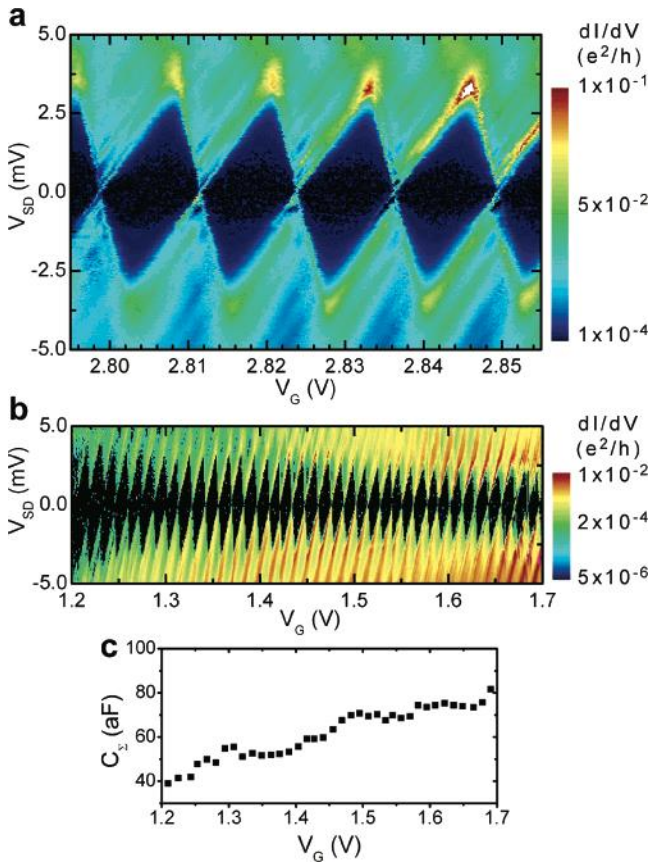


Figure 2.11: (a) Coulomb diamonds of sample 1 probed at $V_{B1} = V_{B2} = 0.85V$, lock-in excitation at 20μV in many-electron regime, $N \approx 100$; (b) sample 2 at $V_{B1} = 0.43V$, $V_{B2} = 0.37V$, lock-in excitation at 50μV. (c) Total capacitance of sample 2 as a function of top gate voltage [10]. *Courtesy of Angus et al., Nano Letters Vol.7, No.7, 2051-2055 (2007)*

In conclusion, this paper presents a fabrication technique and measurements of single quantum dots with tuneable barriers in intrinsic silicon. Quantum dot confinement is demonstrated from these results. This structure enables further investigation of many fundamental properties of silicon quantum dots. Furthermore, quantum dot confinement could lead to further experiments on single-spin manipulation and measurement.

2.4 Charging sensing and spin information

Yang *et al.* [11] investigate the excitation energy spectra for a nearly closed silicon quantum dot, in order to access whether these quantum devices are compatible for developing spin-based quantum computing. Figure 2.12a shows an SEM image with the pulse-bias spectroscopy experimental setup. Here the device uses an SET as a charge sensor for probing the occupancy of the quantum dot in its vicinity. Gate LD is connected to an n-type ohmic, which forms a 2DEG reservoir to supply electrons for the quantum dot. The top gate P defines and controls the electrostatic potential of the dot, and gates LB and RB are used for confinement. The SET is fabricated close enough to the dot such that it creates a capacitive coupling between the SET dot and the measurement dot. This SET is biased by the sensor lock-in amplifier with a small AC signal at frequency f_s through a pre-amplifier. The sensor lock-in current is tuned to the edge of a Coulomb peak in order to obtain a high transconductance for optimal sensitivity. The top gate P is controlled by a DC voltage V_P and also pulsed by a square wave with amplitude V_{pulse} at frequency f_{pulse}. This pulsing frequency is locked with the pulse lock-in amplifier, which is also passed through the pre-amplifier so that the pulsing signal picked up by the sensor from the quantum dot is monitored. By varying the voltage on gate P, i.e. changing the potential in the dot, electrons from the reservoir can tunnel on and off the dot through the tunnel barrier created by gate LB. These tunnelling events are captured by the SET sensor so that we can monitor the status of the dot. The voltage on gate ST is dynamically adjusted via a feedback control to maintain a constant SET current. This keeps the read-out sensitivity unaffected by slow charge drifts and random charge rearrangements. All measurements are performed in a dilution refrigerator at the base temperature of ~50mK.

Schematic energy diagrams of electrons loading and unloading the quantum dot are shown in Figures 2.12b and 2.12c. The tunnel rate is independently controlled by V_{LB}, while V_{RB} raises the right barrier to be completely opaque. In Figure 2.12b, both loading and unloading phases are below the reservoir Fermi level E_F and hence no tunnelling occurs. Conversely, in Figure 2.12c, during the high phase of the pulse (or low in potential), a single electron can tunnel into the quantum dot and tunnel out

during the low pulse phase (or high in potential). This change in dot occupancy induces a current peak in the lock-in detection signal.

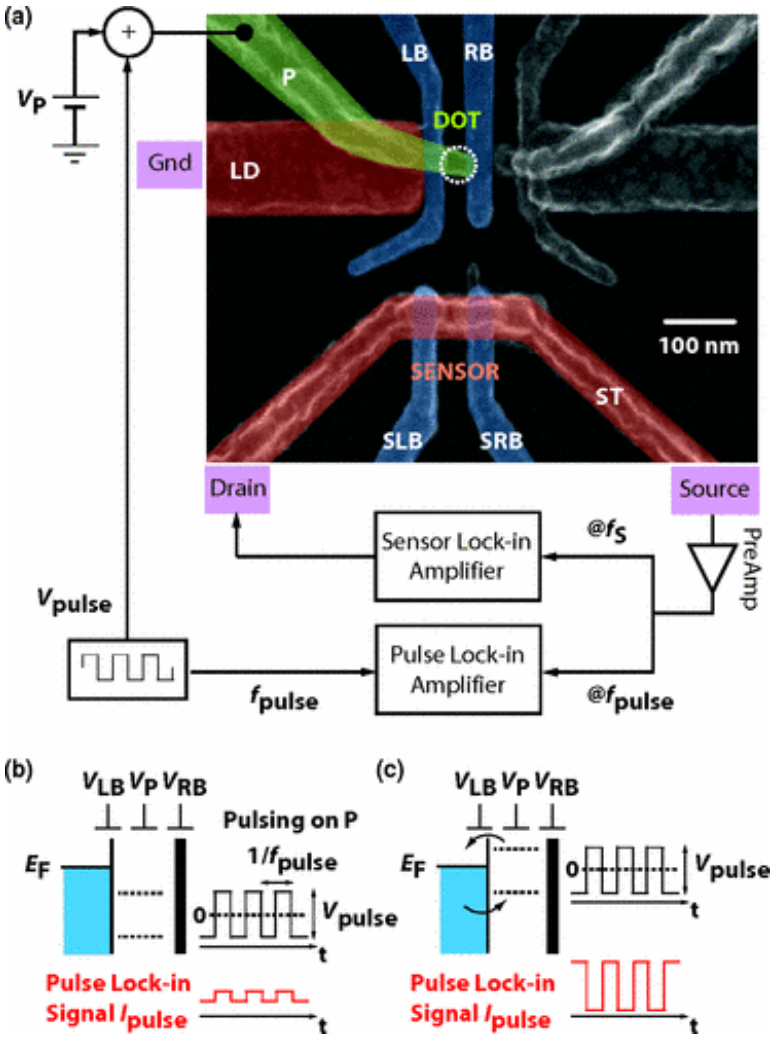


Figure 2.12: (a) False-coloured SEM image of a quantum dot device with integrated SET charge sensor. The measurement setup schematic is also presented. (b) & (c) Schematic energy diagrams with pulsing on gate P at two different V_P offsets [11].
Courtesy of Yang et al., Physics Review B 86, 115319 (2012)

Figure 2.13 shows a measurement of the quantum dot stability map as a function of the right barrier gate voltage V_{RB} and top gate voltage V_P. Each line corresponds to a charge transition of the quantum dot with a slope determined by the coupling between the barrier and the dot. The charging energy increases as the number of electrons decreases, indicating that the dot size is diminished and the dot is in the few-electron regime. Charge transitions are detected identically for pulse signal I_{pulse} and sensor signal I_s as shown in Figure 2.13a and 2.13b, respectively, but a better signal-to-noise

ratio is obtained with I_{pulse}. The 0–1 transition is not visible in Figure 2.13b, due to the fall in the tunnel rate of the first electron. The rate falls below the pulsing frequency, so that insufficient time is provided for it to tunnel on/off the dot. However, the SET is still able to detect that there is a state available for electron tunnelling and hence a transition line can be seen on Figure 2.13a.

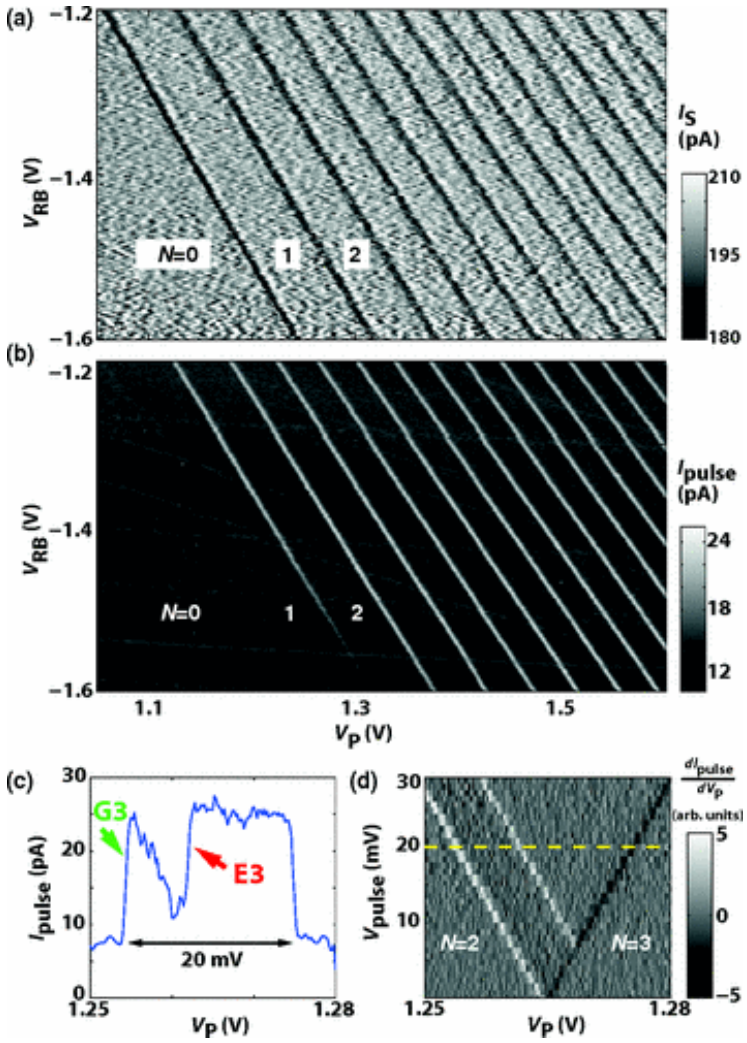


Figure 2.13: (a) Charge stability map diagram of sensor current I_s as a function of V_P and V_{RB}. (b) Stability map of the pulse lock-in signal I_{pulse} measured by the SET sensor. The 0–1 transition is invisible due to the low tunnel rate with respect to the pulsing frequency f_{pulse}. (c) Pulse lock-in detection signal for the 2–3 transition extracted from the yellow line in (d), showing orbital ground and excited states. (d) Derivative of pulse lock-in signal with respect to V_P. Orbital ground and excited states are observed as the two parallel white lines [11].
Courtesy of Yang et al., Physics Review B 86, 115319 (2012)

Excited states of the quantum dot are observed from the 2–3 transition as shown in

Figure 2.13c, taken from the yellow dashed line section in Figure 2.13d. As the three-electron ground state is pulsed below E_F, a charge transition is detected, which causes a peak on the pulse lock-in signal (indicated by the green arrow). The signal then decays gradually as V_P increases, until the excited state is also pulsed below the Fermi level. This results in the second peak on the detection signal (indicated by the red arrow). The signal falls again as no further transition occurs due to Coulomb blockade. Figure 2.13d shows the derivative of the detection signal with respect to V_P as a function of V_{pulse} and V_P. The two white lines represent the orbital ground and excited states at the loading edge, while the black line indicates the unloading stage.

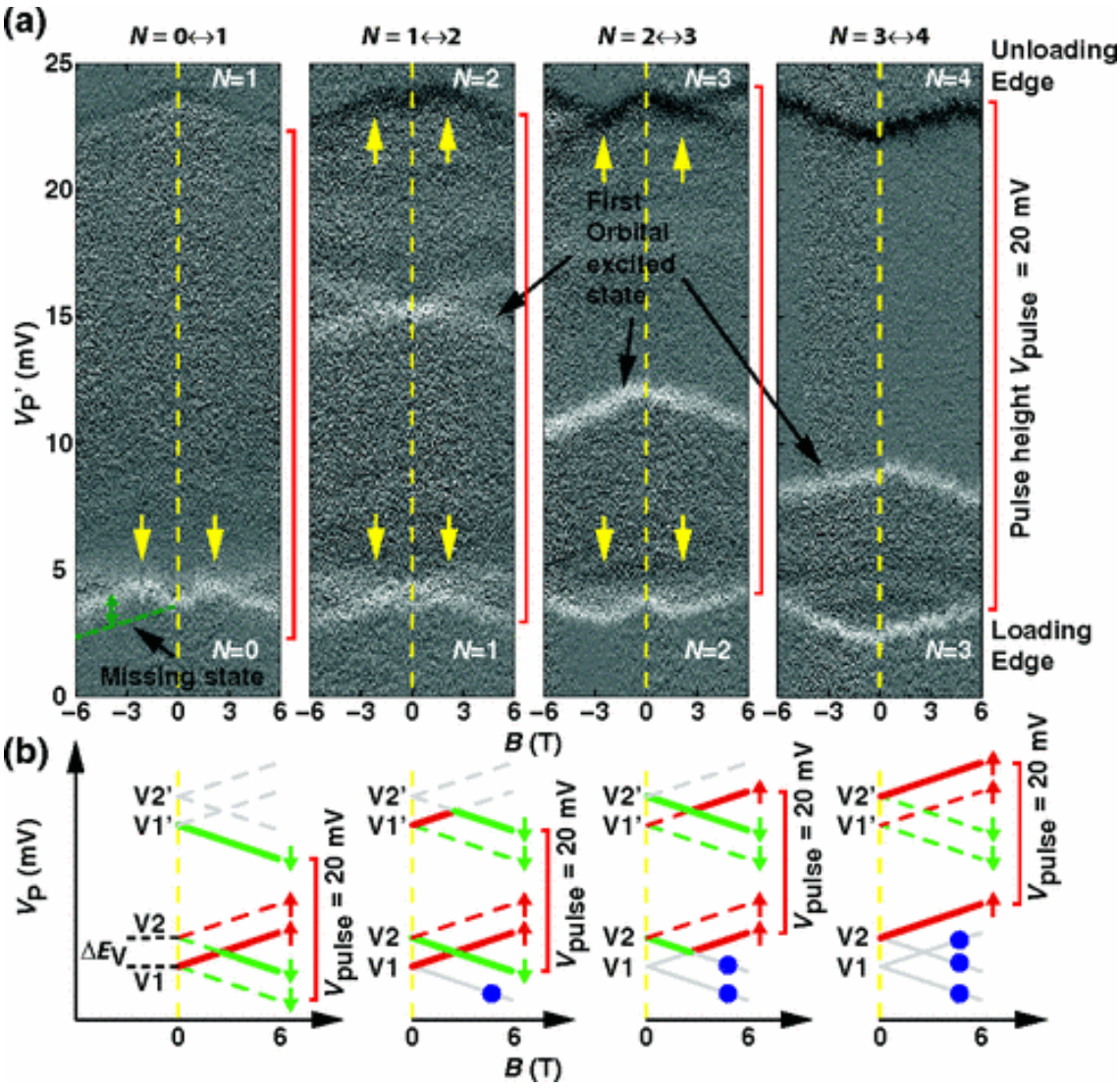


Figure 2.14: (a) Quantum dot occupancy in magnetic field of the first four electrons [11]. Orbital excited states, Zeeman splitting and valley-orbit splitting are observed. (b) Schematic of spin filling of two nondegenerate valley states for magnetic field $0T < B < 6T$. Each valley Zeeman splits into two levels along the B field. The blue dots represent occupied electron states.

Courtesy of Yang et al., Physics Review B 86, 115319 (2012)

To study the spin-valley interaction, spin filling of the first four electrons into the valley states is examined in this paper. A magnetic field is applied parallel to the oxide interface in the range $-6T < B < 6T$ to Zeeman shift the ground and excited states. The derivative of the pulse lock-in current dI_{pulse}/dV_P is measured as a function of V_P and B, as shown in Figure 2.14a.

The unloading edge of charge transitions is considered, and appears as dark lines. First, at the 0–1 transition, the unloading edge moves towards a less positive V_P along the increasing magnetic field. This indicates that the first electron is spin-down $|\downarrow\rangle$. Next, for the second transition (1–2), the energy level increases with magnetic field for $B < 2T$. The energy level decreases with B above 2T. This indicates that a spin-up electron is unloaded at low magnetic field ($B < 2T$); at $B > 2T$, the upper valley ground state has a lower potential than the lower valley excited state, hence a spin-down electron is unloaded in this case. A similar kink is also observed for the 2–3 transition at $B \sim 2T$, while the edge moves downwards at low B and upwards at high B. This indicates that a spin-down electron is first occupied at the low field, and a spin-up electron at high field. Finally, in the 3–4 transition the edge moves upwards along the magnetic field, confirming that a spin-up electron is unloaded. The white lines between the loading and unloading edges are the orbital excited states.

A spin-filling schematic diagram is also depicted in Figure 2.14b. The first electron always fills the lower valley V1 as a spin-down for all B. The second electron from the 1–2 transition fills V1 as a spin-up for low B, forming a singlet state ($|\downarrow\uparrow\rangle - |\uparrow\downarrow\rangle$). At high B, the Zeeman energy exceeds the valley-splitting E_V so that a spin-down electron is preferentially loaded into the upper valley V2, forming a triplet state $|\downarrow\downarrow\rangle$. Similarly, a spin-down electron loads into the upper valley V2 at the lower field; but an electron loads into V1 as a spin-up once the Zeeman energy exceeds E_V for the 2–3 transition. The fourth electron transition always fills V2 as a spin-up.

This paper studies excited states of silicon quantum dots, and introduces the charge sensing and pulsed-gating techniques. An extensive analysis is performed on the spin, valley and orbital states of the first four electrons confined in the quantum dot.

Chapter 3
Si-MOS multiplexer

In this chapter, we discuss all research work of the Si-MOS multiplexer project in detail. We start by introducing the multiplexing device design and its fabrication process, followed by a series of tests with relevant issues and discussions. A secondary ion mass spectrometry (SIMS) study of two samples is also included. A summary of the project and design modification is given at the end of the chapter.

3.1 Design and fabrication

The first version of the Si-MOS multiplexer was designed in AutoCAD by R. Leon (one of our team members) during his undergraduate thesis project. The design consists of two parts: a small-scale test circuit and a full-scale multiplexer. During Leon's project, he generated the design in AutoCAD and discussed the fabrication procedure with the ANFF process engineering team. The multiplexer was then fabricated by a process engineer and handed to Leon by the end of his thesis project. Due to the limited time available, Leon only managed to test a few devices on the small-scale test circuits. The multiplexer itself was left untested. This project was then passed to me as the beginning of my Master's research project.

The multiplexer AutoCAD design consists of multiple layers of structures represented in different colours. The following section explains the design layer by layer to describe the entire multiplexer. For ease of explanation, the fabrication process will be simplified. Detail process and parameters are not included in this thesis, as the fabrication recipe includes confidential information of the research group. As mentioned, the multiplexer is designed and fabricated based on an Si-MOS multi-layer structure, i.e. the device is fabricated layer by layer, using intrinsic silicon as the substrate. Figure 3.1 shows the first layer pattern, which is the p-type channel stoppers. The black background represents the silicon substrate and the (enclosed) cyan rectangles indicate the channel stoppers. A thick oxide is grown, patterned via photolithography [20] and etched to act

as the mask for thermal diffusion. Boron at a concentration of $10^{17}cm^{-3}$ is then thermally diffused into silicon to form channel stoppers, followed by a drive-in oxidation which also oxidises the silicon surface.

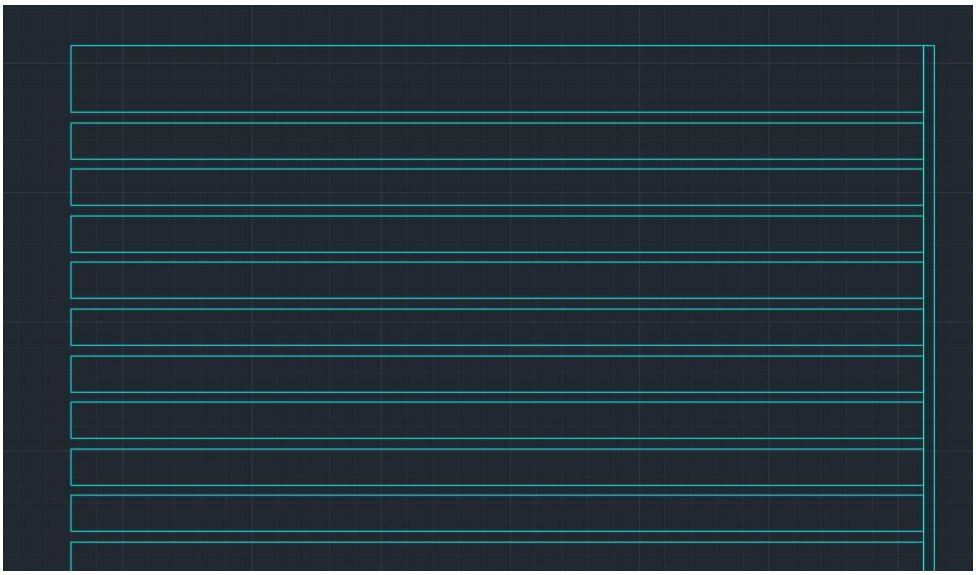


Figure 3.1: AutoCAD design of the multiplexer first layer. The p-type channel stoppers (cyan rectangles) are thermally diffused into intrinsic silicon (black).

The n-type channels, or n-fingers, follow as the second layer in red. Figure 3.2 shows the design along with a schematic cross-section. The n-fingers are patterned and diffused between the channel stoppers in a similar way, with a phosphorous doping concentration of $10^{20}cm^{-3}$. The cross-section depicts the doping profile of an arbitrary n-finger.

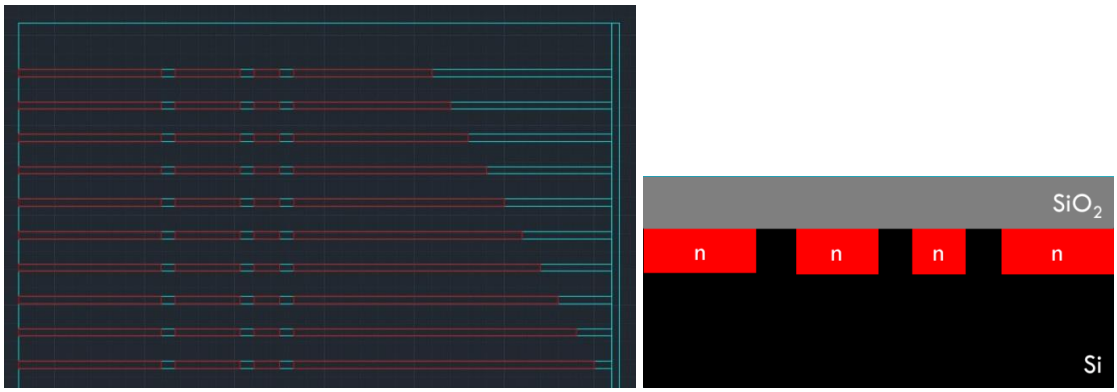


Figure 3.2: AutoCAD design of the multiplexer second layer. The n-fingers thermally diffuse between the p-type channel stoppers; the doping profile is shown in the schematic cross-section.

The third layer comprises ohmic contact deposition. Figure 3.3 shows the locations where ohmic contacts are deposited in orange. The contacts are formed by patterning and etching through the thick oxide using HF, followed by an e-beam evaporation [18] of aluminium and platinum. The result is that the ohmic contacts have a structure of platinum stacking on top of aluminium to prevent aluminium being oxidised in air, and aluminium is in contact with the n-doping at both ends of the n-fingers. Platinum does not oxidise, so it covers the contact surface to ensure electrical conductivity when depositing other metals later in the process.

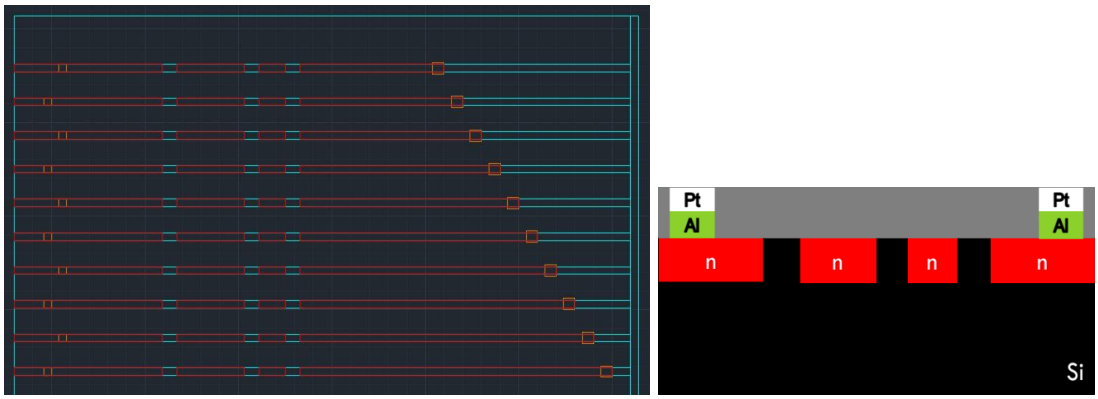


Figure 3.3: AutoCAD design of the multiplexer third layer. Platinum–aluminium ohmic contacts are fabricated via patterning, etching and e-beam evaporation.

The fourth layer is the growing thin-oxide. Figure 3.4 indicates the location of the thin-oxide windows in pink. The thin-oxides are grown by etching through the thick oxide and thermally oxidise to a thickness of 7.5nm. Note that there is a thin-oxide region on the left-hand side of the design, which is not shown in the schematic cross-section.

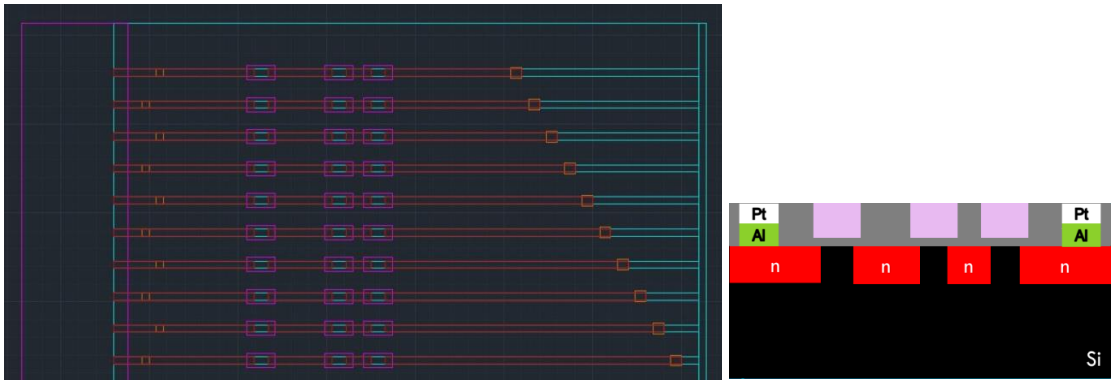


Figure 3.4: AutoCAD design of the multiplexer fourth layer. 7.5nm-thin oxides are grown in the regions shown in pink.

The fifth layer includes aluminium gates and bond-pad deposition, and its design is shown in green in Figure 3.5. Each gate is connected to its own bond-pad to form an electrical connection. Aluminium gates either run on top of thin-oxide regions between the n-finger gaps, or on the right-hand side ohmic contacts to perform different functions. The schematic cross-section shows the metal gating structures. The bond-pads provide access to external connections to control the device, and all gates are deposited via e-beam evaporation [18]. The device is finished by depositing titanium/platinum cross-markers in yellow around the large thin-oxide region for EBL alignment use. The final thickness of the field oxide is designed to be approximately 200nm.

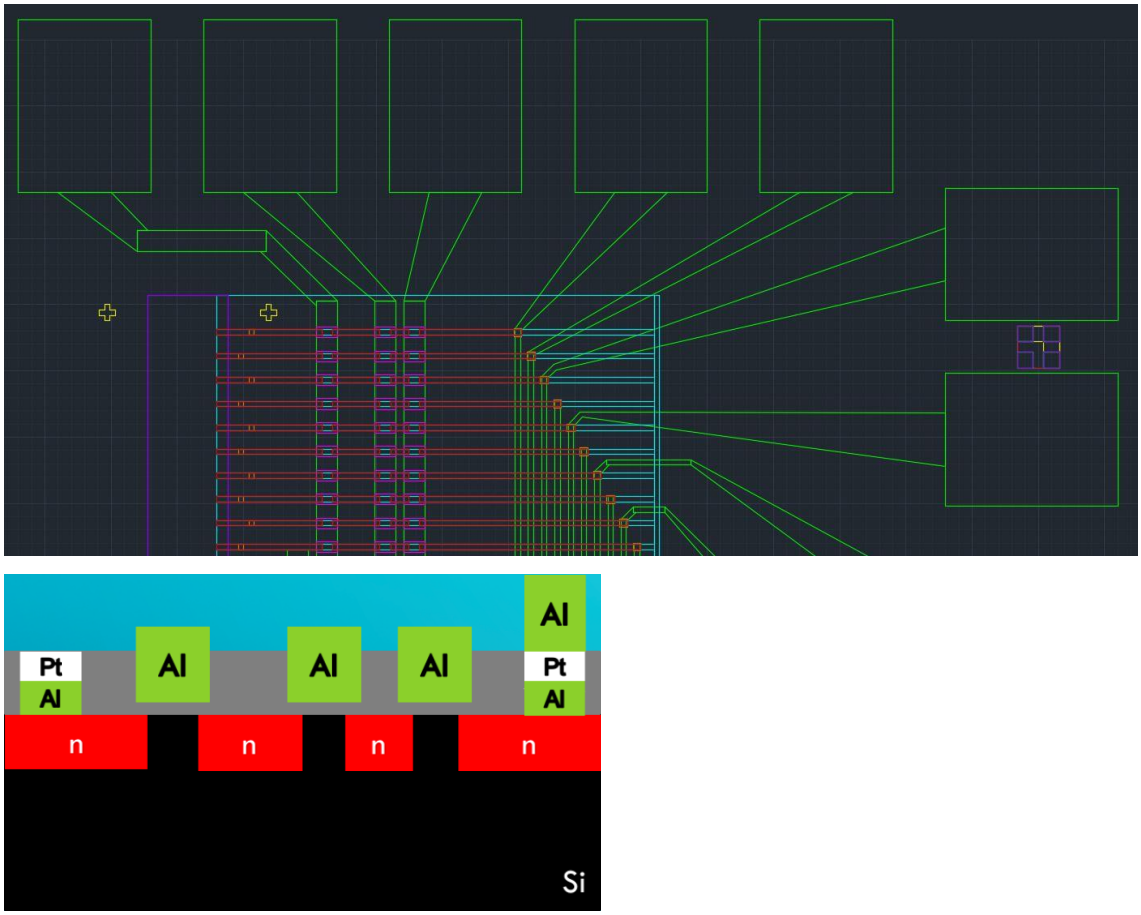


Figure 3.5: AutoCAD design of the multiplexer's fifth layer. Aluminium gates and bond-pads are deposited on top of small thin-oxide windows and ohmic contacts via e-beam evaporation. The yellow cross-markers are used for EBL alignment.

The device shown so far is a partial structure of the multiplexer, for ease of explaining its design and fabrication process. This partial structure replicates itself seven times to

form the entire multiplexer design as shown in Figure 3.6. Here, eight individual parts are labelled *1~8* correspondingly, where we used *part 1* to explain the design from above. The other parts have an identical structure, except for different addressing gate *S1~S6* combinations.

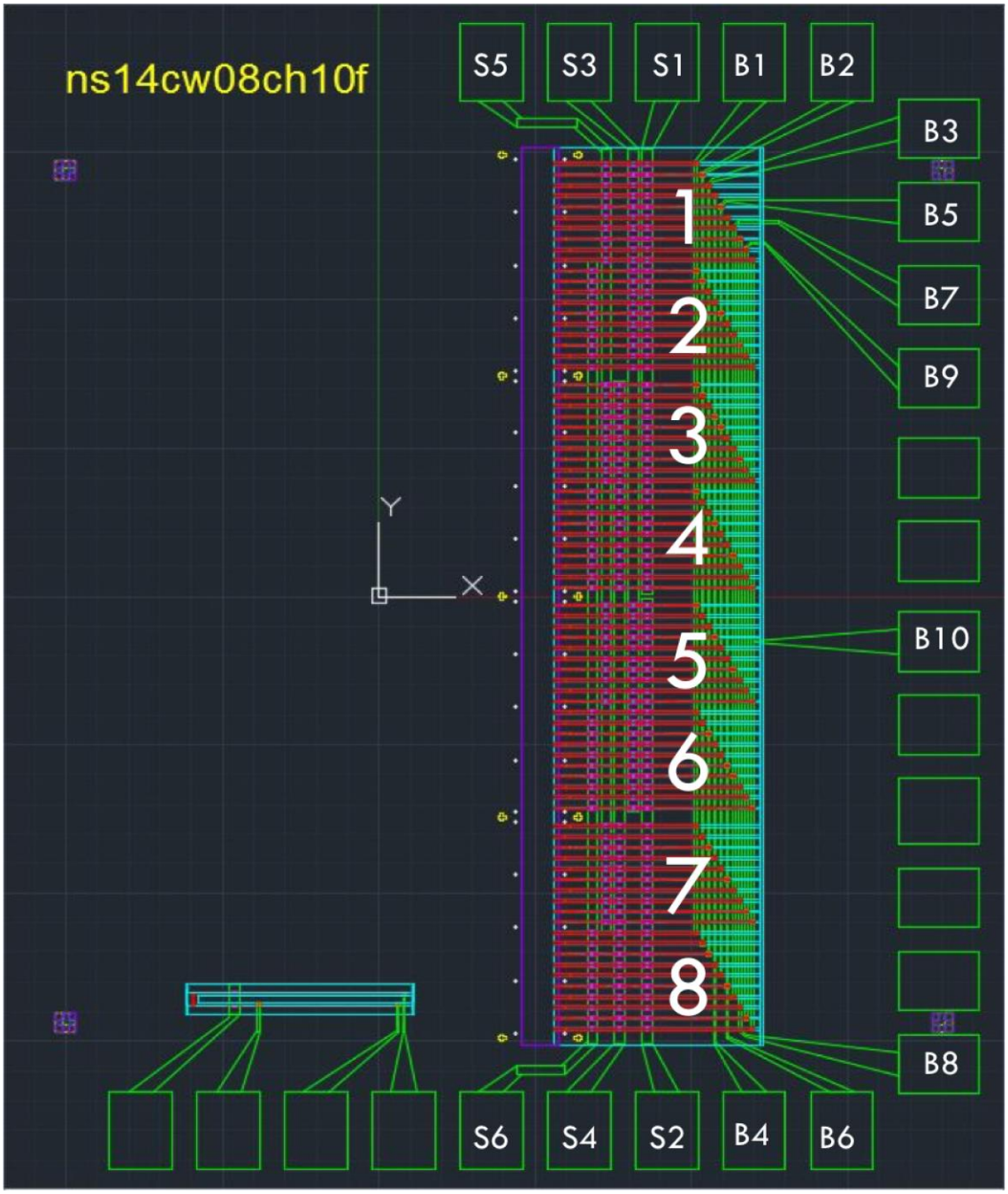


Figure 3.6: Si-MOS multiplexer design with p-type channel stoppers. A test circuit is included on the bottom left. The multiplexer consists of eight parts labelled *1~8*, which can be addressed individually by turning on the corresponding addressing gates *S1~S6*. Control gates *B1~B10* connect the corresponding n-finger in each part via the ohmic contacts.

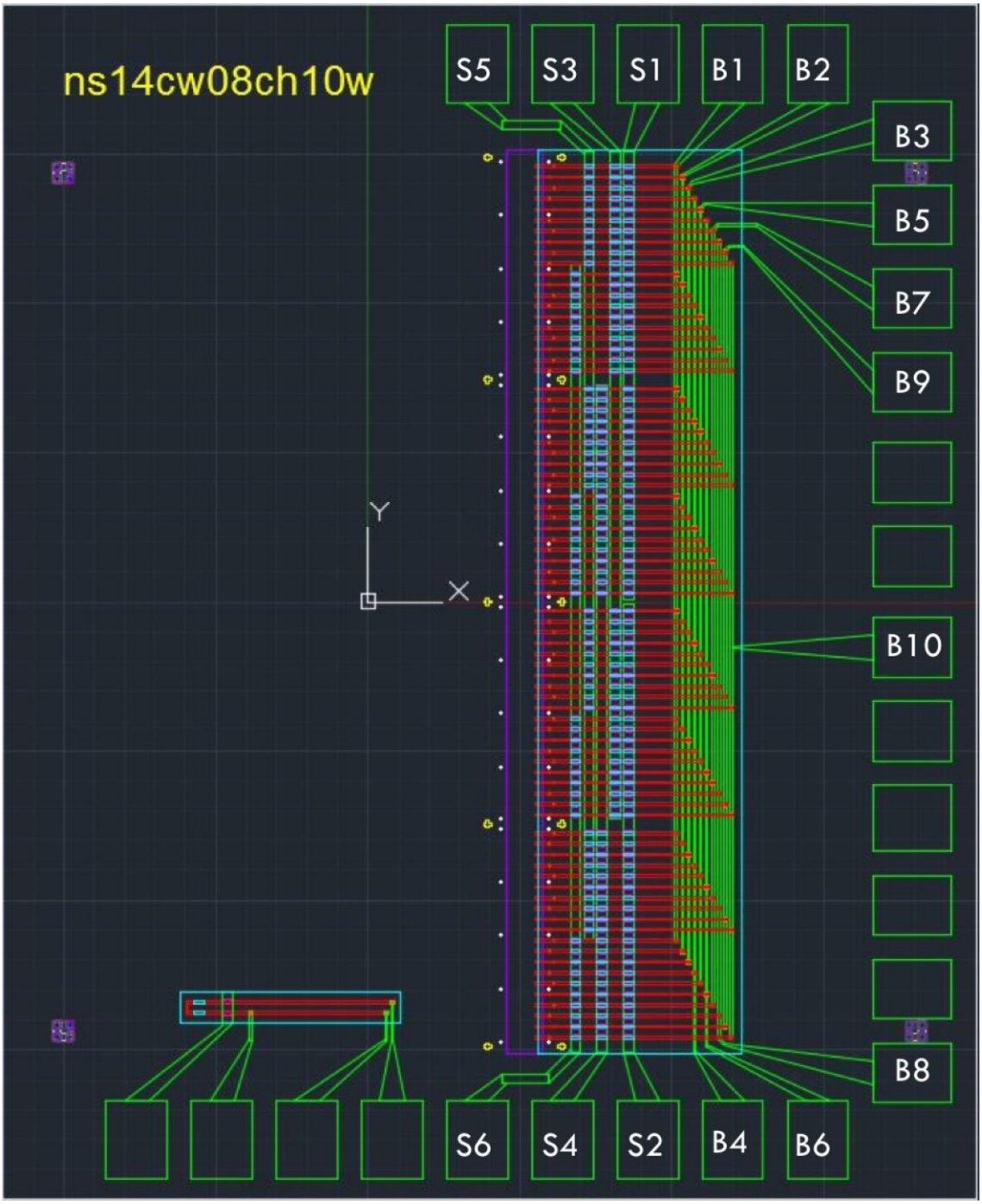


Figure 3.7: p-type well multiplexer design. A large p-type well forms the first layer, which encloses the entire device. Other parts remain the same as in the p-type channel stoppers design.

The design consists of a small-scale test circuit on the bottom left, which is not used in the project. The main part is the full-scale multiplexer, which includes eight identical parts with different addressing gate layouts. Control gates *B1~B10* connect to their corresponding n-fingers via the ohmic contacts on the right-hand side in all eight parts. For example, gate *B1* always connects to the first n-fingers in any of the eight parts.

Meanwhile, ohmic contacts on the left-hand side are reserved for making connections with nanoscale devices fabricated in the future. The code on the top left denotes the design variation of this specific device. Here, "ns" denotes n-finger separation, which means that the distance between each n-finger is 14μm; "cw" represents channel width, i.e. the width between the n-type doped regions within a thin-oxide window, which is 8μm in this design; "ch" is the number of n-fingers, where there are 10 n-fingers in each part of this design; and finally the "f" indicates that this is a finger-type channel stoppers design. A well-type channel stoppers design, whereby the code ends with a "w", is shown in Figure 3.7. The p-type channel stoppers are replaced by a p-type well enclosing the entire device. We aim to test and verify whether a p-type channel stopper or a p-type well would perform better in the experiment. In this thesis project, only devices with labels beginning "ns14" are used. All n-fingers are 4μm wide.

We now explain the principle of multiplexing with the aid of Figure 3.8. Here, as an example, we address the third n-finger from *part 1*. We first address *part 1* by switching on addressing gates *S1, S3 and S5*, as these three gates are in contact with the thin-oxide windows. These gates are coloured yellow for clarity. This structure forms MOSFET switches that create conducting current paths at the silicon/thin oxide interface when turned on. Hence, the entire n-finger becomes conducting, and signals from the right ohmic contact can now be sent to the left contact. This happens to all of the n-fingers within *part 1*. By this point, any signal sent by control gates *B1~B10* can reach the left ends via the corresponding n-fingers. In this example we send a signal to gate *B3* as labelled in red. This signal can be passed to the third n-finger of all eight parts, but only the third n-finger of *part 1* can receive it (shown in green).

Other parts are not addressed as at least one of the addressing gates is turned off and hence no signal from the control gates can be passed through. Here, gates *S2, S4 and S6* remain turned off. The addressing gates that are run on top of parts without thin-oxide windows are bypassed by the field oxide. For example, gate *S5* also runs through *part 2*, but it does not address this part because the field oxide is thick enough to prevent a conductive path forming beneath the interface. Hence, there is only one set of addressing gates for each part to be addressed. To address *part 2*, we switch on *S1, S3*

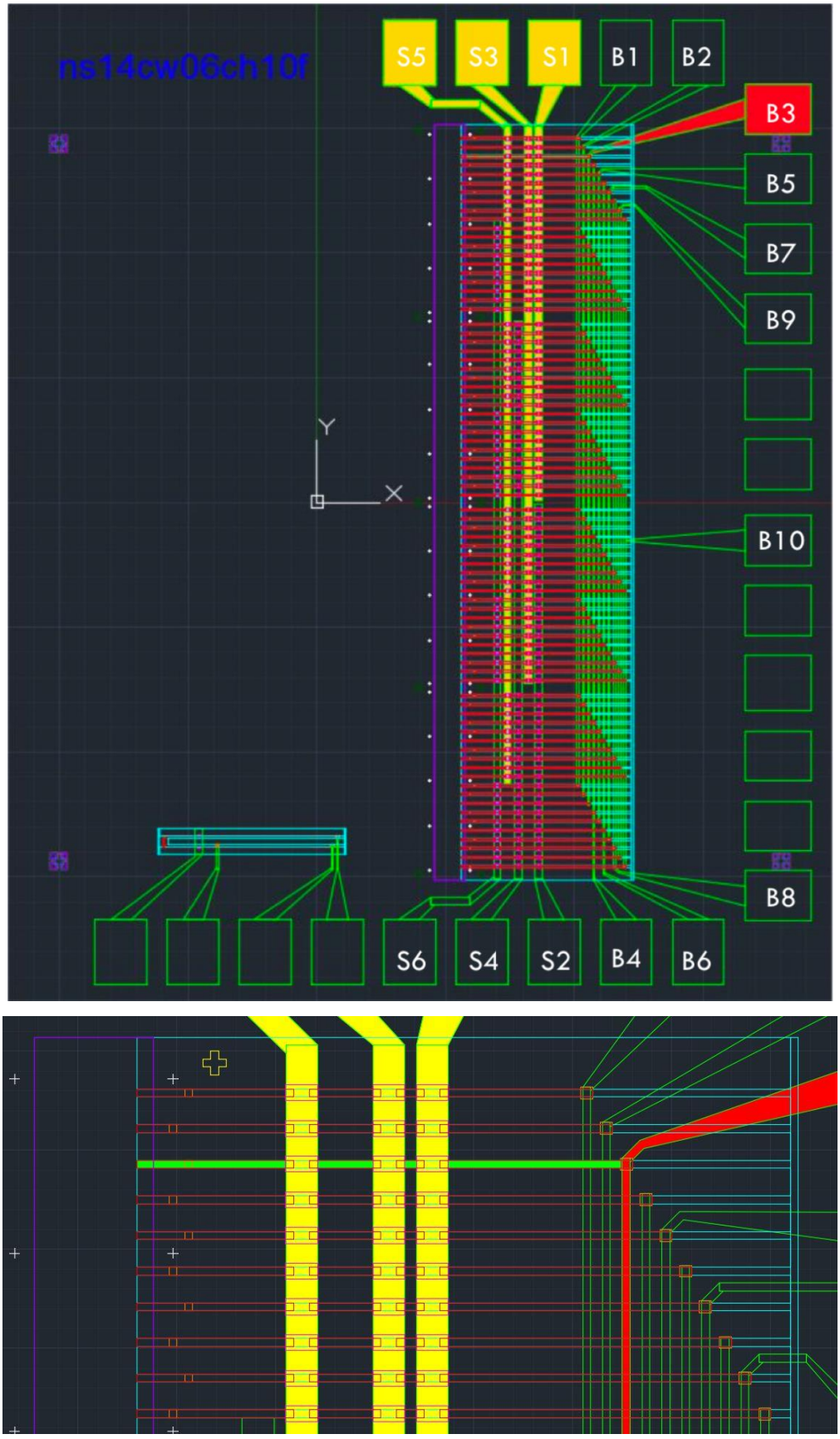


Figure 3.8: The principle of multiplexing. An example here is to address the third n-finger of *part 1.* Addressing gates *S1, S3 and S5* are switched on and the signal is passed via gate *B3.*

and S6. Similarly, *S1, S4 and S5* for *part 3; S1, S4 and S6* for *part 4; S2, S3 and S5* for *part 5; S2, S3 and S6* for *part 6; S2, S4 and S5* for *part 7;* and *S2, S4 and S6* for *part 8.*

We design this multiplexer to have eight quantum dot devices to be fabricated within the thin-oxide region. Each gate electrode of a device is attached to an n-finger, so that a maximum of ten electrodes is allowed. The multiplexer is able to independently address and operate each of the eight quantum dot devices. Therefore, we expect to test eight devices in one 4K dipping session. To achieve this, we must ensure the robustness and reliability of the multiplexer. Hence, a series of extensive testing needs to be carried out to examine the aforementioned aspects. The following subsections describe different types of tests and discuss their experimental outcomes.

3.2 Leakage test

Three identical batches of multiplexers are fabricated to ensure a sufficient number of samples to create measurement statistics. We randomly chose three samples from *batch 1*, one from *batch 2* and one from *batch 3* to perform a leakage test. These were all blank samples without any nanoscale devices fabricated in the thin-oxide region. We performed the leakage test by connecting the "Output-HI" of an SMU to the tested gate at 4K, while all other gates were grounded at 0V. We set the SMU current compliance to 10μA and swept the SMU voltage from -4V ~ 4V. We defined a leakage as the case where the current hits compliance.

Figure 3.9 shows two leakage test results of two gates *S1* and *B1* of a sample from *Batch 1* labelled *ns14cw04ch10f*. *S1* shows no leakage as it is simply the measurement noise from the instruments. *B1* hits the compliance when the voltage is swept to 1.76V and this current leaks to other parts of the multiplexer. Thus, we record that *B1* leaks at 1.76V. Table 3.1 outlines the leakage test results for this sample.

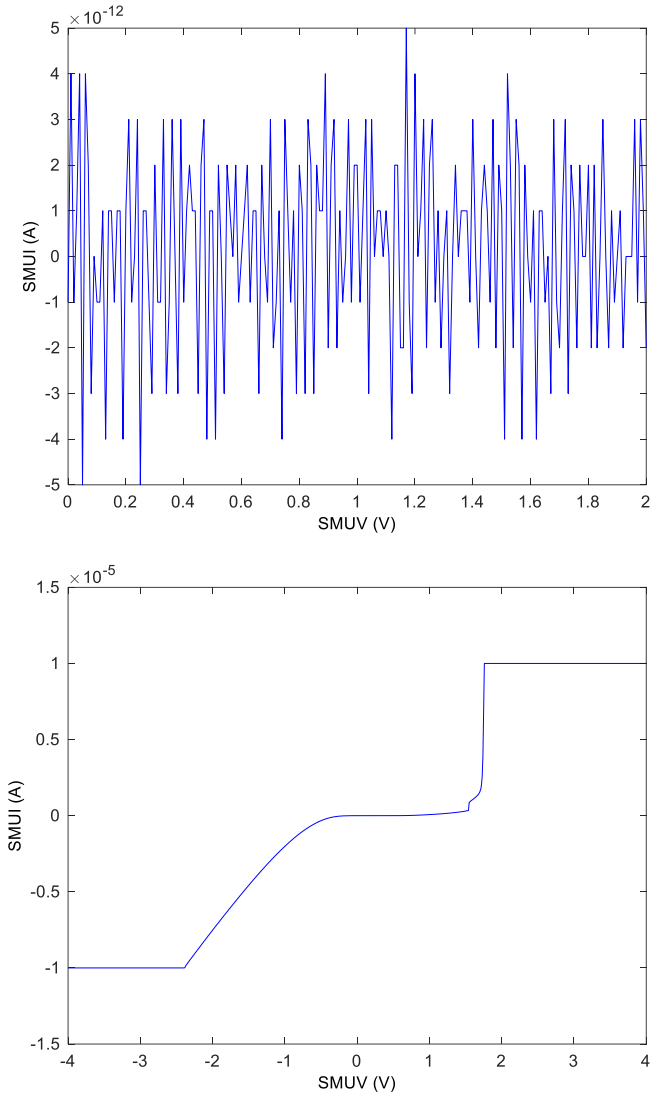


Figure 3.9: Leakage test results of *S1* and *B1* of a sample from *batch 1*. *S1* shows no leakage but *B1* starts to leak to other parts of the multiplexer at 1.76V.

Gates	Leaks at (V)
B1	1.76
B2	1.45
B3	1.44
B4	3.6
B5	1.03
B6	2.47
B7	0.68
B8	No
B9	No
B10	1.79

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

Table 3.1: Leakage test results of *Batch 1 – ns14cw04ch10f*.

Similarly, for *Batch 1 – ns14cw04ch10w*, we have:

Gates	Leaks at (V)
B1	No
B2	No
B3	No
B4	No
B5	3.05
B6	No
B7	No
B8	No
B9	No
B10	No

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

Table 3.2: Leakage test results of *Batch 1 – ns14cw04ch10w*.

For *Batch 1 – ns14cw08ch10w*:

Gates	Leaks at (V)
B1	3.38
B2	No
B3	2.84
B4	3.69
B5	3.12
B6	3.59
B7	No
B8	2.82
B9	3.8
B10	No

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

Table 3.3: Leakage test results of *Batch 1 – ns14cw08ch10w*.

For *Batch 2 – ns14cw08ch10w*:

Gates	Leaks at (V)
B1	2.16
B2	3.03
B3	2.15
B4	3.72
B5	2.84
B6	No
B7	3.78
B8	2.92
B9	No
B10	3.18

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

Table 3.4: Leakage test results of *Batch 2 – ns14cw08ch10w*.

For *Batch 3 - ns14cw08ch10w*:

Gates	Leaks at (V)
B1	1.98
B2	2.13
B3	2.23
B4	2.18
B5	2.01
B6	2.04
B7	2.14
B8	2.19
B9	No
B10	3.65

Gates	Leaks at (V)
S1	No
S2	2.74
S3	No
S4	No
S5	No
S6	No

Table 3.5: Leakage test results of *Batch 3 – ns14cw08ch10w*.

From the five sets of results presented above, we can see that all of the tested samples have n-finger leakages, and start to leak at a certain applied voltage. We performed a quick test to determine the leakage paths and found that these n-fingers were leaking to each other. The conclusion is that above a certain voltage, the channel stoppers experience p-n junction reverse-bias breakdown, so that they cannot resist current flow. This leakage current eventually flows to its nearest low potential point, which is a grounded n-finger. We also found a leaking addressing gate in Table 3.5; *S2* leaks to a few n-fingers, and we believe that it leaks through the thin-oxide windows where the oxide was not grown properly during the fabrication process. Despite these issues, we

believe that we can still try to operate the multiplexer with the limitations of these leakage voltages.

3.3 MOSFETs turn-on test

We started to test the operation with a simple device structure; in this case, we chose MOSFETs. A MOSFET is a simple switch consisting of a gate electrode that sits between two ohmic regions named the source and drain. When a voltage is applied to the gate above the threshold, a current path forms and conducts the source and drain, and we say that the MOSFET is turned on. In this test, we select three n-fingers from each part of the multiplexer to create MOSFETs and test whether the multiplexer can address and operate these MOSFETs.

Figure 3.10 shows the MOSFET turn-on test design. We first transformed the AutoCAD design file into Raith [17] EBL design software. We then drew the design of the MOSFETs in red and fabricated them on the multiplexer samples using EBL [17], aluminium e-beam evaporation [18] and lift-off [21]. One n-finger is chosen to be the gate, and this gate electrode is attached to the left ohmic contact of the n-finger. The gate electrode overlaps two other n-fingers and forms the source and drain, respectively. For instance, as shown in the insert of Figure 3.10, we used the eighth n-finger from *part 5* to operate as the gate and the sixth and seventh n-fingers to be the source and drain. We expect that when a voltage (above the threshold) is applied to the gate n-finger with a bias on source and drain, a current is conducted through the source and drain n-fingers.

In this design, we selected different combinations of gate, source and drain n-fingers at different parts of the multiplexer. This is to ensure that we are addressing and operating exactly the desired device without having two or more devices sharing the same sets of n-fingers, which would cause ambiguity. The channel width of all MOSFETs is 1μm.

We chose one sample from *Batch 1* and one from *Batch 2* to fabricate MOSFETs on, both with the same design specification, namely *ns14cw06ch10w*. As per usual, we started with the leakage test. The results are shown in Tables 3.7 and 3.8.

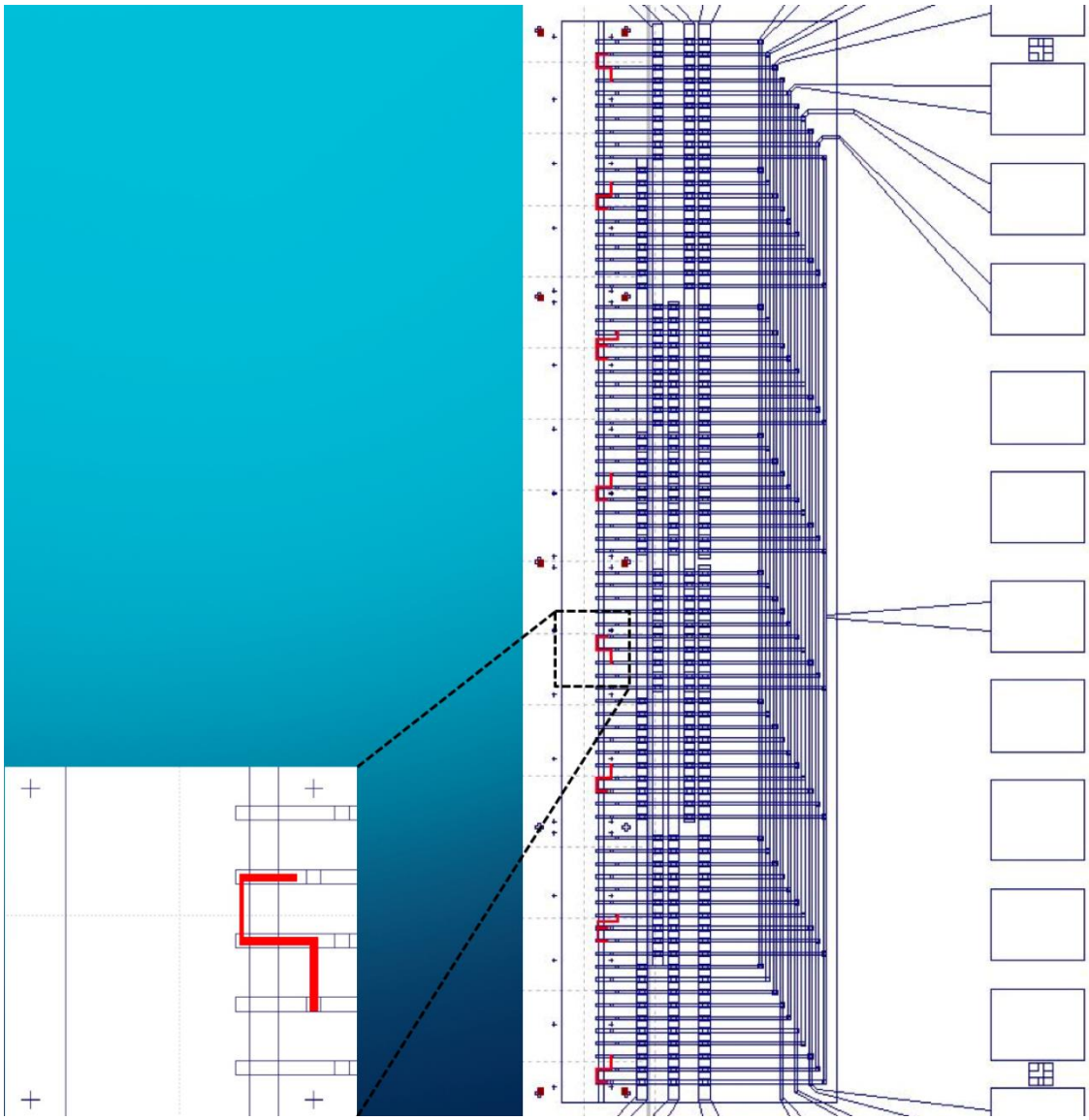


Figure 3.10: Design of the multiplexer MOSFETs turn-on test. MOSFETs are made with different sets of gate, source and drain n-finger combinations. The multiplexer can be tested by addressing and operating individual MOSFETs.

Table 3.6 lists the n-finger arrangement of this design.

Part	1	2	3	4	5	6	7	8
Gate	B4	B2	B3	B4	B8	B6	B7	B8
Source	B3	B3	B4	B5	B7	B7	B8	B9
Drain	B2	B4	B5	B6	B6	B8	B9	B10

Table 3.6: List of MOSFETs turn-on test n-fingers arrangements.

Gates	Leaks at (V)
B1	No
B2	0.88
B3	3.78
B4	3.4
B5	No
B6	0.8
B7	0.45
B8	0.71
B9	No
B10	0.84

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

Table 3.7: Leakage test results of *Batch 1 – ns14cw06ch10w* with MOSFETs.

Gates	Leaks at (V)
B1	1.45
B2	1.6
B3	1.58
B4	1.56
B5	1.59
B6	1.82
B7	1.62
B8	1.92
B9	1.85
B10	3.24

Gates	Leaks at (V)
S1	1.14
S2	No
S3	3.38
S4	2.99
S5	No
S6	No

Table 3.8: Leakage test results of *Batch 2 – ns14cw06ch10w* with MOSFETs.

We can see that the sample from *Batch 1* has no addressing gate leakage, but n-fingers start to leak at a very low voltage, with the exception of B3 and B4. The sample from *Batch 2* has some leakages on addressing gates, while the n-finger operation windows are wider as they generally have higher leakage voltages.

For the MOSFETs test, we ungrounded and left all other gates floating while only connecting the gate, source and drain of the MOSFET that we were operating. Hence, we can ignore the limitations on leakage voltages since we have eliminated all possible leakage paths. We biased the source and drain through a lock-in amplifier with an AC voltage of 100μV. A DC voltage source was used to operate the gate. For each part of the multiplexer, we first connected the measurement instruments to their corresponding device electrical contacts. We then set up the source-drain bias and turned on addressing gates for the testing part. Finally, we swept the gate voltage and measured the source-drain current through the lock-in amplifier.

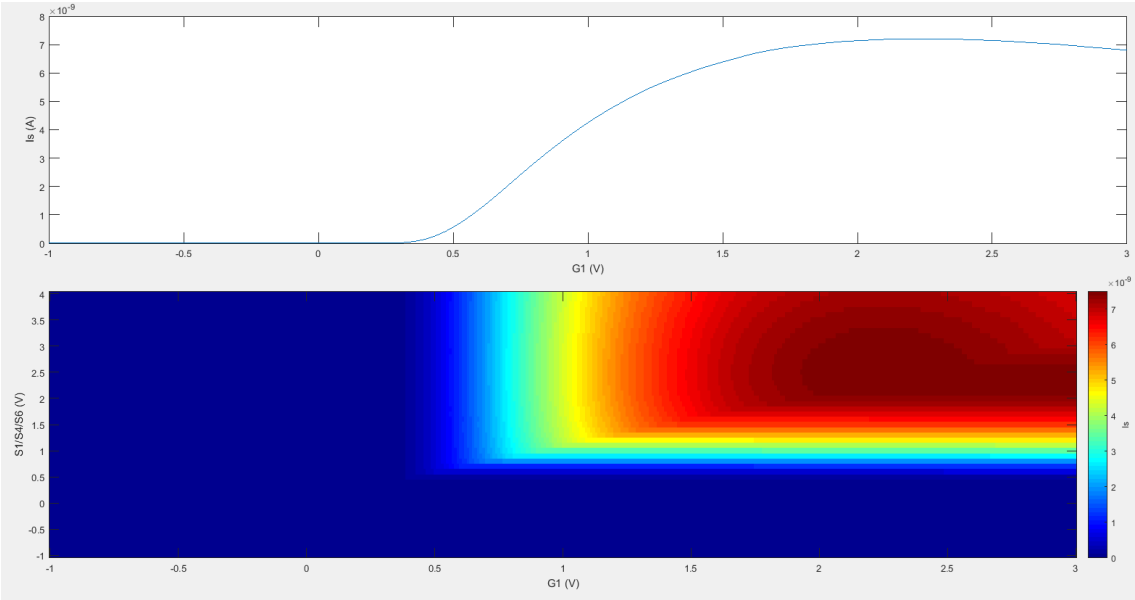


Figure 3.11: Measurement results of a turned on MOSFET. The upper plot shows the source-drain current as a function of the gate voltage. The threshold voltage is approximately 0.4V and the device saturates at about 2V with saturation current 7nA. The colour map shows the source-drain current as a function of addressing gates (S1, S4 and S6) voltage and MOSFET gate voltage. The MOSFET only turns on when addressing gates are fully turned on at 1.5V and above and when the MOFSET gate voltage exceeds the threshold. B4 (V) range from -1V to 3V, S1/S4/S5 (V) range from -1 to 4V, and Is range from 0 to 80nA.

Among the 16 MOSFETs from the two samples, we found only one turned-on MOSFET from *part 4* of the *Batch 1* sample. The corresponding measurement result is shown in Figure 3.11. The upper subplot shows a MOSFET turn-on curve, i.e. the source-drain current as a function of the gate voltage. We swept the voltage from -1V ~ 3V and this MOSFET started to turn on at approximately 0.4V. The current increases

along with increasing gate voltage until the device saturates at around 2V with a saturation current of 7nA. The lower colour map shows the source-drain current as a function of the addressing gates voltage and MOSFET gate voltage. The addressing gates (S1, S4 and S6) are fully turned on at 1.5V. Any voltage above this value is the optimal voltage to operate these switches. The MOSFET turns on only when addressing gates are turned on and the MOSFET gate voltage exceeds the threshold.

In this test, we found that only one of the 16 MOSFETs turned on. We concluded a number of reasons why the other MOSFETs did not turn on:

1. The n-fingers fail to conduct current for some reason,
2. Gate electrodes are not in good contact with the ohmic contacts,
3. Addressing gates are not turned on properly,
4. MOSFETs are broken during the fabrication process.

We inspected the samples under a microscope and confirmed that the continuity of the n-fingers was good. The MOSFETs were also fabricated properly. Hence, we need to investigate further with a focus on reasons 2 and 3. From this successfully turned-on MOSFET, we can confirm that the multiplexer is able to address individual parts and operate devices fabricated on-chip. The next task is to troubleshoot problems that cause the MOSFETs not to turn on.

3.4 N-fingers turn-on test

Since any on-chip devices are operated by the multiplexer n-fingers, we must test and ensure that every element on the n-fingers is conducting properly. Because all n-fingers are fabricated in the same process, we can assume that they are highly similar and therefore can test a few from one sample instead of testing all 80, which is not efficient.

We selected one n-finger to test from each part of the multiplexer; the design is shown in Figure 3.12. Two bond-pads are made via EBL [17], aluminium e-beam evaporation [18] and lift-off [21], with connections to the test n-fingers. We attach the first n-finger from *part 1*, the second n-finger from *part 2* and the third n-finger from *part 3* to the green bond-pad P1; similarly, the fourth n-finger from *part 4*, the fifth n-finger from *part 5*, the sixth n-finger from *part 6*, the seventh n-finger from *part 7*, the eighth n-finger from *part 8* and the tenth n-finger from *part 3* for an extra set of data to the red bond-pad P2.

To conduct the n-fingers turn-on test, we applied 1V from the SMU to the corresponding bond-pad (B1–B10) of the test n-finger and grounded either P1 or P2, according to which the test n-finger was attached to. We then addressed this part of the multiplexer by switching on the addressing gates, and expect to measure a current that flows through the n-finger. The other gates remained floating to eliminate any chance of leakage during the test.

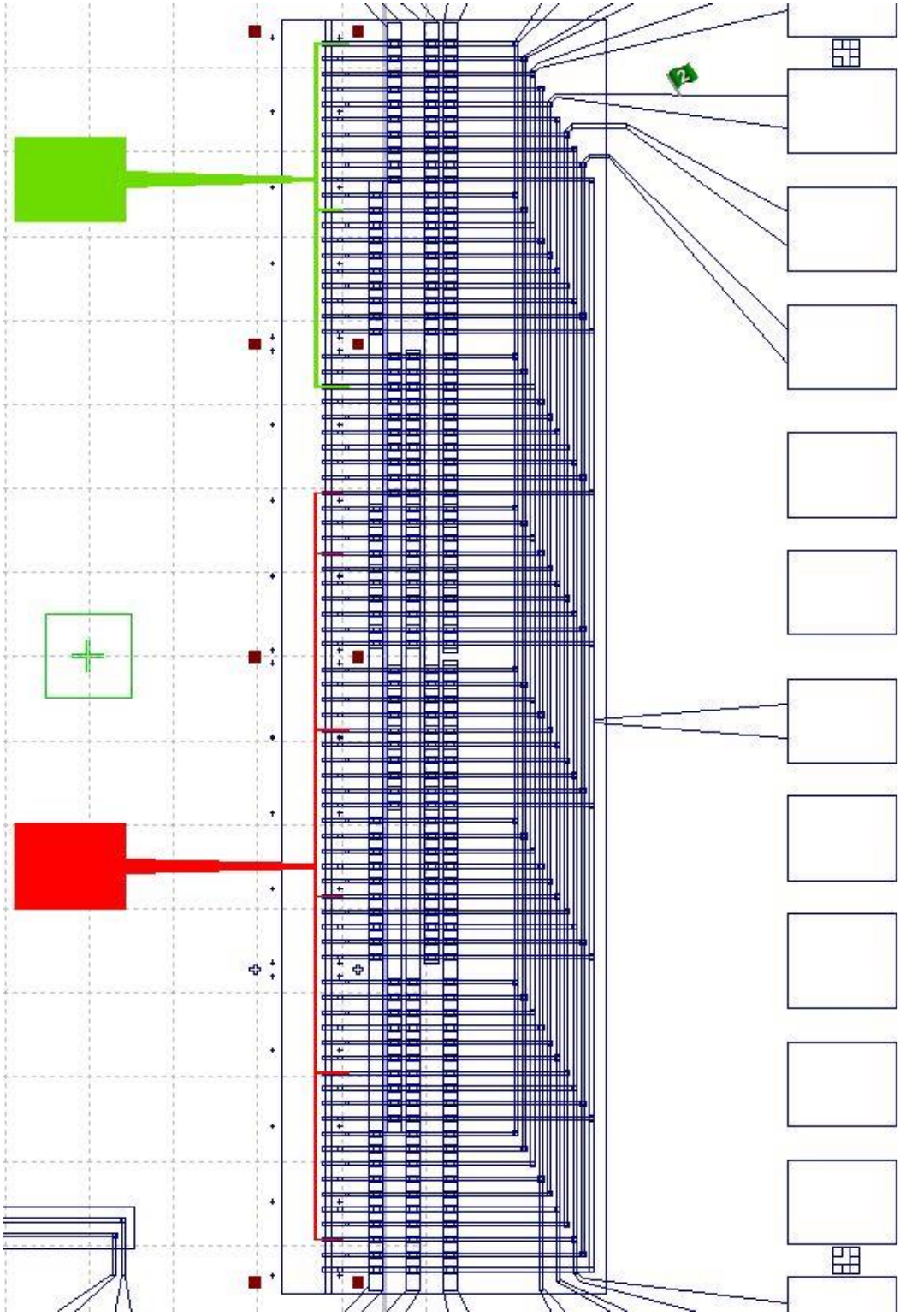


Figure 3.12: Design of the multiplexer n-fingers turn-on test. Two bond-pads were fabricated and attached to several test n-fingers. We tested these n-fingers by biasing them through the bond-pads and addressing their corresponding part. A current is then measured on the properly conducted n-fingers.

We selected one sample, *ns14cw08ch10f*, from *Batch 1*; and three samples from *Batch 2*, *ns14cw04ch10w*, *ns14cw06ch10w* and *ns14cw06ch10f*, to fabricate the above structure. Again, we began with the leakage test on the samples, and the results are listed below.

Gates	Leaks at (V)
B1	3.46
B2	1.49
B3	1.46
B4	1.39
B5	1.53
B6	1.54
B7	1.49
B8	2.92
B9	No
B10	3.72

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	No
S6	No

P1	No
P2	1.24

Table 3.9: Leakage test results of *Batch 1 – ns14cw08ch10f* with n-fingers test structure.

Gates	Leaks at (V)
B1	1.45
B2	1.45
B3	1.52
B4	1.01
B5	0.91
B6	0.89
B7	1.57
B8	2.7
B9	No
B10	0.96

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	2.43
S5	No
S6	No

P1	2.62
P2	2.41

Table 3.10: Leakage test results of *Batch 2 – ns14cw04ch10w* with n-fingers test structure.

Gates	Leaks at (V)
B1	1.64
B2	1.62
B3	1.51
B4	1.65
B5	1.66
B6	1.6
B7	1.61
B8	1.75
B9	1.61
B10	2.82

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	3.47
S5	No
S6	No

P1	No
P2	No

Table 3.11: Leakage test results of *Batch 2 – ns14cw06ch10w* with n-fingers test structure.

Gates	Leaks at (V)
B1	1.95
B2	1.6
B3	1.63
B4	1.47
B5	1.74
B6	1.29
B7	1.56
B8	2.63
B9	No
B10	3.17

Gates	Leaks at (V)
S1	No
S2	No
S3	No
S4	No
S5	1.92
S6	2

P1	No
P2	No

Table 3.12: Leakage test results of *Batch 2 – ns14cw06ch10f* with n-fingers test structure.

From the leakage test, we are confident that the test bond-pads do not leak to the gates with 1V DC bias. Hence, we were confident in proceeding to the n-fingers turn-on test. We performed the test on the n-fingers of each sample independently with the method mentioned above.

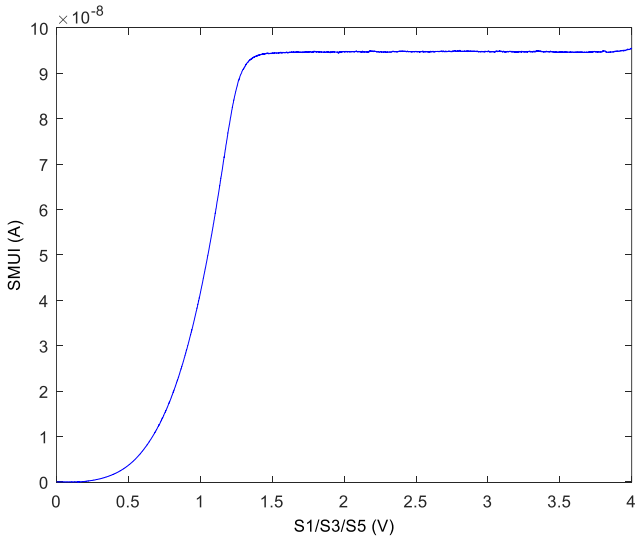


Figure 3.13: Measurement result of the n-fingers turn-on test for *Batch 1 - ns14cw08ch10f*, with n-finger *B1* to test bond-pad *P1*. 1V DC bias is applied through *B1* to *P1* and addressing gates *S1, S3 and S5* are swept from 0–4V. The addressing gate turns on and conducts the n-finger, and the current is measured to calculate the n-finger resistance.

The measurement result of *Batch 1 – ns14cw08ch10f*, *B1* to *P1* is shown in Figure 3.13 as an example. Here, we swept the addressing gates voltage from 0V to 4V. The current through the n-finger is measured as a function of the addressing gates voltage. We determined that these gates switch on at about 0.4V and saturate at around 1.5V. We can measure the saturation current and compute the resistance through this n-finger via Ohms law. In this case, we have the channel current of 94.7nA when the addressing switches reach 1.5V.This current saturates, as it is limited by the channel resistance of the addressing gates, with 1V bias between the n-fingers. Hence, the n-finger resistance is calculated as 1V/94.7nA = 10.56MΩ. We computed the resistances of all test n-fingers, and the results are listed in the tables below.

Test finger	Resistance (MΩ)
B1 - P1	10.56
B2 - P1	10.31
B3 - P1	Compliance
B4 - P2	4.41
B5 - P2	1.5
B6 - P2	7.65
B7 - P2	6.76
B8 - P2	1.05
B10 - P2	Leakage

Table 3.13: n-finger resistances of *Batch 1 – ns14cw08ch10f.*

For the sample *Batch 1 – ns14cw08ch10f*, the n-finger resistances vary from 1.05MΩ to 10.56MΩ. The n-finger *B3* has a relatively lower resistance as it hits compliance before saturation. We exclude it as an outliner. *B10* leaks to *P2* when a small voltage is applied and so it is also excluded. The *Batch 2 – ns14cw04ch10w* sample has no turn-on n-fingers, and we consider this as a sample with errors from the fabrication process.

Test finger	Resistance (MΩ)
B1 - P1	Not turned on
B2 - P1	Not turned on
B3 - P1	43.79
B4 - P2	121.46
B5 - P2	35.8
B6 - P2	Not turned on
B7 - P2	37.97
B8 - P2	85.23
B10 - P2	32.36

Table 3.14: n-finger resistances of *Batch 2 – ns14cw06ch10w*.

Test finger	Resistance (MΩ)
B1 - P1	500
B2 - P1	485.44
B3 - P1	486.62
B4 - P2	546.45
B5 - P2	448.43
B6 - P2	Not turned on
B7 - P2	121.21
B8 - P2	197.04
B10 - P2	Not turned on

Table 3.15: n-finger resistances of *Batch 2 – ns14cw06ch10f.*

From the results above, 74% n-fingers conduct and their resistances lie within the MΩ regime. These resistances vary across different samples by more than an order of magnitude. Initially, we expected the n-finger resistances to be similar since they were made under the same fabrication process; however, the actual measurement turned out to be quite different. We believe that errors may be involved in any step of the process, but this is very challenging to troubleshoot. In addition, we designed the n-finger

resistances to lie within the range of kΩ, but the measured values all fall within the MΩ range. This could be a design issue or fabrication error.

From the design, we know that n-fingers consist of three elements: n-type doping, Al/Pt ohmic contacts and addressing gate switches. Any of these elements could contribute to the unusually high resistances, and should be tested individually to verify this. We fabricated a number of Al/Pt stack structures with the same thicknesses and dimensions as the multiplexer ohmic contacts and measured their resistances; all of the results are within 1kΩ. Hence, this ohmic contact structure provides good electrical conductivity and does not create any significant resistance. We have to further investigate n-type doping, deposition of ohmic contacts onto the samples and the addressing gate switches.

In regards to the leakage issues, we observed that across the 14 randomly selected device from the three different batches, most of the n-fingers have leakage from one finger to the others. These leakages exist and have similar thresholds on both the p-channels and p-well designs, regardless to the channel widths. There are no specific trends and evidence to indicate which type of design and which batch have better leakage tolerances. However, the main cause of leakage is that the p-type channel stoppers or p-well have not reached the desired depth during the fabrication process. This is discussed in more details in the next session.

3.5 SIMS analysis

SIMS analysis [12] is able to study a sample surface or a thin film by sputtering the sample with a primary ion beam and collecting ejected secondary ions from the sample. The mass–charge ratios of these secondary ions are then analysed with a mass spectrometer to determine the composition of the sample from its surface to a certain depth. We mainly used SIMS to study n-type doping and characteristics of the ohmic contacts. In addition, we also studied p-type doping and the silicon dioxide thickness. We selected a *ns14cw08ch10f* sample from *Batch 1* and a *ns14cw08ch10w* sample from *Batch 2*. The two samples were passed to Dr. B. Gong from the School of Chemistry at UNSW to conduct the SIMS experiment.

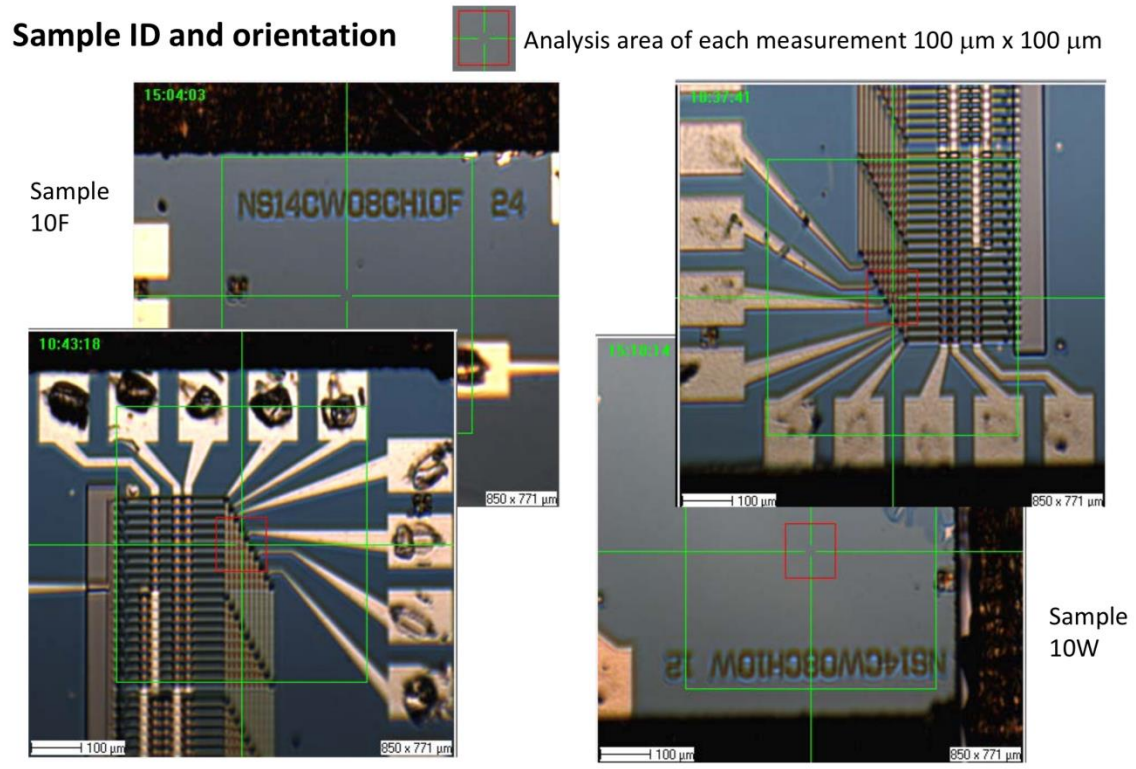


Figure 3.14: SIMS analysis areas of the two samples. The red boxes indicate areas for analysis.

We selected one area with SiO_2 only and another with multiplexer structures to analyse the SiO_2 thickness and the multiplexer structural details, respectively, for both samples. Figure 3.14 indicates the analysis areas with red boxes; the dimensions of these areas are all 100µm × 100µm. We begin with the SiO_2 thickness analysis of both samples. Figures 3.15 and 3.16 show the results of samples *ns14cw08ch10f* and *ns14cw08ch10w*, respectively. We can see from both graphs that the oxygen ion intensities drop significantly at a certain point, concurrent with the rise in silicon ion intensities. These changes indicate that the primary ions have sputtered through the SiO_2 and reached the Si below. Therefore, we can measure the thicknesses according to where the drops occur. From the results, we established that the SiO_2 thickness of sample *Batch 1 – ns14cw08ch10f* is 148nm and that of *Batch 2 – ns14cw08ch10w* is 157nm. Both samples have thinner thicknesses than our design thickness of 200nm. Therefore, we cannot guarantee that the field oxides are sufficiently thick to bypass any effects produced by the gates on top.

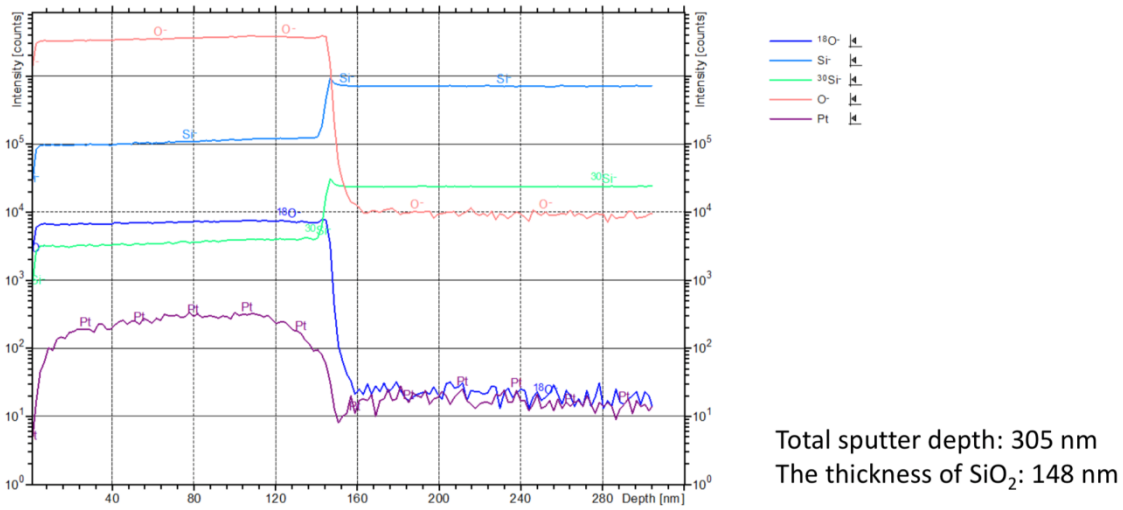


Figure 3.15: SIMS analysis of SiO_2 thickness for sample *Batch 1 – ns14cw08ch10f*

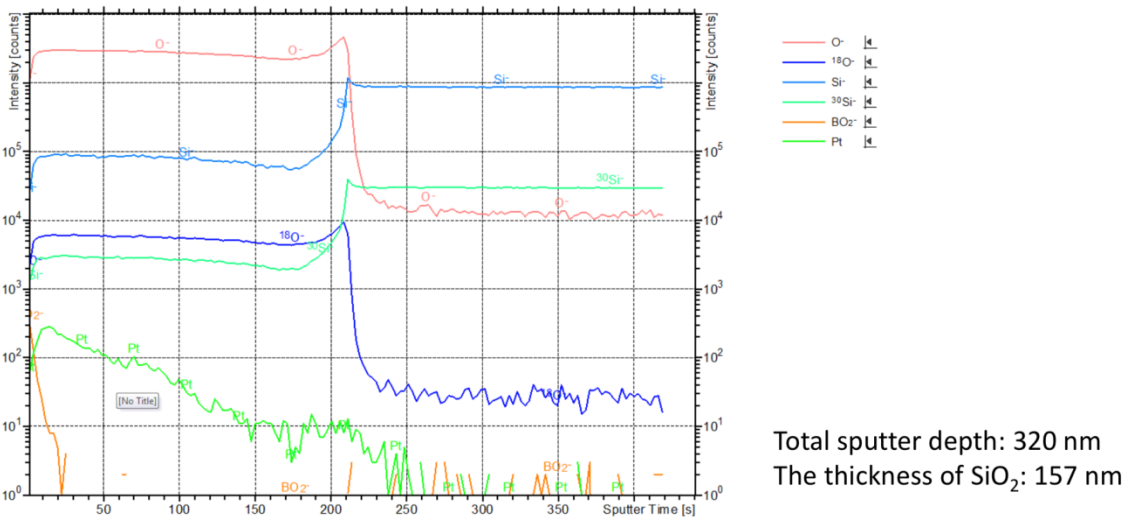


Figure 3.16: SIMS analysis of SiO_2 thickness for sample *Batch 2 – ns14cw08ch10w*

We now move to the detailed study of the multiplexer structure. Figure 3.17 shows the SIMS analysis results of different secondary ions in the form of colour maps for sample *Batch 1 – ns14cw08ch10f*. These maps show the intensity of each specific ion within the analysed area. From the P^- map, we can confirm that the n-type doping channels exhibit good continuity for every n-finger scanned. We can also see good continuity for the top gates from the Al^- maps. Regarding the ohmic contacts, Pt^- and $AlPt^-$ maps indicate that these metals are deposited properly within the contact regions. Note that the dark regions in the SiO_2^- map indicate that oxides in the ohmic contact regions are etched completely before depositing the contact metals. Hence, we are confident that the ohmic contacts are fabricated correctly.

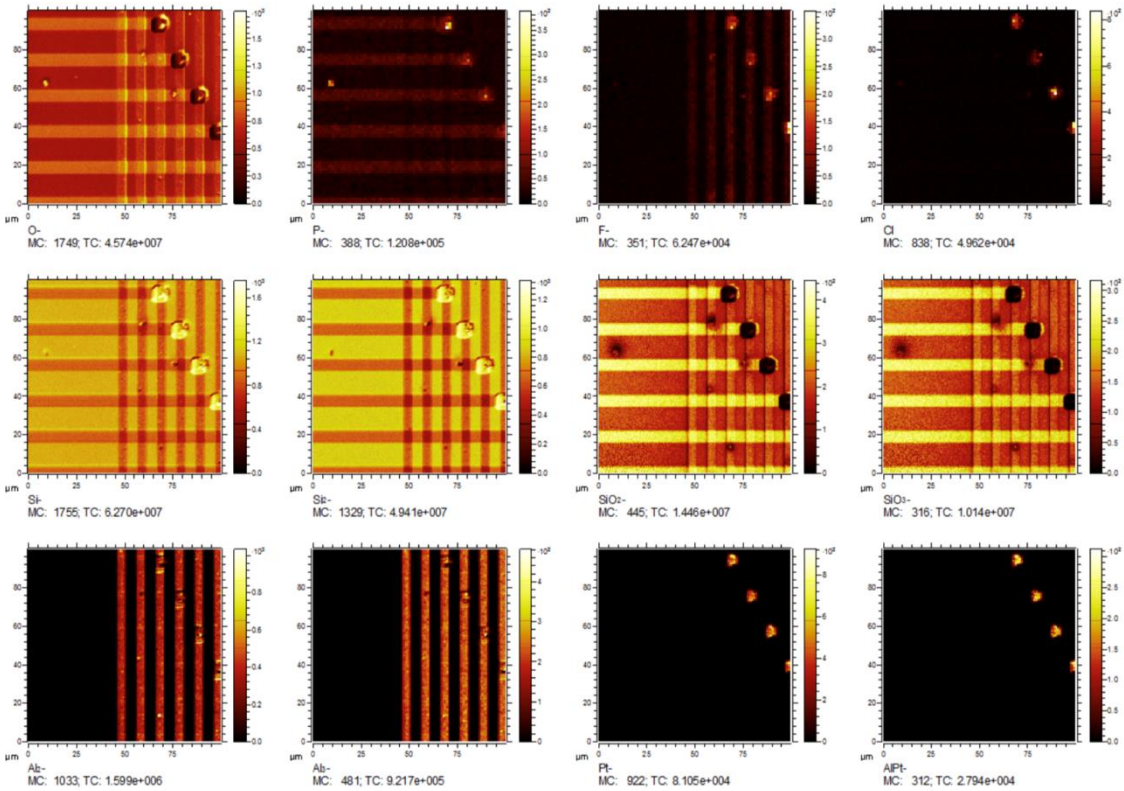


Figure 3.17: SIMS analysis of multiplexer structure for sample *Batch 1 – ns14cw08ch10f*. The colour maps indicate the intensity of each secondary ion within the analysed area. Both the n-fingers and aluminium gates show good continuities. Furthermore, ohmic contacts are deposited properly.

We observe similar results for the sample *Batch 2 – ns14cw08ch10w*, as shown in Figure 3.18. However, the top gates are more likely to be made of *Pt* instead of *Al*, as they have higher intensity in the Pt^- map. We believe that this is a mistake made by the process engineer during fabrication, but this does not affect the conductivity of the top gates.

From the results of the two samples described above, we are convinced that the ohmic contacts are properly deposited onto the multiplexers. Considering the Al/Pt stack structure resistance test results mentioned earlier, clearly, the ohmic contacts would not contribute any factor towards the MΩ range resistance values. We now focus on the study of n-fingers. The only parameter that determines the doping (sheet) resistance is the doping concentration. Thus, we use SIMS to analyse the phosphorus doping concentration of the n-fingers.

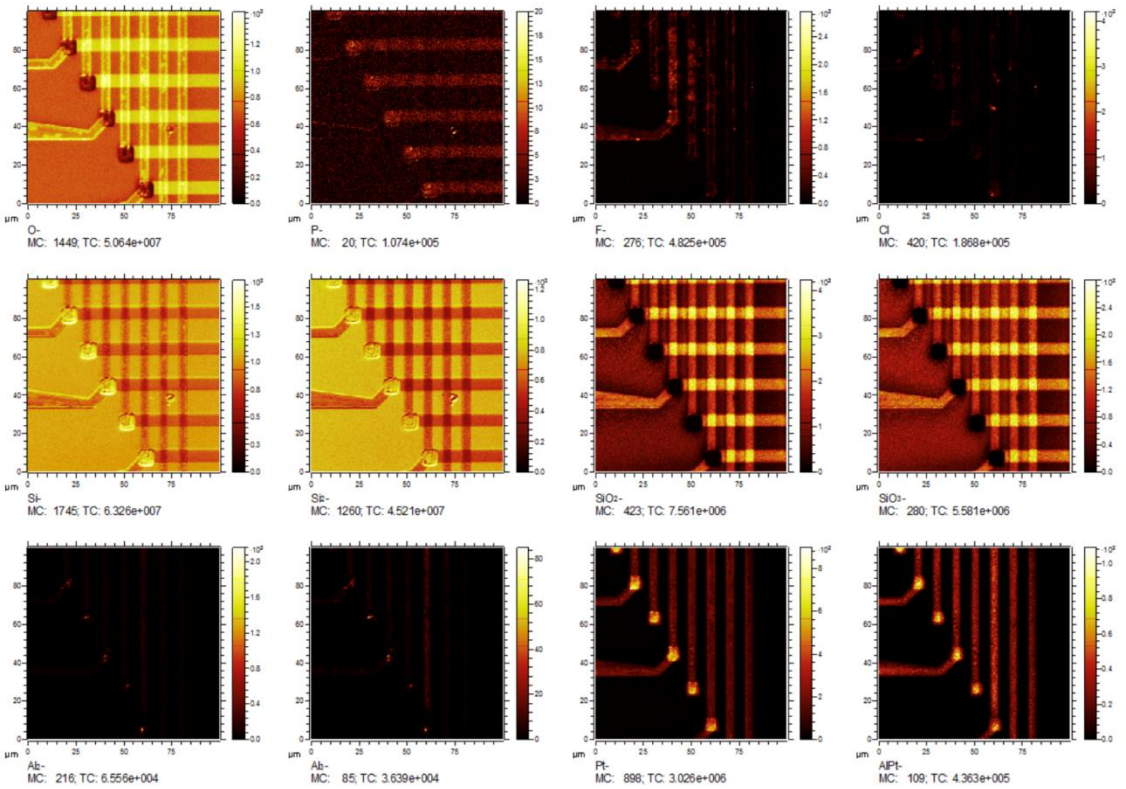


Figure 3.18: SIMS analysis of the multiplexer structure of sample *Batch 2 – ns14cw08ch10w*. The n-fingers and top gates exhibit good continuity, and ohmic contacts are fabricated properly. The top gates are likely to be mistakenly deposited with Pt instead of Al.

The phosphorus depth profile analyses for samples *Batch 1 – ns14cw08ch10f* and *Batch 2 – ns14cw08ch10w* are shown in Figure 3.19 and 3.20, respectively. As shown by the purple line in Figure 3.19, the *P* concentration increases gradually as the sample is sputtered. The concentration reaches 10^{20} at 400s sputter time and remains at the same level, which indicates that the primary ions have reached the depth of the n-type doping and the target secondary ions are detected and profiled. We obtain a similar result for the sample shown in Figure 3.20, where the *P* concentration (red line) reaches 10^{20} at about 200s sputter time.

The results from both figures show that the phosphorus concentration of the n-fingers is 10^{20}, which agrees with our design doping concentration. The n-finger resistance at this level of concentration is negligible as the sheet resistance is less than 1Ω [13]. Hence, we are confident in concluding that n-type doping does not contribute a significant value to the n-finger resistance within the MΩ range.

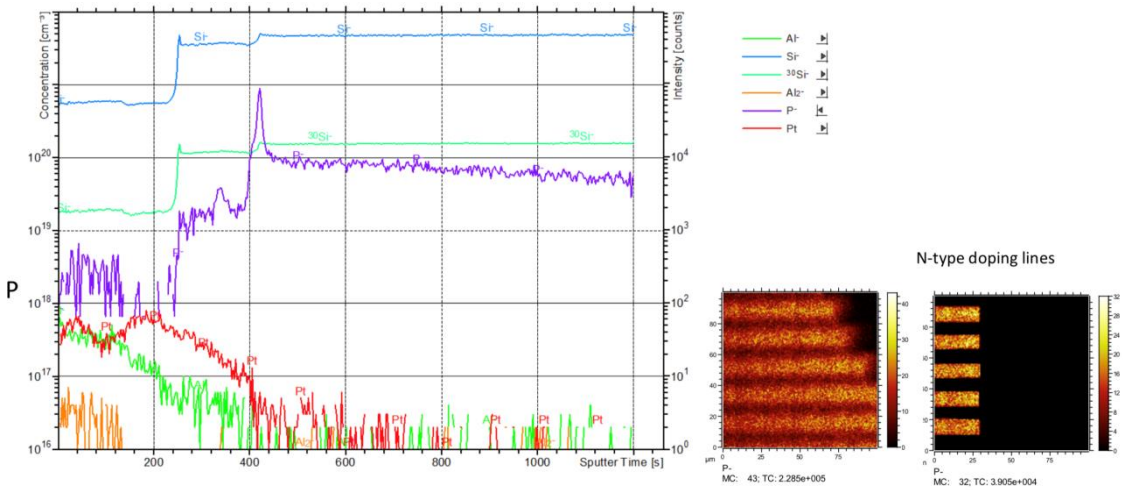


Figure 3.19: SIMS analysis of phosphorus depth profile for sample *Batch 1 – ns14cw08ch10f*

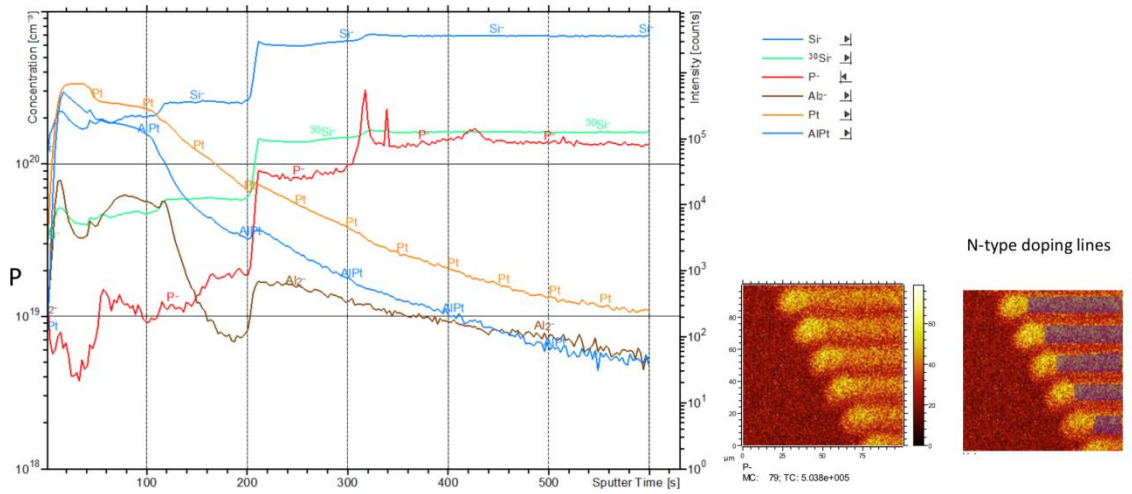


Figure 3.20: SIMS analysis of phosphorus depth profile for sample *Batch 2 – ns14cw08ch10w*

Subsequently, we performed the same analysis to obtain the boron depth profile for the two samples. The results are shown in Figures 3.21 (black line) and 3.22 (red line). From both figures, we can see that the boron concentration drops rapidly from 10^{17} to 10^{16} as sputtering starts. The concentration drops below 10^{15} as the samples are sputtered further. These results reveal that boron diffusion for both samples is not properly driven into the silicon, and the channel stoppers may not even exist between the n-fingers. We believe that this happens to all of the multiplexer samples, as we have measured all tested samples to have leakages across n-fingers. Hence, we conclude that the p-type channel stoppers are not diffused properly into the silicon substrate, such that they do not reach the desired depth at the specified concentration, and we believe that this is the main cause of n-finger leakage.

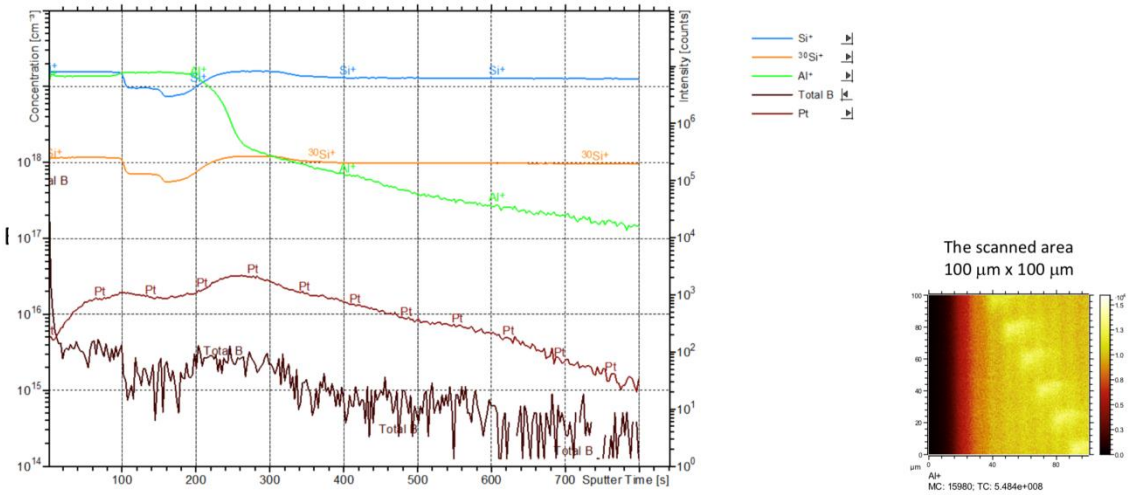


Figure 3.21: SIMS analysis of boron depth profile for sample *Batch 1 – ns14cw08ch10f*

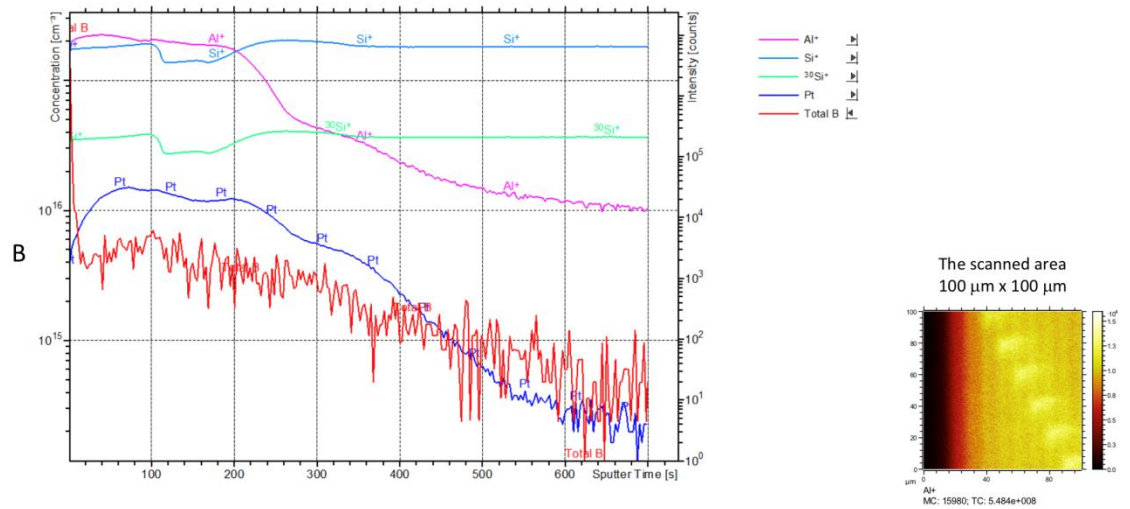


Figure 3.22: SIMS analysis of boron depth profile for sample *Batch 2 – ns14cw08ch10w*

To summarise the SIMS analyses, we observe that the silicon dioxide thicknesses are thinner than our design thickness. Moreover, the doping concentration and depth of boron do not meet the standards for p-type channel stoppers. However, the ohmic contacts and n-type doping are fabricated properly. For the n-finger MΩ resistances, the only element remaining to be examined is the addressing gate switches.

3.6 Design modification

We analyse the addressing gate switches by performing a theoretical calculation of MOSFET channel resistance. The source-drain current of a MOSFET is given by the equation [14] below, where the MOSFET is in saturation mode:

$$I_D = \frac{W}{L}\frac{\mu_n C_{ox}}{2}\left(V_{gs} - V_{th}\right)^2$$

where W and L are the MOSFET channel width and length, μ_n is the electron mobility, C_{ox} is the thin-oxide capacitance, V_{gs} is the voltage between gate and source, and V_{th} is the threshold voltage.

Here, we ignore the effect of channel length modulation as we do not operate the switches in pinch-off mode. Hence, the channel resistance is:

$$R = \frac{V_{DS}}{I_D} = \frac{L}{W}\frac{2V_{DS}}{\mu_n C_{ox}\left(V_{gs} - V_{th}\right)^2}$$

The thin-oxide capacitance is given by the equation [15]:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where $\varepsilon_0 \approx 8.854\times10^{-12}$ is the dielectric constant, $\varepsilon_r = 3.9$ is the relative permittivity for silicon dioxide, A is the oxide area, and d is the oxide thickness. We cannot measure the actual thin-oxide thicknesses, since they are covered by the aluminium gates. Therefore we assume our design thickness, d = 7.5nm. We take the thin-oxide width and length as 4μm and 6μm, respectively, which are the dimensions of a tested *ns14cw06ch10w* sample. Hence, the thin-oxide capacitance is calculated as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r A}{d} = \frac{8.854 \times 10^{-12} \times 3.9 \times 4 \times 10^{-6} \times 6 \times 10^{-6}}{7.5 \times 10^{-9}} = 110.5fF$$

The electron mobility is temperature dependent and it is difficult to determine this parameter for our samples. An electron mobility of 12,000cm^2/Vs for an n-channel MOSFET is measured at 4K in this publication [16] and we take this value as a reference for our calculation. Our source-drain bias is 1V and gate voltage is 2V, with a threshold voltage of 0.4V. Hence, our channel resistance is calculated as:

$$R = \frac{6 \times 10^{-6}}{4 \times 10^{-6}} \frac{2 \times 1}{12000 \times 110.5 \times 10^{-15} \times (2 - 0.4)^2} = 883.77 M\Omega$$

This value agrees with our n-finger resistances within the MΩ range. The n-fingers have a lower value, possibly because the multiplexer samples have a higher electron mobility.

From the theoretical calculations above, we can see that the current design of the addressing gate switches creates a very high resistance, which makes device operation on the multiplexer difficult. This requires us to redesign the thin-oxide window structure. However, to achieve kΩ-range resistances, we need to reduce the current n-finger resistance by 10^3 ~ 10^4 times. To do so, we either need to increase the thin-oxide capacitance or the electron mobility, or the product of both parameters, by 10^3 ~ 10^4. The electron mobility is very difficult to determine for the samples used here, and if we increase the thin-oxide capacitance by increasing *A* and/or decreasing *d*, these parameters would exceed our design specifications. Furthermore, no alternative dielectric materials are available in our laboratory that would help to increase the capacitance. All these results suggest that the address gates have a flaw in the original design and they need to be redesigned to an entirely new structure.

In terms of design modification, the addressing switches need to be redesigned with a lower resistance. We also need to grow a thicker field oxide, and ensure that it is at least 200nm. Regarding the channel stoppers, we can implement ion implantation so that boron can be shot into the silicon substrate at a controlled depth and concentration. Feedback has been provided to the multiplexer designer and the project supervisor and co-supervisors. The Si-MOS multiplexer project is now on hold until a further decision is made.

Chapter 4
Depletion mode charge sensor

This chapter covers the depletion mode charge sensor project, from design to fabrication and measurement. This project is carried out in collaboration with C. Zhang, another Master by research candidate in the group. Zhang carried out the device design and computer-based simulation in her first year of study, while I fabricated the devices, and we measured together during our second year. We begin by introducing the device design in this chapter, followed by studies relevant to fabrication. We fabricated five batches of devices and measured a number from each batch. Two devices were found to pass 4K dipping, and we discuss their dilution fridge measurements.

4.1 Design

The depletion mode charge sensor is a modified version of our qubit device SET sensor. From Figure 1.2, we can see in the current design the ST gate overlaps the two barrier gates, LB and RB. As mentioned earlier, this structure may create a complex conduction band profile in silicon when the device is cooled, and result in strain-induced quantum dots. The depletion mode charge sensor is designed such that the two barriers are separated from the top gate, in order to minimise strain effects, while we are still able to pinch off the device in depletion mode.

Figure 4.1 shows the design of the device. We separate the barriers and top gate by pulling the two barriers (blue) SLB1(2) and SRB1(2) backwards to a separation distance of 30nm. The top gate (red) ST1(2) shape is also modified such that there is a convex point at the centre. A confinement barrier is added near this centre point to assist confining the quantum dot. Both devices are identical in terms of their design parameters with opposite orientation. We expect to operate the device so that it forms a single quantum dot (green) under the top gate centre convex point while the two barriers pinch off the top gate channel in depletion mode.

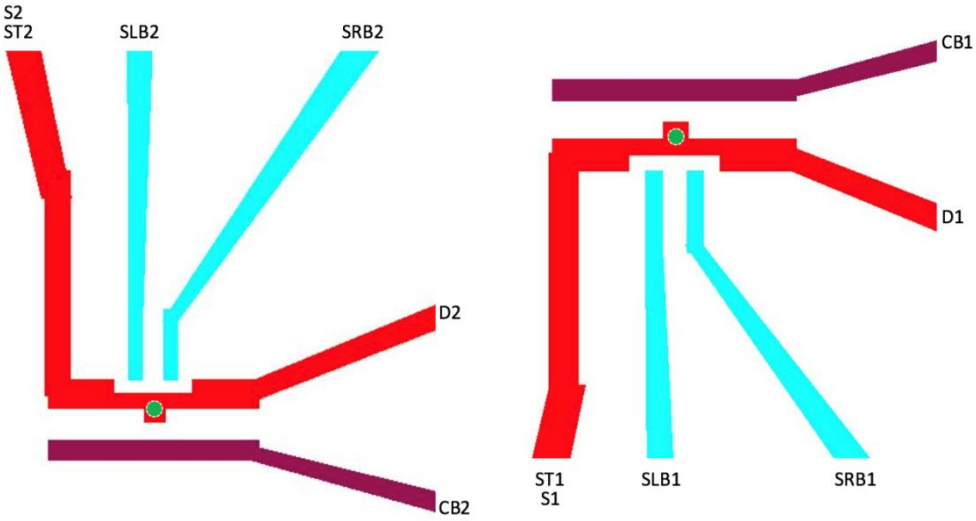


Figure 4.1: Design of the depletion mode charge sensors. Two devices with identical design are packed within one single pixel with one oriented opposite to the other one. The top gates are coloured in red and labelled as ST1 and ST2, respectively. The barrier gates are shown in blue and labelled as SLB1(2) and SRB1(2), the left and right barriers for each device. CB1 and CB2 are the confinement barriers. We design the device to form a quantum dot at the centre of the top gate, as labelled in green.

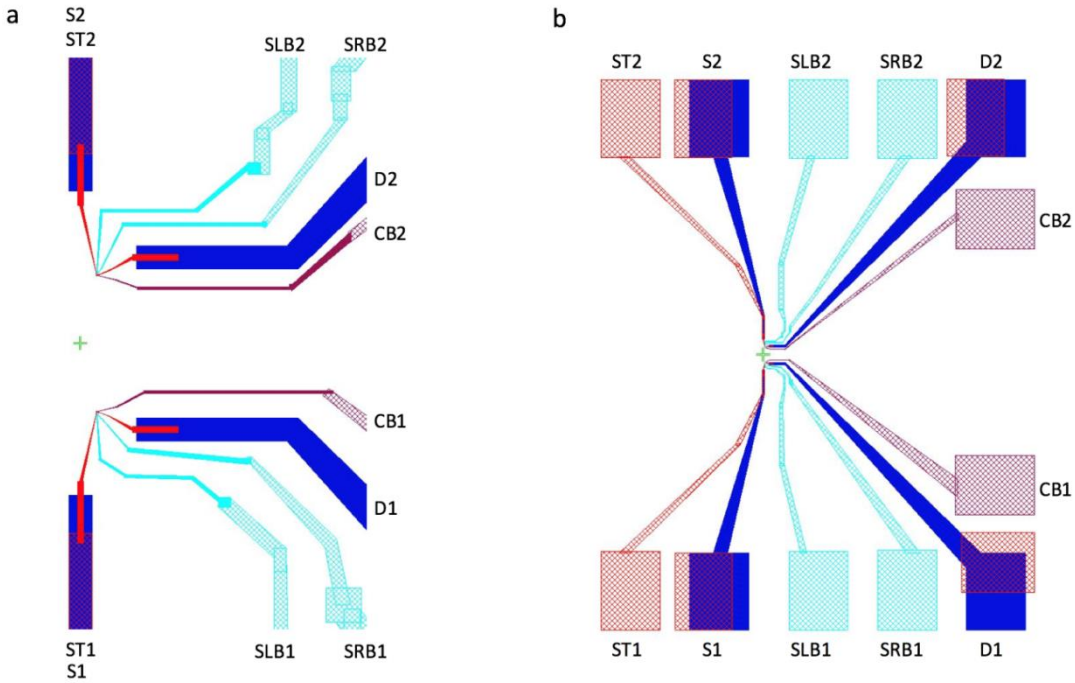


Figure 4.2: a) Nanoscale design view showing the nanostructures of the device connections. ST1 and ST2 run on top of their corresponding source ohmics S1 and S2 and return to drains D1 and D2, creating a conduction path when turning on the device. b) Microscale design view showing the microstructure fan-out and bond-pads of the devices.

The nanoscale view of the design shown in Figure 4.2a indicates the nanostructure device connections and a single pixel of a sample batch at its nano-region. The four dark blue fingers are phosphorus-doped ohmic regions, which are used as sources and drains for the devices. Since each device only needs two ohmics, one source and one drain, we can fabricate two devices in one pixel. The top gates ST1 and ST2 overlap the sources S1 and S2, respectively, and connect to their drains D1 and D2, respectively; thus current paths can form when the devices are turned on. Boron-doped channel stoppers are placed between every ohmic region, which is not shown in the design, but will be visualised later in SEM images. These channel stoppers are designed to prevent leakages across the ohmic regions. Zooming out further, the design microscale view in Figure 4.2b shows the device microstructure fan-outs and bond-pads for gate electrodes and ohmic regions.

4.2 EBL dose test and test write

Before making a batch of devices, we carried out a trial fabrication and formulated the parameters in each process. Our trial includes two parts: the EBL dose test and EBL test write. We begin with the dose test. The aim of the dose test is to find the exact amount of electron dosage applied to fabricate the device gates that produces the optimal result; i.e. the pattern and dimension should be as close as possible to the design.

We selected a dummy sample to carry out the dose test. First, the sample was coated with approximately 160nm PMMA A4 resist and post-baked on a hot plate. The sample was then loaded into our EBL system, Raith 150 TWO [17], set up with a 7.5μm aperture size and 100μm write-field. We test-wrote the barrier gates and top gates separately at four different electron dosages: 500μC, 550μC, 600μC and 650μC. The patterned sample was then developed in MIBK/IPA, deposited 40nm of aluminium via e-beam evaporation [18], and lift-off [21] in Acetone for 2~3 hours. Finally, the sample was rinsed with IPA and inspected under SEM. Figures 4.3 and 4.4 show the dose test results for the barrier gates and top gates, respectively. The four subplots *a, b, c* and *d* in both figures represent the results at dosages of 500μC, 550μC, 600μC and 650μC. By

inspecting the SEM images, we decided that Figure 4.3b and Figure 4.4c show the most promising results. Hence, we chose 550μC for the barrier gates and 600μC for the top gate as the EBL dosages to make our devices.

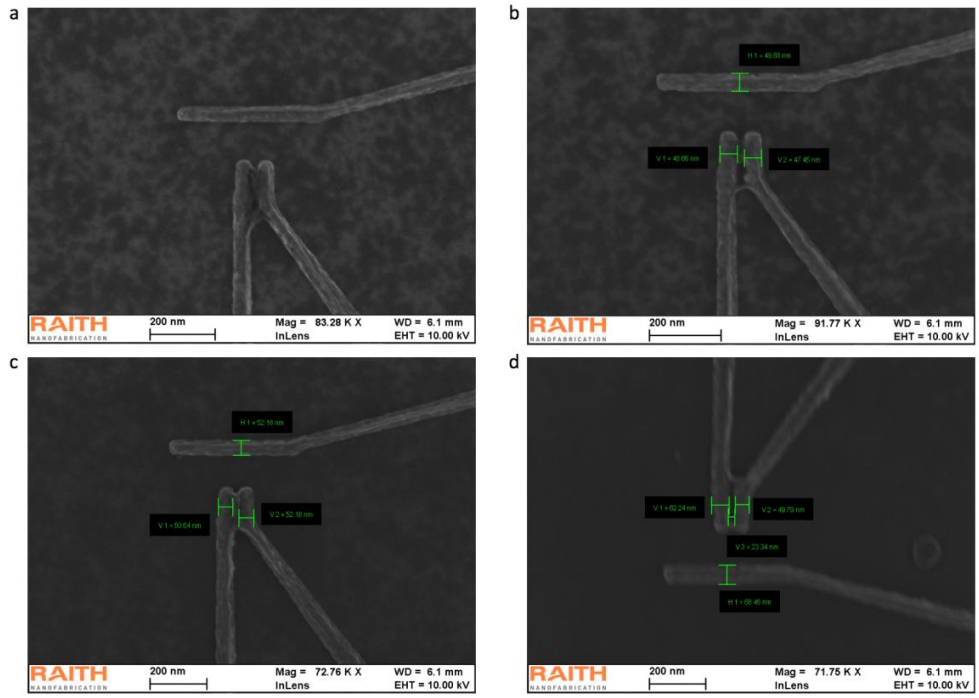


Figure 4.3: SEM images of dose test results for barrier gates at dosages of: (a) 500μC, (b) 550μC, (c) 600μC and (d) 650μC.

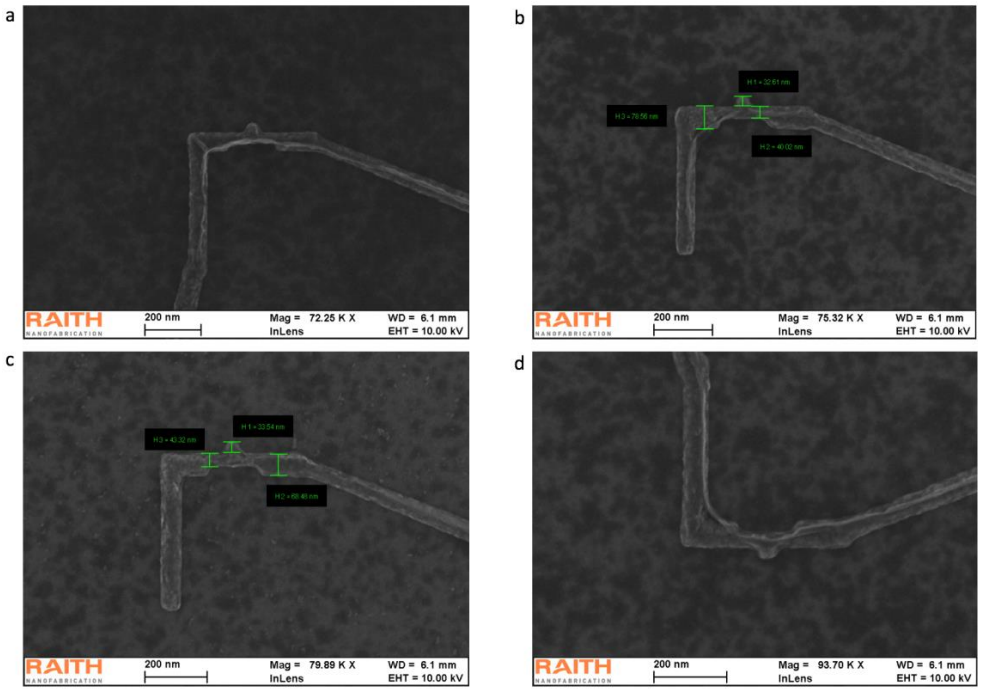


Figure 4.4: SEM images of dose test results for top gates at dosages of: (a) 500μC, (b) 550μC, (c) 600μC and (d) 650μC.

Next, we move to the EBL test write. The idea of this test is to verify whether the actual fabrication outcome matches its design. In general, the actual patterns do not exactly match to the design parameters, and we need to adjust the design according to the pattern dimensions. In the test write, we fabricated all of the gate electrodes in a single EBL write using the same fabrication process and parameters as in the previous dose test. Furthermore, we test wrote a number of variant structures by changing the barrier gate widths and the distance between the barriers and top gates.

The test write results of these variants are shown in Figure 4.5 with different subplots. In Figure 4.5a, both barriers are too wide and placed too close to each other, in addition to being too close to the top gate. As a consequence, all of the patterns merged. The result of a thinner barrier design variant is shown in Figure 4.5b. Here, we can see that the barrier patterns are thinner than in Figure 4.5a, but the SLB gate is missing. We believe that the barriers are still slightly too wide, so that the resist between the two barriers becomes too narrow after EBL patterning. The result is that this very narrow resist cannot support itself and collapses onto the SLB pattern during resist development, so that no metal is deposited on the desired area to form the SLB gate. Figure 4.5c shows the result of two separated barriers, which are however still merged with the top gate. The result of the same barrier width as in Figure 4.5a but a higher separation between the barriers and top gate is shown in Figure 4.5d. Here the two barriers are merged, but are separated from the top gate. We combined the design parameters from Figures 4.5c and 4.5d to test write the device, and the result is shown in Figure 4.5e with measurements. The barrier gates are roughly 44nm wide with a 27nm gap in-between, which is within the tolerance of our design. Moreover, the barriers are aligned to the top gate convex point and separated by 27nm. We conclude this as a successful test write. The same tests are performed on the other device with the opposite orientation and a similar result is achieved, as shown in Figure 4.5f.

We also ran the test write on nanostructure and microstructure connections, and the results are shown in Figures 4.5g and 4.5h, respectively. We can see from Figure 4.5g that the top gate electrodes are aligned to the source and drain ohmic regions. The fan-outs and bond-pads from both subplots indicate good connections of the device gates.

From Figure 4.5h, we can see a square enclosure in a light colour with lines extending towards the centre of the pixel between every ohmic region. These are the p-type channel stoppers that prevent current leakage from occurring between the n-type ohmics.

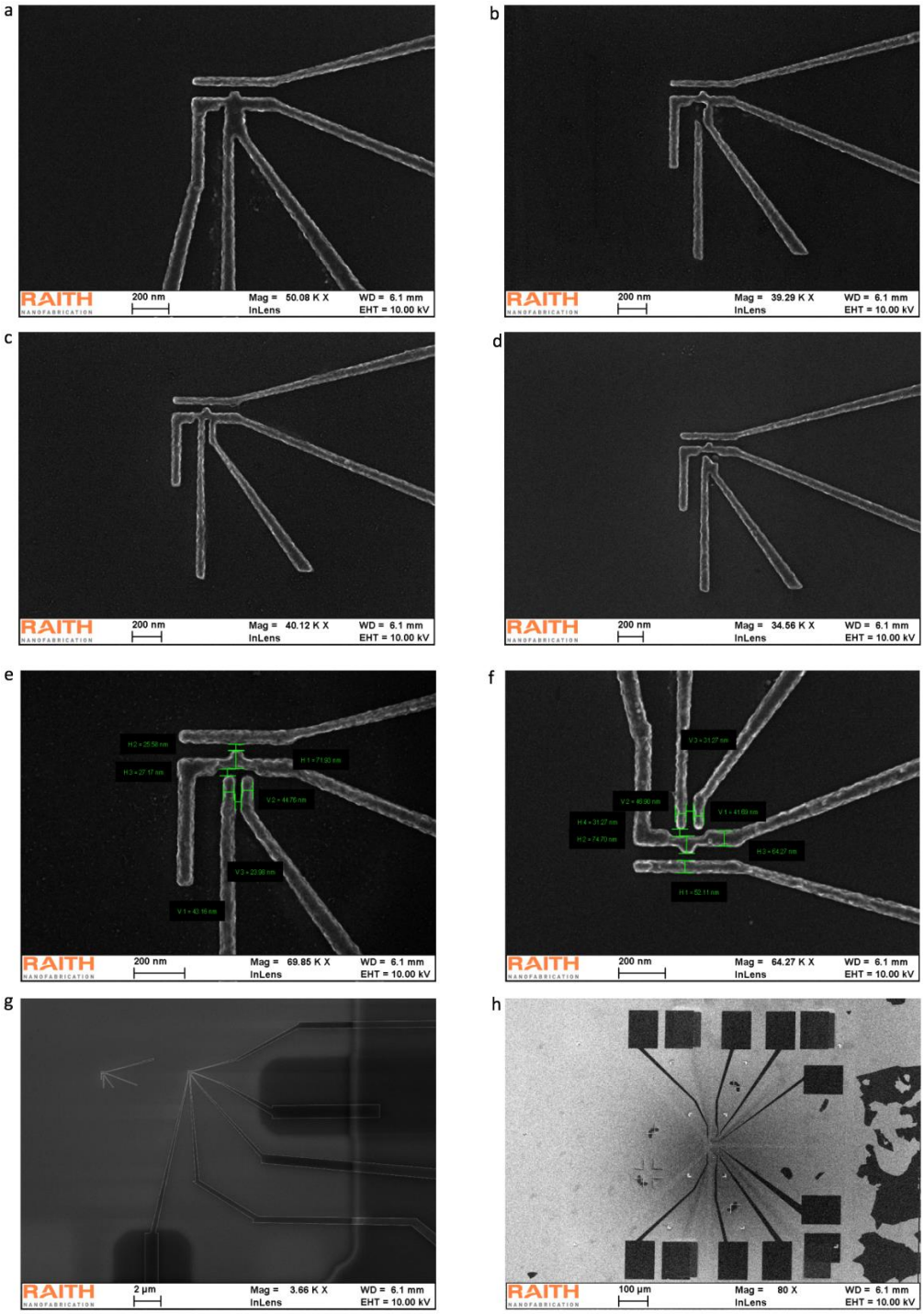


Figure 4.5: EBL test write results. (a) Barrier gates are too wide and too close to the top gate. (b) Barriers are narrowed but SLB is missing due to collapse of the resist. (c) Barriers narrowed further and separated. (d) Barriers moved downwards and separated from top gate. (e) and (f)

Successful test writes with measurements. (g) Nanostructure connections, with source and drain aligned to their ohmic regions. (h) Microstructure fan-outs and bond-pads.

4.3 Measurement

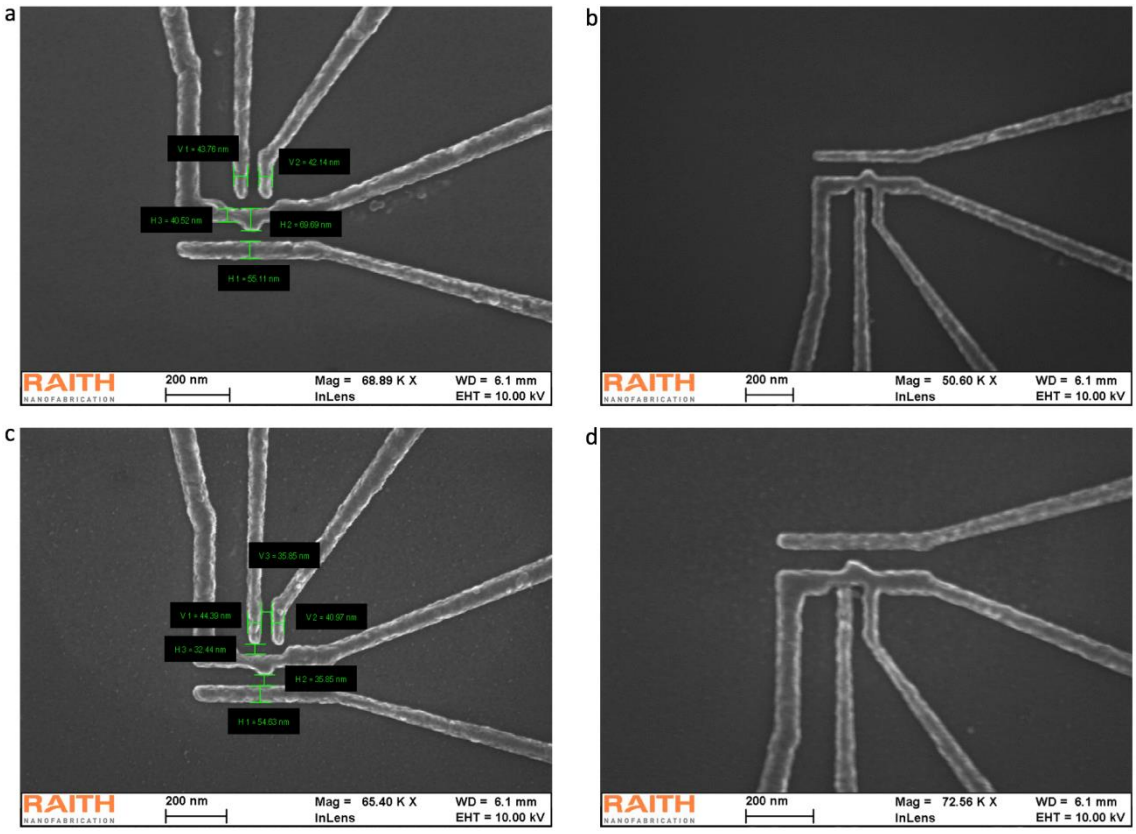
With the success in EBL test writes, we can now fabricate device batches and conduct experiments. Throughout the project, we fabricated five batches of the depletion mode charge sensors, and found one device from *batch 2* and one from *batch 5* that passed 4K dipping. These samples were loaded into the dilution refrigerator and measured at the base temperature of ~50mK. In the following we mainly focus on discussing the results of these two samples, along with a dipping summary of all the tested devices from each batch.

4.3.1 Batch 1

In the first batch, we used the same design, process and parameters as in the test write and fabricated 15 pixels of devices in a 3×5 layout, using a sample piece from the *"MV12"* natural silicon stock. The sample was then diced and bonded to a PCB one pixel at a time for measurement. Table 4.1 shows the chip map of this batch with a brief summary. We imaged pixels R3C4 and R2C5 using SEM because they had fabrication defects, but were still able to make use of them to verify the nanofabrication outcome. SEM images of the two pixels are shown in Figure 4.6.

	C1	C2	C3	C4	C5
R3	Ready to measure	Dipped Turn on & pinch off, No CO on top device Bad bottom device	Ready to measure	Broken SRB on bottom device Used for SEM	Dipped Bad pinch off on top device Bad bottom device
R2	Ready to measure	Ready to measure	Ready to measure	Ready to measure	Misalignment due to missing alignment markers Used for SEM
R1	Ready to measure	Dipped Bad pinch off on top device Bad bottom device	Ready to measure	Dipped Turn on & pinch off, No CO on top device Bad bottom device	Dipped Bad pinch off on top device Bad bottom device

Table 4.1: Chip map of depletion mode charge sensor *Batch 1* with a brief summary.



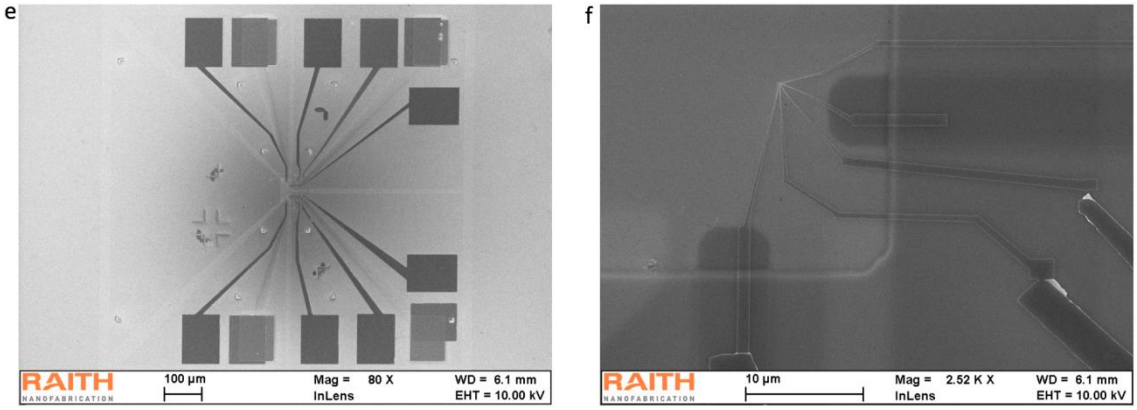


Figure 4.6: SEM images of depletion mode charge sensors *Batch 1*, (a) top and (b) bottom devices of R3C4; (c) top and (d) bottom devices of R2C5. (e) R3C4 microstructure showing broken SRB1 fan-out. (f) R2C5 fan-out area showing misalignment.

As shown in Figures 4.6a–d, both pixels display good images of the devices on top but the devices at the bottom have merged, which contradicts the test write results. This is probably due to the electron beam losing its proximity at some sections within a writefield; we believe that this problem happens to all other pixels. However, the devices on top turn out to be well fabricated and thus we have confidence to measure them. As presented in Table 4.1, we dipped five pixels in the 4K dewar. Only R3C2 and R1C4 indicate that their top devices turn on and pinch off, while the other three pixels provide poor pinch-off results on their SLBs/SRBs. Note that all dipped pixels were found to have merged bottom devices as we carried out the leakage test, i.e. ST1, SLB1 and SRB1 are short circuited to each other. Here, we discuss the results from the R3C2 top device; R1C4 achieves very similar results.

The experiment was set up by applying a 100µV AC bias through S2 and D2 using a lock-in amplifier, and connecting each gate to a DC power source. First, we test the device turn-on by sweeping ST voltage; the result is shown in Figure 4.7a. ST2 turns on at approximately 1V and the current increases as the top gate voltage increases. Both SLB2 and SRB2 can pinch off the current channel at about -4V, as shown in Figures 4.7b and 4.7c, respectively.

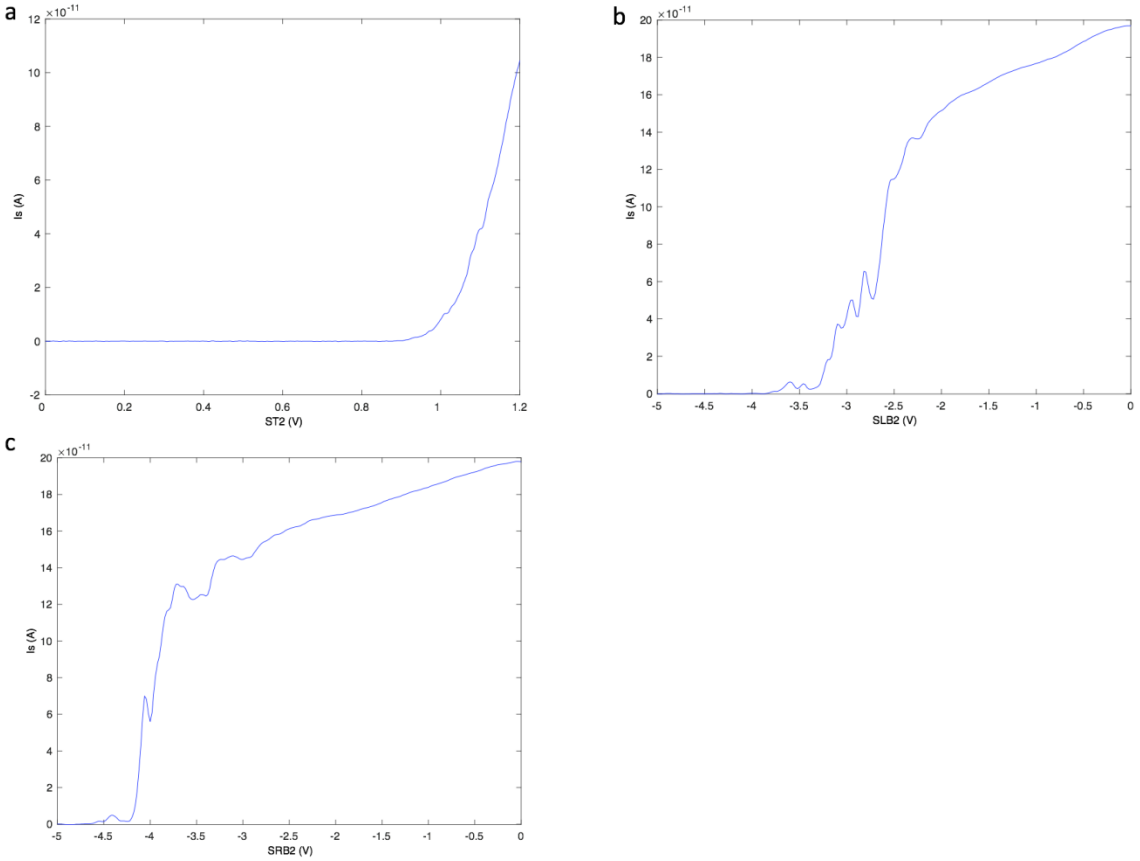


Figure 4.7: Depletion mode charge sensor *Batch 1 – R3C2* 4K dipping results. (a) ST2 turn-on curve; (b) SLB2 and (c) SRB2 pinch-off curves.

Next, we characterised the device by sweeping the channel current as a function of SLB2 and SRB2 voltages; the result is shown in Figure 4.8. Evidently, this device behaves similarly to an SET, where the colour map indicates that the top gate can be pinched to form a quantum dot, and the quantum dot shows dependencies on the two barriers with two different slopes. We then attempted to tune this device to its high transconductance points and seek Coulomb oscillations. However, we were not able to obtain any oscillations when sweeping on ST2, SLB2 or SRB2.

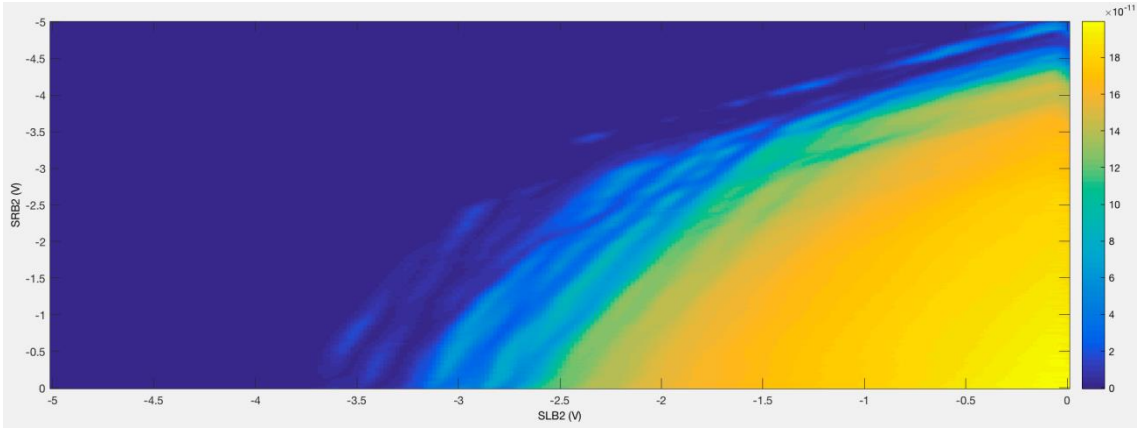


Figure 4.8: Depletion mode charge sensor *Batch 1 – R3C2* 4K dipping result, with the top gate channel current plotted as a function of SLB2 and SRB2 voltages. The plot shows that a quantum dot can form under ST2 with dependencies on SLB2 and SRB2.

From the *Batch 1* dipping results, we verify that the depletion mode charge sensors have similar characteristics to the normal SET. We can turn on a device and pinch off the current channel to form a quantum dot under the top gate. The dot also exhibits dependencies on the two barriers, indicated by two different slopes. We have not yet obtained Coulomb oscillations or diamonds on the device tested in this batch. Since fabrication defects occurred on the bottom devices, we decided to abandon the rest of the batch and move onto fabricating a new batch to fix the bottom devices issue.

4.3.2 Batch 2

Before making the second batch, we quickly repeated the test writes for the bottom devices and investigated the proximity shift problem. The solution was to pull the two barrier gates slightly further from the top gate, so that the actual patterns no longer merged. We used the same design and parameters from *Batch 1*, with the introduction of a 5nm aluminium oxide layer between the barrier gates and top gate via ALD [19]. Addition of this aluminium oxide layer can reduce the capacitive coupling between the SET island (or dot) and the top gate, so that it enhances the control of the SET conduction by the tunnel barrier gates. The ALD layer was also applied to all future batches of devices reported in this thesis. Therefore, in terms of process, we first patterned and deposited CB, SLB and SRB; then we deposited the aluminium oxide ALD layer; and finally we patterned and deposited ST. For *Batch 2*, we selected a 4×4 sample from the *"MV14"* natural silicon stock and made 15 pixels of devices. Table 4.2

shows the chip map with a brief summary. We clamped the sample to the EBL stage on pixel R4C1 so that there was no device on this pixel. Four pixels along R1 experienced misalignment, and R4C2 was imaged under SEM.

	C1	C2	C3	C4
R4	Raith clamp No device	SEM	Ready to dip Dipped 28/3/17 Bad CO and diamonds	Ready to dip
R3	Ready to dip	Ready to dip	Ready to dip Dipped 30/3/17 Not very good SLB1 vs SRB1	Ready to dip Dipped 31/3/17 Both SD leakages
R2	Ready to dip Dipped 4/4/17 Good / into RF2V	Ready to dip	Ready to dip Dipped 24/3/17 Bad SLB1 vs SRB1	Ready to dip Dipped 27/3/17 Bad SLB1 pinch off SET2 SD leakage
R1	Misalignment	Misalignment	Misalignment	Misalignment

Table 4.2: Chip map of depletion mode charge sensor for *Batch 2*.

Figure 4.9 shows the SEM images of R4C2. We selected this pixel deliberately for SEM imaging due to the lift-off defect, as circled in red in Figure 4.9b, but this did not affect the inspection of the fabrication outcome. Figures 4.9a and 4.9b show a good connection on the bond-pads and fan-outs of both devices. Desirable device structures and alignments are shown in Figures 4.9c and 4.9d for the top and bottom devices, respectively. Features of the barrier and top gates were measured and found to be within tolerance. Hence, we are confident that we can measure devices on this batch. We dipped six pixels at 4K and found a device on R2C1 that passed 4K dipping. The other five pixels have issues such as source/drain leakage and poor barrier pinch-off, so we only discuss further the pixel on R2C1.

The experiment was set up using the same configuration as the device in *Batch 1*. The top device on R2C1 also experienced source/drain leakage, and this leakage path could not be pinched off even with negatively biasing SLB2 and SRB2. However, the 4K

dipping results for the bottom device seemed promising. Figure 4.10 shows the device turn-on and barrier pinch-off. With the introduction of a 5nm aluminium oxide ALD layer, we can see that the ST turn-on voltage is at approximately 1.8V, which is higher than that of the device tested in *Batch 1*. We expect this because an increase in dielectric thickness would require a higher turn-on voltage, and the experimental result approves this statement. In contrast, the two barriers can both pinch off at less negative voltages. The *Batch 1* device pinched off beyond -3V, while this device fully pinches off beyond -1.5V for both SLB1 and SRB1. Again, the additional ALD layer assists the pinch-off effects since the ST1 gate is now less coupled to the 2DEG underneath. As a result, channel depletion is easier on both barriers.

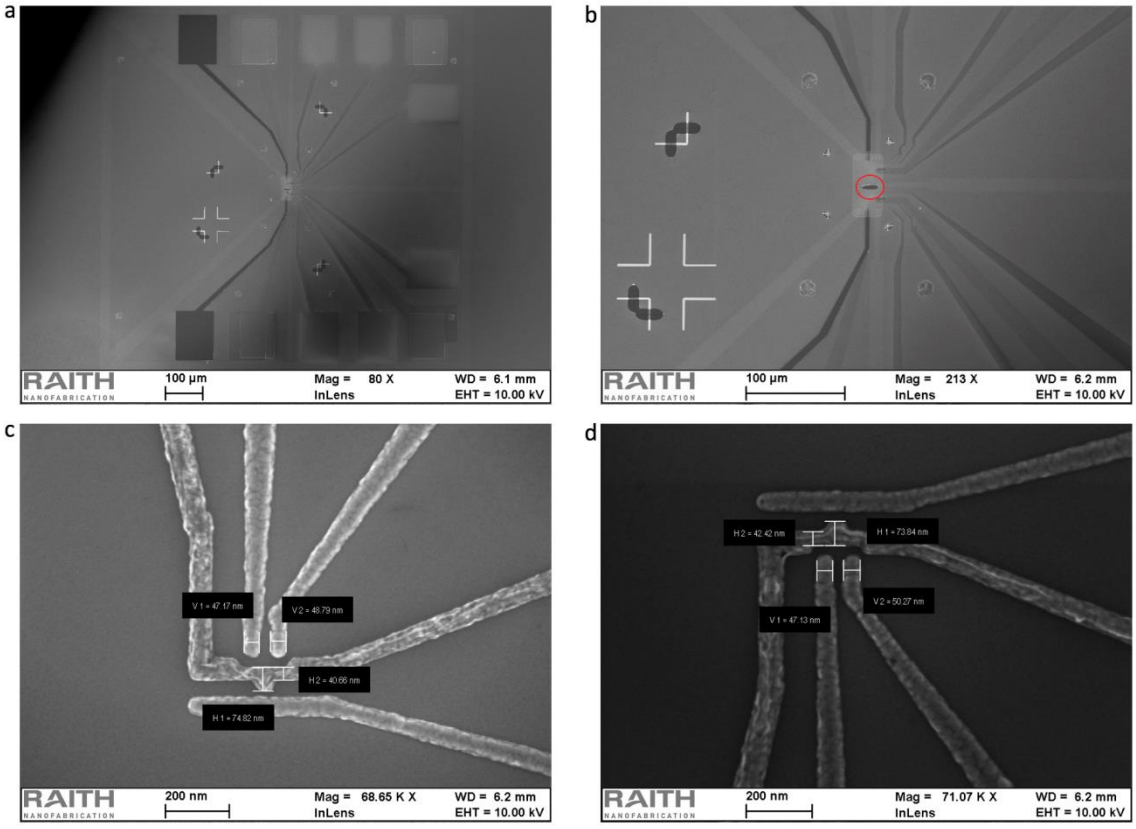


Figure 4.9: SEM images of depletion mode charge sensor *Batch 2* – R4C2, (a) entire pixel and (b) nanoscale region, with a lift-off defect circled in red. (c) Device on the top and (d) bottom.

We now explore the device characterisation through the measurement of channel current as a function of SLB1 and SRB1 voltages; the result is shown in Figure 4.11. We can see two slopes showing the dependencies of the two barriers, which is similar to the result obtained from the device in *Batch 1*. Again, we tuned the device to its high

transconductance point and sought Coulomb oscillation. We obtained a result, shown in Figure 4.12, that could indicate a Coulomb oscillation occurring; but it is affected by a number of quantum dots under the ST gate. Hence, the oscillation curve is less regular than expected.

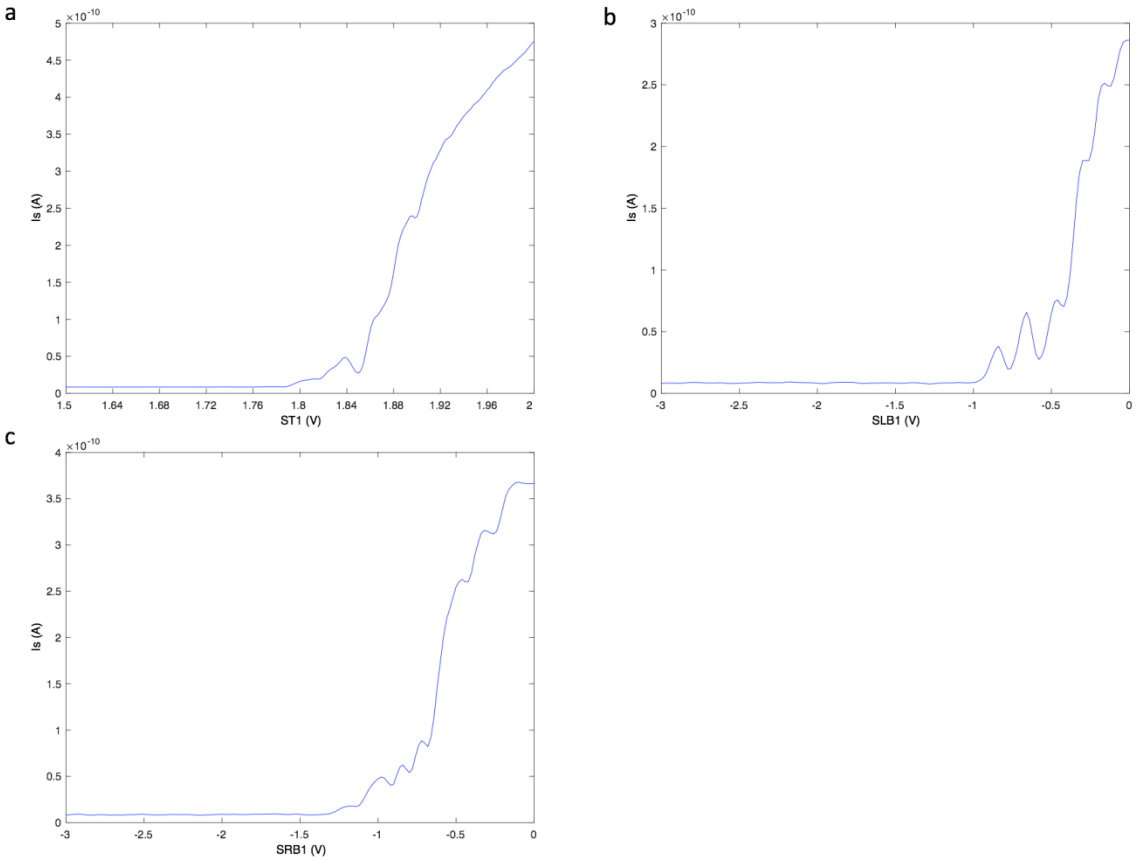


Figure 4.10: Depletion mode charge sensor *Batch 2 – R2C1*; (a) ST1 turn-on, (b) SLB1 and (c) SRB1 pinch-off at 4K.

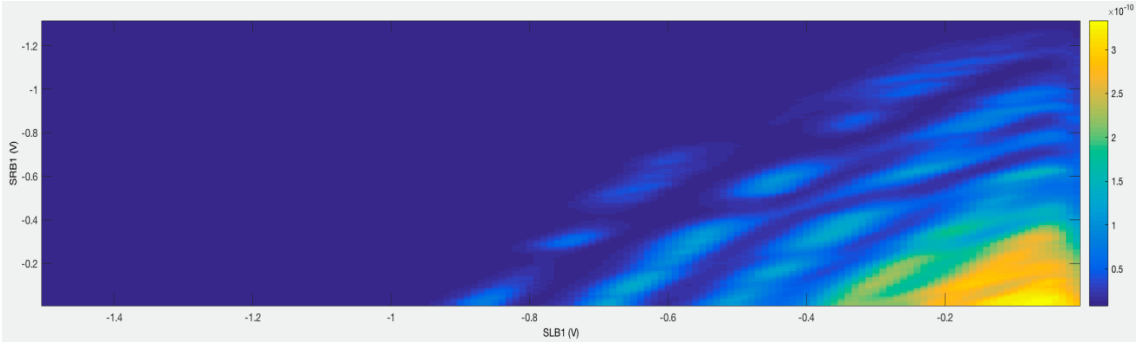


Figure 4.11: Depletion mode charge sensor *Batch 2 – R2C1* channel current as a function of SLB1 and SRB1 voltages, showing dependencies on the two barriers at 4K.

We also investigated Coulomb diamonds by biasing S1/D1 with a DC source and measuring the channel current as a function of the ST1 voltage and S1/D1 DC bias. Figure 4.13 shows the measurement result, and Coulomb diamonds are visible. Again, these diamonds overlap with one quantum dot and another. We expect to improve these results when measuring the device at lower temperatures in a dilution refrigerator.

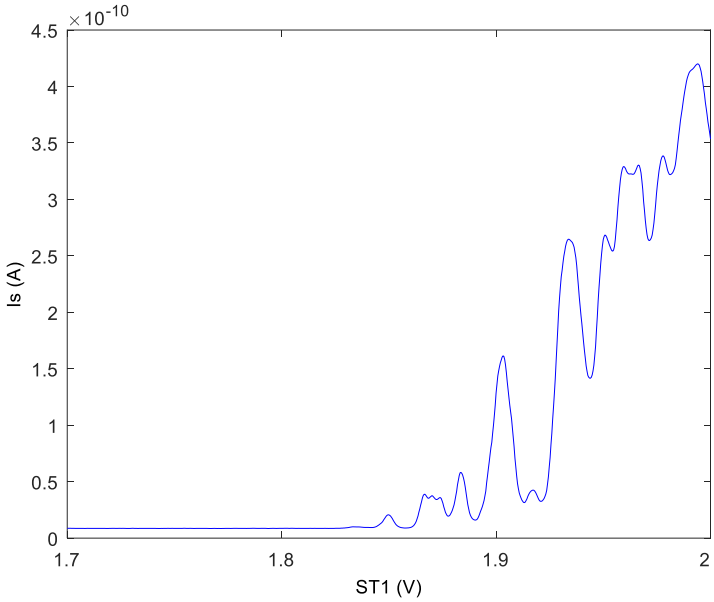


Figure 4.12: Depletion mode charge sensor *Batch 2 – R2C1* Coulomb oscillations at 4K.

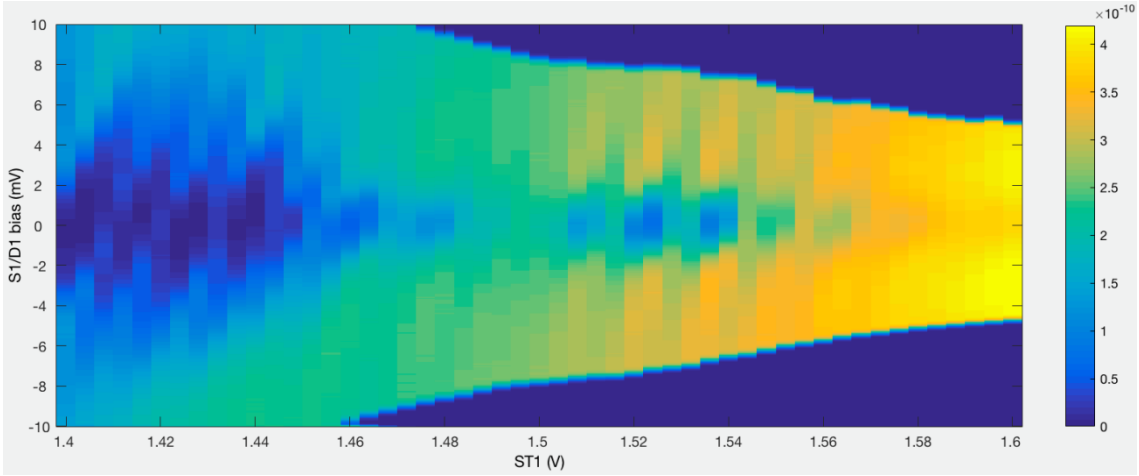


Figure 4.13: Depletion mode charge sensor *Batch 2 – R2C1* Coulomb diamonds at 4K.

Next, we loaded the device into the dilution refrigerator and set up the experiment with the same configuration as for 4K dipping. We quickly confirmed that the device turned on and pinched off at base temperature. Again, we characterised the device by scanning

the channel current as a function of SLB1 and SRB1 voltages; the result is shown in Figure 4.14. Again, we obtain two slopes which show dependencies on SLB1 and SRB1 at ~50mK. Then, we sought Coulomb oscillations by tuning the device to its high transconductance point and slowly sweeping the ST1 voltage.

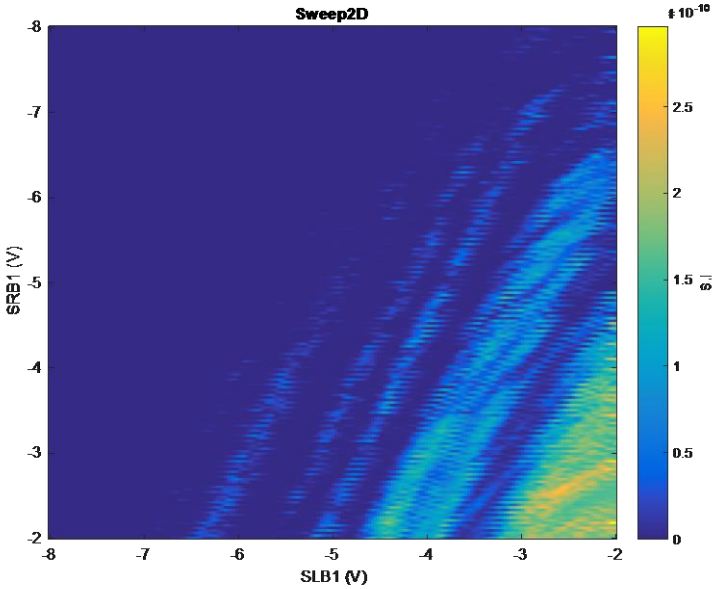


Figure 4.14: Depletion mode charge sensor *Batch 2 – R2C1* channel current as a function of SLB1 and SRB1 voltages, showing dependencies on the two barriers at base temperature.

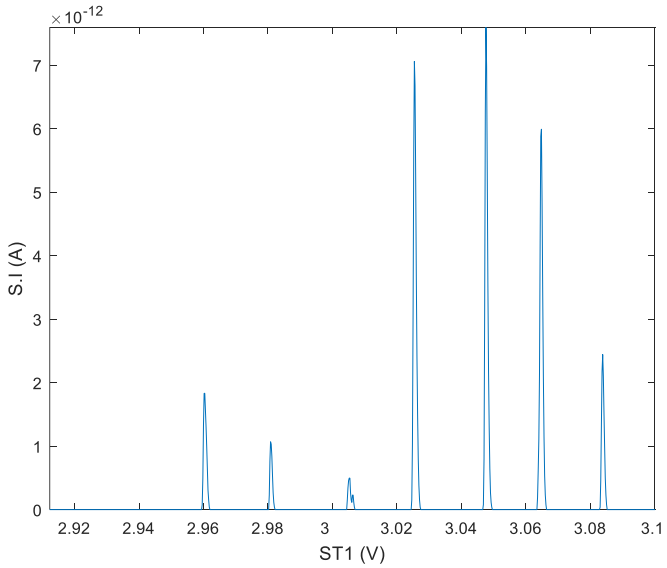


Figure 4.15: Depletion mode charge sensor *Batch 2 – R2C1* Coulomb oscillations at ~50mK.

Figure 4.15 shows the result of Coulomb oscillations. At base temperature, we can obtain a more regular oscillation curve. We can see clear charge transitions of the main dot. Finally, we study the Coulomb diamonds; the result is shown in Figure 4.16. We used the same measurement technique and obtained a number of discrete diamonds. The depletion mode charge sensor behaves very similarly to an SET at ~50mK temperature, and we are now confident in the possibility to investigate the charge-sensing characteristics of this device architecture.

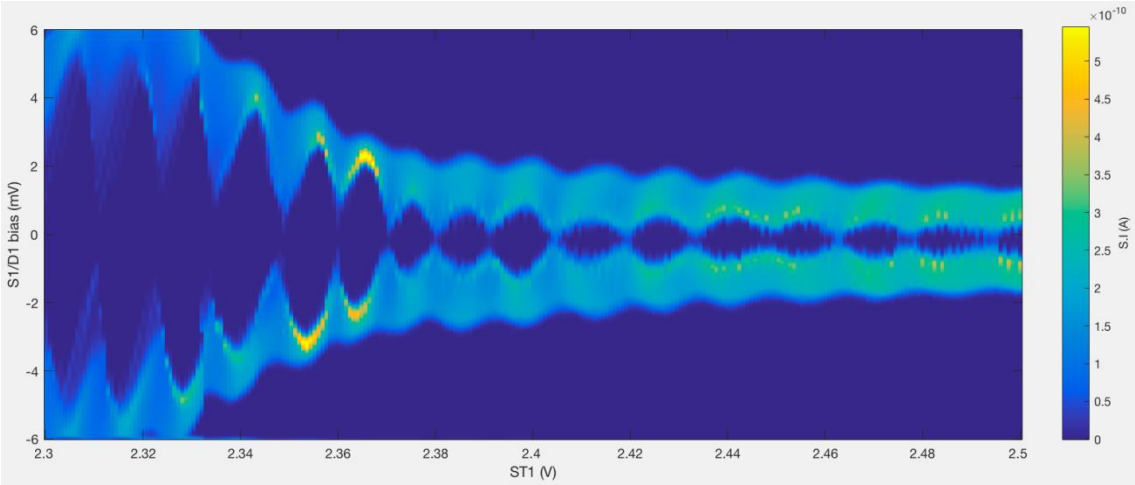


Figure 4.16: Depletion mode charge sensor *Batch 2 – R2C1* Coulomb diamonds at ~50mK.

4.3.3 Batch 3

In order to perform charge sensing, the two charge sensors must be placed sufficiently close together so that their quantum dots can capacitive couple to each other. Therefore, in *Batch 3* we moved the two devices closer and operate one as a sensor that monitors the quantum dot occupancy of the other. The design is shown in Figure 4.17. We placed the two devices within 100nm at the centre of the pixel and extended the nanostructure connections. Only one confinement barrier is used in this design, and is placed between the ST1 and ST2 gates. The microstructure patterns remain unchanged.

The chip map of *Batch 3* is outlined in Table 4.3 with a brief summary. We inspected pixels R1C3, R1C4 and R4C2 under SEM and found that devices on all three pixels had broken barrier gates. The corresponding SEM images are shown in Figure 4.18. We also dipped several pixels from different sections of the batch and found that most of them

had no pinch-off on their SLB and/or SRB gates. We believe that barrier gates on these pixels were also broken, so that they were unable to pinch off the channels.

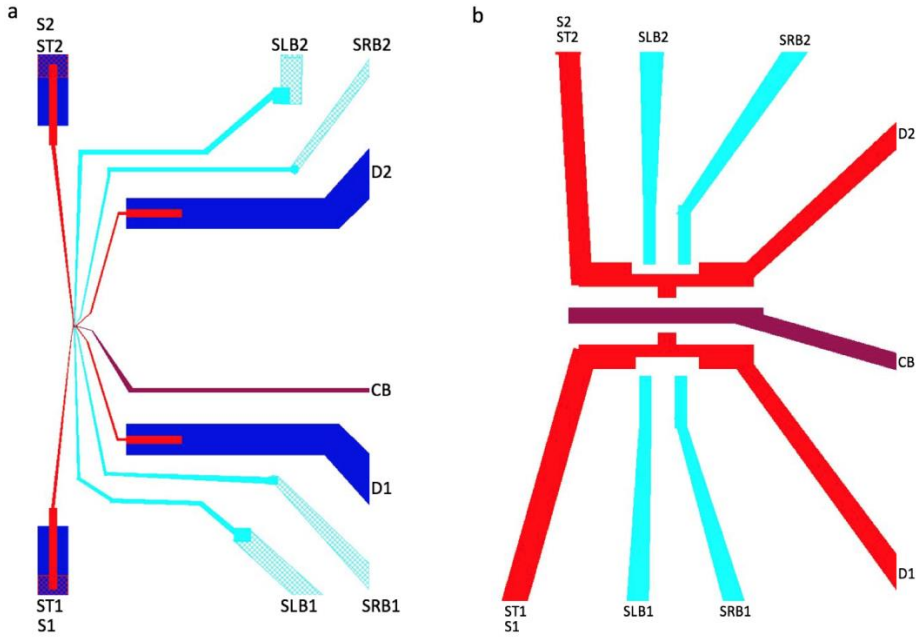


Figure 4.17: Depletion mode charge sensor *Batch 3* design. (a) Nanostructure connections are extended as the two devices are placed at the pixel centre, and (b) they are placed within 100nm from each other with a CB in-between.

	C1	C2	C3	C4
R4	Raith clamp No device	SEM	Bond: 11/5/2017 Dip: 17/5/2017 Bad pinch off	Bond: Dip:
R3	Bond: Dip: SRB1 & SLB2 no pinch off	Bond: Dip: ST no turn on	Bond: Dip:	Bond: Dip:
R2	Bond: Dip: ST1 no turn on SLB2 vs SRB2 bad	Bond: Dip: SRB2 no pinch off	Bond: 4/5/2017 Dip: SET2 good SRB1 no pinch off	Bond: 9/5/2017 Dip: 9/5/2017 Bad SLB1 vs SRB1
R1	Bond: 11/5/2017 Dip: 17/5/2017 SLB no pinch off	Bond: Dip:	SEM	SEM Broken CB

Table 4.3: Chip map of depletion mode charge sensor *Batch 3*.

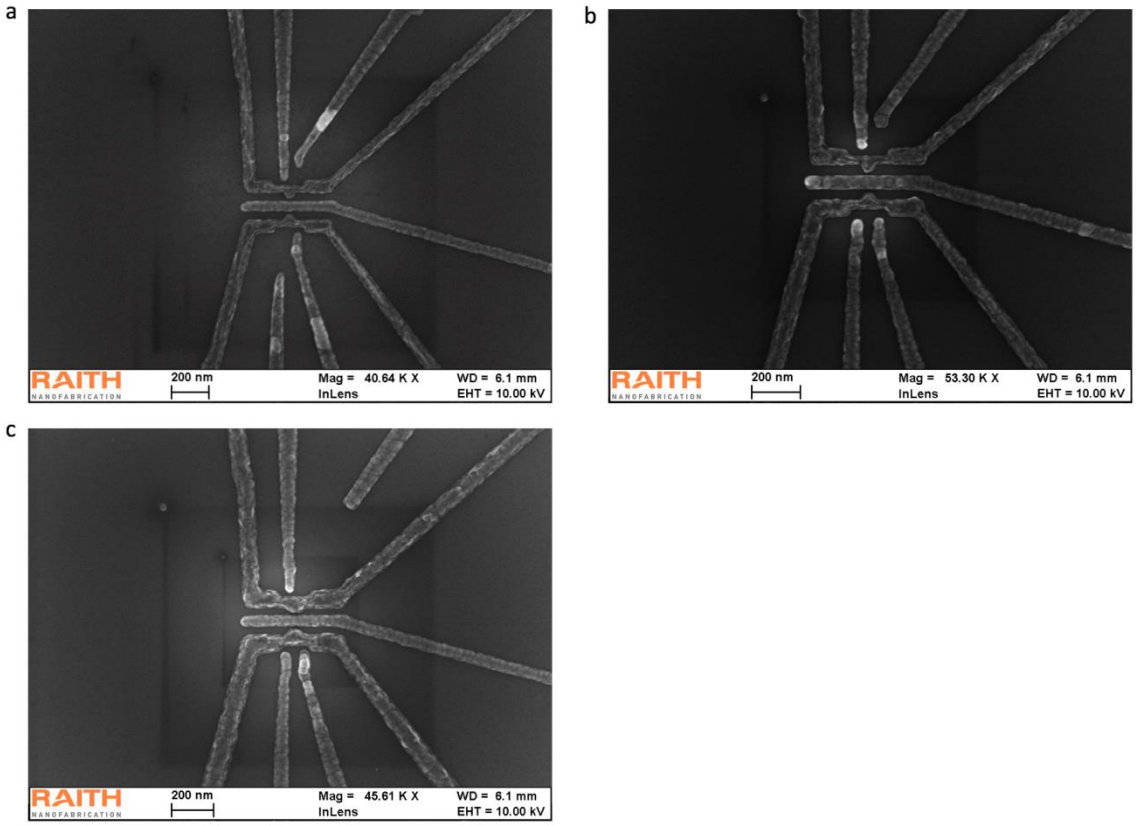


Figure 4.18: SEM images of depletion mode charge sensor *Batch 3*: (a) R1C3, (b) R1C4 and (c) R4C2. All three pixels show broken SLB and/or SRB on their devices.

We conclude that this batch has a lift-off issue on the barrier gates and this can happen by chance. However, the alignment and layout of the patterns achieve the expected outcome, so that we are confident in using the same fabrication procedure for this modified design. We decided to abandon this batch and move onto making a new batch using the same design and process.

4.3.4 Batch 4

In *Batch 4*, we used the new natural silicon stock named *MV16*, which only became available before making this batch. As we experienced source/drain leakage on several devices from the previous batches, which used the *MV14* stock, we decided to make the new batch using the new stock. We fabricated the batch using the identical design and process as for *Batch 3*, and inspected a set of promising devices at pixel R3C1. Figure 4.19 shows the SEM images of this pixel with measurements. We can see that the two

devices are perfectly aligned to each other and the pattern sizes all lie within our design tolerance. Hence, we are confident that we can conduct experiments using the devices from this batch.

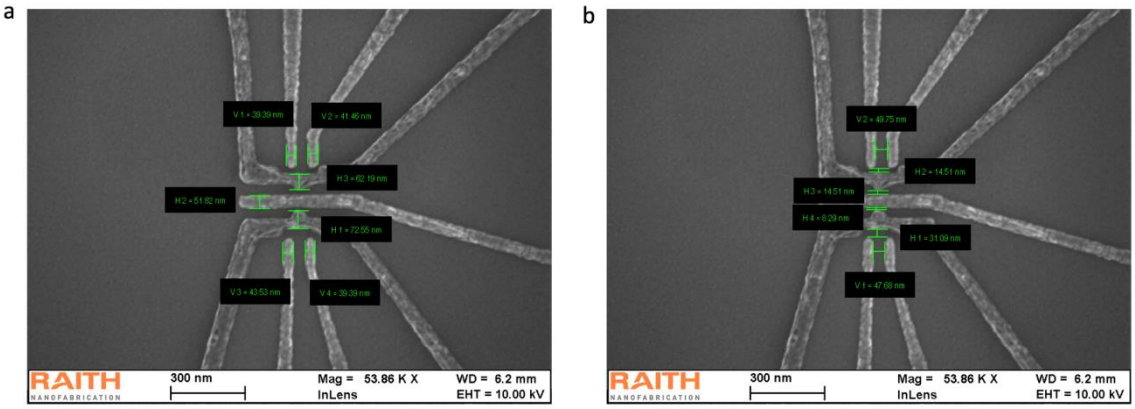


Figure 4.19: SEM images of depletion mode charge sensor *Batch 4 – R3C1*, showing that both devices well aligned and well patterned with measurements.

	C1	C2	C3	C4
R4	Raith clamp No device	SEM Bad lift-off	Bad pixel	SEM Broken ST2
R3	SEM Very good looking	Bond: Dip:	Bond: Dip:	Bond: Dip: No turn on
R2	Bond: 18/5/2017 Dip: 18/5/2017 No turn on	Bond: Dip: No turn on	Bond: 22/5/2017 Dip: 22/5/2017 No turn on	Bond: 18/5/2017 Dip: 19/5/2017 No turn on
R1	Bond: 18/5/2017 Dip: 19/5/2017 No turn on	Bond: Dip: SET2 turn on SRB2 no pinch off	Bond: 19/5/2017 Dip: 22/5/2017 No turn on	Bond: 17/5/2017 Dip: 18/5/2017 ST1 Oscillations

Table 4.4: Chip map of depletion mode charge sensor *Batch 4* with a brief summary.

A chip map with a brief summary for *Batch 4* is presented in Table 4.4. We dipped nine pixels and found that seven had no device turn-on. The other two pixels had only one device turn-on, with poor characteristics. Hence, we were unable to conduct further experiments with these devices. We believe that this new stock might have had some

source/drain-related issues, and we reported this to the research team for further investigation. Again, we had to abandon the batch and make another new one using the old *MV14* stock.

4.3.5 Batch 5

We repeated the same process and fabricated *Batch 5* using the *MV14* natural silicon stock. Table 4.5 outlines the chip map with a brief summary. We SEM-imaged pixels R4C2 and R1C4, and found good images from R1C4 as shown in Figure 4.20. We also dipped a number of devices and found that both devices from R2C1 passed 4K dipping. We now focus on discussing the dipping and dilution refrigerator measurements of this pixel.

	C1	C2	C3	C4
R4	Raith clamp No device	SEM Broken SRB2 @ nanostructure	Bond: Dip: SET1 no turn on Weak SLB2 pinch off	Bond: Dip:
R3	Bond: Dip:	Bond: Dip:	Bond: Dip: Weak SLB1 pinch off SET2 no turn on	Bond: Dip: No turn on
R2	Bond: Dip: Good/put into RF3	Bond: Dip:	Bond: Dip: Weak SLB1 pinch off	Bond: Dip:
R1	Bond: Dip: SET1 no turn on SET2 SD leakage	Bond: Dip:	Bond: Dip: Bad SLB1 vs SRB1 SET2 no turn on	SEM Good looking!

Table 4.5: Chip map of depletion mode charge sensor *Batch 5* with a brief summary.

Figures 4.20a and 4.20b show good connections on the microstructure and nanostructure fan-outs with good alignments. The appearances of the two devices are shown in Figures 4.20c and 4.20d, respectively, with measurements. Both devices are aligned perfectly with each other, and their distance is within 100nm. The sizes of the patterns are between 40–60nm, with are all within tolerance. SLB and SRB gates on

both devices are also well aligned to the top gate centre points. Hence, we are confident in conducting experiments with this batch.

We dipped seven pixels and found that pixel R2C1 passed the 4K dipping test. Concerning the other pixels, one of the devices did not turn on or pixels experienced poor barrier pinch-off issues, so that they were unable to carry out charge sensing. In the following, we only discuss the results from pixel R2C1, starting with the 4K dipping measurement.

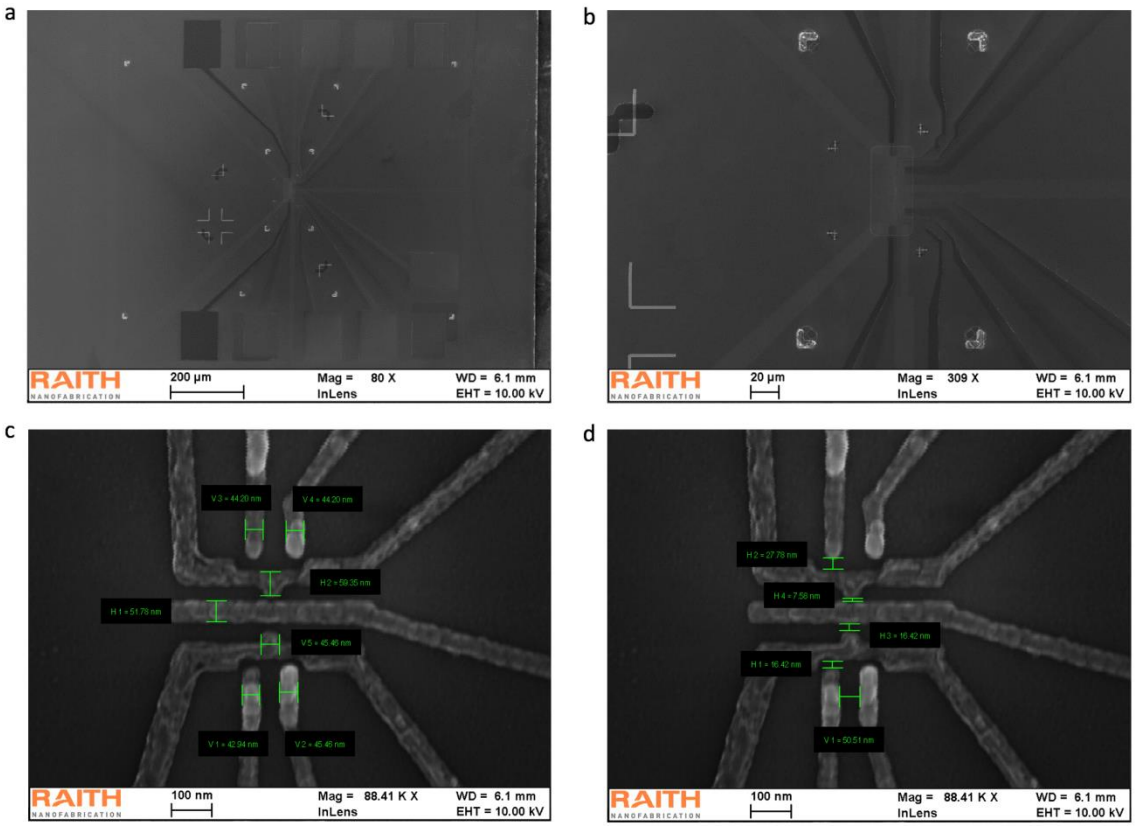


Figure 4.20: SEM images of depletion mode charge sensor *Batch 5 – R1C4*: (a) microstructure fan-outs and (b) nanostructure connections. (c) and (d) the two devices with measurements.

As usual, we began with the leakage test and found no gate or source/drain leakages on either device. Then, we examined the top gate turn-on and barrier gates pinch-off; the results are shown in Figure 4.21. Both devices turn on at approximately 1.4V, as can be seen from Figures 4.21a and 4.21d. SLB1 and SRB1 fully pinch off beyond -1.5V, while SLB2 and SRB2 achieve similar results with a slightly lower pinch-off voltage at beyond -2V.

Next, we characterised the barriers of both devices by scanning the channel currents as a function of their SLBs and SRBs, and the results are shown in Figure 4.22. From Figure 4.22a, we can see that the quantum dot dependencies of SLB1 and SRB1 are almost equal, as there is only one obvious slope at an angle of ~45° to both SLB1 and SRB1. SLB2 and SRB2 show two different dependencies with two slopes, as illustrated in Figure 4.22b, which is similar to the results obtained in the previous device batches.

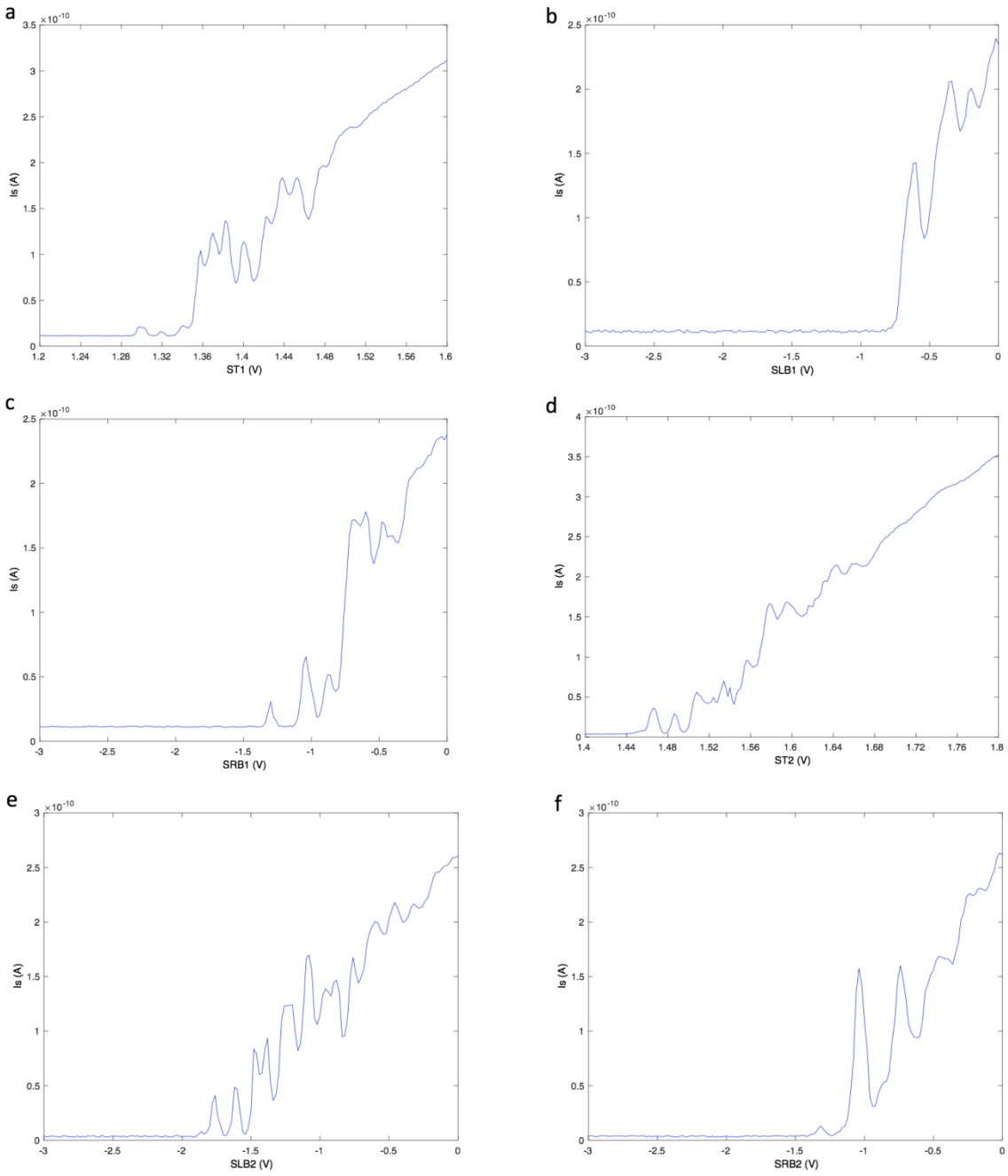
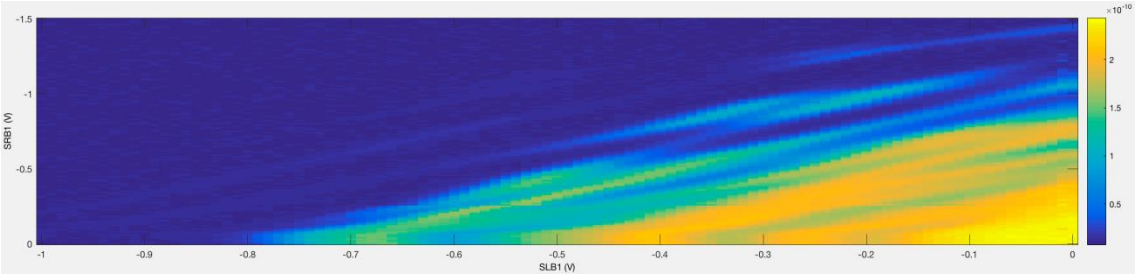


Figure 4.21: 4K dipping results of depletion mode charge sensor *Batch 5 – R2C1*: (a) ST1 turn-on, (b) SLB1 and (c) SRB1 pinch-off; (d) ST2 turn-on, (e) SLB2 and (f) SRB2 pinch-off.

Following SLB/SRB characterisation, we tuned both devices to their high transconductance points and sought Coulomb oscillations based on the colour maps. We can obtain a result for each device that resembles Coulomb oscillations but with distortion, as shown in Figure 4.23. According to the results from *Batch 2 – R2C1*, here we do not expect to see satisfactory oscillations at 4K, since it is difficult to confine a single quantum dot at this temperature. We shall see better results when the devices are measured at lower temperature in a dilution refrigerator, hence we did not proceed to measuring Coulomb diamonds at this stage.

a: SLB1 range from -1 to 0, SRB1 range from -1.5 to 0.



b: SLB2 range from -2 to 0, SRB2 range from -1.5 to 0.

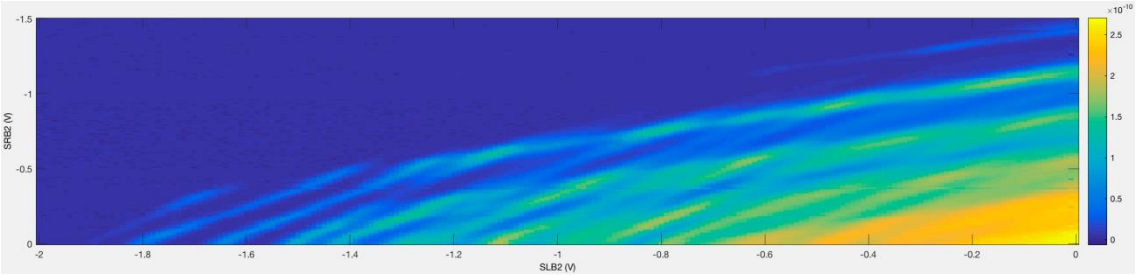


Figure 4.22: Depletion mode charge sensor *Batch 5 – R2C1* barrier characterisation at 4K. (a) ST1 channel current as a function of SLB1 and SRB1. Only one slope shows an equal dot dependency on both barriers. (b) ST2 channel current as a function of SLB2 and SRB2, showing different dependencies with two slopes.

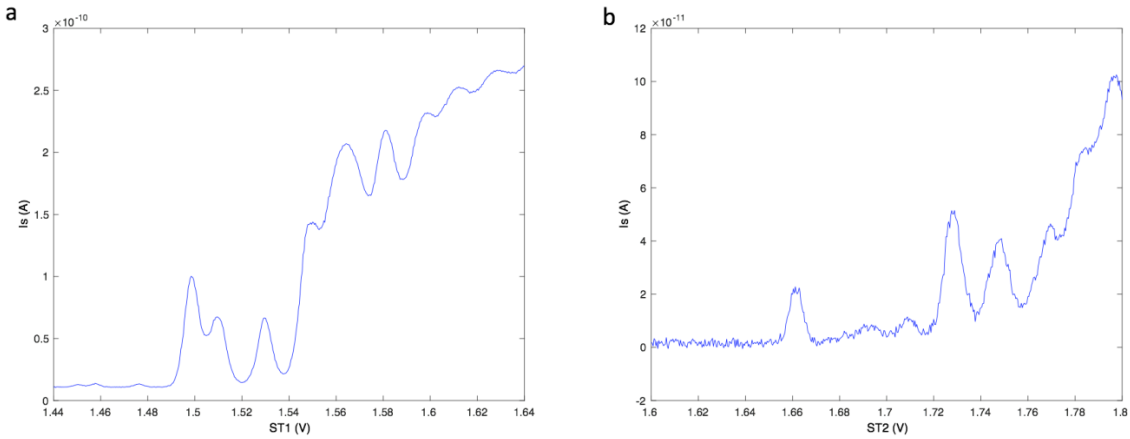


Figure 4.23: Depletion mode charge sensor *Batch 5 – R2C1* Coulomb oscillations at 4K.

We now discuss the dilution refrigerator measurement and results. After loading the chip into the refrigerator and cooling to base temperature, we quickly tested whether both devices would turn on and pinch off properly, and found that ST2 turned on as usual while ST1 did not turn on. The cause could be broken wires or connections on ST1 and/or S1/D1, or simply that the device could not turn on at base temperature. If either S1 or D1 lost connection, we could still form a quantum dot under ST1 using the other ohmic in contact. We decided to examine this later and to begin characterising ST2, SLB2 and SRB2. The results are shown in Figure 4.24. ST2 turns on at ~1.65V, which is about 0.2V higher than the result obtained during 4K dipping. This is normal, as a slightly higher turn-on voltage may be required at lower temperature. Both barriers pinch-off beyond -1.5V, similar to the results at 4K.

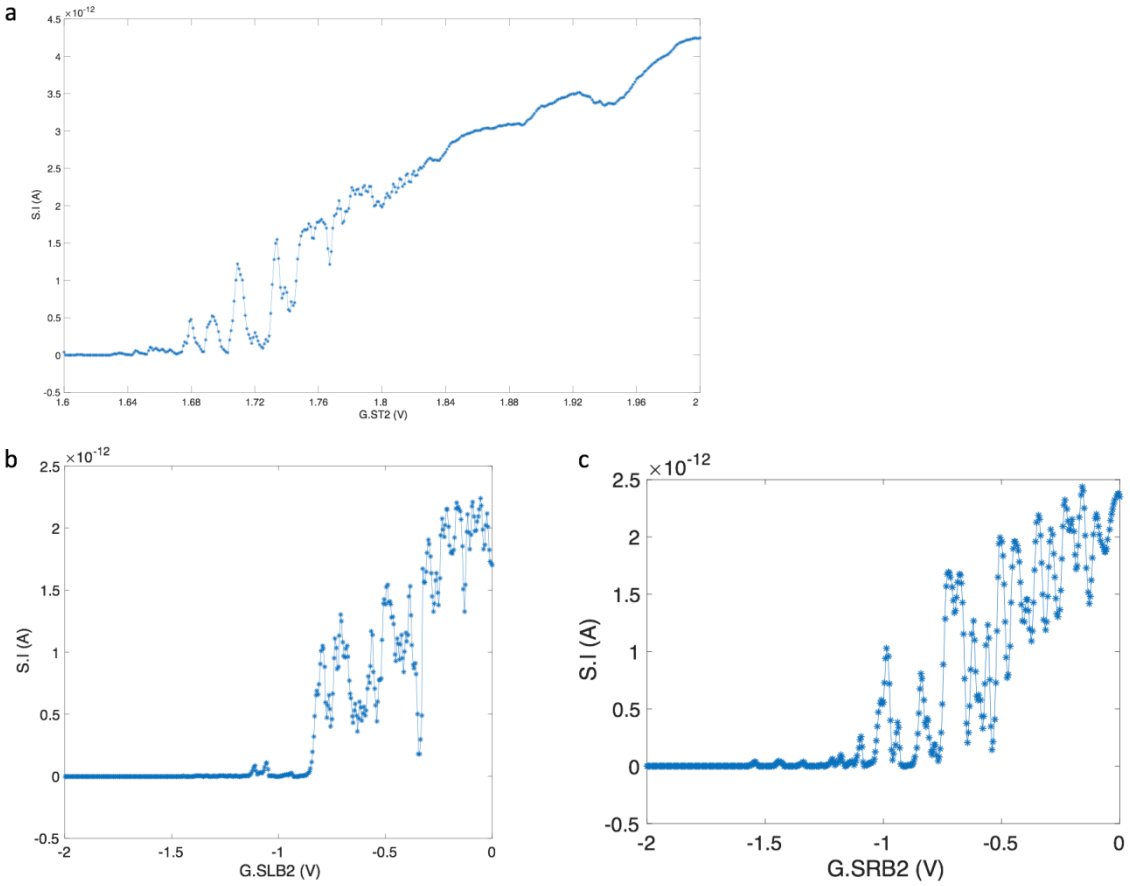


Figure 4.24: Depletion mode charge sensor *Batch 5 – R2C1* measurement at ~50mK. (a) ST2 turn-on, (b) SLB2 and (c) SRB2 pinch-off.

Next, we examined the relationship between SLB2 and SRB2 by measuring the channel current as a function of the two barriers; Figure 4.25 shows the result. Clearly, we can see two different slopes that represent the dependencies on SLB2 and SRB2. We selected an arbitrary high transconductance point where the two slopes intersect, and slowly scanned the ST2 voltage to seek Coulomb peaks and oscillations. The result is shown in Figure 4.26, and a number of sharp Coulomb peaks are obtained at 2V ~ 2.08V.

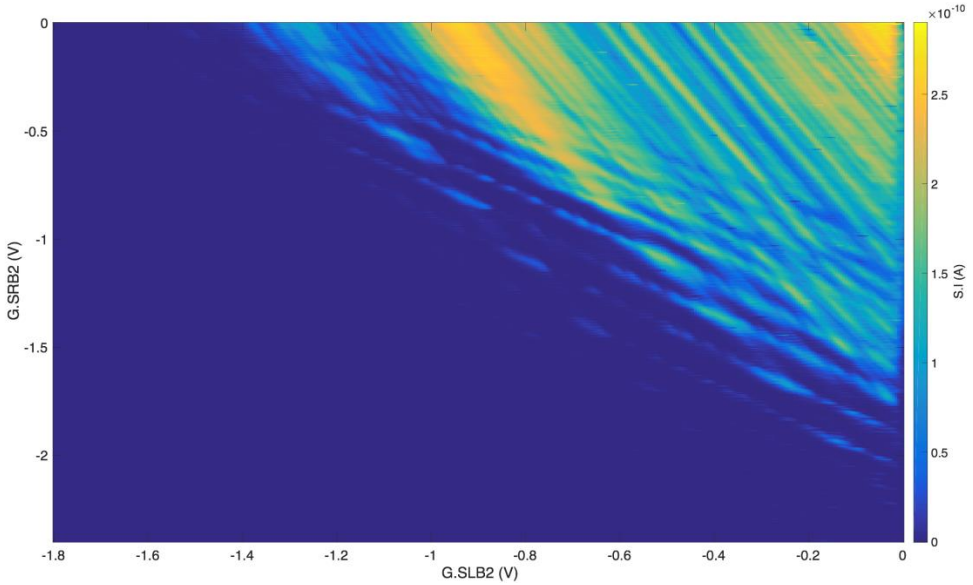


Figure 4.25: Depletion mode charge sensor *Batch 5 – R2C1*, the ST2 channel current as a function of SLB2 and SRB2 voltages. Two slopes clearly represent dependencies on the two barriers.

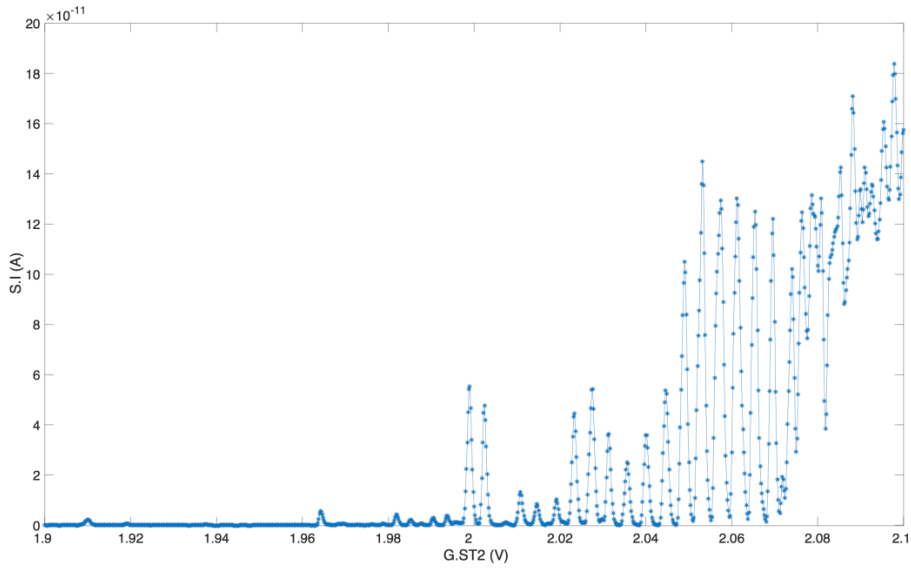


Figure 4.26: Depletion mode charge sensor *Batch 5 – R2C1* Coulomb oscillations.

We also study Coulomb diamonds; Figure 4.27 shows the result. By scanning the channel current as a function of ST2 voltage and S2/D2 DC bias voltage, we obtained a number of diamonds. At this stage, we can conclude that this device also behaves like a normal SET and we can configure it to perform the charge sensing experiment.

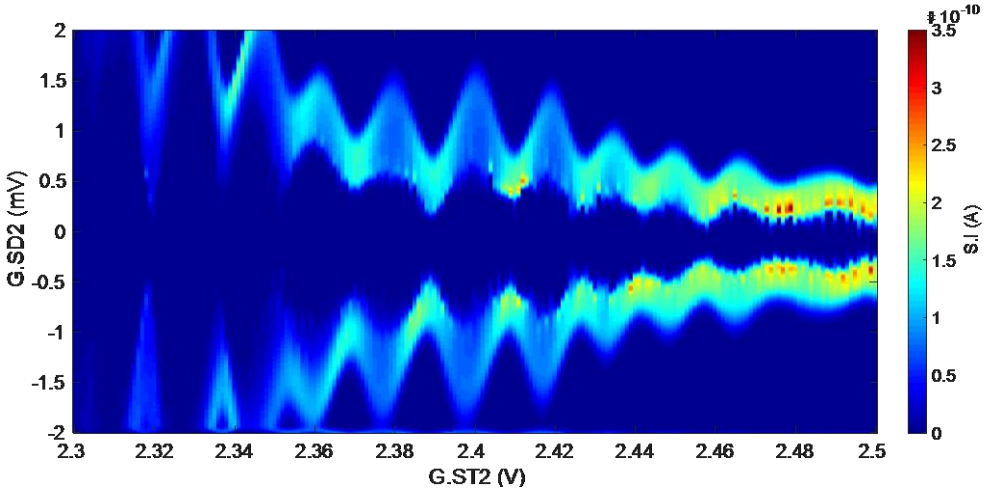


Figure 4.27: Depletion mode charge sensor *Batch 5 – R2C1* Coulomb diamonds.

We set up the experiment as per pulse-bias spectroscopy as described in *Chapter 2 – section 2.4*. A schematic diagram of the setup is shown in Figure 4.28. We used ST1, SLB1 and SRB1 to create a quantum dot below the centre point of ST1, and tuned ST2, SLB2 and SRB2 to become a charge sensor that monitors the quantum dot occupancy at ST1. We biased S2/D2 using a lock-in amplifier at frequency f_{sensor} with 100μV amplitude, and the ST2 channel current was fed into a pre-amp to amplify the signal for better readout. We selected a steep point from an arbitrary Coulomb peak, so that the sensor was at high sensitivity, and applied a feedback to SRB2 to compensate any slow charge shifting and to maintain the sensitivity. A square-wave pulsing signal was generated at frequency f_{pulse} and amplitude V_{pulse}, and combined with a DC signal V_{ST1}. This signal was connected to ST1 to control the quantum dot status. Another lock-in amplifier that locks at f_{pulse} was fed from the pre-amp, such that the signal from the quantum dot being picked up by the sensor would be detectable by this lock-in amplifier. S1 and D1 remained grounded and each gate electrode was connected to a DC voltage source, which is not drawn in the diagram.

Because ST1 does not turn on, we cannot characterise SLB1/SRB1 and tuned these barriers to confine a quantum dot. Instead, we made SRB1 opaque by setting its voltage to -4.5V so that it creates a high-potential barrier under ST1 at the SRB1 side. Then, we slowly varied the voltages on SLB1 and ST1 while monitoring the signal on the dot lock-in amplifier. This signal indicates that a quantum dot is formed under ST1 and is detected by the sensor.

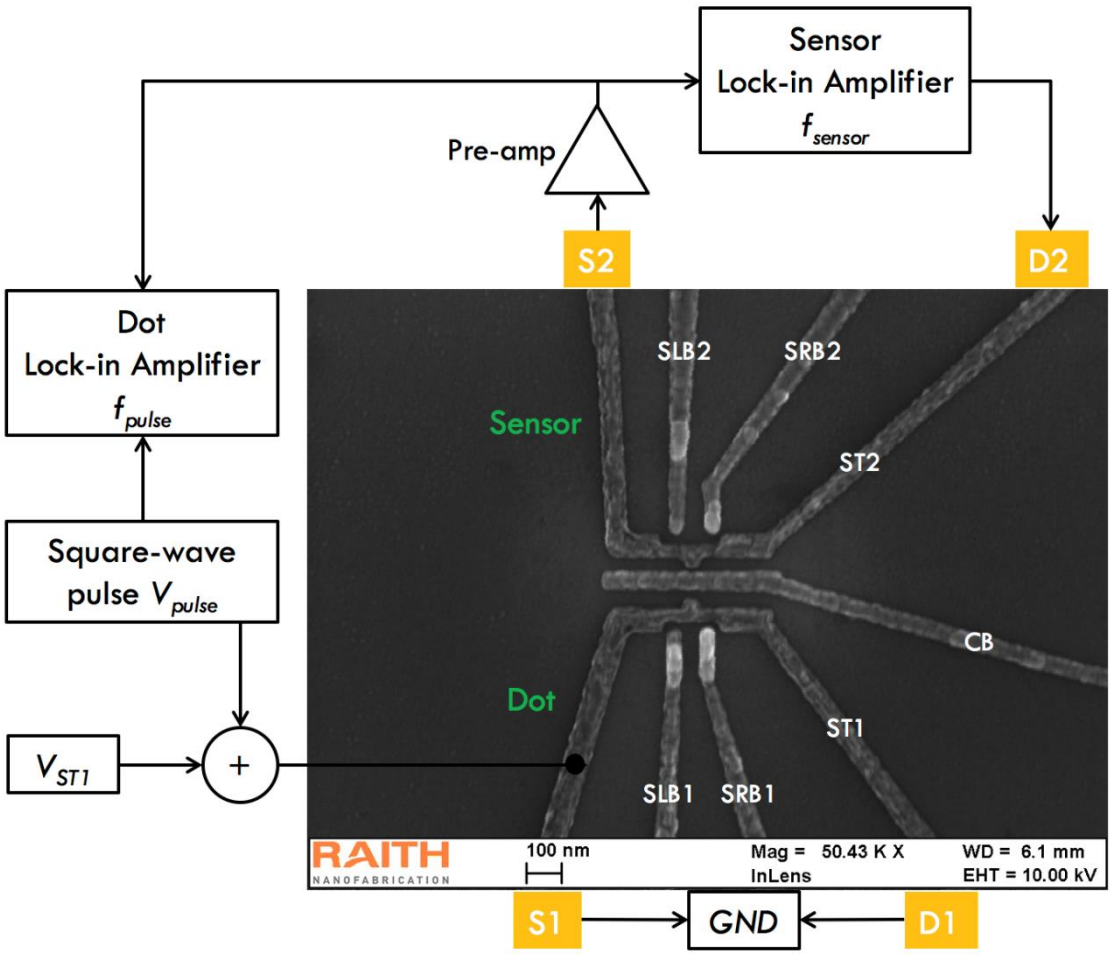


Figure 4.28: Pulse-bias spectroscopy setup for depletion mode charge sensor to perform the charge sensing experiment. ST1, SLB1 and SRB1 are used to confine a quantum dot, and ST2, SLB2 and SRB2 are tuned as a charge sensor to monitor the dot occupancy under ST1.

With this technique, we managed to confine a quantum dot under ST1 and manipulate its status by sweeping ST1 vs SLB1, and measured the signal on the dot lock-in amplifier. Figure 4.29 shows a charge transition stability diagram. Clearly, we see eight charge transitions between 1.6V to 1.8V ST1 voltage, as indicated by the yellow lines in the figure. Each line represents an electron tunnelling on/off the quantum dot. Here, SLB1 acts as a tunnel barrier, and by changing it slowly the tunnel rate also changes slowly, so that the transitions occur at a slightly different ST1 voltage and the lines form a small gradient in the colour map.

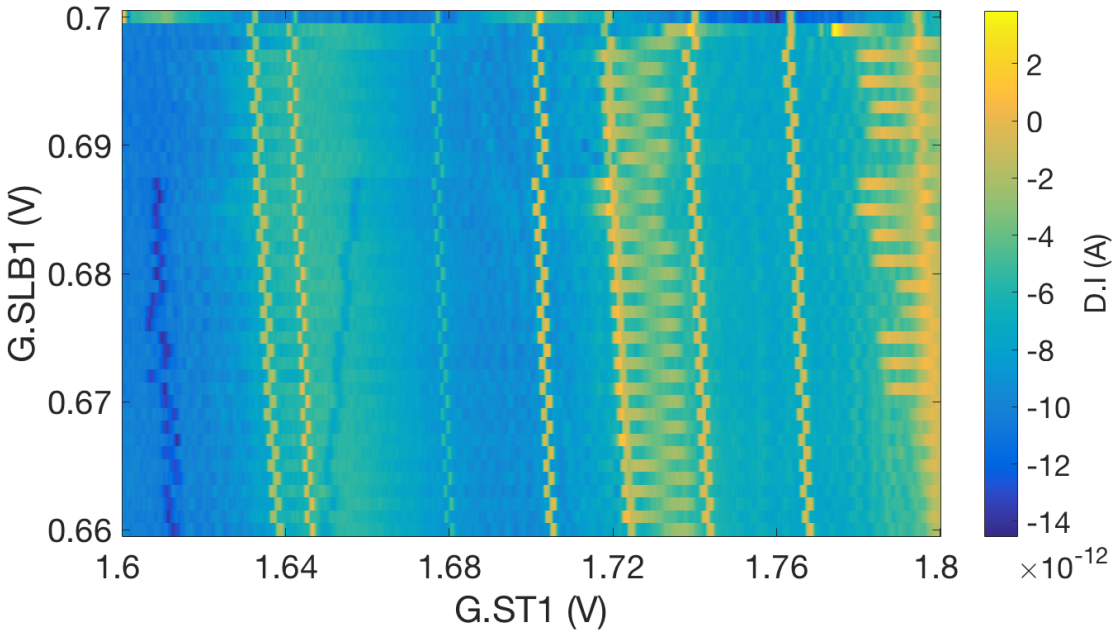


Figure 4.29: Charge transition stability diagram of depletion mode charge sensor. SRB1 is set to be opaque and SLB1 is used as a tunnel barrier. By sweeping the ST1 voltage, electrons tunnel on/off the quantum dot one at a time, and these transitions are represented by the yellow lines.

Now, we can conclude that the depletion mode charge sensor design architecture is able to operate like an SET charge sensor. A quantum dot can be confined below the top gate where the two barriers pinch off the channel in depletion mode. This quantum dot can capacitive couple to another quantum dot in the vicinity and monitor its occupancy. For the next step, we attempted to examine the spin information of the electrons inside the dot by applying a static magnetic field to the measurement. This may be difficult to determine because we expect the quantum dot to be in a many-electron regime, where the valley-orbit structure is in a highly complex form so that the spin orientation is unclear. It is also challenging for this simple architecture to pinch the dot to its first few electrons status, as it has less control ability than the device described in *section 2.4*. However, it is still worth examining how the magnetic field affects the charge transitions and whether this sensor can detect any distinguishable changes.

We applied different magnetic field strengths (1T, 2T, 3T, 4T, 5T and 6T) to the device and performed the same measurement at a finer scale; the results of 1T, 3T and 6T are shown in Figure 4.30. As the magnetic field strength varies, the transitions occur at slightly different levels, indicating that the magnetic field changes the spin-filling order, which can be detected by the sensor.

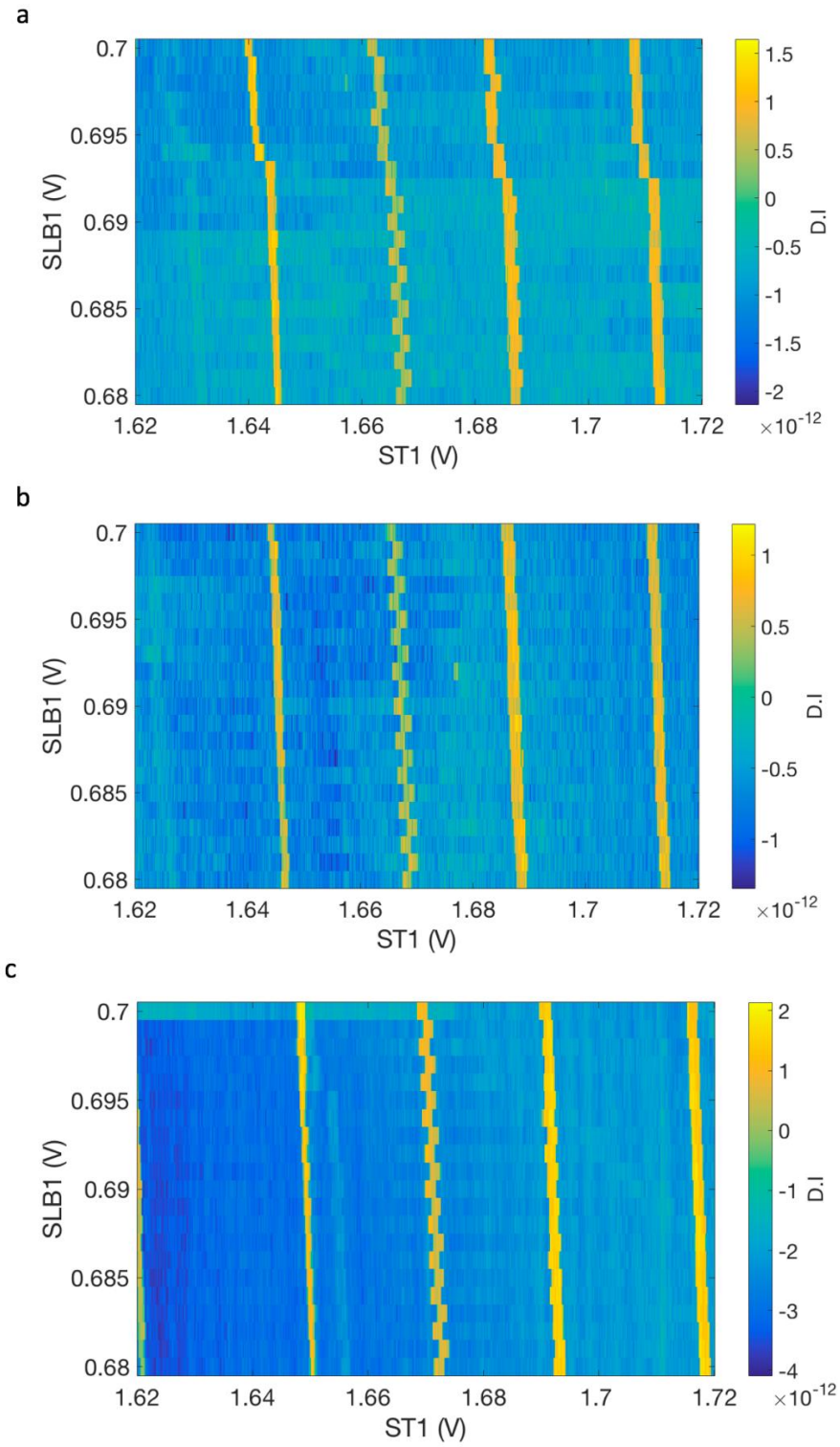


Figure 4.30: Charge stability diagrams of depletion mode charge sensor with applied magnetic field at (a)1T, (b)3T and (c)6T. Transitions occur at slightly different voltages as magnetic field strengths vary, indicating that the magnetic field changes the spin-filling order.

We attempted to determine spin orientation by sweeping the magnetic field and ST1 voltages to seek the “kinks”, but the sensor started to drift away after the magnetic field swept beyond 2T, even with feedback compensation. Therefore, we were unable to generate a full measurement and study this device further. We decided to end our experiment and conclude the project at this stage.

4.4 Project summary

In this project, we modified the SET architecture by separating the top gate and two barrier gates, and aimed to verify whether this device structure can operate as a quantum dot charge sensor. We measured two samples at the base temperature of a dilution refrigerator and found that devices on both samples behaved like normal SETs. We also investigated charge sensing by placing two depletion mode charge sensors close to each other, using one to confine a quantum dot and the other as a sensor to monitor the quantum dot occupancy. Charge transitions were observed by performing pulse-bias spectroscopy, and we confirmed that the sensor was able to detect transitions through capacitive coupling. We did not manage to obtain spin information as the sensor drifted away when the magnetic field strength increased.

During base temperature measurements, we did not observe any unintentional quantum dots on either sample. However, with only two samples measured, we still do not have enough evidence to confirm that this device structure has reduced or even eliminated the chance of forming unintentional quantum dots. We need to measure a large volume of devices in the long term to create a statistical analysis to be able to prove this statement.

Chapter 5
Conclusion

In this chapter, we summarise the two research projects, the Si-MOS multiplexer and depletion mode charge sensor, and provide a conclusion to the thesis. Suggestions on future work for the two projects are also outlined as a reference for other candidates to continue the projects.

5.1 Thesis summary

In *Chapter1*, we gave an introduction to quantum computing concepts and the current research progress of the UNSW silicon quantum dot qubit research team. We also introduced the two research projects involved in this thesis and their motivations. A literature review was given in *Chapter 2* and mentioned the relevant research publications from previous years.

The research performed for the Si-MOS multiplexer project was presented in *Chapter 3*, including the design, a series of tests conducted at 4K, SIMS analysis and the design modification. We explained the design layer by layer with a simplified fabrication process and the function of each layer. Leakage tests, MOSFET turn-on tests and n-finger turn-on tests were conducted on a number of samples to study their characteristics. We found that the n-fingers on all of these samples experienced leakages to the other n-fingers. Only one of 16 MOSFETs turned on in the MOSFET tests, while most of the n-fingers were correctly addressed and conducted current in the n-fingers test. However, high resistances were observed on all of these turned-on n-fingers, caused by high channel resistance of the addressing gates. A SIMS analysis was conducted on two samples, and we found that n-type doping and ohmic contacts were fabricated properly. The p-type channel stoppers had a shallower profile and lower doping concentration than the design, which was likely the cause of the n-finger leakage. The field oxide was also thinner than the design thickness, and might be unable to bypass the accumulation effects from the aluminium gates. Design modifications were

suggested as solutions to the addressed issues, and this project is pending a decision to proceed.

The depletion mode charge sensor project was discussed in *Chapter 4*. We modified the SET design by separating the overlapping of the top and barrier gates, and fabricated and measured these modified devices. We were able to turn on and pinch off the devices in depletion mode, and observed similar characteristics to normal SETs. We configured two devices to be capacitively coupled to each other, and performed pulse-bias spectroscopy experiments. We managed to confine a quantum dot using one of the devices while the other acted as a charge sensor. The sensor successfully monitored the charge transitions on the quantum dot, hence we could operate these devices as charge sensors. We have not yet collected enough statistical data to prove that this device architecture can minimise the formation of strain-induced quantum dots. This requires a long-term study and measurement of a large volume of devices.

5.2 Future work

We have proposed a design modification for the Si-MOS multiplexer. To make a new batch in the future, ion implantation is required to replace the thermal diffusion for the p-type channel stoppers so that the doping profile can reach the desired depth. A thicker field oxide needs to be grown to guarantee sufficient thickness to bypass the top gates, preferably 300nm or thicker. The addressing switches have to be redesigned so that their channel resistances are within the kΩ range. We suggest that the same series of tests can be conducted on a new batch and compared with the results presented in this thesis to determine any improvements on the addressed issues.

For the depletion mode charge sensor project, we need to measure a large volume of devices and conduct a statistical analysis on whether this device architecture can reduce the chance of forming strain-induced quantum dots. We could also replace the SET with this sensor on qubit devices, and check whether the depletion mode charge sensor can perform tasks in more complex experiments.

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