Electrostatically defined few-electron double quantum dot in silicon

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(Received 13 February 2009; accepted 1 April 2009; published online 27 April 2009)

A few-electron double quantum dot was fabricated using metal-oxide-semiconductor-compatible technology and low-temperature transport measurements were performed to study the energy spectrum of the device. The double dot structure is electrically tunable, enabling the interdot coupling to be adjusted over a wide range, as observed in the charge stability diagram. Resonant single-electron tunneling through ground and excited states of the double dot was clearly observed in bias spectroscopy measurements. © 2009 American Institute of Physics.

[DOI: 10.1063/1.3124242]

Electrostatically defined single and double quantum dot (DQD) systems in GaAs/AlGaAs heterostructures12 are the current benchmark for the implementation of Loss and D-Vincenzo’s criteria using semiconductor qubits.3–5 Although the nuclear spins inherently present in GaAs provide a fast relaxation, silicon has a natural advantage in this respect since the only stable isotope with a nuclear spin is 29Si. The 4.7% abundance of this isotope in natural Si can be reduced by isotopic purification, resulting in nearly nuclear-spin-free crystals. This should, in principle, increase the coherence time of electron-spin qubits in Si.7,8 Initial demonstrations of Si-based DQD systems for spin qubits9,10 have stimulated a number of recent studies of DQDs in both multigated silicon-on-insulator11,12 and Si/SiGe13 structures.

In this letter, we report the fabrication of a few-electron DQD and its electrical measurement at milliKelvin temperatures. The DQD is based upon a recently developed double-gated Si QD,14 which was also shown to operate effectively as a radio-frequency (rf) single electron transistor.15 Our approach provides a simple method of producing multigate silicon QDs without the need for complementary-metal-oxide-semiconductor (MOS) process technologies, such as polysilicon deposition and etching. The morphology of the DQD device is investigated using cross-sectional transmission electron microscopy (XTEM) analysis. Transport spectroscopy demonstrates the ability to tune the DQD from the weakly coupled to strongly coupled regime. In the weakly coupled regime, extracted capacitances of the system show good agreement with simple modeling using FASTCAP.16

The devices investigated in this work were fabricated on near-intrinsic Si wafers (ρ > 10 kΩ cm at 300 K). After definition of n+ Ohmic contacts by phosphorus diffusion through a masked sacrificial thermal oxide, a 200 nm field oxide was grown. In the active device region (30 × 30 μm2), the field oxide was etched locally and replaced by an 8-nm thick-high-quality SiO2 gate oxide, grown in an ultradry oxidation furnace at 800 °C in O2 and dichloroethylene. Three Al barrier gates (BGs) were then patterned by electron beam lithography (EBL), thermal evaporation and lift-off. The BGs were next passivated by plasma oxidation,14,17 resulting in an electrically insulating Al2O3 layer surrounding the BGs. The Al top gate (TG) was defined in a second EBL step aligned to the lower gates with an accuracy of ~20 nm. Finally, the devices were annealed at 400 °C for 15 min in forming gas (95%N2/5%H2) to reduce the Si/SiO2 interface trap density (DN). Deep-level transient spectroscopy of similarly processed structures revealed DN of order 5 × 1010 cm−2 eV−1 near the conduction band edge.18

Figures 1(a) and 1(b) show a scanning electron microscope (SEM) image and a schematic cross section of a DQD device. The TG which extends over the source and drain n+ contacts and three BGs are used to form a two-dimensional electron gas (2DEG) under the thin SiO2 layer. The BGs are used to locally deplete the 2DEG, forming three tunnel barriers that define two dots in series. The dots are geometrically defined by the distance between adjacent BGs (~30 nm) and by the TG width (~50 nm). The outer BGs and TG are used to control the electron occ-

![Image]

FIG. 1. (Color online) (a) SEM image of the Si MOS DQD. The three BGs and the TG have widths ~30 and ~50 nm, respectively. The Al BGs were plasma-oxidized to isolate them from the TG. (b) Schematic cross section of the device. Source and drain n+ contacts (red) were formed by phosphorus diffusion into the Si substrate (light blue). The TG induces a 2DEG and the BGs create three potential barriers, forming two dots. The size of the dots is estimated to be 30 × 50 nm2. (c) Color-enhanced XTEM image of a similar device. (d) Enlarged XTEM image, showing sharp interfaces between the Si substrate, SiO2 gate oxide, Al2O3, and the Al TG.
cupacencies electrostatically and the middle BG is used to control the interdot coupling.

Figure 1(c) shows an XTEM image along the TG (i.e., perpendicular to the BGs). Apart from an increased (200 nm) TG width in order to aid XTEM sample preparation, this device is nominally identical to the device used in electrical measurements. The XTEM image confirms the target 5 nm Al2O3 layer thickness from the plasma oxidation process used (100 mTorr, 50 W incident rf O2 plasma, 150 °C for 3 min). Interestingly, at the interface between the TG and the SiO2, we find an additional Al2O3 layer [~2 nm thick, see Fig. 1(d)] which could be due to the oxidation of the Al TG via chemical interaction with the SiO2 below. We note that the Al BGs, initially evaporated to a thickness of 30 nm, show an Al core of only ~20 nm in diameter after plasma oxidation, consistent with the formation of a ~5 nm Al2O3 insulator. This is sufficient to allow differential biases of up to 4 V between the upper and lower gates with negligible leakage.

Electrical (dc) transport measurements were performed in a dilution refrigerator at a base temperature of ~50 mK. A source-drain excitation voltage $V_{sd}=50 \mu V$ at a modulation frequency of 13 Hz was used to monitor the differential conductance $dI/dV_{sd}$. The source-drain dc current $I_{SD}$ was measured with a room-temperature current preamplifier. Initially, the left (right) dot was characterized independently by setting the right (left) BG voltage $V_{BR}(V_{BL})$ equal to the TG voltage $V_{TOP}$. The middle BG voltage $V_{BM}$ was fixed at $V_{BM}=0.818$ V. Under these conditions Coulomb diamonds were recorded and the charging energy of the left (right) dot, was determined to be $E_C=5$ meV (~2.5 meV) at $V_{TOP}=1.6$ V. Therefore, the total capacitance of the left (right) dot was $C_{\Sigma , left(right)}=e^2/E_C=30$ aF (~60 aF) at $V_{BL}=0.76$ V ($V_{BR}=0.76$ V). For comparison, these parameters, were modeled using FASTCAP which calculates capacitances based on a finite element approach. Using the lithographic device dimensions as input, we obtained a total capacitance $C_S=30$ aF for both dots, in good agreement with the experimental value for the left dot but at variance with that of the right dot by a factor of two. Such variations in capacitance from dot to dot could result from physical asymmetries in real devices, as evidenced by the XTEM image in Fig. 1(c), or from the presence of fixed charge in the gate oxide or at interfaces which can modify the effective gate potentials.

We estimate the electron occupancy of a single dot using two methods. The first uses Hall measurements of a similar MOS field-effect transistor (MOSFET) device from which the electron density is determined to be $n=3.5 \times (V_{TOP}-V_{TH})10^{12}$ cm$^{-2}$, where $V_{TH}$ is the threshold voltage. When operated as a simple MOSFET, our device showed $V_{TH} \approx 1.25$ V. Hence, at $V_{TOP}=1.6$ V we estimate the 2DEG density of our device to be $n=1.2 \times 10^{12}$ cm$^{-2}$, resulting in a dot occupancy of $N \approx 20$ electrons for a 30 $\times$ 50 nm$^2$ dot size. The second method estimates electron occupancy by counting Coulomb oscillations from $V_{TH}$, assuming no free electrons in the dots below $V_{TH}$. This method derives a dot occupancy of $N=15$, in reasonable agreement with the previous method.

Figure 2 shows the differential conductance $dI/dV_{sd}$ of the DQD as a function of the BG voltages $V_{BL}$ and $V_{BR}$, for a fixed TG voltage $V_{TOP}=1.6$ V and source drain voltage $V_{SD}=0$ V for two different middle BG voltages $V_{BM}$. In Fig. 2(a), the relatively low middle BG voltage $V_{BM}=0.814$ V and therefore high central barrier separates the two dots, resulting in the characteristic honeycomb-shaped charge stability diagram. By calculating the voltage ratios $\Delta V_{BM}/\Delta V_{BR}(\Delta V_{MB}/\Delta V_{BL})$, we can estimate the ratios of the mutual capacitance to the total dot capacitance $C_m/C_{\Sigma , left(right)} \approx 0.10(0.07)$, indicating that the DQD is in the weak coupling regime.2 There, we observe characteristic triple points resulting from the alignment of the electrochemical potentials of the dots and the leads. In addition, current is observed along the sides of the hexagons, which can occur when the dots are strongly coupled to the leads and second-order cotunneling processes occur.20 Increasing the middle BG voltage to $V_{BM}=0.838$ V, the mutual capacitance increases and dominates the system ($C_m/C_{\Sigma , left(right)} ~ 1$). This occurs when the middle barrier is reduced and a single (merged) large dot is formed, resulting in diagonal parallel Coulomb lines, as observed in Fig. 2(b).

Figure 3(a) shows transport data through the DQD in the weak coupling regime $V_{BM}=0.802$ V, $V_{TOP}=1.4$ V and $V_{SD}=-1.0$ mV. For $|V_{SD}|>0$ the triple points evolve into bias triangles, reflecting the occurrence of transport within the bias windows.2 In a DQD system, two types of coupling can be distinguished: capacitive coupling and tunnel coupling. While capacitive coupling is a purely classical effect,
tunnel coupling arises from the overlap of electron wave functions, classified by the fractional splitting ratio \( F = 2\Delta V / \Delta V_p \), where \( \Delta V \) is the splitting between the paired triangles and \( \Delta V_p \) is the diagonal separation between triangle pairs in Fig. 3(a).\(^{21,22}\) Here, we find \( F \approx 0.2 \), indicating that the two dots is dominated by capacitive coupling, and may therefore be modeled using a capacitive approach.

From the dimensions of the hexagon and triangles in Fig. 3(a) we obtain the capacitances defining the system,\(^2\) namely: the total capacitances of the left and right dots, \( C_{\text{L}} \); the mutual capacitance between the two dots \( C_m \); the relative capacitances between each side BG and its immediate neighboring dot \( C_{\text{BL} (\text{BR})} \); the cross capacitance between each side BG and the next neighboring dot \( C_{\text{BLL} (\text{BR})} \); the mutual capacitance between the two dots \( C_{\text{m}} \); the cross capacitance between each side BG and its immediate neighboring dot \( C_{\text{BL} (\text{BR})} \); and the cross capacitance between each side BG and the next neighboring dot \( C_{\text{BLL} (\text{BR})} \). These results agree well with FASTCAP modeling (see Table I). With the capacitances defined, we obtain the interaction energy between the two dots, using the current structure enabled the formation of two nearly identical dots by appropriate tuning of the BG voltages, our group is developing a three-layer structure, where TGs control the islands, a second layer of gates provides contacts to source and drain, and a third layer provides the BGs. This structure allows the electron reservoirs to remain populated even for low occupations in the dots.

Figures 3(b) and 3(c) show fine scans of bias triangles at \( V_{\text{SD}} = 1.0 \) mV and 0.5 mV, respectively. Resonant tunneling through the ground state (GS) and excited states (ES) of the DQD is clearly observed in the spectroscopy data. With increasing \( V_{\text{SD}} \), the triangular conducting regions become larger allowing more discrete levels in the bias window and the overlap of the triangle pairs increases. Figure 3(d) shows a plot of \( I_{\text{SD}} \) as a function of detuning energy, \( \epsilon \) (Ref. 23) between levels of the DQD. This \( I_{\text{SD}} \) line trace is extracted from a cut of the bias triangle, as shown in Fig. 3(b), where the GS and ES resonances are indicated by the labels a–d. The energy splitting of the first ES b to its GS a is \( \approx 300 \) μeV. We roughly estimate the average energy-level spacing of a dot via Weyl’s formula \( \Delta E = 2\pi \hbar^2 g/m^*A \), where \( A \) is the area of the dot. For a 2DEG system in Si, the effective mass of the electrons \( m^* = 0.19m_e \) and the degeneracy \( g = 4 \), taking into account the spin and valley degeneracies.

We then calculate \( \Delta E \approx 400 \) μeV: the expected average level spacing if all symmetries are broken. Since no field is applied to the dots, the spacing would be a factor of 2 larger or \( \approx 800 \) μeV. In Fig. 3(d), we monitor transport through a serial configuration of two dots along the line cut presented in Fig. 3(b). In this case, we move the energy levels in both dots in opposite directions with respect to each other resulting in an effective factor of two reductions in the expected level splitting, in good agreement with the experimental data.

In conclusion, we have presented a tunable double-gated DQD defined in intrinsic Si. The fabrication of the device is reproducible and MOS-compatible, enabling integration into more complex designs. Device capacitances extracted from the transport measurements were in good agreement with FASTCAP modeling. Detailed bias spectroscopy of the DQD presented evidence of resonant tunneling through GS and ES, indicating that the system was in the few-electron regime. To reduce the electron number to a single electron in each dot we propose the incorporation of additional plunger gates, independently controlling each dot, together with an integrated charge detector\(^6\) to monitor the dot occupations. Such Si-based DQD structures would have excellent potential for the investigation of the the spin-based qubits in Si.

The authors thank D. Barber and R.P. Starrett, and E. Gauja for technical support, C.C. Escott, K.W. Chan, and H. Yang for the help with the FASTCAP modeling, and M.A. Eriksson, F.A. Zwanenburg, and L.D. Macks for helpful comments with the manuscript. This work was supported by the Australian Research Council, the Australian Government, and by the U.S. National Security Agency and U.S. Army Research Office (under Contract No. W911NF-04-1-0290).

\(^23\) Using formula \( \alpha_{\text{left}} \approx \alpha_{\text{right}} \approx 0.17(\alpha_p = 0.19) \), where \( \alpha_{\text{left}} \) and \( \alpha_{\text{right}} \) are defined in Fig. 3(b).